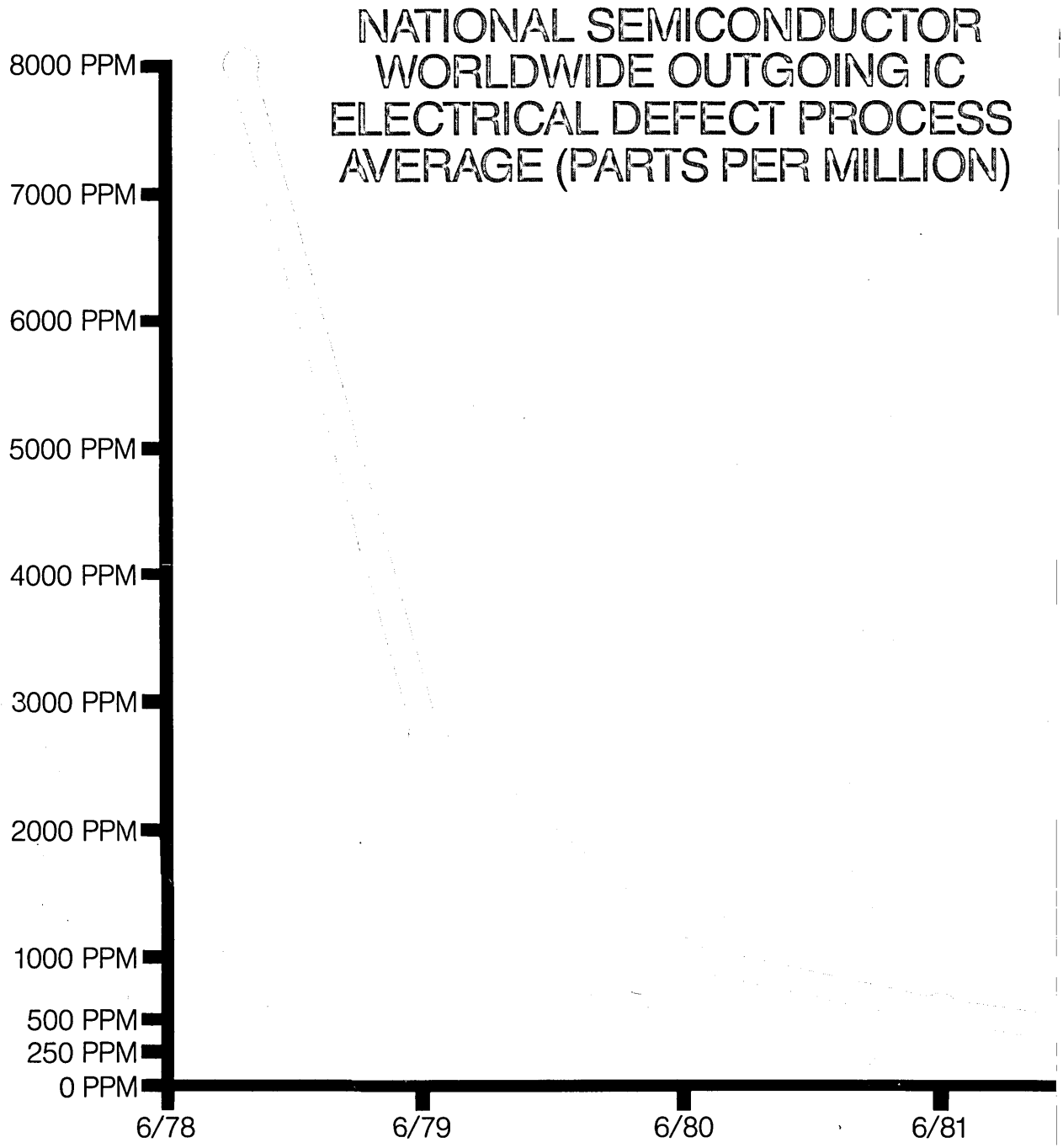
IC MASTER

VOL. II

1983

Engineering design begins with the IC MASTER

$95.00


NATIONAL SEMICONDUCTOR
WORLDWIDE OUTGOING IC
ELECTRICAL DEFECT PROCESS
AVERAGE (PARTS PER MILLION)
8000 PPM
7000 PPM
6000 PPM
5000 PPM
4000 PPM
3000 PPM
2000 PPM
1000 PPM
500 PPM
250 PPM
0 PPM
6/78
6/79
6/80
6/81

IN 1980, WE REJECTED ACCEPTABLE QUALITY LEVELS OTHERS STILL ACCEPT TODAY.

AUGUST 1982
189 PPM

6/82

At National Semiconductor, we take rejection very personally.

That's why we moved so dramatically towards zero defects during the last four years.

All the way from 8,000 parts-per-million in September, 1978 to a remarkably low 189 parts-per-million in August, 1982. A truly astounding 4,100% improvement.

We've made a corporate commitment to achieve the highest product quality in the industry. And that means all our people, from top management to the loading dock, consider quality the highest priority for all our products.

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We won't settle for less.

No matter what others are willing to settle for.

Making CMOS do more.

National Semiconductor

GET HIGH TECHNOLOGY WITHOUT HIGH ANXIETY.

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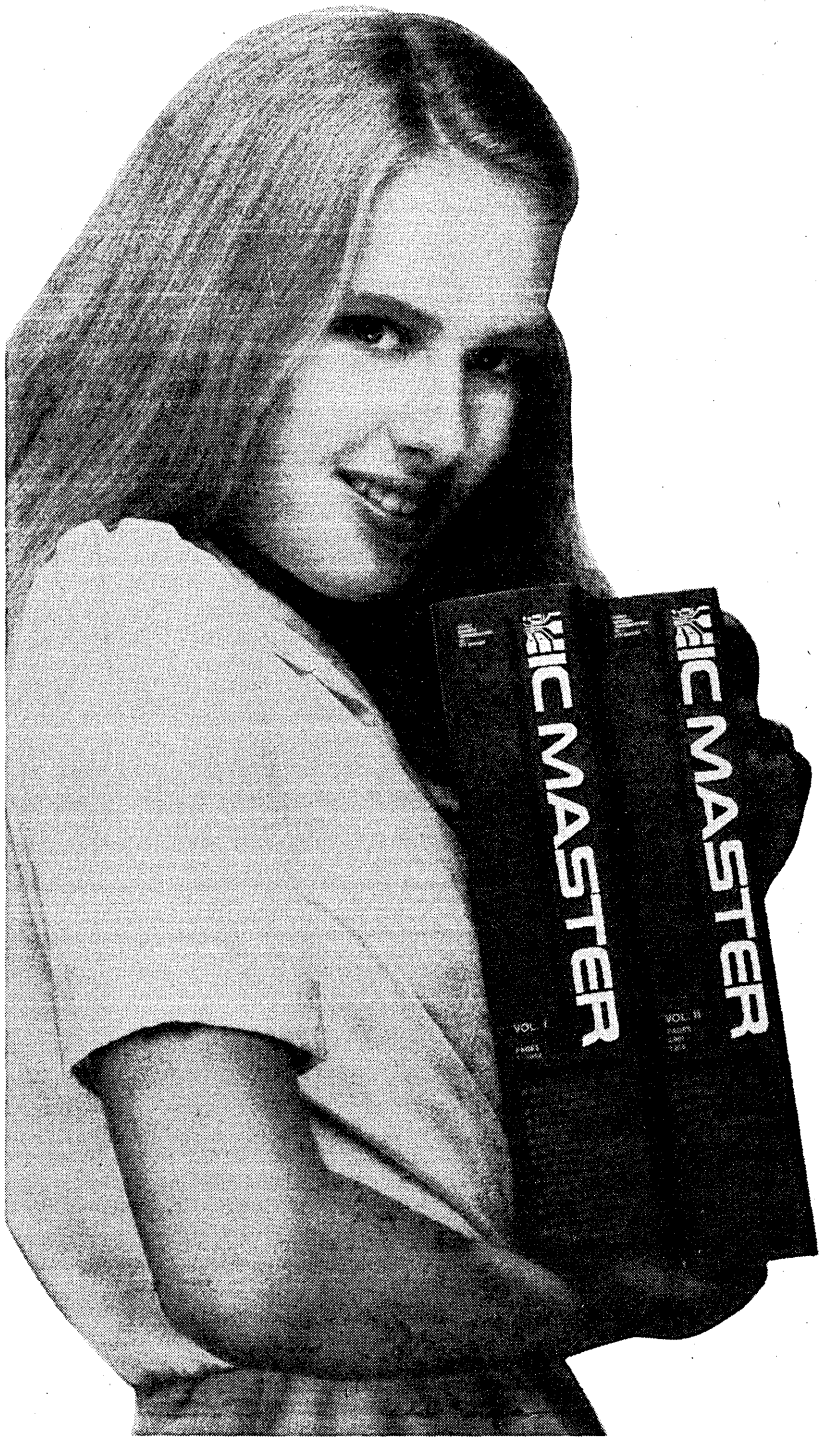
SCHWEBER ELECTRONICS

1983

IC MASTER

VOLUME II



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1983

IC MASTER

VOLUME II

Engineering design begins with the IC MASTER

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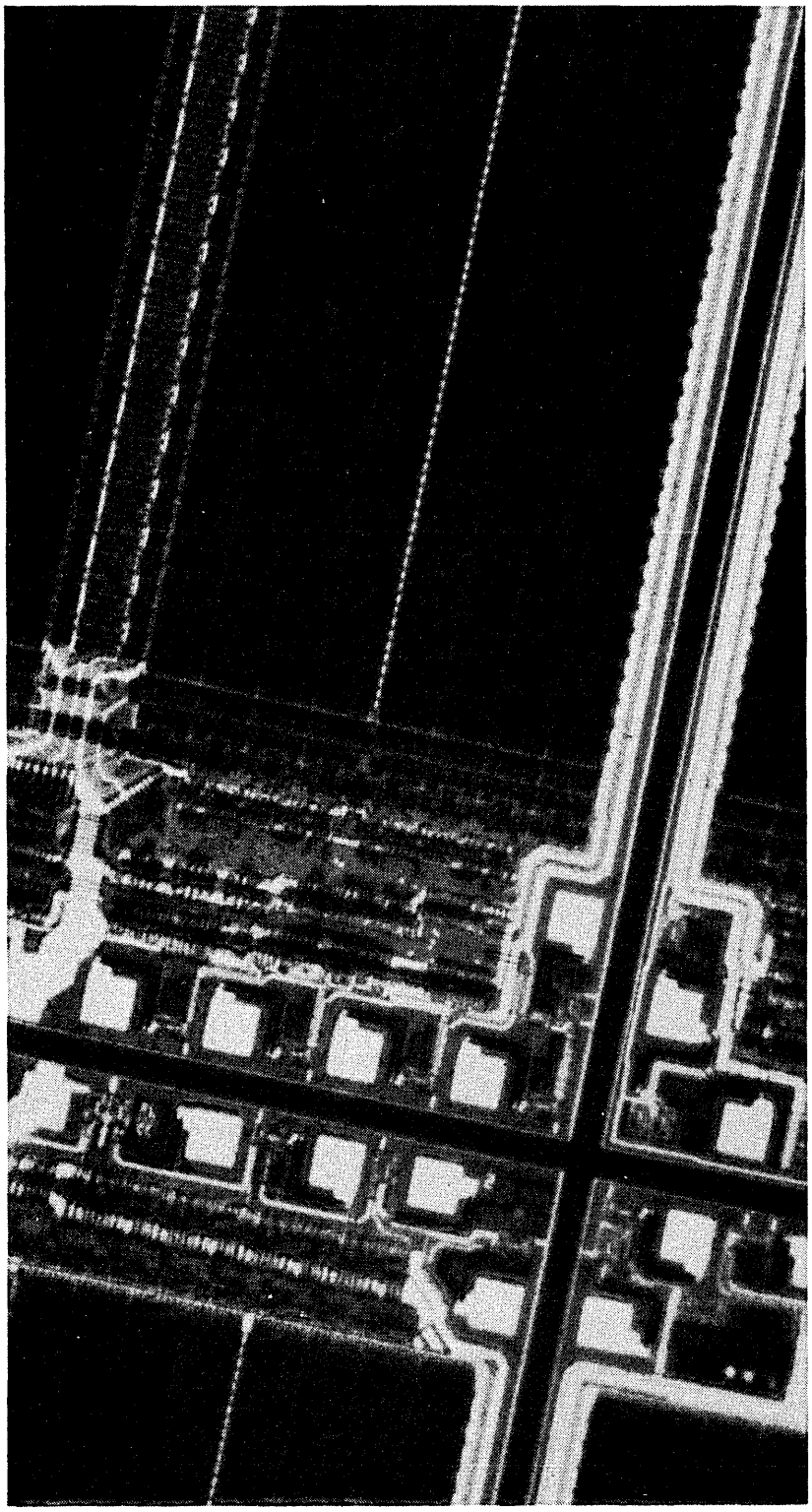


CMOS Static RAM (Integrated Device Technology Photo)

IMPORTANT FEATURES OF YOUR IC MASTER

ONE COMPLETE SOURCE

IC MASTER is the original and only complete guide to currently available integrated circuits, microcomputer boards, development systems, PROM programmers, gate arrays, and other related components of concern to the design engineer. It has become the first place to look in the critical selection of ICs, boards, systems, and equipment. If only one device can fit the requirements of a new design or if hundreds are available, you can find out in seconds by using the IC MASTER.

EASY TO USE

The IC MASTER saves you time. No longer do you have to spend long, tedious hours and days searching through manufacturers' catalogs and data sheets for information. The MASTER gives you—at your fingertips—an easy way to narrow your IC choices quickly, accurately, and systematically with the knowledge that you have just surveyed the entire industry.

PART NUMBER INDEX

This revolutionary index lists all device types made by over 225 manufacturers in numerical sequence excluding prefixes or suffixes. You can find a device number even though you do not know either the full part number or even the manufacturer. Once a basic device number is located in the index, you can obtain instant identification of all manufacturers making a device by that number, regardless of function, and determine the full part number designation. All page references to data sheet material and any existing application note abstracts are also provided. The Part Number Index should not be used as an alternate source directory because two manufacturers may use the same part number, by coincidence, for totally different devices.

PART NUMBER GUIDE

The information in this guide allows you to break down each company's part numbering system into product temperature ranges, packaging variations, and functions. It is an invaluable tool for the elimination of costly and time-consuming ordering errors caused by lack of standardization from manufacturer to manufacturer in part numbering systems.

APPLICATION NOTE DIRECTORY

Application note descriptions are arranged alphabetically by function and application category. Each note's description identifies the specific device or devices featured, provides a 25 to 30 word abstract, and identifies both the manufacturer that originated the note and the specific application note number. This section provides all the information necessary for you to update your application note files speedily, or thoroughly research the existence of application note material for a specific design problem.

MILITARY PARTS DIRECTORY

Cross reference chart identifies all IC devices having received JAN qualification. This chart includes a cross reference listing of device numbers and corresponding military standard 38510 slash numbers and vice versa.

MILITARY DEVICE TESTING TABLE

This table identifies IC manufacturers who test to military standard 38510 and the screening to military standard 883 that they provide.

MILITARY PARTS INDEX

This guide to JAN qualifed parts makes it possible to search devices by function, and to determine if a JAN qualified part exists for a particular functional need.

ADVERTISERS' PRODUCT INDEX

This index directs the reader to detailed product information for the parts whose manufacturers have included data sheets in IC MASTER. When you are looking for data on a particular manufacturer's products, this index provides the fastest way to find the information you seek.

ALTERNATE SOURCE DIRECTORY

The most comprehensive industry-wide, pin-for-pin, functional equivalent Alternate Source Directory ever compiled. This directory is updated by asking all IC manufacturers to identify each competitive device for which they make a pin-for-pin substitute.

MASTER SELECTION GUIDE

Each guide is organized by specifications and categories to direct the reader easily and quickly to the device most likely to fill the requirements of a particular application. Once the reader finds those devices that are closest to his needs, he sees available sources, and is directed to additional data if provided by advertisers.

MANUFACTURERS AND DISTRIBUTORS DIRECTORY

Locations and phone numbers are given for manufacturers' field sales offices, representatives, and distributors, both domestic and international.

Typical Problems Solved by IC MASTER

- **Find All Products That Meet Desired Specifications**
- **Obtain Data For A Particular Device • Decode Part Numbers**
- **Determine Alternate Sources • Plus Much More**

An engineer can use IC MASTER to solve a wide variety of problems. Answers provided to engineers by IC MASTER can range from finding the device that best meets a particular set of specifications to helping to determine which family of devices should be used in building a system.

Some of the typical problems that IC MASTER can solve are illustrated in the following examples:

Who makes a TTL 4-bit binary full-adder with look-ahead carry?

All functions are listed, in alphabetical order, in the Master Selection Guide Index. In this case, the engineer looks under adders; in the column adjacent to adders, he sees that all types of adders are listed. The particular adder being sought is covered in the Digital section of IC MASTER.

Now that the engineer knows that the devices he seeks are catalogued in the Digital section, he can turn to the Digital Master Selection Guide and see the page number where information on these devices can be obtained.

When he turns to this page, he will notice that certain device numbers and manufacturers are printed in bold face type while others appear in regular type face. Bold face type is used whenever a part's manufacturer has provided a data sheet for the device in IC MASTER. The page number assigned to the data sheet also appears in bold face type so that the engineer can turn to it directly.

Who Makes a High-Speed 12-Bit, Analog-to-Digital Converter With Guaranteed ± ½ LSB Linearity and 13-μsec or Faster Conversion Time?

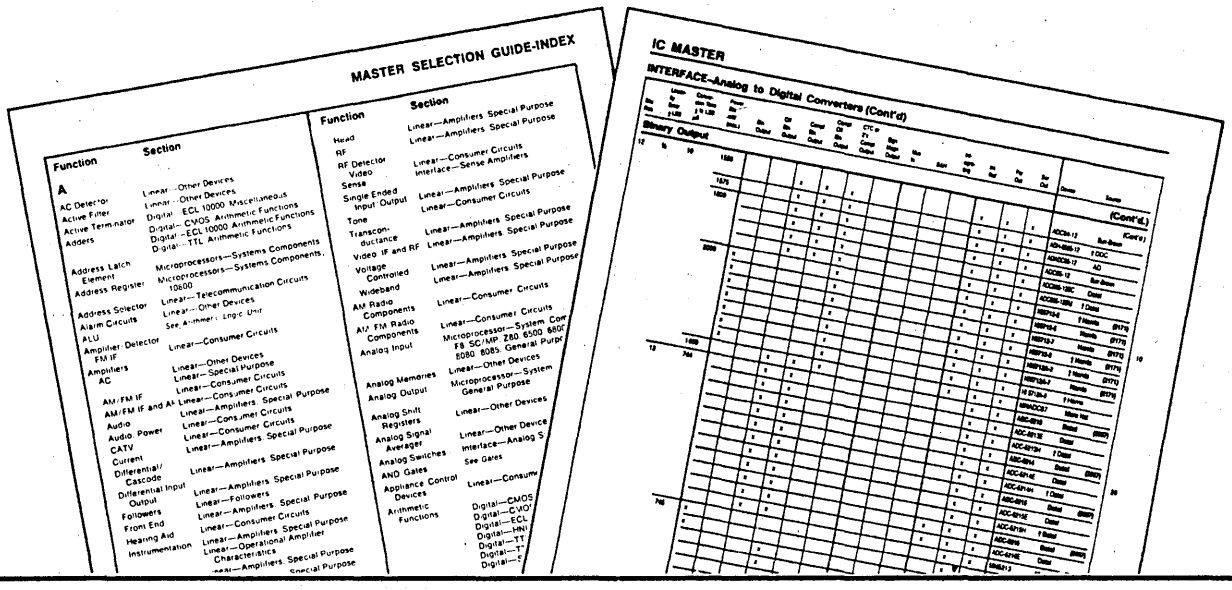
Many manufacturers make devices that meet these specifications including Analog Devices, Burr-Brown, Datel-Intersil, Data Device Corp., Harris, Hybrid Systems, Micro Networks, and Teledyne Philbrick.

The Master Selection Guide for Interface makes it possible for an engineer to find every device that meets the above specifications, regardless of who makes it, in seconds.

The Interface section is organized by product classification; an engineer can turn immediately to the category of interest such as analog switches with drivers, multiplexers, a/d converters with binary output a/d converters with decimal output, d/a converters, display drivers, error checking circuits, keyboard encoder-decoders, line drivers, line transceivers, memory and peripheral drivers, sense amplifiers, etc.

To find every 12-bit analog-to-digital converter with guaranteed ± ½ LSB linearity and 13-μsec or faster conversion time, all an engineer has to do is turn directly to the analog-to-digital converter section of the Interface Master Selection Guide.

In this section, devices are organized by key parameters. Under resolution, the engineer finds 12-bit; next he looks under linearity error for ± ½ LSB and then he looks under conversion time for devices with 13-μsec or faster specifications.



Ways to Use IC Master

What application notes are available on emulating logic functions with PROMs?

IC MASTER provides the most complete listing of application notes available in print. It is easy to find the right application notes by looking in IC MASTER because the application note directory is organized by function.

There are two ways to look up an application note. An engineer can turn to the index page and find the appropriate function or category such as instrumentation amplifiers, multiplexers, or PROMs.

If he knows the device number, he can look it up in the part number index at the front of IC MASTER and see all of the application notes concerning that device. For example, under 8275, a programmable CRT controller listed in the part number index, the reader is referred to the listing for an Intel application note entitled "CRT Terminal Design Using the 8275 and 8279."

To find an application note concerning the use of PROMs to emulate logic functions, the engineer can turn to the application note section on PROMs and see what notes can be of help.

Each listing in the application note directory provides a detailed descriptive passage for the note, gives its length and identifies the manufacturer who publishes it.

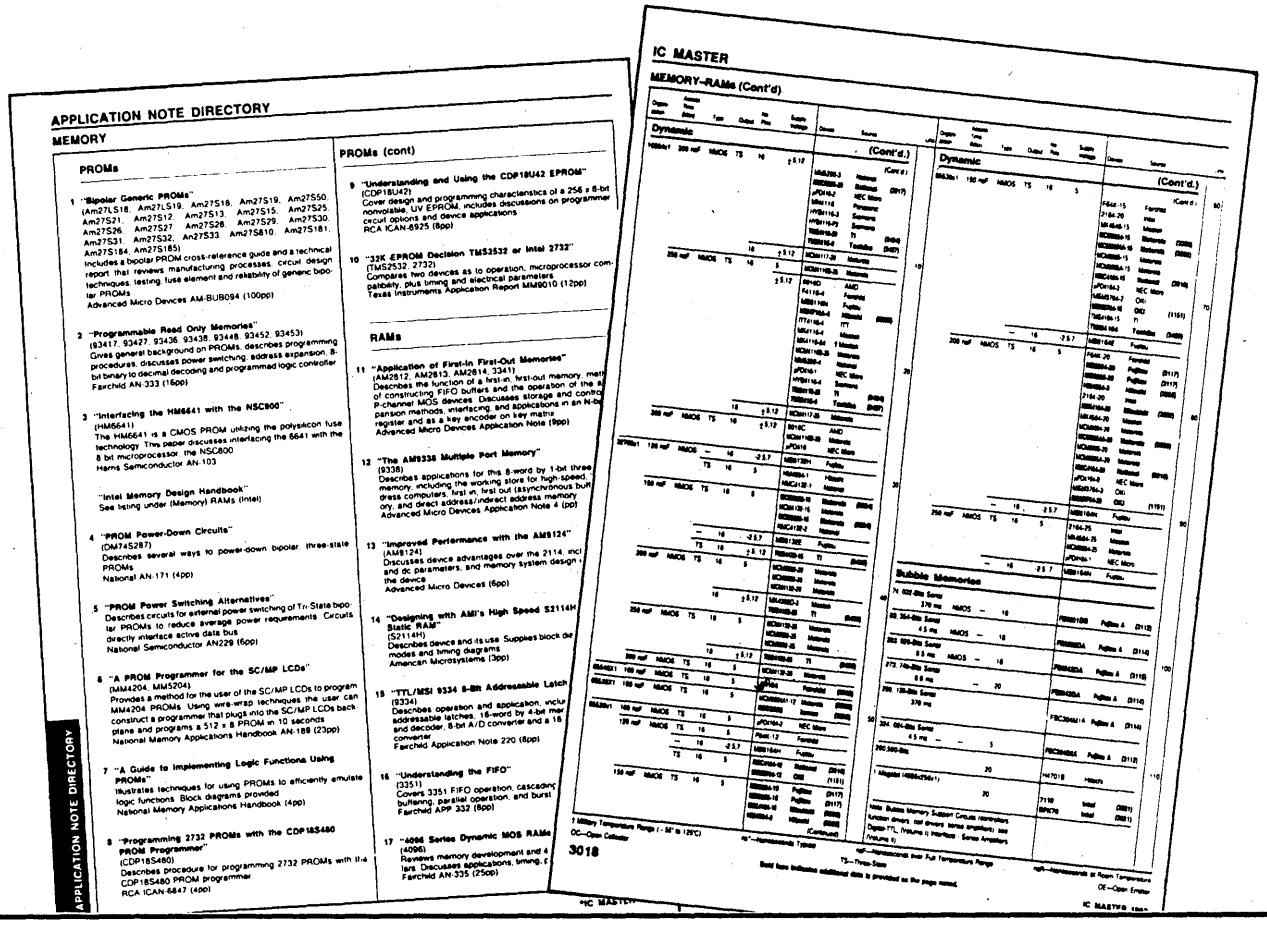
Who makes a 64K dynamic RAM with an access time of 120 ns or faster?

The Memory Section in IC MASTER has a Master Selection Guide which provides initial selection information and data on PROMs, RAMs, ROMs and other types of memories. Each device is characterized by organization (words and bit/word) and access time.

For example, if an engineer was looking for a 64K dynamic RAM, his first step would be to determine organization (words and bit/word). Next, he would locate the desired access time.

When devices are available made by various processes such as NMOS, CMOS, ECL, TTL, etc., the engineer can choose the device that best suits his needs. For further definition, output type, supply voltage and number of pins are listed along with the manufacturer's part number and name.

The engineer's next step in his memory selection process would be to study the applicable data for 64K dynamic RAMs provided by IC manufacturers and pick the most appropriate device. Literally hundreds of pages of engineering data on memories appear in IC MASTER.



Ways to Use IC Master

I need to choose between a full custom or a semi-custom/gate array solution to my design problem.

To help designers weigh custom solutions against semi-custom/gate array approaches, IC MASTER provides a Master Selection Guide on Custom/Semi-Custom and a special section entitled "Options for Going Custom." In this section, the advantages and disadvantages of various custom/semi-custom techniques are covered.

The capabilities of IC manufacturers are tabulated for easy comparison; additional information such as available design aids and testing services is also provided.

My application requires microcomputer boards. How do I start?

Single and multiple board microcomputers are arranged by manufacturer. Under each manufacturer, boards are grouped in sequence according to data word size and, within that grouping, according to the microprocessor on which they are based. Hardware and software support are listed for each board.

A supplementary selection guide is included for microcomputer support boards. The boards are grouped according to supported computer systems.

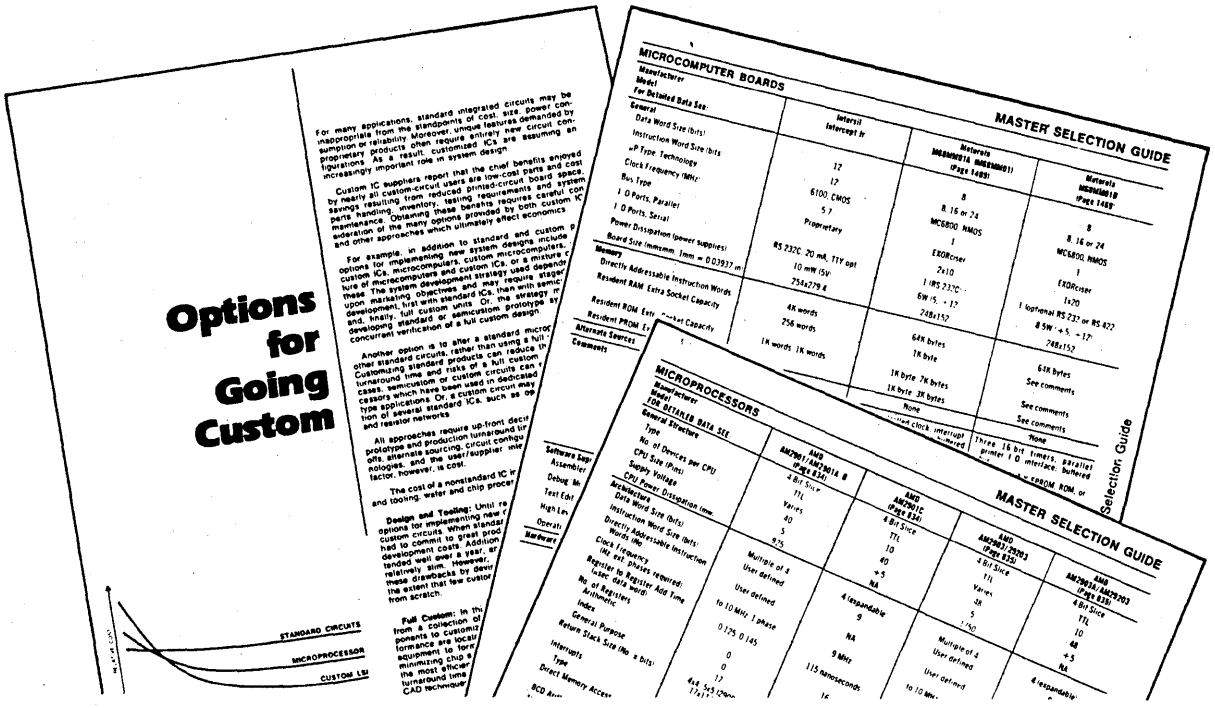
With so many mircoprocessors available, where do I begin?

Simply turn to the Master Selection Guide for Microprocessors. There you will find a listing of all microprocessors currently available and key parameters allowing you to narrow down your selection to a range of products that will meet your major requirements.

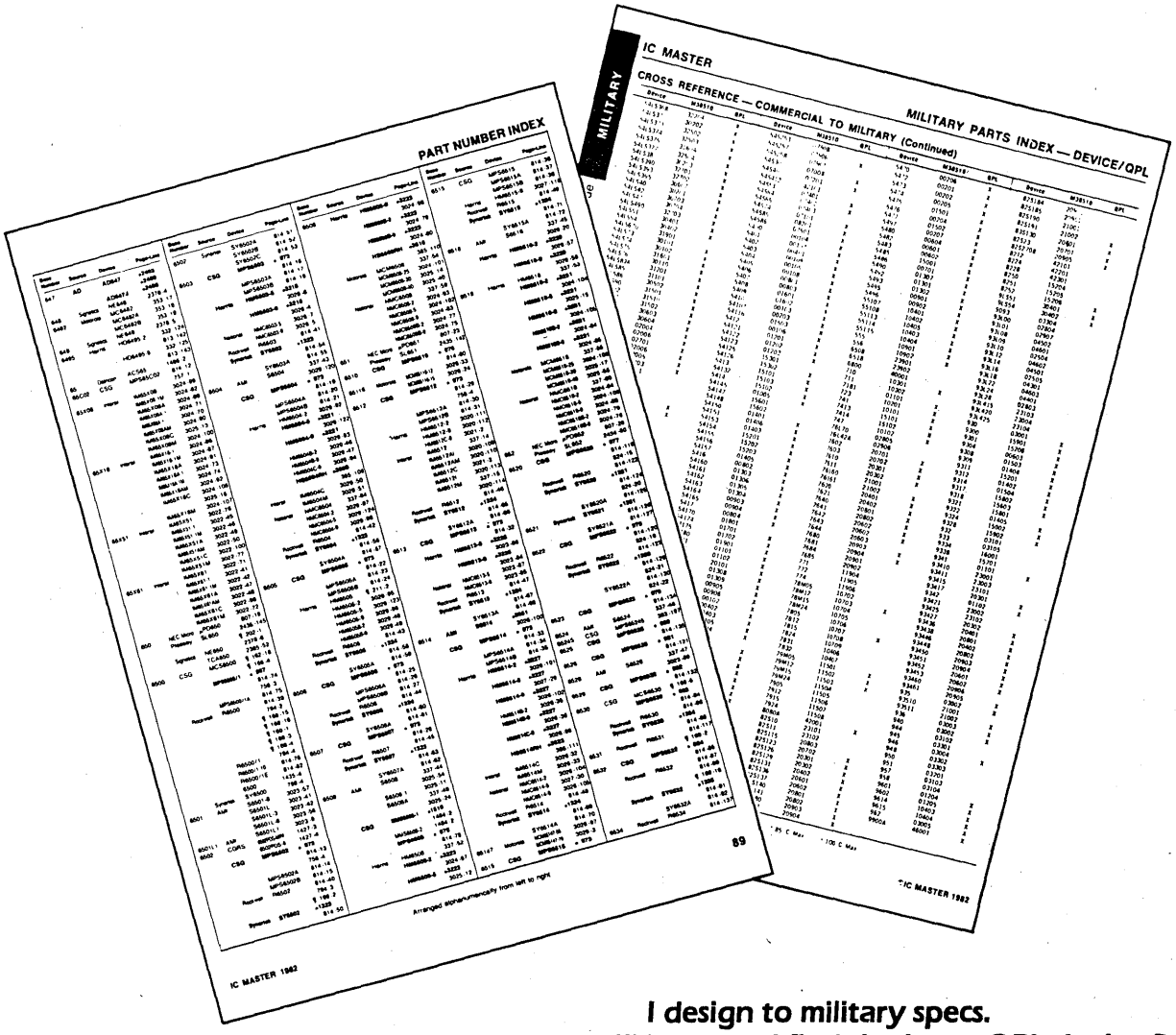
Once the microprocessor that best fits the application has been chosen, the next step is to go to the "system components" section. Here all of the available peripheral devices that work with each microprocessor are arranged by function. Thus, if the microprocessor that has been selected is the 8048, system components specifically developed for use with the 8048 are listed, organized by function.

A "general purpose" section follows the "system components" section and describes devices that can be used with more than one microprocessor family.

Finally, hundreds of pages of the latest microprocessor data sheets, provided by IC manufacturers, are presented, arranged in alphabetical order by manufacturer. Each data sheet is easily found thanks to boldfaced page-number references in the Master Selection Guide.



Ways to Use IC Master



If an engineer knows that the basic part number is 6508, where does he look first?

The place to look is the part number index. Here, all of the prefixes and suffixes have been stripped away to leave only the basic number. This makes it possible to see the manufacturer of every part with the same base number at a glance. Parts with the same base number, it should be kept in mind, are not necessarily identical; in fact, one could be a memory while another might be a linear device. (To find replacements, one should look in the alternate source directory, not in the part number index.)

Under 6508, the engineer would see a number of devices listed and the page and line numbers where data is given for each of the devices. If an application note concerning any of the devices is available, the location of its listing is also shown.

I design to military specs. Where can I find the latest QPL devices?

The IC MASTER includes a comprehensive military parts directory. Within this directory, tables and charts are provided to answer virtually every information need of the engineer involved in military or high-reliability equipment design.

All integrated circuits with JAN qualification are listed in IC MASTER. A cross reference table, relating device numbers to mil spec numbers, is arranged according to device number. A second table, arranged by M-38510 number, makes it possible to look up the part number when the mil spec number is known.

In addition, ICs are also organized by product section and function, which allows the user to find the proper IC without having to know either the commercial or the military part number.

This section of IC MASTER also includes a table showing the capability of manufacturers to perform MIL-STD-883 screening and high-reliability testing.

ADVERTISERS INDEX

INTRODUCTION TO INTERFACE

The Master Selection Guide provides sufficient information for making initial product selections. All devices that appear in this section, both in the initial selection guide and the data pages, are included in all indexes. These index listings lead to the page and line on that page where each device appears.

In the Interface Section the selection parameters differ drastically for each category; therefore each has its own format. The analog to digital converter category has two formats: one for binary output devices and another for decimal units. Some of the products in this section, primarily analog to digital and digital to analog converters, may be hybrids; the hybrids listed are only those packaged to be compatible with ICs.

This section is not complicated by reference to package styles; the package style suffixes are usually deleted. For more information on each companies' suffixes, see the Part Number Guide. Throughout the Master Selection Guide, each full military temperature range (−55°C to 125°C) device is indicated by a (†) before the manufacturer's name. Manufacturers' names are normally spelled out; however, a few are abbreviated and the abbreviations are explained on page 2612.

CATEGORY

Detailed Product Information provided by:

The manufacturers listed above have provided detailed information on their latest and most significant products.

EINFÜHRUNG INTERFACE-SCHALTUNGEN

Der Master Selection Guide für Interfaceschaltungen enhält alle Informationen, die Sie für die Erstauswahl Ihres Produkts benötigen. Die Bauteile, die in diesem Abschnitt erscheinen, sowohl im Selection Guide als auch auf den Datenblättern, sind in allen Master Indexes enthalten. Diese Register verweisen auf die Seite und Zeile, auf der das entsprechende Bauelement vorkommt.

Im Interface-Teil unterscheiden sich die Auswahl-Parameter drastisch für jede Kategorie; daher hat jede ihre eigene Tabelle. Für Analog-Digital-Wandler gibt es zwei Tabellen: eine für Bauteile mit Binär-Ausgang und eine weitere für Dezimal-Bauteile. Einige Produkte in diesem Teil, hauptsächlich Analog-Digital und Digital-Analog Wandler, können hybride Bauelemente sein. Es werden nur solche hybriden Bauteile aufgeführt, deren Gehäuse kompatibel zu ICs sind.

Dieser Abschnitt wird nicht durch Hinweise auf Gehäuseformen kompliziert. Die entsprechenden Suffixe sind meistens weggelassen. Weitere Information über die Suffixe jedes Herstellers erhalten Sie über das Numerische Typenverzeichnis. Im ganzen Master Selection Guide sind alle Bauteile mit militärischem Temperaturbereich (—55°C bis 125°C) durch ein Kreuz (†) vor dem Namen des Herstellers gekennzeichnet. Die Namen der Hersteller sind normalerweise ausgeschreiben; einge jedoch sind abgekürzt. Die Abkürzungen werden auf S. 2612 erklärt.

INTRODUCTION AUX INTERFACES

Le Guide Général de Sélection fournit suffisamment de renseignements pour permettre des sélections initiales de produits. Tous les appareils cités dans cette Section, à la fois dans la Premier Guide de Sélection et dans les feuilles de données, sont inclus dans tous les index. Ces index indiquent à quelle page et à quelle ligne sur cette page il a été fait mention de tel appareil.

Dans la Section "Interfaces", les paramètres de sélection changent pour chaque categorie, ce qui implique un format spécial pour chacun. Les convertisseurs analogues et digitaux ont deux formats : un pour les appareils à sortie binaire et un autre pour les unités décimales. Certains produits de cette Section, notamment les convertisseurs d'analogue à digital et de digital à analogue, peuvent être des hybrides. Les hybrides énumerés sont ceux qui possédent un boitier compatible aux circuits intégrés.

Cette Section ne fait pas référence aux types de boitier; les suffixes indiquant le type de boitier sont généralement omis. Pour plus d'information sur les suffixes employés par chaque société, reportez-vous au Guide des Numéros de Pièces. Dans tout le Guide Général de Sélection chaque appareil avec sélection complète de températures imposées par l'Armée (—55°C à 125°C) est indiqué par le signe (†), juste avant le nom du fabricant, Les noms des fabricants sont généralement écrits en entier, certains cependant sont abrégés. Reportez-vous à la page 2612 pour connaître la signification de ces abréviations.

INTRODUCCIÓN A ZONA INTERFACIAL

La Guía Maestra de Selección provee suficiente información para hacer selecciones iniciales de producto. Todas las componentes que aparecen en esta sección, ya sea en la guía de selección inicial o en las páginas de datos, están incluídas entodos los ostros índices. Estas listas de índices los conduce a la página y linea de aquella página donde se encuentra cada componente.

En la sección de Zona Interfacial la selección de parámetros difiere drásticamente para cada categoría; de tal manera que cada una tiene su propio formato. La categoría de convertidores analógicos a digitales tiene dos formatos: uno para componentes de salida binaria y otro para unidades decimales. Algunos de los productos en esta sección, principalmente convertidores analógico a digital y digital a analógico, pueden ser híbridos; los híbridos en la lista son solo aquellos de estilo constructivo compatible con CI*.

Esta sección no es complicada por referencias al estilo constructivo; los sufijos que denotan estilo constructivo han sido generalmente omitidos. Para información adicional sobre sufijos de las compañías, refiérase a la Guía de Número de Pieza. A lo largo de la Guía de Selección Maestra, cada intérvalo completo de temperatura para uso militar (55°C a 125°C) de la componente aparece indicada por el signo (†) que precede al nombre del fabricante. Los nombres de los fabricantes no son generalmente deletreados; sin embargo, algunos aparecen abreviados y las abrieviaturas son explicadas en la página 2612.

インターフェイスへの案内

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INTERFACE–Analog Switches

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range V	Supply Voltage, V	Device	Source	Line
Switches with Drivers							
SPST	CMOS	50	±11	±15,5	IH5140M	† Intersil	
			±15,5	±15,5	**DG5040A**	**† Siliconix (2779,2813)**	
					DG5040C	**Siliconix (2779,2813)**	
		75	±10	±15,5	IH5140C	Intersil	
			±11	±15,5	**HI5040-2**	**† Harris (2643,3288)**	
					HI5040-5	**Harris (2643,3288)**	
					IH5040M	† Intersil	
		80	±10	±15,5	IH5040C	Intersil	
	JFET	6	−5 to 10	±15	CAG6	† Teledyne C	
			−5 to 4	±15,5	CAG10A	† Teledyne C	10
		10	−5 to 10	±15	CAG6-10	† Teledyne C	
			−5 to 4	±15,5	CAG10C	† Teledyne C	
		15	−10 to 5	±15,5	CAG10D	† Teledyne C	
		30	±5	±5,5	CAG10	† Teledyne C	
			±8	−18,12	IH5001	Intersil	
		50	−10 to 4	±15,5	CAG10B	† Teledyne C	
			−10 to 5	−15,5	CAG14	† Teledyne C	
			±8	−18,12	IH5002	Intersil	
			±10	±15	2110BE	† Teledyne C	
		60	±10	±18,5	CAG30	† Teledyne C	20
		100	±5	±15	2107BE	† Teledyne C	
	PMOS	80-300	±10	−20,10	TL610I	TI	
					TL610M	† TI	
		100-400	±10	−20,10	TL610C	TI	
2xSPST	CMOS	35	±10	±15,5	IH5048M	† Intersil	
		45	±10	±15,5	IH5048C	Intersil	
		50	±7.5	±15.5	DGM181B	Intersil	
			±10	±15.5	DGM182A	† Intersil	
			±11	±15,5	IH5141M	† Intersil	
			±15	±15	**HI300**	**Harris (2630,3287)**	30
					HI304	**Harris (2630,3287)**	
					HI381	**Harris (2635,3288)**	
					HI400	Harris	
					DG300A	**† Siliconix (2779)**	
					DG300AA	**† Siliconix (2779)**	
					DG300AB	**Siliconix (2779)**	
					DG300AC	**Siliconix (2779)**	
					DG300B	**Siliconix (2779)**	
					DG300C	**Siliconix (2779)**	
					DG304A	**† Siliconix (2779)**	40
					DG304AA	**† Siliconix (2779)**	
					DG304AB	**Siliconix (2779)**	
					DG304AC	**Siliconix (2779)**	
					DG304B	**Siliconix (2779)**	
					DG304C	**Siliconix (2779)**	
					DG381A	**† Siliconix (2779)**	
					DG381AA	**† Siliconix (2779)**	
					DG381AB	**Siliconix (2779)**	
					DG381AC	**Siliconix (2779)**	
					DG381B	**† Siliconix (2779)**	50
					DG381C	**† Siliconix (2779)**	
				±15,5	**HI5048-2**	**† Harris (2643)**	
					HI5048-5	**Harris (2643)**	
					DG5041A	**† Siliconix (2779,2813)**	
					DG5041C	**Siliconix (2779,2813)**	
		70	±14	±15	DG200M	† Intersil	
					IH5200	† Intersil	
						(Continued)	

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range V	Supply Voltage, V	Device	Source	Line
						(Cont'd)	
2xSPST	CMOS	70	±15	±15	**ADG200A**	**† AD (3176)**	
					HI200-2	**† Harris (2624,3287)**	
					MP200DIA	**Micro Pwr (401)**	60
					DG200A	**† Siliconix (2779,2784)**	
					DG200AA	**† Siliconix (2779,2784)**	
		75	±10	±15,5	DGM182B	Intersil	
					IH5141C	Intersil	
			±11	±15,5	DG200	Intersil	
					IH200M	† Intersil	
					IH5041M	† Intersil	
			±15	±15,5	**HI5041-2**	**† Harris (2643)**	
					HI5041-5	**Harris (2643)**	
		80	±10	±15,5	IH200C	Intersil	70
					IH5041C	Intersil	
			±14	±15	DG200C	Intersil	
					IH5200C	Intersil	
			±15	±15	**ADG200B**	**AD (3176)**	
					ADG200C	**AD (3176)**	
					HI200-5	**Harris (2624,3287)**	
					MP200DIB	**Micro Pwr (401)**	
					MP200DIC	**Micro Pwr (401)**	
					DG200AB	**Siliconix (2779,2784)**	
					DG200AC	**Siliconix (2779,2784)**	80
					DG200B	**Siliconix (2779,2784)**	
					DG200C	**Siliconix (2779,2784)**	
		90	±15	±15	**AD7592DIB**	**AD (3176)**	
					AD7592DIK	**AD (3176)**	
	JFET	6	−6 to 10	−18,15	CAG27	† Teledyne C	
		10	−6 to 10	−18,15	CAG27-10	† Teledyne C	
			−7.5 to 15	±15,5	DG180A	† Intersil	
					DG180B	Intersil	
					DG180A	**† Siliconix (2779)**	
					DG180B	**Siliconix (2779)**	90
			±10	−18,12	DG141A	† Intersil	
					IH5005	† Intersil	
					AH0141	**† National (3344)**	
					AH0141C	**National (3344)**	
					DG141A	† Siliconix	
				−20,10,5	DG180A	† Intersil	
					DG180B	Intersil	
					DG180A	† Siliconix	
					DG180B	Siliconix	
		15	±7.5	±15	DG151A	† Intersil	100
					AH0151	**† National (3344)**	
					AH0151C	**National (3344)**	
					DG151A	† Siliconix	
			±8	−18,12	DG141B	Intersil	
					DG441A	Intersil	
					DG141B	Siliconix	
		20	±5.5	±15	DG151B	Intersil	
					DG451A	Intersil	
					DG151B	Siliconix	
		30	−6 to 10	−18,15	CAG24	† Teledyne C	110
			−7.5 to 15	±15,5	DG181A	† Intersil	
					IH181M	† Intersil	
					AM181	† National	
					DG181A	**† Siliconix (2779)**	
			−12.5 to 10				
				−20,10,5	DG181A	† Intersil	
						(Continued)	

DT¹ means four terminals with a pair of normally open and normally closed contacts.

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INTERFACE–Analog Switches (Cont'd)

Switches with Drivers (Cont'd)

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range V	Supply Voltage, V	Device	Source		Line
2xSPST	JFET	30	−12.5 to 10				(Cont'd)	
				−20,10,5	IH181M	† Intersil		
					AM181	† National		
					DG181A	† Siliconix		
			±10	−18,12	DG133A	† Intersil		
					IH5003	† Intersil		
					IH5006	† Intersil		
					AH0133	**† National**	**(3344)**	
					AH0133C	**National**	**(3344)**	
					DG133A	† Siliconix		
				−20	CDA2-3	† Teledyne C		10
		35	±8	−18,12	DG433A	† Intersil		
		50	−7.5 to 15	±15,5	DG181B	Intersil		
					IH181C	Intersil		
					DG181B	**Siliconix**	**(2779)**	
			−10 to 15	±15,5	AM281	National		
			−12.5 to 10					
				−20,10,5	DG181B	Intersil		
					IH181C	Intersil		
					DG181B	Siliconix		
			−15 to 10	−20,10,5	AM281	National		
			±7.5	±15	DG152A	† Intersil		20
					AH0152	**† National**	**(3344)**	
					AH0152C	**National**	**(3344)**	
					DG152A	† Siliconix		
			±8	−18,12	DG133B	Intersil		
					DG133B	Siliconix		
			±10	−18,12	IH5004	Intersil		
				−18,15	CAG13	† Teledyne C		
					CAG42	† Teledyne C		
					CAG45A	† Teledyne C		
		75	−7.5 to 15	±15,5	AM182	† National		30
			−10 to 15	±15,5	DG182A	† Intersil		
					IH182M	† Intersil		
					DG182A	**† Siliconix**	**(2779)**	
			−12.5 to 10					
				−20,10,5	AM182	† National		
			−15 to 10	−20,10,5	DG182A	† Intersil		
					IH182M	† Intersil		
					AM281	National		
					DG182A	† Siliconix		
			±10	±15	TL182M	† TI		
			±15	±10	SW-05B	† PMI		40
					SW-05F	PMI		
		80	±8	−18,12	DG434A	Intersil		
			±10	−18,12	DG134A	† Intersil		
					IH5007	Intersil		
					AH0134	**† National**	**(3344)**	
					AH0134C	**National**	**(3344)**	
					DG134A	† Siliconix		
		100	−10 to 15	±15,5	DG182B	Intersil		
					IH182C	Intersil		
					AM282	National		50
					DG182B	**Siliconix**	**(2779)**	
			−15 to 10	−20,10,5	DG182B	Intersil		
					IH182C	Intersil		
					AM282	National		
					DG182B	Siliconix		
			±5.5	±15	DG452A	Intersil		
					DG152B	Siliconix		
			±8	−18,12	DG134B	Intersil		
					DG134B	Siliconix		
			±10	±15,5	TL182C	TI		60
					TL182I	TI		

(Continued)

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range V	Supply Voltage, V	Device	Source		Line
2xSPST	JFET						(Cont'd)	
		300	−7.5 to 15	±15,5	**DG281A**	**† Siliconix**	**(2779)**	
					DG281B	**Siliconix**	**(2779)**	
	PMOS	50	±15	±15	HI401	Harris		
		75-200	−5 to 10	±15,5	DGM111A	† Siliconix		
			±10	−20,10,5	DGM111A	† Siliconix		
		75-250	−5 to 10	±15,5	DGM111B	Siliconix		
			±10	−20,10,5	DGM111B	Siliconix		
		100-450	±10	−20,10,5	DG111	† Intersil		
					DG112	† Intersil		70
4xSPST Common Output								
	PMOS	100-450	±10	−20,10	DG116	† Intersil		
				−20,10,5	DG118	† Intersil		
		150-450	±10	−20,10,5	DG172A	† Siliconix		
		150-500	±10	−20,10,5	DG172B	Siliconix		
		200-600	±10	−20,10,5	DG172C	Siliconix		
4xSPST Var. Comb. of Normally On/Off, with Disable								
	FET	85	±10	±15	SW03B	† PMI		
					SW03F	PMI		
					SW04B	† PMI		
					SW04F	PMI		
					SW06	PMI		80
4xSPST Various Combinations of Normally On/Off								
	FET	80 *	±10	±15	SW-201B	PMI		
					SW-202B	PMI		
		85	±10	±15	SW01B	† PMI		
					SW01F	PMI		
					SW02B	† PMI		
					SW02F	PMI		
		100	±10	±15	SW-201F	PMI		
					SW-202F	PMI		
	JFET	100	±10	−18,15	CAG48A	† Teledyne C		
		200	±10	±15,0	**LF11201**	**† National**	**(3318)**	90
					LF11202	**† National**	**(3318)**	
					LF11331	**† National**	**(3318)**	
					LF11332	**† National**	**(3318)**	
					LF11333	**† National**	**(3318)**	
		250	±10	±15,0	**LF13201**	**National**	**(3318)**	
					LF13202	**National**	**(3318)**	
					LF13331	**National**	**(3318)**	
					LF13332	**National**	**(3318)**	
					LF13333	**National**	**(3318)**	
	PMOS	200-600	±10	−20,10,5	**AH0015**	**† National**	**(3344)**	100
					AH0015C	**National**	**(3344)**	
4xSPST	CMOS	50	±15	±15	**HI201HS-2**	**† Harris**	**(2626,3287)**	
					HI201HS-5	**Harris**	**(2626,3287)**	
		75	±11	±15,5	IH201M	† Intersil		
					IH202M	† Intersil		
					IH5052M	† Intersil		
					IH5053M	† Intersil		
		80	±10	±15	**MP201DIA**	**† Micro Pwr**	**(401)**	
					MP201DIB	**Micro Pwr**	**(401)**	
				±15,5	IH201C	Intersil		110
					IH202C	Intersil		
					IH5052C	Intersil		
					IH5053C	Intersil		
			±14	±15	DG201M	† Intersil		
					IH5201M	† Intersil		
			±15	±15	**ADG201A**	**† AD**	**(3176)**	
					HI201-2	**† Harris**	**(2626,3287)**	
		90	±15	±15	**AD7590DIB**	**AD**	**(3176)**	
					AD7590DIK	**AD**	**(3176)**	
					AD7591DIB	**AD**	**(3176)**	120
					AD7591DIK	**AD**	**(3176)**	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Analog Switches (Cont'd)

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range V	Supply Voltage, V	Device	Source	Line
Switches with Drivers						**(Cont'd)**	
4xSPST	CMOS	90	±15	±15		(Cont'd)	
					DG221A	**†Siliconix (2794)**	
					DG221C	**Siliconix (2794)**	
		100	±14	±15	DG201C	Intersil	
					IH5201C	Intersil	
			±15	±15	**AD7510DIJ**	**AD (3176)**	
					AD7510DIK	**AD (3176)**	
					AD7510DIS	**†AD (3176)**	
					AD7511DIJ	**AD (3176)**	
					AD7511DIK	**AD (3176)**	
					AD7511DIS	**†AD (3176)**	10
					AD7511DIT	**†AD (3176)**	
					ADG201B	**AD (3176)**	
					ADG201C	**AD (3176)**	
					HI201-5	**Harris (2626,3287)**	
					MP7510DIJ	**Micro Pwr (401)**	
					MP7510DIK	**Micro Pwr (401)**	
					MP7510DIS	**†Micro Pwr (401)**	
					MP7511DIJ	**Micro Pwr (401)**	
					MP7511DIK	**Micro Pwr (401)**	
					MP7511DIS	**†Micro Pwr (401)**	20
					MP7511DIT	**†Micro Pwr (401)**	
					DG308A	**†Siliconix (2779,2798)**	
					DG308C	**Siliconix (2779,2798)**	
					DG309A	**†Siliconix (2779,2800)**	
					DG309C	**Siliconix (2779,2800)**	
		175	±15	±15	**DG201A**	**†Siliconix (2779,2786)**	
					DG201AA	**†Siliconix (2779,2779,2786)**	
					DG202A	**†Siliconix (2779,2788)**	
					DG202B	**Siliconix (2779,2788)**	
					DG211C	**Siliconix (2779,2790)**	30
					DG212C	**Siliconix (2779,2792)**	
		200	±15	±15	**DG201AB**	**†Siliconix (2779,2786)**	
					DG201AC	**†Siliconix (2779,2786)**	
					DG201B	**Siliconix (2779,2786)**	
					DG201C	**Siliconix (2779,2786)**	
					DG202C	**Siliconix (2779,2788)**	
		280	±7.5	±7.5	F4066BC	Fairchild	
					F4066BM	† Fairchild	
					HD14066B	Hitachi	
					MC14066BA	† Motorola	40
					MC14066BC	Motorola	
					CD4066BC	**National (3318)**	
					CD4066BM	**†National (3318)**	
					CD4066A	**†RCA (748)**	
					CD4066AE	**RCA (748)**	
					CD4066B	**†RCA (748)**	
					CD4066BE	**RCA (748)**	
					HCC4066B	† SGS	
					HCF4066B	SGS	
					N4066A	Signetics	50
					883/4066B	† SSS	
					SCL4066B	SSS	
					TC4066B	Toshiba	
						(Continued)	

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range V	Supply Voltage, V	Device	Source	Line
4xSPST	CMOS					(Cont'd)	
		400	±7.5	±7.5	HD14016B	Hitachi	
					MC14016BA	† Motorola	
					MC14016BC	Motorola	
					883/4016B	† SSS	
					SCL4016B	SSS	
					CM4016A	† Solitron	
					CM4016AE	Solitron	60
					TC4016B	Toshiba	
		800	±7.5	±7.5	F4016C	Fairchild	
					F4016M	† Fairchild	
		850	Inverted Control ±7.5				
				±7.5	883/4416B	† SSS	
					SCL4416B	SSS	
			±7.5	±7.5	**CD4016BC**	**National (3318)**	
					CD4016BM	**†National (3318)**	
					CD4016A	**†RCA (748)**	
					CD4016AE	**RCA (748)**	
					CD4016B	**†RCA (748)**	70
					CD4016BE	**RCA (748)**	
					HCC4016B	† SGS	
					HCF4016B	SGS	
					CM4016A	† Solitron	
					CM4016AE	Solitron	
					CM4116A	† Solitron	
					CM4116AE	Solitron	
	DMOS	70	±7.5	±15	**SD5001**	**Siliconix (2824)**	
					SD5002	**Siliconix (2824)**	
			±10	±15	**SD5000**	**Siliconix (2824)**	80
			±15	±15	**SD5200**	**Siliconix (2824)**	
	FET	100	±10	±15	SW201B	† PMI	
					SW201F	PMI	
					SW202B	† PMI	
					SW202F	PMI	
	JFET	10	±10	−18,2.8	CAM604A	† Teledyne C	
		30	±7.5	±15,5	AM193	National	
		50	−10 to 5	−15,5	CAG49	† Teledyne C	
			±10	±18,−7	CAG50	† Teledyne C	
		60	±10	−18,5	CAG49	† Teledyne C	90
		75	±10	±15	SW7510A	† PMI	
					SW7510B	† PMI	
					SW7510E	PMI	
					SW7510F	PMI	
					SW7511A	† PMI	
					SW7511B	† PMI	
					SW7511E	PMI	
					SW7511F	PMI	
				±15,5	AM194	National	
5xSPST	Common Output						
	PMOS	100-450	±10	−20,10	DG123	†Intersil	100
					DG123A	† Siliconix	
				−20,10,5	DG125	† Intersil	
					DG125A	† Siliconix	
		125-500	±10	−20,10	DG123B	Intersil	
					DG123B	Siliconix	
				−20,10,5	DG125B	Intersil	
					DG125B	Siliconix	
SPDT for D/A							
	NPN-PNP						
		10	0 to -10	−15	CDA1-3	† Teledyne C	
			10	10	CDA4A	† Teledyne C	
			±10	−15,5	CDA23	† Teledyne C	110
				±15	CDA6	† Teledyne C	

DT¹ means four terminals with a pair of normally open and normally closed contacts.

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INTERFACE–Analog Switches (Cont'd)

Switches with Drivers (Cont'd)

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range V	Supply Voltage, V	Device	Source		Line
SPDT [1]	CMOS	35	±10	±15,5	IH5050M	† Intersil		
		45	±10	±15,5	IH5050C	Intersil		
		50	±11	±15,5	IH5142M	† Intersil		
			±15	±15	**HI301**	**Harris**		
							(2630,3287)	
					HI305	**Harris**		
							(2630,3287)	
					HI387	**Harris**		
							(2635,3288)	
					DG301A	**† Siliconix**	(2779)	
					DG301AA	**† Siliconix**	(2779)	
					DG301AB	**Siliconix**	(2779)	
					DG301AC	**Siliconix**	(2779)	10
					DG301B	**Siliconix**	(2779)	
					DG301C	**Siliconix**	(2779)	
					DG305A	**† Siliconix**	(2779)	
					DG305AA	**† Siliconix**	(2779)	
					DG305AB	**Siliconix**	(2779)	
					DG305AC	**Siliconix**	(2779)	
					DG305B	**Siliconix**	(2779)	
					DG305C	**Siliconix**	(2779)	
					DG387A	**† Siliconix**	(2779)	
					DG387AA	**† Siliconix**	(2779)	20
					DG387AB	**Siliconix**	(2779)	
					DG387AC	**Siliconix**	(2779)	
					DG387B	**Siliconix**	(2779)	
					DG387C	**Siliconix**	(2779)	
				±15,5	**HI5050-2**	**† Harris**	(2643)	
					HI5050-5	**Harris**	(2643)	
					DG5042A	**† Siliconix**		
							(2779,2813)	
					DG5042C	**Siliconix**		
							(2779,2813)	
		75	±10	±15,5	IH5142C	Intersil		
			±11	±15,5	IH5042M	† Intersil		30
			±15	±15,5	**HI5042-2**	**† Harris**	(2643)	
					HI5042-5	**Harris**	(2643)	
		80	±10	±15,5	IH5042C	Intersil		
	JFET	6	−5 to 10	±15	CAG7	† Teledyne C		
		10	−5 to 10	±15	CAG7-10	† Teledyne C		
			−7.5 to 15	±15,5	DG186A	† Intersil		
					DG186B	Intersil		
					DG186A	**† Siliconix**	(2779)	
					DG186B	**Siliconix**	(2779)	
			−12.5 to 10					
				−20,10,5	DG186A	† Intersil		40
					DG186B	Intersil		
					DG186A	† Siliconix		
					DG186B	Siliconix		
			±10	±18,12	DG146A	† Intersil		
					AH0146	**† National**	(3344)	
					AH0146C	**National**	(3344)	
					DG146A	Siliconix		
		15	±7.5	±15	DG161A	† Intersil		
					AH0161	**† National**	(3344)	
					AH0161C	**National**	(3344)	50
					DG161A	Siliconix		
			±8	±18,12	DG146B	Intersil		
					DG446A	Intersil		
					DG146B	Siliconix		
		20	±5.5	±15	DG461A	Intersil		
					DG161B	Siliconix		
		30	−7.5 to 15	±15,5	DG187A	† Intersil		
					IH187M	† Intersil		
					AM187	† National		
					DG187A	**† Siliconix**	(2779)	60

(Continued)

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range V	Supply Voltage, V	Device	Source		Line
SPDT [1]	JFET	30					(Cont'd)	
			−12.5 to 10					
				−20,10,5	DG187A	† Intersil		
					IH187M	† Intersil		
					AM187	† National		
					DG187A	† Siliconix		
			±10	±18,12	DG144A	† Intersil		
					AH0144	**† National**	(3344)	
					AH0144C	**National**	(3344)	
					DG144A	† Siliconix		
		35	±8	±8,12	DG444A	Intersil		
		50	−7.5 to 15	±15,5	DG187B	Intersil		70
					IH187C	Intersil		
					DG187B	**Siliconix**	(2779)	
			−10 to 15	±15,5	AM287	National		
			−12.5 to 10					
				−20,10,5	DG187B	Intersil		
					IH187C	Intersil		
					DG187B	Siliconix		
			−15 to 10	−20,10,5	AM287	National		
			±7.5	±15	DG162A	† Intersil		
					AH0162	**† National**	(3344)	
					AH0162C	**National**	(3344)	80
					DG162A	† Siliconix		
			±8	±15	2126BG	† Teledyne C		
				±18,12	DG144B	Intersil		
					DG144B	Siliconix		
		75	−7.5 to 15	±15,5	AM188	† National		
			−10 to 15	±15,5	DG188A	† Intersil		
					IH188M	† Intersil		
					DG188A	**† Siliconix**	(2779)	
			−12.5 to 10					
				−20,10,5	AM188	† National		
			−15 to 10	−20,10,5	DG188A	† Intersil		90
					IH188M	† Intersil		
					DG188A	† Siliconix		
			±10	±15,5	TL188M	† TI		
		80	±8	±18,12	DG443A	Intersil		
			±10	−18,12	DG143	† Intersil		
					AH0143	**† National**	(3344)	
					AH0143C	**National**	(3344)	
					DG143A	† Siliconix		
		100	−10 to 15	±15,5	DG188B	Intersil		
					IH188C	Intersil		100
					AM288	National		
					DG188B	**Siliconix**	(2779)	
			−15 to 10	−20,10,5	DG188B	Intersil		
					IH188C	Intersil		
					AM288	National		
					DG188B	Siliconix		
			±5.5	±15	DG162B	Siliconix		
			±8	±15	DG462A	Intersil		
			±10	−18,12	DG143B	Siliconix		
				±15	**AH2114**	**† National**	(3344)	110
				±15,5	TL188C	TI		
					TL188I	TI		
		125	±10	±15	**AH2114C**	**National**	(3344)	
		300	−7.5 to 15	±15,5	**DG287A**	**† Siliconix**	(2779)	
					DG287B	**Siliconix**	(2779)	
	NPN-PNP							
		10	±10	−15,5	CDA23	† Teledyne C		
	PMOS	100-400	±10	−20,10	TL604I	TI		
					TL604M	† TI		
		200-600	±10	−20,10	TL604C	TI		
SPDT	JFET	50	−10 to 5	−15,5	CDA18	† Teledyne C		120
	PMOS	100-400	±10	−20,10	SI3002A	† Siliconix		

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Analog Switches (Cont'd)

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range V	Supply Voltage, V	Device	Source	Line
Switches with Drivers						**(Cont'd)**	
SPDT	PMOS	100-400	±10	−20,10		(Cont'd)	
					SI3002B	Siliconix	
					TL601I	TI	
					TL601M	† TI	
					TL607I	TI	
					TL607M	† TI	
		200 *	±10	−20,10	SH3002C	Fairchild	
					SH3002M	† Fairchild	
		200-600	±10	−20,10	TL601C	TI	
					TL607C	TI	
2xSPDT [1]							
	CMOS	35	±10	±15,5	IH5051M	† Intersil	10
		45	±10	±15,5	IH5051C	Intersil	
		50	±11	±15,5	IH5143M	† Intersil	
			±15	±15	**HI303**	**Harris (2630,3288)**	
					HI307	**Harris (2630,3288)**	
					HI390	**Harris (2635,3288)**	
					DG303A	**† Siliconix (2780)**	
					DG303AA	**† Siliconix (2780)**	
					DG303AB	**Siliconix (2780)**	
					DG303AC	**Siliconix (2780)**	
					DG303B	**Siliconix (2780)**	20
					DG303C	**Siliconix (2780)**	
					DG307A	**† Siliconix (2780)**	
					DG307AA	**† Siliconix (2780)**	
					DG307AB	**Siliconix (2780)**	
					DG307AC	**Siliconix (2780)**	
					DG307B	**Siliconix (2780)**	
					DG307C	**Siliconix (2780)**	
					DG390A	**† Siliconix (2780)**	
					DG390AA	**† Siliconix (2780)**	
					DG390AB	**Siliconix (2780)**	30
					DG390AC	**Siliconix (2780)**	
					DG390B	**Siliconix (2780)**	
					DG390C	**Siliconix (2780)**	
				±15,5	**HI5051-2**	**† Harris (2643,3288)**	
					HI5051-5	**Harris (2643,3288)**	
					DG243A	**† Siliconix (2780,2796)**	
					DG243C	**Siliconix (2780,2796)**	
					DG5043A	**† Siliconix (2780,2813)**	
					DG5043C	**Siliconix (2780,2813)**	
		75	±10	±15,5	IH5143C	Intersil	40
			±11	±15,5	IH5043M	† Intersil	
			±15	±15,5	**HI5043-2**	**† Harris (2643,3288)**	
					HI5043-5	**Harris (2643,3288)**	
		80	±10	±15,5	IH5043C	Intersil	
		100	±15	±15	**AD7512DIJ**	**AD (3176)**	
					AD7512DIK	**AD (3176)**	
					AD7512DIS	**† AD (3176)**	
					AD7512DIT	**† AD (3176)**	
					MP7512DIJ	**Micro Pwr (401)**	
					MP7512DIK	**Micro Pwr (401)**	50
					MP7512DIS	**† Micro Pwr (401)**	
					MP7512DIT	**† Micro Pwr (401)**	
	JFET	10	−7.5 to 15	±15,5	DG189A	† Intersil	
						(Continued)	

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range V	Supply Voltage, V	Device	Source	Line
2xSPDT [1]							
	JFET	10	−7.5 to 15	±15,5		(Cont'd)	
					DG189B	Intersil	
					DG189A	**† Siliconix (2780)**	
					DG189B	**Siliconix (2780)**	
			−12.5 to 15				
				−20,15,5	DG189A	† Intersil	
					DG189B	Intersil	
					DG189A	† Siliconix	
					DG189B	Siliconix	60
		30	−7.5 to 15	±15,5	DG190A	† Intersil	
					DG190B	Intersil	
					IH190M	† Intersil	
					AM190	† National	
					DG190A	**† Siliconix (2780)**	
			−12 to 15	−20,15,5	DG190A	† Intersil	
					DG190B	Intersil	
					IH190M	† Intersil	
					AM190	† National	
					DG190A	† Siliconix	70
		50	−7.5 to 15	±15,5	**DG190B**	**Siliconix (2780)**	
			−10 to 15	±15,5	AM290	National	
			−12.5 to 15				
				−20,10,5	DG190B	Siliconix	
			−15 to 10	−20,10,5	AM290	National	
		75	−7.5 to 15	±15,5	AM191	† National	
			−10 to 15	±15,5	DG191A	† Intersil	
					IH191M	† Intersil	
					DG191A	**† Siliconix (2780)**	
			−12.5 to 15				
				−20,10,5	AM191	† National	
			−15 to 10	−20,10,5	DG191A	† Intersil	80
					IH191M	† Intersil	
					DG191A	† Siliconix	
		100	−10 to 15	±15,5	DG191B	Intersil	
					IH191C	Intersil	
					AM291	National	
					DG191B	**Siliconix (2780)**	
			−15 to 10	−20,10,5	DG191B	Intersil	
					IH191C	Intersil	
					AM291	National	
					DG191B	Siliconix	90
		125	±10	±15,5	TL191M	† TI	
		150	±10	±15,5	TL191C	TI	
					TL191I	TI	
		300	−7.5 to 15	±15,5	**DG290A**	**† Siliconix (2780)**	
					DG290B	**Siliconix (2780)**	
	PNP	10	±10	±15	CDA29A	† Teledyne C	
3xSPDT	CMOS	280	±7.5	±7.5	F4053BC	Fairchild	
					F4053BM	† Fairchild	
					HD14053B	Hitachi	
					MC14053BA	† Motorola	100
					MC14053BC	Motorola	
					CD4053BC	**National (3318)**	
					CD4053BM	**† National (3318)**	
					CD4053B	**† RCA (748)**	
					CD4053BE	**RCA (748)**	
					HCC4053B	† SGS	
					HCF4053B	SGS	
					883/4053B	† SSS	
					SCL4053B	SSS	
					CM4053A	† Solitron	110
					CM4053AE	Solitron	
					TC4053B	Toshiba	
4xSPDT for D/A (current switch)							
	NPN	—	−10 to -3	±15	ULN-2140A	Sprague	
					ULS-2140H	† Sprague	

DT[1] means four terminals with a pair of normally open and normally closed contacts.

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INTERFACE–Analog Switches (Cont'd)

Switches with Drivers (Cont'd)

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range V	Supply Voltage, V	Device	Source	Line
4xSPDT for D/A							
	CMOS	100	0.1	8	AD7519J	AD	
4xSPDT	CMOS	—	—	8	MC14551BA	† Motorola	
					MC14551BC	Motorola	
	JFET	35	±10	−15,5	HCS310	HyComp	
	NMOS	—	—	8	DG515A	† Siliconix	
					DG515B	Siliconix	
					DG515C	Siliconix	
	PNP	7	0 to -10	−15	CDA11-S12	Teledyne C	
		10	0 to -10	−15	CDA11	Teledyne C	
10xSPDT for D/A							
	NMOS	—	—	8	DG516A	† Siliconix	10
					DG516B	Siliconix	
					DG516C	Siliconix	
DPST	CMOS	50	±15	±15	**DG384AA**	**† Siliconix (2780)**	
					DG384AB	**Siliconix (2780)**	
					DG384AC	**Siliconix (2780)**	
		75	±11	±15,5	IH5044M	† Intersil	
					IH5144C	Intersil	
					IH5144M	† Intersil	
					DG5044A	**† Siliconix (2780,2813)**	
					DG5044C	**Siliconix (2780,2813)**	20
			±15	±15,5	**HI5044-2**	**† Harris (2643)**	
					HI5044-5	**Harris (2643)**	
		80	±10	±15,5	IH5044C	Intersil	
					IH5044M	† Intersil	
	PMOS	200	±10	±12	SH3003C	Fairchild	
					SH3003M	† Fairchild	
2xDPST Common Output							
	PMOS	100-450	±10	−20,10,5	DGM122A	† Siliconix	
		125-500	±10	−20,10,5	DGM122B	Siliconix	
		200-600	±10	−20,10,5	**AH0019**	**† National (3344)**	
					AH0019C	**National (3344)**	30
2xDPST Three Control Input							
	CMOS	200	±15	±15,5	HI1800A-5	Harris	
2xDPST	CMOS	35	±10	±15,5	IH5049M	† Intersil	
		45	±10	±15,5	IH5049C	Intersil	
		50	±11	±15,5	IH5145M	† Intersil	
			±15	±15	**HI302**	**Harris (2630,3288)**	
					HI306	**Harris (2630,3288)**	
					HI384	**Harris (2635,3288)**	
					DG302A	**† Siliconix (2780)**	
					DG302AA	**† Siliconix (2780)**	
					DG302AB	**Siliconix (2780)**	40
					DG302AC	**Siliconix (2780)**	
					DG302B	**Siliconix (2780)**	
					DG302C	**Siliconix (2780)**	
					DG306A	**† Siliconix (2780)**	
					DG306AA	**† Siliconix (2780)**	
					DG306AB	**Siliconix (2780)**	
					DG306AC	**Siliconix (2780)**	
					DG306B	**Siliconix (2780)**	
					DG306C	**Siliconix (2780)**	
					DG384A	**† Siliconix (2780)**	50
					DG384B	**Siliconix (2780)**	
					DG384C	**Siliconix (2780)**	
				±15,5	**HI5049-2**	**† Harris (2643)**	
					HI5049-5	**Harris (2643)**	
					DG5045A	**† Siliconix (2780,2813)**	
					DG5045C	**Siliconix (2780,2813)**	

(Continued)

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range V	Supply Voltage, V	Device	Source	Line
						(Cont'd)	
2xDPST	CMOS	75	±10	±15,5	IH5145C	Intersil	
			±11	±15,5	IH5045M	† Intersil	
			±15	±15,5	**HI5045-2**	**† Harris (2643,3288)**	
					HI5045-5	**Harris (2643,3288)**	60
		80	±10	±15,5	IH5045C	Intersil	
	JFET	10	−7.5 to 15	±15,5	DG183A	† Intersil	
					DG183B	Intersil	
					DG183A	**† Siliconix (2780)**	
					DG183B	**Siliconix (2780)**	
			−12.5 to 10				
				−20,10,5	DG183A	† Intersil	
					DG183B	Intersil	
					DG183A	† Siliconix	
					DG183B	Siliconix	
			±10	−18,12	DG140A	† Intersil	70
					AH0140	**† National (3344)**	
					AH0140C	**National (3344)**	
					DG140A	† Siliconix	
		15	±7.5	±15	DG153A	† Intersil	
					AH0153	**† National (3344)**	
					AH0153C	**National (3344)**	
					DG153A	† Siliconix	
			±8	−18,12	DG440A	Intersil	
					DG140B	Siliconix	
		20	±5.5	±15	DG153B	Intersil	80
					DG453A	Intersil	
					DG153B	Siliconix	
		30	−7.5 to 15	±15,5	DG184A	† Intersil	
					IH184M	† Intersil	
					AM184	† National	
					DG184A	**† Siliconix (2780)**	
			−12.5 to 10				
				−20,10,5	DG184A	† Intersil	
					IH184M	† Intersil	
					AM184	† National	
					DG184A	† Siliconix	90
			±10	−18,12	DG129A	† Intersil	
					AH0129	**† National (3343)**	
					AH0129C	**National (3343)**	
					DG129A	† Siliconix	
		35	±8	−18,12	DG429A	Intersil	
		50	−7.5 to 15	±15,5	DG184B	Intersil	
					IH184C	Intersil	
					DG184B	**Siliconix (2780)**	
			−10 to 15	±15,5	AM284	National	
			−12.5 to 15				
				−20,10,5	DG184B	Intersil	100
					IH184C	Intersil	
					DG184B	Siliconix	
			−15 to 10	−20,10,5	AM284	National	
			±7.5	±15	DG154A	† Intersil	
					AH0154	† National	
					AH0154C	National	
					DG154A	† Siliconix	
			±8	−18,12	DG129B	Siliconix	
		60	±10	−18,15	CS4R101A	† Teledyne C	
		75	−7.5 to 15	±15,5	AM185	† National	110
			−10 to 15	±15,5	DG185A	† Intersil	
					IH185M	† Intersil	
					DG185A	**† Siliconix (2780)**	
			−12.5 to 10				
				−20,10,5	AM185	† National	
			−15 to 10	−20,10,5	DG185A	† Intersil	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Analog Switches (Cont'd)

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range V	Supply Voltage, V	Device	Source		Line
Switches with Drivers							**(Cont'd)**	
2xDPST	JFET	75	−15 to 10	−20,10,5			(Cont'd)	
					IH185M	† Intersil		
					DG185A	† Siliconix		
		80	±8	−18,12	DG426A	Intersil		
			±10	−18,12	DG126A	† Intersil		
					AH0126	**† National**	**(3344)**	
					AH0126C	**National**	**(3344)**	
					DG126A	† Siliconix		
		100	−10 to 15	±15,5	DG185B	Intersil		
					IH185C	Intersil		
					AM285	National		10
					DG185B	**Siliconix**	**(2780)**	
			−15 to 10	−20,10,5	DG185B	Intersil		
					IH185C	Intersil		
					AM285	National		
					DG185B	Siliconix		
			±5.5	±15	DG154B	Intersil		
					DG454A	Intersil		
					DG154B	Siliconix		
			±8	−18,12	DG126B	Siliconix		
		125	±10	±15,5	TL185M	† TI		20
		150	±10	±15,5	TL185C	TI		
					TL185I	TI		
		300	−7.5 to 15	±15,5	**DG284A**	**† Siliconix**	**(2780)**	
					DG284B	**Siliconix**	**(2780)**	
3xDPST Common Output								
	PMOS	100-450	±10	−20,10	DG120	† Intersil		
				−20,10,5	DG121	† Intersil		
DPDT with followers								
					TDA1527	Signetics		
DPDT[1]	CMOS	50	±15	±15,5	**HI5046A-2**	**† Harris**	**(2643)**	
					HI5046A-5	**Harris**	**(2643)**	
		75	±11	±15,5	IH5046M	† Intersil		30
			±15	±15,5	**HI5046-2**	**† Harris**	**(2643)**	
					HI5046-5	**Harris**	**(2643)**	
		80	±10	±15,5	IH5046C	Intersil		
	JFET	10	±10	−18,12	DG145A	† Intersil		
					AH0145	**† National**	**(3344)**	
					AH0145C	**National**	**(3344)**	
					DG145A	† Siliconix		
		15	±7.5	±15	DG163A	† Intersil		
					AH0163	**† National**	**(3344)**	
					AH0163C	**National**	**(3344)**	40
					DG163A	† Siliconix		
			±8	−18,12	DG445A	Intersil		
					DG145B	Siliconix		
		20	±5.5	±15	DG163B	Intersil		
					DG463A	Intersil		
					DG163B	Siliconix		
		30	±10	−18,12	DG139A	† Intersil		
					AH0139	**† National**	**(3344)**	
					AH0139C	**National**	**(3344)**	
					DG139A	† Siliconix		50
		35	±8	−18,12	DG439A	Intersil		
		50	±7.5	±15	DG164A	† Intersil		
					AH0164	**† National**	**(3344)**	
					AH0164C	**National**	**(3344)**	
					DG164A	† Siliconix		
			±8	−18,12	DG139B	Siliconix		
		80	±8	−18,12	DG442A	Intersil		
			±10	−18,12	DG142A	† Intersil		
					AH0142	**† National**	**(3344)**	
					AH0142C	**National**	**(3344)**	60
					DG142A	† Siliconix		
		100	±5.5	±15	DG164B	Intersil		
							(Continued)	

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range V	Supply Voltage, V	Device	Source		Line
DPDT[1]	JFET	100	±5.5	±15			(Cont'd)	
					DG464A	Intersil		
					DG164B	Siliconix		
			±10	−18,12	DG142B	Siliconix		
DPDT	PMOS	200-600	±10	−20,10,5	**AH0014**	**† National**	**(3344)**	
					AH0014C	**National**	**(3344)**	
2xDPDT with Followers								
					TDA1028	Signetics		
2xDPDT	PMOS	150-1000	0 to -18	−(5-21)	TDA1195	Siemens		
DP4T with Followers								
					TDA1029	Signetics		70
4PDT for D/A								
	PNP	10	±10	±15,5	CDA28A	† Teledyne C		
4PST	CMOS	50	±15	±15,5	**HI5047A-2**	**† Harris**	**(2643)**	
					HI5047A-5	**Harris**	**(2643)**	
		75	±11	±15,5	IH5047M	† Intersil		
			±15	±15,5	**HI5047-2**	**† Harris**	**(2643)**	
					HI5047-5	**Harris**	**(2643)**	
		80	±10	±15,5	IH5047C	Intersil		
Switches without Drivers								
SPST	JFET	30	±10		AM1000	† National		
		50	±15		AM1001	† National		
		100	0 to (Drive-4)					
					IH5037C	Intersil		80
					IH5037M	† Intersil		
			±0.2		IH5021C	† Intersil		
					IH5021M	† Intersil		
					IH5023C	Intersil		
					IH5023M	† Intersil		
			±10		AM1002	† National		
		150	0 to (Drive-4)					
					IH5038C	Intersil		
					IH5038M	† Intersil		
			±0.2		IH5022C	Intersil		
					IH5022M	† Intersil		90
					IH5024C	Intersil		
					IH5024M	† Intersil		
2xSPST Common Output								
	JFET	100	0 to (Drive-4)					
					IH5035C	Intersil		
					IH5035M	† Intersil		
			±0.2		IH5019C	Intersil		
					IH5019M	† Intersil		
		150	0 to (Drive-4)					
					IH5034C	Intersil		
					IH5034M	† Intersil		
			±0.2		IH5018C	Intersil		
					IH5018M	† Intersil		100
2xSPST	JFET	100	0 to (Drive-4)					
					IH5033C	Intersil		
					IH5033M	† Intersil		
			±0.2		IH5017C	Intersil		
					IH5017M	† Intersil		
		150	0 to (Drive-4)					
					IH5036C	Intersil		
					IH5036M	† Intersil		
			±0.2		IH5020C	Intersil		
					IH5020M	† Intersil		
3xSPST Common Output								
	JFET	100	0 to (Drive-4)					
					IH5029C	Intersil		
					IH5029M	† Intersil		110
			±0.2		IH5013C	Intersil		
					IH5013M	† Intersil		
							(Continued)	

DT[1] means four terminals with a pair of normally open and normally closed contacts.

IC MASTER

INTERFACE–Analog Switches (Cont'd)

Switches without Drivers (Cont'd)

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range V	Supply Voltage, V	Device	Source		Line
3xSPST Common Output	JFET						(Cont'd)	
		150	0 to (Drive-4)		IH5030C	Intersil		
					IH5030M	† Intersil		
			±0.2		IH5014C	Intersil		
					IH5014M	† Intersil		
3xSPST	JFET	100	0 to (Drive-4)		IH5031C	Intersil		
					IH5031M	† Intersil		
			±0.2		IH5015C	Intersil		
					IH5015M	† Intersil		
		150	0 to (Drive-4)		IH5032C	Intersil		
					IH5032M	† Intersil		10
			±0.2		IH5016C	Intersil		
					IH5016M	† Intersil		
	PMOS	200-600			MM455	† Intersil		
					MM555	Intersil		
4xSPST Common Output	JFET	—			G129	Intersil		
					G130	† Intersil		
					G131	† Intersil		
					G132	† Intersil		
					G1350	Intersil		
					G1360	Intersil		20
		100	0 to (Drive-4)		IH5025C	Intersil		
					IH5025M	† Intersil		
			±0.2		IH5009C	Intersil		
					IH5009M	† Intersil		
					AH5009C	**National**	**(3318)**	
					AM9709C	National		
					AM97C09	National		
		150	0 to (Drive-4)		IH5026C	Intersil		
					IH5026M	† Intersil		
			±0.2		IH5010C	Intersil		30
					IH5010M	† Intersil		
					AH5010C	**National**	**(3318)**	
					AM9710C	National		
					AM97C10C	National		
	PMOS	—			G124	Intersil		
					MM451	† Intersil		
					MM551	Intersil		
4xSPST Two Outputs	JFET	—			G123	Intersil		
	PMOS	—			G123A	† Siliconix		
					G123B	Siliconix		40
4xSPST	JFET	—			G125	† Intersil		
					G126	† Intersil		
					G127	† Intersil		
					G128	† Intersil		
					G1330	Intersil		
					G1340	Intersil		
		100	0 to (Drive-4)		IH5027C	Intersil		
					IH5027M	† Intersil		
			±0.2		IH5011C	Intersil		
					IH5011M	† Intersil		50
					AH5011C	**National**	**(3318)**	
					AM9711C	National		
					AM97C11C	National		
		150	0 to (Drive-4)		IH5028C	Intersil		
					IH5028M	† Intersil		

(Continued)

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range V	Supply Voltage, V	Device	Source		Line
4xSPST	JFET	150					(Cont'd)	
			±0.2		IH5012C	Intersil		
					IH5012M	† Intersil		
					AH5012C	**National**	**(3318)**	
					AM9712C	National		
					AM97C12C	National		60
	PMOS	200-600			MM452	† Intersil		
					MM552	Intersil		
5xSPST Common Output plus Output Switch	PMOS	—			G117A	† Intersil		
					G117B	Intersil		
					G117A	† Siliconix		
5xSPST Common Output	PMOS	—			G116A	† Intersil		
					G116B	Intersil		
					G116A	† Siliconix		
					G116B	Siliconix		
6xSPST Common Output	PMOS	—			G115A	† Intersil		70
					G115B	Intersil		
					G118A	† Intersil		
					G118B	Intersil		
					AM2009	† National		
					AM2009C	National		
					G115A	† Siliconix		
					G115B	Siliconix		
					G118A	† Siliconix		
2xDPST Common Output	PMOS	—			MM450	† Intersil		
					MM550	Intersil		80
					G122A	† Siliconix		
3xDPST Common Output	PMOS	—			G119A	† Intersil		
					G119B	Intersil		
					G119A	† Siliconix		
					G119B	Siliconix		

Drivers

High Current Switch (to drive power transistor switches)					SG1629	† Silicon G		
					SG3629	Silicon G		
2 Channel					D112C	Intersil		
					D112M	† Intersil		
					D113C	Intersil		90
					D113M	† Intersil		
					D120C	Intersil		
					D120M	† Intersil		
					D121C	Intersil		
					D121M	† Intersil		
					D139A	† Siliconix		
					D139B	Siliconix		
					D139C	Siliconix		
4 Channel					D129	Intersil		
					D129A	† Siliconix		100
					D129B	Siliconix		
6 Channel					D123C	Intersil		
					D123M	† Intersil		
					D125C	Intersil		
					D125M	† Intersil		
					D123A	† Siliconix		
					D123B	Siliconix		
					D125A	† Siliconix		
					D125B	Siliconix		
					CDR125A	† Teledyne C		110

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Analog Switches (Cont'd)

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range V	Supply Voltage, V	Device	Source		Line
Multiplexers								
4 channel. See Switches 4xSPST								
Crosspoint Switches								
					MC142100	**Motorola**	**(3298)**	
					MC145100	**Motorola**	**(3298)**	
					MC3416	Motorola		
					RC4444	Raytheon		
					RM4444	† Raytheon		
					CD22100	**RCA**	**(749,753)**	
					CD22101	**RCA**	**(749,754)**	
					CD22102	**RCA**	**(749,754)**	
					D169	Siliconix		10
4 Channel Differential								
	—	6.5	±15	±15	HI529	Harris		
		900	±10	±15	**HI539-2**	**† Harris**	**(2674,3288)**	
					HI539-5	**Harris**	**(2674,3288)**	
	CMOS	230	±15	±15	**MP7502DIS**	**† Micro Pwr**	**(401,2749)**	
					MP7509DIS	**† Micro Pwr**	**(401)**	
		250	±15	±15	**MVD-409**	**Datel**	**(2622)**	
					MVD-409M	**† Datel**	**(2622)**	
		270	±7.5	±7.5	MC14529BA	† Motorola		
					MC14529BC	Motorola		
					CD4529BC	National		20
					CD4529BM	† National		
		280	±7.5	±7.5	F4052BC	Fairchild		
					F4052BM	† Fairchild		
					HD14052B	Hitachi		
					MC14052BA	† Motorola		
					MC14052BC	Motorola		
					CD4052BC	**National**	**(3318)**	
					CD4052BM	**† National**	**(3318)**	
					CD4052B	**† RCA**	**(748)**	
					CD4052BE	**RCA**	**(748)**	30
					HCC4052B	† SGS		
					HCF4052B	SGS		
					883/4052B	† SSS		
					SCL4052B	SSS		
					CM4052B	† Solitron		
					CM4052BE	Solitron		
					TC4052B	Toshiba		
		300	±15	±15	**AD7502J**	**AD**	**(3176)**	
					AD7502K	**AD**	**(3176)**	
					AD7502S	**† AD**	**(3176)**	40
					HI509-2	**† Harris**	**(2654,3288)**	
					HI509-5	**Harris**	**(2654,3288)**	
					IH6208M	† Intersil		
		320	±15	±15	**MP7502DIJ**	**Micro Pwr**	**(401,2749)**	
					MP7502DIK	**Micro Pwr**	**(401,2749)**	
					MP7509DIJ	**Micro Pwr**	**(401)**	
					MP7509DIK	**Micro Pwr**	**(401)**	
		350	±15	±15	IH6208C	Intersil		
		400	±15	±15	HI1828A-2	† Harris		
					HI1828A-5	Harris		50
					DG506AA	**† Siliconix**	**(2802)**	
					DG509A	**† Siliconix**	**(2804)**	
					DG509AA	**† Siliconix**	**(2804)**	
		450	±15	±15	**DG506AB**	**Siliconix**	**(2802)**	
					DG506AC	**Siliconix**	**(2802)**	
					DG509AB	**Siliconix**	**(2804)**	
							(Continued)	

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range V	Supply Voltage, V	Device	Source		Line
4 Channel Differential							(Cont'd)	
	CMOS	450	±15	±15	**DG509AC**	**Siliconix**	**(2804)**	
					DG509B	**Siliconix**	**(2804)**	
					DG509C	**Siliconix**	**(2804)**	
		750	±15	±15	MPC801	Burr-Brown		60
		1000	±13	±15	IH5208M	† Intersil		
		1200	±13	±15	IH5208C	Intersil		
		1300	±15	±15	MPC4D	Burr-Brown		
		1500	±15	±15	**MXD-409**	**Datel**	**(2622)**	
					MXD-409M	**† Datel**	**(2622)**	
					HI509A-2	**† Harris**	**(2654,3288)**	
		1800	±15	±15	**HI509A-5**	**Harris**	**(2654,3288)**	
	JFET	260	−15 to 11.5	±15	MUX-24A	† PMI		
					MUX-24E	PMI		
		350 *	−15 to 12	±15	**LF11509**	**† National**	**(3318)**	70
					LF13509	National		
		370	−15 to 12	±15	MUX-24B	† PMI		
					MUX-24F	PMI		
4 Channel Sequential Commutator								
	PMOS	200-600	±10	−24,12	MM554	National		
4 Channel Video								
	CMOS	450	±15	±15	**HI524-2**	**† Harris**	**(2669,3288)**	
					HI524-5	**Harris**	**(2669,3288)**	
4 Channel Video Multiplexer								
	CMOS	270	±7.5	±7.5	MC14529BA	† Motorola		
					MC14529BC	Motorola		
					CD4529BC	National		
					CD4529BM	† National		80
4 Channel with Input Latch								
	CMOS	400	±15	±15	**DG529A**	**† Siliconix**	**(2806)**	
		450	±15	±15	**DG529C**	**Siliconix**	**(2806)**	
6 Channel								
	CMOS	150	±8	±8	MS504	RTC		
	JFET	60	±10	−18,2.8	CAM601A	† Teledyne C		
8 Channel								
	CMOS	230	±15	±15	**MP7501DIS**	**† Micro Pwr**	**(401,2749)**	
					MP7503DIS	**† Micro Pwr**	**(401,2749)**	
					MP7508DIS	**† Micro Pwr**	**(401)**	
		250	±15	±15	**MV-808**	**Datel**	**(2622)**	
					MV-808M	**† Datel**	**(2622)**	
		280	±7.5	±7.5	F4051BC	Fairchild		90
					F4051BM	† Fairchild		
					HD14051B	Hitachi		
					MC14051BA	† Motorola		
					MC14051BC	Motorola		
					CD4501BC	**National**	**(3318)**	
					CD4501BM	**† National**	**(3318)**	
					CD4051B	**† RCA**	**(748)**	
					CD4051BE	**RCA**	**(748)**	
					HCC4051B	† SGS		
					HCF4051B	SGS		100
					883/4051B	† SSS		
					SCL4051B	SSS		
					CM4051A	† Solitron		
					CM4051AE	Solitron		
					TC4051B	Toshiba		
		300	±15	±15	**AD7501J**	**AD**	**(3176)**	
					AD7501K	**AD**	**(3176)**	
					AD7501S	**† AD**	**(3176)**	
					AD7503J	**AD**	**(3176)**	
							(Continued)	

DT¹ means four terminals with a pair of normally open and normally closed contacts.

IC MASTER

INTERFACE–Analog Switches (Cont'd)

Multiplexers (Cont'd)

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range V	Supply Voltage, V	Device	Source		Line
8 Channel							(Cont'd)	
	CMOS	300	±15	±15	**AD7503K**	**AD**	**(3176)**	
					AD7503S	**†AD**	**(3176)**	
					HI508-2	**†Harris**	**(2654,3288)**	
					HI508-5	**Harris**	**(2654,3288)**	
					IH6108M	† Intersil		
		320	±15	±15	**MP7501DIJ**	**Micro Pwr**	**(401,2749)**	
					MP7501DIK	**Micro Pwr**	**(401,2749)**	
					MP7503DIJ	**Micro Pwr**	**(401,2749)**	
					MP7503DIK	**Micro Pwr**	**(401,2749)**	
					MP7508DIJ	**Micro Pwr**	**(401)**	10
					MP7508DIK	**Micro Pwr**	**(401)**	
		350	±15	±15	IH6108C	Intersil		
		400	±15	±15	**DG508A**	**†Siliconix**	**(2804)**	
					DG508AA	**†Siliconix**	**(2804)**	
				±15,5	**HI1818A-2**	**†Harris**	**(3288)**	
					HI1818A-5	**Harris**	**(3288)**	
		450	±15	±15	**DG508AB**	**Siliconix**	**(2804)**	
					DG508AC	**Siliconix**	**(2804)**	
					DG508B	**Siliconix**	**(2804)**	
					DG508C	**Siliconix**	**(2804)**	20
		750	±15	±15	MX-818	Datel		
					MX-818M	† Datel		
		1000	±13	±15	IH5108M	† Intersil		
		1200	±13	±15	IH5108C	Intersil		
		1300	±15	±15	MPC8S	Burr-Brown		
		1500	±15	±15	MN4708	Analogic		
					MX-808	**Datel**	**(2622)**	
					MX-808M	**†Datel**	**(2622)**	
					HI508A-2	**†Harris**	**(2654,3288)**	
					HS508ARH	† Harris		30
		1800	±15	±15	**HI508A-5**	**Harris**	**(2654,3288)**	
	JFET	260	−15 to 11.5	±15	MUX-08E	PMI		
					MUX-88E	PMI		
		300	−15 to 12	±15	MUX-08A	† PMI		
		350 *	−15 to 12	±15	**LF11508**	**†National**	**(3318)**	
					LF13508	National		
		370	−15 to 12	±25	MUX-08F	PMI		
					MUX-88F	PMI		
		400	−15 to 12	±15	DMX-88E	PMI		
					MUX-08B	† PMI		40
		520	−15 to 12	±15	DMX-88F	PMI		
	PMOS	150-250	±5	−20,5	DG501A	† Siliconix		
					DG501B	Siliconix		
					DG501C	Siliconix		
		150-400	±5	−20,5	SI3705	Siliconix		
		150-800	±10	−20,10	DG503A	† Siliconix		
					DG503B	Siliconix		
		200-600	±5	−15,5	DG501A	† Siliconix		
		200-800	±5	−15,5	DG501B	Siliconix		
					DG501C	Siliconix		50
		250-400	±5	−15,5	**AM3705**	**National**	**(3318)**	
					AM3705C	**National**	**(3318)**	
		450	−15	−20	3708	Fairchild		
8 Channel Differential								
	CMOS	230	±15	±15	**MP7507DIS**	**†Micro Pwr**	**(401,2749)**	
		250	±7.5	±7.5	MC14097BA	† Motorola		
					MC14097BC	Motorola		
		270	±15	±15	**MVD-807**	**Datel**	**(2622)**	
					MVD-807M	**†Datel**	**(2622)**	
		280	±7.5	±7.5	**CD4097B**	**†RCA**	**(748)**	
					CD4097BE	**RCA**	**(748)**	60
					HCC4097B	† SGS		
					HCF4097B	SGS		
		320	±15	±15	**MP7507DIJ**	**Micro Pwr**	**(401,2749)**	
					MP7507DIK	**Micro Pwr**	**(401,2749)**	
		400	±15	±15	**AD7507S**	**†AD**	**(3176)**	
					AD7507T	**†AD**	**(3176)**	
					HI507-2	**†Harris**	**(2650,3288)**	
					HI507-5	**Harris**	**(2650,3288)**	
					DG507A	**†Siliconix**	**(2802)**	
					DG507AA	**†Siliconix**	**(2802)**	70
					DG528A	**†Siliconix**	**(2806)**	
		450	±15	±15	**AD7507J**	**AD**	**(3176)**	
					AD7507K	**AD**	**(3176)**	
					DG507AB	**Siliconix**	**(2802)**	
					DG507AC	**Siliconix**	**(2802)**	
					DG507B	**Siliconix**	**(2802)**	
					DG507C	**Siliconix**	**(2802)**	
					DG528C	**Siliconix**	**(2806)**	
		600	±10	±15	**HI518-2**	**†Harris**	**(2666,3288)**	
					HI518-5	**Harris**	**(2666,3288)**	80
					IH6216C	Intersil		
					IH6216M	† Intersil		
		750	±15	±15	MPC800	Burr-Brown		
		1300	±15	±15	MPC8D	Burr-Brown		
		1500	±15	±15	**MXD-807**	**Datel**	**(2622)**	
					MXD-807M	**†Datel**	**(2622)**	
					HI507A-2	**†Harris**	**(2650,3288)**	
		1800	±15	±15	MN4708D	Analogic		
					HI507A-5	**Harris**	**(2650,3288)**	
	JFET	300	−15 to 11	±15	MUX-28A	† PMI		90
					MUX-28E	PMI		
		450	−15 to 11.5	±15	MUX-28B	† PMI		
					MUX-28F	PMI		
8 Channel Differential with Storage, Counter								
	PMOS	750	±5	−12,5	AY5-1016	GI		
					AY6-4016	† GI		
8 Channel, BCD Input, Latch								
	PMOS	—	60	0-70	**LS7110**	**LSI Comp**	**(696)**	
16 Channel								
	CMOS	—	±15	±15	TC5023	Toshiba		
		170	±15	±15	**MV-1606M**	**†Datel**	**(2622)**	
		230	±15	±15	**MP7506DIS**	**†Micro Pwr**	**(401,2749)**	
		250	±15	±15	MC14067BA	† Motorola		100
					MC14067BC	Motorola		
		270	±15	±15	**MV-1606**	**Datel**	**(2622)**	
		280	±7.5	±7.5	F4067BC	Fairchild		
					F4067BM	Fairchild		
					CD4067B	**†RCA**	**(748)**	
					CD4067BE	**RCA**	**(748)**	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Analog Switches (Cont'd)

Multiplexers (Cont'd)

Function	Switch Type	ON Resistance 25°C, Ω	Analog Signal Range V	Supply Voltage, V	Device	Source		Line
16 Channel							(Cont'd)	
	CMOS	280	±7.5	±7.5	HCC4067B	† SGS		
					HCF4067B	SGS		
		320	±15,5	±15,5	**MP7506DIJ**	**Micro Pwr**	**(401,2749)**	
					MP7506DIK	**Micro Pwr**	**(401,2749)**	
		400	±15	±15	**AD7506S**	**†AD**	**(3176)**	
					AD7506T	**†AD**	**(3176)**	
					HI506-2	**†Harris**	**(2650,3288)**	
					HI506-5	**Harris**	**(2650,3288)**	
					DG506A	**†Siliconix**	**(2802)**	
		450	±15	±15	**AD7506J**	**AD**	**(3176)**	10
					AD7506K	**AD**	**(3176)**	
					DG506B	**Siliconix**	**(2802)**	
					DG506C	**Siliconix**	**(2802)**	
		600	±10	±15	**HI516-2**	**†Harris**	**(2663,3288)**	
					HI516-5	**Harris**	**(2663,3288)**	
					IH6116C	Intersil		
					IH6116M	† Intersil		
		750	±15	±15	MX-1616	Datel		
					MX-1616M	† Datel		
		1000	−5 to 15	±15,5	HI1840-5	Harris		20
		1200	±15	±15	**MX-1606M**	**†Datel**	**(2622)**	
		1300	±15	±15	MPC16S	Burr-Brown		
		1500	±15	±15	**MX-1606**	**Datel**	**(2622)**	
					HI506A-2	**†Harris**	**(2650,3288)**	
		1800	±15	±15	MN4716	Analogic		
					HI506A-5	**Harris**	**(2650,3288)**	
		5000	−5 to 15	±15,5	HI1840-2	† Harris		
			±5 to 15	±15,5	HS1840RH	† Harris		
	JFET	300	−15 to 11	±15	MUX-16A	† PMI		
					MUX-16E	PMI		30
		450	−15 to 11.5	±15	MUX-16B	† PMI		
					MUX-16F	PMI		

DT¹ means four terminals with a pair of normally open and normally closed contacts.

IC MASTER

INTERFACE–Analog to Digital Converters

Bits Res.	Linearity Error ±LSB	Conversion Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Output	Off. Bin. Output	Compl. Bin. Output	Compl. Off. Bin. Output	CTC or 2's Compl. Output	Sign. Magn. Output	Mux. In.	S&H	Integrating	Int. Ref.	Par. Out	Ser. Out	Device	Source	Line
Binary Output																		
3	1/8	0.02	—	x												ADCHU3B	Datel	
4	1/4	0.033 *	250	x		x		x			x			x		**TDC1021**	**†TRW (3438)**	
				x		x		x			x			x		TDC1021	TRW	
6	—	1	—										x			**MAH-0801**	**AD (3175)**	
	1/8	—														**AD5010K**	**AD (3175)**	
																AD6020K	**AD (3175)**	
	1/4	0.02	450	x	x						x			x		SDA5010	Siemens	
				x	x						x			x		SDA6020	Siemens	
	1/2	0.02	1000	x												ZN440CJ	Ferranti	
		0.033 *	1000	x		x		x			x			x		**TDC1014**	**†TRW (3438)**	10
				x		x		x			x			x		TDC1014	TRW	
		0.066	315										x	x		**CA3300**	**RCA (3357)**	
		90	120	x											x	NE5036	Signetics	
		100	100	x										x		NE5037	Signetics	
		100MHz	—	x	x		x							x		**TDC1029**	**TRW (3438)**	
		1000	20 *	x											x	TL507C	TI	
7	1/4	—	1200	x										x		**MC10315L**	**Motorola (2760)**	
				x										x		**MC10317L**	**Motorola (2760)**	
	1/2	20MHz	—	x	x		x							x		**TDC1027**	**TRW (3438)**	
	1	—	100 *											x	x	TM1070	Telmos	20
8	—	1	—										x			**MAH-1001**	**AD (3175)**	
	1/4	9	—		x	x							x	x		ZN447E-8	DDC	
					x	x							x	x		ZN447J-8	† DDC	
		100 *	875	x										x		ADC0801	† Intersil	
				x										x		ADC0801C	Intersil	
		110	875	x										x		ADC0801C	National	
				x										x		ADC0801M	† National	
	1/2	0.033 *	2500	x		x		x			x			x		**TDC1007**	**†TRW (3438)**	
				x		x		x			x			x		TDC1007	TRW	
		0.066	315										x	x		**CA3308**	**RCA (3359)**	30
		0.4	400	x										x		**TDC1001**	**TRW (3438)**	
		0.6	1250	x	x			x						x	x	**ADC-815MC**	**Datel (2619)**	
				x	x			x						x	x	**ADC-815MM**	**†Datel (2618)**	
		0.9	1400			x	x						x	x	x	DDC-5101	† DDC	
			1550	x	x									x	x	**ADC-5101**	**Datel (2621)**	
				x	x									x	x	**ADC-5101E**	**Datel (2621)**	
				x		x								x	x	**ADC-5101H**	**†Datel (2618,2621)**	
				x		x	x						x	x	x	MN5101	Micro Net	
				x		x	x						x	x	x	MN5101H	† Micro Net	
		1	400	x										x		**TDC1002**	**TRW (3438)**	40
			500 *	x	x								x	x	x	ZN433BJ-8	Ferranti	
				x	x								x	x	x	ZN433CJ-8	Ferranti	
				x	x								x	x	x	ZN433J-8	† Ferranti	
			1250	x	x			x						x	x	**ADC-825MC**	**Datel (2619)**	
				x	x			x						x	x	**ADC-825MM**	**†Datel (2618)**	
		1 *	—	x				x					x			**AM6108**	**AMD (3103)**	
		1.2	1800			x	x						x			**HAS-0802**	**AD (3175)**	
		1.5	1550	x		x	x						x	x	x	MN5100	Micro Net	
				x		x	x						x	x	x	MN5100H	† Micro Net	
		2.5	35 *	x							x			x		**ADC0820**	**National (3321)**	50
			650	x	x			x					x	x		ADC541B-8	† Hybrid Sys	
				x	x			x					x	x		ADC541C-8	Hybrid Sys	
						x	x	x					x	x	x	ADC542B-8	† Hybrid Sys	
						x	x	x					x	x	x	ADC542C-8	Hybrid Sys	
			915			x							x	x	x	MN5140	Micro Net	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Analog to Digital Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Conversion Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Output	Off. Bin. Output	Compl. Bin. Output	Compl. Off. Bin. Output	CTC or 2's Compl. Output	Sign. Magn. Output	Mux. In.	S&H	Integrating	Int. Ref.	Par. Out	Ser. Out	Device	Source	Line
Binary Output																	**(Cont'd)**	
																	(Cont'd)	
8	1/2	2.5	915			x							x	x	x	MN5140H	† Micro Net	
					x								x	x	x	MN5141	Micro Net	
					x								x	x	x	MN5141H	† Micro Net	
					x								x	x	x	MN5142	Micro Net	
					x								x	x	x	MN5142H	† Micro Net	
				x									x	x	x	MN5143	Micro Net	
				x									x	x	x	MN5143H	† Micro Net	
			1000			x							x	x	x	MN5130	Micro Net	
						x							x	x	x	MN5130H	† Micro Net	
					x								x	x	x	MN5131	Micro Net	10
					x								x	x	x	MN5131H	† Micro Net	
					x								x	x	x	MN5132	Micro Net	
					x								x	x	x	MN5132H	† Micro Net	
				x									x	x	x	MN5133	Micro Net	
				x									x	x	x	MN5133H	† Micro Net	
				x	x	x							x	x	x	MN5150	Micro Net	
		2.8	650			x	x	x					x	x	x	HSADC82	Hybrid Sys	
			900			x	x	x								ADC82A	Burr-Brown	
		6	1000			x							x	x	x	MN5120	Micro Net	
						x							x	x	x	MN5120H	† Micro Net	20
					x								x	x	x	MN5121	Micro Net	
					x								x	x	x	MN5121H	† Micro Net	
					x								x	x	x	MN5122	Micro Net	
					x								x	x	x	MN5122H	† Micro Net	
				x									x	x	x	MN5123	Micro Net	
				x									x	x	x	MN5123H	† Micro Net	
		7	1165		x					x	x		x	x	x	MN7100	Micro Net	
					x					x	x		x	x	x	MN7100H	† Micro Net	
					x					x	x		x	x	x	MN7120	Micro Net	
					x					x	x		x	x	x	MN7120H	† Micro Net	30
		8	—	x									x			ZN437E-8	Ferranti	
				x	x								x			ZN437J-8	† Ferranti	
		9	—		x	x							x	x		ZN448E-8	Ferranti	
					x	x							x	x		ZN448J-8	† Ferranti	
		12	720				x						x	x	x	MN509	Micro Net	
							x						x	x	x	MN509H	† Micro Net	
			900	x									x	x	x	MN502	Micro Net	
				x									x	x	x	MN502H	† Micro Net	
							x						x	x	x	MN503	Micro Net	
							x						x	x	x	MN503H	† Micro Net	40
						x							x	x	x	MN504	Micro Net	
						x							x	x	x	MN504H	† Micro Net	
							x						x	x	x	MN507	Micro Net	
							x						x	x	x	MN507H	† Micro Net	
		15	30	x	x		x						x			**AD7574B**	**AD (3174)**	
				x	x		x						x			**AD7574K**	**AD (3174)**	
				x	x		x						x			**AD7574T**	**†AD (3174)**	
				x	x		x						x			**MP7574B**	**Micro Pwr (401,2749)**	
				x	x		x						x			**MP7574K**	**Micro Pwr (401,2749)**	
					x		x						x			**MP7574T**	**Micro Pwr (401,2749)**	50
			125 *	x	x								x	x		ZN427E-8	Ferranti	
				x	x								x	x		ZN427J-8	† Ferranti	

(Continued)

Bin.—Binary
Off.—Offset
Compl.—Complementary
Magn.—Magnitude
CTC—Compl. 2's Compl.
Int. Ref.—Internal Reference
Mux. In—Multiplexed Inputs
S&H—Sample and Hold
Par. Out—Parallel Output
Ser. Out—Serial Output

IC MASTER

INTERFACE–Analog to Digital Converters (Cont'd)

Binary Output (Cont'd)

Bits Res.	Linearity Error ±LSB	Conversion Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Output	Off. Bin. Output	Compl. Bin. Output	Compl. Off. Bin. Output	CTC or 2's Compl. Output	Sign. Magn. Output	Mux. In.	S&H	Integrating	Int. Ref.	Par. Out	Ser. Out	Device	Source	Line
																	(Cont'd)	
8	1/2	17	300	x										x		**ME5034**	**Signetics (3396)**	
		20	350 *	x	x								x	x	x	ZN432-8	† Ferranti	
					x								x	x	x	ZN432B-8	Ferranti	
					x								x	x	x	ZN432C-8	Ferranti	
				x	x								x	x	x	ZN432E-8	Ferranti	
		30	—	x									x			**AD673J**	**AD (3174)**	
				x									x			**AD673S**	**† AD (3174)**	
		40	5 *	x	x									x	x	AD7570J	AD	
				x	x									x	x	**MP7570J**	**Micro Pwr (401,2749)**	
				x	x									x	x	**MP7570P**	**† Micro Pwr (401,2749)**	10
			10 *	x						x				x		**ADC0844**	**National (3324)**	
			175 *	x	x								x	x		**AD570J**	**AD (3174)**	
				x	x								x	x		**AD570S**	**† AD (3174)**	
				x	x								x	x		**MCE570J**	**Micro Eng (4440)**	
				x	x								x	x		**MCE570S**	**† Micro Eng (4440)**	
		60MHz	—	x	x		x							x		**TDC1025**	**TRW (3438)**	
		66.6	—	x												AD8581L	AD	
		80	10	x											x	**ADC0831B**	**National (3319,3322)**	
				x											x	**ADC0832B**	**National (3319,3322)**	
				x											x	**ADC0833B**	**National (3319,3323)**	20
				x											x	**ADC0834B**	**National (3319,3322)**	
				x											x	**ADC0838B**	**National (3319,3322)**	
		100	30	x						x				x		**ADC0808**	**National (3319)**	
				x						x				x		**ADC0816**	**† National (3319)**	
				x						x				x		ADC0808	TI	
			70			x							x	x	x	ADC-830	Datel	
							x						x	x	x	MN5065	Micro Net	
							x						x	x	x	MN5065H	† Micro Net	
						x							x	x	x	MN5066	Micro Net	
						x							x	x	x	MN5066H	† Micro Net	30
		100 *	875	x										x		ADC0802	† Intersil	
				x										x		ADC0802C	Intersil	
				x										x		ADC0803	† Intersil	
				x										x		ADC0803C	Intersil	
				x										x		**ADC0802**	**† National (3319)**	
				x										x		**ADC0802C**	**National (3319)**	
				x										x		**ADC0803**	**† National (3319)**	
				x										x		**ADC0803C**	**National (3319)**	
		108 *	6.8	x						x				x		MK50808	Mostek	
				x						x				x		MK50816	Mostek	40
		300	15 *	x						x						**TL530**	**TI (2865)**	
				x												**TL532**	**TI (2868)**	
		1250 *	20 *	x	x									x		4140	Teledyne P	
				x	x									x		4143	Teledyne P	
				x	x									x		4143-01	† Teledyne P	
		1800	20	x	x							x		x		**ADC-EK8B**	**Datel (2619)**	
			25	x								x		x		TSC8700	Teledyne S	
				x								x		x		TSC8703	Teledyne S	
			43	x										x		**ADC-ET8BM**	**† Datel (2619)**	
			50	x										x		**ADC-ET8BC**	**Datel (2619)**	50

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

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INTERFACE–Analog to Digital Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Conversion Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Output	Off. Bin. Output	Compl. Bin. Output	Compl. Off. Bin. Output	CTC or 2's Compl. Output	Sign. Magn. Output	Mux. In.	S&H	Integrating	Int. Ref.	Par. Out	Ser. Out	Device	Source	Line
Binary Output																	**(Cont'd)**	
8																	(Cont'd)	
	3/4	15	30	x	x		x						x			**AD7574A**	**AD (3174)**	
				x	x		x						x			**AD7574J**	**AD (3174)**	
				x	x		x						x			**AD7574S**	**†AD (3174)**	
				x	x		x						x			**MP7574A**	**† Micro Pwr (401,2749)**	
				x	x		x						x			**MP7574J**	**Micro Pwr (401,2749)**	
				x	x		x						x			**MP7574S**	**† Micro Pwr (401,2749)**	
		66.6	—	x												**AD7581K**	**AD (3174)**	
		70	2.5 *	x						x				x		TL520	TI	
	1	2.5	1010		x										x	HS5131B	† Hybrid Sys	
					x										x	HS5131C	Hybrid Sys	10
		9	—		x	x							x	x		ZN449E-8	DDC	
					x	x							x	x		ZN449J-8	† DDC	
		80	10	x											x	**ADC0831C**	**National (3319,3322)**	
				x												**ADC0832C**	**National (3319,3322)**	
				x											x	**ADC0833C**	**National (3319,3323)**	
				x											x	**ADC0834C**	**National (3319,3322)**	
				x											x	**ADC0838C**	**National (3319,3322)**	
		100	2.5 *	x						x				x		TL521	TI	
			30	x						x				x		**ADC0817**	**†National (3319)**	
				x						x				x		ADC809	National	20
				x						x				x		ADC809	TI	
		100 *	875	x										x		ADC0804	† Intersil	
				x										x		ADC0804C	Intersil	
				x										x		**ADC0804C**	**National (3319)**	
		103	875	x										x		ADC0804	TI	
		110	875	x										x		**ADC0805C**	**National (3319)**	
				x										x		**ADC0805M**	**†National (3319)**	
		112 *	15	x						x					x	µPD7001	NEC-Micro	
		300	15 *	x						x						**TL531**	**TI (2866)**	
				x												**TL533**	**TI (2867)**	30
		2000	6.5 *	x									x		x	TC5091	Toshiba	
			300	x									x		x	TC5090	Toshiba	
	2	50	255	x										x		**ADC0800PC**	**National (3319)**	
		80	255	x										x		**ADC0800P**	**†National (3319)**	
8 (analog input for microprocessors)																		
	1/2	2.5	1350	x						x						MP20	Burr-Brown	
				x						x						MP21	Burr-Brown	
		32	50 *	x												MC14444	Motorola	
		400	1000	x						x		x				AD7583K	AD	
8 (analog to pulse width converter for microprocessor systems)																		
	1/2	—	15 *							x						MC14443	Motorola	
		32	50 *							x						MC14447	Motorola	40
			75 *							x						µA9708C	Fairchild	
										x						µA9708M	† Fairchild	
8 (D/A, A/D, with counter)																		
	1/2	500	150	x	x								x	x		**ADC-MC8BC**	**Datel (2619)**	
				x	x								x	x		ADC-MC8BM	† Datel	

Bin.—Binary
Off.—Offset
Compl.—Complementary
Magn.—Magnitude
CTC—Compl. 2's Compl.
Int. Ref.—Internal Reference
Mux. In—Multiplexed Inputs
S&H—Sample and Hold
Par. Out—Parallel Output
Ser. Out—Serial Output

IC MASTER

INTERFACE-Analog to Digital Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Conversion Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Output	Off. Bin. Output	Compl. Bin. Output	Compl. Off. Bin. Output	CTC or 2's Compl. Output	Sign. Magn. Output	Mux. In.	S&H	Integrating	Int. Ref.	Par. Out	Ser. Out	Device	Source	Line
Binary Output																	**(Cont'd)**	
9	1/2	1	500 *	x	x								x	x	x	ZN433BJ-9	† DDC	
				x	x								x	x	x	ZN433CJ-9	† DDC	
				x	x								x	x	x	ZN433J-9	† DDC	
		20	350	x	x								x	x	x	ZN432E-9	Ferranti	
			350 *	x	x								x	x		ZN432BJ-9	Ferranti	
				x	x								x	x		ZN432CJ-9	Ferranti	
				x	x								x	x		ZN432J-9	† Ferranti	
9 (video A/D converter)																		
	1/2	0.02	2500	x				x								**TDC1019J**	**TRW**	**(3438)**
10	—	3	—										x			**MAS-1202**	**AD**	**(3175)**
	1/4	18	—			x	x	x					x	x	x	**ADC1280**	**National**	**(3344)** 10
	1/2	0.8	3600	x	x			x					x	x	x	**ADC-816MC**	**Datel**	**(2619)**
				x	x			x					x	x	x	**ADC-816MM**	† **Datel**	**(2618)**
		1	500 *	x	x								x	x	x	**ADC-856C**	**Datel**	**(2621)**
				x	x								x	x	x	ADC-856M	† Datel	
				x	x								x	x	x	ZN433BJ-10	Ferranti	
				x	x								x	x	x	ZN433CJ-10	Ferranti	
				x	x								x	x	x	ZN433J-10	† Ferranti	
				x	x								x	x	x	ZN433CK-10	DDC	
				x	x								x	x	x	ZN433K-10	DDC	
		1.4	1800 *			x	x						x			**HAS-1002**	**AD**	**(3175)** 20
			3600	x	x			x					x	x	x	**ADC-826MC**	**Datel**	**(2619)**
				x	x			x					x	x	x	**ADC-826MM**	† **Datel**	**(2618)**
		1.8	755 *	x	x								x	x	x	**AD579B**	**AD**	**(3175)**
				x	x								x	x	x	**AD579K**	**AD**	**(3175)**
				x	x								x	x	x	**AD579T**	† **AD**	**(3175)**
		2.2	755 *	x	x								x	x	x	**AD579J**	**AD**	**(3175)**
		5	1400 *			x	x	x					x	x	x	MN5240-10	Micro Net	
			1600 *			x	x	x					x	x	x	DDC-5240-10	† DDC	
		6	1100			x	x	x					x	x	x	**ADC-84-10**	**Datel**	**(2619)**
						x	x	x					x	x	x	**ADC-85C-10**	**Datel**	**(2619)** 30
			1200			x	x	x					x	x	x	DDCADC87-10	DDC	
			1200 *			x	x	x					x	x	x	DDCADC85-10	DDC	
		8	1400 *			x	x	x					x	x	x	MNADC84-10	Micro Net	
						x	x	x					x	x	x	MNADC85-10	† Micro Net	
		10	1100			x	x	x					x	x	x	**ADC-87-10**	**Datel**	**(2618)**
			1500			x	x	x					x	x	x	**ADADC84-10**	**AD**	**(3175)**
						x	x	x					x	x	x	ADC84-10	Burr-Brown	
			1800			x	x	x					x	x	x	**ADADC85-10**	**AD**	**(3175)**
					x	x	x	x					x	x	x	ADC85-10	Burr-Brown	
		15	—	x									x			**AD573K**	**AD**	**(3174)** 40
				x									x			**AD573S**	† **AD**	**(3174)**
													x	x		ZN442E	Ferranti	
													x	x		ZN442J	† Ferranti	
		18	—			x	x	x					x	x	x	**ADC1080**	**National**	**(3319,3344)**
		20	350 *	x	x								x	x	x	ZN432-10	† Ferranti	
				x	x								x	x	x	ZN432B-10	Ferranti	
				x	x								x	x	x	ZN432C-10	Ferranti	
				x	x								x	x	x	ZN432E-10	Ferranti	
				x	x								x	x	x	ZN432CK-10	DDC	
				x	x								x	x	x	ZN432K-10	DDC	50

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

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INTERFACE–Analog to Digital Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Conversion Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Output	Off. Bin. Output	Compl. Bin. Output	Compl. Off. Bin. Output	CTC or 2's Compl. Output	Sign. Magn. Output	Mux. In.	S&H	Integrating	Int. Ref.	Par. Out	Ser. Out	Device	Source	Line
Binary Output																	**(Cont'd)**	
																	(Cont'd)	
10	1/2	21	800			x	x	x					x	x	x	**ADADC80-15**	**AD (3174)**	
						x	x	x					x	x	x	**ADADC80Z-10**	**† AD (3174)**	
		30	300	x	x								x	x		**AD571K**	**AD (3174)**	
				x	x								x	x		MP571K	Micro Pwr	
		120	5 *	x	x									x	x	AD7570L	AD	
				x	x									x	x	**MP7570L**	**Micro Pwr (401,2749)**	
				x	x									x	x	**MP7570S**	**† Micro Pwr (401,2749)**	
		200	—	x										x		**ADC1001B**	**National (3319)**	
				x										x		**ADC1021B**	**National (3319)**	
		5000	20 *	x	x									x		4144	Teledyne P	10
		6000	20	x	x							x		x		**ADC-EK10B**	**Datel (2619)**	
			25	x								x		x		TSC8701	Teledyne S	
				x								x		x		TSC8704	Teledyne S	
			43	x										x		**ADC-ET10BM**	**† Datel (2619)**	
			50	x										x		**ADC-ET10BC**	**Datel (2619)**	
	1	15	—	x									x			**AD573J**	**AD (3174)**	
		30	300	x	x								x	x		**AD571J**	**AD (3174)**	
				x	x								x	x		**AD571S**	**† AD (3174)**	
				x	x								x	x		MP571J	Micro Pwr	
				x	x								x	x		MP571S	† Micro Pwr	20
				x	x								x	x		**MCE571J**	**Micro Eng (4440)**	
				x	x								x	x		**MCE571S**	**† Micro Eng (4440)**	
		200	—	x										x		**ADC1001C**	**National (3319)**	
				x										x		**ADC1021C**	**National (3319)**	
10 Plus Sign																		
	1/2	80	—	x	x		x							x	x	**AD7571K**	**AD (3171,3174)**	
				x	x		x							x	x	**AD7571T**	**† AD (3171,3174)**	
	1	80	—	x	x		x							x	x	**AD7571J**	**AD (3171,3174)**	
				x	x		x							x	x	**AD7571S**	**† AD (3171,3174)**	
11	1	15	500	x	x								x	x		**HS574J**	**Hybrid Sys (2743)**	
				x	x								x	x		**HS574S**	**† Hybrid Sys (2743)**	30
12	1/2	1	1500			x	x	x					x	x	x	MN5245	Micro Net	
		2	1800 *	x	x			x					x	x	x	ADC-8516-12	DDC	
			1900	x	x			x					x	x	x	**ADC-817MC**	**Datel (2619)**	
				x	x			x					x	x	x	**ADC-817MM**	**† Datel (2618)**	
			2500			x	x	x					x	x	x	ADC00401	DDC	
		2.2	1800 *			x	x						x			**HAS-1202**	**AD (3175)**	
		3	775 *	x	x								x	x		**AD578L**	**AD (3172,3175)**	
			1900	x	x			x					x	x	x	**ADC-827MC**	**Datel (2621)**	
				x	x			x					x	x	x	**ADC-827MM**	**† Datel (2618)**	
		3.5	1.8	x	x			x					x	x	x	ADC60-12	Burr-Brown	40
		4.5	755 *	x	x								x	x	x	**AD578K**	**AD (3172,3175)**	
			775 *	x	x								x	x	x	**AD578T**	**† AD (3172,3175)**	
		5	—													**AD5240K**	**AD (3175)**	
																AD5240S	**AD (3175)**	
			1400 *			x	x	x					x	x	x	MN5240-12	Micro Net	
						x	x	x					x	x	x	4189	Teledyne P	
			1600 *			x	x	x					x	x	x	DDC-5240-12	† DDC	
			2175			x	x	x					x	x	x	ADH-8586-12	† DDC	
		6	775 *	x	x								x	x	x	**AD578J**	**AD (3172,3175)**	
				x	x								x	x	x	**AD578S**	**† AD (3172,3175)**	50
		7	1200 *			x	x	x					x	x	x	TDADC85	Teledyne P	
						x	x	x					x	x	x	TDADC87	† Teledyne P	

(Continued)

Bin.—Binary
Off.—Offset
Compl.—Complementary
Magn.—Magnitude
CTC—Compl. 2's Compl.
Int. Ref.—Internal Reference
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S&H—Sample and Hold
Par. Out—Parallel Output
Ser. Out—Serial Output

INTERFACE–Analog to Digital Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Conversion Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Output	Off. Bin. Output	Compl. Bin. Output	Compl. Off. Bin. Output	CTC or 2's Compl. Output	Sign. Magn. Output	Mux. In.	S&H	Integrating	Int. Ref.	Par. Out	Ser. Out	Device	Source	Line
Binary Output																	**(Cont'd)**	
																	(Cont'd)	
12	1/2	8	1400 *			x	x	x					x	x	x	MNADC84-12	Micro Net	
						x	x	x					x	x	x	MNADC85-12	Micro Net	
						x	x	x					x	x	x	MNADC87	Micro Net	
			1500			x	x	x					x	x	x	ADC87/MIL	† Burr-Brown	
						x	x	x					x	x	x	ADC87U	Burr-Brown	
			2000			x	x	x					x	x	x	**ADC-HZ12BGC**	**Datel (2619)**	
						x	x	x					x	x	x	**ADC-HZ12BMM**	**† Datel (2618)**	
		9	2150			x	x				x		x	x	x	ADC-HS12BMC	Datel	
						x	x				x		x	x	x	**ADC-HS12BMM**	**† Datel (2618)**	
		9 *	2845	x	x					x	x		x	x		**HDAS-16MC**	**Datel (2623)**	10
				x	x					x	x		x	x		**HDAS-16MM**	**† Datel (2620)**	
				x	x					x	x		x	x		**HDAS-8MC**	**Datel (2623)**	
				x	x					x	x		x	x		**HDAS-8MM**	**† Datel (2620)**	
		10	1100			x	x	x					x	x	x	ADC-84-12	Datel	
						x	x	x					x	x	x	ADC-85-12	Datel	
						x	x	x					x	x	x	ADC-85C-12	Datel	
					x	x	x	x					x	x	x	ADC-87-12	Datel	
			1200			x	x	x					x	x	x	**HSADC85B**	**† Hybrid Sys (2744)**	
						x	x	x					x	x	x	**HSADC85C**	**Hybrid Sys (2744)**	
			1200 *			x	x	x					x	x	x	DDCADC85-12	DDC	20
						x	x	x					x	x	x	DDCADC87-12	DDC	
			1550			x	x	x					x	x	x	**ADADC84-12**	**AD (3175)**	
						x	x	x					x	x	x	ADC84-12	Burr-Brown	
			1575			x	x	x					x	x	x	ADH-8585-12	† DDC	
			1800			x	x	x					x	x	x	**ADADC85-12**	**AD (3175)**	
						x	x	x					x	x	x	ADC85-12	Burr-Brown	
			2000	x				x					x	x	x	**HI5712-2**	**† Harris (2704,3288,3291)**	
				x				x					x	x	x	**HI5712-5**	**Harris (2704,3288,3291)**	
				x				x					x	x	x	**HI5712-7**	**Harris (2704,3288,3291)**	
				x				x					x	x	x	**HI5712-8**	**† Harris (2704,3288,3291)**	30
				x				x					x	x	x	**HI5712A-2**	**† Harris (2704,3288,3291)**	
				x				x					x	x	x	**HI5712A-7**	**Harris (2704,3288,3291)**	
				x				x					x	x	x	**HI5712A-8**	**† Harris (2704,3288,3291)**	
		13	744			x	x							x	x	**ADC-5213**	**Datel (2621)**	
						x	x							x	x	**ADC-5213E**	**Datel (2621)**	
						x	x							x	x	**ADC-5213H**	**† Datel (2618,2621)**	
						x	x							x	x	**ADC-5214**	**Datel (2621)**	
						x	x							x	x	**ADC-5214E**	**Datel (2621)**	
						x	x							x	x	**ADC-5214H**	**† Datel (2618,2621)**	
						x	x							x	x	**ADC-5215**	**Datel (2621)**	40
						x	x							x	x	**ADC-5215E**	**Datel (2621)**	
						x	x							x	x	**ADC-5215H**	**† Datel (2618,2621)**	
			745	x										x	x	MN5213	Micro Net	
				x										x	x	MN5213H	† Micro Net	
						x								x	x	MN5214	Micro Net	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Analog to Digital Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Conversion Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Output	Off. Bin. Output	Compl. Bin. Output	Compl. Off. Bin. Output	CTC or 2's Compl. Output	Sign. Magn. Output	Mux. In.	S&H	Integrating	Int. Ref.	Par. Out	Ser. Out	Device	Source	Line
Binary Output																	**(Cont'd)**	
12	1/2	13	745														(Cont'd)	
							x							x	x	MN5214H	† Micro Net	
							x							x	x	MN5215	Micro Net	
							x							x	x	MN5215H	† Micro Net	
			915			x	x						x	x	x	**ADC-5210**	**Datel (2621)**	
						x	x						x	x	x	**ADC-5210E**	**Datel (2621)**	
						x	x						x	x	x	**ADC-5210H**	**† Datel (2618,2621)**	
						x	x						x	x	x	**ADC-5211**	**Datel (2621)**	
						x	x						x	x	x	**ADC-5211E**	**Datel (2621)**	
						x	x						x	x	x	**ADC-5211H**	**† Datel (2618,2621)**	
						x	x						x	x	x	**ADC-5212**	**Datel (2621)**	10
						x	x						x	x	x	**ADC-5212E**	**Datel (2621)**	
						x	x						x	x	x	**ADC-5212H**	**† Datel (2618,2621)**	
						x	x						x	x	x	**ADC-5216**	**Datel (2621)**	
						x	x						x	x	x	**ADC-5216E**	**Datel (2621)**	
						x	x							x	x	**ADC-5216H**	**† Datel (2618,2621)**	
						x							x	x	x	ADC582B-12	† Hybrid Sys	
						x							x	x	x	ADC582C-12	Hybrid Sys	
						x	x						x	x	x	DDC-5210-1	† DDC	
						x	x						x	x	x	DDC-5211-1	† DDC	
						x	x						x	x	x	DDC-5212-1	† DDC	20
						x	x						x	x	x	DDC-5216-1	† DDC	
						x	x						x	x	x	DDC5210-3	DDC	
						x	x						x	x	x	DDC5211-3	DDC	
						x	x						x	x	x	DDC5212-3	DDC	
						x	x						x	x	x	DDC5216-3	DDC	
						x	x						x	x	x	MN5210	Micro Net	
						x	x						x	x	x	MN5210H	† Micro Net	
						x	x						x	x	x	MN5211	Micro Net	
						x	x						x	x	x	MN5211H	† Micro Net	
						x	x						x	x	x	MN5212	Micro Net	30
						x	x						x	x	x	MN5212H	† Micro Net	
						x	x						x	x	x	MN5216	Micro Net	
						x	x						x	x	x	MN5216H	† Micro Net	
						x	x						x	x	x	TP5210	† Teledyne P	
			1000	x									x	x	x	**AD5210**	**AD (3174)**	
							x						x	x	x	**AD5211**	**AD (3174)**	
							x						x	x	x	AD5212	AD	
				x										x	x	AD5213	AD	
							x							x	x	**AD5214**	**AD (3174)**	
							x							x	x	AD5215	AD	40
						x							x	x	x	AD5216	AD	
		15	500	x	x								x	x		**HS574K**	**Hybrid Sys (2743)**	
				x	x								x	x		**HS574L**	**Hybrid Sys (2743)**	
		20	725			x	x	x					x	x	x	ADC581B-12	† Hybrid Sys	
						x	x	x					x	x	x	ADC581C-12	Hybrid Sys	
			2000			x	x	x					x	x	x	**ADC-HX12BGC**	**Datel (2619)**	
						x	x	x					x	x	x	**ADC-HX12BMM**	**† Datel (2618)**	
		25	360 *	x	x								x		x	**HI574A**	**Harris (2712)**	
			725	x	x								x		x	**AD574AK**	**AD (3174)**	
			800			x	x	x					x	x	x	**ADADC80-12**	**AD (3174)**	50
						x	x	x					x	x	x	**ADADC80Z-12**	**† AD (3174)**	
			925	x	x			x					x	x	x	**AD572A**	**AD (3174)**	

(Continued)

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Ser. Out—Serial Output

IC MASTER

INTERFACE–Analog to Digital Converters (Cont'd)

Binary Output (Cont'd)

Bits Res.	Linearity Error ±LSB	Conversion Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Output	Off. Bin. Output	Compl. Bin. Output	Compl. Off. Bin. Output	CTC or 2's Compl. Output	Sign. Magn. Output	Mux. In.	S&H	Integrating	Int. Ref.	Par. Out	Ser. Out	Device	Source		Line
																		(Cont'd)	
12	1/2	25	925	x	x			x					x	x	x	**AD572B**	**AD**	**(3174)**	
				x	x			x					x	x	x	**AD572S**	**†AD**	**(3174)**	
			950 *			x	x	x					x	x	x	ADC80-12	Burr-Brown		
						x	x	x					x	x	x	ADC80A-12	Burr-Brown		
		30	—	x	x			x			x					HI5812	Harris		
			780	x	x								x		x	**AD574K**	**AD**	**(3174)**	
				x									x		x	**AD574L**	**AD**	**(3174)**	
				x	x								x		x	**AD574S**	**†AD**	**(3174)**	
				x	x								x		x	**AD574T**	**†AD**	**(3174)**	
				x									x		x	**AD574U**	**†AD**	**(3174)**	10
				x	x								x		x	MCD574K	Micro Eng		
				x									x		x	**MCE574L**	**Micro Eng**	**(4440)**	
				x	x								x		x	**MCE574S**	**†Micro Eng**	**(4440)**	
				x	x								x		x	**MCE574T**	**†Micro Eng**	**(4440)**	
				x									x		x	**MCE574U**	**†Micro Eng**	**(4440)**	
		35	620	x	x								x		x	**AD574ZL**	**AD**	**(3174)**	
				x	x								x		x	**AD574ZS**	**†AD**	**(3174)**	
				x	x								x		x	**AD574ZT**	**†AD**	**(3174)**	
				x	x								x		x	**AD574ZU**	**†AD**	**(3174)**	
				x	x								x		x	**MCE574ZL**	**Micro Eng**	**(4440)**	20
				x	x								x		x	**MCE574ZS**	**†Micro Eng**	**(4440)**	
				x	x								x		x	**MCE574ZT**	**†Micro Eng**	**(4440)**	
				x	x								x		x	**MCE574ZU**	**Micro Eng**	**(4440)**	
		50	725	x										x	x	**AD504B**	**AD**	**(3153)**	
				x									x	x	x	AD5201B	AD		
				x									x	x	x	AD5201T	† AD		
				x									x	x	x	AD5202B	AD		
				x									x	x	x	AD5202T	† AD		
				x										x	x	AD5204T	† AD		
				x										x	x	AD5205B	AD		30
				x										x	x	AD5205T	† AD		
			745	x										x	x	MN5203	Micro Net		
				x										x	x	MN5203H	† Micro Net		
							x							x	x	MN5204	Micro Net		
							x							x	x	MN5204H	† Micro Net		
							x							x	x	MN5205	Micro Net		
							x							x	x	MN5205H	† Micro Net		
			770	x	x			x					x	x	x	ADC10HT	† Burr-Brown		
			915			x	x						x	x	x	DDC-5200-1	† DDC		
						x	x						x	x	x	DDC-5201-1	† DDC		40
						x	x						x	x	x	DDC-5202-1	† DDC		
						x	x						x	x	x	DDC-5206-1	† DDC		
						x	x						x	x	x	DDC5200-3	DDC		
						x	x						x	x	x	DDC5201-3	DDC		
						x	x						x	x	x	DDC5202-3	DDC		
						x	x						x	x	x	DDC5206-3	DDC		
				x									x	x	x	MN5200	Micro Net		
				x									x	x	x	MN5200H	† Micro Net		
							x						x	x	x	MN5201	Micro Net		
							x						x*	x	x	MN5201H	† Micro Net		50
							x						x	x	x	MN5202	Micro Net		
							x						x	x	x	MN5202H	† Micro Net		
						x							x	x	x	MN5206	Micro Net		
						x							x	x	x	MN5206H	† Micro Net		
			1000				x						x	x	x	AD5201	AD		

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

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INTERFACE–Analog to Digital Converters (Cont'd)

Binary Output (Cont'd)

Bits Res.	Linearity Error ±LSB	Conversion Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Output	Off. Bin. Output	Compl. Bin. Output	Compl. Off. Bin. Output	CTC or 2's Compl. Output	Sign. Magn. Output	Mux. In.	S&H	Integrating	Int. Ref.	Par. Out	Ser. Out	Device	Source		Line
12	1/2	50	1000				x						x	x	x	AD5202	AD		
				x										x	x	AD5203	AD		
							x							x	x	AD5204	AD		
							x							x	x	AD5205	AD		
						x							x	x	x	AD5206	AD		
		175	80	x									x	x	x	MN5250	Micro Net		
				x									x	x	x	MN5250H	† Micro Net		
							x						x	x	x	MN5251	Micro Net		
							x						x	x	x	MN5251H	† Micro Net		
							x						x	x	x	MN5252	Micro Net		10
							x						x	x	x	MN5252H	† Micro Net		
						x							x	x	x	MN5253	Micro Net		
						x							x	x	x	MN5253H	† Micro Net		
		200	210	x										x	x	**ADC1210**	**National**	**(3344)**	
				x										x	x	**ADC1210C**	**National**	**(3344)**	
		250	311													MN5700	Micro Net		
		300	112	x	x			x					x	x	x	**ADC-HC12BMC**	**Datel**	**(2619)**	
				x	x			x					x	x	x	**ADC-HC12BMM**	**† Datel**	**(2618)**	
		2400	43	x										x		**ADC-ET12BM**	**† Datel**	**(2619)**	
		5000	15	x										x		µPD7002	NEC-Micro		20
		20000	20	x	x									x		4145	Teledyne P		
		24000	20	x	x							x		x		**ADC-EK12B**	**Datel**	**(2619)**	
			25	x								x		x		TSC8702	Teledyne S		
				x								x		x		TSC8705	Teledyne S		
		100000	20	x					x			x	x	x		ICL7109	Intersil		
				x					x			x	x	x	x	**TSC7109C**	**Teledyne S**	**(2847)**	
				x					x			x	x	x	x	**TSC7109M**	**† Teledyne S**	**(2847)**	
	1	2	2700	x	x			x					x	x	x	ADH-8516-11	DDC		
		5	1600 *			x	x	x					x	x	x	DDC-5240-12	† DDC		
		15	500	x	x								x	x		**HS574T**	**† Hybrid Sys**	**(2743)**	30
				x	x								x	x		**HS574U**	**† Hybrid Sys**	**(2743)**	
		25	390	x									x			**MCE574AS**	**† Micro Eng**	**(4440)**	
			725	x	x								x			**AD574AJ**	**AD**	**(3174)**	
				x	x								x			**AD574AS**	**† AD**	**(3174)**	
		30	780	x	x								x		x	**AD574J**	**AD**	**(3174)**	
				x	x								x		x	**MCE574J**	**Micro Eng**	**(4440)**	
		35	620	x	x								x		x	**AD574ZJ**	**AD**	**(3174)**	
				x	x								x		x	**AD574ZK**	**AD**	**(3174)**	
				x	x								x		x	**MCE574ZJ**	**Micro Eng**	**(4440)**	
				x	x								x		x	**MCE574ZK**	**Micro Eng**	**(4440)**	40
		50	725	x									x	x	x	AD5201A	AD		
				x									x	x	x	AD5201S	† AD		
				x									x	x	x	AD5202A	AD		
				x									x	x	x	AD5202S	† AD		
				x										x	x	AD5204A	AD		
				x										x	x	AD5204S	† AD		
				x										x	x	AD5205A	AD		
				x										x	x	AD5205S	† AD		
	1 1/2	2400	50	x										x		**ADC-ET12BC**	**Datel**	**(2619)**	
	2	3	2175			x	x	x					x	x	x	ADH-8586-10	† DDC		50

(Continued)

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ADVERTISERS INDEX

IC MASTER

INTERFACE–Analog to Digital Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Conversion Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Output	Off. Bin. Output	Compl. Bin. Output	Compl. Off. Bin. Output	CTC or 2's Compl. Output	Sign. Magn. Output	Mux. In.	S&H	Integrating	Int. Ref.	Par. Out	Ser. Out	Device	Source	Line
Binary Output																	**(Cont'd)**	
12	2																(Cont'd)	
		6	1575			x	x	x					x	x	x	ADH-8585-10 †	DDC	
		200	210	x										x	x	**ADC1211**	**† National (3344)**	
				x										x	x	**ADC1211C**	**National (3344)**	
12 Plus Sign																		
	—	160 ms	—	x												**AD7552**	**AD (3174)**	
12 Plus Sign (2 device set)																		
	1/2	36000	—	x					x					x	x	ADB1200C	National	
12 (2 device set)																		
	1/2	15	785	x									x	x	x	**HS5210B**	**† Hybrid Sys (2744)**	
				x									x	x	x	**HS5210C**	**Hybrid Sys (2744)**	
				x									x	x	x	**HS5211B**	**† Hybrid Sys (2744)**	
				x									x	x	x	**HS5211C**	**Hybrid Sys (2744)**	
				x									x	x	x	**HS5212B**	**† Hybrid Sys (2744)**	10
				x									x	x	x	**HS5212C**	**Hybrid Sys (2744)**	
				x										x	x	**HS5213B**	**† Hybrid Sys (2744)**	
				x										x	x	**HS5213C**	**Hybrid Sys (2744)**	
				x										x	x	**HS5214B**	**† Hybrid Sys (2744)**	
				x										x	x	**HS5214C**	**Hybrid Sys (2744)**	
				x										x	x	**HS5215B**	**† Hybrid Sys (2744)**	
				x										x	x	**HS5215C**	**Hybrid Sys (2744)**	
				x									x	x	x	**HS5216B**	**† Hybrid Sys (2744)**	
				x									x	x	x	**HS5216C**	**Hybrid Sys (2744)**	
		250000	40	x					x			x	x	x		ICL7104-12	Intersil	20
			360	x					x			x	x	x		ICL8052A	Intersil	
12 (3-Digit BCD)																		
	1/4	1200	20									x		x		ADC-EK12DC	Datel	
												x		x		ADC-EK12DM	† Datel	
	1	6000 *	50									x	x		x	AD2020	AD	
13	1/2	40000 *	64					x						x		**MP7550B**	**Micro Pwr (401,2749)**	
			72					x				x		x	x	**AD7550B**	**AD (3174)**	
14	1/2	250	300				x						x	x	x	MN5260	Micro Net	
14 (2 device set)																		
	1/2	250000	40	x					x			x	x	x		ICL7104-14	Intersil	
			360	x					x			x	x	x		ICL8052A	Intersil	
14 (3 1/2-Digit BCD)																		
	1/2	10000	20											x		4146	Teledyne P	30
15	2	400000	20	x					x						x	**TSC800AC**	**Teledyne S (2853)**	
				x					x						x	**TSC800AM**	**† Teledyne S (2853)**	
	4	400000	20	x					x						x	**TSC800BC**	**Teledyne S (2853)**	
				x					x						x	**TSC800BM**	**† Teledyne S (2853)**	
16	1/2	100	1200	x	x			x						x		HS9516-4	Hybrid Sys	
		170	2500	x	x			x					x	x	x	ADC731K	Burr-Brown	
				x	x			x					x	x	x	ADC73K	Burr-Brown	
	1	15	—													ADC76	Burr-Brown	
		50	—	x		x	x	x						x	x	**ADADC71K**	**AD (3173)**	
				x		x	x	x						x	x	**ADADC72K**	**AD (3173)**	40
		100	1200	x	x			x						x		HS9516-5	Hybrid Sys	
		170	2500	x	x			x					x	x	x	ADC731J	Burr-Brown	
				x	x			x					x	x	x	ADC73J	Burr-Brown	
	1 *	17	1550			x	x	x					x	x	x	PCM75K	Burr-Brown	
	2	50	—	x		x	x	x						x	x	**ADADC71J**	**AD (3173)**	
				x		x	x	x						x	x	**ADADC72J**	**AD (3173)**	
			1800 *			x	x	x					x	x	x	ADC71K	Burr-Brown	
						x	x	x					x	x	x	ADC72	Burr-Brown	
		100	1200	x	x			x						x		HS9516-6	Hybrid Sys	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Analog to Digital Converters (Cont'd)

Binary Output (Cont'd)

Bits Res.	Linearity Error ±LSB	Conversion Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Output	Off. Bin. Output	Compl. Bin. Output	Compl. Off. Bin. Output	CTC or 2's Compl. Output	Sign. Magn. Output	Mux. In.	S&H	Integrating	Int. Ref.	Par. Out	Ser. Out	Device	Source	Line
16																(Cont'd)		
	2 *	17	1550			x	x	x					x	x	x	PCM75J	Burr-Brown	
	4	50	1440			x	x	x					x	x	x	MN5282	Micro Net	
		100	1440			x	x	x					x	x	x	MN5280	Micro Net	
	8	50	1800 *			x	x	x					x	x	x	ADC71J	Burr-Brown	
16 (2 device set)																		
	1/2	250000	40	x					x			x	x	x		ICL7104-16	Intersil	
			360	x					x			x	x	x		ICL8052A	Intersil	

Bin.—Binary
Off.—Offset
Compl.—Complementary
Magn.—Magnitude
CTC—Compl. 2's Compl.
Int. Ref.—Internal Reference
Mux. In—Multiplexed Inputs
S&H—Sample and Hold
Par. Out—Parallel Output
Ser. Out—Serial Output

IC MASTER

INTERFACE–Analog to Digital Converters (Cont'd)

Digits	Device	Source	Line
Decimal Output			
3 1/2 Digits, Integrating	ICL7106	Intersil	
	ICL7107	Intersil	
	ICL7116	Intersil	
	ICL7117	Intersil	
	ICL7126	Intersil	
	MP7138	**Micro Pwr (401,2749)**	
	MP7138A	**Micro Pwr (401,2749)**	
	MC14433	Motorola	
	ADC3511	National	
	ADD3501	National	10
	14433	Teledyne S	
	14433A	Teledyne S	
	TSC7106	Teledyne S	
	TSC7107	Teledyne S	
	TSC7116	Teledyne S	
	TSC7117	Teledyne S	
	TSC7126	**Teledyne S (2848)**	
3 Digits, Dual Slope, Building Block, for Microprocessor Systems, e.g. TMS1000	TL505C	TI	
3 Digits, Dual Slope, 2 Device Sets	**CA3161**	**RCA (3361)**	
	CA3162	**RCA (3356)**	20
3 1/2 Digits, Drives LCD DVM Display	ZN450	Ferranti	
	ZN451	Ferranti	
3 1/2 Digits, Integrating, 2 Device Sets	ICL7101	Intersil	
	ICL7103	Intersil	
	ICL8052	Intersil	
	ICL8053	Intersil	
	ICL8068	Intersil	
	LD110	Siliconix	
	LD111A	Siliconix	
3 1/2 Digits, Dual Slope	TSC8751	Teledyne S	30
3 1/2—4 1/2 Digits, Ramp type, 2 Device Sets	MC1405	Motorola	
	MC14435	Motorola	
	MC14435E	† Motorola	
	MC1505	† Motorola	
3 1/2	TSC8750	Teledyne S	
3 3/4 Digits, Integrating	ZNA216E	Ferranti	
	ZNA216J	† Ferranti	
	ADC3711	National	
	ADD3701	National	
4 1/2 Digits, Dual Slope	ICL7135	Intersil	40
	TSC7135	**Teledyne S (2850)**	
4 1/2 Digits, Dual Slope, 2 Device Sets	ICL7103A	Intersil	
	ICL8053A	Intersil	
	ICL8068A	Intersil	
	ADB4500	National	
	LF13300	National	
	LD120	Siliconix	
	LD121A	**Siliconix (2817)**	
	LD122	**Siliconix (2817)**	

† Military Temperature Range (−55° to 125°C)

* Typical Value

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INTERFACE–Digital to Analog Converters

D/A Converters

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source	Line
Dual 8-Bit, Data Latches, Addressable																		
	1	—	1350	x						x			x		x	MP10	Burr-Brown	
				x						x			x		x	MP11	Burr-Brown	
4	1/4	0.3	85		x					x	X		x			ZN434E	Ferranti	
4 (video digital converter)																		
	1/2	0.004	1040	x								x				**HDG-0405**	**AD (3169)**	
6	1/8	3	250			x	x			x			x			MP550Z	† Micro Pwr	
						x	x			x			x			DAC-01A	† PMI	
	1/4	3	250			x	x			x			x			DAC-01	Micro Pwr	
						x	x			x			x			DAC-01B	† Micro Pwr	
						x	x			x			x			DAC-01C	Micro Pwr	
						x	x			x			x			DAC-01D	Micro Pwr	10
						x	x			x			x			DAC-01F	† Micro Pwr	
						x	x			x			x			DAC-01H	Micro Pwr	
						x	x	x		x			x			**MP5520A**	**† Micro Pwr (401,2749)**	
						x	x	x		x			x			**MP5520B**	**† Micro Pwr (401,2749)**	
						x	x	x		x			x			**MP5520C**	**Micro Pwr (401,2749)**	
						x	x	x		x			x			**MP5520F**	**† Micro Pwr (401,2749)**	
						x	x	x		x			x			**MP5520H**	**Micro Pwr (401,2749)**	
						x	x									µPC603	NEC-Electron	
						x	x			x			x			DAC-01	† PMI	
						x	x			x			x			DAC-01B	† PMI	20
						x	x			x			x			DAC-01C	PMI	
						x	x			x			x			DAC-01F	† PMI	
						x	x			x			x			DAC-01H	PMI	
						x	x			x			x			DAC-206A	† PMI	
						x	x			x			x			DAC-206B	† PMI	
						x	x			x			x			DAC-206E	PMI	
						x	x			x			x			DAC-206F	PMI	
	1/2	0.3	240			x	x							x		**MC1406**	**Motorola (2759)**	
						x	x							x		**MC1506**	**† Motorola (2759)**	
		1 *	45 *	x						x	x		x			ZN426E-6	Ferranti	30
		3	200			x	x	x		x			x			**MP5520D**	**Micro Pwr (401,2749)**	
			250			x	x			x			x			DAC-01D	PMI	
6 (A/D,D/A,with counter)																		
	1/2	2.0	175	x						x	x		x			ZN425E-6	Ferranti	
6 (video digital converter)																		
	1/2	0.006	1350	x								x				**HDG-0605**	**AD (3169)**	
6/12-Binary Serial																		
	1/2	—	5							x	x			x	x	µA9706C	Fairchild	
7	1/2	1 *	45 *	x						x	x		x			ZN426E-7	Ferranti	
				x						x	x		x			ZN429E-7	Ferranti	
7 (A/D,D/A,with counter)																		
	1/2	2.0	175	x						x	x		x			ZN425E-7	Ferranti	
8	—	0.005	—	x								x	x	x		**AD9768**	**† AD (3162,3169)**	
	1/16 *	0.04 *	450	x						x				x		HI5609-2	† Harris	40
				x						x				x		HI5609-5	Harris	
				x						x				x		HI5609-8	† Harris	
	1/8	0.04 *	450	x						x				x		HI5607-2	† Harris	
				x						x				x		HI5607-5	Harris	
				x						x				x		HI5607-8	† Harris	
				x						x				x		HI5608-2	† Harris	

(Continued)

Bin.—Binary
Off.—Offset
Compl.—Complementary
Magn.—Magnitude
Int Ref.—Internal Reference
CTC—Compl. 2's Compl.
Mult.—Multiplying

IC MASTER

INTERFACE-Digital to Analog Converters (Cont'd)

D/A Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source	Line
																	(Cont'd)	
8	1/8	0.04 *	450	x						x				x		HI5608-5	Harris	
				x						x				x		HI5608-8	† Harris	
		0.15	1.5 *	x	x	x	x				x			x		**AD7523L**	**AD (3164)**	
				x	x	x	x				x			x		AD7523L	Intersil	
				x	x	x	x				x			x		AD7523U	† Intersil	
				x	x	x	x				x			x		**MP7523L**	**Micro Pwr (401,2749)**	
		0.15 *	20 *	x	x					x	x			x	x	**AD7524C**	**AD (3164)**	
				x	x	x	x				x			x	x	**AD7524L**	**AD (3164)**	
				x	x	x	x			x	x			x	x	**AD7524U**	**† AD (3164)**	
				x	x	x	x				x			x	x	**MP7524L**	**Micro Pwr (401,2749)**	10
				x	x	x	x				x			x	x	**MP7524U**	**† Micro Pwr (401,2749)**	
			670	x	x	x	x				x			x		AD7523J	Intersil	
				x	x	x	x				x			x		AD7523S	† Intersil	
		1	30	x						x	x			x		**DAC0830**	**National (3320)**	
		1 *	—	x						x	x		x			ZN438	Ferranti	
	1/4	0.01	850	x								x				**HDS-0810E**	**AD (3169)**	
				x								x				**HDS-0810EM**	**† AD (3169)**	
				x								x				**MC10318-9**	**Motorola (2759)**	
		0.045	700	x							x	x				**HI5618A-2**	**† Harris (2686,3288)**	
				x							x	x				**HI5618A-5**	**Harris (2686,3288)**	20
		0.085	33	x	x	x	x			x	x	x		x		DAC-080QF	AMD	
		0.135	174	x	x	x	x			x	x	x		x		DAC-08A	† AMD	
				x	x	x	x			x	x	x		x		ADDAC-08A	† AD	
					x	x	x			x	x	x		x		ADDAC-08H	AD	
				x	x	x	x			x	x	x		x		DAC-08A	† Motorola	
				x	x	x	x			x	x	x		x		DAC-08H	Motorola	
				x	x	x	x			x	x	x		x		**DAC0800A**	**† National (3320)**	
				x	x	x	x			x				x		**DAC0802**	**† National (3320)**	
				x	x	x	x			x				x		**DAC0802C**	**National (3320)**	
				x	x	x	x			x	x	x		x		DAC-08A	† PMI	30
				x	x	x	x			x	x	x		x		DAC-08H	PMI	
				x	x	x	x			x	x	x		x		DAC-08A	† Raytheon	
				x	x	x	x			x	x	x		x		DAC-08H	Raytheon	
				x	x	x	x			x	x	x		x		DAC-08A	† Signetics	
				x	x	x	x			x	x	x		x		DAC-08H	Signetics	
		0.15	1.5 *	x	x	x	x				x			x		**AD7523K**	**AD (3164)**	
				x	x	x	x				x			x		AD7523K	Intersil	
				x	x	x	x				x			x		AD7523T	† Intersil	
				x	x	x	x				x			x		**MP7523K**	**Micro Pwr (401,2749)**	
		0.15 *	20 *	x	x					x	x			x	x	**AD7524B**	**AD (3164)**	40
				x	x	x	x			x	x			x	x	**AD7524K**	**AD (3164)**	
				x	x	x	x			x	x			x	x	**AD7524T**	**† AD (3164)**	
				x	x	x	x				x			x	x	**MP7524K**	**Micro Pwr (401,2749)**	
				x	x	x	x				x			x	x	**MP7524T**	**† Micro Pwr (401,2749)**	
		0.16 *	123(5V)	x	x	x	x	x		x	x			x	x	AM6080AC	AMD	
				x	x	x	x	x		x	x			x	x	AM6080AM	† AMD	
				x	x	x	x	x	x	x	x			x	x	AM6081AC	AMD	
				x	x	x	x	x	x	x	x			x	x	AM6081AM	† AMD	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

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INTERFACE–Digital to Analog Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB μS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source		Line
D/A Converters																		**(Cont'd)**	
																		(Cont'd)	
8	1/4	0.2 *	255 *	x						x	x	x	x	x	x	NE5119	Signetics		
				x						x	x	x	x	x	x	SE5119	† Signetics		
			1300 *			x	x				x	x		x		**HDH-0802**	**AD**	**(3169)**	
						x	x				x	x		x		**HDH-0802M**	**†AD**	**(3169)**	
		0.25	170	x	x					x				x	x	DAC888A	† PMI		
				x	x					x				x	x	DAC888E	PMI		
		0.25 *	265	x	x					x	x			x		**AD1408-9**	**AD**	**(3164)**	
				x	x					x	x			x		**AD1508-9**	**†AD**	**(3164)**	
		0.5	120 *	x									x	x		DAC-808	PMI		
		1	30	x						x	x			x		**DAC0831**	**National**	**(3320)**	10
		1.5	375	x						x	x		x		x	**AD558K**	**AD**	**(3164)**	
		2 *	255	x						x	x	x	x	x	x	NE5019	Signetics		
				x						x	x	x	x	x	x	SE5019	† Signetics		
		20 *	735 *	x	x						x	x				**HDS-0820**	**AD**	**(3169)**	
				x	x						x	x				**HDS-0820M**	**†AD**	**(3169)**	
	3/8	1.5	375	x						x	x		x		x	**AD558T**	**†AD**	**(3164)**	
	1/2	0.005	—									x		x		SP9768	Plessey		
		0.01	450	x		x				x					x	**TDC1016-8**	**TRW**	**(3438)**	
		0.01 *	675	x								x				**MC10318**	**Motorola**	**(2759)**	
		0.025	630	x	x					x			x			**DAC-HF8BMM**	**† Datel**	**(2620)**	20
				x	x					x			x			DAC-HFBMC	Datel		
		0.045	700	x						x	x					**HI5618B-2**	**† Harris**	**(2686,3288)**	
				x						x	x					**HI5618B-5**	**Harris**	**(2686,3288)**	
		0.12	240			x	x			x			x			DAC90B	Burr-Brown		
						x	x			x			x			DAC90S	† Burr-Brown		
			255	x						x	x	x	x	x	x	NE5118	Signetics		
				x						x	x	x	x	x	x	SE5118	† Signetics		
		0.135	174	x	x	x	x			x	x	x		x		DAC-08	† AMD		
				x	x	x	x			x	x	x		x		**ADDAC-08**	**†AD**	**(3164)**	
				x	x	x				x	x	x		x		μA0801	† Fairchild		30
				x	x	x	x			x	x	x		x		DAC-08	† Motorola		
				x	x	x				x				x		**DAC0800**	**†National**	**(3320)**	
				x	x	x	x			x	x	x		x		DAC-08	† PMI		
				x	x	x	x			x	x	x		x		DAC-08	† Raytheon		
				x	x	x	x			x	x	x		x		DAC-08	† Signetics		
			570	x						x			x			MN3015	Micro Net		
				x						x			x			MN3015H	† Micro Net		
		0.14 *	130 *	x	x					x			x		x	**MC6890A**	**†Motorola**	**(2758)**	
		0.15	1.5 *	x	x	x	x				x			x		**AD7523J**	**AD**	**(3164)**	
				x	x	x	x				x			x		**AD7523S**	**†AD**	**(3164)**	40
				x	x	x	x				x			x		**MP7523J**	**Micro Pwr**	**(401,2749)**	
			136	x	x					x	x	x		x		**DAC-08BC**	**Datel**	**(2621)**	
				x	x					x	x	x		x		DAC-08BM	† Datel		
			174	x	x	x	x			x	x	x		x		DAC-08E	AMD		
				x	x	x	x			x	x	x		x		ADDAC-08E	AD		
				x	x	x	x			x	x	x		x		μA0801E	Fairchild		
				x	x	x	x			x	x	x		x		DAC-08E	Motorola		
				x	x	x				x				x		**DAC0800C**	**National**	**(3320)**	
				x	x	x				x				x		μPC624	NEC-Electron		
				x	x	x	x			x	x	x		x		DAC-08E	PMI		50
				x	x	x	x			x	x	x		x		DAC-08E	Raytheon		
				x	x	x	x			x	x	x		x		DAC-08E	Signetics		

(Continued)

Bin.—Binary
Off.—Offset
Compl.—Complementary
Magn.—Magnitude
Int Ref.—Internal Reference
CTC—Compl. 2's Compl.
Mult.—Multiplying

IC MASTER

INTERFACE-Digital to Analog Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source		Line
D/A Converters																		**(Cont'd)**	
																		(Cont'd)	
8	1/2																		
		0.15 *	20 *	x	x					x	x			x	x	**AD7524A**	**AD**	**(3164)**	
				x	x	x	x				x			x	x	**AD7524J**	**AD**	**(3164)**	
				x	x	x	x				x			x	x	**AD7524S**	**†AD**	**(3164)**	
				x	x	x	x				x			x	x	**MP7524J**	**Micro Pwr**	**(401,2749)**	
				x	x	x	x				x			x	x	**MP7524S**	**†Micro Pwr**	**(401,2749)**	
			305	x						x	x			x		**DAC0808**	**†National**	**(3320)**	
				x						x	x			x		**DAC0808C**	**National**	**(3320)**	
		0.16 *	123	x	x	x	x	x		x	x			x	x	AM6080C	AMD		
				x	x	x	x	x		x	x			x	x	AM6080M	† AMD		
				x	x	x	x	x	x	x	x			x	x	AM6081C	AMD		10
				x	x	x	x	x	x	x	x			x	x	AM6081M	† AMD		
		0.20 *	130 *	x	x					x			x		x	**MC6890**	**Motorola**	**(2758)**	
		0.22	20 *	x	x					x	x			x	x	**AD7528K**	**AD**	**(3164)**	
				x	x					x	x			x	x	**AD7528L**	**AD**	**(3164)**	
				x	x					x	x			x	x	**AD7528T**	**†AD**	**(3164)**	
				x	x					x	x			x	x	**AD7528U**	**†AD**	**(3164)**	
		0.25	170	x	x					x				x	x	DAC888B	† PMI		
				x	x					x				x	x	DAC888F	PMI		
		0.25 *	265	x						x	x			x		SSS1408A-8	AMD		
				x						x	x			x		SSS1508A-8	† AMD		20
				x	x					x	x			x		**AD1408-8**	**AD**	**(3164)**	
				x	x					x	x			x		**AD1508-8**	**†AD**	**(3164)**	
				x	x					x	x			x		DAC-1408A-8	PMI		
				x	x					x	x			x		DAC-1508A-8	† PMI		
		0.25/1.0	900			x	x	x		x			x	x		DAC82K	Burr-Brown		
						x	x	x		x			x	x		DAC82S	† Burr-Brown		
		0.3 *	305	x						x	x			x		1408-8	AMD		
				x						x	x			x		1508-8	† AMD		
				x	x					x	x			x		**DAC-IC8BC**	**Datel**	**(2621)**	
				x	x					x	x			x		DAC-IC8BM	† Datel		30
				x						x	x			x		µA0802	† Fairchild		
				x						x	x			x		µA0802A	Fairchild		
				x										x		**MC1408-8**	**Motorola**	**(2759)**	
				x										x		**MC1508-8**	**†Motorola**	**(2759)**	
				x						x				x		LM1408-8	National		
				x						x				x		LM1508-8	† National		
				x						x				x		MC1408-8	Signetics		
				x						x				x		MC1508-8	† Signetics		
		0.375	300	x	x	x				x			x			DAC-100C	Micro Pwr		
		0.6 *	500	x		x				x			x		x	**XR9201**	**Exar**	**(3193)**	40
		0.8	100 *	x	x					x	x		x		x	ZN428E-8	Ferranti		
				x	x					x	x		x		x	ZN428J-8	† Ferranti		
		1	30	x						x	x			x		DAC0832	National		
			45 *	x						x	x		x			ZN426E-8	Ferranti		
				x						x	x		x			ZN426J-8	† Ferranti		
				x						x	x					ZN429E-8	Ferranti		
				x						x	x					ZN429J-8	† Ferranti		
			750	x						x			x			MN3008	Micro Net		
				x						x			x			MN3008H	† Micro Net		
					x					x			x			MN3009	Micro Net		50
					x					x			x			MN3009H	† Micro Net		

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Digital to Analog Converters (Cont'd)

D/A Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source	Line
																		(Cont'd)
8	1/2	1.5	75 *	x						x	x		x		x	**AD558J**	**AD (3164)**	
			300	x	x					x	x			x		DAC331B-8	† Hybrid Sys	
				x	x					x	x			x		DAC331C-8	Hybrid Sys	
		2 *	255	x	x					x			x			**DAC-UP8BC**	**Datel (2621)**	
				x	x					x			x			DAC-UP8BM	† Datel	
			255 *	x						x	x	x	x	x	x	NE5018	Signetics	
				x						x	x	x	x	x	x	SE5018	† Signetics	
		2.5	570	x	x	x				x			x			MN3014	Micro Net	
				x	x	x				x			x			MN3014H	† Micro Net	
		3	680	x	x								x			HS3020B	† Hybrid Sys	10
				x	x								x			HS3020C	Hybrid Sys	
			830	x	x	x				x			x		x	MN3020	Micro Net	
				x	x	x				x			x		x	MN3020H	† Micro Net	
		4	1080	x	x		x			x	x		x		x	DAC336B-8	† Hybrid Sys	
				x	x		x			x	x		x		x	DAC336C-8	Hybrid Sys	
		20	285	x						x	x		x			DAC336B-1	† Hybrid Sys	
				x						x	x		x			DAC337B-0	† Hybrid Sys	
				x						x	x		x			DAC337B-2	† Hybrid Sys	
				x						x	x		x			DAC337C-0	Hybrid Sys	
				x						x	x		x			DAC337C-1	Hybrid Sys	20
				x						x	x		x			DAC337C-2	Hybrid Sys	
		23 *	585			x				x	x		x			MN3000	Micro Net	
						x				x	x		x			MN3000H	† Micro Net	
					x					x	x		x			MN3001	Micro Net	
					x					x	x		x			MN3001H	† Micro Net	
				x						x	x		x			MN3002	Micro Net	
				x						x	x		x			MN3002H	† Micro Net	
					x					x	x		x			MN3006	Micro Net	
					x					x	x		x			MN3006H	† Micro Net	
		30	570	x	x	x				x			x			MN3013	Micro Net	30
				x	x	x				x			x			MN3013H	† Micro Net	
		40	300		x					x	x		x			DAC337B-6	† Hybrid Sys	
					x					x	x		x			DAC337C-6	Hybrid Sys	
	3/4	1.5	375	x						x	x		x		x	**AD558S**	**† AD (3164)**	
	1	0.01 *	675	x								x		x		**MC10318C-7**	**Motorola (2759)**	
		0.07	305	x						x	x			x		MC1408-7	Signetics	
		0.15	174	x	x	x	x			x	x	x		x		DAC-08C	AMD	
				x	x	x	x			x	x	x		x		ADDAC-08C	AD	
				x	x	x	x			x	x	x		x		µA0801C	Fairchild	
				x	x	x	x			x	x	x		x		DAC-08C	Motorola	40
				x	x	x				x				x		**DAC0801C**	**National (3320)**	
				x	x	x	x			x	x	x		x		DAC-08C	PMI	
				x	x	x	x			x	x	x		x		DAC-08C	Raytheon	
				x	x	x	x			x	x	x		x		DAC-08C	Signetics	
		0.22	20 *	x	x					x	x			x	x	**AD7528J**	**AD (3164)**	
				x	x					x	x			x	x	**AD7528S**	**† AD (3164)**	
		0.25 *	265	x	x					x	x			x		SSS1408A-7	AMD	
				x	x					x	x			x		**AD1408-7**	**AD (3164)**	
				x	x					x	x			x		µA0802B	Fairchild	
				x	x					x	x			x		DAC-1408A-7	PMI	50
		0.3 *	305	x						x	x			x		1408-7	AMD	
				x										x		**MC1408-7**	**Motorola (2759)**	
				x						x				x		**DAC0807C**	**National (3320)**	
				x						x				x		LM1408-7	National	

(Continued)

Bin.—Binary
Off.—Offset
Compl.—Complementary
Magn.—Magnitude
Int Ref.—Internal Reference
CTC—Compl. 2's Compl.
Mult.—Multiplying

IC MASTER

INTERFACE–Digital to Analog Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source		Line
D/A Converters																		**(Cont'd)**	
8																		(Cont'd)	
	1 1/4	0.3 *	305	x							x			x		**MC3408**	**Motorola**	**(2759)**	
	2	0.01 *	675	x								x		x		**MC10318C-6**	**Motorola**	**(2759)**	
		0.25 *	265	x	x					x	x			x		DAC1408A-6	AMD		
				x	x					x	x			x		µA0802C	Fairchild		
				x	x					x	x			x		DAC-1408A-6	PMI		
		0.3 *	305	x						x	x			x		1408-6	AMD		
				x										x		**MC1408-6**	**Motorola**	**(2759)**	
				x						x				x		**DAC0806C**	**National**	**(3320)**	
				x						x				x		LM1408-6	National		
8 (A/D, D/A, with counter)																			
	1/2	2.0	175	x						x	x		x			ZN425E-8	Ferranti		10
	1	2.0	175	x						x	x		x			ZN425J-8	† Ferranti		
8 (D/A, with counter/clock)																			
	1/2	0.8	—	x						x	x		x			ZN435E-8	Ferranti		
				x						x	x		x			ZN435J-8	† Ferranti		
8 Plus Sign																			
	1/2	20	750	x						x				x		MN380	Micro Net		
				x						x				x		MN380H	† Micro Net		
8 (video digital converter)																			
	1/4	0.010	1976	x								x				HDD-0810	AD		
				x								x				HDD-0810M	† AD		
			2028	x								x				HDD-0810C	AD		
				x								x				HDD-0810CM	† AD		
	1/2	0.008	1660	x								x				**HDG-0805**	**AD**	**(3169)**	20
8 (7-Bits plus Sign) Companding																			
	—	0.5 *	192							x						AM6072C	AMD		
										x						AM6072M	† AMD		
	1/2 step																		
		0.5	192							x						AM6070AC	AMD		
										x						AM6070AM	† AMD		
										x	x	x		x		DAC-76B	† PMI		
										x	x			x		DAC-76E	PMI		
										x	x	x		x		DAC-86E	PMI		
										x	x	x		x		DAC-87E	PMI		
			207							x	x	x		x		DAC-88E	PMI		
			500							x	x	x		x		DAC-89E	PMI		30
	1 step	0.5	192							x						AM6070C	AMD		
										x						AM6070M	† AMD		
		0.5 *	192							x	x	x		x		DAC-76	† PMI		
										x	x	x		x		DAC-76C	PMI		
										x	x	x		x		DAC-86C	PMI		
										x	x	x		x		DAC-87C	PMI		
			207							x	x	x		x		DAC-88C	PMI		
			500							x	x	x		x		DAC-89C	PMI		
	1 1/2 step																		
		0.5 *	192							x	x	x		x		DAC-76D	PMI		
8-2 Digit BCD																			
	1/4	0.135	194							x	x	x		x		DAC-20A	† Motorola		40
										x	x	x		x		DAC-20E	Motorola		
	1/2	0.135	194							x	x	x		x		DAC-20	† Motorola		
										x	x	x		x		DAC-20C	Motorola		
		0.15	194							x	x	x		x		DAC-20C	PMI		
		23 *	630							x	x		x			MN3010	Micro Net		
										x	x		x			MN3010H	† Micro Net		
9	1/2	0.01	450	x		x				x					x	**TDC1016-9**	**TRW**	**(3438)**	

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Digital to Analog Converters (Cont'd)

D/A Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source	Line
9 (8-Bits plus Sign)																		
	1/4	0.75	500	x					x	x	x		x	x		DAC-208A	† PMI	
				x					x	x	x		x	x		DAC-208E	PMI	
	1/2	0.75	500	x					x	x	x		x	x		DAC-208B	† PMI	
				x					x	x	x		x	x		DAC-208F	PMI	
10	1/8	0.5 *	50	x	x	x	x			x	x			x		MP7620J	Micro Pwr	
	1/4 *	0.6 *	780	x						x	x			x		**HI5610-2**	**† Harris (2683,3288)**	
				x						x	x			x		**HI5610-4**	**Harris (2683,3288)**	
				x						x	x			x		**HI5610-5**	**Harris (2683,3288)**	
				x						x	x			x		**HI5610-8**	**† Harris (2683,3288)**	
	1/4	0.025 *	735	x	x					x	x					**HDS-1025**	**AD (3169)**	10
				x	x					x	x					**HDS-1025M**	**† AD (3169)**	
		0.25 *	275	x	x					x	x		x			**AD561K**	**AD (3164)**	
				x	x					x	x		x			**AD561T**	**† AD (3164)**	
				x	x					x	x		x			MP561K	Micro Pwr	
				x	x					x	x		x			MP561T	† Micro Pwr	
		0.3 *	1300			x	x			x	x		x			**HDH-1003**	**AD (3169)**	
		0.5 *	50	x	x	x	x			x	x			x		MP7620K	Micro Pwr	
	1/2	0.01	450	x		x				x					x	**TDC1016-10**	**TRW (3438)**	
		0.025	705	x	x					x			x			**DAC-HF10BMC**	**Datel (2621)**	
				x	x					x			x			**DAC-HF10BMM**	**† Datel (2620)**	20
		0.15	450	x	x	x	x			x	x	x		x		DAC-10B	† PMI	
				x	x	x	x			x	x	x		x		DAC-10C	† PMI	
				x	x	x	x			x	x	x		x		DAC-10F	PMI	
				x	x	x	x			x	x	x		x		DAC-10G	PMI	
		0.25	380	x							x			x		**MC3410**	**Motorola (2759)**	
				x							x			x		**MC3510**	**† Motorola (2759)**	
				x							x			x		MC3410	Signetics	
			390	x	x					x	x					DAC-IC10B	Datel	
				x	x					x	x					DAC-IC10BM	† Datel	
		0.25 *	275	x	x					x	x		x			**AD561J**	**AD (3164)**	30
				x	x					x	x		x			**AD561S**	**AD (3164)**	
				x	x					x	x		x			MP561J	Micro Pwr	
				x	x					x	x		x			MP561S	† Micro Pwr	
		0.3	—	x	x						x			x		**AD7527C**	**AD (3164)**	
				x	x						x			x		**AD7527GC**	**AD (3164)**	
				x	x						x			x		**AD7527GL**	**AD (3164)**	
				x	x						x			x		**AD7527GU**	**† AD (3164)**	
				x	x						x			x		**AD7527L**	**AD (3164)**	
				x	x						x			x		**AD7527U**	**† AD (3164)**	
		0.375	300			x	x			x			x			**MP5560A**	**† Micro Pwr (2749)**	40
						x	x			x			x			DAC-100A	† PMI	
						x	x			x			x			DAC-100A	PMI	
		0.5	30	x	x					x	x			x		DAC-HA10BC-1	Datel	
				x	x					x	x			x		DAC-HA10BM-1	† Datel	
		0.5 *	0.025	x	x					x	x			x		**DAC-HA10BC**	**Datel (2621)**	
				x	x					x	x			x		**DAC-HA10BM**	**† Datel (2620)**	
			20 *	x	x	x	x			x	x			x		**AD7520L**	**AD (3164)**	

(Continued)

Bin.—Binary
Off.—Offset
Compl.—Complementary
Magn.—Magnitude
Int Ref.—Internal Reference
CTC—Compl. 2's Compl.
Mult.—Multiplying

IC MASTER

INTERFACE–Digital to Analog Converters (Cont'd)

D/A Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source	Line
																	(Cont'd)	
10	1/2	0.5 *	20 *	x	x	x	x			x	x			x		**AD7520U**	**†AD (3164)**	
				x	x	x	x			x	x			x		**AD7530L**	**AD (3164)**	
				x	x	x	x							x		AD7520L	Intersil	
				x	x	x	x							x		AD7520U	† Intersil	
				x	x	x	x			x	x			x		AD7530L	Intersil	
				x	x	x	x			x	x			x		**MP7520L**	**Micro Pwr (401,2749)**	
				x	x	x	x			x	x			x		**MP7520P**	**Micro Pwr (401,2749)**	
				x	x	x	x			x	x			x		**MP7520U**	**†Micro Pwr (401,2749)**	
				x	x	x	x			x	x			x		**MP7530**	**Micro Pwr (401,2749)**	
			20 *	x	x	x	x			x				x	x	**DAC1000**	**†National (3320)**	10
				x	x	x	x			x	x			x	x	**DAC1000C**	**National (3320)**	
				x	x	x	x			x	x			x	x	DAC1003	† National	
				x						x	x			x	x	DAC1003C	National	
				x	x	x	X			x	x			x	x	**DAC1006**	**†National (3320)**	
				x	x	x	X			x	x			x	x	**DAC1006C**	**National (3320)**	
			40	x	x	x	X			x	x			x	x	**AD7522L**	**AD (3164)**	
				x	x	x	X			x	x			x	x	**AD7522U**	**†AD (3164)**	
				x	x					x	x			x	x	**MP7522L**	**Micro Pwr (401,2749)**	
				x	x	x	x			x	x			x	x	**MP7522U**	**†Micro Pwr (401,2749)**	
			50	x	x	x	x			x	x			x		MP7620L	Micro Pwr	20
		0.6	30	x	x	x	x			x	x			x		**AD7533C**	**AD (3164)**	
				x	x	x	x			x	x			x		**AD7533L**	**AD (3164)**	
				x	x	x	x			x	x			x		**AD7533U**	**†AD (3164)**	
		0.8 *	30 *	x	x	x	x			x	x			x		AD7533L	Intersil	
				x	x	x	x			x	x			x		AD7533U	† Intersil	
				x	x	x	x			x	x			x		**MP7533L**	**Micro Pwr (401,2749)**	
				x	x	x	x			x	x			x		**MP7533U**	**†Micro Pwr (401,2749)**	
		1.5	30	x	x					x	x			x		DAC331B-10	† Hybrid Sys	
				x	x					x	x			x		DAC331C-10	Hybrid Sys	
		4 *	255	x						x	x	x	x	x	x	NE5020	Signetics	30
		10	715			x	x			x			x			MN3040	Micro Net	
						x	x			x			x			MN3040H	† Micro Net	
		15	165	x				x		x	x			x		DAC348B-10	† Hybrid Sys	
				x				x		x	x			x		DAC348C-10	Hybrid Sys	
		20	150			x	x			x	x		x			DAC347LPB-10B	† Hybrid Sys	
						x				x	x		x			DAC347LPB-10U	† Hybrid Sys	
						x	x			x	x		x			DAC347LPC-10B	Hybrid Sys	
						x				x	x		x			DAC347LPC-10U	Hybrid Sys	
			285		x					x	x		x			DAC337B-4	† Hybrid Sys	
				x						x	x		x			DAC337B-5	† Hybrid Sys	40
					x					x	x		x			DAC337C-4	Hybrid Sys	
				x						x	x		x			DAC337C-5	Hybrid Sys	
		23 *	585			x				x			x			MN3003	Micro Net	
						x				x			x			MN3003H	† Micro Net	
					x					x			x			MN3004	† Micro Net	
					x					x			x			MN3004H	† Micro Net	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Digital to Analog Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source		Line
D/A Converters																		**(Cont'd)**	
																		(Cont'd)	
10	1/2	23 *	585	x						x			x			MN3005	Micro Net		
				x						x			x			MN3005H	† Micro Net		
					x					x			x			MN3007	Micro Net		
					x					x			x			MN3007H	† Micro Net		
		30	—		x					x				x		M/D2005-1	HyComp		
		40	300			x				x	x		x			DAC337B-3	† Hybrid Sys		
					x					x	x		x			DAC337B-7	† Hybrid Sys		
						x				x	x		x			DAC337C-3	Hybrid Sys		
					x					x	x		x			DAC337C-7	Hybrid Sys		
		500 *	24	x						x	x			x		AD7520L	National		10
				x						x	x			x		AD7520U	† National		
				x						x	x			x		**DAC1020**	**† National**	**(3320)**	
				x						x	x			x		**DAC1020C**	**National**	**(3320)**	
	1/2	0.01	990	x								x				**HDS-1015E**	**AD**	**(3169)**	
				x								x				**HDS-1015EM**	**† AD**	**(3169)**	
		0.135	276	x		x				x	x			x		DAC-10B	Raytheon		
				x		x				x	x			x		DAC-10C	Raytheon		
				x		x				x	x			x		DAC-10F	Raytheon		
		0.25	380	x						x	x			x		MC3510	Signetics		
		0.25 *	300	x						x	x		x	x		**NE5410**	**Signetics**	**(3413)**	20
				x						x	x		x	x		**SE5410**	**Signetics**	**(3413)**	
		0.3 *	1300			x	x			x	x		x			HDH1003M	† AD		
		0.375	250			x	x	x		x			x			**ADDAC100K**	**AD**	**(3164)**	
						x	x	x		x			x			**ADDAC100L**	**AD**	**(3164)**	
						x	x	x		x			x			**ADDAC100T**	**† AD**	**(3164)**	
	1	0.15	276	x		x				x	x			x		DAC-10G	Raytheon		
		0.25	—		x	x				x	x		x			DAC-101E	PMI		
			380	x							x			x		**MC3410C**	**Motorola**	**(2759)**	
				x						x	x			x		MC3410C	Signetics		
			390	x	x					x	x			x		**DAC-IC10BC**	**Datel**	**(2621)**	30
		0.3	—	x	x						x			x		**AD7527B**	**AD**	**(3164)**	
				x	x						x			x		**AD7527K**	**AD**	**(3164)**	
				x	x						x			x		**AD7527T**	**† AD**	**(3164)**	
			300			x	x			x			x			**MP5560B**	**† Micro Pwr**	**(2749)**	
						x	x			x			x			DAC-100B	† PMI		
		0.375	250			x	x	x		x			x			**ADDAC100J**	**AD**	**(3164)**	
						x	x	x		x			x			**ADDAC100S**	**† AD**	**(3164)**	
		0.5 *	20 *	x	x	x	x			x	x			x		**AD7520K**	**AD**	**(3164)**	
				x	x	x	x			x	x			x		**AD7520T**	**† AD**	**(3164)**	
				x	x	x	x			x	x			x		**AD7530K**	**AD**	**(3164)**	40
				x	x	x	x			x	x			x		AD7520K	Intersil		
				x	x	x	x			x	x			x		AD7520T	† Intersil		
				x	x	x	x			x	x			x		AD7530K	Intersil		
				x	x	x	x			x	x			x		**MP7520K**	**Micro Pwr**	**(401,2749)**	
				x	x	x	x			x	x			x		**MP7520N**	**Micro Pwr**	**(401,2749)**	
				x	x	x	x			x	x			x		**MP7520T**	**† Micro Pwr**	**(401,2749)**	
				x	x	x	x			x	x			x		**MP7530K**	**Micro Pwr**	**(401,2749)**	
				x	x	x	x			x	x			x	x	DAC1001	† National		
				x	x	x	x			x	x			x	x	DAC1001C	National		
				x	x	x	x			x	x			x	x	DAC1004	† National		50
				x	x	x	x			x	x			x	x	DAC1004C	National		

(Continued)

Bin.—Binary
Off.—Offset
Compl.—Complementary
Magn.—Magnitude
Int Ref.—Internal Reference
CTC—Compl. 2's Compl.
Mult.—Multiplying

IC MASTER

INTERFACE–Digital to Analog Converters (Cont'd)

D/A Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source		Line
																		(Cont'd)	
10	1	0.5 *	20 *	x	x	x	x			x	x			x	x	**DAC1007**	**†National**	**(3320)**	
				x	x	x	x			x	x			x	x	**DAC1007C**	**National**	**(3320)**	
			40	x	x	x	x			x	x			x	x	**AD7522K**	**AD**	**(3164)**	
				x	x	x	x			x	x			x	x	**AD7522T**	**†AD**	**(3164)**	
			50	x	x	x	x			x	x			x	x	**MP7522K**	**Micro Pwr**	**(401,2749)**	
				x	x	x	x			x	x			x	x	**MP7522T**	**†Micro Pwr**	**(401,2749)**	
				x	x	x	x			x	x			x		MP7620M	Micro Pwr		
		0.6	30	x	x	x	x			x	x			x		**AD7533B**	**AD**	**(3164)**	
				x	x	x	x			x	x			x		**AD7533K**	**AD**	**(3164)**	
				x	x	x	x			x	x			x		**AD7533T**	**†AD**	**(3164)**	10
		0.8 *	30 *	x	x	x	x			x	x			x		AD7533K	Intersil		
				x	x	x	x			x	x			x		AD7533T	† Intersil		
				x	x	x	x			x	x			x		**MP7533K**	**Micro Pwr**	**(401,2749)**	
		1.5 *	300		x			x		x	x		x			DAC-04AC	PMI		
					x			x		x	x		x			DAC-04BC	PMI		
					x			x		x	x		x			DAC-06E	PMI		
			350	x						x	x		x			DAC-03AD	PMI		
				x						x	x		x			DAC-03BD	PMI		
		5	435	x	x								x			**DAC-UP10B**	**Datel**	**(2615)**	
		500 *	24	x						x	x			x		AD7520K	National		20
				x						x	x			x		AD7520T	National		
				x						x	x			x		**DAC1021**	**†National**	**(3320)**	
				x						x	x			x		**DAC1021C**	**National**	**(3320)**	
	2	0.225	300			x	x			x			x			**MP5560C**	**†Micro Pwr**	**(2749)**	
						x	x			x			x			MP5560C	Micro Pwr		
						x	x			x			x			DAC-100C	† PMI		
						x	x			x			x			DAC-100C	PMI		
		0.25	225		x	x				x	x			x		DAC-101F	PMI		
		0.5 *	20 *	x	x	x	x			x	x			x		**AD7520J**	**AD**	**(3164)**	
				x	x	x	x			x	x			x		**AD7520S**	**†AD**	**(3164)**	30
				x	x	x	x			x	x			x		**AD7530J**	**AD**	**(3164)**	
				x	x	x	x			x	x			x		AD7520J	Intersil		
				x	x	x	x			x	x			x		AD7520S	† Intersil		
				x	x	x	x			x	x			x		AD7530J	Intersil		
				x	x	x	x			x	x			x		**MP7520J**	**Micro Pwr**	**(401,2749)**	
				x	x	x	x			x	x			x		**MP7520M**	**†Micro Pwr**	**(401,2749)**	
				x	x	x	x			x	x			x		**MP7520S**	**Micro Pwr**	**(401,2749)**	
				x	x	x	x			x	x			x		**MP7530J**	**Micro Pwr**	**(401,2749)**	
				x	x	x	x			x	x			x		**DAC1002**	**†National**	**(3320)**	
				x	x	x	x			x	x			x	x	**DAC1002C**	**National**	**(3320)**	40
				x	x	x	x			x	x			x		DAC1005	† National		
				x	x	x	x			x	x					DAC1005C	National		
				x	x	x	x			x	x					**DAC1008**	**†National**	**(3320)**	
				x	x	x	x			x	x			x	x	**DAC1008C**	**National**	**(3320)**	
			40	x	x	x	x			x	x			x	x	**AD7522J**	**AD**	**(3164)**	
				x	x	x	x			x	x			x	x	**AD7522S**	**†AD**	**(3164)**	
			50	x	x	x	x			x	x			x	x	**MP7522J**	**Micro Pwr**	**(401,2749)**	
				x	x	x	x			x	x			x	x	**MP7522S**	**†Micro Pwr**	**(401,2749)**	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Digital to Analog Converters (Cont'd)

D/A Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source	Line
																	(Cont'd)	
10	2	0.6	30	x	x	x	x			x	x			x		**AD7533A**	**AD (3164)**	
				x	x	x	x			x	x			x		**AD7533J**	**AD (3164)**	
				x	x	x	x			x	x			x		**AD7533S**	**†AD (3164)**	
		0.8 *	30 *	x	x	x	x			x	x			x		AD7533J	Intersil	
				x	x	x				x	x			x		AD7533S	† Intersil	
				x	x	x	x			x	x			x		**MP7533S**	**† Micro Pwr (401,2749)**	
				x	x	x	x			x	x			x		**MP7533T**	**† Micro Pwr (401,2749)**	
				x	x	x	x			x	x			x		MP7533T	Micro Pwr	
		1.5 *	300		x			x		x	x		x			DAC-04CC	PMI	
					x			x		x	x		x			DAC-06F	PMI	10
			350	x						x	x		x			DAC-03CD	PMI	
					x			x		x	x		x			DAC-06A	PMI	
		500 *	24	x						x	x			x		AD7520J	National	
				x						x	x			x		AD7520S	† National	
				x						x	x			x		**DAC1022**	**† National (3320)**	
				x						x	x			x		**DAC1022C**	**National (3320)**	
	3	0.225	300			x	x			x			x			**MP5560D**	**Micro Pwr (2749)**	
						x	x			x			x			DAC-100D	† PMI	
						x	x			x			x			DAC-100D	PMI	
		0.5 *	50	x	x	x	x			x	x			x		**MP7520H**	**Micro Pwr (401,2749)**	20
		1.5 *	350		x			x		x	x		x			DAC-06B	PMI	
	4	0.2	—		x	x				x	x		x			DAC-10G	PMI	
		1.5 *	300		x			x		x	x		x			DAC-06G	PMI	
			350	x						x	x		x			DAC-03DD	PMI	
		2.5 *	350					x		x	x		x			DAC-04DD	PMI	
	5	1.5 *	350					x		x	x		x			DAC-06C	† PMI	
	8	0.5 *	50	x	x	x	x			x	x			x		**MP7520G**	**Micro Pwr (401,2749)**	
10 Companding	1/2 Step	0.5	260						x							DAC-78E	PMI	
	1 Step	0.5	260						x							DAC-78F	PMI	
	1 1/2 Step	0.5	260						x							DAC-78G	PMI	30
10 Plus Sign	1/2	1.5 *	350	x					x	x	x		x			DAC-05E	PMI	
			500	x					x	x	x		x			DAC-210A	† PMI	
				x					x	x	x		x			DAC-210B	† PMI	
				x					x	x	x		x			DAC-210E	PMI	
		6	300	x												µPC610	NEC-Electron	
	1	1.5 *	300	x					x	x	x		x			DAC-210G	PMI	
			350	x					x	x	x		x			DAC-02AC	PMI	
				x					x	x	x		x			DAC-02BC	PMI	
			500	x					x	x	x		x			DAC-210F	PMI	
	2	1.5 *	300	x					x	x	x		x			DAC-02CC	PMI	40
				x					x	x	x		x			DAC-05F	PMI	
			350	x					x	x	x		x			DAC-05A	† PMI	
	3	1.5 *	350	x					x	x	x		x			DAC-05B	† PMI	
				x					x	x	x		x			DAC-05C	PMI	
	4	1.5 *	300	x					x	x	x		x			DAC-05G	PMI	
		2.5 *	350	x					x	x	x		x			DAC-02DD	PMI	

Bin.—Binary
Off.—Offset
Compl.—Complementary
Magn.—Magnitude
Int Ref.—Internal Reference
CTC—Compl. 2's Compl.
Mult.—Multiplying

IC MASTER

INTERFACE–Digital to Analog Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB μS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source	Line
D/A Converters																	**(Cont'd)**	
10 Video Digital Converter																		
	1/2	0.015	2340	x									x			**HDD-1015**	**AD (3169)**	
				x									x			**HDD-1015C**	**AD (3169)**	
				x									x			**HDD-1015M**	**†AD (3169)**	
11 Plus Sign Dynamic Range (7-Bit plus sign format)																		
	1/2 step																	
		0.5	207							x	x	x		x		DAC-88E	PMI	
										x	x	x		x		DAC-89E	PMI	
		0.5 *	207							x	x	x		x		DAC-76B	† PMI	
										x	x	x		x		DAC-76E	PMI	
										x	x	x		x		DAC-86E	PMI	
										x	x	x		x		DAC-87E	PMI	
	1 step	0.5	207							x	x	x		x		DAC-86C	PMI	10
										x	x	x		x		DAC-88C	PMI	
										x	x	x		x		DAC-89C	PMI	
		0.5 *	207							x	x	x		x		DAC-76C	PMI	
										x	x	x		x		DAC-87C	PMI	
12	1/4	0.25	345	x	x					x	x		x			**AD565AK**	**AD (3165)**	
				x	x					x	x		x			**AD565AT**	**†AD (3165)**	
		0.4	—	x	x					x	x					DAC-562M	† Datel	
			210	x	x					x	x		x			**MC3512**	**Motorola (2757)**	
			300	x	x					x	x		x	x		**AD566AK**	**AD (3166)**	
				x	x					x	x		x	x		**AD566AT**	**†AD (3166)**	20
				x	x					x	x		x			**AD566K**	**AD (3166)**	
				x	x					x	x		x			**AD566T**	**†AD (3166)**	
				x	x					x	x		x			MCE566AK	Micro Eng	
				x	x					x	x		x	x		MCE566AT	† Micro Eng	
				x	x					x	x		x	x		MCE566K	Micro Eng	
				x	x					x	x		x			MCE566T	† Micro Eng	
			345	x	x					x	x		x			**AD565K**	**AD (3165)**	
				x	x					x	x		x			**AD565T**	**†AD (3165)**	
				x	x					x	x		x			MCE565K	Micro Eng	
				x	x					x	x		x			MCE565T	† Micro Eng	30
			780	x						x	x			x		**HI562A-2**	**†Harris (3288)**	
				x						x	x			x		**HI562A-8**	**Harris (3288)**	
		0.5	20 *	x	x	x	x			x	x			x		**MP7621C**	**Micro Pwr (401.2749)**	
				x	x	x	x			x	x			x		**MP7621L**	**Micro Pwr (401.2749)**	
				x	x	x	x			x	x			x		**MP7621U**	**†Micro Pwr (401.2749)**	
			375	x	x					x	x		x			HI565AK	Harris	
				x	x					x	x		x			HI565AT	† Harris	
			495	x	x					x	x		x		x	**AD567K**	**AD (3166)**	
		1	64 *	x	x					x	x			x		**HI7541K**	**Harris (2731.3288)**	
				x	x					x	x			x		**HI7541T**	**†Harris (2731.3288)**	40
		1.5	465	x	x					x	x			x		**AD562S/BIN**	**AD (3166.3168)**	
				x	x					x	x			x		AD562S/BIN	Micro Pwr	
			475	x	x					x	x		x			**AD563K/BIN**	**AD (3165)**	
				x	x					x	x		x			**AD563S/BIN**	**†AD (3165)**	
				x	x					x	x		x			**AD563T/BIN**	**†AD (3165)**	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Digital to Analog Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source		Line
D/A Converters																		**(Cont'd)**	
																		(Cont'd)	
12	1/4	1.5 *	200 *	x	x					x	x			x		**MP562**	**Micro Pwr**	**(401,2749)**	
		1.8	500	x	x	x	x			x	x		x	x		MN562-SD-BIN	Analogic		
			700	x	x	x	x			x	x		x	x		MN563-SD-BIN	Analogic		
	1/2	—	35		x			x	x	x					x	**AD7545C**	**AD**	**(3166)**	
					x			x	x	x					x	**AD7545GC**	**AD**	**(3166)**	
					x			x	x	x					x	**AD7545GL**	**AD**	**(3166)**	
					x			x	x	x					x	**AD7545GU**	**AD**	**(3166)**	
					x			x	x	x					x	**AD7545L**	**AD**	**(3166)**	
					x			x	x	x					x	**AD7545U**	**AD**	**(3166)**	
		0.035	—													DAC63	Burr-Brown		10
			855	x	x					x	x					**HDS-1250**	**AD**	**(3169)**	
				x	x					x	x					**HDS-1250M**	† **AD**	**(3169)**	
		0.05	—			x	x			x		x	x			ADH-030II-12	DDC		
		0.050	780	x	x					x			x			**DAC-HF12BMC**	**Datel**	**(2621)**	
				x	x					x			x			DAC-HF12BMM	† Datel		
			1200	x	x					x				x		DAC391B-12	† Hybrid Sys		
				x	x					x				x		DAC391C-12	Hybrid Sys		
			1350			x	x					x	x			DAC397B-12	† Hybrid Sys		
						x	x					x	x			DAC397C-12	Hybrid Sys		
		0.06/1	675			x	x			x			x			DAC-8528-12	† DDC		20
		0.060	395	x	x					x			x			4065	† Teledyne P		
		0.085 *	780	x						x	x			x		HI5612-2	† Harris		
				x						x	x			x		HI5612-4	Harris		
				x						x	x			x		HI5612-5	Harris		
				x						x	x			x		HI5612-8	† Harris		
		0.10	775			x	x			x			x			DAC87-CBI-I	† DDC		
			850			x	x	x		x			x			DAC85LD-CBI-I	DDC		
		0.18	—	x	x					x	x			x		**AD7544B**	**AD**	**(3166)**	
				x	x					x	x			x		**AD7544BG**	**AD**	**(3166)**	
				x	x					x	x			x		**AD7544GK**	**AD**	**(3166)**	30
				x	x					x	x			x		**AD7544GT**	† **AD**	**(3166)**	
				x	x					x	x			x		**AD7544K**	**AD**	**(3166)**	
				x	x					x	x			x		**AD7544T**	† **AD**	**(3166)**	
		0.20	430 *	x	x			x		x	x		x			DAC10HT	† Burr-Brown		
		0.25	345	x	x					x	x		x			**AD565AJ**	**AD**	**(3165)**	
				x	x					x	x		x			**AD565AS**	† **AD**	**(3165)**	
				x	x					x	x		x			MCE565AJ	Micro Eng		
				x	x					x	x		x			MCE565AS	† Micro Eng		
			900			x	x			x			x			4080	† Teledyne P		
						x	x			x			x			4080-83	† Teledyne P		40
						x	x			x			x			4081	Teledyne P		
						x	x			x			x			4081-83	† Teledyne P		
						x	x			x			x			4082	Teledyne P		
						x	x			x			x			4082-83	† Teledyne P		
		0.3	770 *			x				x	x		x			**DAC-85C-CBI-I**	**Datel**	**(2621)**	
						x				x	x		x			DAC-87C-CBI-I	† Datel		
			1000			x				x			x			**HI5680I-5**	**Harris**	**(2689)**	
																		(Continued)	

Bin.—Binary
Off.—Offset
Compl.—Complementary
Magn.—Magnitude
Int Ref.—Internal Reference
CTC—Compl. 2's Compl.
Mult.—Multiplying

IC MASTER

INTERFACE–Digital to Analog Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source		Line
D/A Converters																		**(Cont'd)**	
																		(Cont'd)	
12	1/2	0.3	1000			x				x	x		x			**HI5685I-4**	**Harris**	**(2696)**	
						x	x			x			x			**HI5687I-2**	**†Harris**	**(2700)**	
		0.3/1.5 *																	
			800 *			x	x	x		x			x			DAC650-CBI-I	Burr-Brown		
						x	x	x		x			x			DAC650-CBI-V	Burr-Brown		
						x	x	x		x			x			DAC800-CBI-I	Burr-Brown		
						x	x	x		x			x			DAC800-CBI-V	Burr-Brown		
						x	x	x		x			x			DAC851-CBI-I	† Burr-Brown		
		0.3/2.5 *																	
			500 *			x				x	x		x			**DAC1280AC**	**National**	**(3345)**	
						x				x	x		x			**DAC1285**	**†National**	**(3345)**	
						x				x	x		x			**DAC1285A**	**†National**	**(3345)**	10
						x				x	x		x			**DAC1285AC**	**National**	**(3345)**	
						x				x	x		x			**DAC1285C**	**National**	**(3345)**	
						x				x	x					DAC80-CBI-V	National		
						x				x	x					DAC80Z-CBI-V	National		
						x				x	x					DAC85-CBI-V	National		
						x				x	x					DAC85L-CBI-V	National		
						x				x	x					DAC87-CBI-V	National		
		0.3/3 *	800			x	x	x		x			x			DAC80/CBI	Burr-Brown		
						x	x	x		x			x			DAC85/CBI	Burr-Brown		
						x	x	x		x			x			DAC85C/CBI	Burr-Brown		20
						x	x	x		x			x			DAC87/CBI	† Burr-Brown		
			850			x	x	x		x			x			**ADDAC87/CBI**	**†AD**	**(3165)**	
						x	x	x		x			x			DAC85/CBI	Micro Net		
			925			x	x	x		x			x			**ADDAC80/CBI**	**AD**	**(3164)**	
						x	x	x		x			x			**ADDAC85/CBI**	**†AD**	**(3164)**	
						x	x	x		x			x			**ADDAC85C/CBI**	**AD**	**(3164)**	
		0.35	230	x						x						**HI5660**	**Harris**	**(2730)**	
		0.4	—	x	x					x	x					**DAC-562C**	**Datel**	**(2621)**	
						x	x	x		x						HIDAC801	Harris		
			210	x	x					x	x		x			**MC3412**	**Motorola**	**(2757)**	30
			300	x	x					x	x		x	x		**AD566AJ**	**AD**	**(3166)**	
				x	x					x	x		x	x		**AD566AS**	**†AD**	**(3166)**	
				x	x					x	x		x			**AD566J**	**AD**	**(3166)**	
				x	x					x	x		x			**AD566S**	**†AD**	**(3166)**	
				x	x					x	x		x			MCE565J	Micro Eng		
				x	x					x	x		x			MCE565S	† Micro Eng		
				x	x					x	x		x	x		MCE566AJ	Micro Eng		
				x	x					x	x		x	x		MCE566AS	† Micro Eng		
				x	x					x	x		x			MCE566J	Micro Eng		
				x	x					x	x		x			MCE566S	† Micro Eng		40
			345	x	x					x	x		x			**AD565J**	**AD**	**(3165)**	
				x	x					x	x		x			**AD565S**	**†AD**	**(3165)**	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE-Digital to Analog Converters (Cont'd)

D/A Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source	Line
																		(Cont'd)
12	1/2	0.4	400	x	x					x	x			x		DAC862S	† Burr-Brown	
				x	x	x	x			x	x	x		x		µPC648	NEC-Electron	
			780	x						x	x			x		**HI562A-4**	**Harris (3288)**	
				x						x	x			x		**HI562A-5**	**Harris (3288)**	
		0.5	0.05	x	x					x	x			x		**DAC-HA12BC**	**Datel (2621)**	
				x	x					x	x			x		**DAC-HA12BM**	**† Datel (2620)**	
			10 *	x						x	x			x		DAC1220	† National	
				x						x	x			x		DAC1220C	National	
			20	x	x					x	x			x		DAC-HA12BC-1	Datel	
				x	x					x	x			x		DAC-HA12BM-1	† Datel	10
			312 *	x	x	x	x	x		x	x	x		x		**AM6012C**	**AMD (3101)**	
				x	x	x	x	x		x	x	x		x		**AM6012M**	**† AMD (3101)**	
				x	x	x	x	x		x	x	x		x		**MCE6012C**	**Micro Eng (4440)**	
				x	x	x	x	x		x	x	x		x		**MCE6012M**	**† Micro Eng (4440)**	
			375	x	x					x	x		x			HI565AJ	Harris	
				x	x					x	x		x			HI565AS	† Harris	
			495	x	x					x	x		x		x	**AD567J**	**AD (3166)**	
				x	x					x	x		x		x	**AD567S**	**† AD (3166)**	
			1000	x						x	x			x		**AD562**	**Motorola (2759)**	
				x						x	x		x			**AD563**	**Motorola (2759)**	20
		0.5 *	20 *	x	x	x	x			x	x			x		**MP7623**	**Micro Pwr (401,2749)**	
			1300			x	x			x	x					**HDH-1205**	**AD (3169)**	
						x	x			x	x					**HDH-1205M**	**† AD (3169)**	
		0.6	1410	x	x					x				x		DAC392B-12	Hybrid Sys	
				x	x					x				x		DAC392C-12	Hybrid Sys	
		1	20 *	x	x	x	x			x	x			x		**AD7541B**	**AD (3164,3166)**	
				x	x	x	x			x	x			x		**AD7541K**	**AD (3164,3166)**	
				x	x	x	x			x	x			x		**AD7541T**	**† AD (3164,3166)**	
				x	x	x	x			x	x			x		AD7541B	Intersil	
				x	x	x	x			x	x			x		AD7541K	Intersil	
				x	x	x	x			x	x			x		AD7541T	Intersil	30
				x	x	x	x			x	x			x		**MP7541**	**Micro Pwr (401,2749)**	
				x	x	x	x			x	x			x		**MP7621B**	**Micro Pwr (401,2749)**	
				x	x	x	x			x	x			x		**MP7621K**	**Micro Pwr (401,2749)**	
				x	x	x	x			x	x			x		**MP7621T**	**† Micro Pwr (401,2749)**	
				x	x	x	x			x	x			x		7541T	† Teledyne S	
				x	x	x	x			x	x			x		TSC7541B	Teledyne S	
				x	x	x	x			x	x			x		TSC7541K	Teledyne S	
				x	x	x	x			x	x			x		TSC8641B	† Teledyne S	
				x	x	x	x			x	x			x		TSC8641C	Teledyne S	40
			30	x	x					x	x			x		HS7541B-2	† Hybrid Sys	
				x	x					x	x			x		HS7541C-2	Hybrid Sys	
				x						x	x			x		**DAC1208**	**National (3320)**	
				x						x	x			x		DAC1218	National	
				x						x	x			x		DAC1230	National	
			30 *	x	x					x	x			x		HS7541-4	Hybrid Sys	
			64 *	x	x					x	x			x		**HI7541J**	**Harris (2731,3288)**	
				x	x					x	x			x		**HI7541S**	**† Harris (2731,3288)**	

(Continued)

Bin.—Binary
Off.—Offset
Compl.—Complementary
Magn.—Magnitude
Int Ref.—Internal Reference
CTC—Compl. 2's Compl.
Mult.—Multiplying

IC MASTER

INTERFACE–Digital to Analog Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source	Line
D/A Converters																	**(Cont'd)**	
12	1/2																(Cont'd)	
		1 *	750		x	x				x	x		x			**HSDAC80CBI-I**	**Hybrid Sys (2747)**	
		1/1.5 *	—		•	x	x			x			x			HSDAC87BI/V	† Hybrid Sys	
						x	x			x			x			HSDAC87CI/V	Hybrid Sys	
		1.5	300			x	x			x	x		x			DAC335B-12	† Hybrid Sys	
						x	x			x	x		x			DAC335C-12	Hybrid Sys	
		1.5 *	—	x						x	x		x		x	**AD563J**	**AD (3165)**	
			465	x	x					x	x			x		**AD562K/BIN**	**AD (3166,3168)**	
			475	x	x					x	x		x			**AD563J/BIN**	**AD (3165)**	
			750		x	x				x	x		x			**HSDAC80CBI-V**	**Hybrid Sys (2747)**	
		1.5/2.5 *				x				x	x					**DAC1200**	**† National (3320,3345)**	10
						x				x	x					**DAC1200C**	**National (3320,3345)**	
		1.8	500	x	x	x	x			x	x		x	x		MN562-AD-BIN	Analogic	
				x	x	x	x			x	x		x	x		MN562-ID-BIN	Analogic	
				x	x	x	x			x	x		x	x		MN562-KD-BIN	Analogic	
			700	x	x	x	x			x	x		x	x		MN563-JD-BIN	Analogic	
				x	x	x	x			x	x		x	x		MN563-KD-BIN	Analogic	
				x	x	x	x			x	x		x	x		MN563-TD-BIN	Analogic	
		2	40	x	x					x	x			x		**AD7542B**	**AD (3166)**	
				x	x					x	x			x		**AD7542K**	**AD (3166)**	
				x	x					x	x			x		**AD7542T**	**† AD (3166)**	20
				x						x				x		**AD7543B**	**AD (3166)**	
				x						x				x		**AD7543K**	**AD (3166)**	
			375	x	x					x			x			4058	† Teledyne P	
			375 *	x	x	x				x	x			x		**HS3120B-2**	**† Hybrid Sys (2747)**	
				x	x	x				x	x			x		**HS3120C-2**	**Hybrid Sys (2747)**	
			1900			x	x			x						**HDD-1206J**	**AD (3169)**	
						x	x			x						**HDD-1206S**	**† AD (3169)**	
		2 *	—			x	x			x						DAC345I-12	Hybrid Sys	
		2.5	—	x	x					x	x		x			**DAC338B-12-2**	**Hybrid Sys (2748)**	
		3	30	x	x					x	x			x		DAC331B-12	† Hybrid Sys	30
				x	x					x	x			x		DAC331C-12	Hybrid Sys	
			770 *			x				x	x		x			DAC-85C-CBI-V	Datel	
						x				x	x		x			DAC-87C-CBI-V	† Datel	
			775			x	x			x			x			DAC87-CBI-I	† DDC	
			850			x	x	x		x			x			DAC85LD-CBI-V	DDC	
						x	x	x		x			x			MNDAC87	† Micro Net	
			900	x	x					x			x		x	DAC-HK12BGC	Datel	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Digital to Analog Converters (Cont'd)

D/A Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source		Line
																		(Cont'd)	
12	1/2	3	900					x		x			x		x	DAC-HK12BGC-2	Datel		
				x	x					x			x		x	**DAC-HK12BMM**	**† Datel**	**(2620)**	
								x		x			x		x	HAC-HK12BMM-2	† Datel		
			1000			x				x			x			**HI5680V-5**	**Harris**	**(2689)**	
						x				x	x		x			**HI5685V-4**	**Harris**	**(2696)**	
						x	x			x			x			**HI5687V-2**	**Harris**	**(2700)**	
			1050			x	x			x			x			**DAC-HZ12BGC**	**Datel**	**(2621)**	
						x	x			x			x			HAC-HZ12BMM	† Datel		
		3.5	465	x	x					x	x			x		**AD562A/BCD**	**AD**	**(3166,3168)**	
				x	x					x	x			x		**AD562A/BIN**	**AD**	**(3166,3168)**	10
		4	300	x	x					x	x		x		x	DAC336B-12	† Hybrid Sys		
				x	x					x	x		x		x	DAC336C-12	Hybrid Sys		
		5	450 *	x	x					x	x		x			**HS9338-2**	**Hybrid Sys**	**(2748)**	
			1000		x	x							x			**HS3860B**	**† Hybrid Sys**	**(2748)**	
					x	x							x			**HS3860C**	**Hybrid Sys**	**(2748)**	
		5 *	—			x	x			x						DAC345V-12	Hybrid Sys		
			525 *			x	x			x	x		x			MN3850	† Micro Net		
						x	x			x	x		x			MN3850H	Micro Net		
			675 *			x	x			x			x		x	MN3860	Micro Net		
						x	x			x			x		x	MN3860H	† Micro Net		20
		7	1000			x	x			x			x		x	**AD3860K**	**AD**	**(3166)**	
						x	x			x			x		x	**AD3860S**	**† AD**	**(3166)**	
		8	—	x						x	x					**AD390K**	**AD**	**(3166)**	
			375			x	x			x			x			MN3348	Micro Net		
						x	x			x			x			MN3348H	† Micro Net		
		10	375			x	x			x			x			MN3349	Micro Net		
						x	x			x			x			MN3349H	† Micro Net		
			750			x	x	x		x			x		x	DAC-SL-12	† DDC		
		15	165	x				x		x	x			x		DAC348B-12	† Hybrid Sys		
				x				x		x	x			x		DAC348C-12	Hybrid Sys		30
			300	x	x					x	x		x			DAC349B-12	† Hybrid Sys		
				x	x					x	x		x			DAC349C-12	Hybrid Sys		
				x	x					x	x		x			DAC9349-12	Hybrid Sys		
		20	150			x	x			x	x		x			DAC347LPB-12U	† Hybrid Sys		
						x	x			x	x		x			DAC347LPC-12B	Hybrid Sys		
						x	x			x	x		x			DAC347LPC-12U	Hybrid Sys		
						x	x			x	x		x			HAC347LPB-12B	† Hybrid Sys		
			355			x				x				x		MN3412	Micro Net		
		25	—				x			x	x		x		x	DAC02701	DDC		
			175 *			x				x	x		x			DAC9356	Hybrid Sys		40
		30	—	x		x				x				x		M/DA2000	HyComp		
		35	90			x				x			x			MN371	Micro Net		
						x				x			x			MN371H	† Micro Net		
			150				x			x	x		x			**AD370J**	**AD**	**(3165)**	
							x			x	x		x			**AD370K**	**AD**	**(3165)**	
							x			x	x		x			**AD370S**	**† AD**	**(3165)**	
						x				x	x		x			**AD371J**	**AD**	**(3165)**	

(Continued)

Bin.—Binary
Off.—Offset
Compl.—Complementary
Magn.—Magnitude
Int Ref.—Internal Reference
CTC—Compl. 2's Compl.
Mult.—Multiplying

IC MASTER

INTERFACE-Digital to Analog Converters (Cont'd)

D/A Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source	Line
																	(Cont'd)	
12	1/2	35	1065	x		x				x	x		x			MN3210	Micro Net	
							x			x	x		x			MN3211	Micro Net	
		35 *	—	x	x					x	x		x			DDC1250-12-1	DDC	
				x	x					x	x		x			DDC1250-12-3	DDC	
		50	265				x			x	x		x			DAC356B-12	† Hybrid Sys	
							x			x	x		x			DAC356C-12	Hybrid Sys	
			908				x			x	x		x			DAC356LPB-12	† Hybrid Sys	
							x			x	x		x			DAC356LPC-12	Hybrid Sys	
			1653			x	x					x	x			**HDS-1240E**	**AD (3169)**	
						x	x					x	x			**HDS-1240EM**	**† AD (3169)**	10
		70	90				x			x	x		x			MN370	Micro Net	
							x			x	x		x			MN370H	† Micro Net	
	3/4	8	—	x						x	x					**AD390J**	**AD (3166)**	
	1	—	35		x			x	x	x					x	**AD7545B**	**AD (3166)**	
					x			x	x	x					x	**AD7545K**	**† AD (3166)**	
					x			x	x	x					x	**AD7545T**	**AD (3166)**	
		0.06/1	675			x	x			x			x			DAC-8528-11	† DDC	
		0.18	—	x	x					x	x			x		**AD7544A**	**AD (3166)**	
				x	x					x	x			x		**AD7544J**	**AD (3166)**	
				x	x					x	x			x		**AD7544S**	**AD (3166)**	20
		1	20 *	x	x	x	x			x	x			x		**AD7541A**	**AD (3164,3166)**	
				x	x	x	x			x	x			x		**AD7541J**	**AD (3164,3166)**	
				x	x	x	x			x	x			x		AD7541A	Intersil	
				x	x	x	x			x	x			x		AD7541J	Intersil	
				x	x	x	x			x	x			x		**MP7621A**	**Micro Pwr (401,2749)**	
				x	x	x	x			x	x			x		**MP7621J**	**Micro Pwr (401,2749)**	
				x	x	x	x			x	x			x		**MP7621S**	**† Micro Pwr (401,2749)**	
				x	x	x				x	x			x		7541S	† Teledyne S	
				x	x	x				x	x			x		TSC7441S	† Teledyne S	
				x	x	x				x	x			x		TSC7541A	Teledyne S	30
				x	x	x				x	x			x		TSC7541J	Teledyne S	
				x	x	x				x	x			x		TSC8640B	† Teledyne S	
				x	x	x				x	x			x		TSC8640C	Teledyne S	
			30	x	x					x	x			x		HS7541B-1	† Hybrid Sys	
				x	x					x	x			x		HS7541C-1	Hybrid Sys	
				x						x	x			x		**DAC1209**	**National (3320)**	
				x						x	x			x		DAC1219	National	
				x						x	x			x		DAC1231	National	
			40 *	x	x	x	x			x	x			x	x	**MP7622A**	**Micro Pwr (401,2749)**	
				x	x	x	x			x	x			x	x	**MP7622J**	**Micro Pwr (401,2749)**	40
				x	x	x	x			x	x			x	x	**MP7622S**	**† Micro Pwr (401,2749)**	
			50 *	x	x	x	x			x	x			x		**AD7541S**	**† AD (3164,3166)**	
				x	x	x	x			x	x			x		AD7541L	Intersil	
				x	x	x	x			x	x			x		AD7541S	† Intersil	
		2	40	x	x					x	x			x		**AD7542A**	**AD (3166)**	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Digital to Analog Converters (Cont'd)

D/A Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source	Line
																	(Cont'd)	
12	1	2	40	x	x					x	x			x		AD7542J	AD (3166)	
				x	x					x	x			x		AD7542S	†AD (3166)	
				x	x					x				x		AD7543A	AD (3166)	
				x	x					x				x		AD7543J	AD (3166)	
		2.5	—	x	x					x	x		x			DAC338B-12-1	Hybrid Sys (2748)	
		2.5 *	625 *			x				x	x		x			DAC1280C	National (3345)	
		5	450 *	x	x					x	x		x			HS9338-1	Hybrid Sys (2748)	
		10	750			x	x	x		x			x		x	DAC-SL-11	† DDC	
		20 *	500	x	x					x	x		x		x	DAC9377-16-5	Hybrid Sys (2745)	
		30	—	x		x				x				x		M/DA2005	HyComp	10
		35	150			x				x	x		x			AD371K	AD (3165)	
						x				x	x		x			AD371S	†AD (3165)	
	2	—	35		x			x	x	x					x	AD7545A	AD (3166)	
					x			x	x	x					x	AD7545J	AD (3166)	
					x			x	x	x					x	AD7545S	†AD (3166)	
		0.04	—	x	x							x	x			DA4000	HyComp	
		0.05	—			x	x			x		x	x			ADH-030II-10	DDC	
		0.25	375	x		x				x	x	x		x		DAC312B	† PMI	
				x		x				x	x	x		x		DAC312F	PMI	
		0.5	20 *	x	x	x	x			x	x			x		MP7621H	Micro Pwr (401,2749)	20
				x	x	x	x			x	x			x		MP7621R	†Micro Pwr (401,2749)	
				x	x	x	x			x	x			x		MP7621Z	Micro Pwr (401,2749)	
		0.5 *	20 *	x	x	x	x			x	x			x		AD7521L	AD (3164)	
				x	x	x	x			x	x			x		AD7521U	†AD (3164)	
				x	x	x	x			x	x			x		AD7521L	Intersil	
				x	x	x	x			x	x			x		AD7521U	† Intersil	
				x	x	x	x			x	x			x		AD7531L	Intersil	
				x	x	x	x			x	x			x		MP7521L	Micro Pwr (401,2749)	
				x	x	x	x			x	x			x		MP7521P	Micro Pwr (401,2749)	
				x	x	x	x			x	x			x		MP7521U	†Micro Pwr (401,2749)	30
				x	x	x	x			x	x			x		MP7531L	Micro Pwr (401,2749)	
		0.50	397	x	x	x		x		x	x	x		x		AM6012	Signetics (3383)	
		1	30	x						x	x			x		DAC1210	National	
				x						x	x			x		DAC1232	National	
		2	40 *	x	x	x	x			x	x			x	x	MP7622H	Micro Pwr (401,2749)	
				x	x	x	x			x	x			x	x	MP7622R	†Micro Pwr (401,2749)	
				x	x	x	x			x	x			x	x	MP7622Z	Micro Pwr (401,2749)	
			375 *	x	x	x				x	x			x		DAC3120B-0	† Hybrid Sys (2747)	
				x	x	x				x	x			x		DAC3120C-0	Hybrid Sys (2747)	

(Continued)

Bin.—Binary
Off.—Offset
Compl.—Complementary
Magn.—Magnitude
Int Ref.—Internal Reference
CTC—Compl. 2's Compl.
Mult.—Multiplying

IC MASTER

INTERFACE–Digital to Analog Converters (Cont'd)

D/A Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source	Line
																	(Cont'd)	
12	2	2 *	—			x	x			x						DAC345I-10	Hybrid Sys	
		2.5	—	x	x					x	x		x			**DAC338B-12-0**	**Hybrid Sys (2748)**	
		5	450 *	x	x					x	x		x			**HS9338-0**	**Hybrid Sys (2748)**	
			800			x	x			x	x		x			**DAC1201**	**† National (3320,3345)**	
						x	x			x	x		x			**DAC1201C**	**National (3320,3345)**	
		5 *	—			x	x			x						DAC345V-10	Hybrid Sys	
		20 *	500	x	x					x	x		x		x	**DAC9377-16-4**	**Hybrid Sys (2745)**	
		35 *	—	x	x					x	x		x			DDC1250-10-1	DDC	
				x	x					x	x		x			DDC1250-10-3	DDC	
		500 *	24	x						x	x			x		AD7521L	National	10
				x						x	x			x		AD7521U	† National	
	4	0.5 *	20 *	x	x	x	x			x	x			x		**AD7521K**	**AD (3164)**	
				x	x	x	x			x	x			x		**AD7521T**	**† AD (3164)**	
				x	x	x	x			x	x			x		**AD7531K**	**AD (3164)**	
				x	x	x	x			x	x			x		AD7521K	Intersil	
				x	x	x	x			x	x			x		AD7521T	† Intersil	
				x	x	x	x			x	x			x		AD7531K	Intersil	
				x	x	x	x			x	x			x		**MP7521K**	**Micro Pwr (401,2749)**	
				x	x	x	x			x	x			x		**MP7521N**	**Micro Pwr (401,2749)**	
				x	x	x	x			x	x			x		**MP7521T**	**† Micro Pwr (401,2749)**	20
				x	x	x	x			x	x			x		**MP7531K**	**Micro Pwr (401,2749)**	
		500 *	24	x						x	x			x		AD7521K	National	
				x						x	x			x		AD7521T	† National	
				x						x	x			x		DAC1221	† National	
				x						x	x			x		DAC1221C	National	
	8	0.5 *	20 *	x	x	x	x			x	x			x		**AD7521J**	**AD (3164)**	
				x	x	x	x			x	x			x		**AD7521S**	**† AD (3164)**	
				x	x	x	x			x	x			x		**AD7531J**	**AD (3164)**	
				x	x	x	x			x	x			x		AD7521J	Intersil	
				x	x	x	x			x	x			x		AD7521S	† Intersil	30
				x	x	x	x			x	x			x		AD7531J	Intersil	
				x	x	x	x			x	x			x		**MP7521J**	**Micro Pwr (401,2749)**	
				x	x	x	x			x	x			x		**MP7521M**	**Micro Pwr (401,2749)**	
				x	x	x	x			x	x			x		**MP7521S**	**† Micro Pwr (401,2749)**	
				x	x	x	x			x	x			x		**MP7531J**	**Micro Pwr (401,2749)**	
		500 *	24	x						x	x			x		AD7521J	National	
				x						x	x			x		AD7521S	† National	
				x						x	x			x		DAC1222	† National	
				x						x	x			x		DAC1222C	National	
	16	0.5 *	50	x	x	x	x			x	x			x		**MP7521H**	**Micro Pwr (401,2749)**	40
	32	0.5 *	50	x	x	x	x			x	x			x		**MP7521G**	**Micro Pwr (401,2749)**	

† Military Temperature Range (−55° to 125°C)

* Typical Value

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INTERFACE–Digital to Analog Converters (Cont'd)

D/A Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source	Line
12 Plus Sign Dynamic Range (7-Bit plus sign format)																		
	—	0.5	192							x						AM6072C	AMD	
										x						AM6072M	† AMD	
	1/2 step																	
		0.5	192							x						AM6070AC	AMD	
										x						AM6070AM	† AMD	
			207							x	x	x		x		DAC-86E	PMI	
	1 step	0.5	192							x						AM6070C	AMD	
										x						AM6070M	† AMD	
			207							x	x	x		x		DAC-86C	PMI	
		0.5 *	192							x	x	x		x		DAC-76	† PMI	
12-3 Digit BCD																		
	1/4	0.3	770 *			x				x	x		x			DAC-85C-CCD-I	Datel	10
						x				x	x		x			DAC-87-CCD-I	† Datel	
		0.3/3 *	925							x	x		x			**ADDAC80/CCD**	**AD (3164)**	
						x				x	x		x			**ADDAC85/CCD**	**† AD (3164)**	
						x				x	x		x			**ADDAC85C/CCD**	**AD (3164)**	
		3	770 *			x				x	x		x			DAC-85C-CCD-V	Datel	
						x				x	x		x			DAC-87-CCD-V	† Datel	
			900										x		x	DAC-HK12DGC	Datel	
													x		x	DAC-HK12DMM	† Datel	
		3 *	1050							x			x			DAC-HZ12DGC	Datel	
										x			x			DAC-HZ12DMC	Datel	20
										x			x			DAC-HZ12DMM	† Datel	
	1/2	0.3/3 *	800							x			x			DAC80/CCD	Burr-Brown	
										x			x			DAC85/CCD	† Burr-Brown	
										x			x			DAC85C/CCD	Burr-Brown	
			850 *							x			x			DAC85/CCD	† Micro Net	
										x			x			DAC85C/CCD	Micro Net	
		0.5	30							x	x		x			DAC-HA12DC-1	Datel	
										x	x		x			DAC-HA12DM-1	† Datel	
		0.5 *	0.05							x	x		x			DAC-HA12DC	Datel	
										x	x		x			DAC-HA12DM	† Datel	30
		1.8	500							x	x		x	x		MN562-AD-BCD	Analogic	
										x	x		x	x		MN562-ID-BCD	Analogic	
										x	x		x	x		MN562-KD-BCD	Analogic	
			700							x	x		x	x		MN563-JD-BCD	Analogic	

(Continued)

Bin.—Binary
Off.—Offset
Compl.—Complementary
Magn.—Magnitude
Int Ref.—Internal Reference
CTC—Compl. 2's Compl.
Mult.—Multiplying

IC MASTER

INTERFACE–Digital to Analog Converters (Cont'd)

D/A Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source	Line
12-3 Digit BCD																	(Cont'd)	
	1/2	1.8	700							x	x		x	x		MN563-KD-BCD	Analogic	
										x	x		x	x		MN563-TD-BCS	Analogic	
		15	300	x	x					x	x		x			DAC349B-3D	† Hybrid Sys	
				x	x					x	x		x			DAC349C-3D	Hybrid Sys	
				x						x	x		x			DAC9349-3D	Hybrid Sys	
		35	1065							x	x		x			MN3212	Micro Net	
	1/10	1.5 *	465							x	x			x		**AD562K/BCD**	**AD (3166,3168)**	
										x	x			x		**AD562S/BCD**	**† AD (3166,3168)**	
			475							x	x		x			**AD563J/BCD**	**AD (3165)**	
										x	x		x			**AD563K/BCD**	**AD (3165)**	10
										x	x		x			**AD563S/BCD**	**† AD (3165)**	
										x	x		x			**AD563T/BCD**	**† AD (3165)**	
										x	x		x	x		MN562-SD-BCD	Analogic	
		1.8	700							x	x		x	x		MN563-SD-BCD	Analogic	
12-4 Digit BCD																		
	1/2	20 *	500	x	x					x	x		x		x	**DAC9377-4D**	**Hybrid Sys (2745,2745)**	
13	1	0.1	980				x			x			x			2615-12	DDC	
		1.6	1100				x			x			x			SDAC-12	DDC	
	2	0.1	980				x			x			x			2615-11	DDC	
		1.6	1100				x			x			x			SDAC-11	DDC	
	4	0.1	980				x			x			x			2615-10	DDC	20
		1.6	1100				x			x			x			SDAC-10	DDC	
13 (3 Device Set)																		
	1	1.8	3475					x		x			x			DDAC-12	DDC	
	2	1.8	3475					x		x			x			DDAC-11	DDC	
	4	1.8	3475					x		x			x			DDAC-10	DDC	
14	1/2			x	x					x	x			x		DAC9331-14	Hybrid Sys	
		2	30 *	x	x					x	x			x		**HS3140B-4**	**† Hybrid Sys (2746)**	
				x	x					x	x			x		**HS3140C-4**	**Hybrid Sys (2746)**	
		3	30	x	x					x	x			x		DAC331B-14	† Hybrid Sys	
				x	x					x	x			x		DAC331C-14	Hybrid Sys	
	1	0.5	0.05	x	x					x	x			x		**DAC-HA14BC**	**Datel (2621)**	30
				x	x					x	x			x		**DAC-HA14BM**	**† Datel (2620)**	
			30	x	x					x	x			x		DAC-HA14BC-1	Datel	
				x	x					x	x			x		DAC-HA14BM-1	Datel	
		2	30 *	x	x					x	x			x	x	**MP3140B-4**	**† Micro Pwr (2749)**	
				x	x					x	x			x	x	**MP3140C-4**	**Micro Pwr (2749)**	
			375 *	x	x	x				x	x			x		**HS3140B-3**	**Hybrid Sys (2746)**	
				x	x	x				x	x			x		**HS3140C-3**	**Hybrid Sys (2746)**	
		2 *	20 *	x	x					x	x			x		**MP7614**	**Micro Pwr (401,2749)**	
	2	2	30 *	x	x					x	x			x	x	**MP3140B-3**	**† Micro Pwr (2749)**	
				x	x					x	x			x	x	**MP3140C-3**	**Micro Pwr (2749)**	40
		20	900	x						x				x		DAC-U12-1	† DDC	
	4	20	900	x	x					x				x		DAC-U11-1	† DDC	

† Military Temperature Range (−55° to 125°C)

* Typical Value

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INTERFACE–Digital to Analog Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source	Line
D/A Converters																	**(Cont'd)**	
16	1/2	2 *	60	x	x					x	x			x		DAC370B-16	† Hybrid Sys	
				x	x					x	x			x		DAC370C-16	Hybrid Sys	
				x	x					x	x			x		**DAC9331-16-6**	**Hybrid Sys (2745)**	
				x	x					x	x			x		MP9331-6	Micro Pwr	
		5	—			x	x	x					x	x	x	PCM50K	Burr-Brown	
		5 *	50 *	x	x					x	x			x	x	**AD7546B**	**AD (3166)**	
				x	x					x	x			x	x	**AD7546K**	**AD (3166)**	
		20 *	500	x	x					x	x		x		x	**DAC9377-16-6**	**Hybrid Sys (2745)**	
				x	x					x	x		x		x	**MP9377-16**	**Micro Pwr (401,2749)**	
		35	420	x						x	x		x			MN3310	Micro Net	10
		50	—													DAC736	Burr-Brown	
																DAC74	Burr-Brown	
			500			x	x			x	x		x		x	DAC73	† Burr-Brown	
						x	x			x	x		x		x	DAC73C	Burr-Brown	
	1	1	465	x	x			x		x	x					**HIDAC16B**	**Harris (2722)**	
		2 *	60	x	x					x	x			x		**DAC9331-16-5**	**Hybrid Sys (2745)**	
				x	x					x	x			x		MP9331-5	Micro Pwr	
		5 *	50 *	x	x					x	x			x	x	**AD7546A**	**AD (3166)**	
				x	x					x	x			x	x	**AD7546J**	**AD (3166)**	
	2	1	—			x				x			x			DAC-71-COB-I	Datel	20
						x				x			x			DAC-71-CSB-I	Datel	
						x				x			x			DAC-72C-COB-I	Datel	
						x				x			x			DAC-72C-CSB-I	Datel	
			465	x	x			x		x	x					**HIDAC16C**	**Harris (2722)**	
			1225				x			x			x			**ADDAC71-COB-I**	**AD (3166)**	
						x				x			x			**ADDAC71-CSB-I**	**AD (3166)**	
							x			x			x			**ADDAC72-COB-I**	**AD (3166)**	
						x				x			x			**ADDAC72-CSB-I**	**AD (3166)**	
		2	30	x	x					x	x			x		**HS3160B-4**	**† Hybrid Sys (2746)**	
				x	x					x	x			x		**HS3160C-4**	**Hybrid Sys (2746)**	30
		2 *	60	x	x					x	x			x		**DAC9331-16-4**	**Hybrid Sys (2745)**	
				x	x					x	x			x		MP9331-4	Micro Pwr	
		5	—			x				x			x			DAC-71-COB-V	Datel	
						x				x			x			DAC-71-CSB-V	Datel	
						x				x			x			DAC-72C-COB-V	Datel	
						x				x			x			DAC-72C-CSB-V	Datel	
			1225				x			x			x			**ADDAC71-COB-V**	**AD (3166)**	
						x				x			x			**ADDAC71-CSB-V**	**AD (3166)**	
							x			x			x			**ADDAC72-COB-V**	**AD (3166)**	
						x				x			x			**ADDAC72-CSB-V**	**AD (3166)**	40

(Continued)

Bin.—Binary
Off.—Offset
Compl.—Complementary
Magn.—Magnitude
Int Ref.—Internal Reference
CTC—Compl. 2's Compl.
Mult.—Multiplying

IC MASTER

INTERFACE–Digital to Analog Converters (Cont'd)

D/A Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source	Line
																(Cont'd)		
16	2	10	500				x			x			x			DAC71/COB	† Burr-Brown	
						x				x			x			DAC71/CSB	† Burr-Brown	
					x					x			x			DAC72/COB	† Burr-Brown	
						x				x			x			DAC72/CSB	† Burr-Brown	
		35	1170			x	x			x			x			DAC-HP16BMC	Datel	
						x	x			x			x			DAC-HP16BMC-1	Datel	
						x	x			x			x			**DAC-HP16BMM**	**† Datel (2620)**	
						x	x			x			x			DAC-HP16BMM-1	† Datel	
		50/100 *	575 *			x				x			x			DAC70/CSB	† Burr-Brown	
						x				x			x			DAC70C/CSB	Burr-Brown	10
	3	50/100 *	575 *				x			x			x			DAC70/COB	† Burr-Brown	
							x			x			x			DAC70C/COB	Burr-Brown	
	4	2	—	x	x					x	x			x		**MP7616L**	**Micro Pwr (401,2749)**	
	8	2	—	x	x					x	x			x		**MP7616K**	**Micro Pwr (401,2749)**	
			30	x	x					x	x			x		**HS3160B-3**	**† Hybrid Sys (2746)**	
				x	x					x	x			x		**HS3160C-3**	**Hybrid Sys (2746)**	
16-4 Digit BCD	1/2	15	1170							x			x			DAC-HP16DGC	Datel	
										x			x			DAC-HP16DMC	Datel	
										x			x			DAC-HP16DMM	† Datel	
		35	420							x	x		x			MN3300	Micro Net	20
		50/100 *	575 *							x			x			DAC70/CCD	† Burr-Brown	
										x			x			DAC70C/CCD	Burr-Brown	
	2	1	—			x				x			x			DAC-71-CCD-I	Datel	
						x				x			x			DAC-72C-CCD-I	Datel	
		5	—			x				x			x			DAC-71-CCD-V	Datel	
						x				x			x			DAC-72C-CCD-V	Datel	
		10	1.2							x			x			DAC71/CCD	† Burr-Brown	
18	1	20	60	x	x					x	x		x		x	DAC370B-18	† Hybrid Sys	
				x	x					x	x		x		x	DAC370C-18	Hybrid Sys	
				x	x					x	x		x		x	**MP370B-18**	**† Micro Pwr (401,2749)**	30
				x	x					x	x		x		x	**MP370C-18**	**Micro Pwr (401,2749)**	
			500	x	x					x	x		x			**DAC377-18**	**Hybrid Sys (2745)**	
				x	x					x	x		x		x	**DAC377B-18**	**† Hybrid Sys (2745)**	
				x	x					x	x		x		x	**DAC377C-18**	**Hybrid Sys (2745)**	
				x	x					x	x		x		x	**MP377B-18**	**† Micro Pwr (401)**	
				x	x					x	x		x		x	**MP377C-18**	**Micro Pwr (401)**	

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Display Drivers

Display Drivers

Function	Device	Source	Line
Bargraph Fluorescent			
	XR2276	**Exar** **(3204)**	
Bargraph Gas Discharge Display Driver (module)			
	AW100	AWI	
Bargraph Gas Discharge (module)			
	AW200	AWI	
Bargraph LED	LM3914	National	
	LM3915	National	
	AN6875	Panasonic	
	LB1405	Sanyo	
	LB1409	Sanyo	
	LB1415	Sanyo	
	LB1416	Sanyo	10
	LB1419	Sanyo	
	LB1426	Sanyo	
	LB1436	Sanyo	
	UAA170	Siemens	
	UAA180	Siemens	
	TDA1594	Signetics	
	U237B	Telefunken	
	U244	Telefunken	
	U247B	Telefunken	
	U254	Telefunken	20
	U257B	Telefunken	
	U267B	Telefunken	
	TSC9403	Toshiba	
	TSC9404	Toshiba	
Bargraph LED or Vacuum Fluorescent (module)			
	AW580	AWI	
Bargraph or LED Dot Display Generators			
	XR2277	**Exar** **(3204)**	
	XR2278	**Exar** **(3204)**	
	XR2279	**Exar** **(3205)**	
Bargraph VF	HA12010	Hitachi	
	HA12011	Hitachi	30
	LM3916	National	
	LB1470	Sanyo	
Clock Driver, Dual			
	DS3671	National	
Display Controllers and Keyboard Interface: See Microprocessors-General Purpose			
Lamp Driver			
	CSR301	Teledyne C	
LCD Display Interface (drives 7 to 20-segment linear displays)	SAA1062	Signetics	
LCD Dot Matrix Driver			
	SED1100	Epson	
	SED1300	Epson	
	HLCD0488	Hughes	40
	HLCD0515	Hughes	
	HLCD0538A	Hughes	
	HLCD0539A	Hughes	
	HLCD0540	Hughes	
	HLCD0548	Hughes	
	HLCD0550	Hughes	
	HLCD0551	Hughes	
	HLCD0607	Hughes	
LCD Graphics Driver			
	SED1500	Epson	
LED Bar Display Driver, 10 LEDs			
	TA7612A	Toshiba	50
LED, Cascadable			
	SDA2014	Siemens	
LED Display Driver, 5 LEDs			
	TA7654	Toshiba	
	TA7655	Toshiba	
LED Display Driver, 33 Outputs, 15 mA Sink Capability			
	MM5486	National	

Function	Device	Source	Line
LED Display/Interface (drives 7, 14, 16-segments for linear displays, bar graphs)			
	SAA1060	Signetics	
	SAA1061	Signetics	
LED Driver System, 8 Decade, 8x8 Memory, Decoder (versions either hardwire or processor controlled			
	ICM7218A	Intersil	
	ICM7218B	Intersil	
	ICM7218C	Intersil	
	ICM7218D	Intersil	60
	ICM7218E	Intersil	
LED, Static	U180M	Telefunken	
	U3080M	Telefunken	
Multiplexed LCD Driver, Master and Slave			
	MC145000	Motorola	
	MC145001	Motorola	
	MM58201	National	
Segment Driver for Gas Discharge Displays			
	DI232	Dionics	
	DI242	Dionics	
Universal (LED, LCD, or vacuum fluorescent)			
	S2809	AMI	
BCD (hexadecimal) to 7-Segment Decoder/Driver with Latch Active Low, Open Collector			
	9370C	Fairchild	70
BCD (hexadecimal) to 7-Segment Latch/Decoder/Driver (CMOS with bipolar output)			
	MC14495	Motorola	
	UCN-4805A	Sprague	
	UCN-4806A	Sprague	
BCD (hexadecimal) to 7-Segment LED Decoder/Driver, Constant Current, with Latch			
	9368C	Fairchild	
BCD Plus 1 to 7-Segment			
	LM1017	National	
	U143	Telefunken	
BCD to 7-Segment Decoder/Driver			
	MC14547BA	† Motorola	
	MC14547BC	Motorola	
BCD to 7-Segment Decoder/Driver, Active High, Open Collector	5449	† Fairchild	
	54LS249	† Fairchild	80
	74LS249	Fairchild	
	74LS49	Fairchild	
	HD74LS249	Hitachi	
	HD74LS49	Hitachi	
	MC5449	† Motorola	
	MC7449	Motorola	
	SN54LS249	Motorola	
	SN54LS49	† Motorola	
	SN74LS249	† Motorola	
	SN74LS49	Motorola	90
	DM54LS249	† National	
	DM54LS49	† National	
	DM74LS249	National	
	DM74LS49	National	
	N8T06	Signetics	
	SN54249	**† TI** **(914)**	
	SN5449	**† TI** **(847)**	
	SN54LS249	**† TI** **(914)**	
	SN54LS49	**† TI** **(847)**	
	SN74249	**TI** **(914)**	100
	SN7449	**TI** **(847)**	
	SN74LS249	**TI** **(914)**	
	SN74LS49	**TI** **(847)**	
BCD to 7-Segment Decoder/Driver, Active High, Resistive Pull-Up	5448	† Fairchild	
	54LS48	† Fairchild	
	7448	Fairchild	
	74LS248	Fairchild	
	74LS48	Fairchild	

(Continued)

Function	Device	Source	Line
BCD to 7-Segment Decoder/Driver, Active High, Resistive Pull-Up			(Cont'd)
	9307C	Fairchild	
	9307M	† Fairchild	110
	HD74LS248	Hitachi	
	HD74LS48	Hitachi	
	MC5448	† Motorola	
	MC7448	Motorola	
	MC8307	Motorola	
	MC9307	† Motorola	
	SN54LS248	† Motorola	
	SN54LS48	† Motorola	
	SN74LS248	Motorola	
	SN74LS48	Motorola	120
	DM5448	† National	
	DM54LS248	† National	
	DM54LS48	† National	
	DM7448	National	
	DM74LS248	National	
	DM74LS48	National	
	DS8856	National	
	N8T05	Signetics	
	S8T05	† Signetics	
	SN54248	**† TI** **(914)**	130
	SN5448	**† TI** **(847)**	
	SN54LS248	**† TI** **(914)**	
	SN54LS48	**† TI** **(847)**	
	SN74248	**TI** **(914)**	
	SN7448	**TI** **(847)**	
	SN74LS248	**TI** **(914)**	
	SN74LS48	**TI** **(847)**	
BCD to 7-Segment Decoder/Driver, Active Low, Open Collector	54LS347	† Fairchild	
	74LS347	Fairchild	
	74LS447	Fairchild	140
	MC4039	Motorola	
	S8T04	† Signetics	
	SN54LS347	**† TI** **(931)**	
	SN54LS447	**† TI** **(950)**	
	SN74LS347	**TI** **(931)**	
	SN74LS447	**TI** **(950)**	
BCD to 7-Segment Decoder/Driver, Active Low, Open Collector, 15 V Output	5447	† Fairchild	
	54LS247	† Fairchild	
	7447	Fairchild	
	74LS247	Fairchild	150
	74LS47	Fairchild	
	9317BC	Fairchild	
	9317BM	† Fairchild	
	HD7447A	Hitachi	
	HD74LS247	Hitachi	
	HD74LS47	Hitachi	
	MC5447	† Motorola	
	MC7447	Motorola	
	SN54LS247	† Motorola	
	SN54LS47	† Motorola	160
	SN74LS247	Motorola	
	SN74LS47	Motorola	
	DM5447A	† National	
	DM54LS247	† National	
	DM54LS47	† National	
	DM7447A	National	
	DM74LS247	National	
	DM74LS47	National	
	383A/C	Teledyne S	
	383B/M	† Teledyne S	170
	SN54247	**† TI** **(913)**	
	SN5447A	**† TI** **(847)**	
	SN54LS247	**† TI** **(913)**	
	SN54LS247A	**† TI** **(913)**	
	SN54LS47	**† TI** **(847)**	
	SN74247	**TI** **(913)**	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

IC MASTER

INTERFACE–Display Drivers (Cont'd)

Display Drivers (Cont'd)

Function	Device	Source		Line
BCD to 7-Segment Decoder/Driver, Active Low, Open Collector, 15 V Output (Cont'd)				
	SN7447A	**TI**	**(847)**	
	SN74L47	TI		
	SN74LS247	**TI**	**(913)**	
	SN74LS47	**TI**	**(847)**	
BCD to 7-Segment Decoder/Driver, Active Low, Open Collector, 30 V Output				
	5446	† Fairchild		
	7446	Fairchild		
	9317CC	Fairchild		
	9317CM	† Fairchild		
	HD7446A	Hitachi		
	MC5446	† Motorola		10
	MC7446	Motorola		
	DM5446A	† National		
	DM7446A	National		
	SN54246	**† TI**	**(913)**	
	SN5446A	**† TI**	**(847)**	
	SN74246	**TI**	**(913)**	
	SN7446A	**TI**	**(847)**	
BCD to 7-Segment Decoder/Driver, for Fluorescent Displays	CS250	Cherry		
	CS250-1	Cherry		
BCD to 7-Segment Decoder/Driver, for Liquid Crystal Displays	**CD4055B**	**† RCA**	**(748)**	20
	CD4055BE	**RCA**	**(748)**	
	TC4055B	Toshiba		
BCD to 7-Segment Decoder/Driver, 2-Digit, Direct Driver for Common Anode LED Displays	DS8669	National		
BCD to 7-Segment Latch/Decoder/Driver	CS260	Cherry		
BCD to 7-Segment Latch/Decoder/Driver (CMOS with bipolar output)	F4511BC	Fairchild		
	F4511BM	† Fairchild		
	HD14511B	Hitachi		
	MC14511BA	† Motorola		
	MC14511BC	Motorola		
	MC14513BA	† Motorola		30
	MC14513BC	Motorola		
	CD4511BC	National		
	CD4511BM	† National		
	CD4511B	**† RCA**	**(749)**	
	CD4511BE	**RCA**	**(749)**	
	883/4511B	† SSS		
	SCL4511B	SSS		
	CM4511B	† Solitron		
	CM4511BE	Solitron		
BCD to 7-Segment Latch/Decoder/Driver for Common Cathode LED Displays	NE589	Signetics		40
BCD to 7-Segment Latch/Decoder/Driver, for Liquid Crystal Displays	**CD4543BD**	**† RCA**	**(749)**	
	CD4543BE	**RCA**	**(749)**	
BCD to 7-Segment Latch/Decoder/Driver, Output 1-16	SAB3211	Siemens		
BCD to 7-Segment Latch/Decoder/Driver (ripple blanking)	MC14544BA	† Motorola		
	MC14544BC	Motorola		
BCD to 7-Segment Latch/Decoder/Driver (strobed latch), for Liquid Crystal Displays	**LS7100**	**LSI Comp**	**(696)**	
	MC14543BA	† Motorola		
	MC14543BC	Motorola		
	CD4056B	**† RCA**	**(748)**	
	CD4056BE	**RCA**	**(748)**	50
			(Continued)	

Function	Device	Source		Line
BCD to 7-Segment Latch/Decoder/Driver (strobed latch), for Liquid Crystal Displays (Cont'd)				
	883/4543B	† SSS		
	SCL4543B	SSS		
	TC4056B	Toshiba		
BCD to 7-Segment LED Decoder/Driver	CA3168	RCA		
BCD to 7-Segment LED Decoder/Driver, Constant Current	DS8857	National		
	NE587	Signetics		
BCD to 7-Segment LED Decoder/Driver with Latch, Output 0-9,–,E,H,L,P	9374C	Fairchild		
BCD to 7-Segment LED Driver Adjustable Current	DS8858	National		
BCD to 7-Segment LED Latch/Decoder/Driver, with Ripple Blanking	F4734BC	Fairchild		
	F4734BM	† Fairchild		60
BCD-to-Decimal Decoder/Driver (for lamps)	380A/C	Teledyne S		
	380B/M	† Teledyne S		
	381A/C	Teledyne S		
	381B/M	† Teledyne S		
BCD-to-Decimal Decoder/Driver (nixie driver)	7441	Fairchild		
	DM5441A	† National		
	DM7441A	National		
	382A/C	Teledyne S		
	382B/M	† Teledyne S		
BCD-to-Decimal Decoder/Driver with Blanking (for cold cathode indicator tubes)	54141	† Fairchild		70
	74141	Fairchild		
	HD74141	Hitachi		
	MC54141	† Motorola		
	MC74141	Motorola		
	DM54141	† National		
	DM74141	National		
	SN74141	**TI**	**(881)**	
Quad AC Plasma Display Axis Driver	SN55426B	† TI		
	SN55427B	† TI		
	SN75426	TI		80
	SN75427	TI		
Hex TTL to LED Bulb Driver, with Latch	DS8859	National		
	DS8869	National		
2-Digit, 7-Segment Decoder/Driver Interfaces to CPU	MN1205E	Panasonic		
	MN1205P	Panasonic		
	MN1205Q	Panasonic		
3 1/2-Digit Liquid Crystal Clock	C1200	LSI Comp		
4/5-Digit Fluorescent Display Driver	MM5474	National		
	MM5476	National		
	MM5477	National		90
	MM5478	National		
4/5-Digit (serial data input)	**MM5450**	**National**	**(735)**	
	MM5451	**National**	**(735)**	
4/5-Digit Vacuum Fluorescent	**MM5445**	**National**	**(735)**	
	MM5446	**National**	**(735)**	
	MM5447	**National**	**(735)**	
	MM5448	**National**	**(735)**	
	SAA1063	Signetics		
4x5 Matrix LED Decoder/Driver, Interface to CPU	MN1205F	Panasonic		

Function	Device	Source		Line
4x8 Matrix LED Decoder/Driver, Interface to MPU	MN1205A	Panasonic		100
4-Channel Incandescent Lamp Driver	CLD4	Teledyne C		
4-Channel Plasma	**XR2284**	**Exar**	**(3203)**	
4-Character, 18-Segment Triplexed LCD Decoder/Driver	ICM7233	Intersil		
4-Digit Fluorescent	ICM7235	Intersil		
	ICM7235A	Intersil		
	ICM7235AM	Intersil		
	ICM7235M	Intersil		
4-Digit Gas Discharge Display Anode Driver	DI500	Dionics		
	DI502	Dionics		
4-Digit LCD Decoder/Driver	SCL7211	SSS		110
4-Digit LCD Driver	ICM7211AM	Intersil		
	ICM7211M	Intersil		
4-Digit LED Driver	SDA2004	Siemens		
4-Digit LED Driver, Multiplexed BCD or Binary to 7-Segment Decoder/Driver	ICM7212	Intersil		
	ICM7212A	Intersil		
4-Digit LED Driver, BCD or Binary to 7-Segment Decoder/Driver, Data and Digit Select Code Latches for μP Interface	ICM7212AM	Intersil		
	ICM7212M	Intersil		
	UDN-7183	**Sprague**	**(2843)**	
	UDN-7184	**Sprague**	**(2843)**	
	UDN-7186	**Sprague**	**(2843)**	120
	UHP-482	**Sprague**	**(2843)**	
4-Digit Liquid Crystal, Multiplexed BCD to LCD Decoder/Driver, AC Drive	ICM7211	Intersil		
	ICM7211A	Intersil		
	DF412	Siliconix		
	SCL25411	SSS		
4-Digit/Segment Fluorescent	DI503	Dionics		
	DI504	Dionics		
4-Digit (stores segment and address data, drives 7-8 segment digits)	**MM74C911**	**National**	**(735)**	
4-Digit, 17-Segment Alpha-Numeric with Memory, Decoder and LED Drivers	MM74C956	National		
	NSM4307	National		130
	NSM4507	National		
4-Digit, 7-Segment LCD Decoder/Driver	**TSC7211A**	**Teledyne S**	**(2852)**	
4-Digit, 7-Segment LED Decoder/Driver	**TSC700A**	**Teledyne S**	**(2846)**	
	TSC8212A	Teledyne S		
4-Digit/8-Segment Fluorescent	COP470	National		
4-Segment Liquid Crystal	**CD4054B**	**RCA**	**(748)**	
	TC4054B	Toshiba		
4-Segment MOS to LED Anode Driver	75491	Fairchild		
	MC75491	Motorola		
	DS55493	† National		140
	DS75491	National		
	DS75493	National		
	SN75491	TI		
			(Continued)	

† Military Temperature Range (–55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Display Drivers (Cont'd)

Display Drivers (Cont'd)

Function	Device	Source		Line
4-Segment MOS to LED Anode Driver (Cont'd)				
	SN75491A	TI		
	SN75493	TI		
5x7 Dot Matrix LCD/Console Controller				
	CY300	Cybernetic		
5x8 Dot Matrix Multiplexed LCD. On-board memory allows ASCII code and special symbols display without refresh circuitry. (2-chip set)				
	PE7901	Polycore		
	PE7902	Polycore		
5x12 Dot Matrix (up to 80 characters by cascading)				
	10938	Rockwell		
	10939	Rockwell		
5-Character, 18-Segment Triplexed LCD Decoder/Driver				
	ICM7234	Intersil		
5-Digit Fluorescent				
	MSM58291G	OKI		
5-Digit Gas Discharge Display Anode Driver				
	UHD-490	† Sprague		10
	UHP-490	**Sprague**	**(2843)**	
5-Digit LCD Driver, Serial Input, Decoder				
	MSM5829G	OKI		
5-Line Plasma Display Axis Driver				
	DI5140	Dionics		
	DI5180	Dionics		
	DI5240	Dionics		
	DI5280	Dionics		
5-Segment Gas Discharge Display Cathode Driver				
	UHP-480	**Sprague**	**(2843)**	
5-Segment MOS to LED Anode Driver				
	DS8861	National		
5-Step Logarithmic Dual LED Driver				
	TA7666	Toshiba		
	TA7667	Toshiba		20
6-Digit Gas Discharge Display Anode Driver				
	DI505	Dionics		
	DI507	Dionics		
	DI603A	Dionics		
	DI604A	Dionics		
	DI605A	Dionics		
	DS8891	National		
	8891	Signetics		
	UDN-6164	**Sprague**	**(2843)**	
	UHD-491	† Sprague		
	UHP-491	**Sprague**	**(2843)**	30
	UHP-495	**Sprague**	**(2843)**	
	SN75481	TI		
6-Digit LED Driver (low voltage)				
	DS8646	National		
6-Digit MOS to LED Cathode Driver				
	55492A	† Fairchild		
	75492	Fairchild		
	75492A	Fairchild		
	MC75492	Motorola		
	DS75492	National		
	DS75494	National		
	DS8870	National		40
	DS8877	National		
	PS55494	† National		
	NE582-1	Signetics		
	SN75492	TI		
	SN75492A	TI		
	SN75494	TI		
6-Digit/Segment Fluorescent				
	DI508	Dionics		
	DI509	Dionics		
	UDN-6116	**Sprague**	**(2843)**	
	UDN-6126	**Sprague**	**(2843)**	50
6-Digit BCD (stores segment and address data, drives 7-8 segment digits)				
	MM74C912	**National**	**(735)**	
6-Digit Hex (stores segment and address data, drives 7 segments)	**MM74C917**	**National**	**(735)**	
6-Digit, 7-Segment LCD Driver with Decimal Points, or Three 16-Segment Characters. 48-Stage Shift Register, 48-Bit Data Latch and 48-Segment Driver				
	MSM5219	**OKI**	**(3873)**	
7-Digit Gas Discharge Display Anode Driver				
	MC3490	Motorola		
	MC3494	Motorola		
7-Digit MOS to Gas Discharge				
	XR2272	Exar		
7-Digit MOS to LED Cathode Driver				
	SN75497	TI		
7-Digit/Segment MOS to Fluorescent				
	XR2271	Exar		
7-Line Dot Matrix or Segmented				
	SN75581	**TI**	**(2863)**	
7-Segment Gas Discharge Display Cathode Driver				
	DS8885	National		60
	8885	Signetics		
	UHP-481	**Sprague**	**(2843)**	
	SN75584	TI		
7-Segment Gas Discharge Display Cathode Driver, with BCD Decoder	DS7880	† National		
	DS8880	National		
	DS8884A	National		
	DS8980	National		
	DS8880	Signetics		
	SN75480	TI		
7-Segment to BCD Converter/Driver				
	MM54C915	† National		70
	MM74C915	National		
8-Bit Parallel In/Parallel Out Fluorescent (for μP systems)				
	UCN-4815A	**Sprague**	**(2843)**	
	UCS-4815H	† Sprague		
8-Channel Plasma				
	XR2288	**Exar**	**(3203)**	
8-Digit Gas Discharge Display Anode Driver				
	DI510	Dionics		
	DI512	Dionics		
	DI803A	Dionics		
	DI804A	Dionics		
	DI805A	Dionics		
	DS8887	National		80
	DS8897	National		
	UDN-6184	**Sprague**	**(2843)**	
8-Digit MOS to LED Cathode Driver				
	DS8863	National		
	DS8871	National		
	DS8963	National		
8-Digit/Segment Fluorescent				
	DI513	Dionics		
	DI514	Dionics		
	DI514A	Dionics		
	XR6118	**Exar**	**(3205)**	
	XR6128	**Exar**	**(3205)**	90
	NE594	Signetics		
	SA594	Signetics		
	SG6118	Silicon G		
	UDN-6118	**Sprague**	**(2843)**	
	UDN-6128	**Sprague**	**(2843)**	
	UDN-6138	**Sprague**	**(2843)**	
	UDN-6148	**Sprague**	**(2843)**	
8-Digit, 7-Segment Triplexed LCD Decoder/Driver				
	ICM7231	Intersil		
8-Line Fluorescent Driver				
	MSL912R	**OKI**	**(3873)**	
	MSL915R	**OKI**	**(3873)**	100
	MSL916R	OKI		
	MSL917R	**OKI**	**(3873)**	
8-Output Digit-Scan Counter/Decoder for Cold-Cathode Counter Tubes				
	MSL9510R	**OKI**	**(3873)**	
	MSL9511R	**OKI**	**(3873)**	
8-Segment Gas Discharge Display Cathode Driver				
	DI210	Dionics		
	DI2210	Dionics		
	DI230	Dionics		
	DI240	Dionics		
	DI300	Dionics		
	DI302	Dionics		110
	MC3491	Motorola		
	MC3492	Motorola		
	DS7889	† National		
	DS8889	National		
	UDN-7180	**Sprague**	**(2843)**	
8-Segment MOS to LED Anode Driver				
	MC676	Motorola		
	DS8867	National		
9-Digit MOS to LED Cathode Driver				
	DS8872	National		
	DS8920	National		
	DS8973	National		120
	DS8975	National		
	SN75498	TI		
9-Digit MOS to LED Cathode Driver, with Low Battery Indicator	DS8864	National		
	DS8873	National		
9-Digit MOS to LED Cathode Driver with Shift Register Decoding	DS8874	National		
9-Line, 30 LED	U1096B	Telefunken		
9-Segment LED Driver (low voltage)				
	DS8647	National		
	DS8648	National		
10-Bit High-Voltage, High-Current				
	S4534	**AMI**	**(2611)**	
10-Bit Serial In/Parallel Out Fluorescent (for μP systems)				
	UCN-4810A	**Sprague**	**(2843)**	130
	ULN-4810H	† Sprague		
	UCN4810A	TI		
10-Digit, 7-Segment Triplexed LCD Decoder/Driver				
	ICM7232	Intersil		
11-Segment LED Display Drivers				
	MM5485	National		
12-Line Vacuum Fluorescent				
	SN75512A	TI		
	SN75513A	**TI**	**(2861)**	
14-Digit Decoder/Driver				
	DS8665	National		
	DS8666	National		
14-Digit Decoder/Driver, with Low Battery Indicator				
	DS7664	† National		
	DS8664	National		140
14-Segment Decoder/Driver, Interface to CPU				
	MN1205H	Panasonic		
16-Line Fluorescent				
	DS8881	National		
	8881	Signetics		
16-Segment LED Display Drivers				
	MM5484	National		
18-Segment Alphanumeric				
	AC5947	TI		
18-Segment, 16-Character Alphanumeric (30, 35 and 40 volt versions)	10937	Rockwell		

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

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ABBREVIATIONS OF COMPANY NAMES

Action Ins	Action Instruments
AD	Analog Devices
ADT	Advanced Digital Technology
Adapt Sci	Adaptive Science Corp.
Advent	Advent Products, Inc.
Alphatron	Alphatron
AMA	American Automation
AMD	Advanced Micro Devices
AMI	American Microsystems, Inc.
Amperex	Amperex Electronic Corp.
Analogic	Analogic
Analog Sys	Analog Systems
APC	Applied Micro Circuits
Apex	Apex Microtechnology
APM	Applied Microsystems Corp.
Appl Sys	Applied Systems Corp.
APT	Applied Microtechnology
Aptek	Aptek Microsystems
Array Tech	Array Technology
AWI	Analog West
Bedford	Bedford Computer Systems Inc.
Burr-Brown	Burr-Brown Research
CAE	Computer Aided Engineering
Cal Devices	California Devices
Cent Data	Central Data Corp.
Cermetek	Cermetek
CGRS	CGRS Microtech Inc.
Cherry	Cherry Semiconductor
CIC	Custom Integrated Circuits
Citel	Citel, Inc.
Comlinear	Comlinear Corporation
CMA	Custom MOS Arrays
Comark	Comark Corp.
Comdial	Comdial Semiconductor
Comp Auto	Computer Automation
Compas	Compas Microsystems
Cont Logic	Control Logic Inc.
Control Sys	Control Systems Microsystems Div.
CreMicro	Creative Micro Systems
Cromemco	Cromemco, Inc.
CSG	Commodore Semiconductor Group
Cubit	Cubit Inc.
Curtis	Curtis Electro Devices, Inc.
Cybernetic	Cybernetic Micro Systems
Cybersys	Cybersystems
Cybertek	Cybertek Inc.
Data General	Data General
Data I/O	Data I/O
Data Trans	Data Translation
Datel	Datel-Intersil
Datricon	Datricon Corporation
DDC	Data Devices Corporation
DEC	Digital Equipment Corporation
Delco	Delco Electronics
DGM	Digital Microsystems
Digelec	Digelec Corp.
Digitek	Digitek, Inc.
Dionics	Dionics Inc.
Dist Comp	Distributed Computer Systems
Divers Tech	Diversified Technology
E-HI	E-H International, Inc.
Elind	Elind Elettronica Industriale
EL Instr	E & L Instruments
EMM	EMM
Emulogic	Emulogic Inc.
Epson	Epson America, Inc.
ETI Micro	ETI Micro
Exar	Exar Integrated Systems
Fairchild	Fairchild
Ferranti	Ferranti Electric
Fujitsu A	Fujitsu America
Fujitsu	Fujitsu Microelectronics, Inc.
GI	General Instrument
GMS	General Microsystems
GTE Micro	GTE Microcircuits
Harris	Harris Semiconductor
Heurikon	Heurikon Corp.
Hilevel	Hilevel Technology, Inc.
Hitachi	Hitachi America, Ltd.
Holt	Holt Inc.
HP	Hewlett-Packard
Hughes	Hughes Aircraft, Solid State Products
Hybrid Sys	Hybrid Systems
Hycom	Hycom Incorporated
IDT	Integrated Device Technology
IMI	International Microcircuits, Inc.
IMP	International Microelectronic Products
IMS	Industrial Micro-systems Inc.
Inconix	Inconix Corporation
Ind Tech	Inductive Technology
Inmos	Inmos
IntCirEng	Integrated Circuit Engineering
IntCirSys	Integrated Circuit Systems
IntCompSys	Integrated Computer Systems
IntCyber	International Cybernetics
Int Micro	International Microsystems
Int Tech	Integrated Technology Corp.
Intech/FMI	Intech/Function Modules Inc.
Intel	Intel
Interdesign	Interdesign
Intersil	Intersil
Intronics	Intronics
IPI	Integrated Photomatrix Inc.
ITT	ITT Semiconductors
Kinetic Sys	Kinetic Systems
Kontron	Kontron Electronics
Lambda	Lambda Semiconductor
Laserdyne	Laserdyne
LSI Comp	LSI Computer Systems
LSI Logic	LSI Logic Corporation
Master Logic	Master Logic Corporation
Matrix	Matrix Corp.
Matrox	Matrox Electronic Systems
MCC	Microcomputer Control
Micrel	Micrel
Micro Eng	Micro Circuit Engineering
Micro Innov	Micro Innovators
Micropac	Micropac Industries
Micro Net	Micro Networks
Micro Pwr	Micro Power Systems
Micro Sci	Micro Sciences Corp.
Micro Tech	Microcircuits Technology
Micro-Link	Micro-Link Corporation
Micron	Micron Technology
MilerTron	MilerTronics
Miller	Miller Technology
Mitel	Mitel Semiconductor
Mitsubishi	Mitsubishi Electronics
MMI	Monolithic Memories, Inc.
Monosil	Monosil
MonSys	Monolithic Systems Corp.
Mostek	Mostek
Motorola	Motorola Semiconductor
MRC	MRC Systems
Murray	Murray Consulting
National	National Semiconductor
NCR	NCR Corp., Microelectronics Division
NEC-EA	NEC/Electronic Arrays Division
NEC Electron	NEC/Electron Division
NEC Micro	NEC/Microcomputer Division
Nitron	Nitron
Nortek	Nortek
OAE	Oliver Advanced Engineering
Octagon	Octagon Systems Corp.
OEI	Optical Electronics Inc.
Ohio Sci	Ohio Scientific
OKI	OKI Semiconductor
Omnibyte	Omnibyte Corp.
Oscar	I. S. Oscar Assoc.
Panasonic	Panasonic
PC/M	Pacific/Cyber Metrix
Percom	Percom Data Co.
Phoenix	Phoenix Digital Corp.
Pico Design	Pico Design
Polycore	Polycore Electronics
Plessey	Plessy Semiconductors
PMI	Precision Monolithics, Inc.
PragDes	Pragmatic Design Inc.
PREMA	PREMA GmbH
Pro-Log	Pro-Log Corp.
Quay	Quay Corp.
Raytheon	Raytheon Semiconductor
RCA	RCA Solid State Division
RCI Data	RCI Data
RELMS	Relational Memory Systems
Reticon	Reticon
RIFA	RFIA
Rockwell	Rockwell, Microelectronic Devices
RTC	Riehl Time Corporation
Sanken	Sanken Electric
Sanyo	Sanyo
SEEQ	SEEQ Technology, Inc.
Semi Proc	Semi Processes
Siemens	Siemens
Signetics	Signetics
SGS	SGS-ATES Semiconductor
Sharp	Sharp
Silicon G	Silicon General
Siliconix	Siliconix
Silicon Sys	Silicon Systems Inc.
Siltronics	Siltronics
SMC	Standard Microsystems Corp.
Solarise	Solarise Enterprises
Solitron	Solitron Devices
Sprague	Sprague Electric Company
SSM	Solid State Micro Technology for Music
SSS	Solid State Scientific
Stag	Stag Microsystems
Struc. Des.	Structured Design Inc.
Stynetic	Stynetic Systems
Sunrise	Sunrise Electronics
Sunshine	Sunshine Semiconductor
Supertex	Supertex Inc.
Symtek	Symtek Corp.
Synapse	Synapse Corp.
Synertek	Synertek
Sys Innov	Systems Innovations
Tau Zero	Tau Zero Inc.
Tektronix	Tektronix
Telaris	(See Laserdyne)
Teledyne C	Teledyne Crystalonics
Teledyne P	Teledyne Philbrick
Teledyne S	Teledyne Semiconductor
Telefunken	Telefunken
Telephonics	Telephonics LSI
Telmos	Telmos
Teltone	Teltone Corporation
TI	Texas Instruments
Thomson-CSF	Thompson-CSF Components Corp.
TMX	TMX
Topanga	Topanga Data Systems
Toshiba	Toshiba America
Trans-Data	Trans-Data
TRW	TRW-LSI Products
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INTERFACE–Display Drivers (Cont'd)

Function	Device	Source		Line
Display Drivers (Cont'd)				
30-Bit LCD Driver/Register				
	MD4330B	Mitel		
32 Segment LCD				
	MM5452	**National**	**(735)**	
	MM5453	**National**	**(735)**	
	PCE2112	Signetics		
32-Bit High-Voltage				
	S4521	**AMI**	**(2610)**	
	S4535	**AMI**	**(2609)**	
32-Bit LCD	MM58438	National		
32-Line AC Plasma Display Axis Driver				
	SN75500	TI		
	SN75501	TI		
	SN75502	TI		10
	SN75503	TI		
32-Line Vacuum Fluorescent				
	SN75518	**TI**	**(2862)**	
32-Segment LCD Controller/Driver				
	μPD7255	NEC-Micro		
32-Segment LCD Driver				
	MM5483	National		
40-Segment LCD Duplex				
	PCE2100	Signetics		
60-Segment LCD Duplex				
	PCE2110	Signetics		
64-Segment LCD Duplex				
	PCE2111	Signetics		

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Error Checking Circuits

Function	Max. Serial Data Rate, MHz	Supply Voltage, V	Device	Source	Line
Error Checking Circuits					
CRCC Generator	2 *	5	COM8004	SMC	
	3	5	MC8500	Motorola	
			SSI8500	Silicon Sys	
	10	5	9401C	Fairchild	
			9401M	† Fairchild	
			9411C	Fairchild	
			9411M	† Fairchild	
			8X01A	Signetics	
			N9401	**Signetics (1514)**	
Deskew-Queue Register	3 *	5	MC8520	Motorola	10
			SSI8520	Silicon Sys	
Error Detection/Correction Circuit	—	5	**WD8206**	**Western (3995)**	
Error Detection/Correction Circuit (ECL)	—	−5.2	MC10163	Motorola	
			MC10193	Motorola	
			MC10563	† Motorola	
			MC10593	Motorola	
Error Detection/Correction Circuit (TTL)	—	5	9428	Fairchild	
			SN74ALS790	**Motorola (732)**	
			SN54LS630	**† TI (440,979)**	
			SN54LS631	**† TI (440,979)**	20
			SN74LS630	**TI (979)**	
			SN74LS631	**TI (979)**	
		7	MB1412A	Fujitsu	
Error Pattern Register	3	5	MC8501	Motorola	
Expandable Error Checker and Corrector	—	5	**DP8400**	**National (2764)**	
LRCC Data Register	3	5	MC8502	Motorola	
			SSI8502	Silicon Sys	
Polynominal Generator	4 *	5	MC8506	Motorola	
Polynominal Generator/Checker	3.5 *	5	**MC2653**	**Motorola (1360)**	
			MC68653	**Motorola (1360)**	30
			MC8503	Motorola	
	4	5	2653	Signetics	
Universal Polynominal 4-Bit Generator	17 *	5	MC8504	Motorola	
Single Error Hamming Code Detector and Generator	—	5	MC4041	Motorola	

† Military Temperature Range (−55° to 125°C)

* Typical Value

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INTERFACE–Keyboard Encoder-Decoders

No. of Keys	No. of Output Bits	Code	Max. Clock Rate, KHz	Supply Voltage, V	Comments	Device	Source		Line
Keyboard Encoder- Decoders									
16	4	Binary	—	3-15	2 key rollover, 3 state output	MM54C922 MM74C922	† National National		
		External ROM Programmable	—	5	Antibounce, mute, interlock	M190	SGS		
		1 of 16	—	5	Strobe output, key rollover output, 2 of 8 keyboard to binary encoder, one of four row inputs and column inputs (telephone key pads) give binary output, strobe.	**HD0165** **MC14419**	**Harris** **Motorola**	**(2733,3287)** **(3298)**	
20	5	Binary	—	3-15	2 key rollover, 3 state output	MM54C923 MM74C923	† National National		
85	8	ASCII/HEX	1000	4-10.5	Scans and generates code for 53 key ASCII plus 32 non-ASCII keys	**CDP1871** **CDP1871D**	**RCA** **†RCA**	**(1484)** **(1484)**	
				4-6.5	Scans and generates code for 53 key ASCII plus 32 non-ASCII keys	**CDP1871C** **CDP1871CD**	**RCA** **†RCA**	**(1484)** **(1484)**	10
88	8 plus Parity	Mask, Programmable	100	– 12.5	Programmable parity, strobe width, strobe delay. Two key rollover. 8 x 11 matrix, 3 levels.	KR2376	SMC		
90	10	External ROM Programmable	100	– 12.5	9 x 10 matrix, 4 Mode, 2 or N key rollover	KR3600-PRO	SMC		
		Mask, Programmable	100	– 12.5	9 x 10 matrix, 4 Mode, 2 or N key rollover	KR3600	SMC		
112	10	Mask Programmable	66	5	112 bits for internal programming of function keys	AY3-4592	GI		
128	8	Mask Programmable	400	5	16 x 18 matrix, 8-Bit bus interface, 4 rollover modes, UART on chip	**SCN2671A**	**Signetics**	**(1522)**	
	9	Mask Programmable	100	5	16 x 18 matrix, three-state I/O, 2 or 3 key alarm	**MSM3914A**	**OKI**	**(3873)**	

† Military Temperature Range (– 55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Line Circuits

No. Per Device	Output	Party Line	Supply Voltage, V	Comments	Device	Source	Line
Line Drivers—Single Ended							
2	High Current	Yes	5	Coax/Twisted Pair	MC8T23	Motorola	
					DS75123	National	
					N8T23	Signetics	
					N8T23	TI	
					S8T23	TI	
					SN75123	TI	
				Emitter Follower for Coax/Twisted Pair	MC8T13	Motorola	
					DS55121	† National	
					DS75121	National	
					N8T13	Signetics	10
					S8T13	Signetics	
					N8T13	TI	
					SN55121	† TI	
					SN75121	TI	
	−0.5 to 5.5 V	No	5	RS422A, RS423A	μA9639C	TI	
	±4 to 6 V	No	±9 to ±15	RS232, RS423, CCITT V.26, V.28	9636AC	Fairchild	
					9636AM	† Fairchild	
					μA9636A	TI	
	±6 V	No	±12	4 Input	N8T15	Signetics	
	±8 V	No	±12	RS232C	75150	Fairchild	20
					DS75150	National	
					SN55150	† TI	
					SN75150	TI	
3	High Current	No	5	IBM360	HD2904	Hitachi	
	±6 V	No	±12	RS232B/C, CCITT, MIL188	9616	Fairchild	
					9616E	Fairchild	
					9616M	† Fairchild	
4	TTL	No	5	Active Pull-Up	AM2614C	AMD	
					AM2614M	† AMD	
		Yes	5	DS7831 w/o Vcc Clamp	DS7832	† National	30
					DS8832	National	
					DS8832	TI	
				Three-State	RC8T09	Raytheon	
					RM8T09	† Raytheon	
					N8T09	Signetics	
					S8T09	† Signetics	
				2-Input NAND, 80 Ma	96101C	Fairchild	
					96101M	† Fairchild	
				4-Input AND, NAND	DS7831	† National	
					DS8831	National	40
					DS8831	TI	
	0.15 to 4 V	No	7	IBM360/370	**MC3481**	**Motorola** (2753)	
					MC3485	**Motorola** (2753)	
	3.11	No	5	IBM360/370	SN75126	TI	
					SN75130	TI	
	−7 to 12	Yes	5	RS422, Three-State	SN75174	TI	
	−7 to ±12	Yes	5	RS422, Three-State	SN75172	TI	
	±4 to 6 V	No	±5	RS423, RS422 with mode control	DS3691	National	
			±5.5	RS423, RS422 with mode control	DS1691	† National	
		Yes	±5	RS423, Three-State	AM26LS29C	AMD	50
					AM26LS29	Signetics	
			±5.5	RS423, Three-State	AM26LS29M	† AMD	
	±6 to 9 V	No	±9 to ±15	RS232C, CCITT V.24	**XR1488**	**Exar** (3188)	
					μA1488	Fairchild	
					HD75188	Hitachi	
					MC1488	**Motorola** (2753)	
					DS1488	National	
					MC1488	Signetics	
					SG1488	Silicon G	
					MC1488	TI	60
					SN55188	† TI	
					SN75188	TI	
	±4 to 6 V	No	±5	RS423, RS422 with mode control	AM26LS30C	AMD	
					AM26LS30	Signetics	
			±5.5	RS423, RS422 with mode control	AM26LS30M	† AMD	

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

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INTERFACE–Line Circuits (Cont'd)

No. Per Device	Output	Party Line	Supply Voltage, V	Comments	Device	Source		Line
Line Drivers—Single Ended							**(Cont'd)**	
6	NTDS	No	5, −15	NTDS	MOA-268B	† Interdesign		
			5, −5	NTDS Hex Driver	MOF1305B	† Interdesign		
8	TTL	Yes	5	Three-State (also see index for 74S244, 74LS244, 67S304, 67LS304)	AM25LS241C	AMD		
					AM25LS241M	† AMD		
					AM25LS244C	AMD		
					AM25LS244M	† AMD		
					SN54LS241	† AMD		
					SN54LS244	† AMD		
					SN54S241	† AMD		
					SN54S244	† AMD		10
					SN74LS241	AMD		
					SN74LS244	AMD		
					SN74S241	AMD		
					SN74S244	AMD		
					54LS241	† Fairchild		
					54LS541	† Fairchild		
					74LS241	Fairchild		
					74LS244	Fairchild		
					74LS541	Fairchild		
					HD74LS241	Hitachi		20
					HD74LS244	Hitachi		
					M74LS244	Mitsubishi		
					SN54LS241	**† MMI**	**(715)**	
					SN54LS244	**† MMI**	**(715)**	
					SN54LS245	**† MMI**	**(715)**	
					SN54LS341	**† MMI**	**(715)**	
					SN54LS344	**† MMI**	**(715)**	
					SN54S241	**† MMI**	**(715)**	
					SN54S244	**† MMI**	**(715)**	
					SN74LS241	**MMI**	**(715)**	30
					SN74LS244	**MMI**	**(715)**	
					SN74LS245	**MMI**	**(715)**	
					SN74LS341	**MMI**	**(715)**	
					SN74LS344	**MMI**	**(715)**	
					SN74S241	**MMI**	**(715)**	
					SN74S244	**MMI**	**(715)**	
					SN54LS241	† Motorola		
					SN54LS244	† Motorola		
					SN54LS541	† Motorola		
					SN74LS241	Motorola		40
					SN74LS244	Motorola		
					SN74LS541	Motorola		
					DM54S241	† National		
					DM74S241	National		
					MM54C941	† National		
					MM74C941	National		
					74LS241	Signetics		
					74LS244	Signetics		
					74LS541	**Signetics**	**(2775)**	
					SN54ALS241	**† TI**	**(911)**	50
					SN54ALS244	**† TI**	**(912)**	
					SN54LS241	**† TI**	**(911)**	
					SN54LS244	**† TI**	**(912)**	
					SN54LS541	**† TI**	**(960)**	
					SN54S241	**† TI**	**(911)**	
					SN74ALS241	**TI**	**(911)**	
					SN74ALS244	**TI**	**(912)**	
					SN74LS241	**TI**	**(911)**	
					SN74LS244	**TI**	**(912)**	
					SN74LS541	**TI**	**(960)**	60
					SN74S241	**TI**	**(911)**	
				Three-State, Inverting	AM25LS240C	AMD		
					AM25LS240M	† AMD		
					SN54LS240	† AMD		
					SN54S240	AMD		
					SN74LS240	AMD		
					SN74S240	AMD		
					54F240	**† Fairchild**	**(630)**	
					54LS240	† Fairchild		

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

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INTERFACE–Line Circuits (Cont'd)

No. Per Device	Output	Party Line	Supply Voltage, V	Comments	Device	Source		Line
Line Drivers—Single Ended							**(Cont'd)**	
8	TTL	Yes	5	Three-State, Inverting			(Cont'd)	
					54LS540	† Fairchild		
					74F240	**Fairchild**	**(630)**	
					74LS240	Fairchild		
					74LS540	Fairchild		
					M74LS240	Mitsubishi		
					SN54LS240	**† MMI**	**(715)**	
					SN54LS340	**† MMI**	**(715)**	
					SN54S240	**† MMI**	**(715)**	
					SN74LS240	**MMI**	**(715)**	
					SN74S240	**MMI**	**(715)**	10
					SN54LS240	† Motorola		
					SN54LS540	† Motorola		
					SN74LS240	Motorola		
					SN74LS540	Motorola		
					DM54S240	† National		
					DM74S240	National		
					54LS540	**† Signetics**	**(2775)**	
					74LS240	Signetics		
					74LS540	**Signetics**	**(2775)**	
					SN54ALS240	**† TI**	**(910)**	20
					SN54LS240	**† TI**	**(910)**	
					SN54LS540	**† TI**	**(960)**	
					SN54S240	**† TI**	**(910)**	
					SN74ALS240	**TI**	**(910)**	
					SN74LS240	**TI**	**(910)**	
					SN74LS540	**TI**	**(960)**	
					SN74S240	**TI**	**(910)**	
16	TTL	Yes	5	Three-State	**SN54LS365A**	**† TI**	**(935)**	
					SN54LS367A	**† TI**	**(936)**	
					SN74LS365A	**TI**	**(935)**	30
					SN74LS367A	**TI**	**(936)**	
				Three-State, Inverting	**SN54LS366A**	**† TI**	**(935)**	
					SN54LS368A	**† TI**	**(936)**	
					SN74LS366A	**TI**	**(935)**	
					SN74LS368A	**TI**	**(936)**	
Line Drivers—Differential								
See also Drivers under digital logic families								
2	High Current CMOS							
		No	3-15	CMOS 50 mA, 4-Input AND, NAND	MM78C30	† National		
					MM88C30	National		
	High Current TTL	No	5	40 mA, Active Pull-up/Pull-down	9612C	Fairchild		
				40 mA, Open Collector/Active Pull-up	9614C	Fairchild		40
					9614M	† Fairchild		
					DS55114	† National		
					DS75114	National		
					9614C	TI		
					SN55114	† TI		
					SN75114	TI		
				40 mA, RS422	SN55128	† TI		
					SN75158	TI		
				40 mA, 4-Input AND, NAND	54S140	† Fairchild		
					74S140	Fairchild		50
					HD74S140	Hitachi		
					DM74S140	National		
					DS7830	† National		
					DS8830	National		
					54S140	† Signetics		
					74S140	Signetics		
					DS8830	TI		
					SN54S140	**† TI**	**(881)**	
					SN55183	† TI		
					SN74S140	**TI**	**(881)**	60
					SN75183	TI		
		Yes	5	Three-State	DS7831	† National		
					DS8831	National		
					DS8831	TI		

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

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INTERFACE–Line Circuits (Cont'd)

No. Per Device	Output	Party Line	Supply Voltage, V	Comments	Device	Source		Line
Line Drivers—Differential							**(Cont'd)**	
2	High Current TTL	Yes	5				(Cont'd)	
				DS7831 w/o Vcc Clamp	DS7832	† National		
					DS8832	TI		
				40 mA, Open Collector/Active Pull-Up, Three-State	DS55113	† National		
					DS75113	National		
					SN55113	† TI		
					SN75113	TI		
				40 mA, RS422, Three-State	9634C	Fairchild		
					9634M	† Fairchild		
					DS8832	National		
					SN75159	TI		10
	2.5 to 3.5	No	5	High Speed	μA9638C	TI		
	3.5 mA	Yes	±5	Twisted Pair	HD75109	Hitachi		
					MC75109	Motorola		
					SN55109A	† TI		
					SN74109A	**TI**	**(870)**	
	6.5 mA	Yes	±5	Twisted Pair, Level Shifting	55110A	† Fairchild		
					75110A	Fairchild		
					HD75110	Hitachi		
					MC75110	Motorola		
					MC75S110	Motorola		20
					SN55110A	† TI		
					SN75110A	TI		
	18 mA	Yes	±5	Higher Current 75110	SN75112	TI		
	±3 V	Yes	±5	RS422 at Low Data Rates, RS423	AM26LS30C	AMD		
					AM26LS30	Signetics		
			±5.5	RS422 at Low Data Rates, RS423	AM26LS30M	† AMD		
	±5V	No	±15, ±5	ARING 429, 1000K bits data rate	HS3182	† Harris		
4	High Current CMOS							
		No	3-15	CMOS, 25 mA	MM78C29	† National		
					MM88C29	National		
	High Current TTL	No	5	50 Ohm Lines	74128	Signetics		30
					SN74128	**TI**	**(876)**	
				75 Ohm Lines	54128	† Signetics		
					SN54128	**† TI**	**(876)**	
		Yes	5	RS-422, RS-423, Three-State	MC3487	Motorola		
					DS3487	National		
					MC3487	TI		
				Three-State	DS1688	† National		
	11 mA	Yes	±5	Quad 75110	MC3453A	Motorola		
	20 mA	Yes	5	MIL188-114, Three-State	DS1692	† National		
					DS3692	National		40
				RS-422, Three-State	AM26LS31C	AMD		
					AM26LS31M	† AMD		
					AM26LS31	**Motorola**	**(2753)**	
					AM26LS31C	**Motorola**	**(2753)**	
					AM26LS31M	**† Motorola**	**(2753)**	
					DS26LS31C	† National		
					DS26LS31M	National		
					AM26LS31	Signetics		
					AM26LS31C	TI		
					AM26LS31M	† TI		50
	40 mA	Yes	5	RS-422, Fed. 1020, Three-State	SN75151	TI		
					SN75153	TI		

† Military Temperature Range (−55° to 125°C)

* Typical Value

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INTERFACE–Line Circuits (Cont'd)

No. Per Device	Receiver Input Threshold	Common Mode Voltage, V	Supply Voltage, V	Comments	Device	Source	Line
Line Receivers—Single Ended							
Also see Line Receivers-Differential							
2	0.4 to 2.4	± 15	5	Differential Input, Single Ended Data	AM2615C	AMD	
					AM2615M	† AMD	
	±0.1 V (ref)		5	Ext. Ref. Adj. 1.5 to 3.5 V with Optional Internal 2.5 V Reference	SN55142A	† TI	
					SN55143A	† TI	
					SN75142A	TI	
					SN75143A	TI	
				Ext. Reference Adjustable from 1.5 to 3.5 V	MC75140	Motorola	
					SN55140	† TI	
					SN55141	† TI	10
					SN75140	TI	
					SN75141	TI	
	±2.0		5	Hysteresis, EIA/MIL RS232B	N8T16	Signetics	
					DS7822	† National	
					DS8822	National	
3	0.7 to 1.7		5	Hysteresis, IBM360/370	MC8T24	Motorola	
					DS75124	National	
					N8T24	Signetics	
					SN75124	TI	
	0.75 to 2.25		5	Hysteresis, RS232C, CCITT V.24	9617C	Fairchild	20
	0.8 to 2.0 V		5	Hysteresis, High-Speed	MC8T14	Motorola	
					DS55122	† National	
					DS75122	National	
					N8T14	Signetics	
					SN55122	† TI	
					SN75122	TI	
	0.86 to 2.40		5	High-Speed	HD2915	Hitachi	
	1.15 to 1.55		5	IBM360	HD2905	Hitachi	
4	0.75 to 1.5 V		5	RS232C, Programmable Threshold, Hysteresis	μA1489	Fairchild	
					HD75154	Hitachi	30
					MC1489	**Motorola** (2753)	
					DS1489	National	
					MC1489	Signetics	
					SG1489	Silicon G	
					SN55189	† TI	
					SN75189	TI	
	0.75 to 2.25		5	RS232C, Programmable Threshold, Wider Hysteresis than 1489	**XR1489A**	**Exar** (3188)	
					μA1489A	Fairchild	
					HD75189	Hitachi	
					MC1489A	**Motorola** (2753)	40
					DS1489A	National	
					MC1489A	Signetics	
					SG1489A	Silicon G	
					SN55189A	† TI	
	0.97 to 2.65		5	Hysteresis, 120 Ohm System	DS7836	† National	
	1.05 to 2.5		5	Hysteresis, 120 Ohm System	DS8836	National	
	1.2 to 1.8		5	120 Ohm System, No Hysteresis, NOR Input	DS7640	National	
	1.3 to 1.7		5	120 Ohm System, No Hysteresis, NOR Input	DS8640	Fairchild	
	1.7		5	No Hysteresis, NOR Input	96106		50
	1.75 to 2.25 V		5	RS232C, Programmable Threshold, Hysteresis	SN75189	TI	
	5 to 7.5		15	Hysteresis, Interface to CMOS	367A		
					367	Fairchild	
				Hysteresis, Open Collector, Interface to CMOS		National	
	5.5 to 8		12	Hysteresis, Open Collector, Interface to CMOS		Silicon G	
				Hystersis, Interface to CMOS		Silicon G	
	± 3/0.8 to 3		5 or 12	RS232C, Hysteresis, Fail Safe Option		† TI	60
						TI (885)	
						† National	
						Motorola	
6	0.97 to 2.65		5	Hysteresis, 120 Ohm System		(Continued)	
	1.05 to 2.50		5	Hysteresis, 120 Ohm System			

† Military Temperature Range (−55° to 125°C)

* Typical Value

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INTERFACE-Line Circuits (Cont'd)

No. Per Device	Receiver Input Threshold	Common Mode Voltage, V	Supply Voltage, V	Comments	Device	Source	Line
Line Receivers—Single Ended						**(Cont'd)**	
6	1.05 to 2.50		5	Hysteresis, 120 Ohm System		(Cont'd)	
					DS8837	National	
					N8T37	Signetics	
	−1 to 4.5/-1.5 to 13						
			5	NTDS	MOB-272	† Interdesign	
7	0.7 to 1.7		5	IBM360/370	**MC75125**	**Motorola (2753)**	
					MC75127	**Motorola (2753)**	
					DS75125	National	
					DS75127	National	
					SN75125	TI	
					SN75127	TI	
8	0.7 to 1.7		5	IBM360/370	**MC75128**	**Motorola (2753)**	10
					MC75129	**Motorola (2753)**	
					DS75128	National	
					DS75129	National	
					SN75128	TI	
					SN75129	TI	
Line Receivers—Differential							
See also Receivers-listed under Digital-ECL and Digital-HNIL/HTL Miscellaneous sections							
2	±0.010	±3	±5	10 mV, MOS Sense, Active Pull-up	DS75207	National	
					DS75208	National	
					SN75207	TI	
				10 mV, MOS Sense, Open Collector	SN75208	TI	20
				10 mV, MOS Sense, Three-State	DS3604	National	
				75207 with Diode Protected Input Stage	SN75207B	TI	
				75208 with Diode Protected Input Stage	SN75208B	TI	
	±0.025	±3	±5	25 mV, Active Pull-up	55107A	† Fairchild	
					75107A	Fairchild	
					HD75107A	Hitachi	
					MC55107	† Motorola	
					MC75107	Motorola	
				25 mV, Active Pull-Up	DS55107	† National	
					DS75107	National	30
				25 mV, Active Pull-up	SN55107A	† TI	
					SN75107A	TI	
				25 mV, Open Collector	HD75108A	Hitachi	
					MC55108	† Motorola	
					MC75108	Motorola	
					DS55108	† National	
					DS75108	National	
					SN55108A	† TI	
					SN75108A	TI	
				25 mV, Three-State 55107	DS1603	† National	40
					DS3603	National	
				55107A with Diode Protected Input Stage	75107B	Fairchild	
					DS55107	† National	
					DS75107	National	
					SN55107B	† TI	
					SN75107B	TI	
				55108A with Diode Protected Input Stage	75108B	Fairchild	
					DS55108	† National	
					DS75108	National	
					SN55108B	† TI	50
					SN75108B	TI	
		10/15	5	Twisted Pair, ± 15 V CMV. Response Control	DS78LS120	† National	
					DS88LS120	National	
			5	CMOS Compatible, Response Control	DS78C120	† National	
					DS88C120	National	
			5	RS232, RS422/3	9637AC	Fairchild	
					9637AM	† Fairchild	
					SN55157	† TI	
					SN75157	TI	
					μA9637AC	TI	60
						(Continued)	

† Military Temp

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* Typical Value

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INTERFACE–Line Circuits (Cont'd)

No. Per Device	Receiver Input Threshold	Common Mode Voltage, V	Supply Voltage, V	Comments	Device	Source	Line
Line Receivers—Single Ended							
Also see Line Receivers-Differential							
2	0.4 to 2.4	± 15	5	Differential Input, Single Ended Data	AM2615C	AMD	
					AM2615M	† AMD	
	±0.1 V (ref)		5	Ext. Ref. Adj. 1.5 to 3.5 V with Optional Internal 2.5 V Reference	SN55142A	† TI	
					SN55143A	† TI	
					SN75142A	TI	
					SN75143A	TI	
				Ext. Reference Adjustable from 1.5 to 3.5 V	MC75140	Motorola	
					SN55140	† TI	
					SN55141	† TI	10
					SN75140	TI	
					SN75141	TI	
	±2.0		5	Hysteresis, EIA/MIL RS232B	N8T16	Signetics	
					DS7822	† National	
					DS8822	National	
3	0.7 to 1.7		5	Hysteresis, IBM360/370	MC8T24	Motorola	
					DS75124	National	
					N8T24	Signetics	
					SN75124	TI	
	0.75 to 2.25		5	Hysteresis, RS232C, CCITT V.24	9617C	Fairchild	20
	0.8 to 2.0 V		5	Hysteresis, High-Speed	MC8T14	Motorola	
					DS55122	† National	
					DS75122	National	
					N8T14	Signetics	
					SN55122	† TI	
					SN75122	TI	
	0.86 to 2.40		5	High-Speed	HD2915	Hitachi	
	1.15 to 1.55		5	IBM360	HD2905	Hitachi	
4	0.75 to 1.5 V		5	RS232C, Programmable Threshold, Hysteresis	μA1489	Fairchild	
					HD75154	Hitachi	30
					MC1489	**Motorola**	**(2753)**
					DS1489	National	
					MC1489	Signetics	
					SG1489	Silicon G	
					SN55189	† TI	
					SN75189	TI	
	0.75 to 2.25		5	RS232C, Programmable Threshold, Wider Hysteresis than 1489	**XR1489A**	**Exar**	**(3188)**
					μA1489A	Fairchild	
					HD75189	Hitachi	
					MC1489A	**Motorola**	**(2753)** 40
					DS1489A	National	
					MC1489A	Signetics	
					SG1489A	Silicon G	
					SN55189A	† TI	
	0.97 to 2.65		5	Hysteresis, 120 Ohm System	DS7836	† National	
	1.05 to 2.5		5	Hysteresis, 120 Ohm System	DS8836	National	
	1.2 to 1.8		5	120 Ohm System, No Hysteresis, NOR Input	DS7640	† National	
	1.3 to 1.7		5	120 Ohm System, No Hysteresis, NOR Input	DS8640	National	
	1.7		5	No Hysteresis, NOR Input	96106	Fairchild	
	1.75 to 2.25 V		5	RS232C, Programmable Threshold, Hysteresis	SN75189A	TI	50
	5 to 7.5		15	Hysteresis, Interface to CMOS	367A	Teledyne S	
					367M	† Teledyne S	
				Hysteresis, Open Collector, Interface to CMOS	368A	Teledyne S	
	5.5 to 8		12	Hysteresis, Open Collector, Inferface to CMOS Hystersis, Interface to CMOS	368C	Teledyne S	
					367B	Teledyne S	
					367C	† Teledyne S	
	±3/0.8 to 3		5 or 12	RS232C, Hysteresis, Fail Safe Option	55154	† Fairchild	
					75154	Fairchild	
					DS75154	National	
					SG55154	† Silicon G	60
					SG75154	Silicon G	
					SN54154	**† TI**	**(885)**
					SN75154	TI	
6	0.97 to 2.65		5	Hysteresis, 120 Ohm System	DS7837	† National	
	1.05 to 2.50		5	Hysteresis, 120 Ohm System	MC3437	Motorola	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

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INTERFACE-Line Circuits (Cont'd)

No. Per Device	Receiver Input Threshold	Common Mode Voltage, V	Supply Voltage, V	Comments	Device	Source	Line
Line Receivers—Single Ended							**(Cont'd)**
6	1.05 to 2.50		5	Hysteresis, 120 Ohm System			(Cont'd)
					DS8837	National	
					N8T37	Signetics	
	−1 to 4.5/-1.5 to 13						
			5	NTDS	MOB-272	† Interdesign	
7	0.7 to 1.7		5	IBM360/370	**MC75125**	**Motorola**	**(2753)**
					MC75127	**Motorola**	**(2753)**
					DS75125	National	
					DS75127	National	
					SN75125	TI	
					SN75127	TI	
8	0.7 to 1.7		5	IBM360/370	**MC75128**	**Motorola**	**(2753)** 10
					MC75129	**Motorola**	**(2753)**
					DS75128	National	
					DS75129	National	
					SN75128	TI	
					SN75129	TI	
Line Receivers—Differential							
See also Receivers-listed under Digital-ECL and Digital-HNIL/HTL Miscellaneous sections							
2	±0.010	±3	±5	10 mV, MOS Sense, Active Pull-up	DS75207	National	
					DS75208	National	
					SN75207	TI	
				10 mV, MOS Sense, Open Collector	SN75208	TI	20
				10 mV, MOS Sense, Three-State	DS3604	National	
				75207 with Diode Protected Input Stage	SN75207B	TI	
				75208 with Diode Protected Input Stage	SN75208B	TI	
	±0.025	±3	±5	25 mV, Active Pull-up	55107A	† Fairchild	
					75107A	Fairchild	
					HD75107A	Hitachi	
					MC55107	† Motorola	
					MC75107	Motorola	
				25 mV, Active Pull-Up	DS55107	† National	
					DS75107	National	30
				25 mV, Active Pull-up	SN55107A	† TI	
					SN75107A	TI	
				25 mV, Open Collector	HD75108A	Hitachi	
					MC55108	† Motorola	
					MC75108	Motorola	
					DS55108	† National	
					DS75108	National	
					SN55108A	† TI	
					SN75108A	TI	
				25 mV, Three-State 55107	DS1603	† National	40
					DS3603	National	
				55107A with Diode Protected Input Stage	75107B	Fairchild	
					DS55107	† National	
					DS75107	National	
					SN55107B	† TI	
					SN75107B	TI	
				55108A with Diode Protected Input Stage	75108B	Fairchild	
					DS55108	† National	
					DS75108	National	
					SN55108B	† TI	50
					SN75108B	TI	
	±0.2/0.3	±10/15	5	Twisted Pair, ±15 V CMV. Response Control	DS78LS120	† National	
					DS88LS120	National	
		±15	5	CMOS Compatible, Response Control	DS78C120	† National	
					DS88C120	National	
	±0.2/0.5	±7/15	5	RS232, RS422/3	9637AC	Fairchild	
					9637AM	† Fairchild	
					SN55157	† TI	
					SN75157	TI	
					μA9637AC	TI	60

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† Military Temperature Range (−55° to 125°C)

* Typical Value

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INTERFACE–Line Circuits (Cont'd)

Line Receivers—Differential (Cont'd)

No. Per Device	Receiver Input Threshold	Common Mode Voltage, V	Supply Voltage, V	Comments	Device	Source	Line
2						(Cont'd)	
	±0.3/0.3	±0/15	5	± 15 V CMV, Response Control	DS78L20	† National	
	±0.5/1	±0/15	5	± 15 V CMV, Response Control	9615C	Fairchild	
					9615M	† Fairchild	
					DS55115	† National	
					DS75115	National	
					9615C	TI	
					SN55115	† TI	
					SN75115	TI	
		±3/15	5	Twisted Pair, ±3/15 V CMV, Response Control	DS7820A	† National	
					DS8820A	National	10
					DS8820	TI	
					SN55152	† TI	
					SN55182	† TI	
					SN75182	TI	
		± 10/15	5	Twisted Pair, ± 15 V CMV, Response Control	DS7820	† National	
					DS78C20	† National	
					DS8820	National	
					DS88C20	National	
	±0.5/3	±25	± 12	Adjusts RS232C/MIL-188, ±25 V CMV, Hysteresis	SN75152	TI	
4	±0.025	±3	±5	Four 75107, Active Pull-up	MC3450	Motorola	20
					DS1650	† National	
					DS3650	National	
				Four 75108, Open Collector	MC3452	Motorola	
					DS1652	† National	
					DS3652	National	
	±0.2	±3	±5	Three-State, RS422/423	**MC3486**	**Motorola**	**(2753)**
					DS3486	National	
					MC3486	TI	
		±7	±5	Three-State, RS-422/423	AM26LS32C	AMD	
					AM26LS32M	† AMD	30
					DS26LS32C	National	
					DS26LS32M	† National	
					AM26LS32C	TI	
					AM26LS32M	† TI	
		± 12	±5	Three-State, RS-422	SN75173	TI	
					SN75175	TI	
		± 15	±5	50 mV Hysteresis	DS1689	† National	
					DS1690	† National	
					DS3689	National	
					DS3690	National	40
	±0.5	± 15	±5	Three-State	AM26LS33C	AMD	
					AM26LS33M	† AMD	
					DS26LS33C	National	
					DS26LS33M	† National	
					AM26LS33C	TI	
					AM26LS33M	† TI	
	±0.8	−12,±7.5	±5,−5	NTDS	MOF1623B	† Interdesign	

† Military Temperature Range (−55° to 125°C)

* Typical Value

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INTERFACE–Line Circuits (Cont'd)

No. Per Device	Receiver Input Threshold, V	Output	Supply Voltage, V	Comments	Device	Source		Line
Line Transceivers—Single Ended								
Bidirectional Bus Transceiver, Three-State, CMOS								
	—	TTL/CMOS	5	General Purpose Interface Bus	**DS3666**	**National**	**(2768)**	
					DS75160A	**National**	**(2768)**	
					DS75161A	**National**	**(2768)**	
					DS75162A	**National**	**(2768)**	
	0.8 to 2.0	TTL	5	Bidirectional Bus Transceiver/Register, Open Collector	**SN74LS647**	**TI**	**(986)**	
					SN74LS649	**TI**	**(986)**	
				Bidirectional Bus Transceiver, Three-State	G74SC245	GTE Micro		
					G74SC545	GTE Micro		
				Bidirectional Bus Transceiver, Three-State, CMOS	**MD54SC245**	**†Mitel**	**(706)**	
					MD54SC545	**†Mitel**	**(706)**	10
					MD74SC245	**Mitel**	**(702,706)**	
					MD74SC545	**Mitel**	**(706)**	
				General Purpose Interface Bus	**MC3447**	**Motorola**	**(2753,2755)**	
					SN75160	TI		
					SN75160A	TI		
					SN75161	TI		
					SN75161A	TI		
					SN75162	TI		
					SN75162A	TI		
					SN75163	TI		20
4	0.05 to 2.50	TTL	5	Open Collector, 1 V Hysteresis	AM8838	AMD		
					MC3438	Motorola		
					DS8838	National		
					N8T38	Signetics		
	0.21 to 1.84	TTL	5	Open Collector (Inverting), Common Enable	96103M	† Fairchild		
	0.4 to 2.05	TTL	5	Open Collector, Hysteresis	AM26S12AC	AMD		
					AM26S12AM	† AMD		
	0.5 to 2.0	TTL	5	Bus Transceiver, Tridirectional, Open Collector	**SN54LS440**	**†TI**	**(947)**	
					SN54LS441	**†TI**	**(947)**	
					SN54LS448	**†TI**	**(951)**	30
				Bus Transceiver, Tridirectional, Three-State	**SN54LS442**	**†TI**	**(947)**	
					SN54LS443	**†TI**	**(947)**	
					SN54LS444	**†TI**	**(947)**	
	0.6 to 2.0	TTL	5	Bus Transceiver, Tridirectional, Open Collector	**SN74LS440**	**TI**	**(947)**	
					SN74LS441	**TI**	**(947)**	
					SN74LS448	**TI**	**(951)**	
				Bus Transceiver, Tridirectional, Three-State	**SN74LS442**	**TI**	**(947)**	
					SN74LS443	**TI**	**(947)**	
					SN74LS444	**TI**	**(947)**	
				General Purpose Interface Bus, Open Collector, for MOS Input	**MC3446A**	**Motorola**	**(2753)**	40
					MC3446	TI		
	0.7 to 2.0	TTL	5	Three-State, Bus Transceiver	**AM2915AM**	**†AMD**	**(1211)**	
				Three-State, Bus Transceiver, Parity Generator/Checker	**AM2916AM**	**†AMD**	**(1211)**	
					AM2917AM	**†AMD**	**(1212)**	
				Three-State, Hysteresis	AM25LS242M	† AMD		
					AM25LS243M	† AMD		
					SN54LS242	† AMD		
					SN54LS243	† AMD		
					SN54S242	† AMD		
					SN54S243	† AMD		50
					54LS242	† Fairchild		
					54LS243	† Fairchild		
					SN54LS242	† Motorola		
					SN54LS243	† Motorola		
					SN54ALS242	**†TI**	**(911)**	
					SN54ALS243	**†TI**	**(912)**	
					SN54LS242	**†TI**	**(911)**	
					SN54LS243	**†TI**	**(912)**	
	0.8 to 1.8	TTL/MOS	5	Bus Transceiver, Individual Direction Controls	**SN54LS446**	**†TI**	**(950)**	
					SN54LS449	**†TI**	**(951)**	60
				General Purpose Interface Bus, Bidirectional Bus Transceiver, Three-State	AM3448A	AMD		
					μA3448A	Fairchild		
					MC3448A	**Motorola**	**(2753)**	
	0.8 to 2.0	TTL	5	Bus Transceiver, Individual Direction Controls	**SN74LS446**	**TI**	**(950)**	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Line Circuits (Cont'd)

Line Transceivers—Single Ended (Cont'd)

No. Per Device	Receiver Input Threshold, V	Output	Supply Voltage, V	Comments	Device	Source		Line
							(Cont'd)	
					SN74LS449	**TI**	**(951)**	
4	0.8 to 2.0	TTL	5	Bus Transceiver, Individual Direction Controls				
				General Purpose Interface Bus, Open Collector, 100 mA Output	DS8641	Motorola		
					MC3440A	**Motorola**	**(2753)**	
					MC3441A	**Motorola**	**(2753)**	
					MC3443A	**Motorola**	**(2753)**	
					DS3662	National		
					DS7641	† National		
					DS8641	National		
					MC3443	TI		
				Three-State, Bus Transceiver	**AM2915AC**	**AMD**	**(1211)**	10
				Three-State, Bus Transceiver, Parity Generator/Checker	**AM2916AC**	**AMD**	**(1211)**	
					AM2917AC	**AMD**	**(1212)**	
				Three-State, Dual Rank Latches	**SN74S226**	**TI**	**(908)**	
				Three-State, Hysteresis	AM25LS242C	AMD		
					AM25LS243C	AMD		
					SN74LS242	† AMD		
					SN74LS243	AMD		
					SN74S242	AMD		
					SN74S243	AMD		
					74LS242	Fairchild		20
					74LS243	Fairchild		
					SN74LS242	Motorola		
					SN74LS243	Motorola		
					74LS242	Signetics		
					74LS243	Signetics		
					SN74ALS242	**TI**	**(911)**	
					SN74ALS243	**TI**	**(912)**	
					SN74LS242	**TI**	**(911)**	
					SN74LS243	**TI**	**(912)**	
				Three-State (Inverting)	N8T26	AMD		30
					S8T26	† AMD		
					μA8T26A	Fairchild		
					μA8T26AM	† Fairchild		
					HD268T26	Hitachi		
					MC6880	Motorola		
					MC8T26A	Motorola		
					DS8T26A	National		
					DS8T26AM	† National		
					N8T126	Signetics		
					N8T127	Signetics		40
					N8T26A	Signetics		
					S8T126	† Signetics		
					S8T127	† Signetics		
					SN75136	TI		
				Three-State (Non-Inverting)	N8T28A	AMD		
					S8T28A	† AMD		
					μA8T28	Fairchild		
					μA8T28M	† Fairchild		
					MC6889	Motorola		
					MC8T28	Motorola		50
					DS8T28	National		
					DS8T28M	† National		
					N8T128	Signetics		
					N8T129	Signetics		
					N8T28	Signetics		
					S8T128	† Signetics		
					S8T129	† Signetics		
	0.97 to 2.65	TTL	5	Open Collector, 1 V Hysteresis	AM7838	† AMD		
					DS7838	† National		
	1.05 to 2.50	TTL	5	Inverting 7833/8833	DS7835	† National		60
					DS8835	National		
				Inverting 7839/8839	DS7834	† National		
					DS8834	National		
					N8T34	Signetics		
				Three-State, NOR Gate, Transmit Disable, Hysteresis	DS7839	† National		
					DS8839	National		

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

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INTERFACE–Line Circuits (Cont'd)

Line Transceivers—Single Ended (Cont'd)

No. Per Device	Receiver Input Threshold, V	Output	Supply Voltage, V	Comments	Device	Source		Line
							(Cont'd)	
4	1.05 to 2.50	TTL	5	Three-State, T/R Disables, Hysteresis	DS7833	† National		
					DS8833	National		
	1.5 to 2.4	TTL	5	Open Collector, 100 mA Output, Parity Generator/Checker	**AM2907M**	**† AMD**	**(1206)**	
				Q-bus Compatible 2907	**AM2908M**	**† AMD**	**(1206)**	
				2-Input, Open Collector 100 mA Drivers	**AM2905M**	**† AMD**	**(1205)**	
				2-Input, Open Collector 100 mA Drivers, Parity Generator/Checker	**AM2906M**	**† AMD**	**(1205)**	
	1.5 to 3.2	TTL	5	Open Collector, 100 mA Output	SG55138	† Silicon G		
					SN55138	† TI		
	1.6 to 1.8	TTL	5	Open Collector, Hysteresis	AM26S12C	AMD		
					AM26S12M	† AMD		10
	1.6 to 2.3	TTL	5	Open Collector, 100 MA Output, Parity Generator/Checker	**AM2907C**	**AMD**	**(1206)**	
				Q-bus Compatible 2907	**AM2908C**	**AMD**	**(1206)**	
				2-Input, Open Collector 100 mA Drivers	**AM2905C**	**AMD**	**(1205)**	
				2-Input, Open Collector 100 mA Drivers, Parity	**AM2906C**	**AMD**	**(1205)**	
	1.6 to 2.4	TTL	5	Open Collector, 100 mA Output	AM26S10M	† AMD		
					AM26S11M	† AMD		
					9640M	† Fairchild		
					DS26S10M	† National		
					DS26S11M	† National		
					AM26S10M	† TI		20
					AM26S11M	† TI		
	1.75 to 2.25	TTL	5	Open Collector, 100 mA Output	AM26S10C	AMD		
					AM26S11C	AMD		
					9640C	Fairchild		
					MC26S10	Motorola		
					MC26S11	Motorola		
					DS26S10C	National		
					DS26S11C	National		
					AM26S10C	TI		
					AM26S11C	TI		30
					AM2S10C	TI		
	1.8 to 2.9	TTL	5	Open Collector, 100 mA Output	SG75138	Silicon G		
					SN75138	TI		
8	TTL	TTL	5	Bidirectional Bus Transceiver, Three-State	AM7304B	† AMD		
					AM8304	AMD		
					DP8304	National		
	0.5 to 2.0	TTL	5	Bidirectional Bus Transceiver, Open Collector	**54LS641**	**† Signetics**	**(2772)**	
					54LS642	**† Signetics**	**(2772)**	
					74LS641	Signetics		
					74LS641-1	Signetics		40
					74LS642	**Signetics**	**(2772)**	
					74LS642-1	**Signetics**	**(2772)**	
					SN54LS621	**† TI**	**(976)**	
					SN54LS622	**† TI**	**(976)**	
					SN54LS641	**† TI**	**(984)**	
					SN54LS642	**† TI**	**(984)**	
					SN54LS644	**† TI**	**(984)**	
				Bidirectional Bus Transceiver, Three-State	AM7303	† AMD		
					AM7307	† AMD		
					AM7308	† AMD		50
					AM8303	AMD		
					AM8307	AMD		
					AM8308	AMD		
					SN54LS645	**† MMI**	**(715)**	
					SN54LS645-1	**† MMI**	**(715)**	
					DP7303	† National		
					DP7304B	† National		
					DP7307	† National		
					DP7308	† National		
					DP8303	National		60
					DP8304B	National		
					DP8307	National		
					DP8308	National		
					SN54ALS1645	**† TI**	**(1023)**	
					SN54ALS245	**† TI**	**(913)**	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

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INTERFACE–Line Circuits (Cont'd)

Line Transceivers—Single Ended (Cont'd)

No. Per Device	Receiver Input Threshold, V	Output	Supply Voltage, V	Comments	Device	Source		Line
							(Cont'd)	
8	0.5 to 2.0	TTL	5	Bidirectional Bus Transceiver, Three-State	**SN54ALS645**	† **TI**	**(984)**	
					SN54LS620	† **TI**	**(976)**	
					SN54LS623	† **TI**	**(976)**	
					SN54LS640	† **TI**	**(984)**	
					SN54LS643	† **TI**	**(984)**	
					SN54LS645	† **TI**	**(984)**	
					SN54SL245	† TI		
	0.6 to 2.0	TTL	5	Bidirectional Bus Transceiver, Open Collector	**SN74LS621**	**TI**	**(976)**	
					SN74LS622	**TI**	**(976)**	
					SN74LS641	**TI**	**(984)**	10
					SN74LS641-1	**TI**	**(984)**	
					SN74LS642	**TI**	**(984)**	
					SN74LS642-1	**TI**	**(984)**	
					SN74LS644	**TI**	**(984)**	
					SN74LS644-1	**TI**	**(984)**	
				Bidirectional Bus Transceiver, Three-State	**SN74LS645**	**MMI**	**(715)**	
					SN74LS645-1	**MMI**	**(715)**	
					74LS640	Signetics		
					74LS640-1	Signetics		
					74LS645	Signetics		20
					SN74LS245	**TI**	**(913)**	
					SN74LS620	**TI**	**(976)**	
					SN74LS623	**TI**	**(976)**	
					SN74LS640	**TI**	**(984)**	
					SN74LS640-1	**TI**	**(984)**	
					SN74LS643	**TI**	**(984)**	
					SN74LS643-1	**TI**	**(984)**	
					SN74LS645	**TI**	**(984)**	
					SN74LS645-1	**TI**	**(984)**	
	0.7 to 2.0	TTL	5	Bidirectional Bus Transceiver, Open Collector	SN54LS641	† Motorola		30
					SN54LS642	† Motorola		
				Bidirectional Bus Transceiver/Register, Open Collector	**SN54LS647**	† **TI**	**(986)**	
					SN54LS649	† **TI**	**(986)**	
				Bidirectional Bus Transceiver, Three-State	54LS245	† Fairchild		
					SN54LS245	† Motorola		
					SN54LS640	† Motorola		
					SN54LS645	† Motorola		
					SN54LS646	† **TI**	**(986)**	
					SN54LS648	† **TI**	**(986)**	
	0.8 to 2.0	TTL	5	Bidirectional Bus Transceiver, Open Collector	SN74LS641	Motorola		40
					SN74LS642	Motorola		
				Bidirectional Bus Transceiver, Three-State	74LS245	Fairchild		
					M74LS245	Mitsubishi		
					SN74LS245	Motorola		
					SN74LS640	Motorola		
					SN74LS645	Motorola		
					DS3667	† National		
					74LS245	**Signetics**	**(779)**	
					N8T125	Signetics		
					S8T125	† Signetics		50
					SN74ALS1645	**TI**	**(1023)**	
					SN74ALS245	**TI**	**(913)**	
					SN74ALS645	**TI**	**(984)**	
					SN74LS646	**TI**	**(986)**	
					SN74LS648	**TI**	**(986)**	

† Military Temperature Range (−55° to 125°C)

* Typical Value

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INTERFACE–Line Circuits (Cont'd)

No. Per Device	Receiver Input Threshold, V	Output	Supply Voltage, V	Comments	Device	Source	Line
Line Transceivers—Differential							
1		TTL	5	Designed to meet proposed EIA Standard RS485	**DS3695**	**National**	**(2770)**
					DS3696	**National**	**(2770)**
					DS3697	**National**	**(2770)**
					DS3698	**National**	**(2770)**
	±0.5/±1 V	TTL	5	Independent Three-State 55113 Driver and 55115 Receiver	SN55116	† TI	
					SN75116	TI	
				Same as 55116 with Three-State Receiver	SN55118	† TI	
					SN75118	TI	
				Same as 55117 with Three-State Receiver	SN55119	† TI	
					SN75119	TI	10
				Three-State 8 Pin, 40 MA	SN55117	† TI	
					SN75117	TI	

† Military Temperature Range (−55° to 125°C)

* Typical Value

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INTERFACE–Memory and Peripheral Drivers

Memory & Peripheral Drivers

Function	Device	Source	Line
Addressable Peripheral Driver (latched, 8-output driver)			
	NE590	Signetics	
	NE591	Signetics	
	SE590	† Signetics	
BiMOS Latched Driver			
	UCS-4401H	† Sprague	
	UCS-4801H	Sprague	
Bridged Motor Driver			
	MD346	Analog Sys	
Clock Generator/Oscillator, to 10 MHz, 8 and 1 Divider, for Microprocessors			
	ICM7209	† Intersil	
Data Acquisition Controller (intelligent) for A/D Converter			
	CY600	Cybernetic	
Disc Memory Read/Write			
	μPC751	NEC-Electron	
	μPC752	NEC-Electron	10
Driver, Half Bridge, 2 A			
	SG1635	† Silicon G	
	SG3635	Silicon G	
Driver, Open Collector/Emitter, for 150 mA (load connected to negative supply)			
	PBD3520	RIFA	
Driver, Serial Input/16-Bit Parallel Output, High-Voltage, High-Current Outputs			
	TSC9403	**Teledyne S (2854)**	
	TSC9404	**Teledyne S (2854)**	
Driver, to 80 V, 0.2 A			
	DI445	Dionics	
Driver, Single, 125 mA, for Relays, Motors, Lamps			
	PBD3510	RIFA	
	PBD3511	RIFA	
Driver, Dual, to 80 V, 0.2 A			
	DI446	Dionics	
Driver, Dual, 2-Input, Sink or Source 500 mA			
	SG1627	† Silicon G	20
	SG3627	Silicon G	
Driver, 5 Channel, CMOS/PMOS Input (lamp, relay driver, load to negative supply)			
	UDN-2956A	**Sprague (2843)**	
Driver, 5 Channel, CMOS/TTL Input (lamp, relay driver, load to negative supply)			
	UDN-2957A	**Sprague (2843)**	
Driver, 5 Channel Darlington, to 400 mA			
	XR2200	Exar	
	XR2200M	† Exar	
	LB1287	Sanyo	
	LB1288	Sanyo	
Driver, 7 Channel, CMOS/PMOS Input (hammer, lamp, relay driver)	MD402	Analog Sys	
	XR2204	**Exar (3200)**	
	XR2204M	**† Exar (3200)**	30
	9668	Fairchild	
	9668M	† Fairchild	
	MC1416	**Motorola (2753)**	
	PBD352304	RIFA	
	ULN2004	Signetics	
	ULN-2004A	**Sprague (2843)**	
	ULN-2014A	**Sprague (2843)**	
	ULN-2024A	**Sprague (2843)**	
	ULS-2004H	† Sprague	
	ULS-2014H	† Sprague	40
	ULS-2024H	† Sprague	
	SN75469	TI	
	ULN2004A	TI	
Driver, 7 Channel, CMOS/TTL Input (hammer, lamp, relay driver)	**XR2003M**	**† Exar (3199)**	
	XR2203	**Exar (3200)**	
	9667	Fairchild	

(Continued)

Function	Device	Source	Line
Driver, 7 Channel, CMOS/TTL Input (hammer, lamp, relay driver)			(Cont'd)
	9667M	† Fairchild	
	MC1413	**Motorola (2753)**	
	PBD352303	RIFA	
	L203	SGS	50
	ULN2003	Signetics	
	SG2003	Silicon G	
	SG3853	Silicon G	
	ULN-2003A	**Sprague (2843)**	
	ULN-2005A	**Sprague (2843)**	
	ULN-2013A	**Sprague (2843)**	
	ULN-2015A	**Sprague (2843)**	
	ULN-2023A	**Sprague (2843)**	
	ULN-2025A	**Sprague (2843)**	
	ULS-2003H	† Sprague	60
	ULS-2005H	† Sprague	
	ULS-2013H	† Sprague	
	ULS-2015H	† Sprague	
	ULS-2023H	† Sprague	
	ULS-2025H	† Sprague	
	SN75468	TI	
	ULN2003A	TI	
Driver, 7 Channel, MOS/TTL Input (hammer, lamp, relay driver)	**XR2201**	**Exar (3200)**	
	XR2201M	**† Exar (3200)**	
	9665	Fairchild	70
	MC1411	**Motorola (2753)**	
	PBD352301	RIFA	
	L201	SGS	
	ULN2001	Signetics	
	SG2001	Silicon G	
	SG3851	Silicon G	
	ULN-2001A	**Sprague (2843)**	
	ULN-2011A	**Sprague (2843)**	
	ULN-2021A	**Sprague (2843)**	
	ULS-2001H	† Sprague	80
	ULS-2011H	† Sprague	
	ULS-2012H	† Sprague	
	SN75466	TI	
	ULN2001A	TI	
Driver, 7 Channel, PMOS Input (hammer, lamp, relay driver)	**XR2202**	**Exar (3200)**	
	XR2202M	**† Exar (3200)**	
	9666	Fairchild	
	9666M	† Fairchild	
	MC1412	**Motorola (2753)**	
	PBD352302	RIFA	90
	L202	SGS	
	SG2002	Silicon G	
	SG3852	Silicon G	
	ULN-2002A	**Sprague (2843)**	
	ULN-2012A	**Sprague (2843)**	
	ULN-2022A	**Sprague (2843)**	
	ULS-2002H	† Sprague	
	ULS-2022H	† Sprague	
	SN75467	TI	
	ULN2002A	TI	100
Driver, 8 Channel, CMOS/PMOS Input (hammer, lamp, relay driver)	ULN2804	Motorola	
	ULN-2804A	**Sprague (2843)**	
	ULN-2814A	**Sprague (2843)**	
	ULN-2824A	**Sprague (2843)**	
	ULS-2804H	† Sprague	
	ULS-2814H	† Sprague	
	ULS-2824H	† Sprague	
Driver, 8 Channel, CMOS/PMOS Input (lamp, relay driver)	**UDN-2982A**	**Sprague (2843)**	
	UDN-2984A	**Sprague (2843)**	
	UDS-2982H	† Sprague	110
	UDS-2984H	† Sprague	

Function	Device	Source	Line
Driver, 8 Channel, CMOS/TTL Input (hammer, lamp, relay driver)	ULN2803	Motorola	
	NE5090	Signetics	
	SE5090	Signetics	
	ULN-2803A	**Sprague (2843)**	
	ULN-2805A	**Sprague (2843)**	
	ULN-2813A	**Sprague (2843)**	
	ULN-2815A	**Sprague (2843)**	
	ULN-2823A	**Sprague (2843)**	
	ULN-2825A	**Sprague (2843)**	120
	ULS-2803H	† Sprague	
	ULS-2805H	† Sprague	
	ULS-2813H	† Sprague	
	ULS-2815H	† Sprague	
	ULS-2823H	† Sprague	
	ULS-2825H	† Sprague	
Driver, 8 Channel, CMOS/TTL Input (lamps, relay driver)	**UDN-2981A**	**Sprague (2843)**	
	UDN-2983A	**Sprague (2843)**	
	UDS-2981H	† Sprague	
	UDS-2983H	† Sprague	130
Driver, 8 Channel, MOS/TTL Input (hammer, lamp, relay driver)	ULN2801	Motorola	
	ULN-2801A	**Sprague (2843)**	
	ULN-2811A	**Sprague (2843)**	
	ULN-2821A	**Sprague (2843)**	
	ULS-2801H	† Sprague	
	ULS-2811H	† Sprague	
	ULS-2821H	† Sprague	
Driver, 8 Channel, PMOS Input (hammer, lamp, relay driver)	ULN2802	Motorola	
	ULN-2802A	**Sprague (2843)**	
	ULN-2812A	**Sprague (2843)**	140
	ULN-2822A	**Sprague (2843)**	
	ULS-2802H	† Sprague	
	ULS-2812H	† Sprague	
	ULS-2822H	† Sprague	
Driver, 8-Channel Current-Sink Driver	**UDN-2595A**	**Sprague (2843)**	
Driver, 10-Bit, High-Voltage, High-Current	S4534	AMI	
Driver, 32-Bit for Displays, Relays, Solenoids, Print Heads and Motors	S4521	AMI	
	S4535	AMI	
Dynamic RAM Controller	**TMS4500A**	**TI (3960)**	
	WD8207	**Western (3996)**	150
Dynamic RAM Controller/Driver	**DP8408**	**MMI (727)**	
	SN74S408	**MMI (727)**	
	SN74S408-3	**MMI (727,727)**	
Gated Decoder, for SSI104/5	SSI106	Silicon Sys	
Hammer Driver (to 6 A-pulsed output)	**DH0028C**	**National (3344)**	
High Current Switch Driver (to drive high power, high speed NPN switching transistors)	SG1629	† Silicon G	
	SG3629	Silicon G	
High-Voltage Source Drivers	**UDN-6510A**	**Sprague (2843)**	
	UDN-6514A	**Sprague (2843)**	
Memory Driver Dual, 400 mA Sink/Source, Decode (for magnetic memories)	DS3629	National	160
Memory Driver, Dual 600 mA Sink/Source	MC55325	† Motorola	
	MC75325	Motorola	
	DS55325	† National	
	DS75325	National	
	SG55325	† Silicon G	

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† Military Temperature Range (−55° to 125°C)

* Typical Value

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INTERFACE–Memory and Peripheral Drivers (Cont'd)

Memory & Peripheral Drivers (Cont'd)

Function	Device	Source	Line
Memory Driver, Dual 600 mA Sink/Source (Cont'd)			
	SG75325	Silicon G	
	SN55325	† TI	
	SN75325	TI	
Memory Driver, Quad, 600 mA Sink			
	SG55326	† Silicon G	
	SG55327	† Silicon G	
	SG75326	Silicon G	
	SG75327	Silicon G	
	SN55326	† TI	
	SN55327	† TI	
	SN75326	TI	10
	SN75327	TI	
Memory Switch, Quad, 600 mA Sink/Source			
	SN75328	TI	
Modified Frequency Modulation Decoder Data Separator			
	DP8460	**National**	**(2766)**
MOS Clock Driver			
	MH0007	† National	
	MH0007C	National	
	MH0012	† National	
	MH0012C	National	
MOS Dynamic Memory, Address Refresh Logic Circuitry			
	MC8505	Motorola	
MOS Dynamic Memory Interface, Microprocessor to 16 K RAM	MC3480	Motorola	
MOS Dynamic Memory, 4 K Address Multiplexer and Refresh Counter			
	96LS32	† Fairchild	20
	96LS32C	Fairchild	
	MC3232A	Motorola	
MOS Dynamic Memory, 16 K Address Multiplexer and Refresh Counter			
	96LS42C	Fairchild	
	96LS42M	† Fairchild	
	MC3242A	Motorola	
Motor Controller (intelligent) for 4-Phase Stepper Motors			
	CY500	Cybernetic	
	CY512	Cybernetic	
Multi-Mode Dynamic RAM Controller/Driver			
	DP8408	National	
	DP8409	**National**	**(2765)**
Power Peripheral Driver, CMOS/TTL Input (to 150 V, versions: 0.01 to 16 A)			
	VF-01	Supertex	30
	VF-02	Supertex	
	VF-03	Supertex	
	VF-12	Supertex	
	VF-13	Supertex	
Power Peripheral Drivers			
	VN10KE	Siliconix	
	VN10KM	Siliconix	
	VN46AF	Siliconix	
	VN64GA	Siliconix	
	VN66AF	Siliconix	
	VN88AF	Siliconix	40
Printer Controller, for 5x7 Dot Matrix Printers			
	CY480	Cybernetic	
Printer Driver, 5 Channel			
	HD2919	Hitachi	
Printer Solenoid Driver			
	DS3654	National	
Printing Calculator Circuits			
	DS8654	National	
	DS8656	National	
	DS8692	National	
	DS8693	National	
	DS8694	National	
Relay Driver, to 65 V, Sinks 300 mA, OR Input for 48 V Telephone Relays			
	DS1686	† National	
	DS1687	† National	50
	DS3686	National	
	DS3687	National	
Relay Driver, to 70 V, 500 mA			
	CSR301	Teledyne C	
Relay Driver, 5 Channel, to 65 V, 70 mA			
	ITT7163	ITT	
	ITT7164	ITT	
Solenoid Driver	MC3484V2	TI	
	MC3484V4	TI	
Thermal Print Head Driver			
	SN75270	TI	
	SN75490	TI	
	SN75590	TI	60
TTL to MOS Shifter			
Winchester Disc Memory Fault Detector			
	SSI103	Silicon Sys	
Winchester Disc Memory Head Read/Write Circuit, for thin film heads	SSI114	Silicon Sys	
Winchester Disc Memory Head Selector			
	SSI102	Silicon Sys	
Winchester Disc Memory Read/Write Circuit			
	SSI104	Silicon Sys	
Winchester Disc Memory Video Amplifier, for Magnetic Servo Head	SSI101A	Silicon Sys	
Winchester Disc Memory Video Amplifier, for Thin Film Magnetic Heads			
	SSI116	Silicon Sys	
Winchester Disk Memory Read/Write Circuit			
	MB4111	Fujitsu	
	MB4112	Fujitsu	
	SSI105	Silicon Sys	70
	SSI108	Silicon Sys	
	SSI114	Silicon Sys	
	SSI115	Silicon Sys	
Winchester Read/Write Circuit, 6-Channel			
	SSI117	Silicon Sys	
Dual AND Driver, HNIL, 250 mA, Open Collector			
	391A/C	Teledyne S	
Dual AND TTL to MOS Driver (NMOS memory interface)			
	9643	Fairchild	
	SN55363	† TI	
	SN75322	TI	
	SN75363	TI	
Dual Buffer, to 40 V, 2 A			
	LPD4106	Lambda	80
Dual CCD Memory Driver, with Enable Inputs			
	SN75430	TI	
Dual CCD Memory Driver, with Enable Inputs and Protect			
	SN75431	TI	
Dual Channel ECL to MOS Driver (MOS memory interface			
	MC75358	Motorola	
	MC75368	Motorola	
Dual Channel TTL to MOS Memory Interface (for TMS4062, AMS6002, etc.)			
	SN75370	TI	
Dual CMOS or TTL Driver/Translator, up to 30 V			
	IH6201C	Intersil	
	IH6201M	† Intersil	
Dual Darlington Switch, to 80 V, 1.5 A			
	ULN-2061M	**Sprague**	**(2843)**
	ULN-2062M	**Sprague**	**(2843)**
Dual ECL to TTL/MOS Driver			
	SN75441	TI	90
Dual Inverter, to 40 V, 2 A			
	LPD4105	Lambda	
Dual Memory Driver, 400 mA Sink (for magnetic memories)			
	MC4043	Motorola	
Dual MOS Clock Driver			
	0026	Fairchild	
	MMH0026	† Motorola	
	MMH0026C	Motorola	
	DS0025	† National	
	DS0025C	National	
	DS0026	† National	
	DS0026C	National	
	DS0056	† National	100
	DS0056C	National	
	MH0009	† National	
	MH0009C	National	
	MH0013	† National	
	MH0013C	National	
	SN55369	† TI	
	SN75369	TI	
Dual MOS Clock Driver, Bootstrapped for Single Supply Systems	DS1642	National	
	DS1671	National	
	DS1672	National	110
Dual NAND Driver, HNIL, 250 mA, Open Collector			
	392A/C	Teledyne S	
Dual NOR Driver, HNIL, 250 mA, Open Collector			
	394A/C	Teledyne S	
Dual OR Driver, HNIL, 250 mA, Open Collector			
	393A/C	Teledyne S	
Dual Peripheral AND Driver			
	55450B	† Fairchild	
	75450B	Fairchild	
	75451A	Fairchild	
	75451B	Fairchild	
	75461	Fairchild	
	75471	Fairchild	
	HD75450A	Hitachi	120
	HD75451A	Hitachi	
	MC75450	Motorola	
	MC75451	Motorola	
	MC75461	Motorola	
	SN75451B	Motorola	
	DS55450	† National	
	DS55451	† National	
	DS55461	† National	
	DS75450	National	
	DS75451	National	130
	DS75461	National	
	PBD3513	RIFA	
	SG55450	† Silicon G	
	SG55450B	† Silicon G	
	SG55451	† Silicon G	
	SG55460	† Silicon G	
	SG55460B	† Silicon G	
	SG55461	† Silicon G	
	SG75450	Silicon G	
	SG75450B	Silicon G	140
	SG75451	Silicon G	
	SG75460	Silicon G	
	SG75460B	Silicon G	
	SG75461	Silicon G	
	SN55450B	† TI	
	SN55451B	† TI	
	SN55460	† TI	
	SN55461	† TI	
	SN55470	† TI	
	SN55471	† TI	150
	SN75401	TI	
	SN75411	TI	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Memory and Peripheral Drivers (Cont'd)

Memory & Peripheral Drivers (Cont'd)

Function	Device	Source		Line
Dual Peripheral AND Driver (Cont'd)				
	SN75450B	TI		
	SN75451B	TI		
	SN75460	TI		
	SN75461	TI		
	SN75466	TI		
	SN75470	TI		
	SN75471	TI		
	SN75476	TI		
Dual Peripheral AND Driver, for CMOS				
	DS1631	† National		
	DS3631	National		10
Dual Peripheral AND Driver, to 70 V 300 mA				
	SN75446	TI		
Dual Peripheral AND Driver, to 70 V 500 mA				
	SN75416	TI		
Dual Peripheral AND Driver, to 80 V 300 mA				
	DS1611	† National		
	DS3611	National		
	UDN-3611M	**Sprague**	**(2843)**	
	UDN-5711M	**Sprague**	**(2843)**	
	UDS-3611H	† Sprague		
	UDS-5711H	† Sprague		
Dual Peripheral NAND Driver				
	55452B	† Fairchild		
	75452A	Fairchild		20
	75452B	Fairchild		
	75462	Fairchild		
	75472	Fairchild		
	HD75452	Hitachi		
	MC75452	Motorola		
	MC75462	Motorola		
	SN75452B	Motorola		
	DS55452	† National		
	DS55462	† National		
	DS75452	National		30
	DS75462	National		
	SG55452	† Silicon G		
	SG55462	† Silicon G		
	SG75452	Silicon G		
	SG75462	Silicon G		
	SN55452B	† TI		
	SN55462	† TI		
	SN55472	† TI		
	SN75402	TI		
	SN75407	TI		40
	SN75412	TI		
	SN75432	TI		
	SN75447	TI		
	SN75452B	TI		
	SN75462	TI		
	SN75472	TI		
Dual Peripheral NAND Driver, for CMOS				
	DS1632	† National		
	DS3632	National		
Dual Peripheral NAND Driver, to 70 V, 300 mA				
	MC1472	Motorola		
	UDN-5722M	Sprague		50
	SN75477	TI		
Dual Peripheral NAND Driver, to 70 V, 500 mA				
	SN75417	TI		
Dual Peripheral NAND Driver, to 80 V, 300 mA				
	DS1612	† National		
	DS3612	National		
	UDN-3612M	**Sprague**	**(2843)**	
	UDN-5712M	**Sprague**	**(2843)**	
	UDS-3612H	† Sprague		
	UDS-5712H	† Sprague		
Dual Peripheral NOR Driver				
	75474B	Fairchild		
	HD75454	Hitachi		60
	MC75454	Motorola		
	MC75464	Motorola		
	SN75454B	Motorola		
	DS55454	† National		
	DS55464	† National		
	DS75454	National		
	DS75464	National		
	SG55454	† Silicon G		
	SG55464	† Silicon G		
	SG75454	Silicon G		70
	SG75464	Silicon G		
	SN55454B	† TI		
	SN55464	† TI		
	SN55474	† TI		
	SN75404	TI		
	SN75407	**TI**	**(2855)**	
	SN75414	TI		
	SN75434	TI		
	SN75449	TI		
	SN75454B	TI		80
	SN75464	TI		
	SN75474	TI		
	SN75479	TI		
Dual Peripheral NOR Driver, for CMOS				
	DS1634	† National		
	DS3634	National		
Dual Peripheral NOR Driver, to 30 V, 300 mA				
	SN75479	TI		
Dual Peripheral NOR Driver, to 30 V, 500 mA				
	SN75419	TI		
Dual Peripheral NOR Driver, to 80 V, 300 mA				
	DS1614	† National		
	DS3614	National		
	UDN-3614M	**Sprague**	**(2843)**	90
	UDN-5714M	**Sprague**	**(2843)**	
	UDS-3614H	† Sprague		
	UDS-5714H	† Sprague		
Dual Peripheral OR Driver				
	75453A/B	Fairchild		
	HD75453	Hitachi		
	MC75453	Motorola		
	MC75463	Motorola		
	SN75453B	Motorola		
	DS55453	† National		
	DS55463	† National		100
	DS75453	National		
	DS75463	National		
	SG55453	Silicon G		
	SG55463	Silicon G		
	SG75453	Silicon G		
	SG75463	Silicon G		
	SN55453B	† TI		
	SN55463	† TI		
	SN55473	† TI		
	SN75403	TI		110
	SN75408	**TI**	**(2855)**	
	SN75413	TI		
	SN75433	TI		
	SN75448	TI		
	SN75453B	TI		
	SN75463	TI		
	SN75473	TI		
	SN75478	TI		
Dual Peripheral OR Driver, ECL Input				
	SN75441	TI		
Dual Peripheral OR Driver, for CMOS				
	DS1633	† National		120
	DS3633	National		
Dual Peripheral OR Driver, to 30 V, 300 mA				
	SN75478	TI		
Dual Peripheral OR Driver, to 30 V, 500 mA				
	SN75418	TI		
Dual Peripheral OR Driver, to 80 V, 300 mA				
	DS1613	† National		
	DS3613	National		
	UDN-3613M	**Sprague**	**(2843)**	
	UDN-5713M	**Sprague**	**(2843)**	
	UDS-3613H	† Sprague		
	UDS-5713H	† Sprague		
Dual Power MOSFET Driver				
	TSC450C	**Teledyne S**	**(2845)**	130
	TSC450M	**† Teledyne S**	**(2845)**	
Dual TTL to MOS Driver (MOS memory interface)				
	DS75361	National		
	DS75362	National		
	MH8805	National		
	SN75350	TI		
	SN75361A	TI		
Dual 2-Input AND Power Driver (40 V, 2 A)				
	LPD4101	Lambda		
Dual 2-Input NAND Power Driver (40 V, 2 A)				
	LPD4102	Lambda		
Dual 2-Input NOR Power Driver (40 V, 2 A)				
	LPD4103	Lambda		
Dual 2-Input OR Power Driver (40 V, 2 A)				
	LPD4104	Lambda		140
Dual 4-Input AND Driver, HNIL 250 mA Open Collector				
	390A/C	Teledyne S		
Dual 4-Input NAND Driver, HNIL, 250 mA Open Collector				
	395A/C	Teledyne S		
Quad Darlington Switch, to 50 V, 1.5 A				
	SN75064	TI		
	SN75066	TI		
	SN75068	TI		
Quad Darlington Switch, to 80 V, 1.5 A				
	SG2064	Silicon G		
	SG2065	Silicon G		
	SG2066	Silicon G		
	SG2067	Silicon G		
	SG2068	Silicon G		150
	SG2069	Silicon G		
	SG2070	Silicon G		
	SG2071	Silicon G		
	SG2072	Silicon G		
	SG2073	Silicon G		
	SG2074	Silicon G		
	SG2075	Silicon G		
	SG2076	Silicon G		
	SG2077	Silicon G		
	ULN-2064B	**Sprague**	**(2843)**	160
	ULN-2065B	**Sprague**	**(2843)**	
	ULN-2066B	**Sprague**	**(2843)**	
	ULN-2067B	**Sprague**	**(2843)**	
	ULN-2068B	**Sprague**	**(2843)**	
	ULN-2069B	**Sprague**	**(2843)**	
	ULN-2070B	**Sprague**	**(2843)**	
	ULN-2071B	**Sprague**	**(2843)**	
	ULN-2074B	**Sprague**	**(2843)**	
	ULN-2075B	**Sprague**	**(2843)**	
	ULN-2076B	**Sprague**	**(2843)**	170
	ULN-2077B	**Sprague**	**(2843)**	
	ULS-2064H	† Sprague		
	ULS-2065H	† Sprague		
	ULS-2066H	† Sprague		
	ULS-2067H	† Sprague		
	ULS-2068H	† Sprague		
	ULS-2069H	† Sprague		
	ULS-2070H	† Sprague		
	ULS-2071H	† Sprague		

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

IC MASTER

INTERFACE–Memory and Peripheral Drivers (Cont'd)

Memory & Peripheral Drivers (Cont'd)

Function	Device	Source		Line
Quad Darlington Switch, to 80 V, 1.5 A (Cont'd)				
	ULS-2074H	† Sprague		
	ULS-2075H	† Sprague		
	ULS-2076H	† Sprague		
	ULS-2077H	Sprague		
	SN75065	TI		
	SN75067	TI		
	SN75069	TI		
	ULN2064	TI		
	ULN2065	TI		
	ULN2066	TI		10
	ULN2067	TI		
	ULN2068	TI		
	ULN2069	TI		
	ULN2074	TI		
	ULN2075	TI		
Quad Darlington Switch, to -50 V, 1.75 A				
	SG2841	Silicon G		
Quad ECL to MOS Clock Driver				
	HD2922	Hitachi		
Quad High Current Peripheral Driver				
	DS3658	**National**	**(2769)**	
	SN75436	**TI**	**(2856)**	
	SN75437A	**TI**	**(2856)**	20
	SN75438	**TI**	**(2856)**	
Quad Latch/Driver				
	MD121	Analog Sys		
	UCN-4401A	**Sprague**	**(2843)**	
	UCS-4401H	† Sprague		
Quad MOS Clock Driver				
	DS3245	National		
Quad, MOS Memory Decoder/Clock Driver				
	DS36143	National		
Quad MOS Memory I/O Register				
	DS16147	† National		
	DS16177	† National		
	DS1647	† National		
	DS1677	† National		30
	DS36147	National		
	DS36177	National		
	DS3647	National		
	DS3677	National		
Quad Multiplexer/Driver, for MOS Systems				
	DS1648	† National		
	DS1678	† National		
	DS3648	National		
	DS3678	National		
Quad NAND TTL to MOS Driver (MOS memory interface-clock driver)	HD2912	Hitachi		
	HD2916	Hitachi		40
	MC75365	Motorola		
	DS75365	National		
	3207A	Signetics		
	3207A-1	Signetics		
	SN55355	† TI		
	SN55365	† TI		
	SN75365	TI		
	SN75375	TI		
Quad Negative Voltage Relay Driver				
	DS3680	National		
	DS3680	TI		50
Quad NMOS Memory Driver				
	MC3459	Motorola		
	MC3460	Motorola		
	DS1644	† National		
	DS1674	† National		
	DS36144	National		

(Continued)

Function	Device	Source		Line
Quad NMOS Memory Driver (Cont'd)				
	DS3644	National		
	DS3674	National		
Quad PIN Diode Driver (also see: linear-other devices)				
	UDS-5790H	**† Sprague**	**(2843)**	
	UDS-5791H	**† Sprague**	**(2843)**	
Quad Port Driver, for 5270 RAM				
	DS1640	† National		60
	DS1670	† National		
Quad Power Driver, with Enable, Sinks 500 mA				
	UDN-2540B	**Sprague**	**(2843)**	
Quad Power Peripheral Driver				
	VN2410	Siliconix		
	VN3500	Siliconix		
	VN3501	Siliconix		
	VN4000	Siliconix		
	VQ1000	**Siliconix**	**(2835)**	
	VQ1001	Siliconix		
	VQ1004	**Siliconix**	**(2837)**	
	VQ1006	**Siliconix**	**(2837)**	70
	VQ2001	Siliconix		
	VQ2004	Siliconix		
	VQ2006	**Siliconix**	**(2839)**	
	VQ3001	**Siliconix**	**(2841)**	
	VQ7254	Siliconix		
	VC01	Supertex		
	VC02	Supertex		
	VC13	Supertex		
	VQ1000	Supertex		
Quad Predriver, Open Collector, 50 mA Sink (for magnetic memories)	MC4042	Motorola		80
Quad TTL to MOS Driver, Three-State				
	SN75367	TI		
Quad TTL to NMOS Memory Driver (for 2105, 2107, etc.)				
	3245	Fairchild		
	9645	Fairchild		
	3245	Intel		
Quad TTL to NMOS Memory Driver (for 7001, etc.)				
	MC3466	Motorola		
Quad 2-Input AND Driver (to 70 V, sinks 300 mA)				
	UDN-5706A	**Sprague**	**(2843)**	
	UDS-5706H	† Sprague		
Quad 2-Input AND Power Driver, Open Collector (to 100 V, sinks 500 mA)				
	UHC/D-400	† Sprague		
	UHC/D-406	† Sprague		
	UHC/D-500	Sprague		90
	UHC/D-506	Sprague		
	UHP-400	**Sprague**	**(2843)**	
	UHP-406	**Sprague**	**(2843)**	
	UHP-500	**Sprague**	**(2843)**	
	UHP-506	**Sprague**	**(2843)**	
Quad 2-Input NAND Driver (for 70 V, sinks 300 mA)				
	UDN-5707A	**Sprague**	**(2843)**	
	UDS-5707H	† Sprague		
Quad 2-Input NAND Driver, to 30 V, sinks 250 mA				
	MC693	Motorola		
Quad 2-Input NAND Power Driver, Open Collector, to 100 V, Sinks 500 mA				
	UHC/D-407	† Sprague		
	UHC/D-408	† Sprague		100
	UHC/D-507	† Sprague		
	UHC/D-508	† Sprague		
	UHP-407	**Sprague**	**(2843)**	
	UHP-408	**Sprague**	**(2843)**	
	UHP-507	**Sprague**	**(2843)**	
	UHP-508	**Sprague**	**(2843)**	

Function	Device	Source		Line
Quad 2-Input NOR Driver, to 70 V, Sinks 300 mA				
	UDN-5733A	**Sprague**	**(2843)**	
	UDN-5733M	**Sprague**	**(2843)**	
	UDS-5733H	† Sprague		
Quad 2-Input NOR Power Driver, Open Collector, to 100 V, Sinks 500 mA	UHC/D-432	† Sprague		110
	UHC/D-433	† Sprague		
	UHC/D-532	† Sprague		
	UHC/D-533	† Sprague		
	UHP-432	**Sprague**	**(2843)**	
	UHP-433	**Sprague**	**(2843)**	
	UHP-532	**Sprague**	**(2843)**	
	UHP-533	**Sprague**	**(2843)**	
Quad 2-Input OR Driver, to 70 V, Sinks 300 mA				
	UDN-5703A	**Sprague**	**(2843)**	
	UDS-5703H	† Sprague		
Quad 2-Input OR Power Driver, Open Collector, to 100 V, Sinks 500 mA	UHC/D-402	† Sprague		120
	UHC/D-403	† Sprague		
	UHC/D-502	Sprague		
	UHC/D-503	Sprague		
	UHP-402	**Sprague**	**(2843)**	
	UHP-403	**Sprague**	**(2843)**	
	UHP-502	**Sprague**	**(2843)**	
	UHP-503	**Sprague**	**(2843)**	
Hex Driver, CMOS/TTL (line, LED, Relay Driver)				
	MD-210	Analog Sys		
Hex Inverter/MOS Driver, Disable Causes Logic 1 State				
	DS16149	† National		
	DS16179	† National		130
	DS36149	National		
	DS36179	National		
	SN54S436	**† TI**	**(947)**	
	SN54S437	**† TI**	**(947)**	
	SN74S436	**TI**	**(947)**	
	SN74S437	**TI**	**(947)**	
Hex Inverter/MOS Driver, Three-State				
	DS1649	† National		
	DS1679	† National		
	DS3649	National		
	DS3679	National		140
Hex Latch/Driver, for MOS Memories				
	DS1645	† National		
	DS1675	† National		
	DS3645	National		
	DS3675	National		
Hex Universal Driver (400 mA)				
	NE582-1	Signetics		
Octal Dynamic Memory Driver, Three-State				
	AM2965C	AMD		
	AM2965M	† AMD		
	AM2966C	AMD		
	AM2966M	† AMD		
Octal Dynamic RAM Driver, Three-State				
	SN54S700	**† MMI**	**(728)**	150
	SN54S730	**† MMI**	**(728)**	
	SN54S731	**† MMI**	**(728)**	
	SN54S734	**† MMI**	**(728)**	
	SN74S700	**MMI**	**(728)**	
	SN74S730	**MMI**	**(728)**	
	SN74S731	**MMI**	**(728)**	
	SN74S734	**MMI**	**(728)**	
Octal High-Voltage Driver for Electrostatic Printers				
	DH0069	**National**	**(3344)**	
Octal Latched Peripheral Driver				
	DP7310	National		
	DP7311	National		160
	DP8310	National		
	DP8311	National		

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Memory and Peripheral Drivers (Cont'd)

Function	Device	Source		Line
Memory & Peripheral Drivers (Cont'd)				
Octal MOS Driver, Three-State				
	DP84240	**National**	**(2767)**	
	DP84244	**National**	**(2767)**	
	DS1628	† National		
	DS3628	National		
Two Phase Oscillator/Clock Driver (for MOS systems)				
	DS7803	† National		
	DS7807	† National		
	DS8803	National		
	DS8807	National		
Eight Latch/Drivers				
	UCN-4801A	**Sprague**	**(2843)**	
	UCS4801H	† Sprague		10
4-Input AND Current Driver (45 V, to 1.5 A peak)				
	DH0006	**† National**	**(3344)**	
	DH0006C	**National**	**(3344)**	
4-Input AND High Voltage-High Current Driver (4.5 V, to 3 A peak)				
	DH0008	**† National**	**(3344)**	
	DH0008C	**National**	**(3344)**	
4-Input NAND High Voltage, High Current Drivers (40 V, 0.15 to 0.25 A)				
	DH0011	**† National**	**(3344)**	
	DH0011C	**National**	**(3344)**	
4-Input NAND High Voltage, High Current Drivers (50, 70 or 100 V, 0.25 to 0.5 A)				
	DH0017C	**National**	**(3344)**	
	DH0018C	**National**	**(3344)**	
6-Bit MOS Refresh Counter/Driver				
	DS1646	† National		
	DS1676	† National		20
8-Bit Serial Input, Latched Sink Driver				
	UCN-4821A	**Sprague**	**(2843)**	
	UCN-4822A	**Sprague**	**(2843)**	
	UCN-4823A	**Sprague**	**(2843)**	
	UCS-4821H	† Sprague		
	UCS-4822H	† Sprague		
	UCS-4823H	† Sprague		

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

IC MASTER

INTERFACE–Sense Amplifiers

Sense Amplifiers

Function	Device	Source	Line
MOS to TTL Level Converter, High Speed, Three-State	**MC4000**	**Motorola**	**(729)**
	MC4300	**† Motorola**	**(729)**
Translators: See also Digital-TTL (Translators)			
Dual Core Memory Sense Amplifier, Complementary Output, Latch Capability	55S20	Fairchild	
	75S20	† Fairchild	
	SG5520	† Silicon G	
	SG5521	† Silicon G	
	SG7520	Silicon G	
	SG7521	Silicon G	
	SN5520	† TI	10
Dual Core Memory Sense Amplifier/Data Register	SG55236	† Silicon G	
	SG75236	Silicon G	
	SN55236	† TI	
	SN55237	† TI	
Dual Core Memory Sense Amplifier, Separate Inverted Outputs	55S234	Fairchild	
	75S234	† Fairchild	
	SN55234	† TI	
	SN75234	TI	
Dual Core Memory Sense Amplifier, Separate Inverted Outputs, Test Points	75239	Fairchild	
Dual Core Memory Sense Amplifier, Separate Open Collector Outputs	SG5534	† Silicon G	20
	SG5535	† Silicon G	
	SG7534	Silicon G	
	SG7535	Silicon G	
	SN55232	† TI	
Dual Core Memory Sense Amplifier, Separate Open Collector Outputs, Test Points	SG5538	† Silicon G	
	SG5539	† Silicon G	
	SG7538	Silicon G	
	SG7539	Silicon G	
Dual Core Memory Sense Amplifier, Separate Outputs	55S24	Fairchild	
	75S24	† Fairchild	30
	HA1902	Hitachi	
	SG5524	† Silicon G	
	SG5525	† Silicon G	
	SG7524	Silicon G	
	SG7525	Silicon G	
	SN5524	† TI	
Dual Core Memory Sense Amplifier, Separate Outputs, Test Points	SG5528	† Silicon G	
	SG5529	† Silicon G	
	SG7528	Silicon G	
	SG7529	Silicon G	40
	SN5528	† TI	
Dual Core Memory Sense Amplifier, Single Open Collector Output	SG5522	† Silicon G	
	SG5523	Silicon G	
	SG7522	Silicon G	
	SG7523	Silicon G	
	SN5522	† TI	
Dual Formatter/Sense Amplifier for Bubble Memories	7242	Intel	
Dual MOS to TTL Level Converter, Latch, Three-State (Sense Amp)	MC4068	Motorola	
	MC4368	† Motorola	
	MC54468	† Motorola	50
	MC74468	Motorola	
	N8T25	Silicon G	
Dual Sense Amplifier (for MOS memory or line receiver)	DS75207	National	
	DS75208	National	
	SN75207	TI	
	SN75208	TI	
	DS3604	National	
	DS1603	† National	
	DS3603	National	
Dual Sense Amplifier (NMOS memories to ECL 10K)	HD103461	Hitachi	60
	MC3461	Motorola	
Quad Sense Amplifer, Three-State	MC3430	Motorola	
	MC3431	Motorola	
	MC3432	Motorola	
	MC3433	Motorola	
	DS1651	† National	
	DS1653	† National	
	DS3651	National	
	DS3653	National	
Hex MOS Sense Amplifier (MOS to TTL Converter) Three-State	DS3605	National	70
	DS3606	National	
	DS3607	National	
	DS3608	National	
Octal Core Memory Driver	SN55329	† TI	
4-Input Sense Amplifier (for plated wire or thick/thin film memories)	MC1444	Motorola	
	MC1544	† Motorola	

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

INTERFACE–Transmitters-Receivers

Serial Transmitters- Receivers

Function	Max Serial Data Rate in kHz	Supply Voltage, V	Device	Source		Line
(ACIA) Asynchronous Communications Interface Adapter (Links 8-Bit bidirectional data bus to serial asynchronous data communications, including to 6860)	50	5	**S6551**	**AMI**	**(1249)**	
			S68051	**AMI**	**(1249)**	
			S6850	AMI		
			F6850	**Fairchild**	**(1280)**	
			MC6850	**Motorola**	**(1351)**	
Advanced Data Link Controller	2 Mb/s	5	MC854	Motorola		
ARINC-429 Receiver/Transmitter	100	5	HS3282	† Harris		
			WD1993-01	**Western**	**(2877)**	
			WD1993-02	**Western**	**(2877)**	
			WD1993-03	**Western**	**(2877)**	10
ASTRO (asynchronous/synchronous receiver/transmitter) to Interface Serial Communications Channel with a Parallel Digital System (i.e. microprocessors)	1000	12,5	WD1931	Western		
		12, ±5	COM1671	SMC		
			UC1671	**Western**	**(2871)**	
Asynchronous Addressable Receiver/Transmitter	—	4.75-11.5	MM54240	National		
	4.8	3-18	MC14469	Motorola		
Asynchronous Communications Element	56	5	**WD8250**	**Western**	**(2873)**	
Asynchronous Serial Manchester Adapter	1000	5	**HD6408**	**Harris**	**(669,675,1333)**	
Baud Rate Generator (programmable divider)	1000	5	COM8046	SMC		
			COM8046T	SMC		
			COM8126	SMC		20
			COM8126T	SMC		
			COM8146	SMC		
			COM8146T	SMC		
		12,5	COM5026	SMC		
			COM5026T	SMC		
			COM5046	SMC		
			COM5046T	SMC		
		12, ±5	F4702BC	Fairchild		
			F4702BM	† Fairchild		
			HD4702-2	**† Harris**	**(669,1333)**	30
			HD4702-9	**Harris**	**(669,1333)**	
			IM4702	Intersil		
			IM4703	Intersil		
			MC14411	**Motorola**	**(3298)**	
			MM5307	National		
Baud Rate Generator (programmable divider), Dual	307/19.2	5	**WD1943-00**	**Western**	**(2874)**	
			WD1943-02	**Western**	**(2874)**	
			WD1943-05	**Western**	**(2874)**	
		12,5	BR1941-00	Western		
			BR1941-02	Western		40
			BR1941-05	Western		
	614/19.2	5	**WD1943-04**	**Western**	**(2874)**	
			WD1943-06	**Western**	**(2874)**	
		12,5	BR1941-04	Western		
			BR1941-06	Western		
	1000	5	AY-5-8136	GI		
			AY-5-8136T	GI		
			AY-5-8816	GI		
			AY-5-8816T	GI		
			COM8116	SMC		50
			COM8116T	SMC		
			COM8136	SMC		

(Continued)

Function	Max Serial Data Rate in kHz	Supply Voltage, V	Device	Source		Line
Baud Rate Generator (programmable divider), Dual	1000	5				
						(Cont'd)
			COM8136T	SMC		
			WD1945	**Western**	**(2874)**	
		12,5	COM5016	SMC		
			COM5016T	SMC		
			COM5036	SMC		
			COM5036T	SMC		
BOART (Bus Orientated Programmable Asynchronous Receiver/Transmitter	9.6	5	TR1983	Western		
Bus Interface Circuit (MIL-STD1553B)	5000	5	HS3273	† Harris		60
Command/Response Manchester II Converter (MIL-STD-1553B)	1000	5	BUS-8937	† DDC		
			SSM-2012	SSM		
Digital Modern (Modulation, demodulation and supervisory control, up to 600 BPS.)	0.6	5	**MC6860**	**Motorola**	**(1351,3298)**	
DUART (Dual Universal Asynchronous Receiver and Transmitter). Two-channel UART, baud-rate generator, 16-Bit counter/timer, I/O ports.	1000	5	26810	Signetics		
			26814	Signetics		
			26818	Signetics		
			68681	Signetics		
EPCI (Enchanced Programmable Communications Interface) Serial/Parallel receiver/transmitter-Synchronous and asynchronous with baud rate generator.			MC2261A	Motorola		
			MC2261B	Motorola		
			MC2261C	Motorola		70
	1 Kb/s	5	**MC68661A**	**Motorola**	**(1360)**	
	15.6 Kb/s	5	**MC68661C**	**Motorola**	**(1360)**	
	62.5 Kb/s	5	**MC68661B**	**Motorola**	**(1360)**	
	1000 b/s	5	**SCN2661A**	**Signetics**	**(1521)**	
			SCN2661B	**Signetics**	**(1521)**	
			SCN2661C	**Signetics**	**(1521)**	
IBM 3274/3276 Compatible COAX Receiver/Transmitter	2358	5	COM9004	SMC		
Link Controller, X.25 level 2	100	5,12	**WD2501-01**	**Western**	**(2869)**	
			WD2511-01	**Western**	**(2869)**	
	500	5,12	**WD2501-03**	**Western**	**(2869)**	80
			WD2511-05	**Western**	**(2869)**	
	1000	5,12	**WD2501-11**	**Western**	**(2869)**	
			WD2511-11	**Western**	**(2869)**	
Manchester Encoder-Decoder	1000	5	**HD6409-2**	**† Harris**	**(669,680,1333)**	
			HD6409-9	**Harris**	**(669,680,1333)**	
			HS15530RH	† Harris		
	1250	5	**HD15530-2**	**† Harris**	**(669,688,1333)**	
			HD15530-9	**Harris**	**(669,688,1333)**	
			HD15531-2	**† Harris**	**(669,693,1333)**	
			HD15531-9	**Harris**	**(669,693,1333)**	90
	2500	5	**HD15531A**	**Harris**	**(669,693,1333)**	
MPCC (multi-protocol communications controller) Bit and Byte Oriented	1 Mb/s	5	SCN2652A	Signetics		
	2 Mb/s	5	**MC2652**	**Motorola**	**(1359)**	
			MC2652-2	**Motorola**	**(1359)**	
			MC68652	**Motorola**	**(1359)**	
			MC68652-2	**Motorola**	**(1359)**	
			μPD7201	NEC-Electron		

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

IC MASTER

INTERFACE–Transmitters-Receivers (Cont'd)

Serial Transmitters- Receivers (Cont'd)

Function	Max Serial Data Rate in kHz	Supply Voltage, V	Device	Source	Line
MPCC (multi-protocol communications controller) Bit and Byte Oriented	2 Mb/s	5			(Cont'd)
			SCN2652A	**Signetics**	**(1520)**
Parallel to Serial Interface	—	5 V	CY232	Cybernetic	
PCI (Programmable Communications Interface) Serial/parallel receiver/transmitter—synchronous and asynchronous with baud rate generator.	1000 b/s	5	**SCN2651C**	**Signetics**	**(1520)**
PKCC (Programmable Keyboard and Communications Controller) UART, baud rate generator and keyboard encoder	1000 b/s	5	SC2671ACS	Silicon G	
PSAR (Programmable Synchronous-Asynchronous Receiver) Synchronous/Asynchronous serial to parallel converter with programmable character length and programmable serial data rate.	100	−12,5	PT1472B	Western	
	640	−12,5	PT1472B-01	Western	
		−12, ±5	NC2259	Nitron	
PSART (Programmable Synchronous-Asynchronous Receiver-Transmitter) Serial to parallel and parallel to serial converter that can operate in Full Duplex Mode.	50	5	8251	Intel	
			μPD8251	NEC-Micro	
PSAT (Programmable Synchronous-Asynchronous Transmitter) Synchronous/Asynchronous parallel to serial converter that has programmable character length and programmable serial data rate.	100	−12,5	PT1482B	Western	10
	200	−12, ±5	NC2257	Nitron	
			NC2260	Nitron	
	640	−12,5	PT1482B-01	Western	
Receiver/Decoder (Bi-Phase)	3500	5	**DP8343**	**National**	**(2762)**
Receiver/Decoder (Bi-Phase, IBM 3270)	—	5	**DP8341**	**National**	**(2762)**
SDLC/HDLC/ADCCP Controller	500	5	WD193X-00/10	Western	
	1000	5	WD193X-01/11	Western	
	1500	5	WD193X-02/12	Western	
	2000	5	WD193X-03/13	Western	
SPCC (Sync-Protocol Communications Controller) Bit and Byte Oriented	1000	5	F3846	Fairchild	20
			F6856	**Fairchild**	**(1277)**
Synchronous Receiver/Transmitter (Bi-Sync/SDLC)	800	±5,12	μPD379	NEC-Micro	
Synchronous Serial Data Adaptor	2 Mb/s	5	**MC6852**	**Motorola**	**(1351)**
Transceiver, MIL-STD-1553A/B	1000	±12	BUS-8557	† DDC	
		±15/±12	BUS-63105	† DDC	
		±15,5	BUS-8553	† DDC	
			BUS-8554	† DDC	
			BUS-8555/56	† DDC	
			BUS-8559	† DDC	
Transmitter/Decoder (Bi-Phase, IBM 3270)	—	5	**DP8340**	**National**	**(2762)** 30
Transmitter/Encoder (Bi-Phase)	3500	5	**DP8342**	**National**	**(2762)**
UART, MIL-STD-1553A	1000	5	COM1553A	† SMC	
			COM1553B	SMC	
UART (Universal Asynchronous Receiver-Transmitter) (complete serial to parallel and parallel to serial interface)	56	5	**WD2123**	**Western**	**(2875)**
	60	5	**TR1863-00**	**Western**	**(2872)**

(Continued)

Function	Max Serial Data Rate in kHz	Supply Voltage, V	Device	Source	Line
UART (Universal Asynchronous Receiver-Transmitter) (complete serial to parallel and parallel to serial interface)	60	5			(Cont'd)
			TR1865-00	**Western**	**(2872)**
	100	5	HCMP1854C	† Hughes	
			CDP1854AC	**† RCA**	**(1476)**
	125	5	**HD6402C-9**	**Harris**	**(669,672,1333)**
	150	5	**TR1863-02**	**Western**	**(2872)** 40
			TR1865-02	**Western**	**(2872)**
	200	5	**HD6402-2**	**† Harris**	**(669,672,1333)**
			HD6402-9	**Harris**	**(669,672,1333)**
			IM6402	Intersil	
			IM6402M	† Intersil	
			IM6403	Intersil	
			IM6403M	† Intersil	
			CDP6402D	**† RCA**	**(1476)**
			CDP6402E	**RCA**	**(1476)**
			TR1863-04	**Western**	**(2872)** 50
			TR1865-04	**Western**	**(2872)**
	375	5	**HD6402A-2**	**† Harris**	**(669,672,1333)**
			HD6402A-9	**Harris**	**(669,672,1333)**
	400	3-12	HCMP1854	† Hughes	
			CDP1854	**† RCA**	**(1476)**
		5	HD6403A-2	† Harris	
			HD6403A-9	Harris	
	800	5	S1602	AMI	
			MB8868A	Fujitsu	
UART (Universal Asynchronous Receiver-Transmitter) complete serial to parallel and parallel to serial interface.	1.2	−12,5	10371	Rockwell	60
	20	−12,5	TR1402	Western	
			TR1602	Western	
	30	5	AY3-1015D	GI	
		−12,5	MM5303	National	
	40	5	COM1863	SMC	
			COM8017	SMC	
			COM8018	SMC	
			COM8502	SMC	
		−12,5	COM2017	SMC	
			COM2017H	SMC	70
			COM2502	SMC	
			COM2502H	SMC	
	56	5	INS8250	National	
Universal Communications Interface (Receives or transmits data to serial data bus when addressed and commanded by bus. Links the bus to serial or parallel I/O devices.)	500	−10,5	UMC-16	Trans-Data	
USRT (universal synchronous receiver-transmitter) Complete serial to parallel and parallel to serial interface.	250	−12,5	COM2601	SMC	
	500	5	S2350	AMI	
USYNRT (universal synchronous receiver/transmitter) Multi-Protocol, Bit and Byte Oriented	1500	5,12	SND5025	SSS	
			COM5025	SMC	
Dual Channel Asynchronous Serial Interface Circuit			**MC68681**	**Motorola**	**(1360)**

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

Advanced Micro Devices

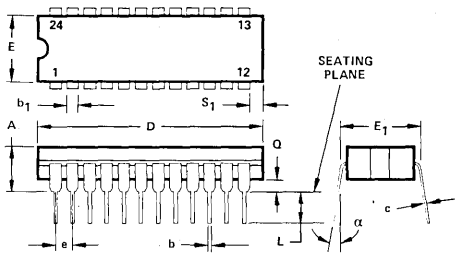
BIPOLAR LSI AND SUPPORT PRODUCTS
High Performance Bus Interface Circuits
The Am29800 Family

DISTINCTIVE CHARACTERISTICS

- Standard I/O pin-out organization
- 48mA Commercial I_{OL}
- 32mA Mil I_{OL}
- Standard clock and output enable pin-outs
- 24-pin slim 0.3 inch wide DIP package
- IMOX Speed
  - 7.5ns typical CP to Y for registers
  - 4.0ns typical D to Y for buffers
- Wide data paths and flexible control
  - 10 bits for video or wide addresses
  - 9 bits for byte plus parity buses
  - 8-bit with multiple enables
- 100% Product assurance screening to MIL-STD-883 requirements

PHYSICAL DIMENSIONS
Dual-In-Line

D-24-SLIM



HERMETIC DUAL IN-LINE PACKAGE

AMD Pkg	D-24-Slim	
Common Name	SLIM CERDIP	
38510 Appendix C	–	
Parameters	Min	Max
A	.140	.220
b	.016	.020
b_1	.045	.065
c	.009	.011
D	1.230	1.285
E	.245	.285
E_1	.290	.320
e	.090	.110
L	.120	.150
Q	.015	.060
S_1	.010	
α	3°	13°

FUNCTIONAL DESCRIPTION

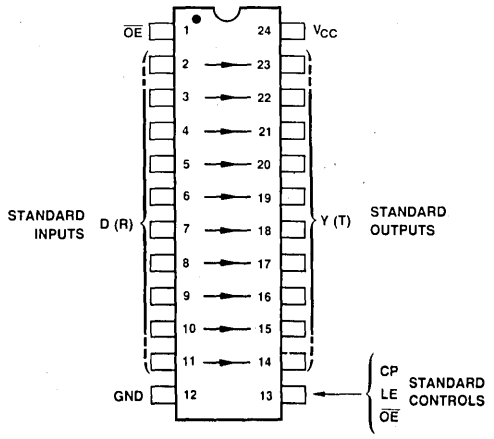
The Am29800 Family provides a completely standardized functional family of registers, latches, buffers, transceivers and parity check-and-regenerate functions optimized for bus interface applications. Each is packaged in the standard 24-pin x 0.3" wide DIP package to allow LSI functionality in the minimum board area. Board layout is eased by the standardization of inputs on the left and outputs on the right, directly across from each other. Output drive levels are standardized at 48mA Commercial and 32mA Military.

All functions are implemented in AMD's new proprietary IMOX™ (Implanted Micro OXide) process to provide the optimum in speed power product. Typical benchmark speeds are 7.5ns typical CP-to-Y for registers, and 4.0ns typical D-to-Y for buffers.

The basic 29800 Family functions are available in 10-bit, 9-bit and 8-bit configurations with broad control flexibility aimed at minimizing the SSI/MSI content of LSI systems. The 10-bit devices make it easy to interface data plus controls or for 2 parts to interface 20-bit address lines. The 9 bits function are ideal for byte plus parity bus structures. The parity check-and-regenerate functions are designed for interfacing non-parity peripherals to parity organized buses.

All of the functional types have the pin-out format shown below.

STANDARDIZED PIN-OUTS
FOR EASY BOARD LAYOUT



BLI-224

Advanced Micro Devices

BIPOLAR LSI AND SUPPORT PRODUCTS
High Performance Bus Interface Circuits
The Am29800 Family

Am29821/822/823/824/825/826

- High-speed parallel registers with positive edge-triggered D-type flip-flops
  - Noninverting CP-Y t_{PD} = 7.5ns typ
  - Inverting CP-Y t_{PD} = 7.5ns typ
- Buffered common Clock Enable ($\overline{EN}$)
- Buffered common asynchronous Clear input ($\overline{CLR}$)
- Three-state outputs glitch free during power-up and down
- Outputs have Schottky clamp to ground
- 48mA Commercial I_{OL}, 32mA MIL I_{OL}
- High capacitance load capability
- Low capacitance inputs and outputs
- I_{OH} specified 2.0V and 2.4V
- 24-pin 0.3" space saving package

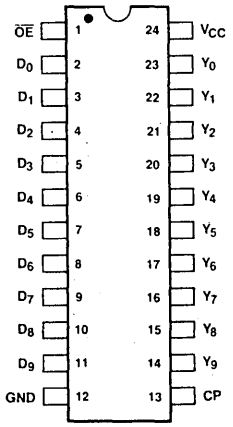
FUNCTIONAL DESCRIPTION

The Am29820 Series bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The Am29821 and Am29822 are buffered, 10-bit wide version of the popular '374 function. The Am29823 and Am29824 are 9-bit wide buffered registers with Clock Enable ($\overline{EN}$) and Clear ($\overline{CLR}$) – ideal for parity bus interfacing in high performance microprogrammed systems. The Am29825 and Am29826 are 8-bit buffered registers with all the '823/4 controls plus multiple enables ($\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$. They are ideal for use as an output port requiring high I_{OL}/I_{OH}.

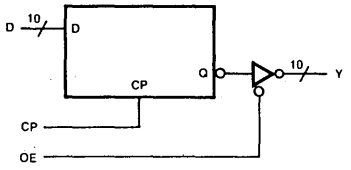
All of the Am29800 high performance interface family are designed for high capacitance load drive capability while providing low capacitance bus loading at both inputs and outputs. All inputs are Schottky diode inputs, and all outputs are designed for low capacitance bus loading in the high impedance state.

	Device		
	10-Bit	9-Bit	8-Bit
Noninverting	Am29821	Am29823	Am29825
Inverting	Am29822	Am29824	Am29826

Am29821/Am29822
10-BIT REGISTERS



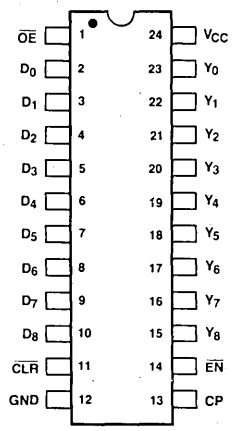
BLI-225



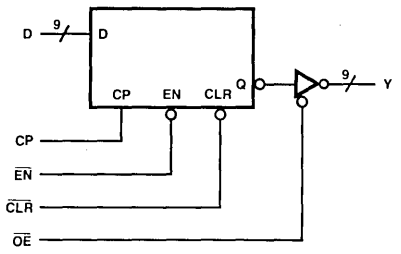
BLI-226

BIPOLAR LSI AND SUPPORT PRODUCTS
High Performance Bus Interface Circuits
The Am29800 Family

Am29823/Am29824
9-BIT REGISTERS

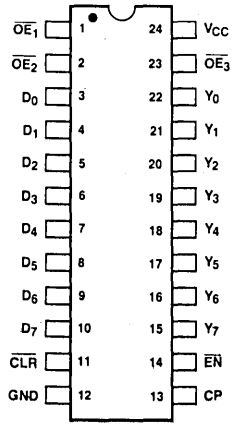


BLI-227

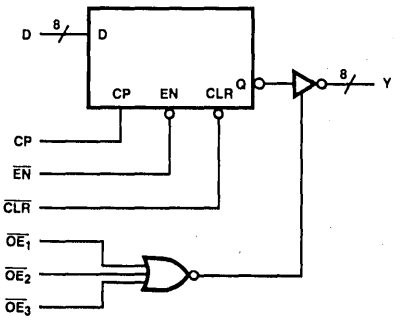


BLI-228

Am29825/Am29826
8-BIT REGISTERS



BLI-229



BLI-230

Advanced Micro Devices

BIPOLAR LSI AND SUPPORT PRODUCTS
High Performance Bus Interface Circuits
The Am29800 Family

Am29827/828, Am29861/862/863/864

- High-speed symmetrical bidirectional transceivers
  - Noninverting t_{PD} = 4.5ns typ
  - Inverting t_{PD} = 3.0ns typ
- High speed buffers and inverters
  - Noninverting t_{PD} = 4.5ns typ
  - Inverting t_{PD} = 3.0ns typ
- 200mV minimum input hysteresis on input data ports
- Three-state outputs glitch-free during power-up and down
- Outputs have Schottky clamp to ground
- 48mA Commercial I_{OL}, 32mA MIL I_{OL}
- High capacitance load capability
- Low capacitance inputs and outputs
- I_{OH} specified 2.0V and 2.4V
- 24-pin 0.3" space saving package

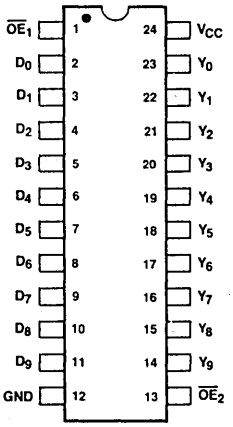
FUNCTIONAL DESCRIPTION

The Am29827 and Am29828 10-bit bus buffers and Am29860 Series bus transceivers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. The 10-bit buffers and 9-bit transceivers have NOR-ed output enables for maximum control flexibility. All buffer and transceiver data inputs have 200mV minimum input hysteresis to provide improved noise rejection.

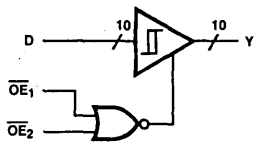
All of the Am29800 high performance interface family are designed for high capacitance load drive capability while providing low capacitance bus loading at both inputs and outputs. All inputs are Schottky diode inputs, and all outputs are designed for low capacitance bus loading in the high impedance state.

	Device		
	10-Bit Buffers	10-Bit Transceivers	9-Bit Transceivers
Noninverting	Am29827	Am29861	Am29863
Inverting	Am29828	Am29862	Am29864

Am29827/Am29828
10-BIT BUS DRIVERS



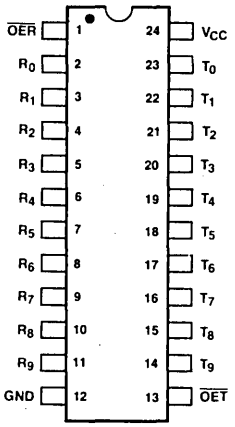
BLI-237



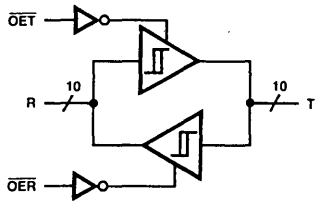
BLI-238

BIPOLAR LSI AND SUPPORT PRODUCTS
High Performance Bus Interface Circuits
The Am29800 Family

Am29861/Am29862
10-BIT TRANSCEIVERS

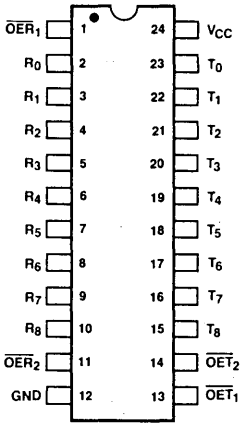


BLI-239

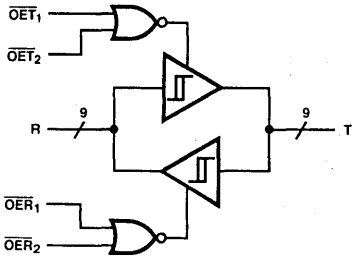


BLI-240

Am29863/Am29864
9-BIT TRANSCEIVERS



BLI-241

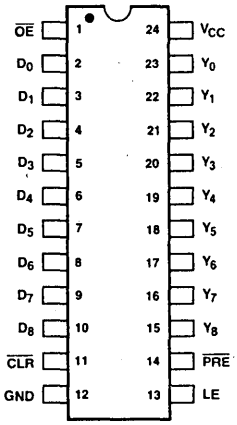


BLI-242

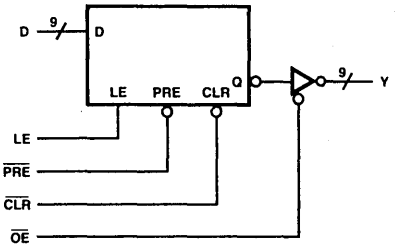
Advanced Micro Devices

BIPOLAR LSI AND SUPPORT PRODUCTS
High Performance Bus Interface Circuits
The Am29800 Family

Am29843/Am29844
9-BIT LATCHES

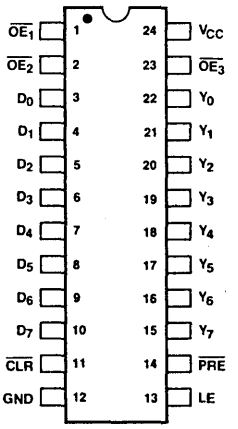


BLI-233

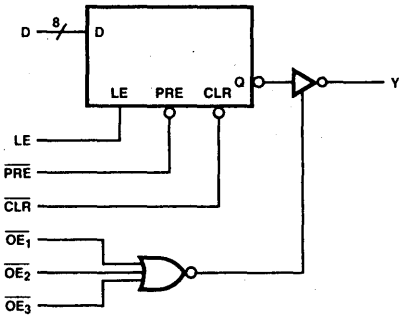


BLI-234

Am29845/Am29846
8-BIT LATCHES



BLI-235



BLI-236

BIPOLAR LSI AND SUPPORT PRODUCTS
High Performance Bus Interface Circuits
The Am29800 Family

Am29833/834

- High speed bidirectional transceivers for 8-bit non-parity to 9-bit with parity ports
  - Noninverting data t_{PD} = 6.0ns typ
  - Inverting data t_{PD} = 6.0ns typ
  - Parity generate t_{PD} = 9.0ns typ
- High speed parity generation for Transmit mode
- High speed parity fault detection for Receive mode
- Clearable, open-collector output, Fault Flag register
- 200mV minimum input hysteresis
- Three-state outputs glitch-free during power-up and down
- Outputs have Schottky clamp to ground
- 48mA Commercial I_{OL}, 32mA MIL I_{OL}
- High capacitance load capability
- Low capacitance inputs and outputs
- I_{OH} specified 2.0V and 2.4V
- 24-pin 0.3" space saving package

FUNCTIONAL DESCRIPTION

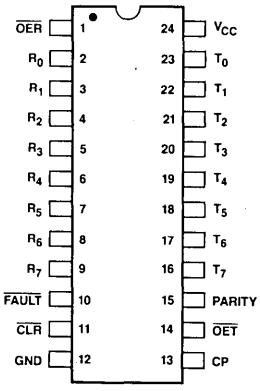
The Am29833 and Am29834 bidirectional transceivers are designed to interface an 8-bit data path without parity to a byte-parity 9-bit data path. All outputs – R_i, T_i and PARITY – have high I_{OL} drive capability and are ideal for device-to-bus or bus-to-bus interfacing.

The internal $\overline{\text{FAULT}}$ flag register is configured as a "one's catcher" to capture and hold any odd-parity fault occurring at the rising edge of the clock, CP. A registered $\overline{\text{FAULT}}$ output remains LOW until cleared. Also, the $\overline{\text{FAULT}}$ output is an open-collector output for wired-OR configurations where byte-parity is used for 16-bit or wider data fuses or where multiple port flags are wired-OR tied together.

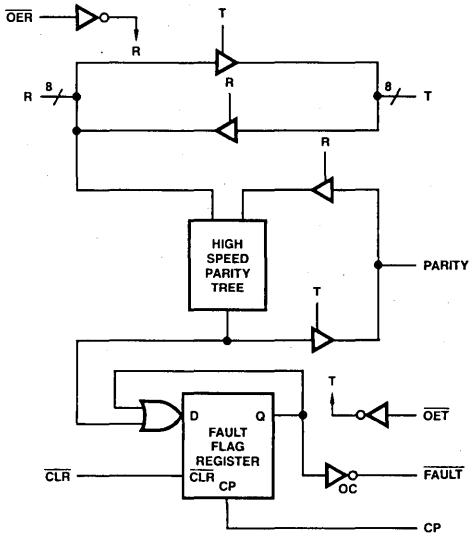
All of the Am29800 high performance interface familiy are designed for high capacitance load drive capability while providing low capacitance bus loading at both inputs and outputs. All inputs are Schottky diode inputs, and all outputs are designed for low capacitance bus loading in the high impedance state.

	Device
Noninverting	Am29833
Inverting	Am29834

Am29833/Am29834
8-BIT TO 9-BIT PARITY TRANSCEIVERS



BLI-243



BLI-244

Advanced Micro Devices

BIPOLAR LSI AND SUPPORT PRODUCTS
High Performance Bus Interface Circuits
The Am29800 Family

Am29841/842/843/844/845/846

- High-speed parallel latches
  - Noninverting transparent t_{PD} = 4.5ns typ
  - Inverting transparent t_{PD} = 6.0ns typ
- Buffered common latch enable input
- Buffered common clear input
- Buffered common preset input
- Three-state outputs glitch-free during power-up and down
- Outputs have Schottky clamp to ground
- 48mA Commercial I_{OL}, 32mA MIL I_{OL}
- High capacitance load capability
- Low capacitance inputs and outputs
- I_{OH} specified 2.0V and 2.4V
- 24-pin 0.3" space saving package

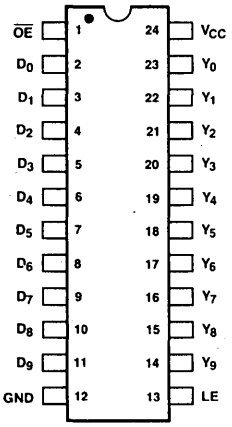
FUNCTIONAL DESCRIPTION

The Am29840 Series bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The Am29841 and Am29842 are buffered, 10-bit wide version of the popular '373 function. The Am29843 and Am29844 are 9-bit wide buffered latches with Preset ($\overline{PRE}$) and Clear ($\overline{CLR}$) – ideal for parity bus interfacing in high performance systems. The Am29845 and Am29846 are 8-bit buffered latches with all the '843/4 controls plus multiple enables ($\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$. They are ideal for use as an output port requiring high I_{OL}/I_{OH}.

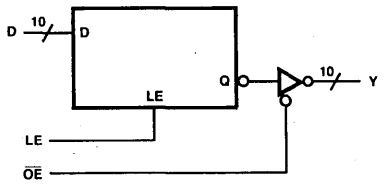
All of the Am29800 high performance interface family are designed for high capacitance load drive capability while providing low capacitance bus loading at both inputs and outputs. All inputs are Schottky diode inputs, and all outputs are designed for low capacitance bus loading in the high impedance state.

	Device		
	10-Bit	9-Bit	8-Bit
Noninverting	Am29841	Am29843	Am29845
Inverting	Am29842	Am29844	Am29846

Am29841/Am29842
10-BIT LATCHES



BLI-231



BLI-232

AMERICAN MICROSYSTEMS, INC.

S4535

32 BIT, HIGH VOLTAGE DRIVER

Features:

- ☐ High Voltage Outputs Capable of 60 Volt Swing
- ☐ Drives Up to 32 Devices
- ☐ Cascadable
- ☐ Requires Only 4 Control Lines

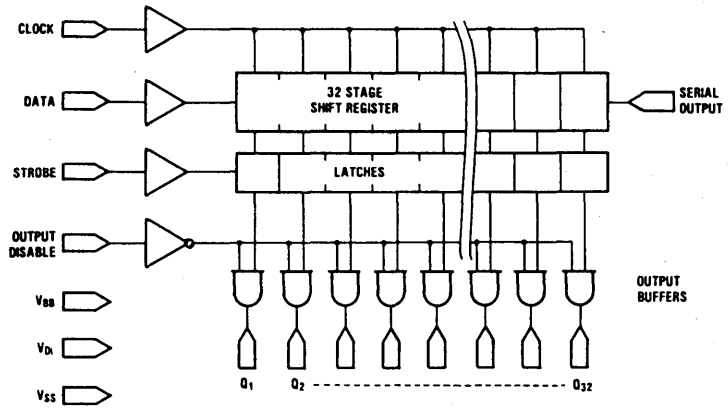
Applications:

- ☐ Vacuum Fluorescent Displays
- ☐ LED and Incandescent Displays
- ☐ Solenoids
- ☐ Print Head Drives
- ☐ DC and Stepping Motors
- ☐ Relays

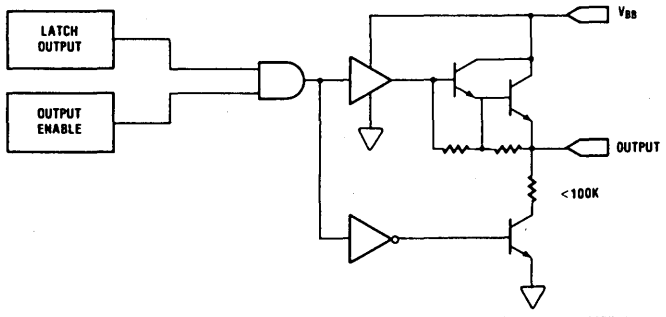
General Description

The AMI S4535 is a high voltage MOS/LSI circuit that drives a variety of output devices, usually under microprocessor control, by converting low level signals such as TTL, and CMOS to high voltage, high current drive signals. This device requires only four control lines due to its serial input construction. It latches the data to be output, or it may be used to bring data directly to the driver. The part acts as a versatile peripheral to drive displays, motors, relays and solenoids within its output limitations of a 60 volt swing and 25mA per drive. It is especially well suited to drive vacuum fluorescent displays due to its high voltage output capability. One circuit will drive up to 32 devices and more can be driven by cascading several drivers together.

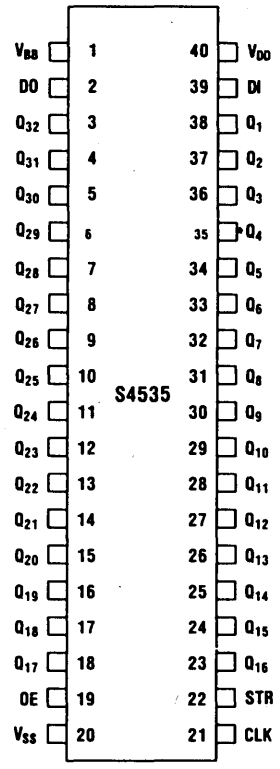
Functional Block Diagram



Output Buffer (Functional Diagram)



Pin Configuration



AMERICAN MICROSYSTEMS, INC.

S4521

32 BIT DRIVER

Features:

- ☐ Drives Up to 32 Devices
- ☐ Cascadable
- ☐ On Chip Oscillator
- ☐ Requires Only 3 Control Lines
- ☐ CMOS Construction For:
  - Wide Supply Range
  - High Noise Immunity
  - Wide Temperature Range

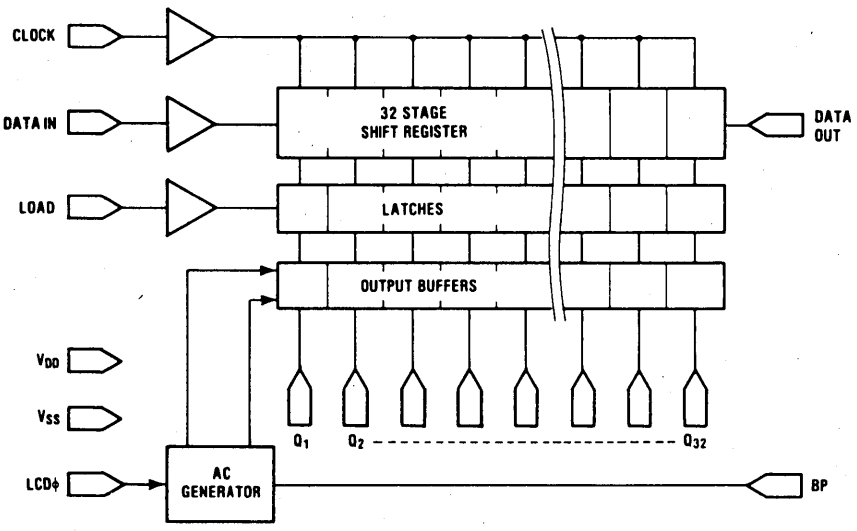
Applications:

- ☐ Liquid Crystal Displays
- ☐ LED and Incandescent Displays
- ☐ Solenoids
- ☐ Print Head Drives
- ☐ DC and Stepping Motors
- ☐ Relays

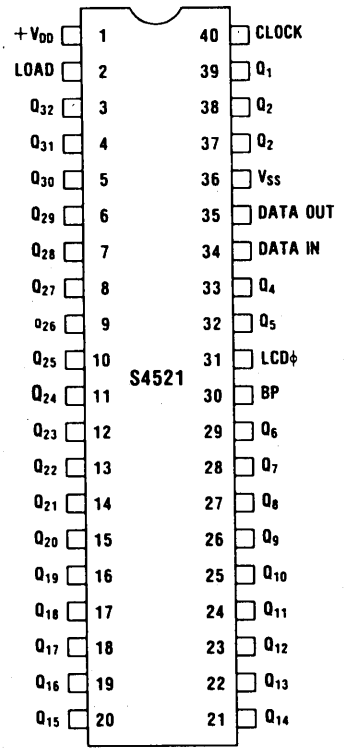
General Description

The AMI S4521 is a MOS/LSI circuit that drives a variety of output devices, usually under microprocessor control. This device requires only three control lines due to its serial input construction. It latches the data to be output, relieving the microprocessor from the task of generating the required waveform, or it may be used to bring data directly to the driver. The part acts as a versatile peripheral to drive displays, motors, relays and solenoids within its output limitations. It is especially well suited to drive liquid crystal displays as a backplane A.C. signal option is provided. The A.C. frequency of the backplane output can be user supplied or generated by attaching a capacitor and resistor to the LCDϕ input, which controls the frequency of the internal oscillator. One circuit will drive up to 32 devices and more can be driven by cascading several drivers together.

Functional Block Diagram



Pin Configuration



AMERICAN MICROSYSTEMS, INC.

S4534

10 BIT, HIGH VOLTAGE, HIGH CURRENT DRIVER

Features:

- ☐ Outputs Capable of 60 Volt Swings at 25mA
- ☐ Drives Up to 10 Devices
- ☐ Cascadable
- ☐ Requires Only 4 Control Lines

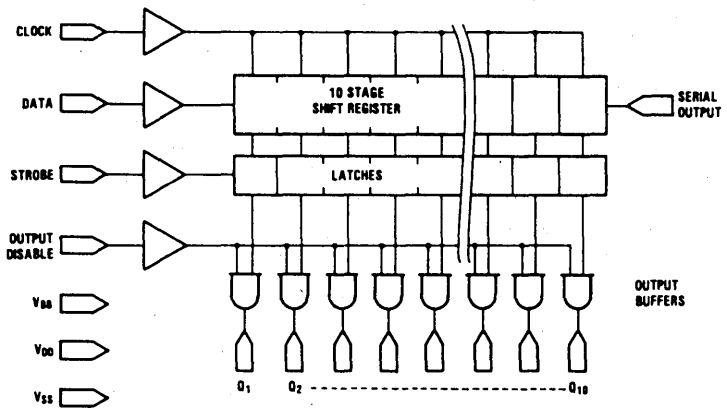
Applications:

- ☐ Vacuum Fluorescent Displays
- ☐ LED and Incandescent Displays
- ☐ Solenoids
- ☐ Print Head Drives
- ☐ DC and Stepping Motors
- ☐ Relays

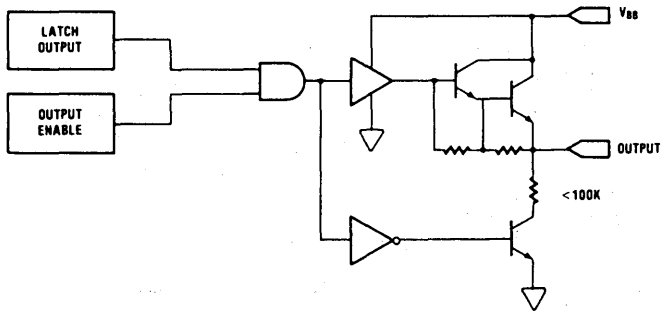
General Description

The AMI S4534 is a high voltage, high current MOS/LSI circuit that drives a variety of output devices, usually under microprocessor control, by converting low level signals such as TTL, and CMOS to high voltage, high current drive signals. This device requires only four control lines due to its serial input construction. It latches the data to be output, or it may be used to bring data directly to the driver. The part acts as a versatile peripheral to drive displays, motors, relays and solenoids within its output limitations of a 60 volt swing and 25mA per drive. It is especially well suited to drive vacuum fluorescent displays due to its high voltage output capability. One circuit will drive up to 10 devices and more can be driven by cascading several drivers together.

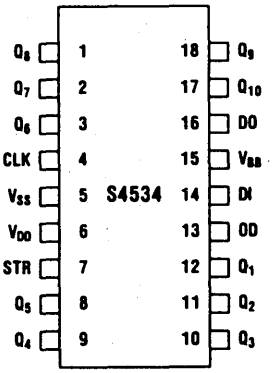
Functional Block Diagram



Output Buffer (Functional Diagram)



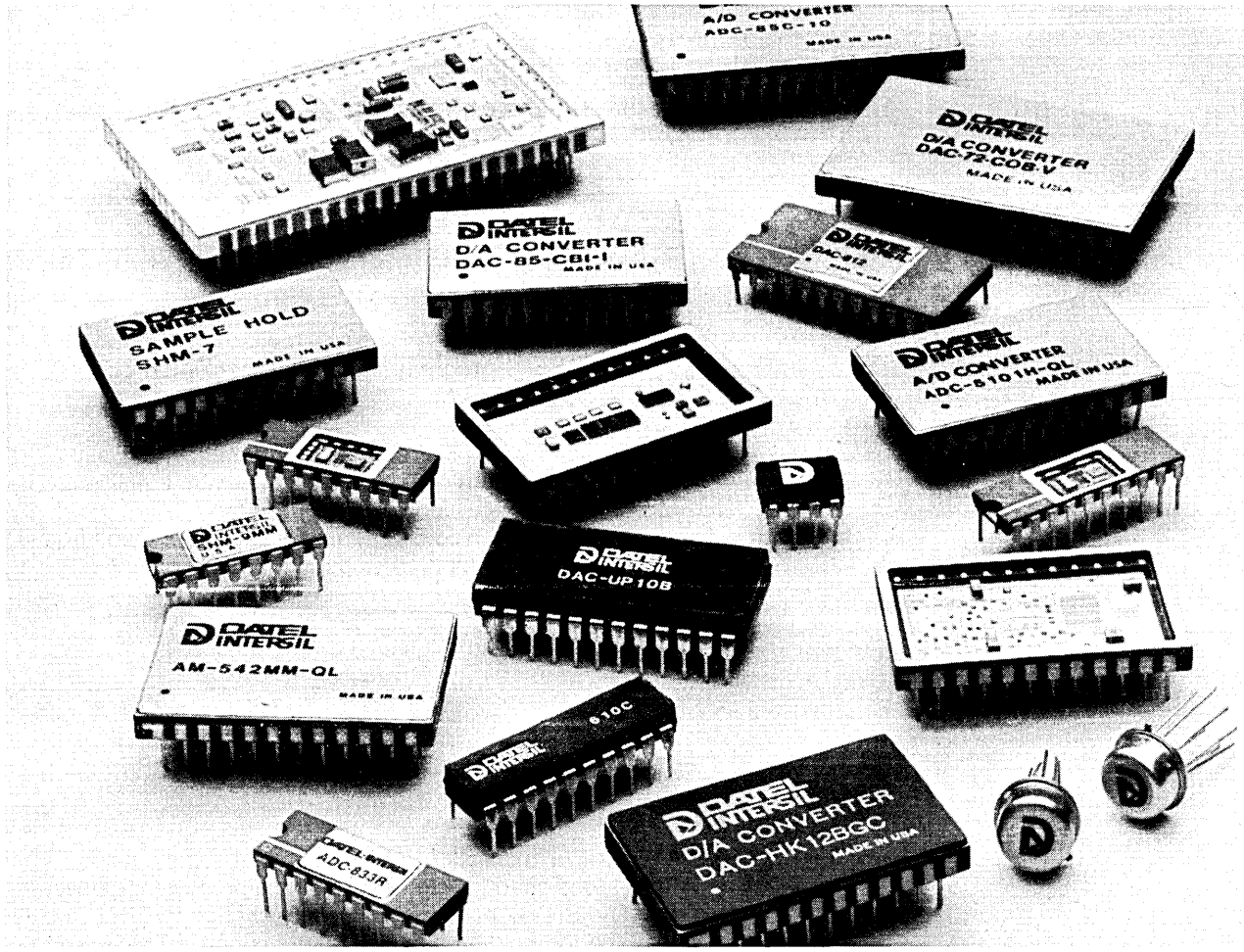
Pin Configuration



ABBREVIATIONS OF COMPANY NAMES

Action Ins	Action Instruments
AD	Analog Devices
ADT	Advanced Digital Technology
Adapt Sci	Adaptive Science Corp.
Advent	Advent Products, Inc.
Alphatron	Alphatron
AMA	American Automation
AMD	Advanced Micro Devices
AMI	American Microsystems, Inc.
Amperex	Amperex Electronic Corp.
Analogic	Analogic
Analog Sys	Analog Systems
APC	Applied Micro Circuits
Apex	Apex Microtechnology
APM	Applied Microsystems Corp.
Appl Sys	Applied Systems Corp.
APT	Applied Microtechnology
Aptek	Aptek Microsystems
Array Tech	Array Technology
AWI	Analog West
Bedford	Bedford Computer Systems Inc.
Burr-Brown	Burr-Brown Research
CAE	Computer Aided Engineering
Cal Devices	California Devices
Cent Data	Central Data Corp.
Cermetek	Cermetek
CGRS	CGRS Microtech Inc.
Cherry	Cherry Semiconductor
CIC	Custom Integrated Circuits
Citel	Citel, Inc.
Comlinear	Comlinear Corporation
CMA	Custom MOS Arrays
Comark	Comark Corp.
Comdial	Comdial Semiconductor
Comp Auto	Computer Automation
Compas	Compas Microsystems
Cont Logic	Control Logic Inc.
Control Sys	Control Systems Microsystems Div.
CreMicro	Creative Micro Systems
Cromemco	Cromemco, Inc.
CSG	Commodore Semiconductor Group
Cubit	Cubit Inc.
Curtis	Curtis Electro Devices, Inc.
Cybernetic	Cybernetic Micro Systems
Cybersys	Cybersystems
Cybertek	Cybertek Inc.
Data General	Data General
Data I/O	Data I/O
Data Trans	Data Translation
Datel	Datel-Intersil
Datricon	Datricon Corporation
DDC	Data Devices Corporation
DEC	Digital Equipment Corporation
Delco	Delco Electronics
DGM	Digital Microsystems
Digelec	Digelec Corp.
Digitek	Digitek, Inc.
Dionics	Dionics Inc.
Dist Comp	Distributed Computer Systems
Divers Tech	Diversified Technology
E-HI	E-H International, Inc.
Elind	Elind Elettronica Industriale
EL Instr	E & L Instruments
EMM	EMM
Emulogic	Emulogic Inc.
Epson	Epson America, Inc.
ETI Micro	ETI Micro
Exar	Exar Integrated Systems
Fairchild	Fairchild
Ferranti	Ferranti Electric
Fujitsu A	Fujitsu America
Fujitsu	Fujitsu Microelectronics, Inc.
GI	General Instrument
GMS	General Microsystems
GTE Micro	GTE Microcircuits
Harris	Harris Semiconductor
Heurikon	Heurikon Corp.
Hilevel	Hilevel Technology, Inc.
Hitachi	Hitachi America, Ltd.
Holt	Holt Inc.
HP	Hewlett-Packard
Hughes	Hughes Aircraft, Solid State Products
Hybrid Sys	Hybrid Systems
Hycom	Hycom Incorporated
IDT	Integrated Device Technology
IMI	International Microcircuits, Inc.
IMP	International Microelectronic Products
IMS	Industrial Micro-systems Inc.
Inconix	Inconix Corporation
Ind Tech	Inductive Technology
Inmos	Inmos
IntCirEng	Integrated Circuit Engineering
IntCirSys	Integrated Circuit Systems
IntCompSys	Integrated Computer Systems
IntCyber	International Cybernetics
Int Micro	International Microsystems
Int Tech	Integrated Technology Corp.
Intech/FMI	Intech/Function Modules Inc.
Intel	Intel
Interdesign	Interdesign
Intersil	Intersil
Intronics	Intronics
IPI	Integrated Photomatrix Inc.
ITT	ITT Semiconductors
Kinetic Sys	Kinetic Systems
Kontron	Kontron Electronics
Lambda	Lambda Semiconductor
Laserdyne	Laserdyne
LSI Comp	LSI Computer Systems
LSI Logic	LSI Logic Corporation
Master Logic	Master Logic Corporation
Matrix	Matrix Corp.
Matrox	Matrox Electronic Systems
MCC	Microcomputer Control
Micrel	Micrel
Micro Eng	Micro Circuit Engineering
Micro Innov	Micro Innovators
Micropac	Micropac Industries
Micro Net	Micro Networks
Micro Pwr	Micro Power Systems
Micro Sci	Micro Sciences Corp.
Micro Tech	Microcircuits Technology
Micro-Link	Micro-Link Corporation
Micron	Micron Technology
MilerTron	MilerTronics
Miller	Miller Technology
Mitel	Mitel Semiconductor
Mitsubishi	Mitsubishi Electronics
MMI	Monolithic Memories, Inc.
Monosil	Monosil
MonSys	Monolithic Systems Corp.
Mostek	Mostek
Motorola	Motorola Semiconductor
MRC	MRC Systems
Murray	Murray Consulting
National	National Semiconductor
NCR	NCR Corp., Microelectronics Division
NEC-EA	NEC/Electronic Arrays Division
NEC Electron	NEC/Electron Division
NEC Micro	NEC/Microcomputer Division
Nitron	Nitron
Nortek	Nortek
OAE	Oliver Advanced Engineering
Octagon	Octagon Systems Corp.
OEI	Optical Electronics Inc.
Ohio Sci	Ohio Scientific
OKI	OKI Semiconductor
Omnibyte	Omnibyte Corp.
Oscar	I. S. Oscar Assoc.
Panasonic	Panasonic
PC/M	Pacific/Cyber Metrix
Percom	Percom Data Co.
Phoenix	Phoenix Digital Corp.
Pico Design	Pico Design
Polycore	Polycore Electronics
Plessey	Plessy Semiconductors
PMI	Precision Monolithics, Inc.
PragDes	Pragmatic Design Inc.
PREMA	PREMA GmbH
Pro-Log	Pro-Log Corp.
Quay	Quay Corp.
Raytheon	Raytheon Semiconductor
RCA	RCA Solid State Division
RCI Data	RCI Data
RELMS	Relational Memory Systems
Reticon	Reticon
RIFA	RFIA
Rockwell	Rockwell, Microelectronic Devices
RTC	Riehl Time Corporation
Sanken	Sanken Electric
Sanyo	Sanyo
SEEQ	SEEQ Technology, Inc.
Semi Proc	Semi Processes
Siemens	Siemens
Signetics	Signetics
SGS	SGS-ATES Semiconductor
Sharp	Sharp
Silicon G	Silicon General
Siliconix	Siliconix
Silicon Sys	Silicon Systems Inc.
Siltronics	Siltronics
SMC	Standard Microsystems Corp.
Solarise	Solarise Enterprises
Solitron	Solitron Devices
Sprague	Sprague Electric Company
SSM	Solid State Micro Technology for Music
SSS	Solid State Scientific
Stag	Stag Microsystems
Struc. Des.	Structured Design Inc.
Stynetic	Stynetic Systems
Sunrise	Sunrise Electronics
Sunshine	Sunshine Semiconductor
Supertex	Supertex Inc.
Symtek	Symtek Corp.
Synapse	Synapse Corp.
Synertek	Synertek
Sys Innov	Systems Innovations
Tau Zero	Tau Zero Inc.
Tektronix	Tektronix
Telaris	(See Laserdyne)
Teledyne C	Teledyne Crystalonics
Teledyne P	Teledyne Philbrick
Teledyne S	Teledyne Semiconductor
Telefunken	Telefunken
Telephonics	Telephonics LSI
Telmos	Telmos
Teltone	Teltone Corporation
TI	Texas Instruments
Thomson-CSF	Thompson-CSF Components Corp.
TMX	TMX
Topanga	Topanga Data Systems
Toshiba	Toshiba America
Trans-Data	Trans-Data
TRW	TRW-LSI Products
Unitrode	Unitrode
Universal	Universal Semiconductor, Inc.
Vantage	Vantage Data Products
VTI	VLSI Technology, Inc.
Votrax	Votrax
Weitek	Weitek Corporation
Western	Western Digital
Wintek	Wintek Corp.
Xicor	Xicor, Inc.
Xycom	Xycom
Zendex	Zendex Corp.
Zilog	Zilog
Zymos	Zymos Corporation

Data Conversion Products



Datel-Intersil is located in Mansfield, Massachusetts, approximately 35 miles from Boston. The modern, 120,000-square-foot facility houses our administrative offices, our components and systems engineering groups, modular and systems production facilities, and the most modern thin-film-hybrid production facility in the industry.

Datel-Intersil offers one of the broadest lines of data-conversion products in the industry. Included are A/D and D/A converters, sample-and-holds, operational and instrumentation amplifiers, and data-acquisition systems — all packaged using the latest in thin-film, hybrid-microelectronic-circuit manufacturing technologies.

Datel-Intersil also offers fast delivery. On standard products, delivery typically runs from stock to four weeks and from six to eight weeks for full military-grade products with Class 883B screening.

Datel-Intersil is dedicated to maintaining its position as an international leader in data-conversion technology. You can depend on Datel-Intersil for a steady flow of new products to meet the growing demand for high-performance data-acquisition products.

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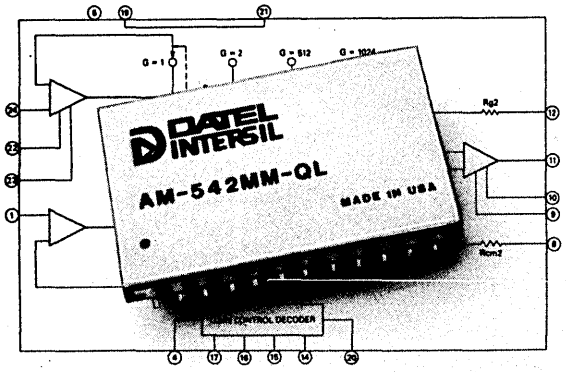
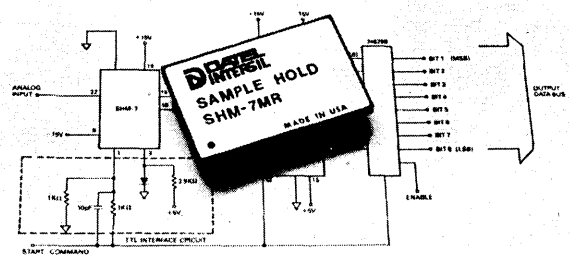
• INTERSIL DATEL GmbH-TEL. (089)530741 • DATEL KK TOKYO-TEL. 793-1031

New Products from Datel Intersil



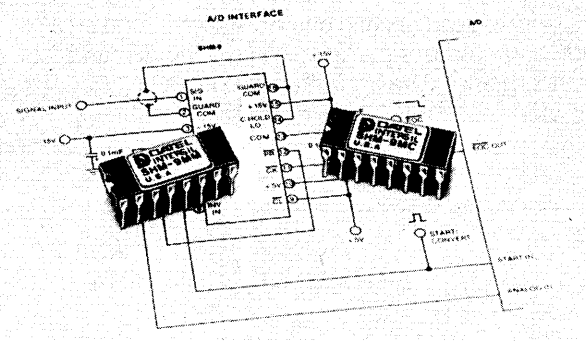
AM-542, AM-543 programmable gain instrumentation amplifiers feature digital gain selection

The AM-542 and AM-543 are high-performance, digitally-controlled, programmable-gain instrumentation amplifiers. The AM-542 permits selection of gains from 1 to 1024 in 11 binary weighted steps; the AM-543 permits selection of gains from 1 to 128 in 8 binary weighted steps. Gain selection is accomplished through the input of a 4-bit word. The AM-542 is optimized for low-drift, low-noise performance while the AM-543 is tailored for high-speed applications.



SHM-7 new video speed sample-hold features ultra-high speed and dual outputs

DATEL-INTERSIL's SHM-7 is an ultra-fast sample-hold amplifier designed for high-speed signal processing applications. The SHM-7 acquires a 2V input change to 0.1% in only 40 ns and the hold mode settling time is only 20 ns; making possible sampling rates of up to 17MHz. A unique feature of the SHM-7 is its dual outputs, each with a ±5V output voltage range at 30 mA and an output impedance of 13Ω. The outputs may be tied together to increase the output current and decrease the output impedance.



SHM-9 fast sample-hold features high performance at low cost

The SHM-9 is a complete, self-contained sample-hold amplifier that combines high performance versatility with low cost ($39.00, 1-24 qty). The SHM-9 includes a bipolar input amplifier, a low-leakage electronic switch, a FET output amplifier, a precision 1000 pF hold capacitor and logic control circuitry. The internal control circuitry allows the SHM-9 to be interfaced with virtually any A/D converter using the converter's Start/Convert and E.O.C. (status) signals. Active laser trimming of highly stable thin-film resistor networks minimizes offset and sample-to-hold offset errors, eliminating the need for external adjustment circuits.

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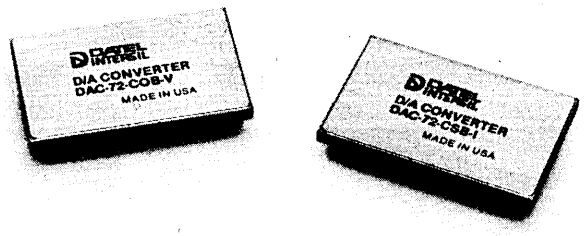
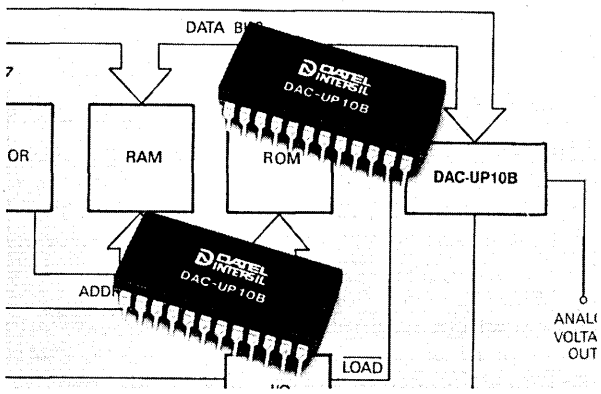


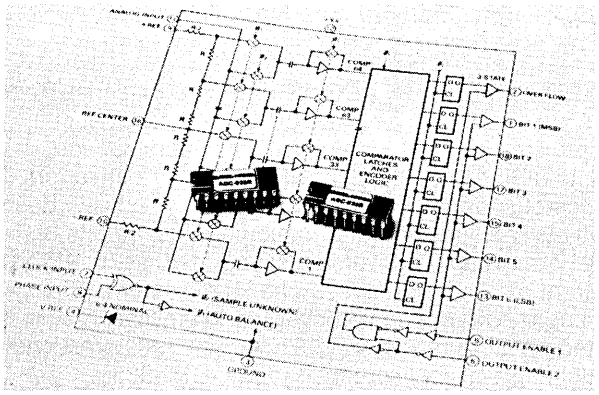
DAC-72 industry standard, high resolution microelectronic D/A converter

The DAC-72 series is a comprehensive family of high performance 16-bit D/A converters offering voltage or current outputs with either complementary binary or 4-digit BCD, TTL compatible, input coding. Linearity error is ±0.003% FSR maximum and settling time for an output voltage step of 20V to ±0.003% is only 10 μs. Current output settling time, 2 mA to ±0.003%, is only 1 μs. All models are cased in a miniature, hermetically sealed, 24-pin package and are completely pin and function compatible with industry standard DAC-72 converters.



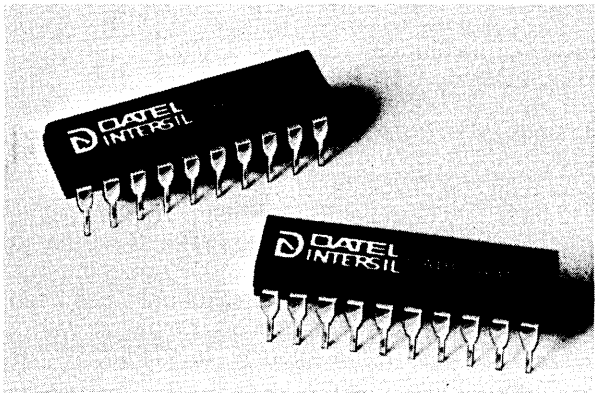
DAC-UP10B new 10-bit D/A with input registers

The DAC-UP10B is a low cost, monolithic, 10-bit D/A converter with internal registers. The device also includes a high-speed output amplifier, stable internal reference, and an input buffer amplifier. Low loading latches, adjustable logic thresholds and addressing capability allow the DAC-UP10B to directly interface with many microprocessor and logic controlled systems. The output voltage range is 0 to +10V for unipolar mode, ±5V for bipolar. A full scale output change settles to within 0.05% FSR in 5 μs.



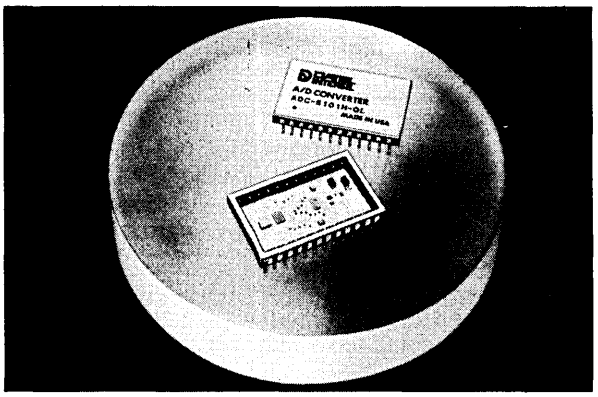
ADC-833 6-bit A/D features video speed at low power

The ADC-833 is a low-power, video-speed, 6-bit flash A/D manufactured with CMOS/SOS technology. The device is capable of digitizing an analog input signal at conversion rates up to 15MHz while its power consumption is only 200mW. The analog input voltage range is +2.5V to +10V, and typical differential linearity error is only ±½ LSB. Outputs are buffered three-state and include an overflow output which allows the user to cascade two units to achieve 7-bit resolution.



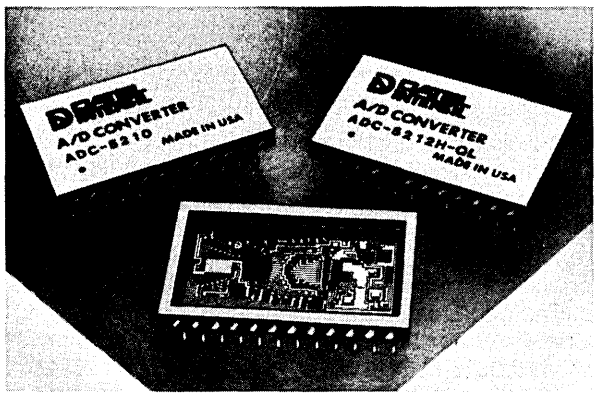
ADC-830 microprocessor compatible 8-bit A/D converter

DATEL-INTERSIL's ADC-830 is a low-cost, monolithic 8-bit A/D converter designed to operate directly with the 8080A control bus via three-state outputs. The device appears as a memory location or I/O port to the microprocessor and thus does not require interfacing logic. Using the successive approximation technique and a modified potentiometric resistor ladder, the ADC-830 achieves an 8-bit conversion in 100 μs with a maximum total adjusted error of only ±½ LSB. Its combination of low cost, small size, and interface versatility make the ADC-830 an ideal choice for many process control and instrumentation applications.



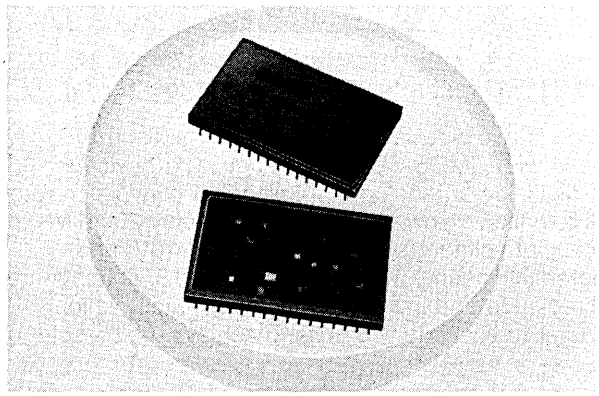
ADC-5101 high speed, 8-bit A/D offers high temperature operation at low cost

The ADC-5101 is a high speed, adjustment-free, 8-bit A/D converter. Pin compatible with standard ADC-5101 converters, these devices offer high accuracy and high speed over the full military operating temperature range of −55°C to +125°C. Designed for operation without external adjustment circuits, the ADC-5101 accomplishes an 8-bit conversion in only 900 ns maximum. Models are available subjected to 100% screening to MIL-STD-883 Class B.



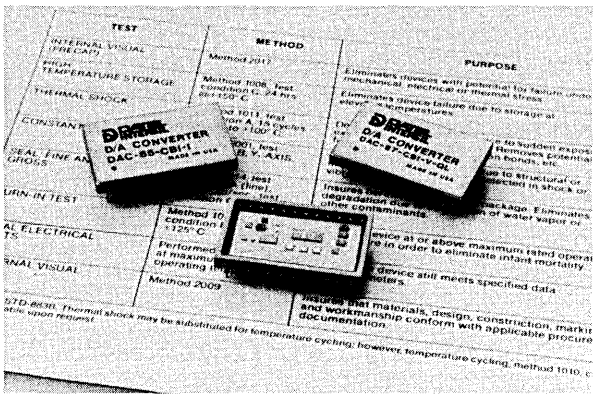
ADC-5210 series adjustment-free 12-bit A/D features high accuracy over military temperature range

The ADC-5210 series are high performance, 12-bit successive approximation A/D converters. Completely pin and function compatible with standard ADC-5210 devices, these models offer significantly improved high-temperature operation at lower cost. Full scale absolute accuracy error is a maximum of ±0.05% FSR at +25°C and only ±0.2% FSR over the full military operating temperature range of −55°C to +125°C; an improvement of 10 LSBs over the error specified on competing devices. MIL-STD-883 screening is available.



ADC-84, 85, 87 new, industry standard military and industrial 12-bit A/D converters

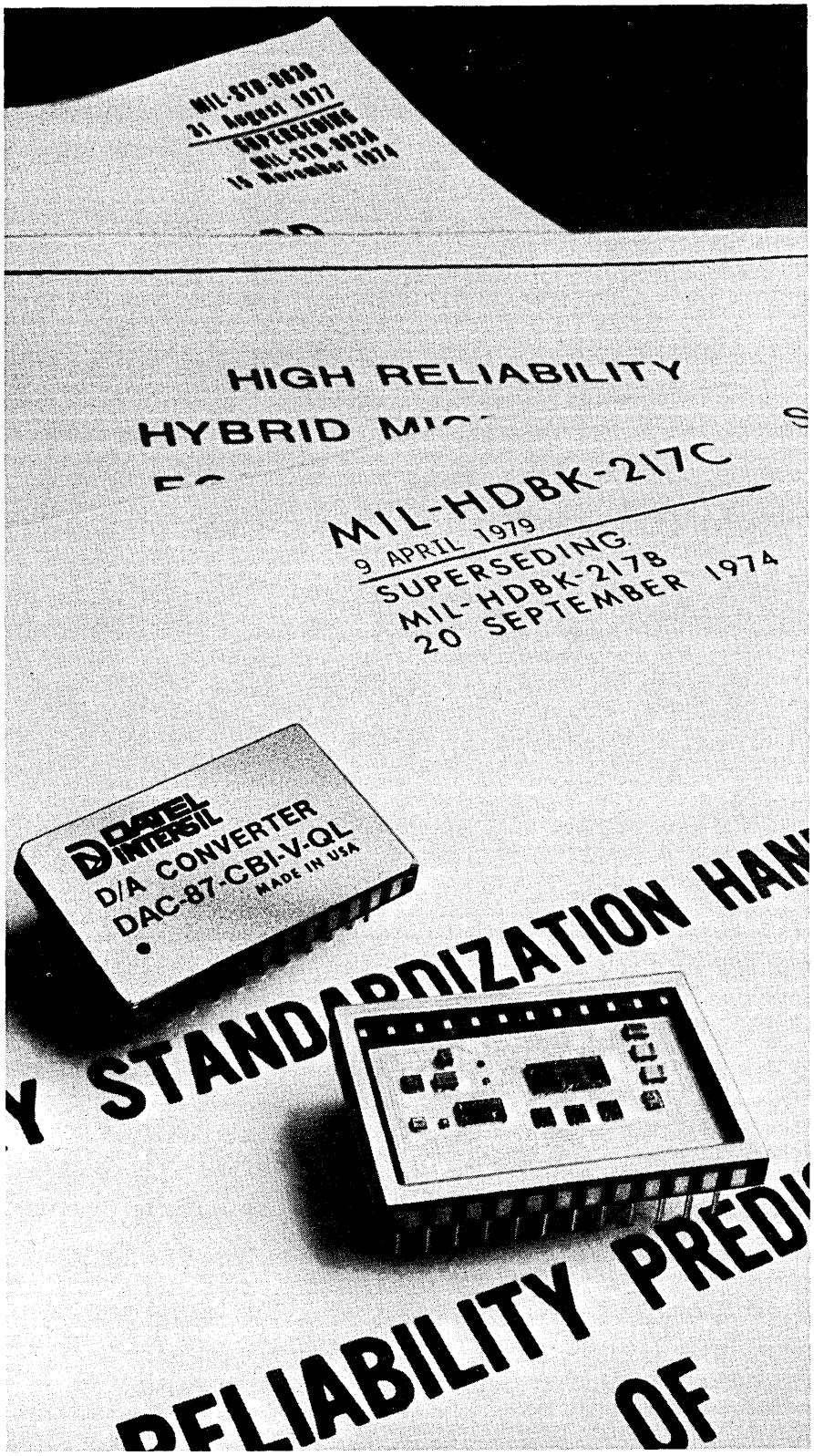
DATEL-INTERSIL's ADC-84, ADC-85, and ADC-87 series devices are high-performance, low-cost 10 and 12-bit successive approximation analog to digital converters. Direct replacements for industry standard ADC-84/85/87 converters, these devices offer improved performance and reliability. Each converter is available in two performance grades; 12 bits of resolution at a maximum conversion speed of 10 μs, or 10 bits of resolution at a conversion speed of 6 μs maximum. The ADC-87 is specified for operation over the full military operating temperature range of −55°C to +125°C. Versions of this model are availabel screened to MIL-STD-883B.



DAC-85, DAC-87 new, industry standard military and industrial 12-bit D/A converter

The DAC-85 and DAC-87 are DATEL-INTERSIL's new high-performance, 12-bit D/A converters. This comprehensive line of D/As allows a choice of voltage or current output models with either 12-bit binary or 3-digit BCD coding. The DAC-87 is specified for operation over the −55°C to +125°C military temperature range, and is available with 100% screening in accordance with MIL-STD-883B. This family of units has been specifically designed to be pin and function compatible with industry standard DAC-85/87 converters while offering substantially improved performance.

MIL-STD-883B HYBRIDS?



Datel-Intersil delivers fast...

Industry standard products . . .
You can get delivery on data conversion hybrids screened to MIL-STD-883B class B from stock to six weeks. And we mean production quantities — not just samples — (of proprietary and second-source industry standard devices). For example, the DAC-87 offers a full range of current or voltage output models with either binary or BCD coding.

Built by the book...
Fast turnaround on mil-spec and hi-rel hybrids is easier for us than for others because Datel-Intersil has one of the largest, most completely automated hybrid production facilities in the industry. And, our entire hybrid operation, including lot control, quality control, calibration control, manufacturing and testing facilities has been designed to comply with MIL-M-38510.

Proven in the field...
Datel-Intersil delivers on performance. Our hybrids are proving their reliability in many of today's most demanding military applications — the F-18, F-16 and XM-1 tank, to name just a few. And, if you happen to need screening beyond 883B class B, such as class S, we are ready to meet your requirements.

To meet your needs...
If you're fed up with trade-offs — in performance, delivery and price — come to Datel-Intersil. We're your dependable source for data conversion hybrids ... made to the industry's highest quality and reliability standards ... delivered when you need them ... at prices that make them the industry's best value.

Want to know more? contact:

DATEL INTERSIL

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PRICES AND SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

Hybrid military products

Datel-Intersil is a recognized industry leader in the design and manufacture of thin film hybrid data conversion products which meet the most demanding reliability requirements for military and aerospace applications per MIL-specifications. Datel-Intersil's data conversion products are currently used in a wide number of military and aerospace flight systems and in high reliability ground support and test systems. Datel-Intersil's modern 120,000 square foot manufacturing facility in Mansfield, Massachusetts includes the most automated and advanced manufacturing, test and calibration equipment available in the industry. This capability, supported by a Quality Assurance Program with full emphasis on product quality assurance and reliability, provides an experienced and reliable source for data converter products to the screening and qualification requirements of Methods 5004, 5005, and 5008 of MIL-STD-883B in compliance with MIL-M-38510 (specified by Datel-Intersil as "Q.L." devices).

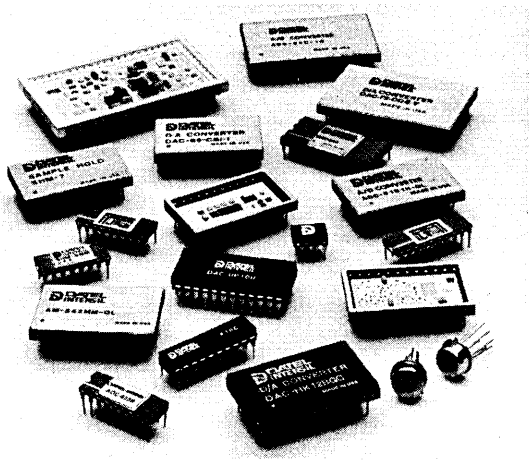
The Quality Assurance operation at Datel-Intersil monitors all areas of manufacturing and test, controls manufacturing and screening standards, maintains lot traceability procedures, and sets material standards to assure product quality. All purchased and internally manufactured components are procured or manufactured to precise specification control drawings. All components are 100% electrically tested and 100% visually inspected either by the vendors or internally within Datel-Intersil's facilities. Assembly and test processes and work stations are carefully monitored by Quality Assurance using fully documented procedures to guarantee high standards of workmanship and quality in all of Datel-Intersil's products.

Datel-Intersil products with the suffix "Q.L." are fully screened in accordance with Methods 5004 and 5008 of MIL-STD-883B as amended by MIL-M-38510. The following list briefly summarizes Datel-Intersil's hybrid military products.

ANALOG-TO-DIGITAL CONVERTERS

	MODEL NO.	RESOLUTION	CONVERSION TIME	LINEARITY	OPERATING TEMP. RANGE (°C)
	ADC-HC12BMM	12 bits	300 µsec	± ½ LSB	−55 to +125
	ADC-HC12BMM-QL	12 bits	300 µsec	± ½ LSB	−55 to +125
	ADC-HS12BMM	12 bits	9 µsec	± ½ LSB	−55 to +100
	ADC-HS12BMM-QL	12 bits	9 µsec	± ½ LSB	−55 to +100
	ADC-HX12BMM	12 bits	20 µsec	± ½ LSB	−55 to +100
	ADC-HX12BMM-QL	12 bits	20 µsec	± ½ LSB	−55 to +100
	ADC-HZ12BMM	12 bits	8 µsec	± ½ LSB	−55 to +100
	ADC-HZ12BMM-QL	12 bits	8 µsec	± ½ LSB	−55 to +100
NEW	ADC-87-10	10 bits	6 µsec	± ½ LSB	−55 to +125
NEW	ADC-87-10-QL	10 bits	6 µsec	± ½ LSB	−55 to +125
NEW	ADC-87-12	12 bits	10 µsec	± ½ LSB	−55 to +125
NEW	ADC-87-12-QL	12 bits	10 µsec	± ½ LSB	−55 to +125
	ADC-815MM	8 bits	700 nsec	± ½ LSB	−55 to +125
	ADC-815MM-QL	8 bits	700 nsec	± ½ LSB	−55 to +125
	ADC-816MM	10 bits	800 nsec	± ½ LSB	−55 to +125
	ADC-816MM-QL	10 bits	800 nsec	± ½ LSB	−55 to +125
	ADC-817MM	12 bits	2 µsec	± ½ LSB	−55 to +125
	ADC-817MM-QL	12 bits	2 µsec	± ½ LSB	−55 to +125
	ADC-825MM	8 bits	1 µsec	± ½ LSB	−55 to +125
	ADC-825MM-QL	8 bits	1 µsec	± ½ LSB	−55 to +125
	ADC-826MM	10 bits	1.4 µsec	± ½ LSB	−55 to +125
	ADC-826MM-QL	10 bits	1.4 µsec	± ½ LSB	−55 to +125
	ADC-827MM	12 bits	3 µsec	± ½ LSB	−55 to +125
	ADC-827MM-QL	12 bits	3 µsec	± ½ LSB	−55 to +125
NEW	ADC-5101H	8 bits	900 nsec	± ½ LSB	−55 to +125
NEW	ADC-5101H-QL	8 bits	900 nsec	± ½ LSB	−55 to +125
NEW	ADC-5210H	12 bits	13 µsec	± ½ LSB	−55 to +125
NEW	ADC-5210H-QL	12 bits	13 µsec	± ½ LSB	−55 to +125
NEW	ADC-5211H	12 bits	13 µsec	± ½ LSB	−55 to +125
NEW	ADC-5211H-QL	12 bits	13 µsec	± ½ LSB	−55 to +125
NEW	ADC-5212H	12 bits	13 µsec	± ½ LSB	−55 to +125
NEW	ADC-5212H-QL	12 bits	13 µsec	± ½ LSB	−55 to +125
NEW	ADC-5213H	12 bits	13 µsec	± ½ LSB	−55 to +125
NEW	ADC-5213H-QL	12 bits	13 µsec	± ½ LSB	−55 to +125
NEW	ADC-5214H	12 bits	13 µsec	± ½ LSB	−55 to +125
NEW	ADC-5214H-QL	12 bits	13 µsec	± ½ LSB	−55 to +125
NEW	ADC-5215H	12 bits	13 µsec	± ½ LSB	−55 to +125
NEW	ADC-5215H-QL	12 bits	13 µsec	± ½ LSB	−55 to +125
NEW	ADC-5216H	12 bits	13 µsec	± ½ LSB	−55 to +125
NEW	ADC-5216H-QL	12 bits	13 µsec	± ½ LSB	−55 to +125

Commercial and Industrial Products



For less demanding commercial/industrial requirements, Datel-Intersil offers a comprehensive selection of high quality data acquisition products. Included are A/D and D/A Converters, Sample and Holds, Operational and Instrumentation Amplifiers and Data Acquisition Subsystems.

Advanced manufacturing techniques, measurement and test equipment, combined with definitive quality assurancy procedures guarantee that all of Datel-Intersil's products meet or exceed the most exacting standards of workmanship. The following list briefly summarizes the commercial and industrial products offered by Datel-Intersil.

ANALOG TO DIGITAL CONVERTERS

	MODEL NO.	RESOLUTION	CONVERSION TIME	LINEARITY	OPERATING TEMP. RANGE (°C)
	ADC-EK8B	8 bits	1.8 msec	± ½ LSB	0 to +70
	ADC-EK10B	10 bits	6 msec	± ½ LSB	−25 to +85
	ADC-EK12B	12 bits	24 msec	± ½ LSB	−25 to +85
	ADC-ET8BC	8 bits	1.8 msec	± ½ LSB	0 to +70
	ADC-ET8BM	8 bits	1.8 msec	± ½ LSB	−55 to +125
	ADC-ET10BC	10 bits	6 msec	± ½ LSB	0 to +70
	ADC-ET10BM	10 bits	6 msec	± ½ LSB	−55 to +125
	ADC-ET12BC	12 bits	24 msec	± ½ LSB	0 to +70
	ADC-ET12BR	12 bits	24 msec	± ½ LSB	−25 to +85
	ADC-ET12BM	12 bits	24 msec	± ½ LSB	−55 to +125
	ADC-HC12BMC	12 bits	300 µsec	± ½ LSB	0 to +70
	ADC-HC12BMR	12 bits	300 µsec	± ½ LSB	−25 to +85
	ADC-HS12BMC	12 bits	9 µsec	± ½ LSB	0 to +70
	ADC-HS12BMR	12 bits	9 µsec	± ½ LSB	−25 to +85
	ADC-HU3BMC	3 bits	20 nsec	0.1% of FSR	0 to +70
	ADC-HU3BMR	3 bits	20 nsec	0.1% of FSR	−25 to +85
	ADC-HU3BMM	3 bits	20 nsec	0.1% of FSR	−55 to +125
	ADC-HX12BGC	12 bits	20 µsec	± ½ LSB	0 to +70
	ADC-HX12BMC	12 bits	20 µsec	± ½ LSB	0 to +70
	ADC-HX12BMR	12 bits	20 µsec	± ½ LSB	−25 to +85
	ADC-HZ12BGC	12 bits	8 µsec	± ½ LSB	0 to +70
	ADC-HZ12BMC	12 bits	8 µsec	± ½ LSB	0 to +70
	ADC-HZ12BMR	12 bits	8 µsec	± ½ LSB	−25 to +85
	ADC-MC8BC	8 bits	500 µsec	± ½ LSB	0 to +70
	ADC-MC8BM	8 bits	500 µsec	± ½ LSB	−55 to +125
NEW	ADC-84-10	10 bits	6 µsec	± ½ LSB	0 to +70
NEW	ADC-84-12	12 bits	10 µsec	± ½ LSB	0 to +70
NEW	ADC-85C-10	10 bits	6 µsec	± ½ LSB	0 to +70
NEW	ADC-85C-12	12 bits	10 µsec	± ½ LSB	0 to +70
NEW	ADC-85-10	10 bits	6 µsec	± ½ LSB	−25 to +85
NEW	ADC-85-12	12 bits	10 µsec	± ½ LSB	−25 to +85
	ADC-815MC	8 bits	700 nsec	± ½ LSB	0 to +70
	ADC-815MR	8 bits	700 nsec	± ½ LSB	−25 to +85
	ADC-816MC	10 bits	800 nsec	± ½ LSB	0 to +70
	ADC-816MR	10 bits	800 nsec	± ½ LSB	−25 to +85
	ADC-817MC	12 bits	2 µsec	± ½ LSB	0 to +70
	ADC-817MR	12 bits	2 µsec	± ½ LSB	−25 to +85
	ADC-825MC	8 bits	1 µsec	± ½ LSB	0 to +70
	ADC-825MR	8 bits	1 µsec	± ½ LSB	−25 to +85
	ADC-826MC	10 bits	1.4 µsec	± ½ LSB	0 to +70

DIGITAL-TO-ANALOG CONVERTERS

	MODEL NO.	RESOLUTION	OUTPUT SETTLING TIME	LINEARITY	OPERATING TEMP. RANGE (°C)
	DAC-HA10BM	10 bits	1.3 μsec	± ½ LSB	– 55 to + 125
	DAC-HA10BM-QL	10 bits	1.3 μsec	± ½ LSB	– 55 to + 125
	DAC-HA12BM	12 bits	5 μsec	± ½ LSB	– 55 to + 125
	DAC-HA12BM-QL	12 bits	5 μsec	± ½ LSB	– 55 to + 125
	DAC-HA14BM	14 bits	7 μsec	± 1 LSB	– 55 to + 125
	DAC-HA14BM-QL	14 bits	7 μsec	± 1 LSB	– 55 to + 125
	DAC-HF8BMM	8 bits	25 nsec	± ½ LSB	– 55 to + 125
	DAC-HF8BMM-QL	8 bits	25 nsec	± ½ LSB	– 55 to + 125
	DAC-HF10BMM	10 bits	25 nsec	± ½ LSB	– 55 to + 125
	DAC-HF10BMM-QL	10 bits	25 nsec	± ½ LSB	– 55 to + 125
	DAC-HF12BMM	12 bits	50 nsec	± ½ LSB	– 55 to + 125
	DAC-HF12BMM-QL	12 bits	50 nsec	± ½ LSB	– 55 to + 125
	DAC-HK12BMM	12 bits	3 μsec	± ½ LSB	– 55 to + 125
	DAC-HK12BMM-QL	12 bits	3 μsec	± ½ LSB	– 55 to + 125
	DAC-HP16BMM	16 bits	15 μsec	± 2 LSB	– 55 to + 125
	DAC-HP16BMM-QL	16 bits	15 μsec	± 2 LSB	– 55 to + 125
	DAC-HZ12BMM	12 bits	3 μsec	± ½ LSB	– 55 to + 125
	DAC-HZ12BMM-QL	12 bits	3 μsec	± ½ LSB	– 55 to + 125
NEW	DAC-87-CBI-I	12 bits	300 nsec	± ½ LSB	– 55 to + 125
NEW	DAC-87-CBI-I-QL	12 bits	300 nsec	± ½ LSB	– 55 to + 125
NEW	DAC-87-CBI-V	12 bits	3 μsec	± ½ LSB	– 55 to + 125
NEW	DAC-87-CBI-V-QL	12 bits	3 μsec	± ½ LSB	– 55 to + 125

SAMPLE-HOLD AMPLIFIERS

MODEL NO.	ACCURACY	ACQUISITION TIME	HOLD MODE DROOP	OPERATING TEMP. RANGE (°C)
SHM-6MM	0.01%	1 μsec	10μV/μsec	– 55 to + 125
SHM-6MM-QL	0.01%	1 μsec	10μV/μsec	– 55 to + 125
SHM-HUMM	0.1%	25 nsec	50μV/μsec	– 55 to + 125
SHM-HUMM-QL	0.1%	25 nsec	50μV/μsec	– 55 to + 125

OPERATIONAL AMPLIFIERS

MODEL NO.	INPUT OFFSET VOLTAGE	GAIN BANDWIDTH	OUTPUT	OPERATING TEMP. RANGE (°C)
AM-500MM	3 mV	130 MHz	± 10V @ 50 mA	– 55 to + 125
AM-500MM-QL	3 mV	130 MHz	± 10V @ 50 mA	– 55 to + 125

DIGITALLY PROGRAMMABLE INSTRUMENTATION AMPLIFIERS

	MODEL NO.	GAIN RANGE	SETTLING TIME	OUTPUT	OPERATING TEMP. RANGE (°C)
NEW	AM-542MM	1 to 1024	150 μsec	± 10.5V @ 5 mA	– 55 to + 125
NEW	AM-542MM-QL	1 to 1024	150 μsec	± 10.5V @ 5 mA	– 55 to + 125

DATA ACQUISITION SUBSYSTEMS

MODEL NO.	RESOLUTION	INPUT CHANNELS	THROUGHPUT RATE	OPERATING TEMP. RANGE (°C)
HDAS-8MM	12 bits	8 Differential	50 kHz	– 55 to + 125
HDAS-8MM-QL	12 bits	8 Differential	50 kHz	– 55 to + 125
HDAS-16MM	12 bits	16 Single-Ended	50 kHz	– 55 to + 125
HDAS-16MM-QL	12 bits	16 Single-Ended	50 kHz	– 55 to + 125

ANALOG TO DIGITAL CONVERTERS

	MODEL NO.	RESOLUTION	CONVERSION TIME	LINEARITY	OPERATING TEMP. RANGE (°C)
	ADC-826MR	10 bits	1.4 μsec	± ½ LSB	– 25 to + 85
	ADC-827MC	12 bits	3 μsec	± ½ LSB	0 to + 70
	ADC-827MR	12 bits	3 μsec	± ½ LSB	– 25 to + 85
NEW	ADC-830C	8 bits	100 μsec	± ½ LSB	0 to + 70
NEW	ADC-833R	6 bits	66 nsec	± ½ LSB	– 25 to + 85
	ADC-856C	10 bits	1μsec/LSB	± ½ LSB	0 to + 70
	ADC-856M	10 bits	1μsec/LSB	± ½ LSB	– 55 to + 125
NEW	ADC-5101	8 bits	900 nsec	± ½ LSB	0 to + 70
NEW	ADC-5101E	8 bits	900 nsec	± ½ LSB	– 25 to + 85
NEW	ADC-5210	12 bits	13 μsec	± ½ LSB	0 to + 70
NEW	ADC-5210E	12 bits	13 μsec	± ½ LSB	– 25 to + 85
NEW	ADC-5211	12 bits	13 μsec	± ½ LSB	0 to + 70
NEW	ADC-5211E	12 bits	13 μsec	± ½ LSB	– 25 to + 85
NEW	ADC-5212	12 bits	13 μsec	± ½ LSB	0 to + 70
NEW	ADC-5212E	12 bits	13 μsec	± ½ LSB	– 25 to + 85
NEW	ADC-5213	12 bits	13 μsec	± ½ LSB	0 to + 70
NEW	ADC-5213E	12 bits	13 μsec	± ½ LSB	– 25 to + 85
NEW	ADC-5214	12 bits	13 μsec	± ½ LSB	0 to + 70
NEW	ADC-5214E	12 bits	13 μsec	± ½ LSB	– 25 to + 85
NEW	ADC-5215	12 bits	13 μsec	± ½ LSB	0 to + 70
NEW	ADC-5215E	12 bits	13 μsec	± ½ LSB	– 25 to + 85
NEW	ADC-5216	12 bits	13 μsec	± ½ LSB	0 to + 70
NEW	ADC-5216E	12 bits	13 μsec	± ½ LSB	– 25 to + 85

DIGITAL TO ANALOG CONVERTERS

	MODEL NO.	RESOLUTION	OUTPUT SETTLING TIME	LINEARITY	OPERATING TEMP. RANGE (°C)
	DAC-HA10BC	10 bits	1.3 μsec	± ½ LSB	0 to + 70
	DAC-HA10BR	10 bits	1.3 μsec	± ½ LSB	– 25 to + 85
	DAC-HA12BC	12 bits	5 μsec	± ½ LSB	0 to + 70
	DAC-HA12BR	12 bits	5 μsec	± ½ LSB	– 25 to + 85
	DAC-HA14BC	14 bits	7 μsec	± ½ LSB	0 to + 70
	DAC-HA14BR	14 bits	7 μsec	± ½ LSB	– 25 to + 85
	DAC-HF8BMC	8 bits	25 nsec	± ½ LSB	0 to + 70
	DAC-HF8BMR	8 bits	25 nsec	± ½ LSB	– 25 to + 85
	DAC-HF10BMC	10 bits	25 nsec	± ½ LSB	0 to + 70
	DAC-HF10BMR	10 bits	25 nsec	± ½ LSB	– 25 to + 85
	DAC-HF12BMC	12 bits	50 nsec	± ½ LSB	0 to + 70
	DAC-HF12BMR	12 bits	50 nsec	± ½ LSB	– 25 to + 85
	DAC-HK12BGC	12 bits	3 μsec	± ½ LSB	0 to + 70
	DAC-HK12BMC	12 bits	3 μsec	± ½ LSB	0 to + 70
	DAC-HK12BMR	12 bits	3 μsec	± ½ LSB	– 25 to + 85
	DAC-HP16BGC	16 bits	15 μsec	± ½ LSB	0 to + 70
	DAC-HP16BMC	16 bits	15 μsec	± ½ LSB	0 to + 70
	DAC-HP16BMR	16 bits	15 μsec	± ½ LSB	– 25 to + 85
	DAC-HZ12BGC	12 bits	3 μsec	± ½ LSB	0 to + 70
	DAC-HZ12BMC	12 bits	3 μsec	± ½ LSB	0 to + 70
	DAC-HZ12BMR	12 bits	3 μsec	± ½ LSB	– 25 to + 85
	DAC-IC8BC	8 bits	300 nsec	± ½ LSB	0 to + 70
	DAC-IC8BM	8 bits	300 nsec	± ½ LSB	– 55 to + 125
	DAC-IC10BC	10 bits	250 nsec	± 1 LSB	0 to + 70
	DAC-IC10B	10 bits	250 nsec	± ½ LSB	0 to + 70
	DAC-IC10BM	10 bits	250 nsec	± ½ LSB	– 55 to + 125
	DAC-UP8BC	8 bits	2 μsec	± ½ LSB	0 to + 70
	DAC-UP8BM	8 bits	2 μsec	± ½ LSB	– 55 to + 125
NEW	DAC-UP10BC	10 bits	5 μsec	± ½ LSB	0 to + 70
	DAC-08BC	8 bits	2 μsec	± ½ LSB	0 to + 70
	DAC-08BM	8 bits	2 μsec	± ½ LSB	– 55 to + 125
NEW	DAC-85C-CBI-I	12 bits	300 nsec	± ½ LSB	0 to + 70
NEW	DAC-85C-CBI-V	12 bits	3 μsec	± ½ LSB	0 to + 70
NEW	DAC-85-CBI-I	12 bits	300 nsec	± ½ LSB	– 25 to + 85
NEW	DAC-85-CBI-V	12 bits	3 μsec	± ½ LSB	– 25 to + 85
NEW	DAC-562C	12 bits	400 nsec	± ½ LSB	0 to + 70
NEW	DAC-562M	12 bits	400 nsec	± ½ LSB	– 55 to + 125
NEW	DAC-608	8 bits	1 μsec	± ½ LSB	0 to + 70
NEW	DAC-610	10 bits	500 nsec	± ½ LSB	0 to + 70
NEW	DAC-612	12 bits	1 μsec	± ½ LSB	– 25 to + 85

SAMPLE-HOLD AMPLIFIERS

	MODEL NO.	ACCURACY	ACQUISITION TIME	HOLD-MODE DROOP	OPERATING TEMP. RANGE (°C)
	SHM-IC-1	0.01%	5 μsec	50μV/msec	0 to +70
	SHM-IC-1M	0.01%	5 μsec	50μV/msec	−55 to +125
	SHM-LM-2	0.01%	6 μsec	200μV/msec	0 to +70
	SHM-LM-2M	0.01%	6 μsec	100μV/msec	−55 to +125
	SHM-HUMC	0.1%	25 nsec	50μV/μsec	0 to +70
	SHM-HUMR	0.1%	25 nsec	50μV/μsec	−25 to +85
	SHM-6MC	0.01%	1 μsec	10μV/μsec	0 to +70
	SHM-6MR	0.01%	1 μsec	10μV/μsec	−25 to +85
NEW	SHM-7MC	0.1%	40 nsec	100mV/msec	0 to +70
NEW	SHM-7MR	0.1%	40 nsec	100mV/msec	−25 to +85

ANALOG MULTIPLEXERS

MODEL NO.	INPUT CHANNELS	ACCESS TIME	CHANNEL ON RESISTANCE	OPERATING TEMP. RANGE (°C)
MV-808	8 Single-Ended	350 nsec	250Ω	0 to +70
MV-808M	8 Single-Ended	350 nsec	250Ω	−55 to +125
MV-1606	16 Single-Ended	300 nsec	270Ω	0 to +70
MV-1606M	16 Single-Ended	300 nsec	270Ω	−55 to +125
MVD-409	4 Differential	350 nsec	250Ω	0 to +70
MVD-409M	4 Differential	350 nsec	250Ω	−55 to +125
MVD-807	8 Differential	300 nsec	270Ω	0 to +70
MVD-807M	8 Differential	300 nsec	270Ω	−55 to +125
MX-808	8 Single-Ended	500 nsec	1.5 kΩ	0 to +70
MX-808M	8 Single-Ended	500 nsec	1.5 kΩ	−55 to +125
MX-818C	8 Single Ended or 4 Differential	125 nsec	750Ω	0 to +70
MX-818M	8 Single-Ended or 4 Differential	125 nsec	750Ω	−55 to +125
MX-1606	16 Single-Ended	500 nsec	1.5 kΩ	0 to +70
MX-1606M	16 Single-Ended	500 nsec	1.5 kΩ	−55 to +125
MX-1616C	16 Single-Ended or 8 Differential	150 nsec	750Ω	0 to +70
MX-1616M	16 Single-Ended or 8 Differential	150 nsec	750Ω	−55 to +125
MXD-409	4 Differential	500 nsec	1.5 kΩ	0 to +70
MXD-409M	4 Differential	500 nsec	1.5 kΩ	−55 to +125
MXD-807	8 Differential	500 nsec	1.5 kΩ	0 to +70
MXD-807M	8 Differential	500 nsec	1.5 kΩ	−55 to +125

OPERATIONAL AMPLIFIERS

	MODEL NO.	INPUT OFFSET VOLTAGE	GAIN BANDWIDTH	OUTPUT	OPERATING TEMP. RANGE (°C)
	AM-410-2C	1.5 mV	18 MHz	±11V @ 8 mA	0 to +70
	AM-410-2M	1 mV	18 MHz	±12V @ 10 mA	−55 to +125
	AM-411-2C	1.5 mV	50 MHz	±11V @ 8 mA	0 to +70
	AM-411-2M	1 mV	60 MHz	±12V @ 10 mA	−55 to +125
NEW	AM-427-A	100 μV	5 MHz	± 11.5V @ 5.75 mA	−25 to +85
NEW	AM-427-B	25 μV	5 MHz	±12V @ 6 mA	−25 to +85
NEW	AM-427-M	100 μV	5 MHz	±11.5V @ 5.75 mA	−55 to +125
	AM-430A	75 μV	2.5 MHz	±10V @ 25 mA	0 to +70
	AM-430B	25 μV	2.5 MHz	±10V @ 25 mA	0 to +70
	AM-430M	75 μV	2.5 MHz	±10V @ 25 mA	−55 to +125
	AM-450-2	8 mV	12 MHz	±10V @ 10 mA	0 to +70
	AM-450-2M	8 mV	12 MHz	±10V @ 10 mA	−55 to +125
	AM-452-2	5 mV	20 MHz	±10V @ 10 mA	0 to +70
	AM-452-2M	5 mV	20 MHz	±10V @ 10 mA	−55 to +125
	AM-453-2	4 mV	10 MHz	±12V @ 20 mA	0 to +70
	AM-453-2M	4 mV	10 MHz	±12V @ 20 mA	−55 to +125
	AM-460-2	5 mV	12 MHz	±10V @ 10 mA	0 to +70
	AM-460-2M	5 mV	12 MHz	±10V @ 10 mA	−55 to +125
	AM-462-2	3 mV	100 MHz	±10V @ 10 mA	0 to +70
	AM-462-2M	3 mV	100 MHz	±10V @ 10 mA	−55 to +125
	AM-464-2	6 mV	4 MHz	±35V @ 10 mA	0 to +70

DATEL-INTERSIL, INC., 11 CABOT BOULEVARD, MANSFIELD, MA 02048/TEL. (617) 339-9341/TWX 710-346-1953/TLX 951340

OPERATIONAL AMPLIFIERS

MODEL NO.	INPUT OFFSET VOLTAGE	GAIN BANDWIDTH	OUTPUT	OPERATING TEMP. RANGE (°C)
AM-464-2M	4 mV	4 MHz	±35V @ 12 mA	−55 to +125
AM-470-2C	5 mV	1 MHz	±12V @ 10 mA	0 to +70
AM-470-2M	3 mV	1 MHz	±12V @ 10 mA	−55 to +125
AM-490-2A	20 μV	3 MHz	±12V @ 10 mA	0 to +70
AM-490-2B	20 μV	3 MHz	±12V @ 10 mA	0 to +70
AM-490-2C	20 μV	3 MHz	±12V @ 10 mA	0 to +70
AM-490-2M	20 μV	3 MHz	±12V @ 10 mA	−55 to +125
AM-500GC	3 mV	130 MHz	±10V @ 50 mA	0 to +70
AM-500MC	3 mV	130 MHz	±10V @ 50 mA	0 to +70
AM-500MR	3 mV	130 MHz	±10V @ 50 mA	−25 to +85

DIGITALLY PROGRAMMABLE INSTRUMENTATION AMPLIFIERS

MODEL NO.	GAIN RANGE	SETTLING TIME	OUTPUT	OPERATING TEMP. RANGE (°C)
AM-542MC	1 to 1024	150 μsec	±10.5V @ 5 mA	0 to +70
AM-542MR	1 to 1024	150 μsec	±10.5V @ 5 mA	−25 to +85
AM-543MC	1 to 128	6 μsec	±11V @ 1 mA	0 to +70
AM-543MR	1 to 128	6 μsec	±11V @ 1 mA	−25 to +85

DATA ACQUISITION SUBSYSTEMS

MODEL NO.	RESOLUTION	INPUT CHANNELS	THROUGHPUT RATE	OPERATING TEMP. RANGE (°C)
DAS-952R	8 bits	16 Single-Ended	17 kHz	−25 to +85
HDAS-8MC	12 bits	8 Differential	50 kHz	0 to +70
HDAS-8MR	12 bits	8 Differential	50 kHz	−25 to +85
HDAS-16MC	12 bits	16 Differential	50 kHz	0 to +70
HDAS-16MR	12 bits	16 Differential	50 kHz	−25 to +85

VOLTAGE TO FREQUENCY CONVERTERS

MODEL NO.	LINEARITY	OUTPUT RANGE	GAIN TEMPCO	OPERATING TEMP. RANGE (°C)
VFQ-1C	0.05%	10 kHz to 100 kHz	40 ppm/°C	0 to +70
VFQ-1R	0.05%	10 kHz to 100 kHz	40 ppm/°C	−25 to +85
VFQ-2C	0.01%	10 kHz to 100 kHz	40 ppm/°C	0 to +70
VFQ-3C	0.25%	10 kHz to 100 kHz	40 ppm/°C	0 to +70

ACTIVE FILTERS

	MODEL NO.	FREQUENCY RANGE	Fo ACCURACY	Q RANGE	OPERATING TEMP. RANGE (°C)
	FLT-U2	0.001 Hz to 200 kHz	±5%	0.1 to 1000	0 to +70
NEW	FLT-U2-M	0.001 Hz to 200 kHz	±5%	0.1 to 1000	−55 to +125

HARRIS

HI-200

Dual SPST CMOS Analog Switch

FEATURES

- ANALOG VOLTAGE RANGE ±15V
- ANALOG CURRENT RANGE 80mA
- TURN-ON TIME 240ns
- LOW R_{ON} 55Ω
- LOW POWER DISSIPATION 15mW
- TTL/CMOS COMPATIBLE

APPLICATIONS

- HIGH FREQUENCY ANALOG SWITCHING
- SAMPLE AND HOLD CIRCUITS
- DIGITAL FILTERS
- OP AMP GAIN SWITCHING NETWORKS

DESCRIPTION

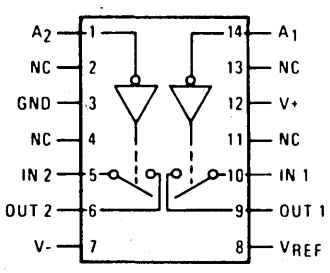
HI-200 is a monolithic device comprising two independently selectable SPST switches which feature fast switching speeds (290ns) combined with low power dissipation (15mW at 25°C). Each switch provides low "ON" resistance operation for input signal voltages up to the supply rails and for signal currents up to 80mA. Employing Dielectric Isolation and CMOS processing, HI-200 operates without any applications problems induced by latch-up or SCR mode phenomena.

All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. HI-200 is an ideal component for use in high frequency analog switching. Typical applications include signal path switching, sample and hold circuit, digital filters,and op amp gain switching networks.

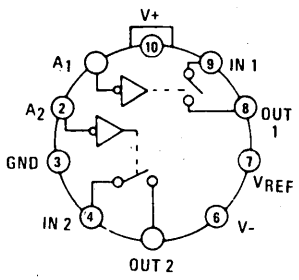
HI-200 is available in DIP and metal (TO-100) cans. HI-200-2 is specified from -55°C to +125°C while HI-200-5 operates from 0°C to +75°C. HI-200 is functionally and pin compatible with other available "200 series" switches.

PINOUT

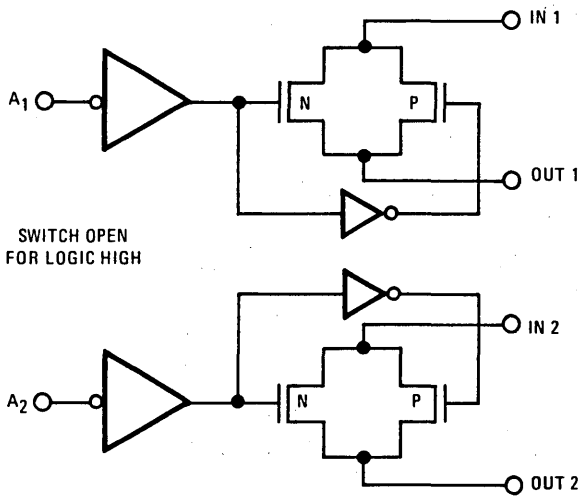
Section 11 for Packaging



Top View



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	44V (±22)	Total Power Dissipation*	450mW
V_{REF} to Ground	+20V, -5V	Operating Temperature	
Digital Input Voltage:	$+V_{Supply}$ +4V	HI-200-2	-55°C to +125°C
	$-V_{Supply}$ -4V	HI-200-4	-20°C to +85°C
Analog Input Voltage (One Switch)	$+V_{Supply}$ +2.0V	HI-200-5	0°C to +75°C
	$-V_{Supply}$ -2.0V	Storage Temperature	-65°C to +150°C

*Derate 6mW/°C Above T_A = 75°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified
Supplies = +15V, -15V; V_{REF} = Open; V_{AH}(Logic Level High) = 2.4V V_{AL}(Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characteristics

		HI-200-2 -55°C to +125°C			HI-200-5 ** 0°C to +75°C			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
ANALOG SWITCH CHARACTERISTICS								
V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
R_{ON}, On Resistance (Note 1)	+25°C		55	70		55	80	Ω
	Full		80	100		72	100	Ω
$I_{S(OFF)}$, Off Input Leakage Current	+25°C		1			1		nA
(Note 6)	Full		100	500		10	500	nA
$I_{D(OFF)}$, Off Output Leakage Current	+25°C		1			1		nA
(Note 6)	Full		100	500		10	500	nA
$I_{D(ON)}$, On Leakage Current (Note 6)	+25°C		.02			.02		nA
	Full		6	500		6	500	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			0.8			0.8	V
V_{AH}, Input High Threshold	Full	2.4			2.4			V
I_A, Input Leakage Current (High or Low) (Note 2)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
t_{OPEN}, Break - Before Make Delay (Note 3)	+25°C		60			60		ns
t_{on}, Switch on Time	+25°C		240	500		240		ns
t_{off}, Switch off Time	+25°C		330	500		500		ns
"Off Isolation" (Note 4)	+25°C		70			70		dB
$C_{S(OFF)}$, Input Switch Capacitance	+25°C		5.5			5.5		pF
$C_{D(OFF)}$, Output Switch Capacitance	+25°C		5.5			5.5		pF
$C_{D(ON)}$, Output Switch Capacitance	+25°C		11			11		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(OFF)}$, Drain-To-Source Capacitance	+25°C		0.5			0.5		pF
POWER REQUIREMENTS (Note 5)	+25°C		15			15		mW
P_D, Power Dissipation	Full			60			60	mW
I^+, Current	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA
I^-, Current	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA

NOTES:
1. V_{OUT} = ±10V I_{OUT} = 1mA
2. Digital Inputs Are MOS Gates - Typical Leakage is Less Than 1nA
3. V_{AH} = 4.0V
4. V_A = +5V, R_L = 1KΩ, C_L = 10pF, V_S = 3VRMS, f = 100kHz
5. V_A = +3V or V_A = OV For Both Switches
6. Refer to leakage current measurement diagram on page (3-8)

** Note: HI-200-4 has same specifications as HI-200-5 over the temperature range -20°C to +85°C.

HARRIS

HI-201

Quad SPST CMOS Analog Switch

FEATURES

- ANALOG VOLTAGE RANGE ±15V
- ANALOG CURRENT RANGE 80mA
- TURN-ON TIME 185ns
- LOW R_{ON} 55 Ω
- LOW POWER DISSIPATION 15mW
- TTL/CMOS COMPATIBLE

APPLICATIONS

- HIGH FREQUENCY ANALOG SWITCHING
- SAMPLE AND HOLD CIRCUITS
- DIGITAL FILTERS
- OP AMP GAIN SWITCHING NETWORKS

DESCRIPTION

HI-201 is a monolithic device comprising four independently selectable SPST switches which feature fast switching speeds (185ns) combined with low power dissipation (15mW at 25°C). Each switch provides low "ON" resistance operation for input signal voltages up to the supply rails and for signal currents up to 80mA. Employing Dielectric Isolation and CMOS processing, HI-201 operates without any applications problems induced by latch-up or SCR-mode phenomena.

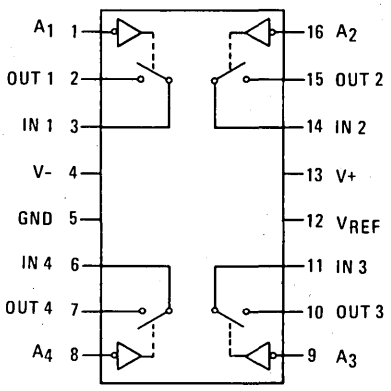
All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. HI-201 is an ideal component for use in high frequency analog switching. Typical applications include signal path switching, sample and hold circuit, digital filters, and op amp gain switching networks.

HI-201 is available in a 16 lead dual-in-line package. HI-201-2 is specified from -55°C to +125°C while HI-201-5 operates from 0°C to +75°C. HI-201 is functionally and pin compatible with other available "200 series" switches.

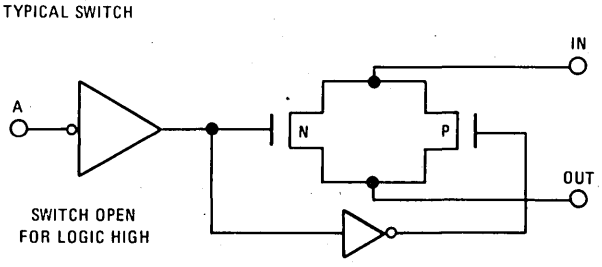
PIN OUT

Section 11 for Packaging

Top View



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 4 and 13	44V (±22)	Total Power Dissipation*	750mW
V_{REF} to Ground	+20V, -5V	Operating Temperature	
Digital Input Voltage:	V_{Supply}(+) +4V	HI-201-2	-55°C to +125°C
	V_{Supply}(-) -4V	HI-201-4	-20°C to +85°C
Analog Input Voltage (One Switch)	$+V_{Supply}$ +2.0V	HI-201-5	0°C to +75°C
	$-V_{Supply}$ -2.0V	Storage Temperature	-65°C to +150°C

*Derate 8mW/°C Above T_A = +75°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified
Supplies = +15V, -15V; V_{REF} = Open; V_{AH} (Logic Level High) = 2.4V V_{AL} (Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characteristics

		HI-201-2 -55°C to +125°C			HI-201-5 ** 0°C to +75°C			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
ANALOG SWITCH CHARACTERISTICS								
V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
R_{ON}, On Resistance (Note 1)	+25°C		55	70		55	80	Ω
	Full		80	100		75	100	Ω
$I_{S(OFF)}$, Off Input Leakage Current	+25°C		2			2		nA
(Note 6)	Full			500			250	nA
$I_{D(OFF)}$, Off Output Leakage Current	+25°C		2			2		nA
(Note 6)	Full			500			250	nA
$I_{D(ON)}$, On Leakage Current (Note 6)	+25°C		2			2		nA
	Full			500			250	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			0.8			0.8	V
V_{AH}, Input High Threshold	Full	2.4			2.4			V
I_A, Input Leakage Current (High or Low) (Note 2)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
t_{OPEN}, Break - Before Make Delay (Note 3)	+25°C		30			30		ns
t_{on}, Switch ON Time	+25°C		185	500		185		ns
t_{off}, Switch OFF Time	+25°C		220	500		220		ns
"Off Isolation" (Note 4)	+25°C		80			80		dB
$C_{S(OFF)}$, Input Switch Capacitance	+25°C		5.5			5.5		pF
$C_{D(OFF)}$, Output Switch Capacitance	+25°C		5.5			5.5		pF
$C_{D(ON)}$, Output Switch Capacitance	+25°C		11			11		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(OFF)}$, Drain-To-Source Capacitance	+25°C		0.5			0.5		pF
POWER REQUIREMENTS (Note 5)	+25°C		15			15		mW
P_D, Power Dissipation	Full			60			60	mW
I+, Current (Pin 13)	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA
I- Current (Pin 4)	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA

NOTES:
1. V_{OUT} = ±10V I_{OUT} = 1mA
2. Digital Inputs Are MOS Gates - Typical Leakage is Less Than 1nA
3. V_{AH} = 4.0V
4. V_A = 5V, R_L = 1KΩ, C_L = 10pF, V_S = 3VRMS, f = 100KHz
5. V_A = +3V or V_A = 0V For all Switches
6. Refer to leakage current measurement diagram on page (3-14)

** Note: HI-201-4 has same specifications as HI-201-5 over the temperature range -20°C to +85°C.

HARRIS

HI-201HS

High Speed Quad SPST CMOS Analog Switch

Preliminary

FEATURES

- ANALOG VOLTAGE RANGE ±15V
- ANALOG CURRENT RANGE 80mA
- TURN-ON TIME 30ns
- LOW R_{ON} 30Ω
- LOW POWER DISSIPATION 120mW
- TTL COMPATIBLE
- LOW CHARGE INJECTION 10pC

APPLICATIONS

- HIGH FREQUENCY ANALOG SWITCHING
- SAMPLE AND HOLD CIRCUITS
- DIGITAL FILTERS
- OP AMP GAIN SWITCHING NETWORKS

DESCRIPTION

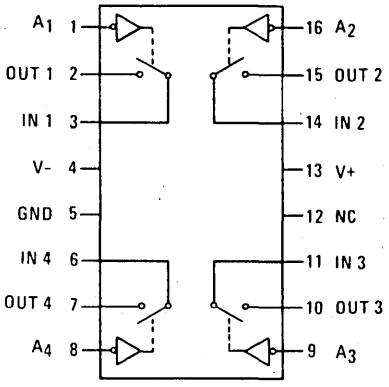
The Harris HI-201HS is a monolithic CMOS analog switch featuring very fast switching speeds and low ON resistance. The device consists of four independently selectable SPST switches and is identical in pinout to the HI-201 quad switch.

Fabricated using the Harris dielectric isolation technology, this TTL compatible device offers improved performance over previously available CMOS analog switches. Featuring switching speeds of 50ns max., low ON resistance of 50Ω max., and wide analog signal range of ±15V, the HI-201HS is designed for any application where improved switching performance, particularly switching speed, is required.

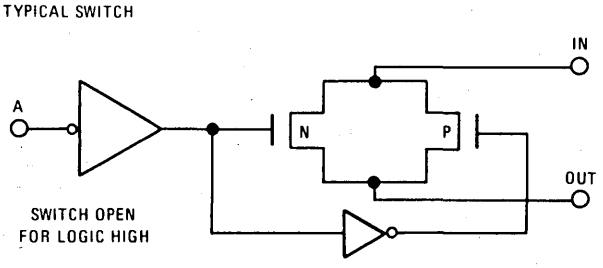
The HI-201HS is available in a 16 lead dual-in-line package. The HI-201HS-2 is specified for the temperature range of -55°C to +125°C and the HI-201HS-5 operates from 0°C to +75°C.

PIN OUT

Top View



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage Between Pins 4 and 13	+36V	Total Power Dissipation*	750mW
		Operating Temperature	
Digital Input Voltage:	V_{Supply}(+) +4V	HI-201HS-2	-55°C to +125°C
	V_{Supply}(-) -4V	HI-201HS-4	-20°C to +85°C
Analog Input Voltage (One Switch)	$+V_{Supply}$ +2.0V	HI-201HS-5	0°C to +75°C
	$-V_{Supply}$ -2.0V	Storage Temperature	-65°C to +150°C

*Derate 8mW/°C Above T_A = +75°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified, Supplies = +15V, -15V; V_{AH} (Logic Level High) = 5.0V; V_{AL} (Logic Level Low) = +0.8V

PARAMETER	TEMP.	HI-201HS-2 HI-201HS-5 MIN.	TYP.	MAX.	UNITS
ANALOG SWITCH CHARACTERISTICS					
V_S, Analog Signal Range	Full	-15		+15	V
R_{ON}, On Resistance (Note 2)	+25°C		30	50	Ω
	Full			75	Ω
$I_{S(OFF)}$, Off Input Leakage Current	+25°C		.3	10	nA
	Full			100	nA
$I_{D(OFF)}$, Off Output Leakage Current	+25°C		.3	10	nA
	Full			100	nA
$I_{D(ON)}$, On Leakage Current	+25°C		.1	10	nA
	Full			100	nA
DIGITAL INPUT CHARACTERISTICS					
V_{AL}, Input Low Threshold	Full			0.8	V
V_{AH}, Input High Threshold	+25°C	2.0			V
	Full	2.4			V
I_{AL}, Input Leakage Current (Low)	Full			500	μA
I_{AH}, Input Leakage Current (High)	Full			40	μA
SWITCHING CHARACTERISTICS					
t_{ON}, Switch ON Time (Note 3)	+25°C		30	50	ns
t_{OFF}, Switch OFF Time (Note 3)	+25°C		40	50	ns
"Off Isolation" (Note 4)	+25°C		72		dB
Crosstalk (Note 5)	+25°C		86		dB
Charge Injection (Note 6)	+25°C		10		pC
$C_{S(OFF)}$, Input Switch Capacitance	+25°C		10		pF
$C_{D(OFF)}$, Output Switch Capacitance	+25°C		10		pF
$C_{D(ON)}$,	+25°C		30		pF
C_A, Digital Input Capacitance	+25°C		18		pF
$C_{DS(OFF)}$, Drain-to-Source Capacitance	+25°C		.5		pF
POWER REQUIREMENTS (Note 7)					
P_D, Power Dissipation	+25°C		120		mW
	Full			240	mW
I^+, Current (Pin 13)	+25°C		4.5		mA
	Full			10.0	mA
I^-, Current (Pin 4)	+25°C		3.5		mA
	Full			6	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. V_{OUT} = ±10V, I_{OUT} = 1mA
3. R_L = 1kΩ, C_L = 35pF, V_{IN} = +10V, V_A = +5V
4. V_A = 5V, R_L = 1KΩ, C_L = 10pF, V_S = 3 VRMS, f = 100kHz
5. V_A = 5V, R_L = 1kΩ, f = 100kHz, V_{IN} = $2V_{p-p}$
6. C_L = 1000pF, V_{IN} = 0V, R_{IN} = 0Ω $\Delta Q = C_L \times \Delta V_O$
7. V_A = 5V or V_A = 0 for all switches.

HARRIS

HI-300 thru HI-307

CMOS Analog Switches

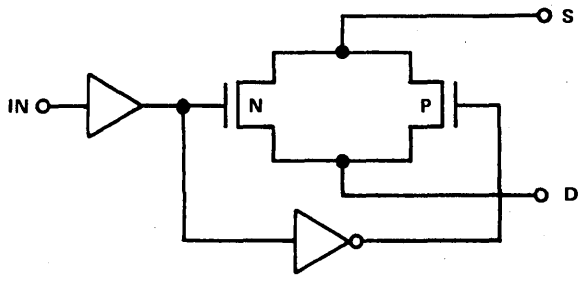
FEATURES

• ANALOG SIGNAL RANGE (±15V SUPPLIES)	±15V
• LOW LEAKAGE (TYP. @ 25°C)	40pA
• LOW LEAKAGE (TYP. @ 125°C)	1nA
• LOW ON RESISTANCE (TYP. @ 25°C)	35Ω
• BREAK-BEFORE-MAKE DELAY (TYP.)	60ns
• CHARGE INJECTION	30pC
• TTL, CMOS COMPATIBLE	
• SYMETRICAL SWITCH ELEMENTS	
• LOW OPERATING POWER (TYP. FOR HI-300 - 303)	1.0mW

APPLICATIONS

- SAMPLE AND HOLD i.e. LOW LEAKAGE SWITCHING
- OP AMP GAIN SWITCHING i.e. LOW ON RESISTANCE
- PORTABLE, BATTERY OPERATED CIRCUITS
- LOW LEVEL SWITCHING CIRCUITS
- DUAL OR SINGLE SUPPLY SYSTEMS

FUNCTIONAL DIAGRAM



TYPICAL SWITCH 300 SERIES

DESCRIPTION

The HI-300 through HI-307 series of switches are monolithic devices fabricated using CMOS technology and the Harris dielectric isolation process. These switches feature break-before-make switching, (HI-301, 303, 305 & 307 only) , low and nearly constant ON resistance over the full analog signal range, and low power dissipation, (a few milliwatts for the HI-300-303, a few hundred microwatts for the HI-304-307).

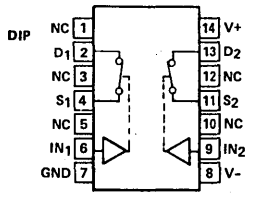
The HI-300-303 are TTL compatible and have a logic "0" condition with an input less than 0.8V and a logic "1" condition with an input greater than 4.0V. The HI-304-307 switches are CMOS compatible and have a low state with an input less than 3.5V and a high state with an input greater than 11V. (See pinouts for switch conditions with a logic "1"input.)

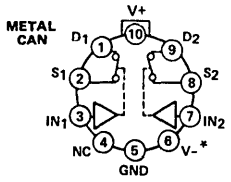
All the devices are available in a 14 pin epoxy or ceramic DIP. The HI-300, 301, 304 and 305 are also available in a 10 pin metal can. Each of the switch types are available in either the -55°C to +125°C or 0°C to +75°C operating ranges.

PINOUTS (SWITCH STATES ARE FOR A LOGIC "1" INPUT)

Section 11 for Packaging

DUAL SPST HI-300 & HI-304
(TOP VIEWS)

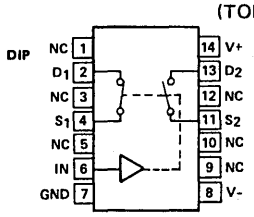


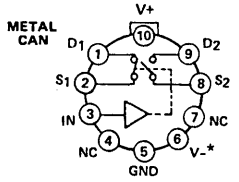


LOGIC	SWITCH
0	OFF
1	ON

*The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

SPDT HI-301 & HI-305
(TOP VIEWS)

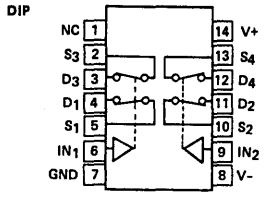




LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

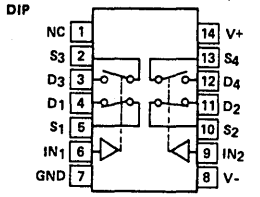
*The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

DUAL DPST HI-302 & HI-306
(TOP VIEW)



LOGIC	SWITCH
0	OFF
1	ON

DUAL SPDT HI-303 & HI-307
(TOP VIEW)



LOGIC	SW 1 SW 2	SW 3 SW 4
0	OFF	ON
1	ON	OFF

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between Supplies	44V (±22V)
Digital Input Voltage	V^+ +4.0V V^- -4.0V
Analog Input Voltage	V^+ 1.5V V^- 1.5V

Total Power Dissipation

14 Pin Epoxy DIP	526mW
14 Pin Ceramic DIP	588mW
10 Pin Metal Can*	435mW

*Derate 6.9mW/0°C Above T_A = 70°C

Operating Temperature	HI-3XX-2	-55°C to +125°C
	HI-3XX-5	0°C to +75°C
Storage Temperature		-65°C to +150°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified; Supplies = +15V, -15V; V_{IN} = Logic Input.
HI-300-303 : V_{IN} - for Logic "1" = 4V, for Logic "0" = 0.8V
HI-304-307 : V_{IN} - for Logic "1" = 11V, for Logic "0" = 3.5V

PARAMETER	TEMP	-55°C to +125°C MIN	-55°C to +125°C TYP	-55°C to +125°C MAX	0°C to +75°C MIN	0°C to +75°C TYP	0°C to +75°C MAX	UNITS
ANALOG SWITCH CHARACTERISTICS								
Analog Signal Range	Full	-15		+15	-15		+15	V
R_{ON} ON Resistance (Note 2)	+25°C		35	50		35	50	Ω
	Full		40	75		40	75	Ω
IS_{OFF} OFF Input Leakage Current (Note 3)	+25°C		0.04	1		0.04	5	nA
	Full		1	100		0.2	100	nA
ID_{OFF} OFF Output Leakage Current (Note 3)	+25°C		0.04	1		0.04	5	nA
	Full		1	100		0.2	100	nA
ID_{ON} ON Leakage Current (Note 4)	+25°C		0.03	1		0.03	5	nA
	Full		0.5	100		0.2	100	nA
DIGITAL INPUT CHARACTERISTICS								
V_{INL} Input Low Level *	Full			0.8			0.8	V
V_{INH} Input High Level *	Full	4			4			V
V_{INL} Input Low Level **	Full			3.5			3.5	V
V_{INH} Input High Level **	Full	11			11			V
I_{INL} Input Leakage Current (Low) (Note 5)	Full			1			1	μA
I_{INH} Input Leakage Current (High) (Note 5)	Full			1			1	μA
SWITCHING CHARACTERISTICS								
t_{OPEN} Break-Before-Make Delay ***	+25°C		60			60		ns
t_{ON} Switch On Time *	+25°C		210	300		210	300	ns
t_{OFF} Switch Off Time *	+25°C		160	250		160	250	ns
t_{ON} Switch On Time **	+25°C		160	250		160	250	ns
t_{OFF} Switch Off Time **	+25°C		100	150		100	150	ns
Off Isolation (Note 6)	+25°C		60			60		dB
Charge Injection (Note 7)	+25°C		3			3		mV
CS_{OFF} Input Switch Capacitance	+25°C		16			16		pF
CD_{OFF} Output Switch Capacitance	+25°C		14			14		pF
CD_{ON} Output Switch Capacitance	+25°C		35			35		pF
C_{IN} (High) Digital Input Capacitance	+25°C		5			5		pF
C_{IN} (Low) Digital Input Capacitance	+25°C		5			5		pF
POWER REQUIREMENTS								
I+ Current * (Note 8)	+25°C		0.09	0.5		0.09	0.5	mA
	Full			1			1	mA
I- Current * (Note 8)	+25°C		0.01	10		0.01	100	μA
	Full			100				μA
I+ Current * (Note 9)	+25°C		0.01	10		0.01	100	μA
	Full			100				μA
I- Current * (Note 9)	+25°C		0.01	10		0.01	100	μA
	Full			100				μA
I+ Current ** (Note 10)	+25°C		0.01	10		0.01	100	μA
	Full			100				μA
I- Current ** (Note 10)	+25°C		0.01	10		0.01	100	μA
	Full			100				μA
I+ Current ** (Note 11)	+25°C		0.01	10		0.01	100	μA
	Full			100				μA
I- Current ** (Note 11)	+25°C		0.01	10		0.01	100	μA
	Full			100				μA

* HI-300 thru HI-303 Only; ** HI-304 thru HI-307 Only; *** HI-301, HI-303, HI-305, HI-307 Only

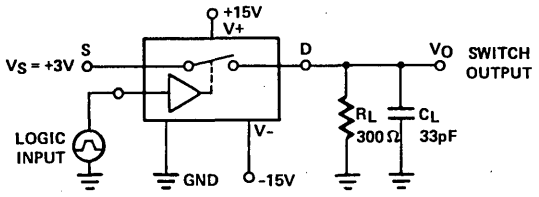
ELECTRICAL CHARACTERISTICS NOTES:

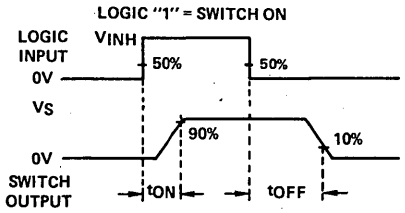
1. As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Characteristics" are the only conditions recommended for satisfactory operation.
2. $V_S = \pm 10V$, $I_{OUT} = -10mA$ On resistance derived from the voltage measured across the switch under the above conditions.
3. $V_S = \pm 14V, V_D = \mp 14V$.
4. $V_S = V_D = \pm 14V$.
5. The digital inputs are diode protected MOS gates and typical leakages of 1nA or less can be expected.
6. $V_S = 1V_{RMS}$, f = 500kHz, $C_L = 15pF$, $R_L = 1k$. $C_L = C_{FIXTURE} + C_{PROBE}$, "Off Isolation" = $20 \log V_S/V_D$.
7. $V_S = 0V$, $C_L = 10{,}000pF$, Logic Drive = 5V pulse. (HI-300 -303) Switches are symmetrical; S and D may be interchanged. Logic Drive = 15V (HI-304-307)
8. $V_{IN} = 4V$ (one input) (all other inputs = 0V)
9. $V_{IN} = 0.8V$ (all inputs).
10. $V_{IN} = 15V$ (all inputs).
11. $V_{IN} = 0V$ (all inputs).
12. To drive from DTL/TTL circuits, pull-up resistors to +5V supply are recommended.

TEST CIRCUITS

SWITCHING TEST CIRCUIT (t_{ON}, t_{OFF})

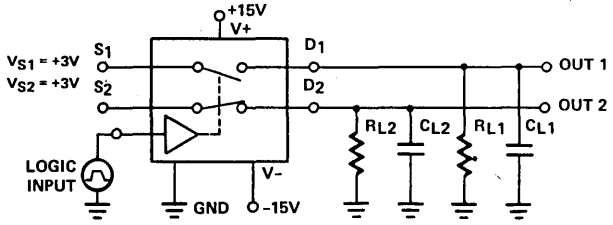
SWITCH TYPE	V_{INH}
HI-300 thru HI-303	4V
HI-304 thru HI-307	15V

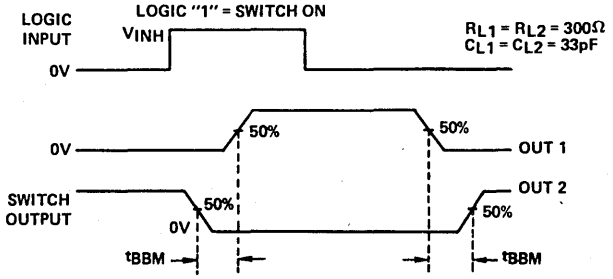




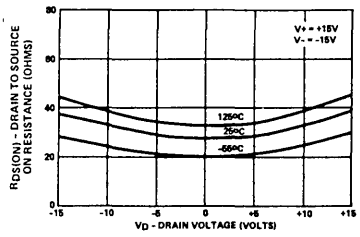
BREAK-BEFORE-MAKE TEST CIRCUIT (t_{BBM})

SWITCH TYPE	V_{INH}
HI-301, HI-303	5V
HI-305, HI-307	15V

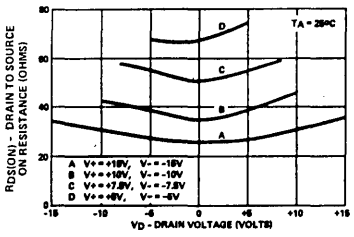




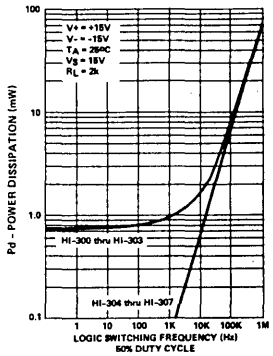
$R_{DS(ON)}$ VS. V_D AND TEMPERATURE



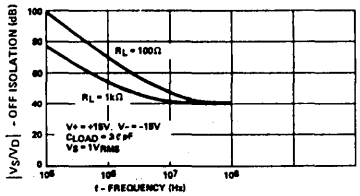
$R_{DS(ON)}$ VS. V_D AND POWER SUPPLY VOLTAGE



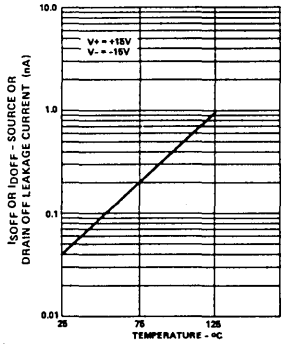
DEVICE POWER DISSIPATION VS. SWITCHING FREQUENCY SINGLE LOGIC INPUT



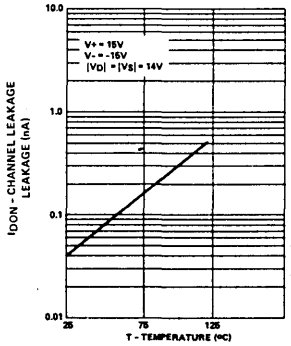
OFF ISOLATION VS. FREQUENCY



$I_{S(OFF)}$ OR $I_{D(OFF)}$ VS. TEMPERATURE *

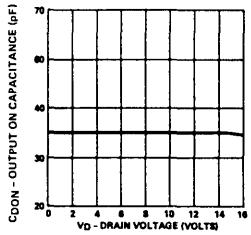


$I_{D(ON)}$ VS. TEMPERATURE *

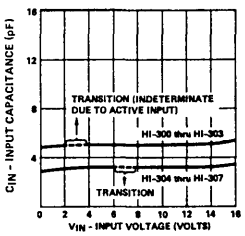


* The net leakage into the source or drain is the n-channel leakage minus the p-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

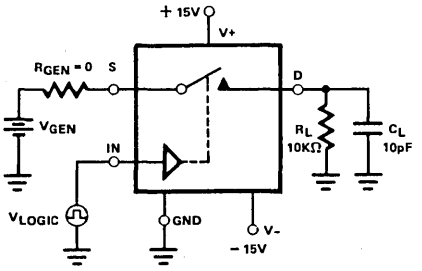
OUTPUT ON CAPACITANCE VS. DRAIN VOLTAGE



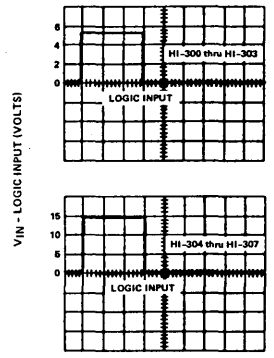
DIGITAL INPUT CAPACITANCE VS. INPUT VOLTAGE

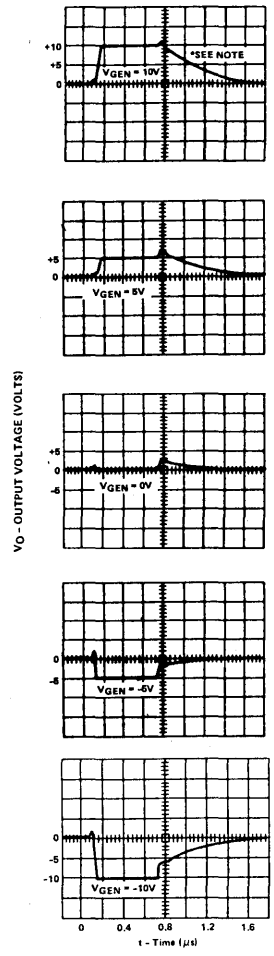


Typical delay, rise, fall, settling times, and switching transients in this circuit.



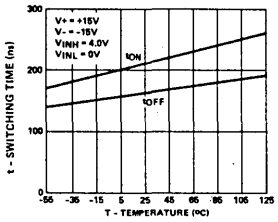
If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.



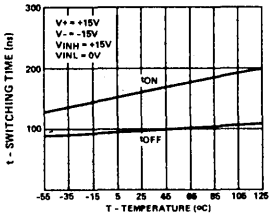


TYPICAL PERFORMANCE CURVES (Continued)

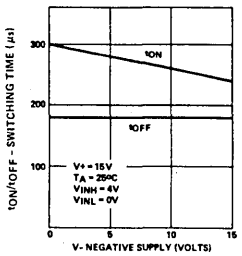
SWITCHING TIME VS. TEMPERATURE HI-300 thru HI-303



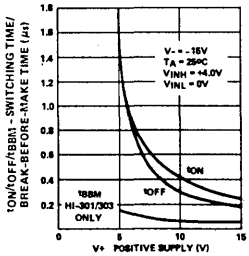
SWITCHING TIME VS. TEMPERATURE HI-304 thru HI-307



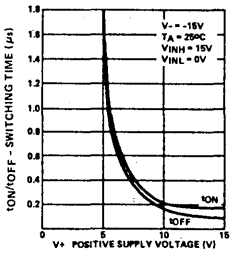
SWITCHING TIME VS. NEGATIVE SUPPLY VOLTAGE HI-300 thru HI-303



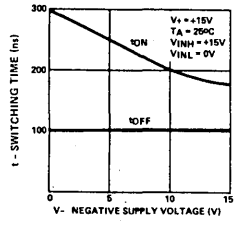
SWITCHING TIME AND BREAK BEFORE MAKE TIME VS. POSITIVE SUPPLY VOLTAGE HI-300 thru HI-303



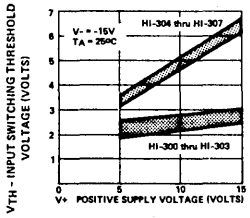
SWITCHING TIME VS. POSITIVE SUPPLY VOLTAGE HI-304 thru HI-307



SWITCHING TIME VS. NEGATIVE SUPPLY VOLTAGE HI-304 thru HI-307



INPUT SWITCHING THRESHOLD VS. POSITIVE SUPPLY VOLTAGE HI-300 thru HI-307



HARRIS

HI-381/384/ 387/390

CMOS Analog Switches

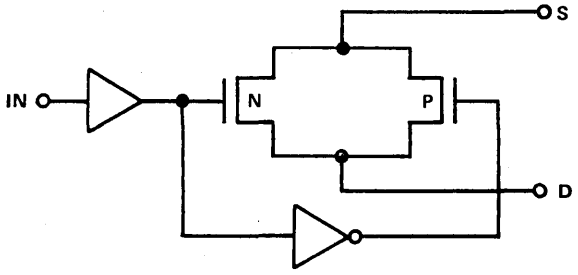
FEATURES

- ANALOG SIGNAL RANGE (±15V SUPPLIES) ±15V
- LOW LEAKAGE (TYP. @ 25°C) 40pA
- LOW LEAKAGE (TYP @ 125°C) 1nA
- LOW ON RESISTANCE (TYP. @ 25°C) 35Ω
- BREAK-BEFORE-MAKE DELAY (TYP.) 60ns
- CHARGE INJECTION 30pC
- TTL COMPATIBLE
- SYMMETRICAL SWITCH ELEMENTS
- LOW OPERATING POWER (TYP.) 1.0mW

APPLICATIONS

- SAMPLE AND HOLD i.e. LOW LEAKAGE SWITCHING
- OP AMP GAIN SWITCHING i.e. LOW ON RESISTANCE
- PORTABLE BATTERY OPERATED CIRCUITS
- LOW LEVEL SWITCHING CIRCUITS
- DUAL OR SINGLE SUPPLY SYSTEMS

FUNCTIONAL DIAGRAM



TYPICAL SWITCH - 300 SERIES

DESCRIPTION

The HI-381 through HI-390 series of switches are monolithic devices fabricated using CMOS technology and the Harris dielectric isolation process. These devices are TTL compatible and are available in four switching configurations. (See device pinout for particular switching function with a logic "1" input.)

These switches feature low leakage and supply currents, low and nearly constant ON resistance over the analog signal range, break-before-make switching and low power dissipation.

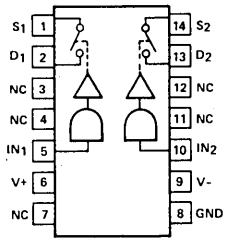
The HI-381 and HI-387 switches are available in a 14 pin epoxy or ceramic DIP or10 pin metal can. The HI-384 and HI-390 are available in a 16 pin epoxy or ceramic DIP. Each of the individual switch types are available in the -55°C to +125°C and 0°C to +75°C operating ranges.

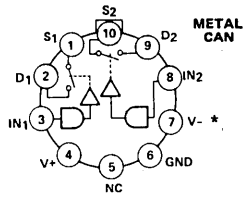
PINOUTS (SWITCH STATES ARE FOR A LOGIC "1" INPUT)

Section 11 for Packaging

DUAL SPST HI-381

(TOP VIEWS)



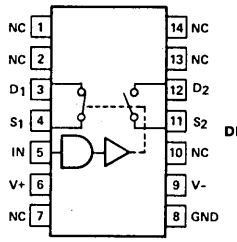


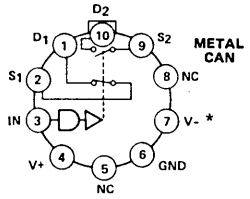
LOGIC	SW 1 SW 2
0	ON
1	OFF

*The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

SPDT HI-387

(TOP VIEWS)



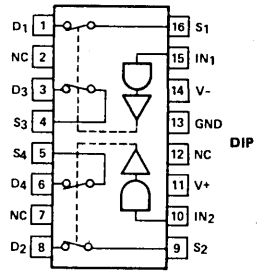


LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

*The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

DUAL DPST HI-384

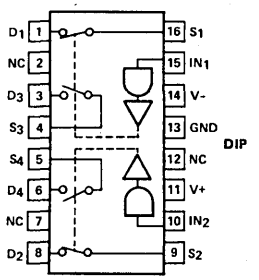
(TOP VIEW)



LOGIC	SW 1 - 4
0	OFF
1	ON

DUAL SPDT HI-390

(TOP VIEW)



LOGIC	SW 1 SW 2	SW 3 SW 4
0	OFF	ON
1	ON	OFF

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between Supplies 44V (±22)

Digital Input Voltage
V^+ +4.0V
V^- -4.0V

Analog Input Voltage
V^+ +1.5V
V^- -1.5V

Storage Temperature Range -65°C to +150°C

Total Power Dissipation

14 Pin Epoxy DIP	526mW
14 Pin Ceramic DIP	588mW
16 Pin Epoxy DIP	625mW
16 Pin Ceramic DIP	685mW
10 Pin Metal Can*	435mW

*Derate 6.9mW/°C above T_A = 70°C

Operating Temperature

HI-3XX-2	-55°C to +125°C
HI-3XX-5	0°C to +75°C

ELECTRICAL CHARACTERISITICS

Unless otherwise specified; Supplies = +15V, -15V; VIN = Logic Input, VIN for logic "1" = 4V, for logic 0 = .8V

		-55°C to +125°C			0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
ANALOG SWITCH CHARACTERISTICS								
Analog Signal Range	FULL	-15		+15	-15		+15	V
R_{ON} ON Resistance (Note 2)	+25°C		35	50		35	50	Ω
	FULL		40	75		40	75	Ω
IS_{OFF} OFF Input Leakage Current (Note 3)	+25°C		.04	1		.04	5	nA
	FULL		1	100		0.2	100	nA
ID_{OFF} OFF Output Leakage Current (Note 3)	+25°C		.04	1		.04	5	nA
	FULL		1	100		0.2	100	nA
ID_{ON} ON Leakage Current (Note 4)	+25°C		.03	1		.03	5	nA
	FULL		0.5	100		0.2	100	nA
DIGITAL INPUT CHARACTERISTICS								
V_{INL} Input Low Level	FULL			.8			.8	V
V_{INH} Input High Level	FULL	4			4			V
I_{INH} Input Leak. Current (High) (Note 5)	FULL			1			1	µA
I_{INL} Input Leak. Current (Low) (Note 5)	FULL			1			1	µA
SWITCHING CHARACTERISTICS								
t_{OPEN}, Break-Before Make Delay (HI-387/390 only)	+25°C		60			60		ns
t_{ON}, Switch ON Time	+25°C		210	300		210	300	ns
t_{OFF}, Switch OFF Time	+25°C		160	250		160	250	ns
OFF Isolation (Note 6)	+25°C		60			60		dB
Charge Injection (Note 7)	+25°C		3			3		mV
CS_{OFF} Input Switch Capacitance	+25°C		16			16		pF
CD_{OFF} Output Switch Capacitance	+25°C		14			14		pF
CD_{ON} Output Switch Capacitance	+25°C		35			35		pF
C_{IN} (High) Digital Input Capacitance	+25°C		5			5		pF
C_{IN} (Low) Digital Input Capacitance	+25°C		5			5		pF
POWER REQUIREMENTS								
I+ Current (Note 8)	+25°C		.09	.5		.09	.5	mA
	FULL			1			1	mA
I- Current (Note 8)	+25°C		.01	10		.01	100	µA
	FULL			100				µA
I+ Current (Note 9)	+25°C		.01	10		.01	100	µA
	FULL			100				µA
I- Current (Note 9)	+25°C		.01	10		.01	100	µA
	FULL			100				µA

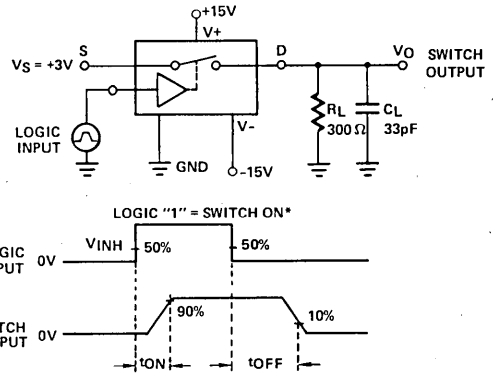
ELECTRICAL CHARACTERISTICS NOTES :

1. As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Characteristics" are the only conditions recommended for satisfactory operation.
2. $V_S = \pm 10V$, $I_{OUT} = -10mA$ on resistance derived from the voltage measured across the switch under the above conditions.
3. $V_S = \pm 14V$, $V_D = \mp 14V$.
4. $V_S = V_D = \pm 14V$.
5. The digital inputs are diode protected MOS gates and typical leakages of 1nA or less can be expected.
6. $V_S = 1V_{RMS}$, f = 500kHz, $C_L = 15pF$, $R_L = 1k$, $C_L = C_{FIXTURE} + C_{PROBE}$, "off isolation" = $20\log V_S/V_D$.
7. $V_S = 0V$, $C_L = 10{,}000pF$, Logic Drive = 5V pulse. Switches are symmetrical; S and D may be interchanged.
8. $V_{IN} = 4V$. (one input) (all other inputs = 0)
9. $V_{IN} = 0.8V$. (all inputs)
10. To drive from DTL/TTL circuits, pull-up resistors to +5V Supply are recommended.

TEST CIRCUITS

SWITCHING TEST CIRCUIT (t_{ON}, t_{OFF})

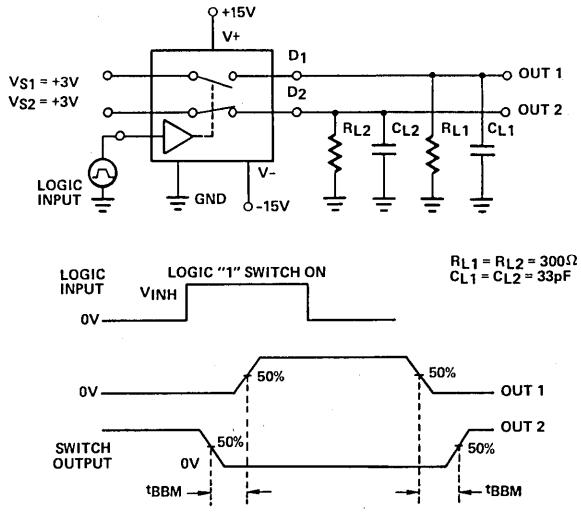
SWITCH TYPE	V_{INH}
HI-381 thru HI-390	5V



*Inverted logic for HI-381

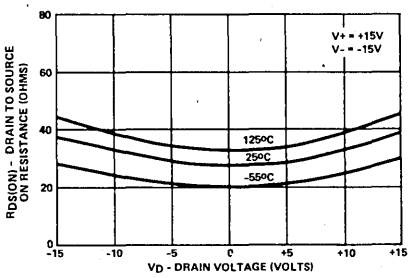
BREAK-BEFORE-MAKE TEST CIRCUIT (t_{BBM})

SWITCH TYPE	V_{INH}
HI-387 and HI-390	5V

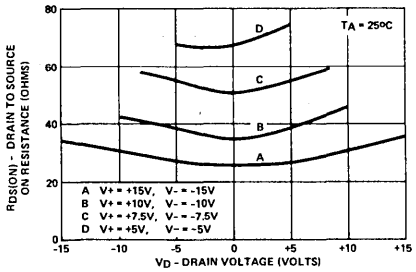


TYPICAL PERFORMANCE CURVES

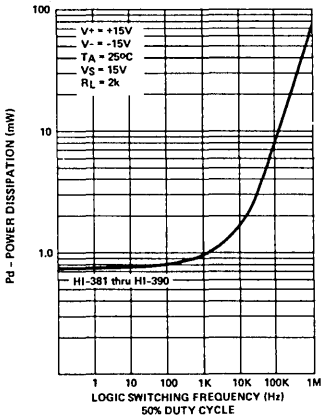
$R_{DS(ON)}$ VS. V_D AND TEMPERATURE



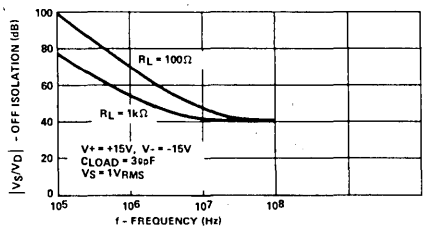
$R_{DS(ON)}$ VS. V_D AND POWER SUPPLY VOLTAGE



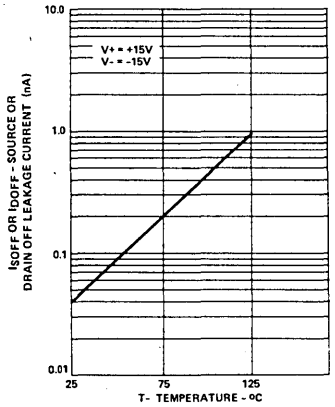
DEVICE POWER DISSIPATION VS. SWITCHING FREQUENCY SINGLE LOGIC INPUT



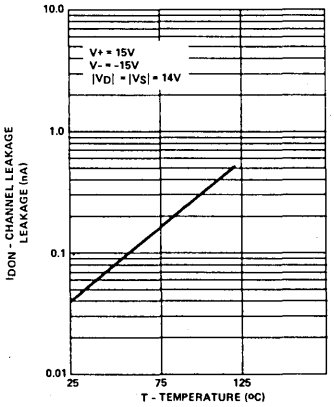
OFF ISOLATION VS. FREQUENCY



I_{SOFF} OR I_{DOFF} VS. TEMPERATURE*

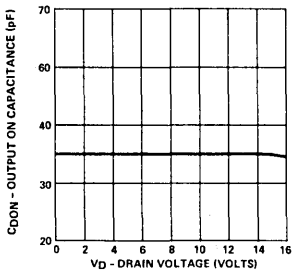


I_{DON} VS. TEMPERATURE*

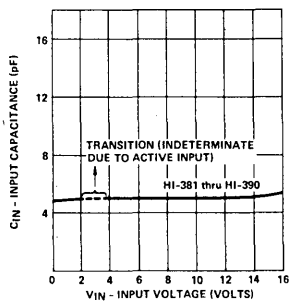


* The net leakage into the source or drain is the n-channel leakage minus the p-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

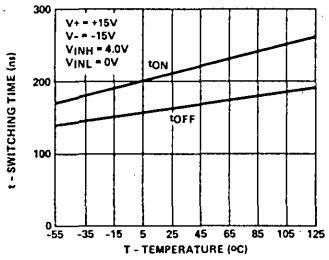
OUTPUT ON CAPACITANCE VS. DRAIN VOLTAGE



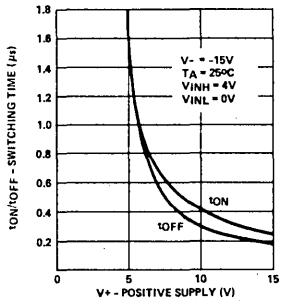
DIGITAL INPUT CAPACITANCE VS. INPUT VOLTAGE



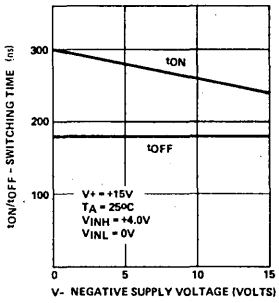
SWITCHING TIME VS. TEMPERATURE HI-381 thru HI-390



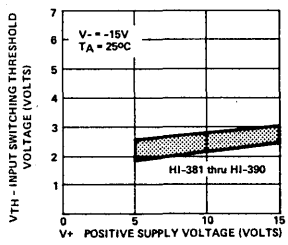
SWITCHING TIME VS. POSITIVE SUPPLY VOLTAGE HI-381 thru HI-390



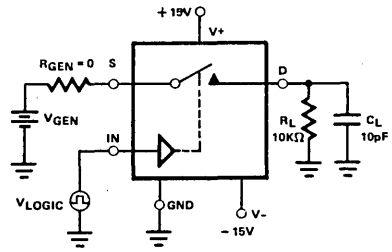
SWITCHING TIME VS. NEGATIVE SUPPLY VOLTAGE HI-381 thru HI-390



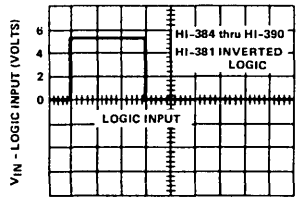
INPUT SWITCHING THRESHOLD VS. POSITIVE SUPPLY VOLTAGE HI-381 thru HI-390

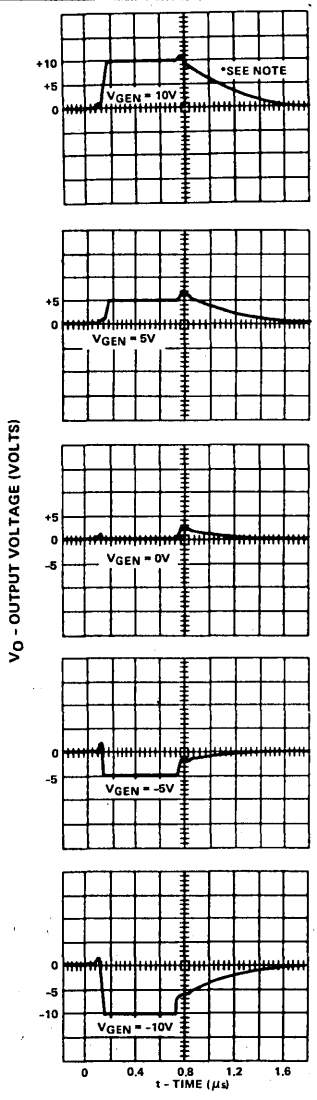


Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.





* NOTE: The turn-off time is primarily limited here by the RC time constant (100ns) of the load.

HARRIS
SEMICONDUCTOR ANALOG PRODUCTS DIVISION

HI-1800A

Low Leakage Dual DPST Analog Switch

FEATURES

- LEAKAGE (TYP.) 40nA
- SIGNAL RANGE ±15V
- "ON" RESISTANCE (TYP.) 125Ω
- ACCESS TIME (TYP.) 500ns
- DTL/TTL COMPATIBLE ADDRESS

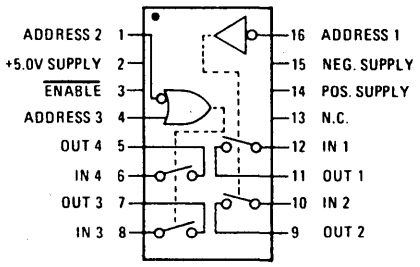
APPLICATIONS

- SIGNAL SELECTOR
- CHOPPER
- SAMPLE AND HOLD
- GAIN SWITCHING

DESCRIPTION

The HI-1800A is a general purpose analog switch which may be used as a signal selector, multiplexer, chopper, or cross-point switch for signals from D.C. to R.F. The configuration is two independent DPST switches with versatile TTL compatibile addressing logic which allows connection as two SPDT, or as a single DPDT, SPDT, or SPST switch by connection of external jumpers. ON resistance decreases correspondingly when switching elements are connected in parallel. The HI-1800A is fabricated on a single dielectrically isolated chip using complementary N and P channel MOS devices. This unique process produces exceptionally low leakage currents, constant ON resistance, low power dissipation, and fast switching. The HI-1800A is available in a hermetic 16 pin dual-in-line package.

PINOUT

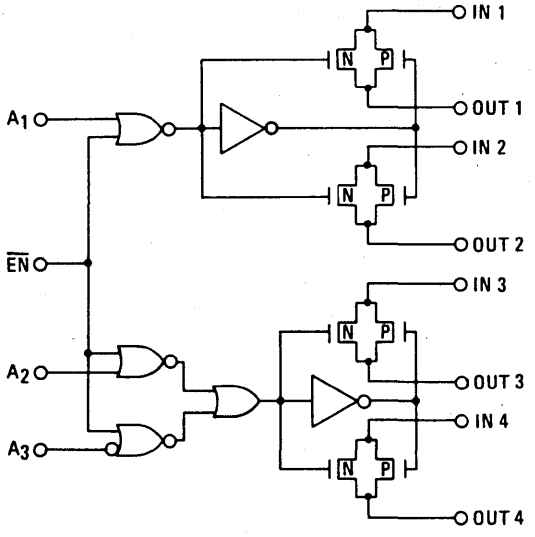


TRUTH TABLE

INPUT ADDRESS				SWITCH CHANNELS			
A1	A2	A3	$\overline{EN}$	1	2	3	4
L	X	X	L	ON	ON		
H	X	X	L	OFF	OFF		
X	L	X	L			ON	ON
X	X	H	L			ON	ON
X	H	L	L			OFF	OFF
X	X	X	H	OFF	OFF	OFF	OFF

H ≥ +4.0V L ≤ +0.4V

FUNCTIONAL DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage Between Pins 14 and 15	40.0V	Digital Input Voltage	V^-_{Supply}, V^+_{Supply}
Logic Supply Voltage, Pin 2	30.0V	Total Power Dissipation	780 mW (Note 2)
Analog Input Voltage: V^+_{Supply} +2V	V^-_{Supply} -2V	Storage Temperature Range	-65^oC to $+150^oC$

ELECTRICAL CHARACTERISTICS

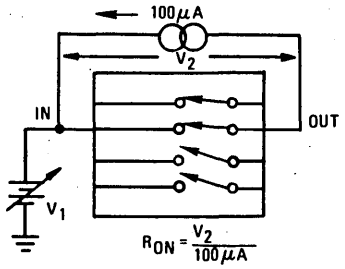
Supplies = +15V, -15V, +5.0V

PARAMETER	TEMP.	HI-1800A-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS					
V_{IN}, Analog Signal Range	Full	-15		+15	V
R_{ON}, ON Resistance (Note 3)	+25°C		125	200	Ω
	Full			250	Ω
I_S (OFF), Input Leakage Current	Full		40	100	nA
I_D (OFF), Output Leakage Current	Full		40	100	nA
I_D (ON), On Channel Leakage Current	Full		40	100	nA
DIGITAL INPUT CHARACTERISTICS					
V_{IL}, Input Low Threshold	Full			0.4	V
V_{IH}, Input High Threshold (Note 4)	Full	4.0			V
I_{IN}, Input Leakage Current	Full		.01	1	μA
SWITCHING CHARACTERISTICS					
t_A, Access Time (Note 5)	+25°C		500		ns
Break-Before-Make Delay	+25°C		200		ns
C_{IN}, Channel Input Capacitance	+25°C		8		pF
C_{OUT}, Channel Output Capacitance	+25°C		8		pF
C_D, Digital Input Capacitance	+25°C		5		pF
POWER REQUIREMENTS					
P_D, Power Dissipation	Full		10		mW
P_{DS}, Standby Power (Note 6)	Full		10		mW
I_+, Current Pin 14	Full		0.001	1	mA
I_-, Current Pin 15	Full		0.5	2	mA
I_L, Current Pin 2	Full		0.5	2	mA

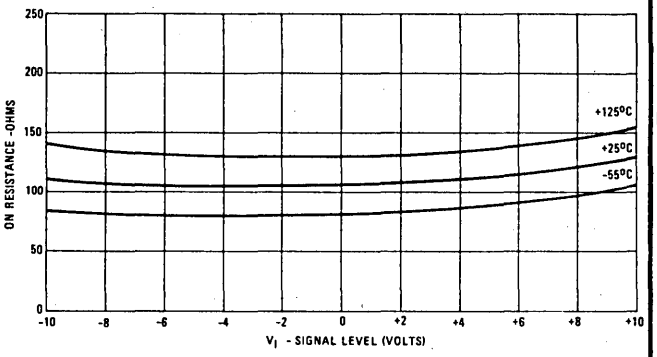
NOTES:
1. Voltage ratings apply when voltages at all other pins are within their nominal operating ranges.
2. Derate 9.25 mW/°C above t_A = +75°C
3. $V_{OUT} = \pm 10V$ $I_{OUT} = -100\mu A$.
4. To drive from DTL/TTL circuits, 1K pullup resistors to +5.0V supply are recommended.
5. Time measured to 90% of final output level; V_{OUT} = -5.0V to +5.0V, Digital Inputs = 0.4V to +4.0V.
6. Voltage at Pin 3, $\overline{ENABLE} \geq +4.0V$.

PERFORMANCE CHARACTERISTICS

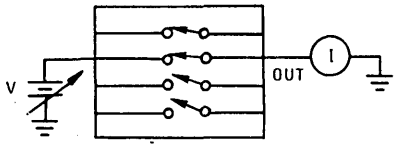
ON RESISTANCE vs ANALOG SIGNAL LEVEL



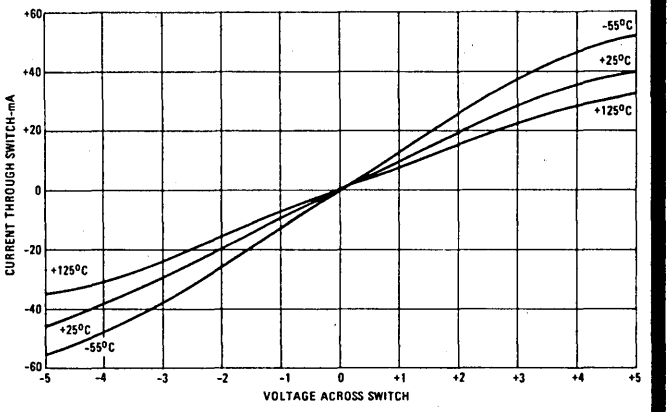
Test Circuit



ON CHANNEL CURRENT vs VOLTAGE

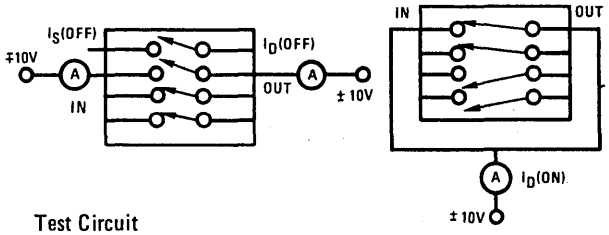


Test Circuit

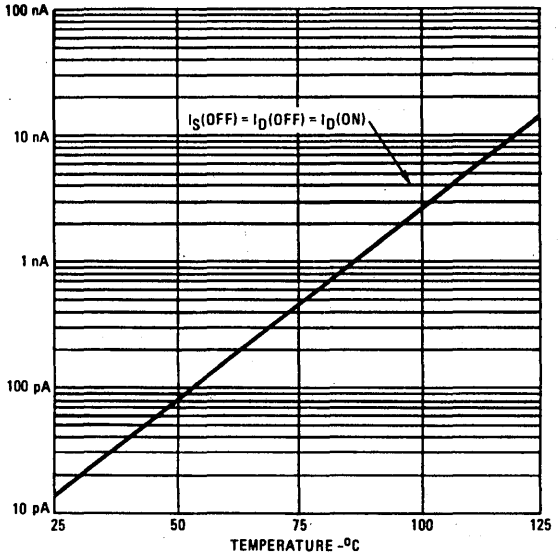


ON/OFF LEAKAGE CURRENTS vs TEMPERATURE

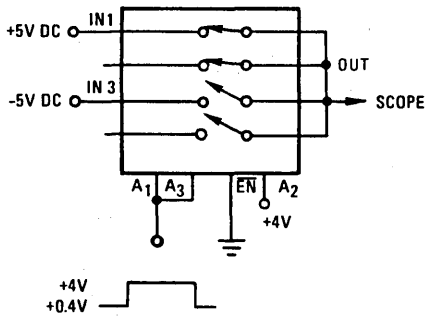
OFF LEAKAGE ON LEAKAGE

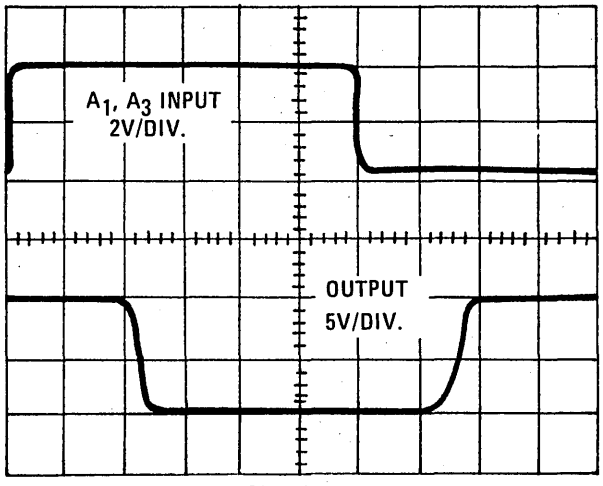


Test Circuit



ACCESS TIME





HARRIS

HI-5040 thru HI-5051
HI-5046A and
HI-5047A

CMOS Analog Switches

FEATURES

- WIDE ANALOG SIGNAL RANGE ±15V
- LOW "ON" RESISTANCE (TYP) 25Ω
- HIGH CURRENT CAPABILITY (TYP) 80mA
- BREAK-BEFORE-MAKE SWITCHING
  - TURN-ON TIME (TYP) 370ns
  - TURN-OFF TIME (TYP) 280ns
- NO LATCH-UP
- INPUT MOS GATES ARE PROTECTED FROM ELECTROSTATIC DISCHARGE
- DTL, TTL, CMOS, PMOS COMPATIBLE

APPLICATIONS

- HIGH FREQUENCY SWITCHING
- SAMPLE AND HOLD
- DIGITAL FILTERS
- OP AMP GAIN SWITCHING

DESCRIPTION

This family of CMOS analog switches offers low-resistance switching performance for analog voltages up to the supply rails and for signal currents up to 80mA. "ON" resistance is low and stays reasonably constant over the full range of operating signal voltage and current. R_{ON} remains exceptionally constant for input voltages between +5V and -5V and currents up to 50mA. Switch impedance also changes very little over temperature, particularly between 0°C and +75°C. R_{ON} is nominally 25 ohms for HI-5048 through HI-5051 and HI-5046A/5047A and 50Ω for HI-5040 through HI-5047.

All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. Performance is further enhanced by Dielectric Isolation processing which insures latch-free operation with very low input and output leakage currents (0.8nA at 25°C). This family of switches also features very low power operation (1.5mW at 25°C).

There are 14 devices in this switch series which are differentiated by type of switch action and value of R_{ON} (see Functional diagram). All devices are available in 16 pin D.I.P. packages. The HI-5040/5050 switches can directly replace IH-5040 series devices and are functionally compatible with the DG 180/190 family. Each switch type is available in the -55°C to +125°C and 0°C to +75°C performance grades.

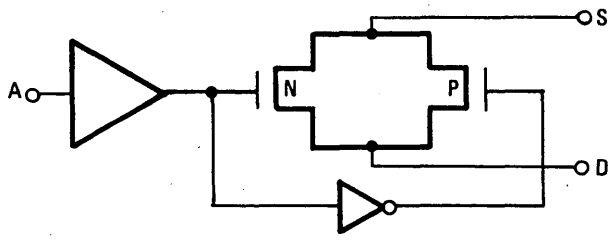
FUNCTIONAL DESCRIPTION

Section 11 for Packaging

PART NUMBER	TYPE	R_{ON}
HI-5040	SPST	75Ω
HI-5041	DUAL SPST	75Ω
HI-5042	SPDT	75Ω
HI-5043	DUAL SPDT	75Ω
HI-5044	DPST	75Ω
HI-5045	DUAL DPST	75Ω
HI-5046	DPDT	75Ω
HI-5046A	DPDT	30Ω
HI-5047	4PST	75Ω
HI-5047A	4PST	30Ω
HI-5048	DUAL SPST	30Ω
HI-5049	DUAL DPST	30Ω
HI-5050	SPDT	30Ω
HI-5051	DUAL SPDT	30Ω

FUNCTIONAL DIAGRAM

TYPICAL DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V^+ - V^-$)	36V
V_R to Ground	V^+, V^-
Digital and Analog Input Voltage	$V^+ + 4V$
	$V^- - 4V$

Analog Current (S to D)	80mA
Total Power Dissipation*	450mW
Operating Temperature	
HI-50XX-2	-55°C to +125°C
HI-50XX-5	0°C to +75°C
Storage Temperature	-65°C to +150°C

*Derate 6mW/°C above T_A = 75°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified

Supplies = +15V, -15V; V_R = 0V; V_{AH} (Logic Level High) = 3.0V; V_{AL} (Logic Level Low) = +0.8V, V_L = +5V

For Test Conditions, consult Performance Characteristics

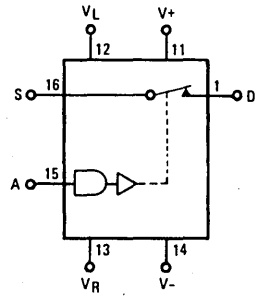
PARAMETER	TEMP	-55°C to +125°C MIN	-55°C to +125°C TYP	-55°C to +125°C MAX	0°C to +75°C MIN	0°C to +75°C TYP	0°C to +75°C MAX	UNITS
ANALOG SWITCH CHARACTERISTICS								
Analog Signal Range	Full	-15		+15	-15		+15	V
Ron, "ON" Resistance (Note 1a)	+25°C		50			50		Ω
	Full			75			75	Ω
Ron, "ON" Resistance (Note 1b)	+25°C		25			25		Ω
	Full			50			50	Ω
Ron, Channel-to-Channel Match (Note 1a)	+25°C		2	10		2	10	Ω
Ron, Channel-to-Channel Match (Note 1b)	+25°C		1	5		1	5	Ω
$I_{S(OFF)} = I_{D(OFF)}$, Off Input or Output Leakage Current	+25°C		0.8			0.8		nA
	Full		100	500		100	500	nA
$I_{D(ON)}$, On Leakage Current	+25°C		0.01			0.01		nA
	Full		2	500		2	500	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			0.8			0.8	V
V_{AH}, Input High Threshold	Full	3.0			3.0			V
I_A, Input Leakage Current (High or Low)	Full		.01	1.0		.01	1.0	μA
SWITCHING CHARACTERISTICS								
t_{on}, Switch "ON" Time	+25°C		370	1000		370	1000	ns
t_{off}, Switch "OFF" Time	+25°C		280	500		280	500	ns
Charge Injection (Note 2)	+25°C		5	20		5		mV
"OFF Isolation" (Note 3)	+25°C	75	80			80		dB
"Crosstalk" (Note 3)	+25°C	80	88			88		dB
$C_{S(OFF)}$, Input Switch Capacitance	+25°C		11			11		pF
$C_{D(OFF)}$, Output Switch Capacitance	+25°C		11			11		pF
$C_{D(ON)}$, Output Switch Capacitance	+25°C		22			22		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(OFF)}$, Drain-To-Source Capacitance	+25°C		0.5			0.5		pF
POWER REQUIREMENTS								
P_D, Quiescent Power Dissipation	+25°C		1.5			1.5		mW
I^+, +15V Quiescent Current	Full			0.3			0.5	mA
I^-, -15V Quiescent Current	Full			0.3			0.5	mA
I_L, +5V Quiescent Current	Full			0.3			0.5	mA
I_R, Gnd Quiescent Current	Full			0.3			0.5	mA

NOTES: 1. $V_{OUT} = \pm 10V$, I_{OUT} = 1mA
a) For HI-5040 thru HI-5047
b) For HI-5048 thru HI-5051, HI-5046A/5047A
2. V_{IN} = 0V, C_L = 10,000pF
3. $R_L = 100\Omega$, f= 100 KHz, $V_{IN} = 2\ V_{PP}$, C_L = 5pF

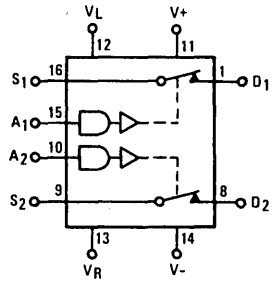
SWITCH FUNCTIONS

SWITCH STATES ARE FOR LOGIC "1" INPUT

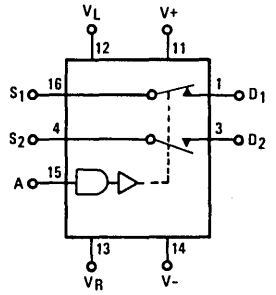
SPST
HI-5040 (75Ω)



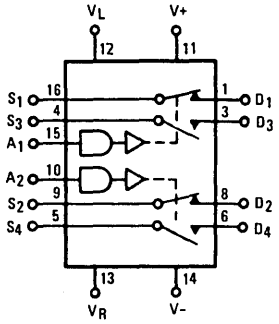
DUAL SPST
HI-5041 (75Ω)



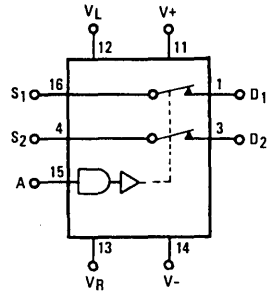
SPDT
HI-5042 (75Ω)



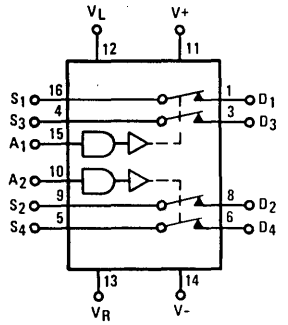
DUAL SPDT
HI-5043 (75Ω)



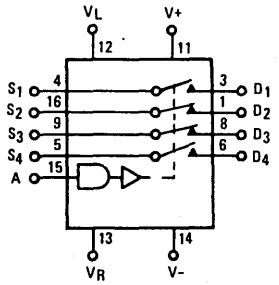
DPST
HI-5044 (75Ω)



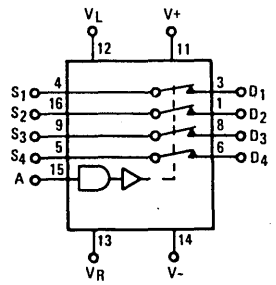
DUAL DPST
HI-5045 (75Ω)



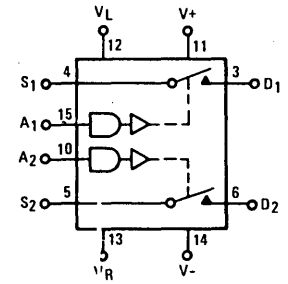
DPDT
HI-5046 (75Ω)
HI-5046A (30Ω)



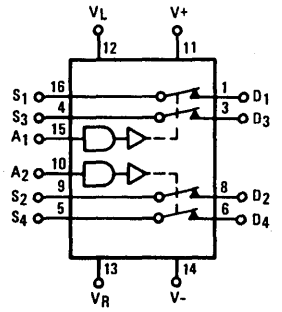
4PST
HI-5047 (75Ω)
HI-5047A (30Ω)



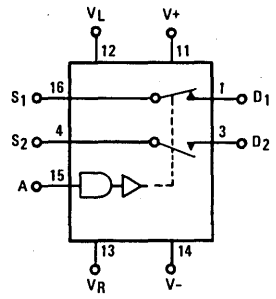
DUAL SPST
HI-5048 (30Ω)



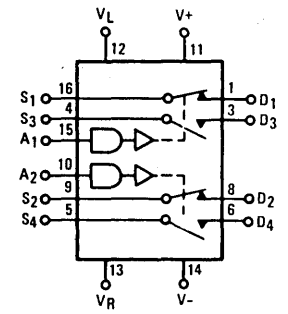
DUAL DPST
HI-5049 (30Ω)



SPDT
HI-5050 (30Ω)



DUAL SPDT
HI-5051 (30Ω)



HARRIS

HI-1818A/1828A

Low Resistance 8 Channel CMOS Analog Multiplexers

FEATURES

- SIGNAL RANGE ±15V
- "ON" RESISTANCE (TYP.) 250Ω
- INPUT LEAKAGE AT +125°C (TYP.) 20nA
- ACCESS TIME (TYP.) 350ns
- POWER CONSUMPTION (TYP.) 5mW
- DTL/TTL COMPATIBLE ADDRESS
- -55°C to +125°C OPERATION

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- PRECISION INSTRUMENTATION
- DEMULTIPLEXING
- SELECTOR SWITCH

DESCRIPTION

The HI-1818A/1828A are monolithic high performance CMOS analog multiplexers offering built-in channel selection decoding plus an inhibit (enable) input for disabling all channels. Dielectric Isolation (DI) processing is used for enhanced reliability and performance (see Application Note 521). Substrate leakage and parasitic capacitance are much lower, resulting in extremely low static errors and high throughput rates. Low output leakage (typically 0.1nA) and low channel ON resistance (250 Ω) assure optimum performance in low level or current mode applications.

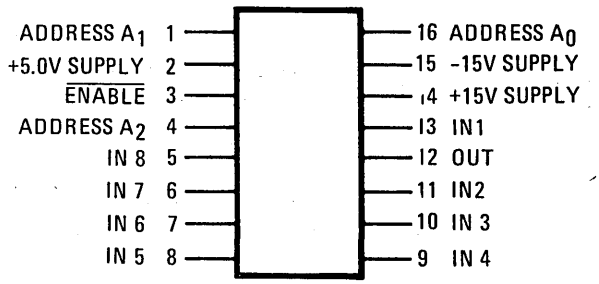
The 1818A is a single-ended 8 channel multiplexer, while the HI-1828A is a differential 4 channel version. Either device is ideally suited for medical instrumentation, telemetry systems, and microprocessor based data acquisition systems.

The HI-1818A-2 and HI-1828A are specified over -55°C to +125°C, while the -5 versions are specified over 0°C to +75°C.

PINOUT

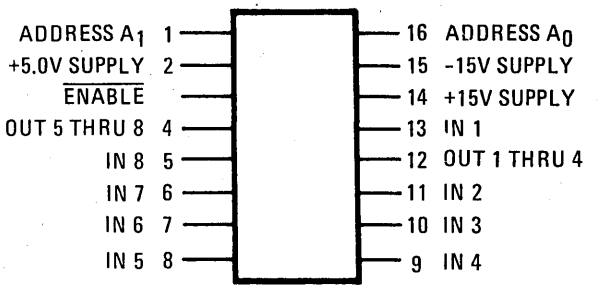
HI-1818A — **Section 11 for Packaging**

Top View



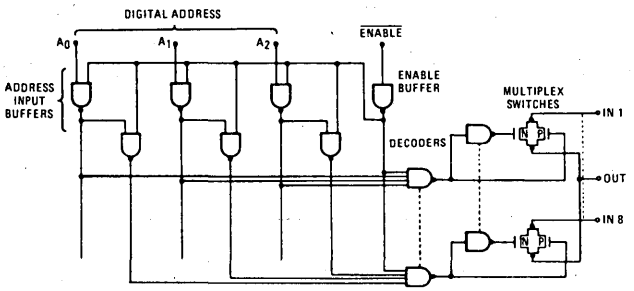
HI-1828A — **Section 11 for Packaging**

Top View

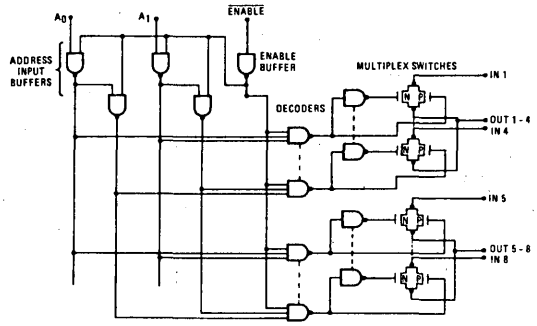


FUNCTIONAL DIAGRAM

HI-1818A



HI-1828A



ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Supply Voltage Between Pins 14 and 15	40.0V	Digital Input Voltage	V-Supply to V+ Supply
Logic Supply Voltage, Pin 2	30.0V	Total Power Dissipation (Note 2)	780mW
Analog Input Voltage: V^+_{Supply}	+2V	Storage Temperature Range	-65°C to +150°C
V^-_{Supply}	-2V		

ELECTRICAL CHARACTERISTICS

Supplies = +15V, -15V, +5V

PARAMETER	TEMP.	HI-1818A-2/1828A-2 -55°C to +125°C MIN.	TYP.	MAX.	HI-1818A-5/1828A-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
* V_{IN}, Analog Signal Range	Full	-15		+15	-15		+15	V
* R_{ON}, ON Resistance (Note 3)	+25°C		250	400		250	400	Ω
	Full		300	500		300	500	Ω
*I_S(OFF), Input Leakage Current	Full		20	50		20	50	nA
*I_D(ON), On Channel Leakage Current								
(HI-1818A)	Full		100	250		100	250	nA
(HI-1828A)	Full		50	125		50	125	nA
*I_D(OFF) Output Leakage Current								
(HI-1818A)	Full		100	250		100	250	nA
(HI-1828A)	Full		50	125		50	125	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			0.4			0.4	V
V_{AH}, Input High Threshold (Note 4)	Full	4.0			4.0			V
$I_{A,}$, Input Leakage Current	Full		.01	1		.01	1	μA
SWITCHING CHARACTERISTICS								
T_S, Access Time (Note 5)	+25°C		350			350		ns
Break-Before-Make Delay	+25°C		100			100		ns
Settling Time (0.1%)	+25°C		1.08			1.08		μs
(0.025%)	+25°C		2.8			2.8		μs
C_{IN}, Channel Input Capacitance	+25°C		4			4		pF
C_{OUT}, Channel Output Capacitance								
(HI-1818A)	+25°C		20			20		pF
(HI-1828A)	+25°C		10			10		pF
C_{DS}(OFF), Drain-To-Source Capacitance	+25°C		0.6			0.6		pF
C_D, Digital Input Capacitance	+25°C		5			5		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		5			5		mW
P_{DS}, Standby Power (Note 6)	Full		5			5		mW
* I_+, Current Pin 14	Full		0.1	0.5		0.1	1	mA
* I_-, Current Pin 15	Full		0.3	1		0.3	2	mA
* I_L, Current Pin 2	Full		0.3	1		0.3	2	mA

NOTES:
1. Voltage ratings apply when voltages at all other pins are within their normal operating ranges.
2. Derate 9.25 mW/°C above 75°C.
3. V_{OUT} = ± 10V I_{OUT} = - 1mA.
4. To drive from DTL/TTL circuits, 1K pull-up resistors to + 5.0V supply are recommended.
5. Time measured to 90% of final output level; V_{OUT} = - 5.0V to +5.0V, Digital Inputs = 0V to + 4.0V.
6. Voltage at Pin 3, $\overline{ENABLE}$ = + 4.0V.

100% Tested for Dash 8 at +25°C and +125°C Only.

TRUTH TABLES

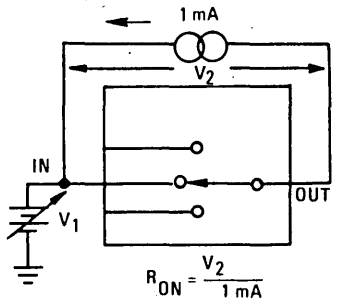
HI-1818A

ADDRESS A_2	A_1	A_0	$\overline{EN}$	"ON" CHANNEL
L	L	L	L	1
L	L	H	L	2
L	H	L	L	3
L	H	H	L	4
H	L	L	L	5
H	L	H	L	6
H	H	L	L	7
H	H	H	L	8
X	X	X	H	NONE

HI-1828A

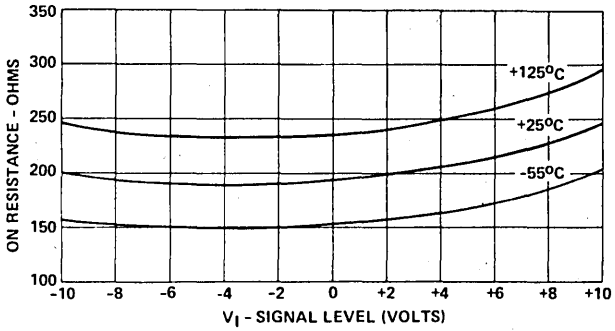
ADDRESS A_1	A_0	$\overline{EN}$	"ON" CHANNELS
L	L	L	1 and 5
L	H	L	2 and 6
H	L	L	3 and 7
H	H	L	4 and 8
X	X	H	NONE

ON RESISTANCE vs ANALOG SIGNAL LEVEL

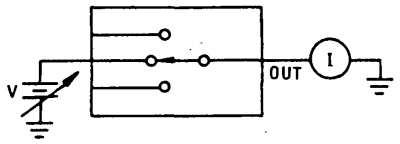


$$R_{ON} = \frac{V_2}{1\ mA}$$

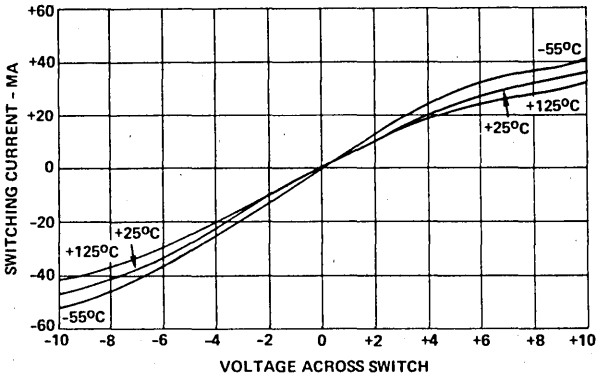
Test Circuit



ON CHANNEL CURRENT vs VOLTAGE

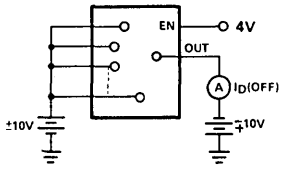


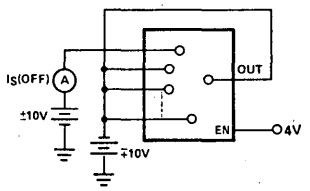
Test Circuit



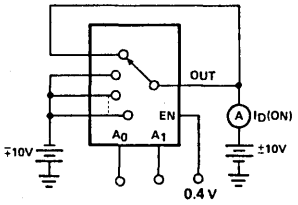
LEAKAGE CURRENTS vs TEMPERATURE

OFF LEAKAGE

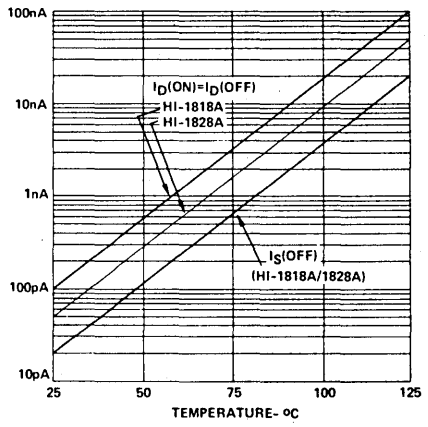




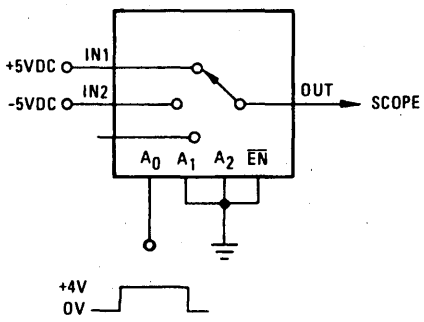
ON LEAKAGE

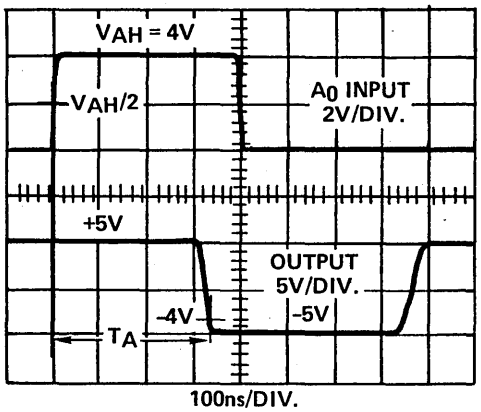


*Two measurements per channel: +10V/-10V and -10V/+10V. (Two measurements per device for ID(OFF): +10V/-10V and -10V/+10V.)



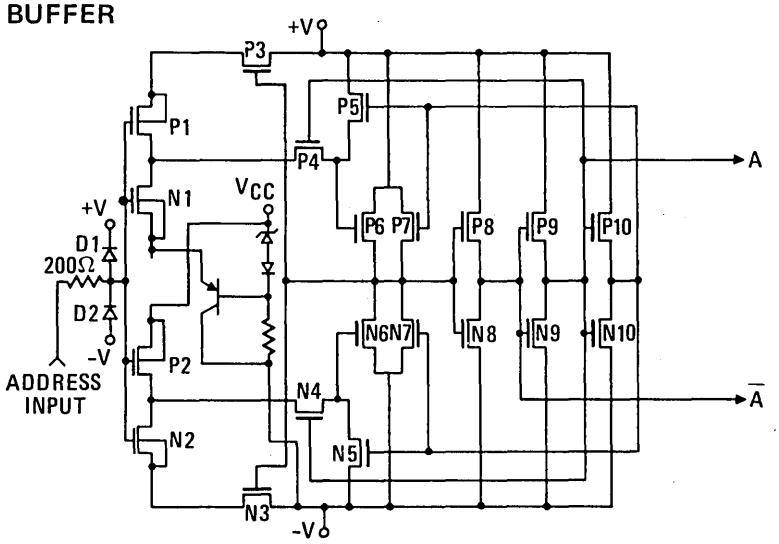
ACCESS TIME





SCHEMATIC DIAGRAM

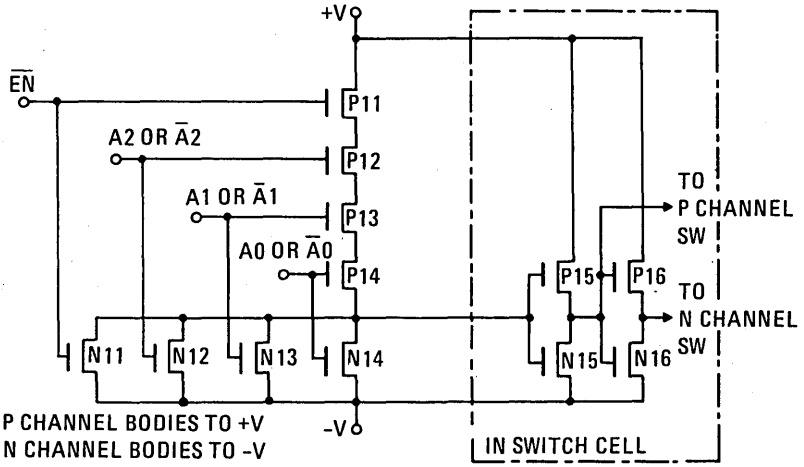
ADDRESS INPUT BUFFER



ALL N-CHANNEL BODIES TO V-

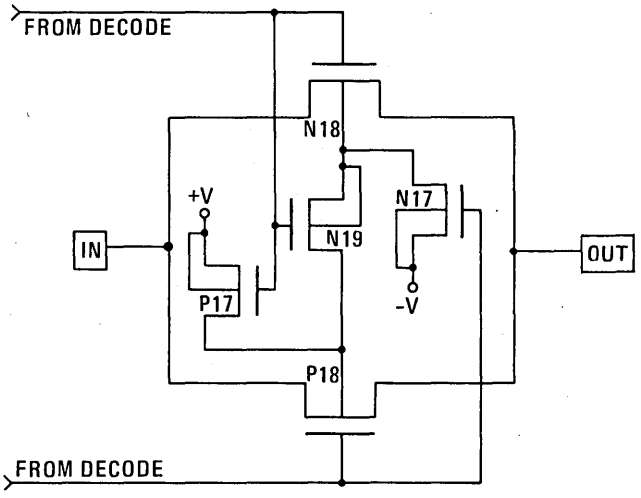
ALL P-CHANNEL BODIES TO V+ UNLESS OTHERWISE INDICATED.

DECODER GATE



A2 OR Ā2 NOT USED FOR HI-1828A

MULTIPLEX SWITCH



HARRIS

HI-506/HI-507

Single 16/Differential 8 Channel CMOS Analog Multiplexers

FEATURES

- LOW ON RESISTANCE (TYP.) 170Ω
- WIDE ANALOG SIGNAL RANGE ±15V
- DIRECTLY TTL/CMOS COMPATIBLE 2.4V (LOGIC "1")
- ACCESS TIME (TYP.) 300ns
- HIGH CURRENT CAPABILITY (TYP.) 50mA
- BREAK-BEFORE-MAKE SWITCHING
- NO LATCH-UP

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- PRECISION INSTRUMENTATION
- DEMULTIPLEXING
- SELECTOR SWITCH

DESCRIPTION

These monolithic CMOS multiplexers each include an array of eight analog switches, a digital decode circuit for channel selection, a voltage reference for logic thresholds, and an ENABLE input for device selection when several mulitplexers are present.

The Dielectic Isolation (DI) process used in fabrication of these devices eliminates the problem of latchup. Also, DI offers much lower substrate leakage and parasitic capacitance than conventional junction - isolated CMOS (See Application Note 521). With the low ON resistance (180Ω typical), this allows low static error, fast channel switching rates, and fast settling.

Switches are guaranteed to break-before-make, so two channels are never shorted together.

The switching threshold for each digital input is established by an internal +5V reference, providing a guaranteed minimum 2.4V for "1" and maximum 0.8V for "0". This allows direct interface without pullup resistors to signals from most logic families: CMOS, TTL, DTL and some PMOS. For protection against transient overvoltage, the digital inputs include a series 200Ω resistor and a diode clamp to each supply.

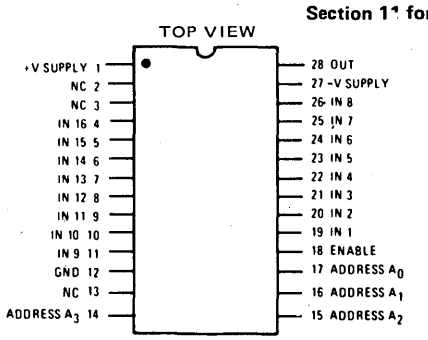
The HI-506 is a sixteen channel single-ended multiplexer, and the HI-507 is an eight channel differential version. The recommended supply voltage is ± 15V; however, reasonable performance is available down to ± 7V. Each device is packaged in a 16 pin DIP.

The HI-506/507 are specified for operation from 0°C to 70°C. The "-2" versions are specified from -55°C to +125°C. "Dash 8" (-8) designates -2 parts which have been screened per Mil-Std-883/ Method 5004/Class B.

PINOUT

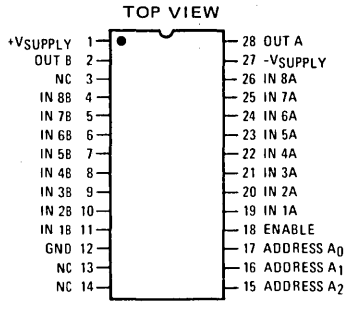
HI-506 — Section 11 for Packaging

TOP VIEW



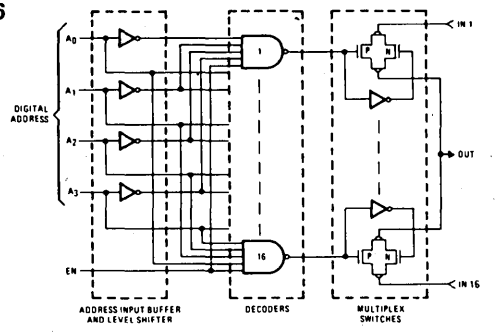
HI-507 — Section 11 for Packaging

TOP VIEW

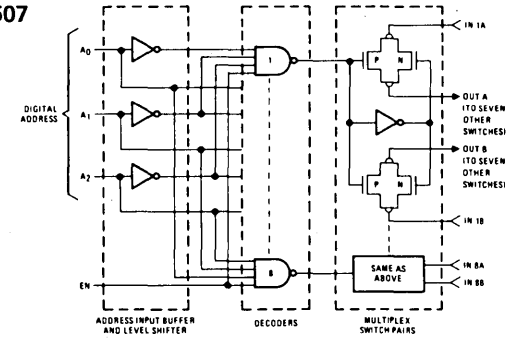


FUNCTIONAL DIAGRAM

HI-506



HI-507



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 1 and 27 40V

V_{EN}, V_A, Digital Input Overvoltage:

V_A { V_{Supply} (+) +4V; V_{Supply} (-) -4V

Analog Input Overvoltage: (Note 6)

V_D or V_S { V_{Supply} (+) +2V; V_{Supply} (-) -2V

Total Power Dissipation* 1200 mW

Operating Temperature:

HI-506/HI-507-2 -55°C to +125°C

HI-506/HI-507-5 0°C to +75°C

Storage Temperature -65°C to +150°C

*Derate 8mW/°C above T_A = +25°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified: Supplies = +15V, -15V; V_{AH}(Logic Level High) = +2.4V, V_{AL}(Logic Level Low) = +0.8V. For Test Conditions, consult Performance Characteristics section.

		HI-506/HI-507-2 -55°C to +125°C			HI-506/HI-507-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
ANALOG CHANNEL CHARACTERISTICS								
* V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
* R_{ON}, On Resistance (Note 1)	+25°C		170	300		270	400	Ω
	Full			400			500	Ω
* ΔR_{ON}, (Between Channels)	+25°C		6			6		%
* $I_{S(OFF)}$, Off Input Leakage Current	+25°C		0.03			0.03		nA
	Full			±50			±50	nA
* $I_{D(OFF)}$, Off Output Leakage Current	+25°C		0.3			1.0		nA
HI-506	Full			±500			±500	nA
HI-507	Full			±250			±250	nA
* $I_{D(ON)}$, On Channel Leakage Current	+25°C		0.3			1.0		nA
HI-506	Full			±500			±500	nA
HI-507	Full			±250			±250	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			+0.8			+0.8	V
V_{AH}, Input High Threshold	Full	+2.4			+2.4			V
* I_A, Input Leakage Current (High or Low)(Note 2)	Full			1.0			5.0	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		300	1000		300		ns
t_{OPEN}, Break-Before Make Delay	+25°C		80			80		ns
$t_{ON(EN)}$, Enable Delay (ON)	+25°C		300	1000		300		ns
$t_{OFF(EN)}$, Enable Delay (OFF)	+25°C		300	1000		300		ns
Settling Time (0.1%)	+25°C		1.2			1.2		μs
(0.025%)	+25°C		2.4			2.4		μs
"Off Isolation" (Note 3)	+25°C		75			75		dB
$C_{S(OFF)}$, Channel Input Capacitance	+25°C		4			4		pF
$C_{D(OFF)}$, Channel Output Capacitance								
HI-506	+25°C		44			44		pF
HI-507	+25°C		22			22		pF
C_A, Digital Input Capacitance	+25°C		2.2			2.2		pF
$C_{DS(OFF)}$, Input to Output Capacitance	+25°C		0.08			0.08		pF
POWER REQUIREMENTS								
* I+, Current Pin 1 (Note 4)	Full		1.7	3.0		3.4	5.0	mA
* I-, Current Pin 27 (Note 4)	Full		0.4	1.0		0.8	2.0	mA
* I+, Standby (Note 5)	Full		1.7	3.0		3.4	5.0	mA
* I-, Standby (Note 5)	Full		0.4	1.0		0.8	2.0	mA

NOTES:
1. V_{OUT} = ±10V, I_{OUT} = -1mA
2. Digital Inputs are Mos Gates. Typical Leakage Less Than 1nA.
3. V_{EN} = 0.8V, R_L = 1K, C_L = 28pF, V_S = 7VRMS, f = 500kHz.
4. V_{EN} = 4.0V, All V_A = 4.0V
5. V_{EN} = 0V, All V_A = 0V
6. If Analog Input Overvoltage Conditions are Anticipated, Use of HI-506A/507A Protected Multiplexers is Recommended. See HI-506A/507A Data Sheet.

* 100% Tested for Dash 8 at +25°C and +125°C Only.

TRUTH TABLES

HI-506

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-507

A_2	A_1	A_0	EN	ON SWITCH PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HARRIS

HI-506A/HI-507A

16 Channel CMOS Analog Multiplexer with Overvoltage Protection

FEATURES

- ANALOG/DIGITAL OVERVOLTAGE PROTECTION
- FAIL SAFE WITH POWER LOSS (NO LATCHUP)
- BREAK-BEFORE-MAKE SWITCHING
- DTL/TTL AND CMOS COMPATIBLE
- ANALOG SIGNAL RANGE ±15V
- ACCESS TIME (TYP.) 500ns
- SUPPLY CURRENT AT 1MHz ADDRESS TOGGLE (TYP.) 4mA
- STANDBY POWER (TYP.) 7.5mW

APPLICATIONS

- DATA ACQUISITION
- INDUSTRIAL CONTROLS
- TELEMETRY

DESCRIPTION

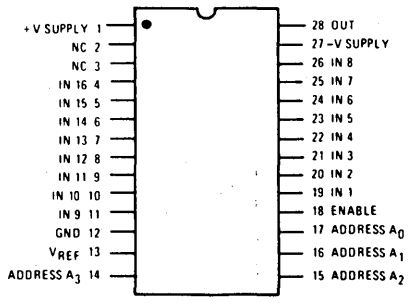
The HI-506A and HI-507A are dielectrically isolated CMOS analog multiplexers incorporating an important feature; they withstand analog input voltages much greater than the supplies. This is essential in any system where the analog inputs originate outside the equipment. They can withstand a continuous input up to 10 volts greater than either supply, which eliminates the possibility of damage when supplies are off, but input signals are present. Equally important they can withstand brief input transient spikes of several hundred volts; which otherwise would require complex external protection networks. Necessarily, ON resistance is somewhat higher than similar unprotected devices, but very low leakage currents combine to produce low errors. Application Notes 520 and 521 further explain these features.

The HI-506A-2 and HI-507A-2 are specified over -55°C to +125°C while the -5 versions are specified over 0°C to +75°C.

PINOUT

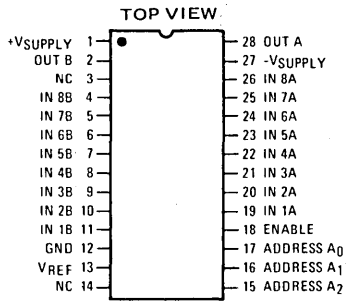
HI-506A — Section 11 for Packaging

TOP VIEW



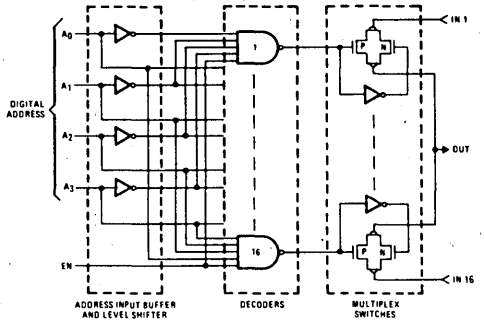
HI-507A — Section 11 for Packaging

TOP VIEW

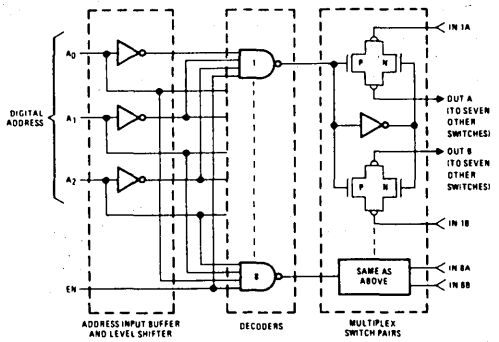


FUNCTIONAL DIAGRAM

HI-506A



HI-507A



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 1 and 27	40V	Total Power Dissipation*	1200mW
V_{REF} to Ground V+ to Ground	+20V	Operating Temperature	
V_{EN}, V_A, Digital Input Overvoltage:		HI-506A/507A-2	-55°C to +125°C
V_A (V_{Supply} (+))	+4V	HI-506A/507A-5	0°C to +75°C
V_A (V_{Supply} (−))	-4V	Storage Temperature	-65°C to +150°C
Analog Overvoltage:			
V_S (V_{Supply} (+))	+20V		
V_S (V_{Supply} (−))	-20V	*Derate 8mW/°C above T_A = +75°C	

ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

Supplies = +15V, -15V; V_{REF} (Pin 13) = Open; V_{AH} (Logic Level High) = +4.0V; V_{AL} (Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characteristics section.

PARAMETER		TEMP.	HI-506A/507A-2 -55°C to +125°C MIN.	TYP.	MAX.	HI-506A/507A-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS									
*V_S, Analog Signal Range		Full	-15		+15	-15		+15	V
*R_{ON}, On Resistance (Note 1)		+25°C		1.2	1.5		1.5	1.8	KΩ
		Full		1.5	2.0		1.8	2.0	KΩ
*I_S (OFF), Off Input Leakage Current		+25°C		0.03			0.03		nA
		Full			±50			±50	nA
*I_D (OFF), Off Output Leakage Current		+25°C		1.0			1.0		nA
	HI-506A	Full			±500			±500	nA
	HI-507A	Full			±250			±250	nA
*I_D (OFF) with Input Overvoltage Applied (Note 2)		+25°C		4.0			4.0		nA
		Full			2.0				μA
*I_D (ON), On Channel Leakage Current		+25°C		0.1			0.1		nA
	HI-506A	Full			±500			±500	nA
	HI-507A	Full			±250			±250	nA
DIGITAL INPUT CHARACTERISTICS									
V_{AL}, Input Low Threshold | TTL Drive		Full			0.8			0.8	V
V_{AH}, Input High Threshold | (Note 7)		Full	4.0			4.0			V
V_{AL} | MOS Drive (Note 3)		+25°C			0.8			0.8	V
V_{AH} |		+25°C	6.0			6.0			V
*I_A, Input Leakage Current (High or Low)		Full			1.0			5.0	μA
SWITCHING CHARACTERISTICS									
t_A, Access Time		+25°C		0.5	1.0		0.5		μs
t_{OPEN}, Break-Before Make Delay		+25°C		80			80		ns
t_{ON} (EN), Enable Delay (ON)		+25°C		300			300		ns
t_{OFF} (EN), Enable Delay (OFF)		+25°C		300			300		ns
Settling Time (0.1%)		+25°C		1.3			1.3		μs
(0.025%)		+25°C		4.4			4.4		μs
"Off Isolation" (Note 4)		+25°C		65			65		dB
C_S (OFF), Channel Input Capacitance		+25°C		5			5		pF
C_D (OFF), Channel Output Capacitance	HI-506A	+25°C		50			50		pF
	HI-507A	+25°C		25			25		pF
C_A, Digital Input Capacitance		+25°C		5			5		pF
C_{DS} (OFF), Input to Output Capacitance		+25°C		0.1			0.1		pF
POWER REQUIREMENTS									
P_D, Power Dissipation		Full		7.5			7.5		mW
*I+, Current Pin 1 (Note 5)		Full		0.5	2.0		0.5	5.0	mA
*I-, Current Pin 27 (Note 5)		Full		0.02	1.0		0.02	2.0	mA
*I+, Standby (Note 6)		Full		0.5	2.0		0.5	5.0	mA
*I-, Standby (Note 6)		Full		0.02	1.0		0.02	2.0	mA

NOTES:
1. V_{OUT} = ±10V, I_{OUT} = -100 μA.
2. Analog Overvoltage = ±33V.
3. V_{REF} = +10V.
4. V_{EN} = 0.8V, R_L = 1K, C_L = 7pF, V_S = 3VRMS, f = 500KHz.
5. V_{EN} = +4.0V.
6. V_{EN} = 0.8V.
7. To drive from DTL/TTL circuits, 1KΩ pull-up resistors to +5.0V supply are recommended.

* 100% Tested for Dash 8 at +25°C and +125°C Only.

TRUTH TABLES

HI-506A

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-507A

A_2	A_1	A_0	EN	ON SWITCH PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HARRIS

HI-508/HI-509

Single 8/Differential 4 Channel CMOS Analog Multiplexer

FEATURES

- FAST ACCESS 220ns
- FAST SETTLING (0.01%) 600ns
- LOW R_{ON} 180 Ω
- BREAK-BEFORE-MAKE SWITCHING
- NO LATCH-UP
- TTL/CMOS COMPATIBLE 2.4V (LOGIC "1")

APPLICATIONS

- PRECISION INSTRUMENTS
- DATA ACQUISITION SYSTEMS
- TELEMETRY

DESCRIPTION

These monolithic CMOS multiplexers each include an array of eight analog switches, a digital decode circuit for channel selection, a voltage reference for logic thresholds, and an ENABLE input for device selection when several multiplexers are present.

The Dielectric Isolation (DI) process used in fabrication of these devices eliminates the problem of latch-up. Also, DI offers much lower substrate leakage and parasitic capacitance than conventional junction-isolated CMOS (see Application Note 521). Combined with the low ON resistance (180Ω typical), these benefits allow low static error, fast channel switching rates, and fast settling.

Switches are guaranteed to break-before-make, so two channels are never shorted together.

The switching threshold for each digital input is established by an internal +5V reference, providing a guaranteed min. 2.4V for "1" and max. 0.8V for "0". This allows direct interface without pull-up resistors to signals from most logic families: CMOS, TTL, DTL, and some PMOS. For protection against transient overvoltage, the digital inputs include a series 200Ω resistor and a diode clamp to each supply.

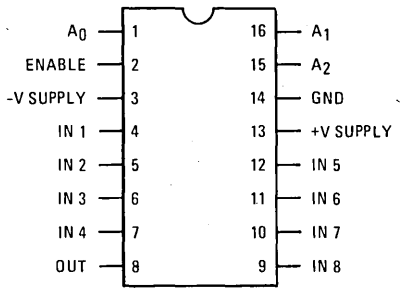
The HI-508 is an eight channel single-ended multiplexer, and the HI-509 is a four channel differential version. The recommended supply voltage is ±15V; however, reasonable performance is available down to ±7V. Each device is packaged in a 16 pin DIP.

The HI-508/509-5 are specified for operation from 0°C to 70°C. The "-2" versions are specified from -55°C to ±125°C. "Dash 8" (-8) designates -2 parts which have been screened per MIL-STD-883/Method 5004/Class B.

PINOUTS

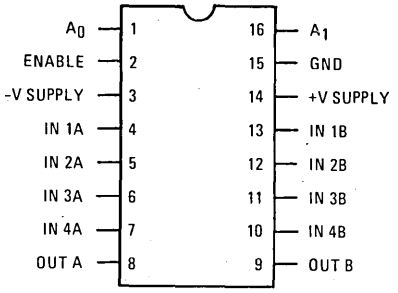
HI-508 — Section 11 for Packaging

TOP VIEW



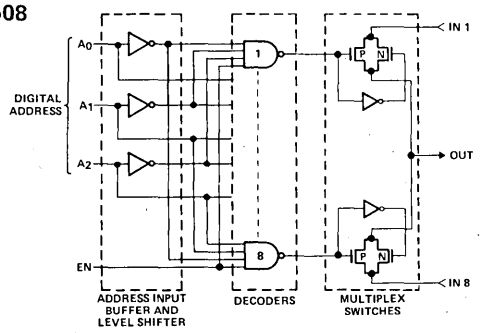
HI-509 — Section 11 for Packaging

TOP VIEW

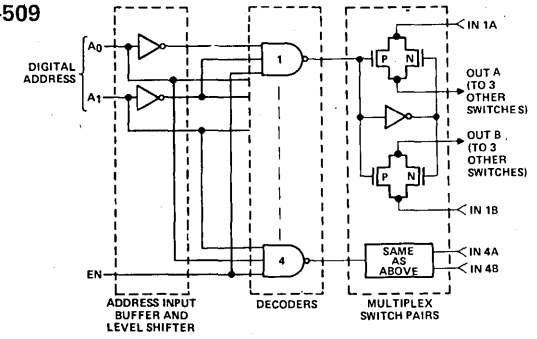


FUNCTIONAL DIAGRAMS

HI-508



HI-509



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

$V_{Supply}^{(+)}$ to $V_{Supply}^{(-)}$ 40V

$V_{Supply}^{(+)}$ to GND 20V

$V_{Supply}^{(-)}$ to GND 20V

Digital Input Overvoltage:

V_{EN}, V_A $\begin{cases} V_{Supply}^{(+)} & +4V \\ V_{Supply}^{(-)} & -4V \end{cases}$

Analog Input Overvoltage (Note 6):

V_D, V_S $\begin{cases} V_{Supply}^{(+)} & +2V \\ V_{Supply}^{(-)} & -2V \end{cases}$

Power Dissipation * 750mW
(Derate 8mW/°C above T_A = +75°C)

Operating Temperature Ranges:
HI-508/509-2, -8 -55°C to +125°C
HI-508/509-5, -6 0°C to 70°C
HI-508/509-1 -55°C to +200°C

Storage Temperature Range -65°C to +150°C

* Package Limitation

ELECTRICAL CHARACTERISTICS Unless otherwise specified: Supplies = ± 15V, GND = 0V

		HI-508/HI-509-2 -55°C to +125°C			HI-508/HI-509-5 0°C to +70°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
ANALOG CHANNEL CHARACTERISTICS								
V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
R_{ON}, On Resistance	+25°C		180	300		180	400	Ω
	Full		230	400		230	500	Ω
ΔR_{ON}, Any Two Channels	+25°C		5			5		%
$I_{S(OFF)}$, Off Input Leakage Current (Note 2)	+25°C			10			10	nA
	Full			50			50	nA
$I_{D(OFF)}$, Off Output Leakage Current	+25°C							
HI-508	Full		10	200		10	200	nA
HI-509	Full		10	100		10	100	nA
$I_{D(ON)}$, On Channel Leakage Current	+25°C							
HI-508	Full		10	200		10	200	nA
HI-509	Full		10	100		10	100	nA
I_{DIFF}, Differential Off Output Leakage Current (HI-509 Only)	+25°C		1	5		1	5	nA
	Full		5	50		5	50	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AH}, High Threshold	Full	2.4			2.4			V
V_{AL}, Low Threshold	Full			0.8			0.8	V
I_A, Input Leakage Current (High or Low) (Note 3)	Full			1			1	μA
SWITCHING CHARACTERISTICS								
t_A, Access (Transition) Time	+25°C		220	500		220	1000	ns
	Full			1000				ns
t_{OPEN}, Break-Before-Make Interval	+25°C		70			70		ns
$t_{ON(EN)}$, Enable Turn-On	+25°C		210			210		ns
$t_{OFF(EN)}$, Enable Turn-Off	+25°C		180			180		ns
t_S, Settling Tme to 0.1%	+25°C		360			360		ns
to 0.01%	+25°C		600			600		ns
Off Isolation (Note 4)	+25°C		68			68		dB
$C_{S(OFF)}$, Channel Input Capacitance	+25°C		5			5		pF
$C_{D(OFF)}$, Channel Output Capacitance	+25°C		21			21		pF
C_A, Digital Input Capacitance	+25°C		3			3		pF
$C_{DS(OFF)}$, Input to Output Capacitance	+25°C		.08			.08		pF
POWER REQUIREMENTS								
I+, Positive Supply Current (Note 5)	Full			2			2	mA
I-, Negative Supply Current (Note 5)	Full			1			1	mA
P_D, Power Dissipation	Full			45			45	mW

NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Ten nanoamps is the practical limit for high speed measurement in the production test environment. Actually, I_S (off) is below 100pA for most devices, at 25°C.
3. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1nA at 25°C.
4. V_{EN} = 0.8V, R_1 = 1K, C_1 = 15pF, V_S = $7V_{RMS}$, f = 500kHz. Worst case isolation occurs on channel 4 (HI-508) and channels 4, 8 (HI-509), due to proximity of the output pins.
5. V_{EN} = 0V or 5V. All V_A = 0.
6. If an overvoltage condition is anticipated (analog input exceeds either power supply voltage), the HARRIS HI-508A/509A multiplexers are recommended.

TRUTH TABLES

HI-508

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-509

A_1	A_0	EN	"ON" CHANNEL
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

HARRIS

HI-508A/509A

8 Channel CMOS Analog Multiplexers with Overvoltage Protection

FEATURES

- ANALOG/DIGITAL OVERVOLTAGE PROTECTION
- FAIL SAFE WITH POWER LOSS (NO LATCHUP)
- BREAK-BEFORE-MAKE SWITCHING
- DTL/TTL AND CMOS COMPATIBLE
- ANALOG SIGNAL RANGE ±15V
- ACCESS TIME (TYP.) 500ns
- SUPPLY CURRENT AT 1MHz ADDRESS TOGGLE (TYP.) 4mA
- STANDBY POWER (TYP.) 7.5mW

APPLICATIONS

- DATA ACQUISITION
- INDUSTRIAL CONTROLS
- TELEMETRY

DESCRIPTION

The HI-508A and HI-509A are dielectrically isolated CMOS analog multiplexers incorporating an important feature; they withstand analog input voltages much greater than the supplies. This is essential in any system where the analog inputs originate outside the equipment. They can withstand a continuous input up to 10 volts greater than either supply, which eliminates the possibility of damage when supplies are off, but input signals are present. Equally important, they can withstand brief input transient spikes of several hundred volts; which otherwise would require complex external protection networks. Necessarily, ON resistance is somewhat higher than similar unprotected devices, but very low leakage currents combine to produce low errors. Application Notes 520 and 521 further explain these features.

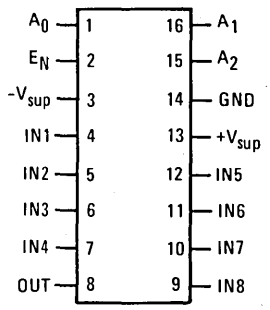
The HI-508A-2 and HI-509A-2 are specified over -55°C to +125°C while the -5 versions are specified over 0°C to +75°C.

PINOUT

HI-508A

Section 11 for Packaging

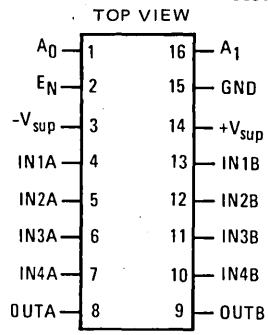
TOP VIEW



HI-509A

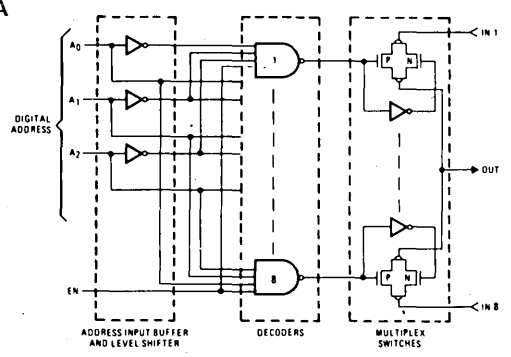
Section 11 for Packaging

TOP VIEW

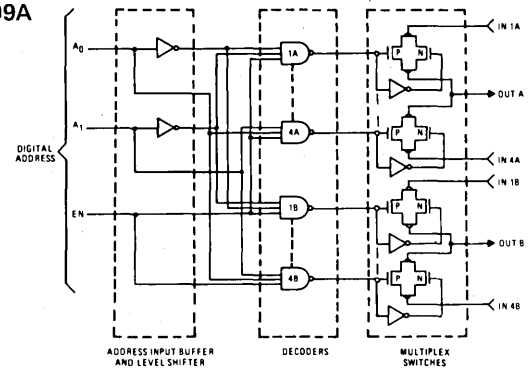


FUNCTIONAL DIAGRAM

HI-508A



HI-509A



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage between Supply Pins 40V

V+ to Ground 20V

V_{EN}, V_A, Digital Input Overvoltage:

V_A { V_{Supply}(+) +4V; V_{Supply} (-) -4V

Analog Input Overvoltage:

V_S { V_{Supply} (+) +20V; V_{Supply} (-) -20V

Total Power Dissipation* 725 mW

Operating Temperature:

HI-508A/HI-509A-2 -55°C to +125°C

HI-508A/HI-509A-5 0°C to +75°C

Storage Temperature -65°C to +150°C

*Derate 8mW/°C above t_A = 75°C

ELECTRICAL CHARACTERISTICS (Unless Otherwise Specified)

Supplies = +15V, -15V; V_{AH} (Logic Level High) = +4.0V; V_{AL} (Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characterisitcs section.

PARAMETER	TEMP.	HI-508A/509A-2 -55°C to +125°C MIN.	TYP.	MAX.	HI-508A/509A-5 0°C to +75°C MIN.	TYP	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
*V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
* R_{ON}, On Resistance (Note 1)	+25°C		1.2	1.5		1.5	1.8	KΩ
	Full		1.5	1.8		1.8	2.0	KΩ
* $I_{S(OFF)}$, Off Input Leakage Current	+25°C		0.03			0.03		nA
	Full			±50			±50	nA
* $I_{D(OFF)}$, Off Output Leakage Current	+25°C		1.0			1.0		nA
HI-508A	Full			±250			±250	nA
HI-509A	Full			±125			±125	nA
* $I_{D(OFF)}$ with Input Overvoltage Applied (Note 2)	+25°C		4.0			4.0		nA
	Full			2.0				μA
* $I_{D(ON)}$, On Channel Leakage Current	+25°C		0.1			0.1		nA
HI-508A	Full			±250			±250	nA
HI-509A				±125			±125	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold (Note 6)	Full			0.8			0.8	V
V_{AH}, Input High Threshold (Note 6)	Full	4.0			4.0			V
* I_A, Input Leakage Current (High or Low)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		0.5	1.0		0.5		μs
t_{OPEN}, Break - Before Make Delay	+25°C		80			80		ns
$t_{ON(EN)}$, Enable Delay (ON)	+25°C		300			300		ns
$t_{OFF(EN)}$, Enable Delay (OFF)	+25°C		300			300		ns
Settling Time (0.1%)	+25°C		1.2			1.2		μs
(0.025%)	+25°C		3.5			3.5		μs
"OFF Isolation" (Note 3)	+25°C		65			65		dB
$C_{S(OFF)}$, Channel Input Capacitance	+25°C		5			5		pF
$C_{D(OFF)}$, Channel Output Capacitance								
HI-508A	+25°C		25			25		pF
HI-509A	+25°C		12			12		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(OFF)}$, Input to Output Capacitance	+25°C		0.1			0.1		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		7.5			7.5		mW
*I+, Current (Note 4)	Full		0.5	2.0		0.5	5.0	mA
*I-, Current (Note 4)	Full		0.02	1.0		0.02	2.0	mA
*I+, Standby (Note 5)	Full		0.5	2.0		0.5	5.0	mA
*I-, Standby (Note 5)	Full		0.02	1.0		0.02	2.0	mA

NOTES:
1. V_{OUT} = ± 10V, I_{OUT} = -100μA
2. Analog Overvoltage = ± 33V
3. V_{EN} = 0.8V, R_L = 1K, C_L = 7pF, V_S = 3V RMS, f = 500KHz
4. V_{EN} = +4.0V
5. V_{EN} = 0.8V
6. To drive from DTL/TTL Circuits, 1KΩ pull-up resistors to +5.0V supply are recommended

* 100% Tested for Dash 8 at +25°C and +125°C Only.

TRUTH TABLES

HI-508A

A_2	A_1	A_0	E_N	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-509A

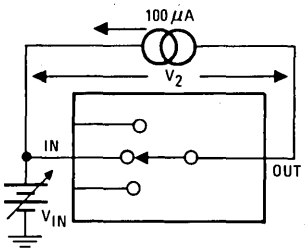
A_1	A_0	EN	ON SWITCH PAIR
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS

UNLESS OTHERWISE SPECIFIED: $T_A = 25^oC$, $V_{SUPPLY} = +15V$, $V_{AH} = +4V$, $V_{AL} = 0.8V$

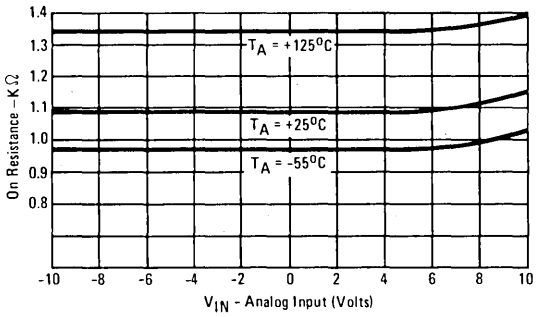
TEST CIRCUIT NO. 1

$R_{ON} = \frac{V_2}{100\mu A}$

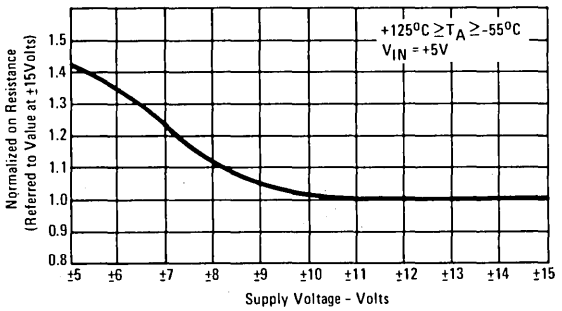


ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE

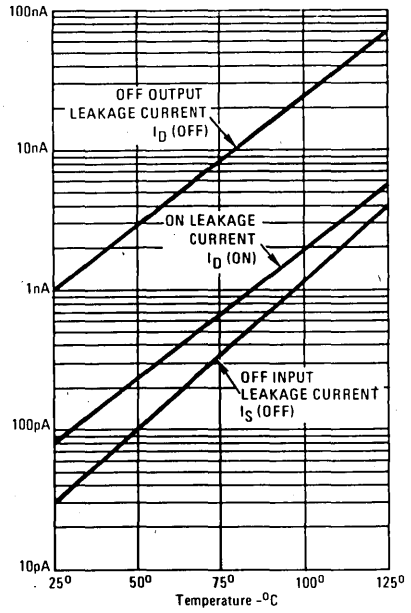
ON RESISTANCE vs. ANALOG INPUT VOLTAGE



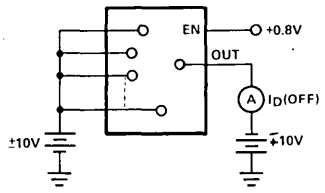
NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE



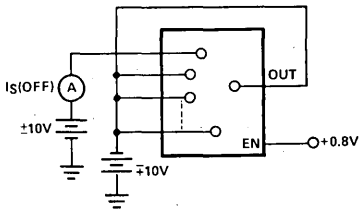
LEAKAGE CURRENT vs. TEMPERATURE



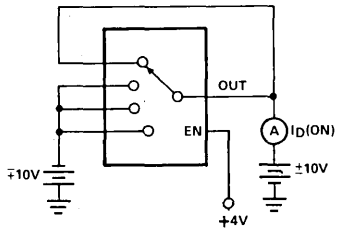
TEST CIRCUIT NO. 2*



TEST CIRCUIT NO. 3*

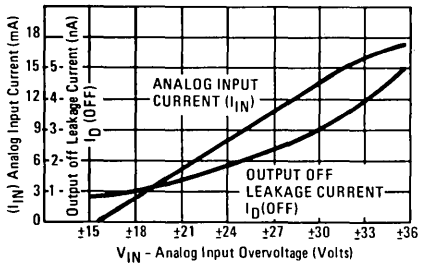


TEST CIRCUIT NO. 4*



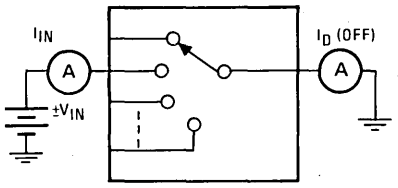
***Two measurements per channel: +10V/-10V and -10V/+10V. (Two measurements per device for $I_{D(OFF)}$: +10V/-10V and -10V/+10V.)**

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



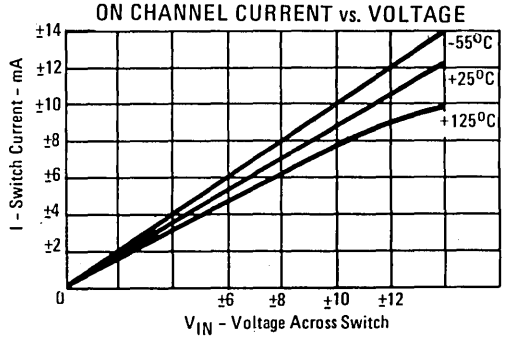
TEST CIRCUIT NO. 5

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



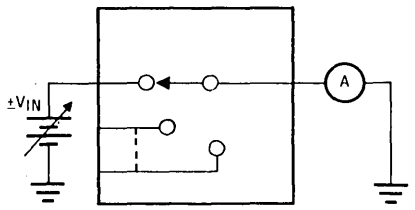
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (continued)

ON CHANNEL CURRENT vs. VOLTAGE

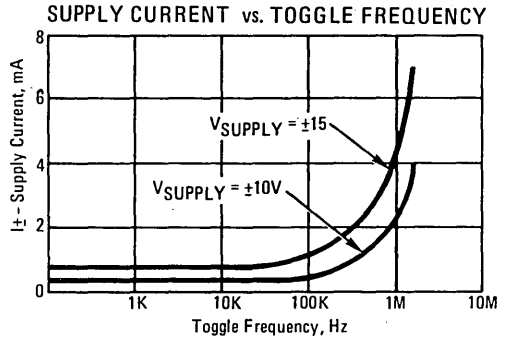


TEST CIRCUIT NO. 6

ON CHANNEL CURRENT vs. VOLTAGE

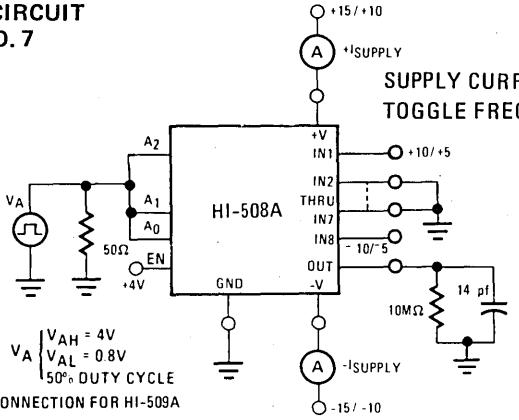


SUPPLY CURRENT vs. TOGGLE FREQUENCY



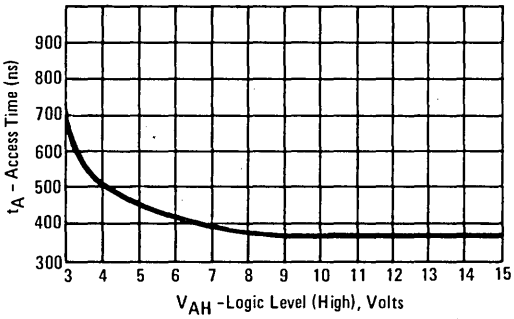
TEST CIRCUIT NO. 7

SUPPLY CURRENT vs. TOGGLE FREQUENCY



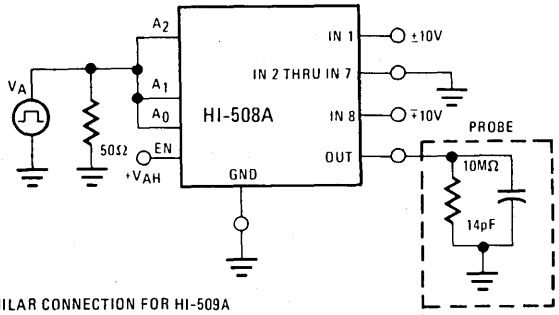
*SIMILAR CONNECTION FOR HI-509A

ACCESS TIME vs. LOGIC LEVEL (HIGH)



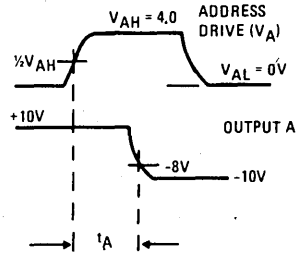
TEST CIRCUIT NO. 8

ACCESS TIME vs. LOGIC LEVEL(HIGH)

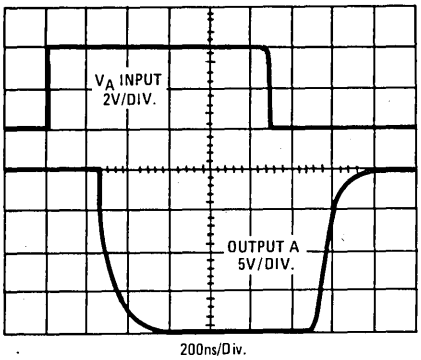


* SIMILAR CONNECTION FOR HI-509A

SWITCHING WAVEFORMS

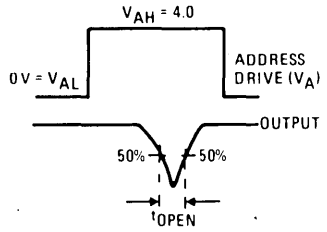


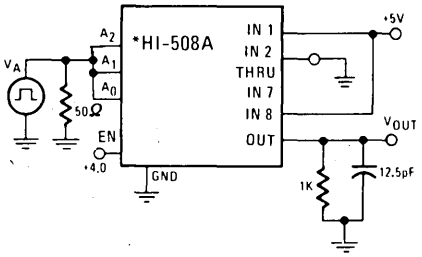
ACCESS TIME



SWITCHING WAVEFORMS (continued)

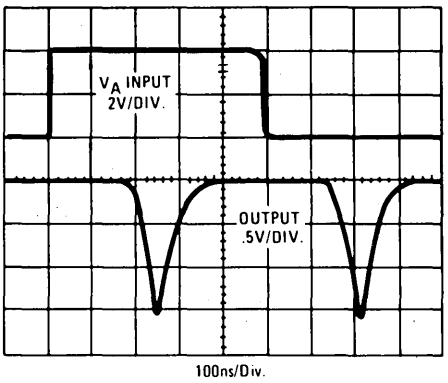
TEST CIRCUIT NO. 9
BREAK BEFORE MAKE DELAY (t_{OPEN})



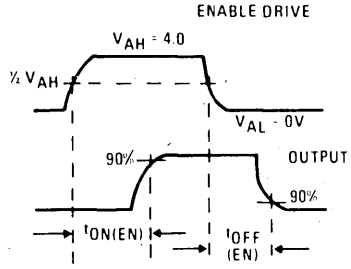


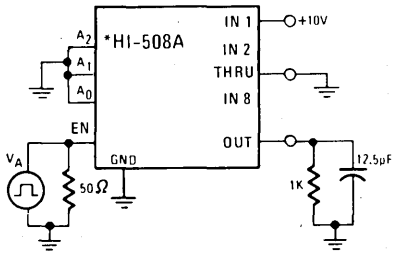
*SIMILAR CONNECTION FOR HI-509A

BREAK BEFORE MAKE DELAY (t_{OPEN})



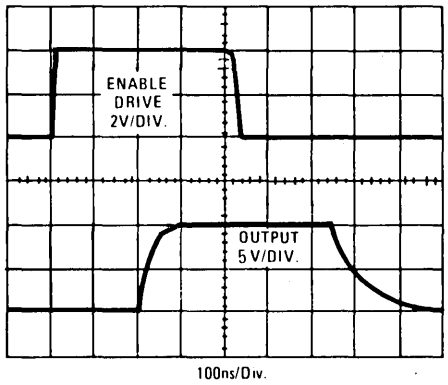
TEST CIRCUIT NO. 10
ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)



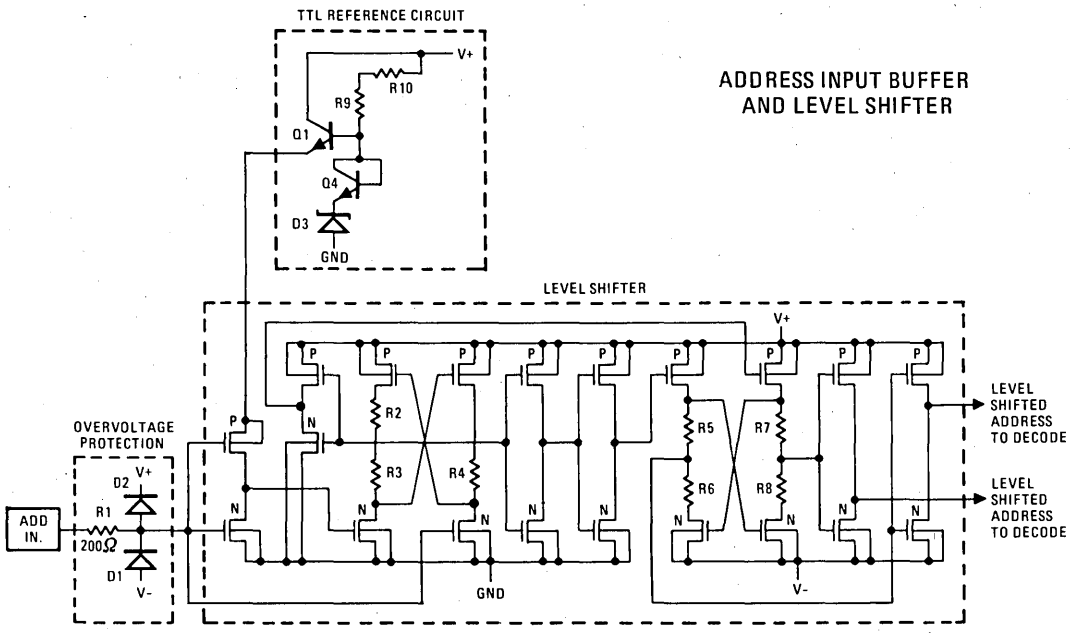


* SIMILAR CONNECTION FOR HI-509A

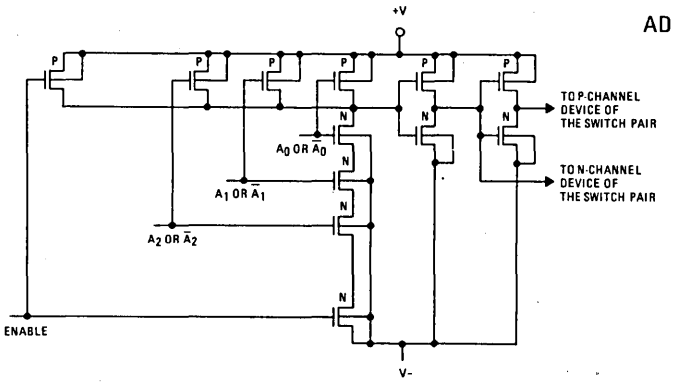
ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)



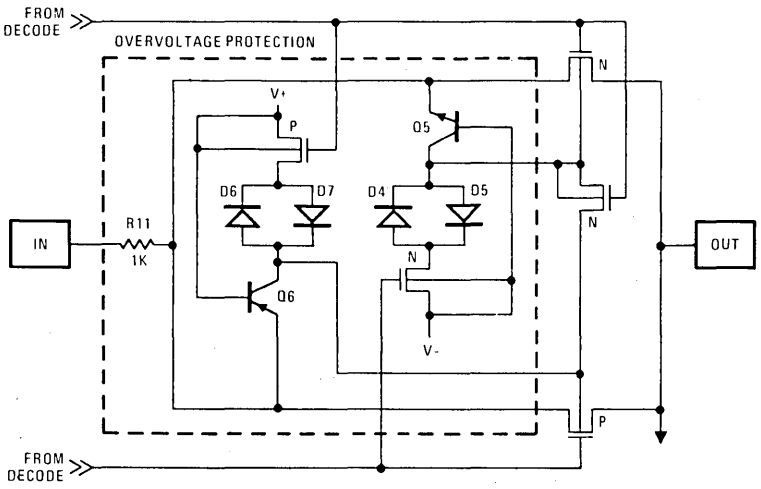
SCHEMATIC DIAGRAMS



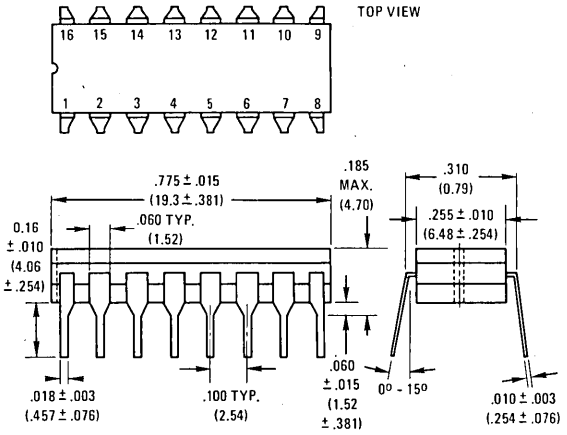
ADDRESS DECODER

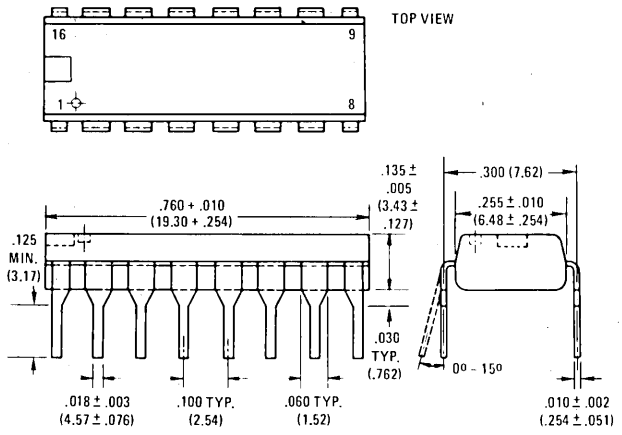


MULTIPLEX SWITCH



PACKAGING





1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions ±.010 (±0.25mm) unless otherwise shown.

ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMPERATURE RANGE	PRODUCT DESCRIPTION
HI1-508/509-1	-55°C to +200°C	Hi-Temp (Includes 160 hours Burn-In)
HI1-508/509-2	-55°C to +125°C	Military
HI1-508/509-5	0°C to +70°C	Commercial
HI1-508/509-6	0°C to +70°C	Unpackaged Chips
HI1-508/509-8	-55°C to +125°C	Screened per MIL-STD-883/5004/ Class B

SALES OFFICES

1503 SO. COAST DRIVE
SUITE 320
COSTA MESA, CA. 92626
(714) 540-2176

SUITE 115
2020 WEST McNAB ROAD
FT. LAUDERDALE, FL. 33309
(305) 971-3200

SUITE 273
555 BROAD HOLLOW ROAD
MELVILLE, N.Y. 11747
(516) 249-4500

17120 DALLAS PARKWAY
DALLAS, TX. 75248
(214) 934-4237

SUITE 300
625 ELLIS STREET
MOUNTAIN VIEW, CA. 94043
(415) 964-6443

415 WEST GOLF ROAD
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ARLINGTON HEIGHTS, IL. 60005
(312) 437-4712

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KETTERING, OH. 45429
(513) 433-5770

33919 NINTH AVE. SOUTH
FEDERAL WAY, WA. 98003
(206) 838-4878

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WOODLAND HILLS, CA. 91364
(213) 992-0686

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177 WORCESTER STREET
WELLESLEY HILLS, MA. 02181
(617) 237-5430

SUITE 325
650 E. SWEDESFORD ROAD
WAYNE, PA. 19087
(215) 687-6680

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PRODUCTS DIVISION
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HARRIS

HI-516

16 Channel/Differential 8 Channel CMOS High Speed Analog Multiplexer

FEATURES

- ACCESS TIME (TYP) 100ns
- SETTLING TIME (TYP TO 0.01%) 800ns
- LOW LEAKAGE I_S OFF 10pA
  I_D OFF 35pA
- LOW CAPACITANCE C_S OFF 2.5pF
  C_D OFF 18pF
- HIGH OFF ISOLATION AT 1MHz 80dB
- LOW CHARGE INJECTION 0.3pC
- SINGLE ENDED TO DIFFERENTIAL SELECTABLE (SDS)
- LOGIC LEVEL SELECTABLE (LLS)

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- PRECISION INSTRUMENTATION
- INDUSTRIAL CONTROL

DESCRIPTION

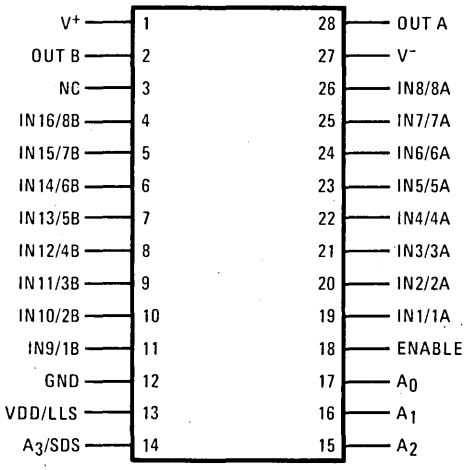
The HI-516 is a monolithic dielectrically isolated, high speed, high performance CMOS analog multiplexer. It offers unique built-in channel selection decoding plus an inhibit input for disabling all channels. The dual function of address input A_3 enables the HI-516 to be user programmed either as a single ended 16-channel multiplexer by connecting 'out A' to 'out B' and using A_3 as a digital address input, or as an 8-channel differential multiplexer by connecting A_3 to the V^- supply. The substrate leakages and parasitic capacitances are reduced substantially using the Harris dielectric isolation process to achieve optimum performances in both high and low level signal applications. The low output leakage current (I_D Off < 100pA @ 25°C) and fast settling (t_{SETTLE} = 800ns to 0.01%) characteristics of the device make it an ideal choice for high speed data acquisition systems, precision instrumentation, and industrial process controls.

The HI-516 is available in a 28 lead dual-in-line package. HI-516-5 is specified for operation over 0°C to +75°C, and the HI-516-2 over -55°C to +125°C. Processing to MIL-STD-883A, Class B screening is available by selecting the HI-516-8.

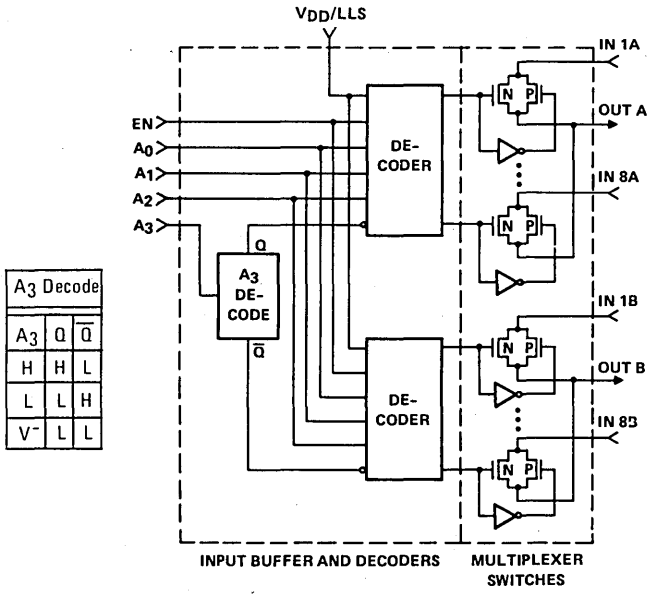
PINOUT

Section 11 for Packaging

TOP VIEW



FUNCTIONAL DIAGRAM



A_3 Decode		
A_3	Q	$\overline{Q}$
H	H	L
L	L	H
V^-	L	L

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Digital Input Overvoltage:

TTL	-6V < V_{AH} < +6V	
	A2 V_{SUPPLY} (-)	-2V
CMOS	V_{SUPPLY}(+)	+2V
	GND	-2V

Analog Input Voltage:

V_S	V_{SUPPLY}(+)	+2V
	V_{SUPPLY}(-)	-2V

Voltage Between Supply Pins	33V
Total Power Dissipation*	1200mW
Operating Temperature Ranges:	
HI-516-2	-55°C to +125°C
HI-516-5	0°C to 75°C
Storage Temperature Range	-65°C to 150°C
*Derate 8mW/°C above t_A	75°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified) Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} (Logic Level Low) = +0.8V; V_{DD}/LLS = Open (Note 6)

PARAMETER	TEMP	-55°C to +125°C MIN	TYP	MAX	0°C to +75°C MIN	TYP	MAX	UNITS
ANALOG CHANNEL CHARACTERISTICS								
V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
R_{ON}, On Resistance (Note 1)	+25°C		620	750		620	750	Ω
	Full		770	1,000		700	1,000	Ω
I_S (OFF), Off Input Leakage Current	+25°C		0.01			0.01		nA
	Full		0.38	50		0.38	50	nA
I_D(OFF), Off Output Leakage Current	+25°C		0.035			0.035		nA
	Full		0.48	100		0.48	100	nA
I_D(ON), On Channel Leakage Current	+25°C		0.04			0.04		nA
	Full		0.56	100		0.56	100	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL} Input Low Threshold (TTL)	Full			0.8			0.8	V
V_{AH} Input High Threshold (TTL)	Full	2.4			2.4			V
V_{AH} Input Low Threshold (CMOS)	Full			$0.3V_{DD}$			$0.3V_{DD}$	V
V_{AH} Input High Threshold (CMOS)	Full	$0.7V_{DD}$			$0.7V_{DD}$			V
I_{AH} Input Leakage Current (High)	Full		0.05	1		0.05	1	μA
I_{AL} Current (Low)	Full		4	25		4	25	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		100	150		100	150	ns
	Full		120	200		120	200	ns
t_{OPEN}, Break before make delay	+25°C		20			20		ns
t_{ON}(EN), Enable Delay (IN)	+25°C		100	150		100		ns
t_{OFF}(EN), Enable Delay (OFF)	+25°C		80	125		80		ns
Settling Time (0.1%)	+25°C		250			250		ns
(0.01%)	+25°C		800			800		ns
Charge Injection (Note 2)	+25°C		0.33			0.33		pC
Off Isolation (Note 3)	+25°C		90			90		dB
C_S(OFF), Channel Input Capacitance	+25°C		2.5			2.5		pF
C_D(OFF), Channel Output Capacitance	+25°C		18			18		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
C_{DS}(OFF), Input to Output Capacitance	+25°C		0.02			0.02		pF
POWER REQUIREMENTS								
PD, Power Dissipation	Full		525			525		mW
I^+, Current (Note 4)	Full		17.5	25		17.5	30	mA
I^-, Current (Note 4)	Full		17.5	25		17.5	30	mA
I^+, Standby (Note 5)	Full		17.0	25		17.0	30	mA
I^-, Standby (Note 5)	Full		17.0	25		17.0	30	mA

NOTES:

1. V_{IN} = ±10V, I_{OUT} = -100μA
2. V_{IN} = 0V, C_L = 100pF, Enable input pulse = 3V, f = 500kHz
3. V_{EN} = 0.8V, V_S = $3V_{RMS}$, f = 500kHz, C_L = 40pF, R_L = 1k, Pin 3 grounded
4. V_{EN} = +2.4V
5. V_{EN} = 0.8V
6. V_{DD}/LLS Pin = Open or Grounded for TTL Compatibility
   V_{DD}/LLS Pin = V_{DD} for CMOS Compatibility

HI-516 USED AS A 16-CHANNEL MULTIPLEXER OR 8 CHANNEL DIFFERENTIAL MULTIPLEXER *

USE A_3 AS DIGITAL ADDRESS INPUT					ON CHANNEL TO	
ENABLE	A_3	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	X	NONE	NONE
H	L	L	L	L	1A	NONE
H	L	L	L	H	2A	NONE
H	L	L	H	L	3A	NONE
H	L	L	H	H	4A	NONE
H	L	H	L	L	5A	NONE
H	L	H	L	H	6A	NONE
H	L	H	H	L	7A	NONE
H	L	H	H	H	8A	NONE
H	H	L	L	L	NONE	1B
H	H	L	L	H	NONE	2B
H	H	L	H	L	NONE	3B
H	H	L	H	H	NONE	4B
H	H	H	L	L	NONE	5B
H	H	H	L	H	NONE	6B
H	H	H	H	L	NONE	7B
H	H	H	H	H	NONE	8B

* For 16-Channel single-ended function, tie 'out A' to 'out B', for dual 8-channel function use the A_3 address pin to select between MUX A and MUX B, where MUX A is selected with A_3 low.

HI-516 USED AS A DIFFERENTIAL 8-CHANNEL MULTIPLEXER

A_3 CONNECT TO V⁻ SUPPLY				ON CHANNEL TO	
ENABLE	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	NONE	NONE
H	L	L	L	1A	1B
H	L	L	H	2A	2B
H	L	H	L	3A	3B
H	L	H	H	4A	4B
H	H	L	L	5A	5B
H	H	L	H	6A	6B
H	H	H	L	7A	7B
H	H	H	H	8A	8B

HARRIS

HI-518

8 Channel/Differential 4 Channel CMOS High Speed Analog Multiplexer

FEATURES

- ACCESS TIME (TYP) 80ns
- SETTLING TIME (0.1%) 250ns
- LOW LEAKAGE I_S (OFF) 50pA
  I_D (OFF) 100pA
- LOW CAPACITANCE (TYP) C_S (OFF) 2pF
  C_D (OFF) 10pF
- HIGH OFF ISOLATION @ (1MHz) 75dB
- SINGLE ENDED TO DIFFERENTIAL MODE SELECTABLE (SDS)
- LOGIC LEVEL SELECTABLE (LLS)
- LOW CHARGE INJECTION 0.3pC

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- INDUSTRIAL CONTROLS
- TELEMETRY

DESCRIPTION

The HI-518 is a monolithic, high performance, high speed Analog Multiplexer, constructed utilizing the Harris Dielectrically isolated CMOS process.

This device has the added feature that it can be user programmed either as a single ended 8-channel multiplexer by connecting 'out A' to 'out B' and using A2 as a digital address input, or as a 4-channel differential multiplexer by connecting A2 to the V^- supply.

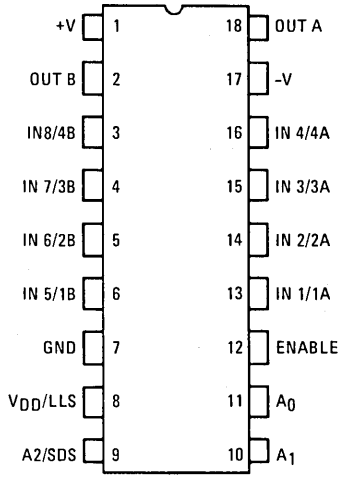
TTL or CMOS compatibility is also selectable. Low leakage current, I_D off < 100pA @ 25°C, and fast settling, 250ns to 0.1%, characteristics of this device make it an ideal choice for high speed data acquisition systems, precision instrumentation and industrial process controls.

The HI-518 is available in an 18 lead Dual-in-Line Package. The HI-518-5 is specified for operation over 0°C to +75°C, and the HI-518-2 over -55°C to +125°C. Processing to MIL-STD-883A Class B screening is available by selecting the HI-518-8.

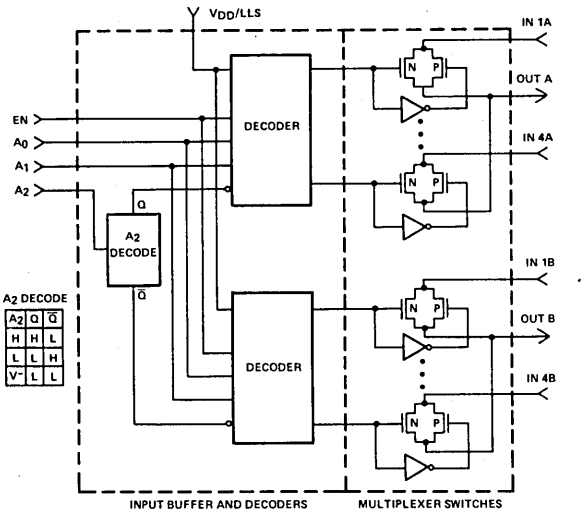
PINOUT

Section 11 for Packaging

TOP VIEW



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Digital Input Overvoltage:

TTL	$-6V < V_{AH} < +6V$	
	A2 V_{SUPPLY} (-)	-2V
CMOS	V_{SUPPLY}(+)	+2V
	GND	-2V

Analog Input Voltage:

V_S	V_{SUPPLY}(+)	+2V
	V_{SUPPLY}(-)	-2V

Voltage Between Supply Pins	33V
Total Power Dissipation*	725mW
Operating Temperature Ranges:	
HI-518-2	-55°C to +125°C
HI-518-5	0°C to 75°C
Storage Temperature Range	-65°C to 150°C
*Derate 8mW/°C above t_A	75°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified) Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} (Logic Level Low) = +0.8V; V_{DD}/LLS = Open (Note 6).

PARAMETER	TEMP	-55°C to +125°C MIN	TYP	MAX	0°C to +75°C MIN	TYP	MAX	UNITS
ANALOG CHANNEL CHARACTERISTICS								
V_S Analog Signal Range	Full	-15		+15	-15		+15	V
R_{ON} On Resistance (Note 1)	+25°C		480	750		480	750	Ω
	Full		700	1000		700	1000	Ω
I_S (OFF) Off Input	+25°C		0.05			0.05		nA
Leakage Current	Full		0.60	50		0.60	50	nA
I_D (OFF) Off Output	+25°C		0.10			0.10		nA
Leakage Current	Full		0.30	50		0.30	50	nA
I_D (ON) On Channel	+25°C		0.10			0.10		nA
Leakage Current	Full		0.30	50		0.30	50	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL} Input Low Threshold (TTL)	Full			0.8			0.8	V
V_{AH} Input High Threshold (TTL)	Full	2.4			2.4			V
V_{AL} Input Low Threshold (CMOS)	Full			$0.3V_{DD}$			$0.3V_{DD}$	V
V_{AH} Input High Threshold (CMOS)	Full	$0.7V_{DD}$			$0.7V_{DD}$			V
I_{AH} Input Leakage Current (High)	Full		0.05	1		0.05	1	μA
I_{AH} Input Leakage Current (Low)	Full		4	20		4	20	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		80	125		80	125	
	Full		110	150		110	150	ns
t_{OPEN}, Break before make Delay	+25°C		20			20		ns
t_{ON} (EN), Enable Delay (ON)	+25°C		80	150		80	150	ns
t_{OFF} (EN), Enable Delay (OFF)	+25°C		60	125		60	125	ns
Settling Time (0.1%)	+25°C		250			250		ns
(0.01%)	+25°C		800			800		
Charge Injection (Note 2)	+25°C		0.3			0.3		pC
Off Isolation (Note 3)	+25°C		86			86		dB
C_S (OFF) Channel Input Capacitance	+25°C		1.9			1.9		pF
C_D (OFF) Channel Output Capacitance	+25°C		10			10		pF
C_A, Digital Input Capacitance	+25°C		3			3		pF
CDS (OFF) Input to Output Capacitance	+25°C		0.02			0.02		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		360	450		360	540	mW
I+, Current (Note 4)	Full		12	15		12	18	mA
I⁻, Current (Note 4)	Full		12	15		12	18	mA
I+, Standby (Note 5)	Full		11.5	15		11.5	18	mA
I⁻, Standby (Note 5)	Full		11.5	15		11.5	18	mA

NOTES:

1. $V_{IN} = \pm 10V$, $I_{OUT} = -100\mu A$
2. $V_{IN} = 0V$, $C_L = 100pF$, Enable Input pulse = 3V, f = 500kHz.
3. $V_{EN} = 0.8V$, $V_S = 3VRMS$, f = 500kHz, $C_L = 40pF$, $R_L = 1k$. Due to the pin to pin capacitance between IN 8/4B (Pin 3) and Out B (Pin 2) channel 8/4B exhibits 60dB of Off Isolation under the above test conditions.
4. $V_{EN} = +2.4V$.
5. $V_{EN} = 0.8V$.
6. VDD/LLS Pin = Open or grounded for TTL compatibility. VDD/LLS Pin = V_{DD} for CMOS compatibility.

TRUTH TABLES

HI-518 USED AS 8 CHANNEL MULTIPLEXER OR
4 CHANNEL DIFFERENTIAL MULTIPLEXER

USE A_2 AS DIGITAL ADDRESS INPUT				ON CHANNEL TO	
ENABLE	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	NONE	NONE
H	L	L	L	1A	NONE
H	L	L	H	2A	NONE
H	L	H	L	3A	NONE
H	L	H	H	4A	NONE
H	H	L	L	NONE	1B
H	H	L	H	NONE	2B
H	H	H	L	NONE	3B
H	H	H	H	NONE	4B

HI-518 USED AS DIFFERENTIAL
4 CHANNEL MULTIPLEXER

A_2 CONNECT TO V^- SUPPLY			ON CHANNEL TO	
ENABLE	A_1	A_0	OUT A	OUT B
L	X	X	NONE	NONE
H	L	L	1A	1B
H	L	H	2A	2B
H	H	L	3A	3B
H	H	H	4A	4B

HARRIS

HI-524

4 Channel Video Multiplexer

FEATURES

- CROSSTALK (10MHz) > 60dB
- FAST ACCESS TIME 150ns
- FAST SETTLING TIME (0.01%) 600ns
- TTL COMPATIBLE

APPLICATIONS

WIDEBAND SWITCHING

- RADAR
- TV VIDEO
- ECM

DESCRIPTION

The HI-524 is a four channel CMOS analog multiplexer designed to process single-ended video signals with bandwidths up to 10MHz. The chip includes a 1 of 4 decoder for channel selection and an Enable input to inhibit all channels (chip select).

Three CMOS transmission gates are used in each channel, as compared to the single gate in more conventional CMOS multiplexers. This provides a double barrier to the unwanted coupling of signals from each input to the output. In addition, Dielectric Isolation (DI) processing helps to insure that Crosstalk exceeds 60dB at 10MHz.

The HI-524 is designed to operate into a wideband buffer amplifier such as the HARRIS HA-5190. The multiplexer chip includes two "on" switches in series, for use as a feedback element with the amplifier. This feedback resistance matches and tracks the channel R_{ON} resistance, to minimize the amplifier V_{OS} and its variation with temperature.

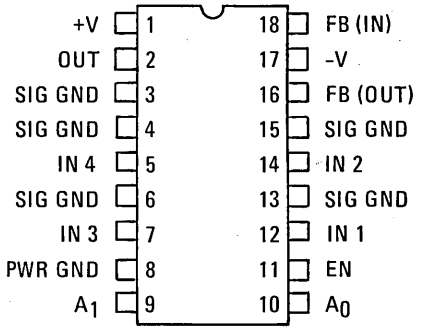
The HI-524 is well suited to the rapid switching of video signals in telemetry, instrumentation, radar and video systems. It is packaged in an 18 pin ceramic DIP and operates on ±15V supplies.

The performance levels available are: HI1-524-2, -55°C to +125°C operating range; HI1-524-5, 0°C to +75°C operating range and HI1-524-8, -55°C to +125°C operating range plus 100% screening per MIL-STD-883/Method 5004/Class B. Chips for hybrid applications are designated HI0-524-6.

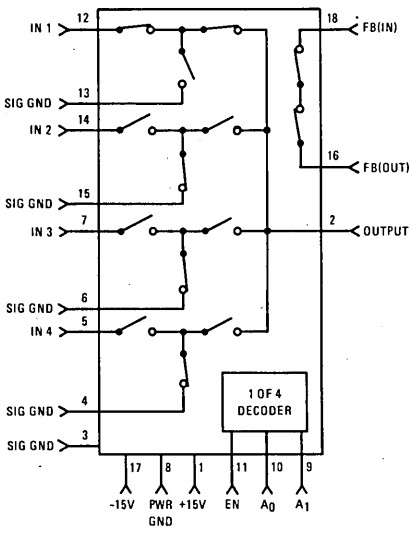
PINOUT

Section 11 for Packaging

TOP VIEW



FUNCTIONAL DIAGRAM



TRUTH TABLE

A_1	A_0	EN	ON CHANNEL
X	X	L	NONE
L	L	H	1*
L	H	H	2
H	L	H	3
H	H	H	4

*CHANNEL 1 IS SHOWN SELECTED IN THE DIAGRAM

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Digital Input Overvoltage:
$-6V < V_{AH} < +6V$

Analog Input (V_S) or Output (V_O)
$+V_{SUPPLY}$ +2V
$-V_{SUPPLY}$ -2V

Voltage Between Supply Pins	33V
Either Supply to Ground	16.5V
Total Power Dissipation	750mW
Operating Temperature Range:	
HI-524-2, -8	-55°C to +125°C
HI-524-5	0°C to 75°C
Storage Temperature Range	-65°C to 150°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified) Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} = (Logic Level Low) = +0.8V; V_{EN} = +2.4V

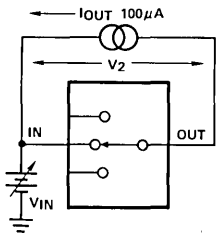
PARAMETER	TEMP	HI-524-2, -8 -55°C to +125°C MIN	TYP	MAX	HI-524-5 0°C to +75°C MIN	TYP	MAX	UNITS
Analog Channel Characteristics								
V_S, Analog Signal Range	Full	-10		+10	-10		+10	V
R_{ON}, On Resistance (Note 1)	+25°C		700			700		Ω
	Full			1.5K			1.5K	Ω
I_S (OFF), Off Input Leakage Current (Note 2)	+25°C		0.2			0.2		nA
	Full			50			50	nA
I_D (OFF), Off Output Leakage Current (Note 2)	+25°C		0.2			0.2		nA
	Full			50			50	nA
I_D (ON), On Channel Leakage Current (Note 2)	+25°C		0.7			0.7		nA
	Full			50			50	nA
3dB Bandwidth: (Note 3)	Full		20			20		MHz
Digital Input Characteristics								
V_{AL} Input Low Threshold (TTL)	Full			0.8			0.8	V
V_{AH} Input High Threshold (TTL)	Full	2.4			2.4			V
I_{AH} Input Leakage Current (High)	Full		0.05	1		0.05	1	μA
I_{AL} Current (Low)	Full		4	25		4	25	μA
Switching Characteristics								
t_A, Access Time (Note 4)	+25°C		150	300		150	300	ns
	Full							ns
t_{OPEN}, Break before make delay (Note 4)	+25°C		20			20		ns
t_{ON} (EN), Enable Delay (ON), R_L = 500Ω	+25°C		180	300		180		ns
t_{OFF} (EN), Enable Delay (OFF), R_L = 500Ω	+25°C		180	250		180		ns
Settling Time (0.1%) (Note 4)	+25°C		200			200		ns
(0.01%)	+25°C		600			600		ns
Crosstalk (Note 5)	+25°C		-65			-65		dB
C_S (OFF), Channel Input Capacitance	+25°C			6		6		pF
C_D (OFF), Channel Output Capacitance	+25°C			4		4		pF
C_A, Digital Input Capacitance	+25°C			5		5		pF
Power Requirements								
P_D, Power Dissipation	Full		540			540		mW
I^+, Current (V_{EN} = 2.4V) (Note 6)	Full		18	25		18	25	mA
I^-, Current (V_{EN} = 2.4V) (Note 6)	Full		18	25		18	25	mA
I^+, Standby (V_{EN} = 0.8V) (Note 6)	Full		18	25		18	25	mA
I^-, Standby (V_{EN} = 0.8V) (Note 6)	Full		18	25		18	25	mA

1. V_{IN} = 0V; I_{OUT} = 100 A (See Test Circuit # 1)
2. $V_O = \pm 10V$; $V_S = \mp 10V$ (See Test Circuits # 2, 3, 4)
3. MUX output is buffered with HA-5190 as shown in Applications section.
4. (See Test Circuit # 5)
5. V_{IN} = 10MHz, $3V_{p-p}$ on one channel, with any other channel selected. (Worst case is channel 3 selected with input on channel 4.) MUX output is buffered with HA-5190 as shown in Applications section. Terminate all channels with 75Ω.
6. Supply currents vary less than 0.5mA for switching rates from DC to 2MHz.

(UNLESS OTHERWISE SPECIFIED T_A = 25°C, V_{SUPPLY} = ±15V, V_{AH} = 2.4V, V_{AL} = 0.8V)

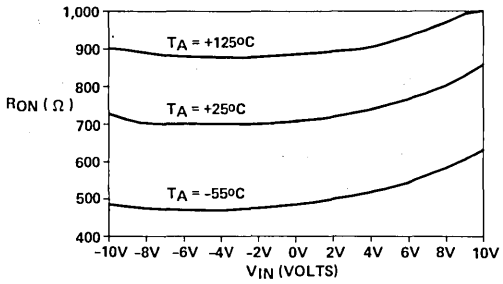
ON RESISTANCE

TEST CIRCUIT NO. 1

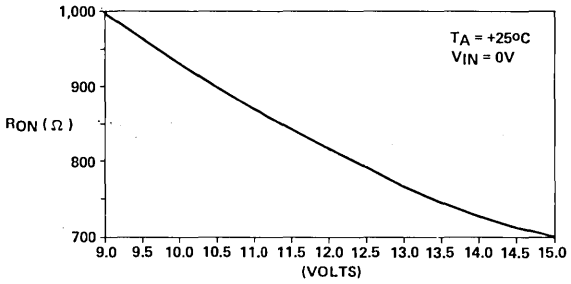


$$R_{ON} = \frac{V_2}{100\mu A}$$

ON RESISTANCE VS. ANALOG INPUT VOLTAGE

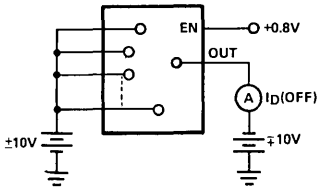


ON RESISTANCE VS. SUPPLY VOLTAGE



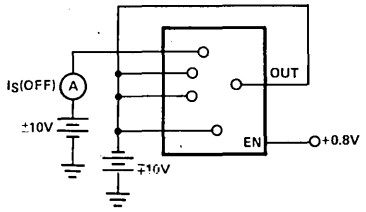
LEAKAGE CURRENT

TEST CIRCUIT NO. 2*

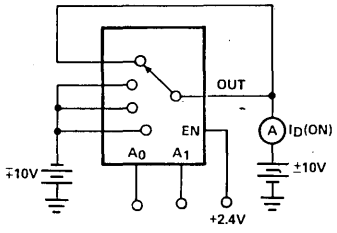


*Two measurements per channel:
+10V/-10V and -10V/+10V.
(Two measurements per device for $I_{D(OFF)}$:
+10V/-10V and -10V/+10V.)

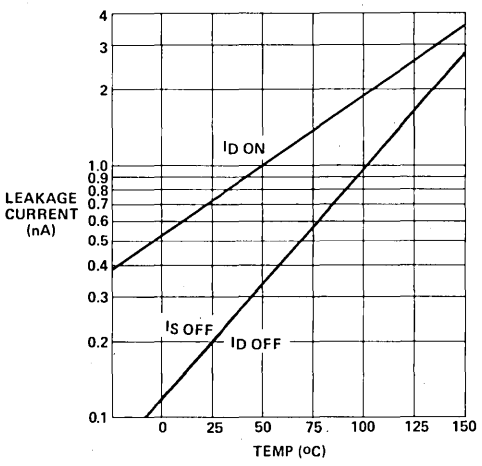
TEST CIRCUIT NO. 3*



TEST CIRCUIT NO. 4*

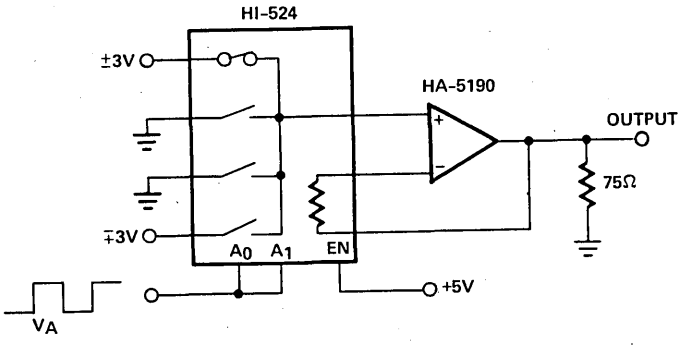


LEAKAGE CURRENT VS. TEMPERATURE

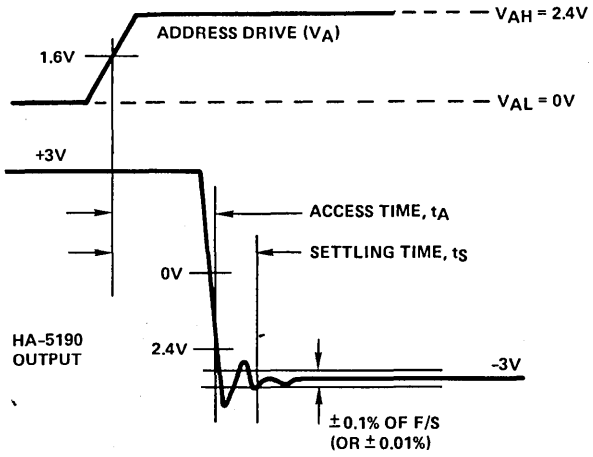


TEST CIRCUIT NO. 5

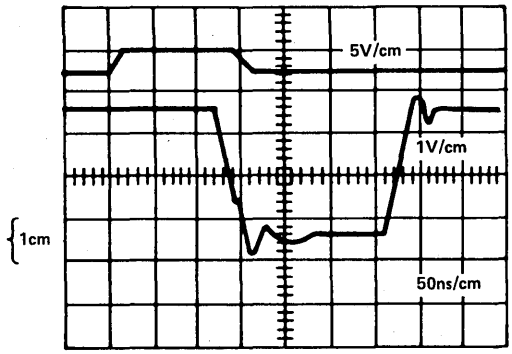
SETTLING TIME
ACCESS TIME
BREAK-BEFORE-MAKE DELAY



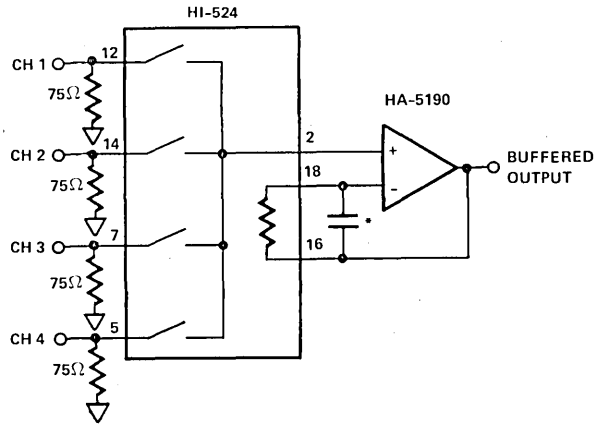
(USE DIFFERENTIAL COMPARATOR PLUG-IN ON SCOPE FOR SETTLING TIME MEASUREMENT.)



ACCESS TIME



- Often it is desirable to buffer the HI-524 output, to avoid loading errors due to the channel "ON" resistance:



* APPROXIMATELY 10pF SHOULD REMOVE ANY LOW LEVEL INSTABILITY AT THE OUTPUT.

- The main requirement for the buffer amplifier is a full power bandwidth high enough to avoid attenuation of the video signal. The HARRIS HA-5190 is well suited for this purpose; in fact the HI-524 was designed to be compatible with the 5190. This 524/5190 combination offers a 3dB bandwidth of at least 20MHz for a 3V peak-to-peak input. As mentioned earlier, the 524 includes a feedback element for the amplifier which matches and tracks the channel "ON" resistance.

- Note that the on-chip feedback element between pins 16 and 18 includes two switches in series, to simulate a channel resistance. These switches open for V_{EN} = Low. This allows two or more HI-524's to operate into one HA-5190, with their feedback elements connected in parallel. Thus, only the selected multiplexer provides feedback, and the amplifier remains stable.

- All HI-524 package pins labeled 'SIG GND' (pins 3, 4, 6, 13, 15) should be externally connected to signal ground for best Crosstalk performance.

- Bypass capacitors (0.1 to 1.0μF) are recommended from each HI-524 supply pin to power ground (pins 1 and 17 to pin 8). Locate the buffer amplifier near the HI-524 so the two capacitors may bypass both devices.

- If an analog input 1V or greater is present when supplies are off, a low resistance is seen from that input to a supply line. (For example, the resistance is approximately 160Ω for an input of -3V.) Current flow may be blocked by a diode in each supply line, or limited by a resistor in series with each channel. The best solution, of course, is to arrange that no digital or analog inputs are present when the power supplies are off.

HARRIS

HI-539

Monolithic, Four Channel, Low Level, Differential Multiplexer

FEATURES

- DIFFERENTIAL PERFORMANCE, TYP.:
  - LOW ΔR_{ON}, +125°C — 5.5Ω
  - LOW $\Delta I_{D(ON)}$, +125°C — 0.6nA
  - LOW Δ(CHARGE INJECTION) — 0.1pC
  - LOW CROSSTALK — -120dB
- SETTLING TIME, ±0.01% — 900ns
- WIDE SUPPLY RANGE — ±5V TO ±18V
- BREAK-BEFORE-MAKE SWITCHING
- NO LATCH-UP

APPLICATIONS

- LOW LEVEL DATA ACQUISITION
- PRECISION INSTRUMENTATION
- TEST SYSTEMS

DESCRIPTION

The Harris HI-539 is a monolithic, four channel, differential multiplexer. Two digital inputs are provided for channel selection, plus an Enable input to disconnect all channels.

Performance is guaranteed for each channel over the range ± 10V, but is optimized for low level differential signals. Leakage current, for example, which varies slightly with input voltage, has its distribution centered at zero for zero input volts.

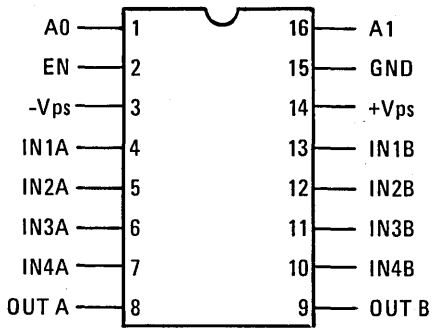
In most monolithic multiplexers, the net differential offset due to thermal effects becomes significant for low level signals. This problem is minimized in the HI-539 by symmetrical placement of critical circuitry with respect to the few heat producing devices.

The HI-539 will be offered in both commercial and military temperature ranges, with screening available for MIL-STD-883, Class B. Supply voltages are ± 15V and power consumption is only 2.5mW. The package is a 16 pin ceramic DIP.

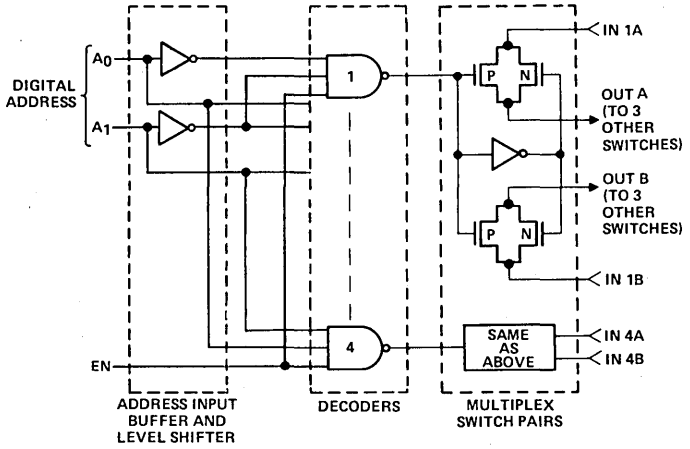
PINOUT

Section 11 for Packaging

TOP VIEW



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Voltage Between Supply Pins (V_{PS+}, V_{PS-}) 40V

Voltage from either Supply to Ground 20V

Analog Input Voltage, V_S $V_{PS-} \leq V_S \leq V_{PS+}$

Digital Input Voltage, V_A $V_{PS-} \leq V_A \leq V_{PS+}$

Storage Temperature Range -65°C to +150°C

Internal Power Dissipation (Derate 8mW/°C above +75°C ambient) 725mW

Operating Temperature Range

HI-539-2, -8 -55°C to +125°C

HI-539-4 -25°C to +85°C

HI-539-5 0°C to +75°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified) Supplies = ± 15V, V_{EN} = +4.0V, V_{AH} (Logic Level High) = +4.0V, V_{AL} (Logic Level Low) = +0.8V. See the Performance Characteristics Section for test circuits and conditions. Selected parameters are defined in the Definitions Section.

PARAMETER	TEMP	HI-539-2, -8		HI-539-4, -5		UNITS
		TYP	MAX (MIN)	TYP	MAX (MIN)	
ANALOG CHANNEL CHARA'S						
V_S, Analog Signal Range	Full		(-10)/+10		(-10)/+10	V
R_{ON}, On Resistance V_{IN} = 0V	+25°C	650	850	650	850	Ω
V_{IN} = ± 10V	+25°C	700	900	700	900	Ω
V_{IN} = 0V	Full	950	1.3K	800	1K	Ω
V_{IN} = ± 10V	Full	1.1k	1.4k	900	1.1k	Ω
ΔR_{ON} [Side A - Side B]						
V_{IN} = 0V	+25°C	4.0	24	4.0	24	Ω
V_{IN} = ± 10V	+25°C	4.5	27	4.5	27	Ω
V_{IN} = 0V	Full	4.75	28	4.0	24	Ω
V_{IN} = ± 10V	Full	5.5	33	4.5	27	Ω
$I_{S(OFF)}$, Off Input Leakage Current (Note 1)						
Condition 0V	+25°C	30	200	30	200	pA
Condition ± 10V	+25°C	100		100		pA
Condition 0V	Full	2	10	0.2	1	nA
Condition ± 10V	Full	5	25	0.5	2.5	nA
$\Delta I_{S(OFF)}$, [Side A - Side B]						
Condition 0V	+25°C	3	100	3	100	pA
Condition ± 10V	+25°C	10		10		pA
Condition 0V	Full	0.2	2	0.02	0.2	nA
Condition ± 10V	Full	0.5	5	0.05	0.5	nA
$I_{D(OFF)}$, Off Output Leakage Current (Note 1)						
Condition 0V	+25°C	30	200	30	200	pA
Condition ± 10V	+25°C	100		100		pA
Condition 0V	Full	2	10	0.2	1	nA
Condition ± 10V	Full	5	25	0.5	2.5	nA
$\Delta I_{D(OFF)}$, [Side A - Side B]						
Condition 0V	+25°C	3	100	3	100	pA
Condition ± 10V	+25°C	10		10		pA
Condition 0V	Full	0.2	2	0.02	0.2	nA
Condition ± 10V	Full	0.5	5	0.05	0.5	nA
$I_{D(ON)}$, On Channel Leakage Current (Note 1)						
Condition 0V	+25°C	50	200	50	200	pA
Condition ± 10V	+25°C	150		150		pA
Condition 0V	Full	5	25	0.5	2.5	nA
Condition ± 10V	Full	6	40	0.8	4.0	nA
$\Delta I_{D(ON)}$ [Side A - Side B]						
Condition 0V	+25°C	10	100	10	100	pA
Condition ± 10V	+25°C	30		30		pA
Condition 0V	Full	0.5	5	0.05	0.5	nA
Condition ± 10V	Full	0.6	6	0.08	0.8	nA
ΔV_{OS}, Differential Offset Voltage	+25°C	0.02	0.04	0.02	0.04	μV
	Full	0.70	10	0.08	1.0	μV

SPECIFICATIONS (Continued)

PARAMETER	TEMP	HI-539-2, -8 TYP	HI-539-2, -8 MAX (MIN)	HI-539-4, -5 TYP	HI-539-4, -5 MAX (MIN)	UNITS
DIGITAL INPUT CHARACTERISTICS						
V_{AL}, Input Low Threshold	Full		0.8		0.8	V
V_{AH}, Input High Threshold	Full		(4.0)		(4.0)	V
I_{AH}, Input Leakage Current (High)	Full		1		1	μA
I_{AL}, Input Leakage Current (Low)	Full		1		1	μA
SWITCHING CHARACTERISTICS						
T_A, Access Time	+25°C	250	750	250	750	ns
	Full	450	1,000	450	1,000	ns
T_{open}, Break-Before-Make Delay	+25°C	85	(30)	85	(30)	ns
	Full		(30)		(30)	ns
$T_{ON(EN)}$, Enable Delay On	+25°C	250	750	250	750	ns
	Full		1,000		1,000	ns
$T_{OFF(EN)}$, Enable Delay Off	+25°C	160	650	160	650	ns
	Full		900		900	ns
Settling Time, to ±0.01%	+25°C	0.9		0.9		μs
Charge Injection (Output)	Full	3		3		pC
Δ Charge Injection (Output)	Full	0.1		0.1		pC
Charge Injection (Input)	Full	10		10		pC
Differential Crosstalk (Note 3)	+25°C	124		124		dB
Single Ended Crostalk (Note 3)	+25°C	100		100		dB
$C_{S(OFF)}$, Channel Input Capacitance	Full	5		5		pF
$C_{D(OFF)}$, Channel Output Capacitance	Full	7		7		pF
$C_{D(ON)}$, Channel On Output Capacitance	Full	17		17		pF
C_{DS}, Input to Output Capacitance (Note 4)	Full	0.08		0.08		pF
C_A, Digital Input Capacitance	Full	3		3		pF
POWER REQUIREMENTS						
P_D, Power Dissipation	+25°C	2.5		2.5		mW
	Full		45		45	mW
I+ Current	+25°C	0.150		0.150		mA
	Full		2.0		2.0	mA
I- Current	+25°C	0.001		0.001		mA
	Full		1.0		1.0	mA
± V, Supply Voltage Range	Full	±15	(±5)/ ±18	±15	(±5)/ ±18	V

NOTES

1. See Test Circuits #2, 3, 4. The condition ±10V means:
   $I_{S(OFF)}$ and $I_{D(OFF)}$: (V_S = +10V, V_D = -10V), then (V_S = -10V, V_D = +10V)
   $I_{D(ON)}$: (+10V, then -10V)
2. ΔV_{OS} (Exclusive of thermocouple effects) = $R_{ON}\,\Delta I_{D(ON)} + I_{D(ON)}\,\Delta R_{ON}$.
   See Applications section for discussion of additional V_{OS} error.
3. V_{IN} = 1kHz, $15V_{p-p}$ on all but the selected channel. See Test Circuit #9.
4. Calculated from typical Single-Ended Crosstalk performance.

HARRIS

HI-562A

12 Bit High Speed Monolithic Digital-to-Analog Converter

FEATURES

- OUTPUT CURRENT 2mA, F.S.
- MONOLITHIC CONSTRUCTION
- EXTREMELY FAST SETTLING 300ns TO 0.01% (TYP.)
- LOW GAIN DRIFT ±10ppm/°C (MAX.)
- EXCELLENT LINEARITY ±1/2 LSB (MAX.)
- DESIGNED FOR MINIMUM GLITCHES
- MONOTONIC OVER TEMPERATURE
- NOTE: HI-562A IS RECOMMENDED FOR NEW DESIGNS

APPLICATIONS

- CRT DISPLAY GENERATION
- HIGH SPEED A/D CONVERTERS
- VIDEO SIGNAL RECONSTRUCTION
- WAVEFORM SYNTHESIZERS
- HIGH SPEED DATA ACQUISITION
- HIGH-REL APPLICATIONS
- PRECISION INSTRUMENTS

DESCRIPTION

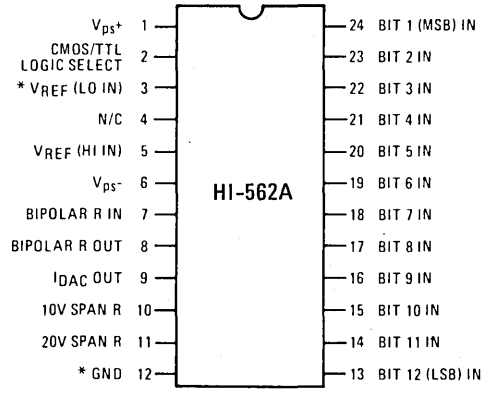
The Harris HI-562A is the first monolithic digital-to-analog converter to combine both ultra-high speed performance and 12-bit accuracy on the same chip. The HI-562A's fast output current settling of 300ns to 0.01% is achieved using dielectric isolation processing to reduce internal parasitics for fast rise and fall times during switching. Output glitches are minimized in the HI-562A by incorporating equally weighted current sources switched into an R-2R ladder network for symmetrical turn-ON and turn-OFF switching times. This creates within the chip a very uniform constant thermal distribution for excellent linearity and also completely eliminates thermal transients during switching. High stability thin film resistor processing together with laser trimming provide the HI-562A with guaranteed true 12-bit linearity to within ±1/2 LSB maximum at +25°C for -4 and -5 parts, and to within ±1/4 LSB maximum at +25°C for -2 and -8 parts. The HI-562A is recommended as a replacement for higher cost hybrid and modular units for increased reliability and accuracy in applications such as CRT displays, precision instruments and data acquisition systems requiring throughput rates as a high as 3.3 MHz for full range transitions. Its small size makes it an ideal choice as the heart of high speed A/D converter designs or as a building block in high speed or high resolution industrial process control systems. The HI-562A is also ideally suited for aircraft and space instrumentation where operation over a wide temperature range is required.

The HI-562A-5 is specified for operation over 0°C to +75°C, the HI-562A-4 over -25°C to +85°C and the HI-562A-2 and HI-562A-8 over -55°C to +125°C. Processing MIL-STD-883A Class B screening is available by selecting the HI-562A-8. All are available in a hermetically sealed 24-lead dual-in-line package.

PINOUT

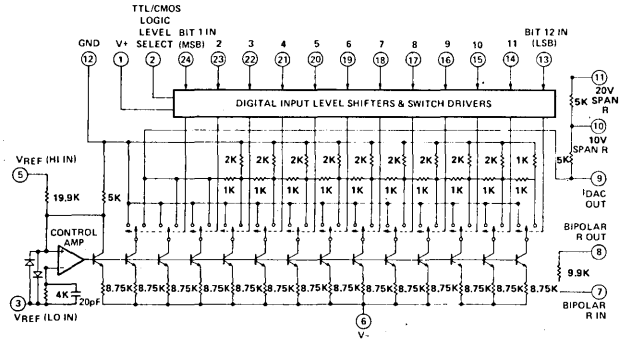
Section 11 for Packaging

TOP VIEW



*Pin 3 connected to bottom case for high frequency shielding.

FUNCTIONAL DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Referred to Ground)[1]

Power Supply Inputs	$V_{ps}+$	+20V
	$V_{ps}-$	-20V
Reference Inputs	V_{REF} (Hi)	$\pm V_{ps}$
Digital Inputs	Bits 1-12	-1V, +12V
	CMOS/TTL Logic Select	-1V, +12V
Outputs	Pins 7, 8, 10, 11	$\pm V_{ps}$
	Pin 9	$+V_{ps}$, -5V

Power Dissipation P_d, Package	1000mW
Operating Temperature Range	
HI-562A-2	-55°C to +125°C
HI-562A-4	-25°C to +85°C
HI-562A-5	0°C to +75°C
HI-562A-8	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS (@ +25°C, $V_{ps}+$ = +5V, $V_{ps}-$ = -15V, V_{REF} = +10V, pin 2 tied to pin 12 unless otherwise noted)

PARAMETER	CONDITIONS	HI-562A-2/HI-562A-8 MIN	HI-562A-2/HI-562A-8 TYP	HI-562A-2/HI-562A-8 MAX	HI-562A-4/HI-562A-5 MIN	HI-562A-4/HI-562A-5 TYP	HI-562A-4/HI-562A-5 MAX	UNITS
INPUT CHARACTERISTICS								
Digital Inputs (3)	Bit ON "Logic 1" Bit OFF "Logic 0"							
TTL Input Voltage (2) Logic "1"	Over full temp. range	2.0			2.0			V
TTL Logic "0"				0.8			0.8	V
TTL Input Current (2) Logic "1"	Pin 2 tied to Pin 12		20	100		20	100	nA
TTL Logic "0"			-50	-100		-50	-100	μA
CMOS Input Voltage Logic "1"	Connect pin 2 to pin 1 for $V_{ps}+ \geq$ 9.5V. Otherwise (for CMOS levels below 8V), connect pin 2 to pin 12.	$0.7V_{ps}+$			$0.7V_{ps}+$			V
CMOS Logic "0"				$0.3V_{ps}+$			$0.3V_{ps}+$	V
CMOS Input Current Logic "1"			20	100		20	100	nA
CMOS Logic "0"			-50	-100		-50	-100	μA
Reference Input Input Resistance			20K			20K		Ω
Input Voltage			+10			+10		V
TRANSFER CHARACTERISTICS								
Resolution	Over full temp. range			12			12	Bits
Nonlinearity (3)	@ +25°C			±1/4		±1/4	±1/2	LSB
	Over full temp. range		±1/2	±1			±1	
Differential Nonlinearity (3)	@ +25°C			±1/4		±1/4	±1/2	LSB
	Over full temp. range			MONOTONICITY GUARANTEED				
Relative Accuracy (6)	With 50 Ω(1%) Trim Resistors							
Gain Error	All Bits ON		±.024	±0.25		±.024	±0.25	
Bipolar Offset Error	All Bits OFF		±.024	±0.25		±.024	±0.25	% FSR (4)
Unipolar Offset Error			±.012	±0.05		±.012	±0.05	
Adjustment Range	See Operating Instructions							
Gain	With 100 ΩTrim		±0.25			±0.25		% FSR
Bipolar Offset	Potentiometers		±0.5			±0.5		
Temperature Stability	Drift specified with internal span resistors for voltage output							
Gain Drift (3)	Over full		±6	±10			±10	ppm of
Offset Drift (3)	temp. range							FSR/°C
Unipolar Offset	All Bits OFF			±2			±2	
Bipolar Offset				±4			±4	
Differential Nonlinearity	Over full temp. range		±1	±2		±2	±2	
Settling Time (3) to ±1/2 LSB	All Bits ON-to-OFF or OFF-to-ON		300	400		300	400	ns

PARAMETER	CONDITIONS	HI-562A-2/HI-562A-8 MIN	HI-562A-2/HI-562A-8 TYP	HI-562A-2/HI-562A-8 MAX	HI-562A-4/HI-562A-5 MIN	HI-562A-4/HI-562A-5 TYP	HI-562A-4/HI-562A-5 MAX	UNITS
Major Carry Transient								
Peak Amplitude	From 011...1 to 100...0 or 100...0 to 011...1		0.7			0.7		mA
Settling Time to 90% Complete			35			35		ns
Power Supply Sensitivity (3)								
Unipolar Offset	All Bits OFF							ppm of FSR/% V_{ps}
V_{ps}+ @ +5V			±0.5			±0.5		
V_{ps}- @ -15V			±0.5			±0.5		
Bipolar Offset	All Bits OFF, Bipolar mode							
V_{ps}+ @ 5V			±1.5			±1.5		
V_{ps}- @ -15V			±1.5			±1.5		
Gain	All Bits ON							
V_{ps}+ @ +5V				±3.5			±3.5	
V_{ps}- @ -15V				±7.5			±7.5	

OUTPUT CHARACTERISTICS

Output Current								
Unipolar			-2.0			-2.0		mA
Bipolar			±1.0			±1.0		
Resistance			2K			2K		ohms
Capacitance			20			20		pF
Output Voltage Ranges								
Unipolar	Using external op amp and internal scaling resistors. See Figure 1 and Table 1 for connections		0 to +5 0 to +10			0 to +5 0 to +10		V
Bipolar			±2.5 ±5 ±10			±2.5 ±5 ±10		
Compliance Limit (3)		-3		+10	-3		+10	V
Compliance Voltage (3)	Over full temp. range		±1.0			±1.0		V
Output Noise	0.1 to 10Hz (All Bits ON) 0.1 to 5MHz (All Bits ON)		30 100			30 100		µV (p-p)

POWER REQUIREMENTS

V_{ps}+ (7)	Over full temp. range	4.5	5	16.5	4.75	5	16.5	V
V_{ps}-		-13.5	-15	-16.5	-13.5	-15	-16.5	
I_{ps}+ (5)	All Bits ON or OFF in either TTL or CMOS mode (25°C)		8	15		8	15	mA
I_{ps}- (5)			16	23		16	23	
I_{ps}+ (5)	Same as above except over full temp. range		11	20		11	20	mA
I_{ps}- (5)			20	30		20	30	
Power Dissipation	+25°C V_{ps}+ = +5V V_{ps}- = -15V		280	420				mW

HARRIS

HI-565A

High Speed Monolithic Digital to Analog Converter with Reference

FEATURES

- DAC AND REFERENCE ON A SINGLE CHIP
- PIN COMPATIBLE WITH AD565A
- VERY HIGH SPEED: SETTLES TO 1/2 LSB IN 250ns, MAX. FULL SCALE SWITCHING TIME 30ns, TYP.
- GUARANTEED FOR OPERATION WITH ±12V SUPPLIES
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- 1/2 LSB MAX NONLINEARITY GUARANTEED OVER TEMPERATURE
- LOW GAIN DRIFT (MAX, DAC PLUS REFERENCE) 25ppm/°C
- LOW POWER DISSIPATION 250mW

APPLICATIONS

- CRT DISPLAYS
- HIGH SPEED A/D CONVERTERS
- SIGNAL RECONSTRUCTION
- WAVEFORM SYNTHESIS

DESCRIPTION

The HI-565A is a fast, 12 bit current output, digital to analog converter. The monolithic chip includes a precision voltage reference, thin-film R-2R ladder, reference control amplifier and twelve high-speed bipolar current switches.

The Harris Semiconductor dielectric isolation process provides latch-free operation while minimizing stray capacitance and leakage currents, to produce an excellent combination of speed and accuracy. Also, ground currents are minimized to produce a low and constant current through the ground terminal, which reduces error due to code-dependent ground currents.

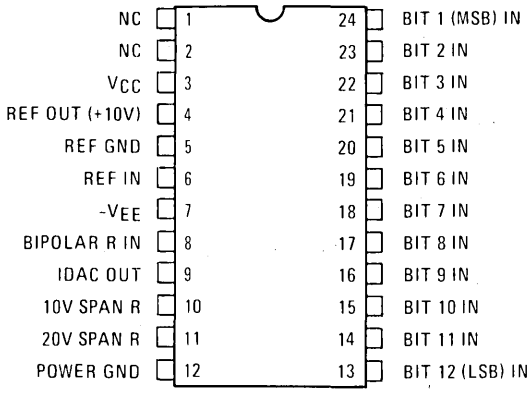
HI-565A dice are laser trimmed for a maximum integral non-linearity error of ±1/4 LSB at +25°C. In addition, the low noise buried zener reference is trimmed both for absolute value and minimum temperature coefficient.

The HI-565A is offered in both commercial and military grades. For high-reliability requirements, additional 100% screening per Mil-Std. 883, Method 5004, Class B is available. See Ordering Information.

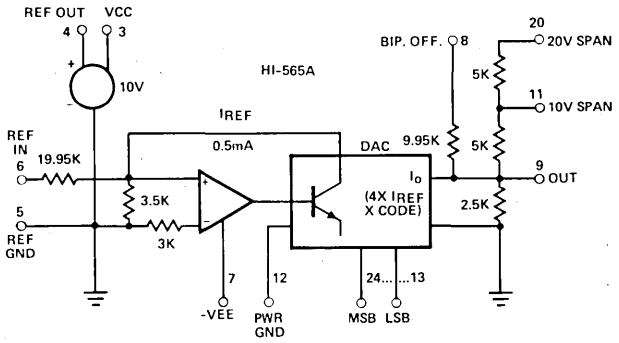
Package is a 24 pin side-brazed ceramic DIP. Power requirement is 250mW, typical.

PINOUT

TOP VIEW



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

V_{CC} to Power Ground	0V to +18V	10V Span R to Reference Ground	±12V
V_{EE} to Power Ground	0V to -18V	20V Span R to Reference Ground	±24V
Voltage on DAC Output (Pin 9)	-3V to +12V	Ref Out	Indefinite Short to Power Ground Momentary Short to V_{CC}
Digital Inputs (Pins 13-24) to Power Ground	-1V to +7.0V	Package Power Dissipation	
Ref In to Reference Ground	±12V	Ceramic (D)	1000mW
Bipolar Offset to Reference Ground	±12V	Plastic (N)	750mW

Absolute maximum ratings are limiting values beyond which the serviceability of the circuit may be impaired.

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = +15V, V_{EE} = -15V, Unless Otherwise Specified)

MODEL	HI-565AJ, HI-565AS			HI-565AK, HI-565AT			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
DATA INPUTS (Note 1) (Pins 13 to 24)							
TTL or 5V CMOS (T_{MIN} to T_{MAX})							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"			+0.8			+0.8	V
Logic Current (Each Bit)							
Bit ON Logic "1"		.01	+1.0		.01	+1.0	µA
Bit OFF Logic "0"		-2.0	-20		-2.0	-20	µA
RESOLUTION			12			12	Bits
OUTPUT							
Current Unipolar (All Bits On)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (All Bits on or Off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (Exclusive of Span Resistors)	1.8k	2.5k	3.2k	1.8k	2.5k	3.2k	Ω
Offset Unipolar		0.01	0.05		0.01	0.05	% of F.S.
Bipolar (Figure 5, R_2 = 50Ω Fixed)		0.05	0.15		0.05	0.1	% of F.S.
Capacitance		20			20		pF
Compliance Voltage, T_{MIN} to T_{MAX}	-1.5		+10	-1.5		+10	V
ACCURACY (Error Relative to Full Scale)							
+25°C		±1/4	±1/2		±1/8	±1/4	LSB
		(0.006)	(0.012)		(0.003)	(0.006)	% of F.S.
T_{MIN} to T_{MAX}		±1/2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% OF F.S.
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{MIN} to T_{MAX}	MONOTONICITY GUARANTEED						
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		15	40		10	25	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2 LSB							
With High,Z External Load (Note 2)		350	500		350	500	ns
With 75Ω External Load		150	250		150	250	ns

SPECIFICATIONS (Continued)

MODEL	HI-565AJ, HI-565AS			HI-565AK, HI-565AT			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
FULL SCALE TRANSITION (From 50% of Logic Input to 90% of Analog Input)							
Rise Time		15	30		15	30	ns
Fall Time		30	50		30	50	ns
TEMPERATURE RANGE							
Operating (HI-565AJ/K)	0		+75	0		+75	°C
(HI-565AS/T)	-55		+125	-55		+125	°C
Storage							
D Package (All)	-65		+150	-65		+150	°C
N Package (J, K)	-25		+150	-25		+150	°C
POWER REQUIREMENTS							
V_{CC}, +11.4 to +16.5V DC		7.0	10.5		7.0	10.5	mA
V_{EE}, -11.4 to -16.5V DC		-9.5	-14.5		-9.5	-14.5	mA
POWER SUPPLY GAIN SENSITIVITY (Note 3)							
V_{CC} = +11.4 to +16.5 VDC		3	10		3	10	ppm of F.S./%
V_{EE} = -11.4 to -16.5 VDC		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT RANGES (See Table 1)	0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10			0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10			V V V V V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R2 (Figure 1)		±0.1	±0.25		±0.1	±0.25	% of F.S.
Bipolar Zero Error with Fixed 50Ω Resistor for R3 (Figure 2)		±0.05	±0.15		±0.05	±0.1	% of F.S.
Gain Adjustment Range (Figure 1)	±0 25			±0.25			% of F.S.
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S.
REFERENCE INPUT							
Input Impedance	15K	20K	25K	15K	20K	25K	
REFERENCE OUTPUT							
Voltage	9.90	10.00	10.10	9.90	10.00	10.10	V
Current (Available for External Loads)	1.5	2.5		1.5	2.5		mA
POWER DISSIPATION		250	375		250	375	mW

NOTES:
1. Guaranteed but not tested over the operating temperature range.
2. See settling time discussion and Figure 3.
3. The Power Supply Gain Sensitivity is tested in reference to a V_{CC}, V_{EE} of ±15V.

HARRIS

HI-5610

10 Bit High Speed Monolithic Digital-to-Analog Converter

Preliminary

FEATURES

- MONOLITHIC CONSTRUCTION
- EXTREMELY FAST SETTLING. . . . . 85ns TO ½LSB TYP.
- LOW GAIN DRIFT. . . . . ±5ppm/°C TYP.
- EXCELLENT LINEARITY OVER TEMPERATURE . . . . . ±½LSB MAX.
- DESIGNED FOR MINIMUM GLITCHES
- MONOTONIC OVER TEMPERATURE

APPLICATIONS

- CRT DISPLAY GENERATION
- HIGH SPEED A/D CONVERTERS
- VIDEO SIGNAL RECONSTRUCTION
- WAVEFORM SYNTHESIZERS
- HIGH SPEED DATA ACQUISITION
- HIGH RELIABILITY APPLICATIONS
- PRECISION INSTRUMENTS

DESCRIPTION

The HI-5610 is an ultra-high speed 10 bit monolithic current output digital-to-analog converter. The fast output current settling of 85ns to ½LSB of its final value is achieved using dielectric isolation processing to reduce internal parasitics for fast rise and fall times during switching. Output glitches are minimized in the HI-5610 by incorporating equally weighted current sources switched into an R-2R ladder network for symmetrical turn-on and turn-off switching times. This creates within the chip a very uniform and constant thermal distribution for excellent linearity and also eliminates thermal transients during switching. High stability thin film resistor processing, together with laser trimming provide the HI-5610 with true 10 bit linearity to within ± ½LSB maximum over operating temperature range. The HI-5610's low offset and gain drift over the operating temperature range assures that its absolute accuracy when referred to a fixed 10V reference will not deviate more than ±1LSB for both unipolar and bipolar operation.

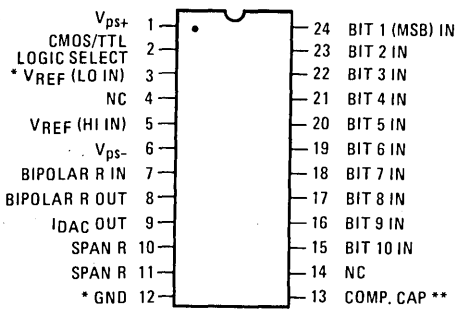
The HI-5610 is recommended as a replacement for high cost hybrid and modular units for increased reliability and accuracy in applications such as CRT Displays, precision instruments and data acquisition system requiring through-put rates as high as 12mHz for full range transitions. Its small size makes it an ideal choice as the essential part of high speed A/D converter designs or as a building block in high speed or high resolution industrial process control systems. The HI-5610 is also ideally suited for aircraft and space instrumentation where operation over a wide temperature range is required.

The HI-5610-5 is specified for operation over 0°C to +75°C, the HI-5610-2 and HI-5610-8 over -55°C to +125°C. Processing to MIL-STD-883A class B screening is available by selecting the HI-5610-8. All are available in a hermetically sealed 24 lead dual-in-line package.

PINOUT

Section 11 for Packaging

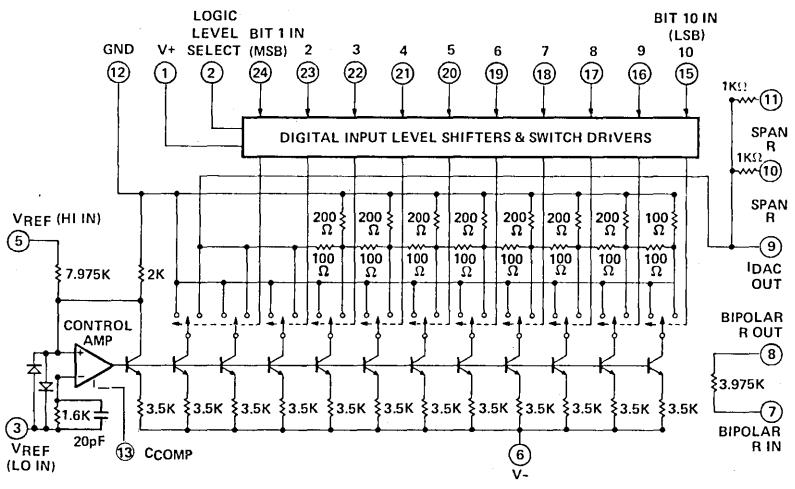
TOP VIEW



* Pin 3 connected to bottom case for high frequency shielding.

** For high speed operation, connect 0.01μF between Pin 13 and GND. Otherwise, leave Pin 13 open.

FUNCTIONAL DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Referred to Ground)[1]

Power Supply Inputs	$V_{ps}+$	+20V
	$V_{ps}-$	-20V
Reference Inputs	VREF (Hi)	$\pm V_{ps}$
	VREF(Lo)	0V
Digital Inputs	Bits 1 - 12	-1V, +12V
	CMOS/TTL Logic Select	-1V, +12V
Outputs	Pins 7, 8, 10, 11	$\pm V_{ps}$
	Pin 9	$+V_{ps}$, -5V

Power Dissipation Pd, Package	1000mW
Operating Temperature Range	
HI-5610-2	-55°C to +125°C
HI-5610-5	0°C to +75°C
HI-5610-8	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS (@ +25°C, $V_{ps}+$, = +5V, $V_{ps}-$ = -15V, V_{REF} = +10V, pin 2 ground unless otherwise noted)

		HI-5610-2 HI-5610-8			HI-5610-5			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Digital Inputs (2)								
TTL Logic Input Voltage (3)								
Logic "1"	Full	2.0			2.0			V
Logic "0"	Full			0.8			0.8	V
Input Current								
Logic "1"	Full		20	100		20	100	nA
Logic "0"	Full		-50	-100		-50	-100	μA
CMOS Logic Input Voltage (4)								
Logic "1"	Full	$0.7V_{ps}+$			$0.7V_{ps}+$			V
Logic "0"	Full			$0.3V_{ps}+$			$0.3V_{ps}+$	V
Input Current								
Logic "1"	Full		20	100		20	100	nA
Logic "0"	Full		-50	-100		-50	-100	μA
Reference Input								
Input Resistance			8K			8K		Ω
Input Voltage (I_{OUT} = 5mA + 20%)			+10			+10		V
TRANSFER CHARACTERISTICS								
Resolution	Full			10			10	Bits
Nonlinearity (5)	25°C			±½			±½	LSB
Differential Nonlinearity (5)	25°C			±½			±½	LSB
Relative Accuracy (6)								
Gain Error								(9)
(Input Code 11....1)			±0.05			±0.05		% FSR
Unipolar Offset Error								
(Input Code 00....0)			±0.05			±0.05		% FSR
Bipolar Offset Error								
(Input Code 00....0)			±0.05			±0.05		% FSR
(Adjustable to zero, see Figure 4, 5)								
Adjustment Range								
Gain			±0.25			±0.25		% FSR
Bipolar Offset			±0.25			±0.25		% FSR
Temperature Stability								
Gain Drift	Full		±5			±5		ppm/°C
Unipolar Offset Drift	Full		±3			±3		ppm/°C
Bipolar Offset Drift	Full		±3			±3		ppm/°C
Differential Nonlinearity	Full		±2			±2		ppm/°C
MONOTONICITY - GUARANTEED OVER FULL OPERATING TEMPERATURE RANGE								
Settling Time to ½LSB (5)								
From all 0's to all 1's						85		ns
From all 1's to all 0's						85		ns
Major Carry Switching to 90% Complete			40			40		ns

PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Power Supply Sensitivity (5)								
$V_{ps}+$ = +5V, $V_{ps}-$ = -13.5V to -16.5V								
Gain								
(Input Code 11....1)				±2			±2	
Unipolar Offset								
(Input Code 00....0)			±0.5			±0.5		
Bipolar Offset								ppm of
(Input Code 00....0)			±1.5			±1.5		FSR/%V_{ps}
$V_{ps}-$ = -15V, $V_{ps}+$ = 4.5V to 5.5V								
Gain								
(Input Code 11....1)				±1			±1	
Unipolar Offset								
(Input Code 00....0)			±0.5			±0.5		
Bipolar Offset								
(Input Code 00....0)			±1.5			±1.5		
OUTPUT CHARACTERISTICS								
Output Current								
Unipolar			-5.0			-5.0		mA
Bipolar			±2.5			±2.5		mA
Output Resistance			200			200		Ω
Output Capacitance			20			20		pF
Output Voltage Range (7)								
Unipolar			+5			+5		V
			+2.5			+2.5		V
Bipolar			±2.5			±2.5		V
			±1.25			±1.25		V
Output Compliance Limit (5)		-3		+10	-3		+10	V
Output Compliance Voltage (5)	Full		±1.5			±1.5		V
Output Noise Voltage (8)								
0.1Hz to 100Hz			10			10		μVp-p
0.1Hz to 1MHz			100			100		μVp-p
POWER REQUIREMENTS								
$V_{ps}+$ (4)	Full	4.5	5	16.5	4.75	5	16.5	V
$V_{ps}-$	Full	-13.5	-15	-16.5	-13.5	-15	-16.5	V
$I_{ps}+$ (All 1's or all 0's in	25°C		9			9		mA
(10) either TTL or CMOS Mode)	Full		20			20		mA
$I_{ps}-$ (Same as above)	25°C		25			25		mA
(10)	Full		30			30		mA

HARRIS

HI-5618A/5618B

8 Bit High Speed Digital-to-Analog Converters

FEATURES

- VERY FAST SETTLING CURRENT OUTPUT 65ns
- MINIMUM NONLINEARITY ERROR
  - HI-5618A ±1/4 LSB MAX
  - HI-5618B ±1/2 LSB MAX
- LOW POWER OPERATION 340mW TYP
- ON-CHIP RESISTORS FOR GAIN AND BIPOLAR OFFSET
- GUARANTEED MONOTONIC OVER TEMPERATURE
- CMOS, TTL, OR DTL COMPATIBLE

APPLICATIONS

- HIGH SPEED PROCESS CONTROL
- CRT DISPLAY GENERATION
- HIGH SPEED A/D CONVERSION
- WAVEFORM SYNTHESIS
- HIGH RELIABILITY APPLICATIONS
- VIDEO SIGNAL RECONSTRUCTION

DESCRIPTION

The HI-5618A/B are very high speed 8 bit current output D/A converters. These monolithic devices are fabricated with dielectrically isolated bipolar processing, which reduces internal parasitic capacitance to allow fast rise and fall times. This achieves a typical full scale settling time of 65ns to ±1/2 LSB. Output glitches are minimized by incorporation of equally weighted current sources, switched to either an R-2R ladder network or ground for symmetrical turn ON and turn OFF times. High stability thin film resistors provide excellent accuracy without trimming. For example, the HI-5618A has ±1/4 LSB maximum nonlinearity error at +25°C, with ±3/8 LSB guaranteed over the full operating temperature range.

The HI-5618A/B are recommended for any application requiring high speed and accurate conversions. They can be used in CRT displays and systems requiring throughput rates as high as 20MHz for full scale transitions. Other applications include high speed process control, defense systems, avionics, and space instrumentation.

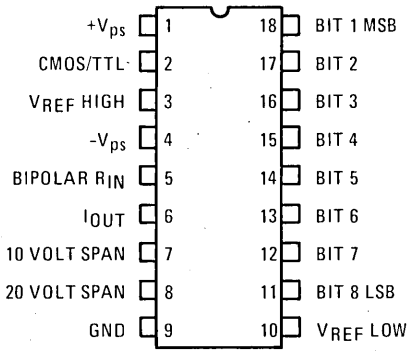
The HI-5618A-5 and HI-5618B-5 are specified for operation from 0°C to +75°C. The "-2" versions are specified from -55°C to +125°C. "Dash 8" (-8) designates parts which have been screened per MIL-STD-883, Method 5004/Class B.

Power requirements are +5V and -15V. Package is an 18 pin DIP, in plastic or ceramic.

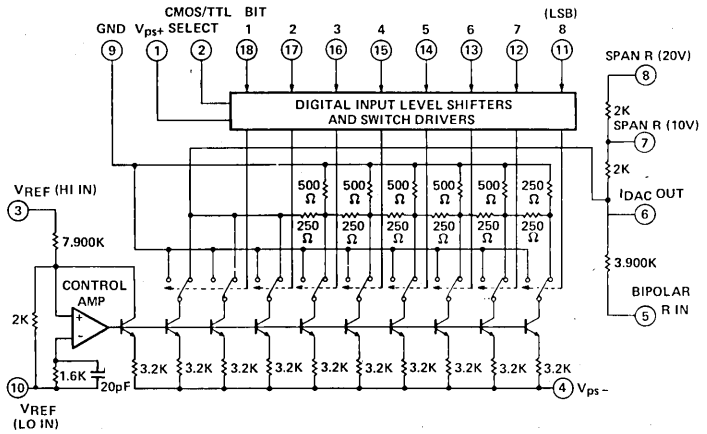
PINOUT

Section 11 for Packaging

TOP VIEW



FUNCTIONAL DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Referred to Ground) (1)

Power Supply Inputs	$V_{ps}+$	+20V
	$V_{ps}-$	-20V
Reference Inputs	V_{REF} (Hi)	$\pm V_{ps}$
	V_{REF} (Lo)	0V
Digital Inputs	Bits 1 - 8	-1V, +12V
CMOS/TTL Logic Select		-1V, +12V
Outputs	Pins 5, 7, 8	$\pm V_{ps}$
	Pin 6	$+V_{ps}$, -2.5V

Power Dissipation Pd, Package	700mW
Operating Temperature Range	
HI-5618A/B-2	-55°C to +125°C
HI-5618A/B-5	0°C to +75°C
HI-5618A/B-8	-55°C to +125°C
Storage Temperature Range	-65°C to 150°C

ELECTRICAL CHARACTERISTICS ($V_{ps}+ = +5V$; $V_{ps}- = -15V$; $V_{REF} = +10V$; Pin 2 to GND, unless otherwise noted)

PARAMETER		TEMP	HI-5618A/B-2 HI-5618A/B-8 MIN	TYP	MAX	HI-5618A/B-5 MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS									
Digital Inputs (2)									
TTL Logic Input Current (3)	Logic "1"	Full	2.0			2.0			V
	Logic "0"	Full			0.8			0.8	V
Input Current	Logic "1"	Full		20	100		20	100	nA
	Logic "0"	Full		-50	-100		-50	-100	μA
CMOS Logic Input Voltage (4)	Logic "1"	Full	$0.7V_{ps}+$			$0.7V_{ps}+$			V
	Logic "0"	Full			$0.3V_{ps}+$			$0.3V_{ps}+$	V
CMOS Logic Input Current	Logic "1"	Full		20	100		20	100	nA
	Logic "0"	Full		-50	-100		-50	-100	μA
Reference Input									
Input Resistance		+25°C		8k			8k		Ω
Input Voltage (I_{OUT} = 5mA ± 20%)		+25°C		+10			+10		V
TRANSFER CHARACTERISTICS									
Resolution		Full		8			8		Bits
Nonlinearity, Integral and Differential	HI-6518A	25°C			±1/4			±1/4	LSB
		Full			±3/8			±3/8	LSB
	HI-5618B	25°C			±1/2			±1/2	LSB
		Full			±5/8			±5/8	LSB
Initial Accuracy (6) (Relative to External +10V Reference)									
Gain		25°C			±2			±2	LSB
Unipolar Zero		25°C			±1/8			±1/8	LSB
Bipolar Offset (Neg. Full Scale)		25°C			±2			±2	LSB
Temperature Stability									
Gain Drift		Full			±1/4			±1/4	LSB
Unipolar Zero Drift		Full			±1/16			±1/16	LSB
Bipolar Zero Drift		Full			±1/4			±1/4	LSB
Settling Time (5) to 1/2 LSB									
High Impedance (11)	(from all 0's to all 1's)	+25°C		65	75		65	75	ns
or	(from all 1's to all 0's)								

SPECIFICATIONS (Continued)

PARAMETER		TEMP	HI-5618A/B-2 HI-5618A/B-8 MIN	TYP	MAX	HI-5618A/B-5 MIN	TYP	MAX	UNITS
TRANSFER CHARACTERISTICS (Continued)									
Glitch (5) - Major Carry Transition									
Duration		+25°C		20			20		ns
Amplitude (See Fig. 4)		+25°C		350			350		mV
Area		+25°C		3500			3500		mV–ns
Power Supply Sensitivity (5)									
$V_{ps}+$ = +5V, $V_{ps}-$ = -13V to -16.5V									
Gain	(Input Code 11 . . . 1)	+25°C			±5			±5	
Unipolar Zero	(Input Code 00 . . . 0)	+25°C		±0.5			±0.5		ppm of
Bipolar Offset	(Input Code 00 . . . 0)	+25°C		±1.5			±1.5		FSR/% Vps (9)
$V_{ps}-$ = -15V, $V_{ps}+$ = 4.5V to 5.5V									
Gain	(Input Code 11 . . . 1)	+25°C			±5			±5	
Unipolar Zero	(Input Code 00 . . . 0)	+25°C		±0.5			±0.5		
Bipolar Offset	(Input Code 00 . . . 0)	+25°C		±1.5			±1.5		
OUTPUT CHARACTERISTICS									
Output Current	Unipolar	+25°C		-5			-5		mA
	Bipolar	+25°C		±2.5			±2.5		mA
Output Resistance		+25°C		500			500		Ω
Output Capacitance		+25°C		20			20		pF
Output Voltage Range (7)	Unipolar	+25°C		+10			+10		V
		+25°C		+5			+5		V
	Bipolar	+25°C		±10			±10		V
		+25°C		±5			±5		V
		+25°C		±2.5			±2.5		V
Output Compliance Voltage (5)		+25°C		±1.5			±1.5		V
Output Noise Voltage (8)	0.1Hz to 100Hz	+25°C		30			30		μV_{p-p}
	0.1Hz to 1Mhz	+25°C		100			100		μV_{p-p}
POWER REQUIREMENTS (4)									
$V_{ps}+$		Full	4.5	5	15	4.75	5	15	V
$V_{ps}-$		Full	−13.5	−15	−16.5	−14.25	−15	-15.75	V
$I_{ps}+$ (10) (All 1's or all 0's in either TTL or CMOS mode) (3, 4)		+25°C		9			9		mA
		Full			12			12	mA
$I_{ps}-$ (10) (All 1's or all 0's in either TTL or CMOS mode) (3, 4)		+25°C		19			19		mA
		Full			26			26	mA

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. The HI-5618 accepts digital input codes in binary format and may be user connected for any one of three binary codes. Straight binary, offset binary, or two's complement binary. (See operating instructions)
3. For TTL and DTL compatibility connect +5V to pin 1 and ground pin 2. The $V_{ps}+$ tolerance is ± 10% for HI-5618A/B -2, -8; and ± 5% for HI-5618A/B-5.
4. For CMOS compatibility connect digital power supply (+4.5V ≤ V_{DD} ≤ +10V) to pin 1 and short pin 2 to pin 1.
5. See definitions.
6. These errors may be adjusted to zero using external potentiometers R_1, R_2, R_3. R_1 and R_2 each provide more than ± 3 LSB's adjustment. (See Operating Instructions). The specifications listed under initial accuracy are based on use of an external op amp, internal span and offset resistors, and 100 Ω ± 1% resistors, in place of R_1 and R_2.
7. Using an external op amp with the internal span and offset resistors. See Operating Instructions.
8. Specified for all "1's" or all "0's" digital input.
9. FSR is "Full Scale Range", i.e., 20V for ± 10V range; 10V for ± 5V range, etc. Nominal full scale output current is 5mA.
10. After 30 seconds warm-up.
11. See Test Circuit, Figure 3.
12. See Test Circuit , Figure 4.

HARRIS

HI-5680

12 Bit Low Cost Monolithic Digital-to-Analog Converter

FEATURES

- DAC 80 ALTERNATE SOURCE
- MONOLITHIC CONSTRUCTION (SINGLE CHIP)
- FAST SETTLING
- GUARANTEED MONOTONIC 0°C to 75°C
- WAFER LASER TRIMMED
- APPLICATIONS RESISTORS ON-CHIP
- ON-BOARD REFERENCE
- DIELECTRIC ISOLATION (DI) PROCESSING
- ±12V POWER SUPPLY OPERATION

APPLICATIONS

- HIGH SPEED A/D CONVERTERS
- PRECISION INSTRUMENTATION
- CRT DISPLAY GENERATION

DESCRIPTION

The HI-5680 is a monolithic, direct replacement for the popular DAC80-CBI, DAC80Z-CBI, and DAC85C-CBI, incorporating the best features of each. Single chip construction, along with several design innovations, make the HI-5680 the optimum choice for low cost, high reliability applications.

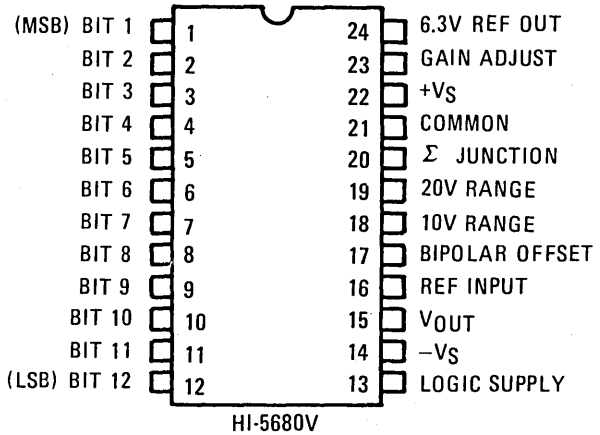
Harris' unique Dielectric Isolation (DI) processing reduces internal parasitics, resulting in fast switching times and minimum glitch. On-board span resistors are provided for good tracking over temperature, and are laser trimmed to high accuracy. These may be used with the on-board op-amp (voltage output models; HI-5680V), or with a user supplied external amplifier (HI-5680I).

Internally, the HI-5680 eliminates code dependent ground currents by routing current from the positive supply to the internal ground node, as determined by an auxiliary R-2R ladder. This results in a cancellation of code dependent ground currents allowing virtually zero variation in current through the package common, pin 21.

The HI-5680 is available in both current and voltage output models which are guaranteed over the 0°C to +75°C temperature range. All models include a buried zener reference featuring low temperature coefficient. In addition, the voltage output models include an on-board output amplifier. Both versions operate with a +5V logic supply and a $\pm V_S$ in the range of ±(11.4V to 16.5V).

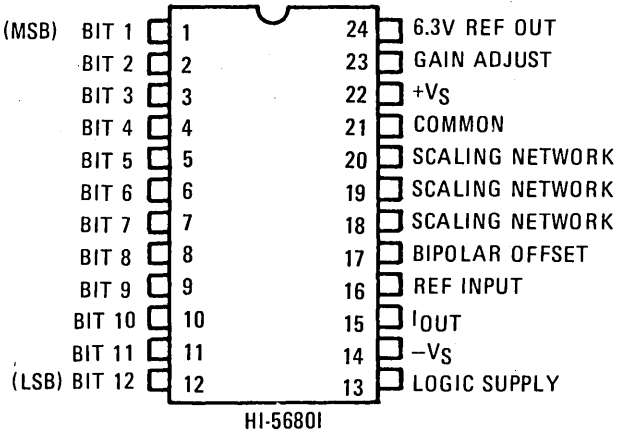
PINOUTS

TOP VIEW



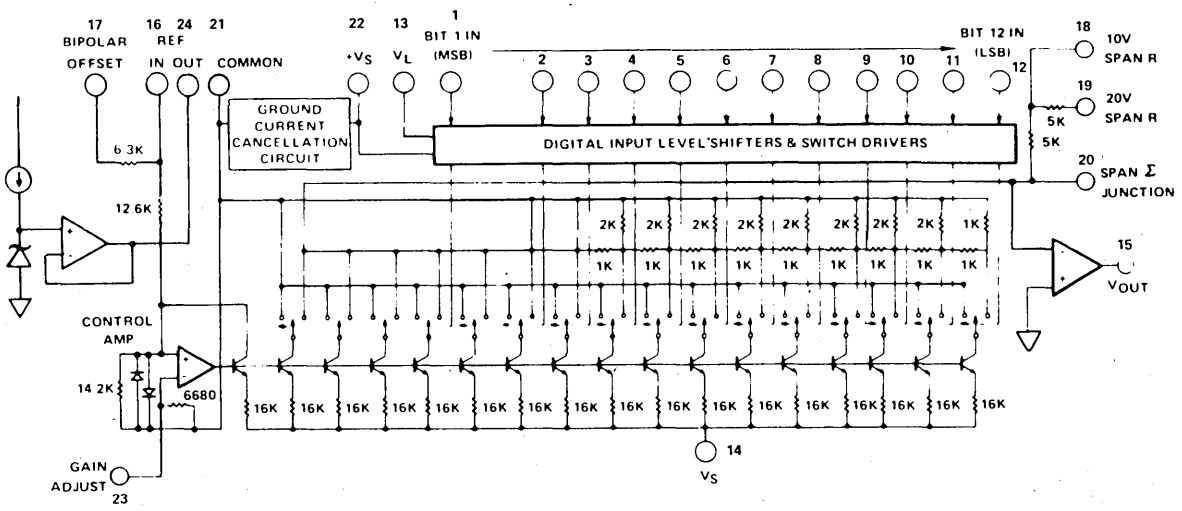
HI-5680V
VOLTAGE OUTPUT

TOP VIEW



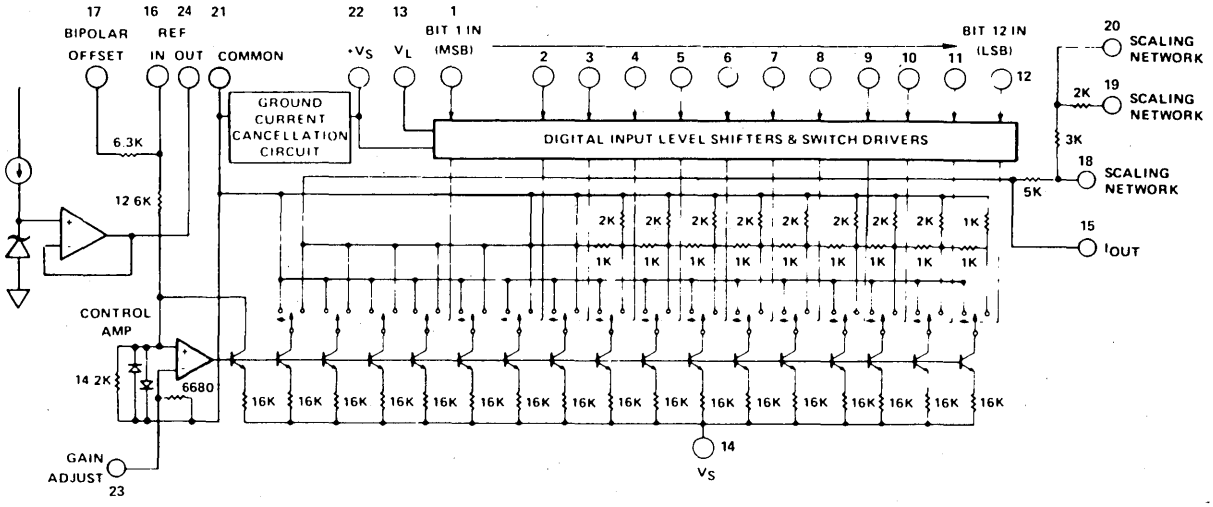
HI-5680I
CURRENT OUTPUT

FUNCTIONAL DIAGRAM VOLTAGE OUTPUT



HI-5680V

FUNCTIONAL DIAGRAM CURRENT OUTPUT



HI-5680I

ABSOLUTE MAXIMUM RATINGS (1)

Power Supply Inputs	$+V_S$	+20V	Power Dissipation	Pd, Package	1000mW
	$-V_S$	−20V			
	$+V_{LOGIC}$	+20V	Operating Temperature Range		
				HI-5680I/V-5	0°C to +75°C
Reference	Input (pin 16)	$+V_S$			
	Output drain	2.5mA	Storage Temperature Range		−65°C to +150°C
Digital Inputs	Bits 1 to 12	−1V to +12V			

ELECTRICAL SPECIFICATIONS

(T_A = +25°C, V_S = ±15V, V_{LOGIC} = +5V, PIN 16 CONNECTED TO PIN 24 UNLESS OTHERWISE SPECIFIED.)

PARAMETER	CONDITIONS	HI-5680X MIN	HI-5680X TYP	HI-5680X MAX	UNITS
DIGITAL INPUT (3)					
Resolution				12	Bits
Logic Levels	TTL Compatible				
Logic "1"	at +1 μA	+2		+5.5	Volts
Logic "0"	at −100 μA	0		+0.8	Volts
ACCURACY (3)	0° to +75°C				
Linearity Error			±¼	±½	LSB
Differential Lin. Error			±½	±¾	LSB
Gain Error (2)			±0.1	±0.3	%FSR
Offset Error (2)			±.05	±0.15	%FSR
Monotonicity			GUARANTEED		
DRIFT (3)	0°C to +75°C				
Total Bipolar Drift (Includes gain, offset and linearity drifts.)				±20	PPM/°C
Total Error	0°C to +75°C				
Unipolar			±.08	±0.15	%FSR
Bipolar			±.06	±.01	%FSR
Gain	Including internal reference		±15	±30	PPM/°C
	Exclusive of internal reference		±5	±7	PPM/°C
Unipolar Offset		±1	±3		PPM/°C
Bipolar Offset		±5	±10		PPM/°C
CONVERSION SPEED (3)					
Voltage Models					
Settling time (3)	to ±0.01% of FSR for FSR Change				
With 10KΩ Feedback			3		μs
With 5KΩ Feedback			1.5		μs
For 1 LSB change			1.5		μs
Slew Rate		10	15		V/μs
Current Models					
Settling time (3)	to ±0.01% of FSR for FSR Change				
10 to 100Ω load			300		ns
1KΩ load			1000		ns
ANALOG OUTPUT					
Voltage Models					
Output current		±5			mA
Output Resistance			.05		Ω
Short Circuit Duration	to common		continuous		

SPECIFICATIONS (continued)

PARAMETER	CONDITIONS	HI-5680X MIN	HI-5680X TYP	HI-5680X MAX	UNITS
ANALOG OUTPUT					
Current Models					
Output Current					
Unipolar			−2		mA
Bipolar			±1		mA
Output Impedance					
Unipolar			15		KΩ
Bipolar			4.4		KΩ
Compliance (3)				±2.5	V
INTERNAL REFERENCE					
Output Voltage		+6.174	+6.3	+6.426	V
Output Impedance			1.5		Ω
External Current				+2.5	mA
Tempco of Drift			20		PPM/°C
POWER SUPPLY SENSITIVITY (3)					
+15V supply			.002		$\frac{\%FSR}{\Delta V_s}$
−15V supply			.002		
+5V supply			.002		
POWER SUPPLY REQUIREMENTS (5)					
Range					
+15V		+11.4	+15	±16.5	V
−15V		−11.4	−15	−16.5	V
+5V		+ 4.5	+ 5	+16.5	V
Current					
+15V			8	16	mA
- 15V			-12	-24	mA
+5V			4.5	9	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Adjustable to zero using external potentiometers.
3. See definitions.
4. FSR is "full scale range" and is 20V for ±10V range, 10V for ±5V range, etc., or 2mA (±20%) for current output.
5. The HI-5680 will operate with supply voltages as low as ±11.4V. It is recommended that output voltage range −10V to +10V not be used if the supply voltages are less than ±12.5V.

DIGITAL INPUTS

The HI-5680 accepts digital input codes in complementary binary, complementary offset binary, and complementary two's complement binary.

DIGITAL INPUT	ANALOG OUTPUT		
	Complimentary Binary	Complimentary Offset Binary	Complementary Two's Complement*
MSB LSB			
000...000	+ Full Scale	+ Full Scale	− LSB
100...000	Mid Scale-1LSB	−1 LSB	+Full Scale
111...111	Zero	− Full Scale	Zero
011...111	+½ Full Scale	Zero	− Full Scale
*Invert MSB with external inverter to obtain CTC Coding			

SETTLING TIME

Settling time is the time required for the output to settle to within the specified error band for any input code transition. It is usually specified for a full scale or major carry transition.

DRIFT

GAIN DRIFT – The change in full scale analog output over the specified temperature range expressed in parts per million of full scale per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H −25°C) and low ranges (+25°C−T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT – The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Offset error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H −25°C) and low (+25°C −T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

ACCURACY

NONLINEARITY – Nonlinearity of a D/A converter is an important measure of its accuracy. It describes the deviation an ideal straight line drawn between zero (all bits OFF) and full scale (all bits ON).

DIFFERENTIAL NONLINEARITY – For a D/A converter, it is the difference between the actual output voltage change and the ideal (1 LSB) voltage change for a one bit change in code. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity; i.e., the output always increases and never decreases for an increasing input.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in −15V, or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE

Compliance voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance limit implies functional operation only and makes no claims to accuracy.

GLITCH

A glitch on the output of a D/A converter is a transient spike resulting from inequal internal ON−OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than turn OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably. (Measured as one half the product of duration and amplitude.)

DECOUPLING AND GROUNDING

For best accuracy and high frequency performance, the grounding and decoupling scheme shown in Figure 1 should be used. Decoupling capacitors should be connected close to the HI-5680 (preferrably to the device pins) and should be tantalum or electrolytic bypassed with ceramic types for best high frequency noise rejection.

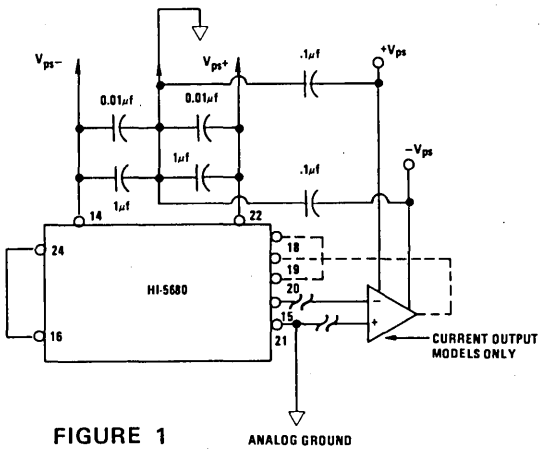


FIGURE 1

REFERENCE SUPPLY

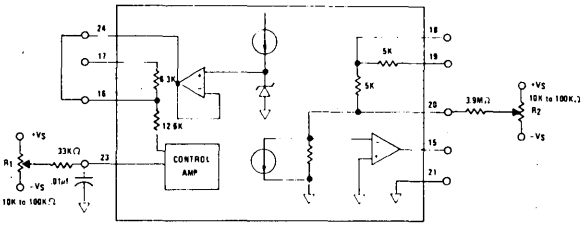
An internal 6.3Volt reference is provided on board all HI-5680 models. This voltage (pin 24) is accurate to ±2% and must be connected to the reference input (pin 16) for specified operation. This reference may be used externally, provided current drain is limited to 2.5mA. An external buffer amplifier is recommended if this reference is to be used to drive other system components. Otherwise, variations in the load driven by the reference will result in gain variations of the HI-5680. All gain adjustments should be made under constant load conditions.

VOLTAGE OUTPUT HI-5680V

RANGE CONNECTIONS

	Range	Connect		
		PIN 15	PIN 17	PIN 19
Unipolar	0 to +5V	18	21	20
	0 to +10V	18	21	N.C.
Bipolar	± 2.5V	18	20	20
	±5V	18	20	N.C.
	±10V	19	20	15

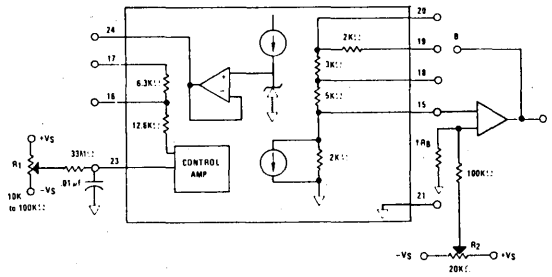
GAIN AND OFFSET CALIBRATION



UNIPOLAR CALIBRATION
Step 1: Offset Turn all bits OFF (11...1) Adjust R_2 for zero volts out
Step 2: Gain Turn all bits ON (00...0) Adjust R_1 for FS-1LSB That Is: 4.9987 for 0 to +5V range 9.9976 for 0 to +10V range
BIPOLAR CALIBRATION*
Step 1: Offset Turn all bits OFF (11...1) Adjust R_2 for Negative FS That Is: −10V for ±10V range −5V for ±5V range −2.5V for ±2.5 range
Step 2: Gain Turn all bits ON (00...0) Adjust R_1 for positive FS-1LSB That Is: +9.995V for ±10V range +4.9976V for ±5V range +2.4988V for ±2.5V range

*Because the DAC transfer junction is theoretically a straight line, this allows only two degrees of freedom for adjustment. For optimum adjustment choose the end points for exact location. (Full scale negative and Full scale positive minus 1 LSB) this leaves an error at zero (half scale) which is no greater than the maximum integral nonlinearity of the device.

CURRENT OUTPUT HI-5680I



CONNECTING AN EXTERNAL AMPLIFIER

To use the HI-5680I with an external amplifier connect as follows:

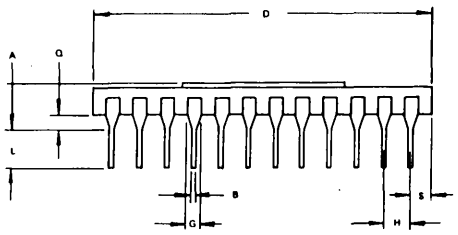
Range	Pin 17 to	Pin 18 to	Pin 19 to	Pin 20 to
0 to +10V	21	B	18*	19*
0 to +5V	21	B	15	N.C.
±10V	15	N.C.	B	N.C.
±5V	15	B	18*	19*
±2.5V	15	B	15	N.C.

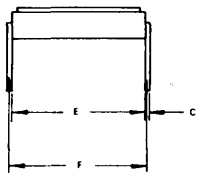
After connecting as shown above, follow gain and offset calibration procedures as outlined under the HI-5680V Voltage output section.

* these connections help reduce stray capacitance in the feedback loop.

† R_B should be chosen to equal the output impedance of the DAC. This may be calculated by $R_b = R_{LADDER}(2K\Omega)//R_{FEEDBACK}$.

PACKAGE DIMENSIONS

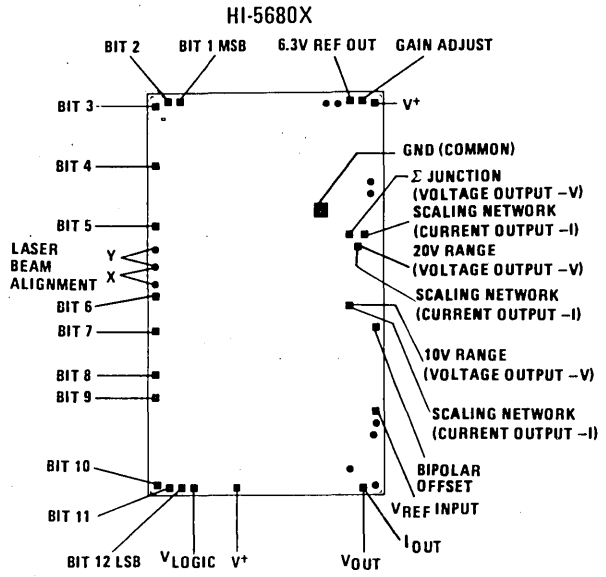




LEAD COUNT	DIM A	DIM B	DIM C	DIM D	DIM E	DIM F	DIM G	DIM H	DIM L	DIM Q	DIM S
24	MIN MAX 225	014 023	008 015	MIN MAX 1.290	500 610	590 620	030 070	100 BSC	120 200	015 075	MIN MAX 098

NOTE MIN. / MAX

CHIP PHOTO



ORDERING INFORMATION

MODEL	INPUT CODE CODE	OUTPUT MODE
HI-5680V-5	Complementary Binary	Voltage
HI-5680I-5	Complementary Binary	Current

HARRIS

HI-5685

High Performance Monolithic 12 Bit Digital-to-Analog Converter

FEATURES

- DAC 85 ALTERNATE SOURCE
- MONOLITHIC CONSTRUCTION (SINGLE CHIP)
- FAST SETTLING
- GUARANTEED MONOTONIC –25°C TO +85°C
- WAFER LASER TRIMMED
- APPLICATIONS RESISTORS ON-CHIP
- ON-BOARD REFERENCE
- DIELECTRIC ISOLATION (DI) PROCESSING
- ±12V POWER SUPPLY OPERATION

APPLICATIONS

- HIGH SPEED A/D CONVERTERS
- PRECISION INSTRUMENTATION
- CRT DISPLAY GENERATION

DESCRIPTION

The HI-5685 is a monolithic direct replacement for the popular DAC85-CBI and the ADDAC85LD-CBI. Single chip construction along with several design innovations make the HI-5685 the optimum choice for low cost, high reliability applications.

Harris' unique Dielectric Isolation (DI) processing reduces internal parasitics resulting in fast switching times and minimum glitch. On board span resistors are provided for good tracking over temperature, and are laser trimmed to high accuracy. These may be used with the on-board op-amp (voltage output models; HI-5685V), or with a user supplied external amplifier (HI-5685I).

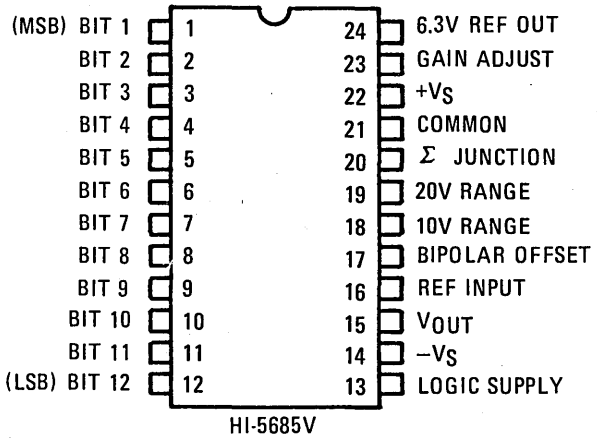
Internally, the HI-5685 eliminates code dependent ground currents by routing current from the positive supply to the internal ground node, as determined by an auxiliary R-2R ladder. This results in a cancellation of code dependent ground currents allowing virtually zero variation in current through the package common, pin 21.

The HI-5685 and HI-5685A are available in both current and voltage output models which are guaranteed over the –25°C to +85°C temperature range. All models include a buried zener reference featuring low temperature coefficient. In addition, the voltage output models include an on-board output amplifier. Both versions operate with a +5V logic supply and a $\pm V_S$ in the range of ±(11.4V to 16.5V).

The HI-5685A offers exceptionally low drift over temperature. Gain drift is a maximum ±10ppm/°C, over –25°C to +85°C.

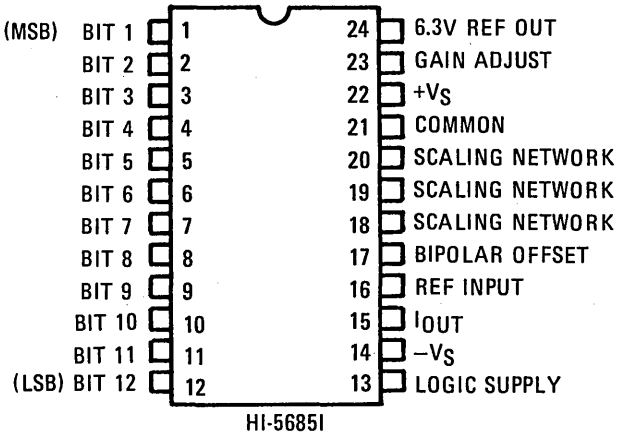
PINOUTS

TOP VIEW



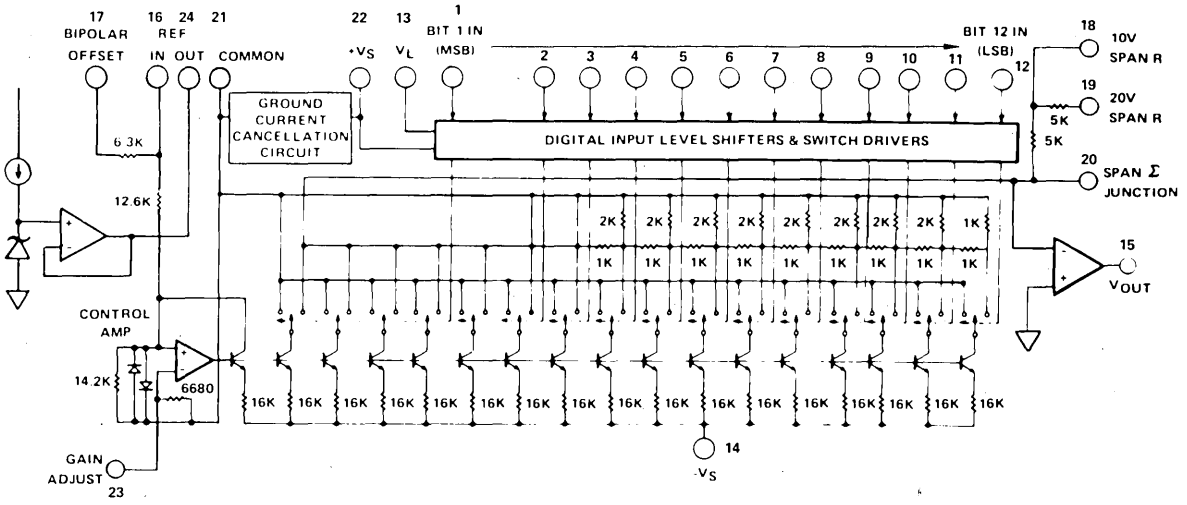
HI-5685V
VOLTAGE OUTPUT

TOP VIEW



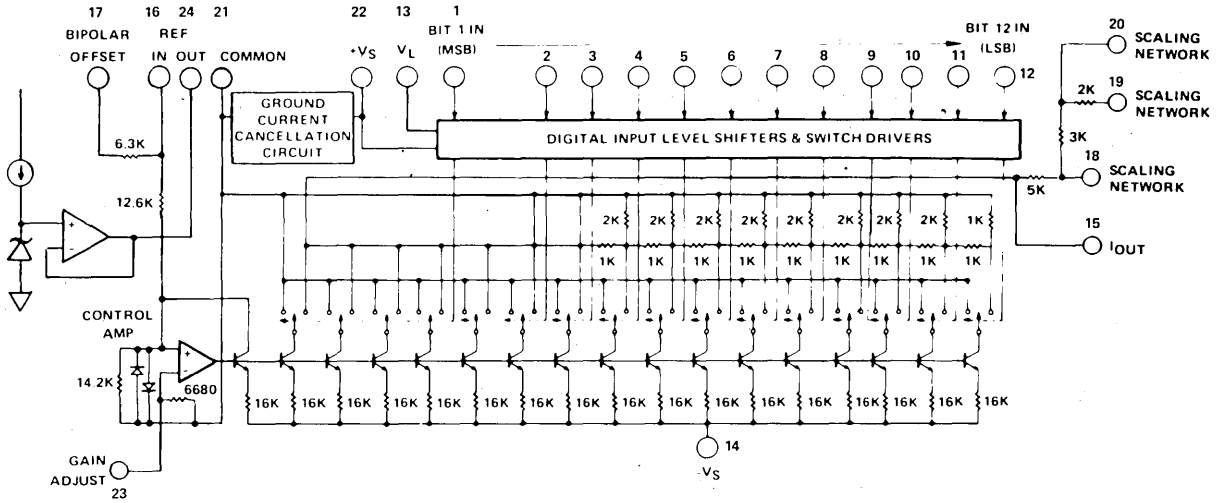
HI-5685I
CURRENT OUTPUT

FUNCTIONAL DIAGRAM VOLTAGE OUTPUT



HI–5685V
HI–5685AV

FUNCTIONAL DIAGRAM CURRENT OUTPUT



HI–5685I
HI–5685AI

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (1)

Power Supply Inputs	$+V_S$	+20V	Power Dissipation		
	$-V_S$	−20V		Pd, Package	1000mW
	$+V_{LOGIC}$	+20V	Operating Temperature Range		
Reference	Input (pin 16)	$\pm V_S$		HI-5685I/V−4	−25°C to +85°C
	Output drain	2.5mA		HI-5685AI/V−4	−25°C to +85°C
Digital Inputs	Bits 1 to 12	−1V to +12V	Storage Temperature Range		−65° to +150°C

ELECTRICAL SPECIFICATIONS

(T_A=+25°C, V_S = ±15V , V_{LOGIC} = 5V, PIN 16 CONNECTED TO PIN 24 UNLESS OTHERWISE SPECIFIED)

PARAMETER	CONDITIONS	HI-5685			
		MIN	TYP	MAX	UNITS
DIGITAL INPUT (3)					
Resolution				12	Bits
Logic Levels	TTL Compatible				
Logic "1"	at +1 µA	+2		+5.5	V
Logic "0"	at −100 µA	0		+0.8	V
Accuracy (3)					
Linearity Error	at +25°C			±½	LSB
	−25°C to +85°C			±½	LSB
Differential Lin. Error			±½		LSB
Gain Error (2)			±0.1		%FSR (4)
Offset Error (2)			±0.05		%FSR
Monotonicity			GUARANTEED		
DRIFT (3) HI-5685	−25°C to +85°C				
Gain				±20	
Offset					
Unipolar			±1		PPM/°C
Bipolar				±10	
DRIFT (3) HI-5685A (Low Drift)	−25°C to +85°C				
Gain				±10	
Offset					PPM/°C
Unipolar			±1		
Bipolar				±5	
CONVERSION SPEED					
Voltage Models					
Settling Time (3)	to ±0.01% of FSR for FSR Change				
With 10KΩFeedback			3		µs
With 5KΩFeedback			1.5		µs
For 1 LSB Change			1.5		µs
Slew Rate			15		V/µs
Current Models					
Settling Time (3)	to ±0.01% of FSR for FSR Change				
10 to 100Ω load			300		ns
1KΩ load			1.0		µs

PARAMETER	CONDITIONS	HI-5685			
		MIN	TYP	MAX	UNITS
ANALOG OUTPUT					
Voltage Models					
Output Current		±5			mA
Output Impedance (DC)			0.05		Ω
Current Models					
Output Current	Full Scale				
Unipolar			−2		mA
Bipolar			±1		mA
Output Resistance					
Unipolar			3.2		KΩ
Bipolar			6.65		KΩ
Compliance (3)		−2.5		+10	V
INTERNAL REFERENCE					
Output voltage		+6.174	+6.3	+6.426	V
Output Impedance			1.5		Ω
External Current				+2.5	mA
Tempco of Drift			±10	±20	PPM/°C
POWER SUPPLY SENSITIVITY (3)					
+15V			.002		$\frac{\%FSR}{\Delta V_S}$
−15V			.002		
+5V			.002		
POWER SUPPLY REQUIREMENTS(5)					
Range					
+15V		+11.4	+15	+16.5	V
−15V		−11.4	−15	−16.5	V
+5V		+4.5	+5	+16.5	V
Current					
+15V			8	16	mA
−15V			-12	-24	mA
+5V			4.5	9	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Adjustable to zero using external potentiometers.
3. See Definitions.
4. FSR is "full scale range" and is 20V for ±10V range, 10V for ±5V range, etc., or 2mA (±20%) for current output.
5. The HI-5685 will operate with supply voltages as low as ±11.4V. It is recommended that output voltage range −10V to +10V not be used if the supply voltages are less than ±12.5V.

HARRIS

HI-5687

Wide Temperature Range Monolithic 12 Bit Digital-to-Analog Converter

FEATURES

- DAC 87 ALTERNATE SOURCE
- MONOLITHIC CONSTRUCTION (SINGLE CHIP)
- FAST SETTLING
- GUARANTEED SPECIFICATIONS −55°C to 125°C
- WAFER LASER TRIMMED
- APPLICATIONS RESISTORS ON-CHIP
- ON-BOARD REFERENCE
- DIELECTRIC ISOLATION (DI) PROCESSING
- ±12V POWER SUPPLY OPERATION
- MIL STD 883 PROCESSING AVAILABLE

APPLICATIONS

- HIGH SPEED A/D CONVERTERS
- PRECISION INSTRUMENTATION
- CRT DISPLAY GENERATION

DESCRIPTION

The HI-5687 is a monolithic direct replacement for the popular DAC87-CBI wide temperature range d-to-a converter. Single chip construction, along with several design innovations make the HI-5687 the optimum choice for low cost, high reliability applications.

Harris' unique Dielectric Isolation (DI) processing reduces internal parasitics resulting in fast switching times and minimum glitch. On board span resistors are provided for good tracking over temperature, and are laser trimmed to high accuracy. These may be used with the on-board op-amp (voltage output models; HI-5687V), or with a user supplied external amplifier (HI-5687I).

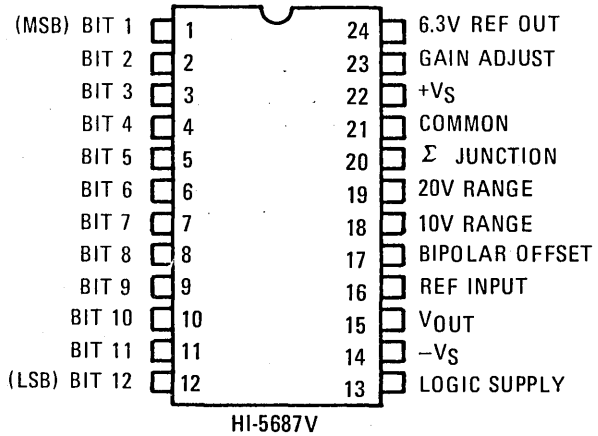
Internally, the HI-5687 eliminates code dependent ground currents by routing current from the positive supply to the internal ground mode, as determined by an auxiliary R-2R ladder. This results in a cancellation of code dependent ground currents allowing virtually zero variation in current through the package common, pin 21.

The HI-5687 is available in both current and voltage output models which are 100% tested over the −55°C to +125°C temperature range. All models include a buried zener reference featuring low temperature coefficient. In addition, the voltage output models include an on-board output amplifier. Both versions operate with a +5V logic supply and a $\pm V_S$ in the range of ±(11.4V to 16.5V).

Processing to MIL-STD-883A CLASS B is available.
See Ordering Information.

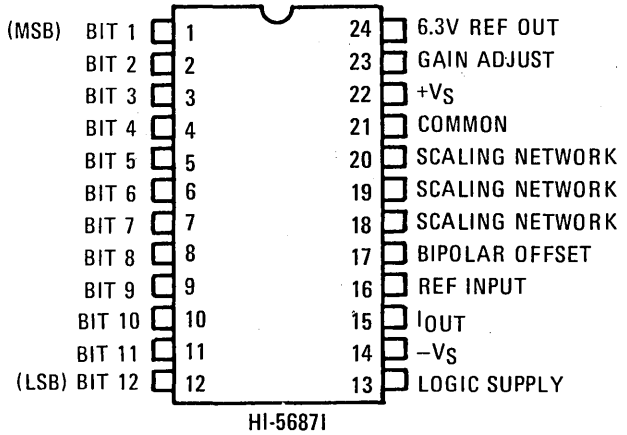
PINOUTS

TOP VIEW



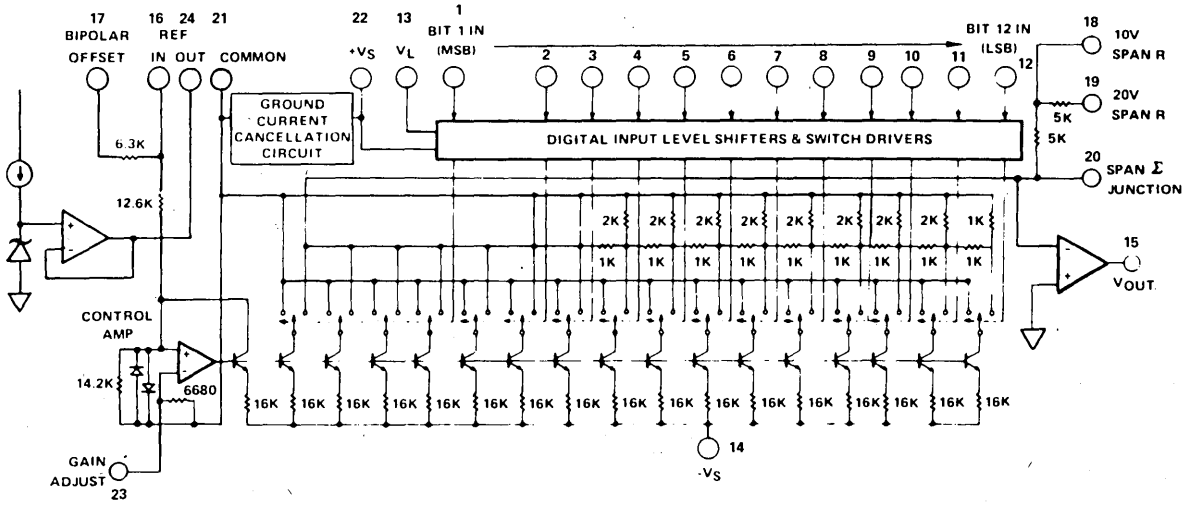
HI-5687V
VOLTAGE OUTPUT

TOP VIEW



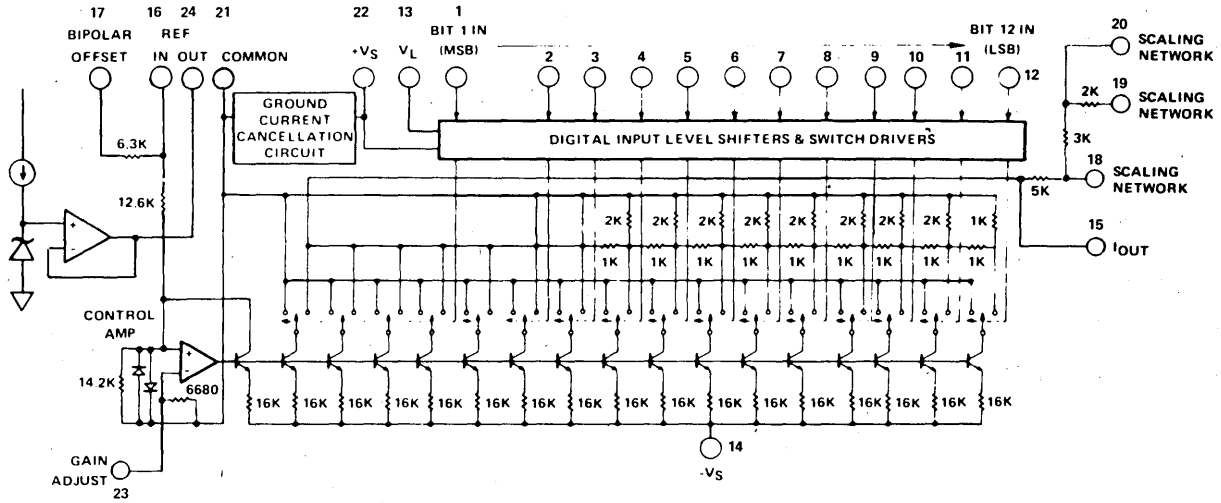
HI-5687I
CURRENT OUTPUT

FUNCTIONAL DIAGRAM VOLTAGE OUTPUT



HI-5687V

FUNCTIONAL DIAGRAM CURRENT OUTPUT



HI-5687I

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (1)

Power Supply Inputs	$+V_S$	+20V	Power Dissipation	Pd, Package	1000mW
	$-V_S$	−20V			
	$+V_{LOGIC}$	+20V	Operating Temperature Range		
				HI-5687I/V-2	−55°C to +125°C
Reference	Input (pin 16)	$\pm V_S$		HI-5687I/V-8	−55°C to +125°C
	Output drain	2.5mA			
			Storage Temperature Range		−65°C to +150°C
Digital Inputs	Bits 1 to 12	−1V to +12V			

ELECTRICAL SPECIFICATIONS

(T_A = +25°C, V_S = ±15V, V_{LOGIC} = +5V, PIN 16 CONNECTED TO PIN 24 UNLESS OTHERWISE SPECIFIED.)

PARAMETER	CONDITIONS	HI-5687 MIN	HI-5687 TYP	HI-5687 MAX	UNITS
DIGITAL INPUT (3)					
Resolution				12	Bits
Logic Levels	TTL Compatible				
Logic "1"	at +1μA	+2		+5.5	V
Logic "0"	at −100μA	0		+0.8	V
ACCURACY (3)					
Linearity Error	At +25°C		±¼	±½	LSB
	−55°C to +125°C			+¾	LSB
Differential Lin. Error	at +25°C			±¾	LSB
	−55°C to +125°C		±½	±1	LSB (4)
Gain Error (2)	−55°C to +125°C		±0.1	±0.2	%FSR
Offset Error (2)	−55°C to +125°C		±0.05	±0.1	%FSR
Monotonicity			GUARANTEED		
DRIFT (3)	−55°C to +125°C				
Total Bipolar Drift (includes gain, offset offset and linearity drifts)			±15	±30	PPM/°C
Total Error					
Unipolar			±0.13	±0.3	%FSR
Bipolar			±0.12	±0.24	%FSR
Gain					
including internal reference			±10	±25	PPM/°C
excluding internal reference			±5	±10	PPM/°C
Unipolar Offset			±1	±3	PPM/°C
CONVERSION SPEED					
Voltage Models					
Settling Time (3)	to ±0.01% of FSR for FSR Change				
With 10KΩ Feedback			3		μs
With 5KΩ Feedback			1.5		μs
For 1 LSB Change			1.5		μs
Slew Rate			15		V/μs
Current Models					
Settling Time (3)	to ±0.01% of FSR for FSR Change				
10 to 100Ω load			300		ns
1KΩ load			1.0		μs

PARAMETER	CONDITIONS	HI-5687			
		MIN	TYP	MAX	UNITS
ANALOG OUTPUT					
Voltage Models					
Output Current		+5			mA
Output Impedance (DC)			0.05		Ω
Current Models					
Output Current	Full Scale				
Unipolar			−2		mA
Bipolar			±1		mA
Output Impedance					
Unipolar		5.0	6.6	8.2	KΩ
Bipolar		2.5	3.3	4.1	KΩ
Compliance (3)		−1.5		+ 10.5	V
INTERNAL REFERENCE					
Output Voltage		+6.174	+6.3	+6.426	V
Output Impedance			1.5		Ω
External Current				+2.5	mA
Tempco of Drift			±5	±10	PPM/°C
POWER SUPPLY SENSITIVITY (3)					
+15V			±.002	±.003	$\frac{\%FSR}{\Delta V_S}$
−15V			±.002	±.003	
+5V			±.002	±.003	
POWER SUPPLY REQUIREMENTS (5)					
Range					
+15V		+11.4	+15	+16.5	V
−15V		−11.4	−15	−16.5	V
+5V		+4.5	+5	+16.5	V
Current					
+15V			8	16	mA
−15V			-12	-24	mA
+5V			4.5	9	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Adjustable to zero using external potentiometers.
3. See Definitions.
4. FSR is a "full scale range" and is 20V for ±10V range, 10V for ±5V range, etc., or 2mA (±20%) for current output.
5. The HI-5687 will operate with supply voltages as low as ±11.4V. It is recommended that output voltage ranges −10V to +10V and not be used if the supply voltages are less than ±12.5V.

HARRIS

HI-5712/5712A

High Performance 12 Bit Analog to Digital Converter

FEATURES

- MICROPROCESSOR COMPATIBLE
- CONVERSION TIME 10μsec MAX OVER TEMP.
- NO MISSING CODES OVER TEMPERATURE
- INTERNAL +10V REFERENCE
- INTERNAL CLOCK WITH EXTERNAL OVERRIDE CAPABILITY
- SERIAL OUTPUT
- TTL/CMOS COMPATIBLE
- TRISTATE PARALLEL OUTPUTS
- 40 PIN DIP
- MIL-STD-883 PROCESSING AVAILABLE

APPLICATIONS

- MULTI-CHANNEL DATA ACQUISITION SYSTEMS
- STATUS MONITORING SYSTEMS
- PROCESS CONTROL SYSTEMS
- INSTRUMENTATION
- HIGH RELIABILITY DAS's

DESCRIPTION

The HI-5712/5712A is a 12-bit successive approximation analog-to-digital converter (ADC) intended for high-speed, high-performance data conversion applications. An 8μs conversion time for an accurate 12 bit conversion with low gain and offset temperature coefficients are among its many features. Numerous functions can be software controlled to meet a variety of ADC requirements.

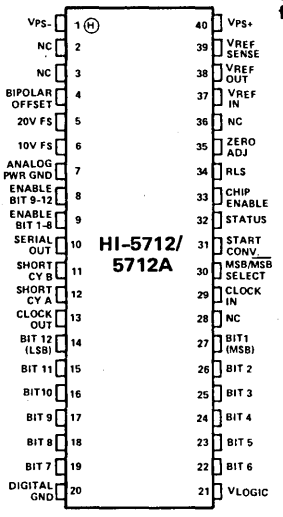
The highly flexible input design accepts user programmed unipolar and bipolar inputs of: 0 to +10V, 0 to +20V, ±5V and ±10V full scale signal levels. The internal precision +10V reference delivers up to 10mA of output current with ultra high temperature stability. This reference is intended for biasing the ADC reference input, although other configurations can be implemented. A remote sense line is provided for applications requiring usage of the precision reference elsewhere in the system.

The output code select line and the short cycle control inputs are latched internally for microprocessor compatibility and provide selection of either binary or 2's complement output code, and resolution of 6, 8, 10 or 12 bits, respectively. A flexible interface is provided for 8, 12 and 16 bit systems via the chip select line and the word length control pins. The latter allows independent tri-state enabling of parallel output bits 1-8 and 9-12. A serial data output line is provided for applications requiring remote data transmission.

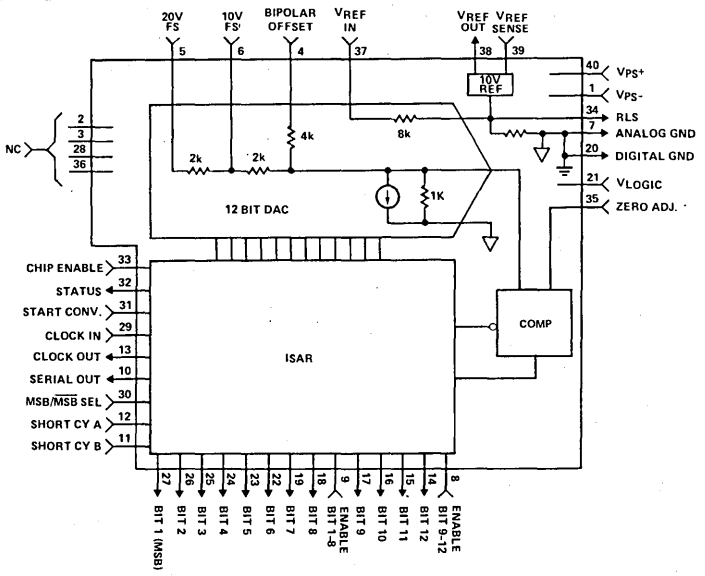
The HI-5712/5712A is manufactured with hermetically sealed leadless chip carriers (LCC's) mounted to both sides of a multi-layer ceramic substrate which results in a compact 40 pin dual-in-line package. The HI-5712A is intended for military, industrial and instrumentation applications. MIL-STD-883 class B and high reliability commercial grades are both available as standard products.

PINOUT

Section 11 for Packaging



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Power Supply Inputs		Power Dissipation (Pd) 2 Watts	
V_{PS}^+	+20V	Operating Temperature Range	
V_{PS}^-	-20V	HI-5712-2, HI-5712A-2	55°C to +125°C
V_{LOGIC}	+10V	HI-5712-5, HI-5712A-5	0°C to +75°C
V_{REF} IN (Pin 37)	0V, V_{PS}^+	HI-5712-7, HI-5712A-7	0°C to +75°C (Hi Rel)
V_{REF} SENSE (Pin 39)	0V, V_{PS}^+	HI-5712-8, HI-5712A-8	-55°C to +125°C (Hi Rel)
Digital Inputs	-1V, V_{LOGIC}	Storage Temperature Range	
			65°C to +150°C

ELECTRICAL CHARACTERISTICS

(T_A = +25°C, V_{PS} = +15V, V_{PS}^- = -15V, V_{LOGIC} = +5V, V_{REF} In = Internal V_{REF}, Full Scale = +10V, Conversion Speed = 9 μs TYP (Internal Clock), 12-BIT Conversion, Unless otherwise noted.)

				HI-5712A-2 HI-5712-2 HI-5712A-8 HI-5712-8			HI-5712A-5 HI-5712-5 HI-5712A-7 HI-5712-7		
PARAMETER		TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION		Full			12			12	BITS
NONLINEARITY	HI-5712A	+25°C		±1/4	±1/2		±1/4	±1/2	LSB
		Full		±1/4	±1/2		±1/4	±1/2	LSB
	HI-5712	+25°C		±1/4	±1/2		±1/4	±1/2	LSB
		Full		±1/2	±1		±1/2	±1	LSB
DIFFERENTIAL NONLINEARITY	HI-5712A	+25°C		±1/4	±1/2		±1/4	±1/2	LSB
		Full		±1/4	±1/2		±1/4	±1/2	LSB
	HI-5712	+25°C		±1/4	±1/2		±1/4	±1/2	LSB
		Full		±1/2	±1		±1/2	±1	LSB
		NO MISSING CODES GUARANTEED OVER TEMPERATURE							
INHERENT QUANTIZATION ERROR		Full			±1/2			±1/2	LSB
UNIPOLAR OFFSET ERROR (Note 2) (Adjustable to Zero)		+25°C		.3	.6		.3	.6	%FSR
BIPOLAR OFFSET ERROR (Note 2) (Adjustable to Zero)		+25°C		.3	.6		.3	.6	%FSR
GAIN ERROR (note 2) (Adjustable to Zero)		+25°C		.1	.3		.1	.3	%FSR
ADJUSTMENT RANGE									
UNIPOLAR OFFSET		+25°C	±1	±2		±1	±2		%FSR
BIPOLAR OFFSET		+25°C	±1	±2		±1	±2		%FSR
GAIN		+25°C			.3			.3	%FSR
TEMPERATURE STABILITY (With Internal V_{REF})									
UNIPOLAR OFFSET DRIFT	HI-5712A	Full		±2	±5		±2	±5	ppm FSR/°C
	HI-5712	Full		±4	±15		±4	±15	ppm FSR/°C
BIPOLAR OFFSET DRIFT	HI-5712A	Full		±4	±10		±4	±10	ppm FSR/°C
	HI-5712	Full		±8	±25		±8	±25	ppm FSR/°C
GAIN DRIFT	HI-5712A	Full		±5	±10		±5	±10	ppm FSR/°C
	HI-5712	Full		±10	±20		±10	±20	ppm FSR/°C
		NO MISSING CODES GUARANTEED OVER TEMPERATURE							

SPECIFICATIONS (Continued)

PARAMETER	TEMP	HI-5712A-2/-8 HI-5712-2/-8 MIN	TYP	MAX	HI-5712A-5/-7 HI-5712-5/-7 MIN	TYP	MAX	UNITS
CONVERSION SPEED (Internal Clock)								
12 BIT	+25°C		9.0	10.0		9.0	10.0	µs
10 BIT	"		6.8	8.5		6.8	8.5	µs
8 BIT	"		5.6	7.0		5.6	7.0	µs
6 BIT	"		4.4	5.4		4.4	5.4	µs
MAXIMUM CONVERSION SPEED AT 12 BITS WITH EXTERNAL CLOCK (Note 3)	Full		6.5			6.5		µs
ANALOG INPUT CHARACTERISTICS								
INPUT VOLTAGE RANGE								
UNIPOLAR	Full	10			10			V
	Full	20			20			V
BIPOLAR	Full	±5	±5		±5	±5		V
	Full	±10	±10		±10	±10		V
INPUT IMPEDANCE								
10V FS (PIN 6)	Full	1.6	2	2.4	1.6	2	2.4	KΩ
20V FS (PIN 5)	Full	3.2	4	4.8	3.2	4	4.8	KΩ
V_{REF} IN (PIN 37)	Full	6.4	8	9.6	6.4	8	9.6	KΩ
ANALOG OUTPUT CHARACTERISTICS								
V_{REF} OUTPUT VOLTAGE	+25°C	9.970	10.000	10.030	9.970	10.000	10.030	V
V_{REF} OUTPUT CURRENT	Full	10			10			mA
VREF OUTPUT TC HI-5712A	Full		±10	±15		±10	±15	ppm FSR/°C
VREF OUTPUT TC HI-5712	Full		±10	±15		±10	±15	ppm FSR/°C
DIGITAL INPUT CHARACTERISTICS								
INPUT VOLTAGE (Note 8)								
LOGIC 1	Full	3.3	2.7		3.3	2.7		V
LOGIC 0	Full		1.2	.8		1.2	.8	V
INPUT CURRENT (Note 8)								
LOGIC 1 (VCC)	Full	-25	0	+25	-25	0	+25	µA
LOGIC 0 (GND)	Full		-200	-400		-200	-400	µA
ETERNAL CLOCK (Note 3)	Full			2.5			2.5	MHz
DIGITAL OUTPUT CHARACTERISTICS								
OUTPUT VOLTAGE								
LOGIC 1 I_{OH} = -800 A	Full	3.5	4.0		3.5	4.0		V
LOGIC 0 I_{OL} = +3.2mA	Full	.2	.4			.2	.4	V
OUTPUT CURRENT								
LOGIC 1 VO = 3.5V	Full	-800	-1000		-800	-1000		µA
LOGIC 0 VO = .4V	Full	3.2	4.0		3.2	4.0		mA
DIGITAL INPUT TIMING CHARACTERISTICS								
CHIP ENABLE TO START CONVERT t_{cd}	Full	50			50			nsec
START CONVERT PULSE LOW t_{scl}	Full	100			100			nsec
START CONVERT PULSE HIGH t_{sch}	Full	50			50			nsec
CONTROL SETUP TIME t_s	Full	100			100			nsec
CONTROL HOLD TIME t_h	Full	100			100			nsec
CLOCK INPUT LOW t_{pwl}	Full	125			125			nsec
CLOCK INPUT HIGH t_{pwh}	Full	150			150			nsec
CLOCK INPUT PERIOD t_{cl}	Full	400			400			nsec
ENABLE 1-8, 9-12 PULSE WIDTH t_{em}	Full	100			100			nsec

PARAMETER	TEMP	HI-5712A-2/-8 HI-5712-2/-8 MIN	TYP	MAX	HI-5712A-5/-7 HI-5712-5/-7 MIN	TYP	MAX	UNITS
DIGITAL OUTPUT TIMING CHARACTERISTICS (See Figure 6)								
THREE STATE ENABLE DELAY t_{oe}	Full		40	50		40	50	nsec
THREE STATE DISABLE DELAY t_{od}	Full		60	100		60	100	nsec
START CONVERT TO STATUS DELAY t_{sd}	Full		70	100		70	100	nsec
START CONVERT TO CLOCK OUT DELAY t_{scd}			200	500		200	500	nsec
CLOCK TO SERIAL OUT DELAY t_{psd}	Full	100	150	200	100	150	200	nsec
LAST CLOCK TO STATUS DELAY t_{scdt}	Full	50	75	100	50	75	100	nsec
PARALLEL DATA TO STATUS DELAY t_{ds}	Full	50	75		50	75		nsec
LAST SERIAL BIT TO STATUS DELAY t_{da}	Full	50	75		50	75		nsec
CLOCK INPUT TO CLOCK OUT DELAY t_{dcl}	Full		25	50		25	50	nsec
PARALLEL DATA OUTPUT CODES								
UNIPOLAR (Note 4)	Positive True Binary							
BIPOLAR (Note 4)	Positive True Offset Binary							
	Positive True Two's Complement Binary							
SERIAL DATA OUTPUT CODE	Positive True NRZ Code							
POWER SUPPLY REQUIREMENTS (Note 5)								
V_{ps}^+	Full	+13.5	+15	+16.5	+13.5	+15	+16.5	V
V_{ps}^-	Full	-13.5	-15	-16.5	-13.5	-15	-16.5	V
V_{LOGIC}	Full	+4.5	+5	+5.5	+4.75	+5	+5.25	V
I_{ps}^+	Full		27	35		27	35	mA
I_{ps}^-	Full		42	50		42	50	mA
I_{LOGIC}	Full		4.5	15		4.5	15	mA
POWER SUPPLY SENSITIVITY (Note 6)								
V_{ps}^+ = +13.5V to +16.5V V_{ps}^- = -15V, V_{LOGIC} = +5V								
UNIPOLAR OFFSET			2	5		2	5	ppm of FSR/ %ΔP.S.
BIPOLAR OFFSET			2	4		2	4	
GAIN			1	3		1	3	
V_{ps}^- = -13.5V to -16.5V V_{ps}^+ = +15V, V_{LOGIC} = +5V								
UNIPOLAR OFFSET			2	5		2	5	
BIPOLAR OFFSET			2	4		2	4	
GAIN			1	3		1	3	
V_{LOGIC} = +4.5V to +5.5V V_{ps}^+ = +15V, Vps- = -15V CONVERSION SPEED (12 Bit with Internal Clock)			±5	±10		±5	±10	%

NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. See Figure 2 for connections. The initial errors are adjustable to zero by using external trim potentiometers as shown in Figure 3, and 4.
3. The HI-5712A will operate at these speeds (for 12 bit conversion), but parametric performance is not guaranteed.
4. See operating instructions for details.
5. After 60 seconds warm-up.
6. See definitions.
7. These terminals will be used in the future for additional functions. Do not make connections to these pins in your system.
8. TTL compatibility guaranteed.

PIN FUNCTIONS AND DESCRIPTIONS

PIN	SYMBOL	DESCRIPTION
1	V_{PS}-	-15V Power Supply Terminal
2	NC	No Connection See Note 7
3	NC	No Connection See Note 7
4	BIPOLAR OFFSET	Connect to V_{REF} for Bipolar Input Mode. See Operating Instructions for Details.
5	20V FS	20V Full Scale Analog Input
6	10V FS	10V Full Scale Analog Input
7	ANALOG GND	Analog Power Supply Return
8	ENABLE BIT 9-12	Output "Three State" Control. An Input "0" Enables Bits 9 through 12, whereas a "1" Switches these Bits to a High Impedance State.
9	ENABLE BIT 1-8	Output "Three State" Control. An Input "0" Enables Bits 1 through 8, whereas a "1" Switches these Bits to a High Impedance State.
10	SERIAL OUT	NRZ Serial Data Output. To be used in Conjunction with Clock Out for Remote Data Transmission
11	SHORT CY B	See Description for Pin 12
12	SHORT CY A	Digital Inputs Applied to short cycle A and B selects a conversion of 6, 8, 10, or 12-bits:

BITS	SHORT CY A	SHORT CY B
6	0	0
8	0	1
10	1	0
12	1	1

PIN	SYMBOL	DESCRIPTION
13	CLOCK OUT	SAR Clock Output. Used for Decoding Serial Out Data
14	BIT 12	Output Data Bit (LSB)
15	BIT 11	Output Data Bit
16	BIT 10	Output Data Bit
17	BIT 9	Output Data Bit
18	BIT 8	Output Data Bit
19	BIT 7	Output Data Bit
20	DIGITAL GND	Digital Power Supply Return
21	V_{LOGIC}	+5V Power Supply Terminal
22	BIT 6	Output Data Bit
23	BIT 5	Output Data Bit
24	BIT 4	Output Data Bit
25	BIT 3	Output Data Bit
26	BIT 2	Output Data Bit
27	BIT 1	Output Data Bit (MSB)
28	NC	No Connection. See Note 7.
29	CLOCK IN	An External Clock Signal Applied to this Input Overrides the Internal Clock.
30	MSB/$\overline{\text{MSB}}$ SEL	Digital Input Pin. A "1" Applied to this Terminal Selects a Straight Binary or Offset Binary Output Code. A "0" Inverts the MSB to Yield a 2's Complement Binary Output Code.
31	START CONV	Digital Input Pin. A High to Low Transition Initiates the ADC Conversion Cycle.
32	STATUS	Digital Output Pin. A "1" Indicates that the ADC is Busy, While a "0" Denotes that Conversion is Completed and Data is Ready for Retrieval.

PIN FUNCTIONS AND DESCRIPTIONS

PIN	SYMBOL	DESCRIPTION
33	CHIP ENABLE	Digital Input Pin. A "1" Forces the Output Data, Serial Out and Status Terminals to a High Impedance State and the ADC is Disabled. A "0" Enables these ADC Functions.
34	RLS	Reference Low Sense.
35	ZERO ADJ	External Zero Adjustment Pin, See Operating Instructions for Details.
36	NC	No Connection. See Note 7.
37	V_{REF} IN	+10V Reference Input to ADC.
38	V_{REF} OUT	Internal +10V Reference Output, Normally Connected to V_{REF} IN (Pin 37).
39	V_{REF} SENSE	Internal +10V Reference Sensing Terminal, Normally connected to V_{REF} Out (Pin 38). See Operating Instructions for Details.
40	V_{ps+}	+15V Power Supply Terminal.

APPLYING THE HI-5712/5712A

OPERATING INSTRUCTIONS

Conventional ADC systems provide maximum performance when the analog and digital ground lines are tied together at the ADC terminals. This minimizes analog interference due to digital switching noise. For optimum performance, this external grounding procedure should be followed in HI-5712/5712A installations to reinforce the unit's internal analog-to-digital ground connections. Under no circumstances should the Reference Low Sense (RLS) terminal (Pin 34) be connected to system ground.

In practice, the Reference Low Sense (RLS) terminal (Pin 34) normally is connected to zero adjust (or error amplifier) input terminal (Pin 35), either directly or through an appropriate resistor network. See figures 3 and 4.

On the HI-5712/5712A substrate, the power supply lines to each active component are bypassed to ground with 0.01 μF chip capacitors for high frequency noise rejection. For best accuracy, the grounding and decoupling schemes shown in Figures 3 and 4 are recommended. The 10μF bypass capacitors shown should be connected as close as possible to the HI-5712/5712A, preferably at the device pin.

For applications where usage of potentiometers is highly undesirable, the trim pots shown in Figures 3 and 4 can either be deleted or replaced by precision fixed resistors. (Delete R_3 and R_4; replace R_1 with 25 ohms). When precision fixed resistors are used, the initial offset error and gain error contributions are as specified in page 2.

NOTE: The HI-5712/5712A may latch up if the device is enabled before applying power. Disabling the device following power turn on will remedy this situation. Care supplies do not excessively overshoot their final value during turn on.

CONTROL AND INTERFACE

The HI-5712/5712A features a versatile set of controlling functions which allows a wide variety of applications, including microprocessor bus interfacing.

When the chip enable is set to low, the internal registers are enabled, and the output data lines can be enabled via the output enable control lines. The conversion cycle is initiated at the falling edge of the start conversion pulse. At this time, the MSB/MSB Select, Short Cycle A, and Short Cycle B control information is latched into the internal registers. The status line is also forced into an active high state indicating that a conversion is taking place. At the end of the conversion cycle the status line will be set to low to signify that the data is ready at the tri-state buffers. The various timing relationships are shown in Figure 1.

There are two distinct modes of operation, namely, continuous conversion and single step conversion. Continuous conversion can be easily achieved by connecting the Status line to the Start Convert pin. In this application, an indecision state may occur during the initial power-on conditions. Normal operation is restored by pulsing the chip enable pin to logic high for a period greater than 100 ns.

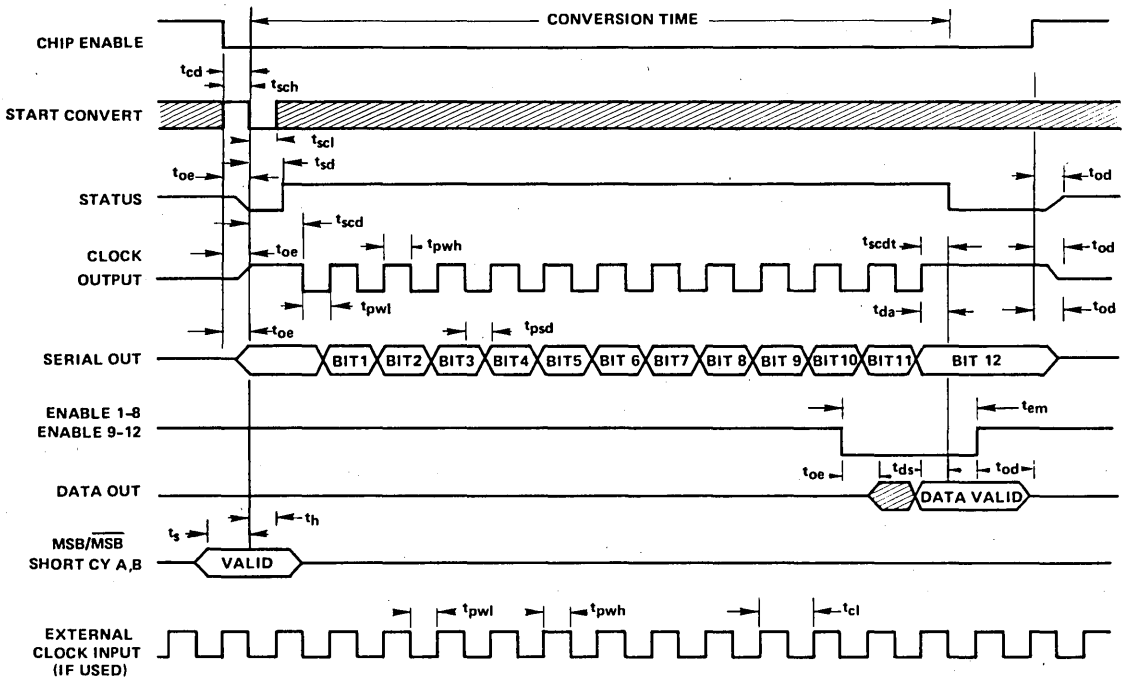


FIGURE 1. HI-5712/5712A TIMING DIAGRAM

REMOTE DATA TRANSMISSION

The Serial Data Out is mainly used for remote data transmission, where only a limited number of wires are available.

Serial Output is bit by bit (MSB first, LSB last) in a NRZ (nonreturn-to-zero) format. It changes state only at the positive going edges of the Clock Out, and remains valid during the whole clock period. Parallel data can be constructed by clocking the serial data into a receiving shift register.

In order to minimize transmission error, the negative-going edge of the clock should be used to clock data into the remote shift register. The parallel data will be valid once the status line returns to low. The clocking scheme is shown in Figure 1.

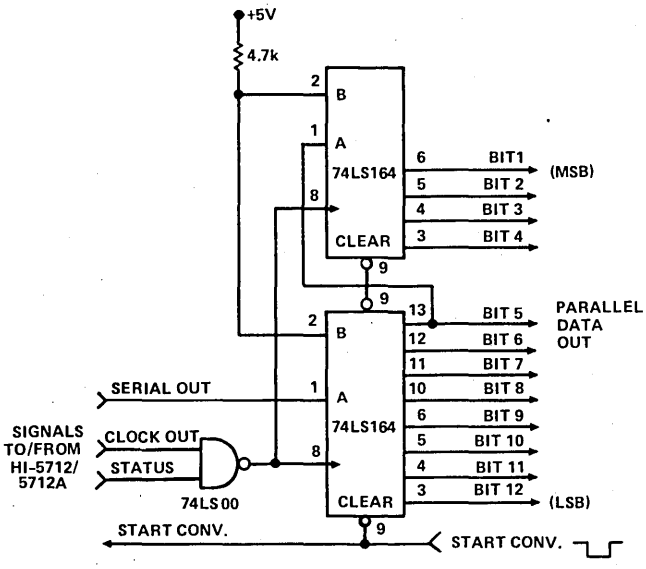


FIGURE 2. DECODING SERIAL DATA OUT

HI-5712/5712A CALIBRATION CHART

OPERATING MODE	ANALOG INPUT CONNECTION	R2 BIAS RESISTOR	MSB/MSB SELECT PIN 30	OFFSET ADJUST ANALOG INPUT VOLTAGE	ADJUST R3 FOR DITHER BETWEEN CODES	GAIN ADJUST ANALOG INPUT VOLTAGE	ADJUST R1 FOR DITHER BETWEEN CODES	LSB WEIGHT
UNIPOLAR STRAIGHT BINARY 0V to +10V	10VFS PIN 6	667Ω	HIGH	+1.22mV	0000 0000 0000 0000 0000 0001	+9.9963V	1111 1111 1110 1111 1111 1111	2.44mV
UNIPOLAR STRAIGHT BINARY 0V to +20V	20VFS PIN 5	800Ω	HIGH	+2.44mV	0000 0000 0000 0000 0000 0001	+19.9927V	1111 1111 1110 1111 1111 1111	4.88mV
BIPOLAR OFFSET BINARY -5V to +5V	10VFS PIN 6	580Ω	HIGH	-4.9988V	0000 0000 0000 0000 0000 0001	+4.9963V	1111 1111 1110 0111 1111 1111	2.44mV
BIPOLAR OFFSET BINARY -10V to +10V	20V FS PIN 5	667Ω	HIGH	-9.9976V	0000 0000 0000 0000 0000 0001	+9.9927V	1111 1111 1110 1111 1111 1111	4.88mV
BIPOLAR 2's COMPLEMENT -5V to +5V	10V FS PIN 5	580Ω	LOW	-4.9988V	1000 0000 0000 1000 0000 0001	+4.9963V	0111 1111 1110 0111 1111 1111	2.44mV
BIPOLAR 2's COMPLEMENT 10V to +10V	20V FS PIN 6	667Ω	LOW	-9.9976V	1000 0000 0000 1000 0000 0001	+9.9927V	0111 1111 1110 0111 1111 1111	4.88mV

CALIBRATION PROCEDURE- Refer to Calibration Chart and to Figures 3 and 4 for appropriate analog input connections, value of bias resistor, and MSB/MSB select.

STEP 1 OFFSET ADJUSTMENT

- Set analog input to the appropriate value for offset adjustment.
- Adjust R3 for dither between codes shown in calibration chart.

STEP 2 GAIN ADJUSTMENT

- Set analog input to the appropriate value for gain adjustment.
- Adjust R1 for dither between codes shown in calibration chart.

NOTE: This calibration procedure insures that the transfer characteristic produced by connecting the midpoints of all quantization intervals passes through the origin.

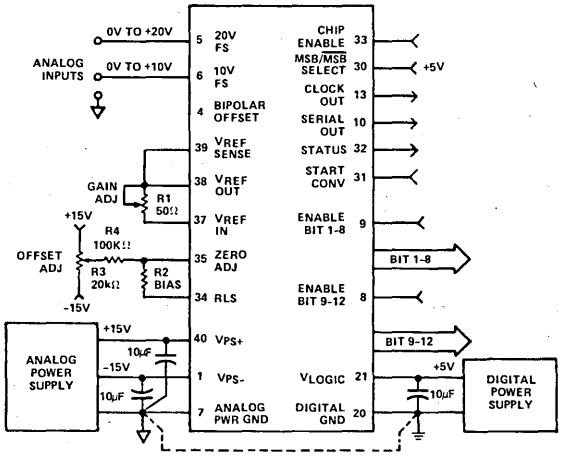


FIGURE 3. UNIPOLAR INPUT CONNECTIONS - STRAIGHT BINARY OUTPUT CODE

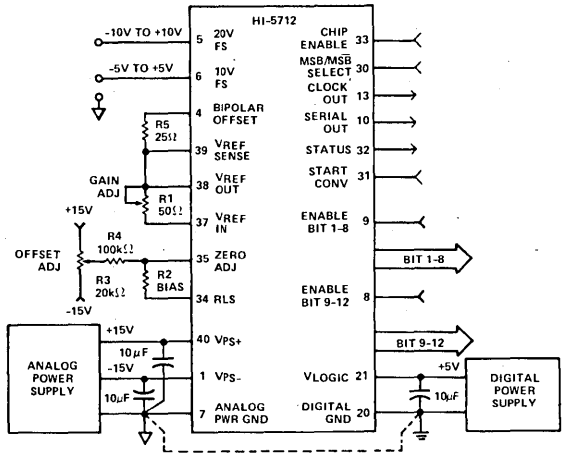


FIGURE 4. BIPOLAR INPUT CONNECTIONS

HARRIS

HI-574A

ADVANCE

Fast, Complete 12-Bit Analog to Digital Converter with Microprocessor Interface

FEATURES

- AD574A SECOND SOURCE
- LOW POWER 360mW
- COMPLETE 12-BIT A/D CONVERTER WITH REFERENCE AND CLOCK
- FULL 8 OR 16-BIT μP INTERFACE
- FAST SUCCESSIVE APPROXIMATION CONVERSION 25μs
- COMPOUND MONOLITHIC CONSTRUCTION
- NO MISSING CODES OVER TEMPERATURE
- LOW GAIN T.C. 10ppm/°C
- LOW COST

APPLICATIONS

- HIGH PERFORMANCE DATA ACQUISITION SYSTEMS
- PRECISION INSTRUMENTATION
- MILITARY AND INDUSTRIAL SYSTEMS

DESCRIPTION

The Harris HI-574A is a complete 12-bit analog-to-digital converter. Successive approximation conversion is performed by two monolithic chips housed in a 28-pin dual-in-line package. This compound monolithic circuit combines Harris' CMOS and Bipolar processes.

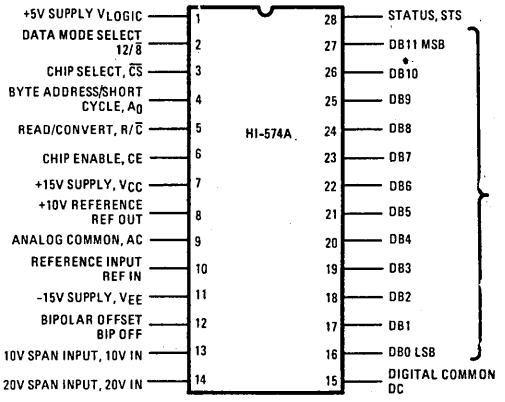
Designed as a direct replacement for the AD574A, the device offers full microprocessor compatibility by both 8 and 16-bit systems via "Three State" output buffer circuitry. Wafer level laser trimming techniques provide close match of ladder resistors, ensuring high accuracy plus a guarantee of no missing codes over temperature. Included in the A/D converter are a 12-bit, high performance digital-to-analog converter, a very stable voltage reference, and an accurate comparator.

In systems where power consumption must be minimized, Harris offers a significant improvement over other manufacturers units. The HI-574A dissipates typically 400mW.

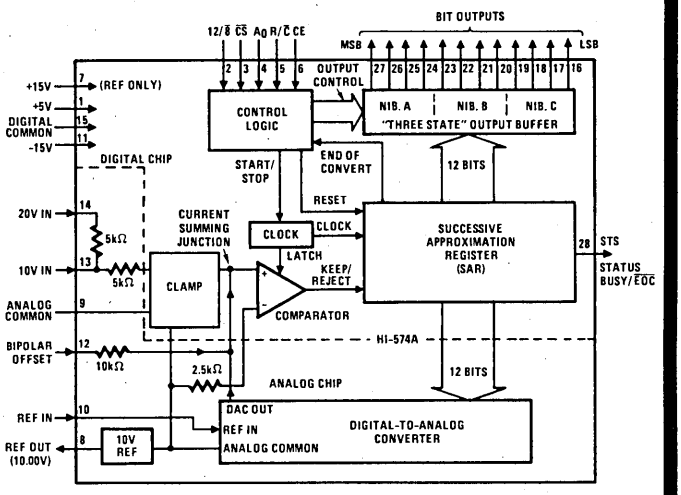
The HI-574A is available in versions which have guaranteed performance over both military and commercial temperature ranges. Screening to MIL-STD-883A, Class B is also available.

PINOUT

TOP VIEW



FUNCTIONAL DIAGRAM



HARRIS

HI-5900

Analog Data Acquisition Signal Processor

FEATURES

- INPUT OVERVOLTAGE PROTECTION
- 50kHz THROUGHPUT
- 12-BIT ACCURACY
- OUTPUT TRACK/HOLD AMPLIFIER
- ZERO OFFSET ADJUSTMENT
- DIFFERENTIAL INPUT CHANNELS
- SOFTWARE CONTROLLED GAIN AND CHANNEL SELECT
- 85dB CMRR
- COMPACT 32 PIN DIP
- MIL-STD-883 SCREENING AVAILABLE

APPLICATIONS

- HIGH PERFORMANCE DATA ACQUISITION
- MILITARY SYSTEMS

DESCRIPTION

The HI-5900 comprises "front end" components of a data acquisition system including an eight channel differential multiplexer, programmable gain instrumentation amplifier (PGA), and Track and Hold amplifier. Adding a timing circuit and one A to D converter yields a complete data acquisition system. A 50kHz channel-to-channel throughput rate is achieved when the HI-5900 is used with a fast 12 bit A to D converter such as HARRIS HI-5712.

Each output line of the input multiplexer is buffered by a high-quality non-inverting amplifier. This isolates each line from source resistances external to the 5900, preserving the high CMRR of the instrumentation amplifier block. Also, the buffers provide a high input impedance for each channel.

The PGA, which includes an op amp, a monolithic resistor network and a four channel differential multiplexer, offers precision gain values of 1,2,4, and 8. The voltage gain is selected by a two bit digital word. The output of the PGA drives the Track and Hold amplifier, and the ground side of the PGA is isolated by a buffer amplifier to maintain a high CMRR.

The output Track/Hold amplifier is a monolithic device, internally connected for non-inverting unity gain. In the sample mode is operates as a high performance buffer amplifier. With an external holding capacitor, it may be switched to HOLD with an aperture delay of 50ns and 10pC of charge transfer.

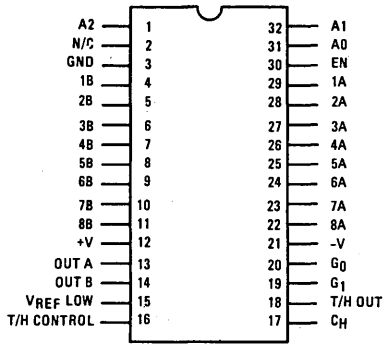
The packaging technique involves monolithic chips mounted in leadless chip carriers (LCC's) and soldered to both sides of a multilayer ceramic substrate. Each LCC may undergo reliability screening such as MIL-STD-883, Method 5004/Class B, before assembly on the substrate. The resulting package is a compact 32 pin DIP.

The HI-5900 is offered as a high performance front-end section for military and industrial data acquisition systems. It is designed for interface with computers and is well suited for high-rel applications.

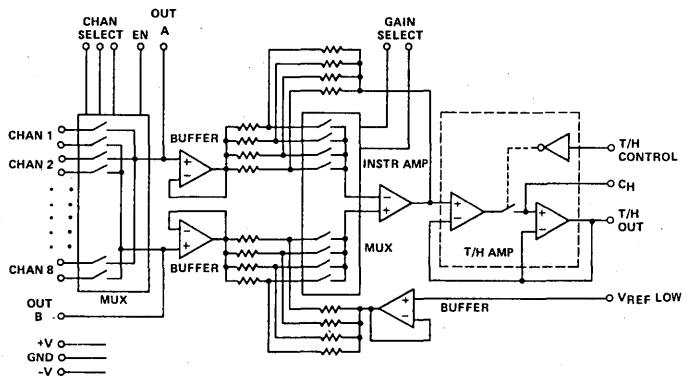
PINOUT

Section 11 for Packaging

TOP VIEW



FUNCTIONAL DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V- Terminals 40V
Digital Input Overvoltage (Multiplexers)
V_{Supply} (+) +4V
V_{Supply} (-) -4V
Analog Input Overvoltage
V_{Supply} (+) +20V
V_{Supply} (-) -20V

Output Current: Short Circuit Protected
Operating Temperature Range
HA-5900-5: $0^oC \leq T_A \leq +75^oC$
HA-5900-2: $-55^oC \leq T_A \leq +125^oC$
Storage Temperature Range: $-65^oC \leq T_A \leq +150^oC$
Internal Power Dissipation: 650mW
T/H Control Input: +8, -15V

ELECTRICAL CHARACTERISTICS Unless otherwise specified: $V_S = \pm 15V$; $C_H = 1000pF$; $V_{IH} = 4.0V$; $V_{IL} = 0.8V$

		HI-5900-2 -55°C to +125°C			HI-5900-5 0°C to +70°C			
PARAMETER	TEMP	MIN	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
ANALOG INPUT CHAR., EACH CHANNEL								
Offset Voltage	+25°C		2	7		3	10	mV
	Full			9			12	mV
Bias Current	+25°C		80	300		80	300	nA
	Full		90	600		80	600	nA
Offset Current	+25°C		15	150		20	150	nA
	Full		30	300		30	300	nA
Common Mode Range	Full	±10			±10			V
Common Mode Rejection Ratio ($V_{CM} = \pm 10V$) Any Gain	Full	80	85		74	85		dB
DIGITAL INPUT CHAR.								
Multiplexer Digital Input Current (High or Low)	Full		0.5	1		0.5	1	µA
Track/Hold Digital Input Current								
$V_{IN} \leq 0.8V$	Full			0.8			0.8	mA
$V_{IN} \geq 4.0V$	Full			20			20	µA
TRANSFER CHARACTERISTICS								
Small Signal Bandwidth (Gain = 1)	+25°C		2			2		MHz
Full Power Bandwidth (Gain = 1, $V_O = \pm 10V$)	+25°C		70			70		kHz
Crosstalk (Sample Mode, Gain = 8, 1kHz 20VP-P Input on all but Selected Channel)	+25°C	-80	-90		-80	-90		dB
"Off Isolation (Hold Mode, Gain = 1, 1kHz 20V P-P Input)	+25°C		-76			-76		dB
Acquisition Time (Note 2), to 0.01%	+25°C		9			9		µs
Gain - Absolute Error								
Gain Of 1, 2,	Full		0.01	0.1		0.01	0.2	%
Gain Of 4, & 8	Full		0.01	0.2		0.01	0.2	%
OUTPUT CHARACTERISTICS								
Output Voltage Swing	Full	±10			±10			V
Output Current	+25°C	±10			±10			mA
Output Resistance	+25°C		5			5		Ω
DYNAMIC CHARACTERISTICS								
t_{ON}, Enable (MUX)	+25°C		300			300		ns
t_{OFF}, Enable (MUX)	+25°C		300			300		ns
Slew Rate	+25°C		±4			±4		V/µs
Droop Rate (T/H)	+25°C		5			5		nV/µs
	Full			20			5	µV/µs
Charge Transfer (T/H)	25°C		10			10		pC
Aperture Delay (T/H)	+25°C		50			50		ns
Aperture Uncertainty (T/H)	+25°C		5			5		ns
POWER SUPPLY CHARACTERISTICS								
I_+	+25°C			13			13	mA
	Full		8.5	15		8.0	15	mA
I_-	+25°C			13			13	mA
	Full		6.5	15		6.0	15	mA
Power Supply Rejection Ratio, V+	Full	76	90		70	90		dB
Power Supply Rejection Ratio, V-	Full	80	100		80	100		dB

NOTES:
1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Acquisition Time is defined for a change of channel (+10V on chan. 1 to 0V on chan. 8) with simultaneous change from HOLD to TRACK mode. Gain = 1.

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HI-5901

Analog Data Acquisition Signal Processor

FEATURES

- INPUT OVERVOLTAGE PROTECTION
- SOFTWARE CONTROLLED GAIN AND INPUT CHANNEL SELECTION
- 16 PSEUDO-DIFFERENTIAL/SINGLE ENDED INPUT CHANNELS
- GAINS OF-1,-2,-4 AND-8
- -90dB CROSSTALK
- 0.01% GAIN ERROR
- 9μs ACQUISITION TIME
- DROOP RATE: 5nV/μsec
- LOW POWER DISSIPATION 250mW
- COMPACT 32 PIN DIP
- MIL-STD-883 SCREENING AVAILABLE

APPLICATIONS

- MULTI-CHANNEL DATA ACQUISITION SYSTEMS
- STATUS MONITORING SYSTEMS
- PROCESS CONTROL SYSTEMS
- INSTRUMENTATION
- HIGH RELIABILITY DAS's

DESCRIPTION

The HI-5901 is a data acquisiton front end subsystem intended for multisensor based high-level applications, requiring conversion of analog input data to digital form for computer processing. It provides sixteen single-ended or pseudo-differential channels of fault-protected multiplexed inputs, programmable gains of-1,-2,-4,-8 and a buffered track and hold output block compatible with any commercially available A/D converter. All these functions are digitally selectable through appropriate coding of seven control terminals. Input channel expansion can be easily implemented through addition of external multiplexers and proper utilization of the enable-command pin.

Being self-contained units except for the holding capacitor, they facilitate user applications and eliminate the need for selection of high-priced precision resistors or labor intensive adjustments to achieve the accuracy levels specified.

This product provides channel to channel throughput rates of 50kHz at ±10 volt signal range when used in connection with a fast 12 bit A/D converter such as the HI-5712. In addition, it offers excellent input characteristics such as low input offset voltage with offset nulling capability, low input currents, very high input impedance, and very low crosstalk. Typical acquisition time and gain error are 9 microseconds and ±0.01%, respectively. The internal track and hold amplifier features aperture delay of 50ns, 10pC of charge transfer error, and a droop rate of 5nV/μsec. Total power dissipation is only 250mW.

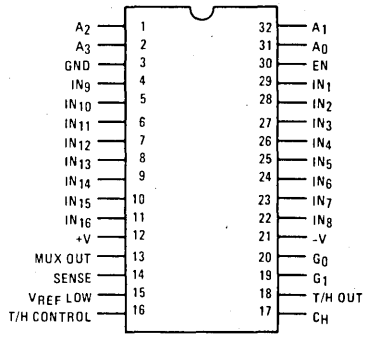
A complete high-speed and high precision data acquisition system with 15 bits of dynamic range can be easily implemented with only three components: the HI-5901, the HI-5712, and an offset nulling DAC. Board space required is 3 square inches and total weight is less than 25 grams.

The manufacturing technique adopted for the HI-5901 involves monolithic dice packaged in leadless chip carriers (LCC's) and soldered to both sides of a multilayer ceramic substrate. The resulting product is a compact and easy-to-use 32 pin DIP.

The HI-5901 is intended for military, aerospace, industrial and instrumentation applications. MIL-STD-883 Class B and high reliability commercial grades are both available as standard products.

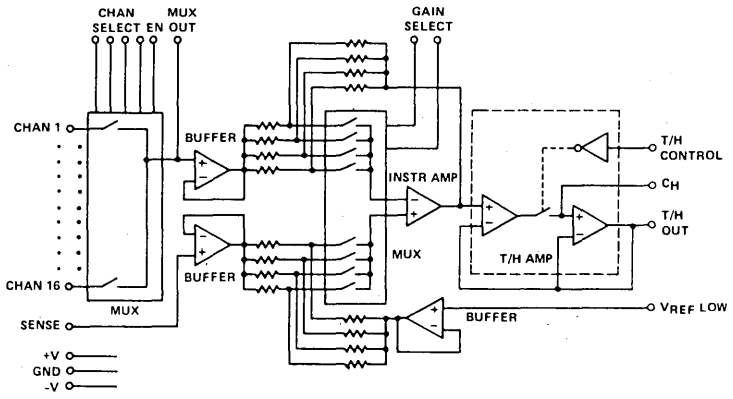
PINOUT

TOP VIEW



CAUTION: This device is sensitive to electrostatic discharge.

FUNCTIONAL DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V- Terminals 40V

Digital Input Overvoltage (Multiplexers)

V_{Supply} (+) +4V

V_{Supply} (-) -4V

Analog Input Overvoltage

V_{Supply} (+) +20V

V_{Supply} (-) -20V

Output Current: Short Circuit Protected

Operating Temperature Range

HA-5901-5, -7: $0^oC \leq T_A \leq +75^oC$

HA-5901-2, -8: $-55^oC \leq T_A \leq +125^oC$

Storage Temperature Range: $-65^oC \leq T_A \leq +150^oC$

Internal Power Dissipation: 650mW

T/H Control Input: +8, -15V

ELECTRICAL CHARACTERISTICS Unless otherwise specified: $V_S = \pm 15V$; $C_H = 1000pF$; $V_{IH} = 4.0V$; $V_{IL} = 0.8V$

		HI-5901-2, -8 -55°C to +125°C			HI-5901-5, -7 0°C to +70°C			
PARAMETER	TEMP	MIN	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
ANALOG INPUT CHAR., EACH CHANNEL								
Offset Voltage	+25°C		2	7.5		3	10.5	mV
	Full			9.5			13	mV
Bias Current	+25°C		80	300		80	300	nA
	Full		90	600		80	600	nA
Offset Current	+25°C		15	150		20	150	nA
	Full		30	300		30	300	nA
Common Mode Range	Full	±10			±10			V
Common Mode Rejection Ratio (V_{CM} = ±10V) Any Gain	Full	80	85		74	85		dB
DIGITAL INPUT CHAR.								
Multiplexer Digital Input Current (High or Low)	Full		0.5	1		0.5	1	µA
Track/Hold Digital Input Current								
$V_{IN} \leq 0.8V$	Full			0.8			0.8	mA
$V_{IN} \geq 4.0V$	Full			20			20	µA
TRANSFER CHARACTERISTICS								
Small Signal Bandwidth (Gain = 1)	+25°C		2			2		MHz
Full Power Bandwidth (Gain = 1, V_O = ±10V)	+25°C		70			70		kHz
Crosstalk (Sample Mode, Gain = 8, 1kHz 20VP -P Input on all but Selected Channel)	+25°C	-80	-90		-80	-90		dB
"Off Isolation (Hold Mode, Gain = 1, 1kHz 20V P-P Input)	+25°C		-76			-76		dB
Acquisition Time (Note 2), to 0.01%	+25°C		9			9		µs
Gain - Absolute Error								
Gain Of 1, 2, 4, & 8	Full		0.01	0.1		0.01	0.2	%
OUTPUT CHARACTERISTICS								
Output Voltage Swing	Full	±10			±10			V
Output Current	+25°C	±10			±10			mA
Output Resistance	+25°C		5			5		Ω
DYNAMIC CHARACTERISTICS								
t_{ON}, Enable (MUX)	+25°C		300			300		ns
t_{OFF}, Enable (MUX)	+25°C		300			300		ns
Slew Rate	+25°C		±4			±4		V/µs
Droop Rate (T/H)	+25°C		5			5		nV/µs
	Full			20			5	µV/µs
Charge Transfer (T/H)	25°C		10			10		pC
Aperture Delay (T/H)	+25°C		50			50		ns
Aperture Uncertainty (T/H)	+25°C		5			5		ns
POWER SUPPLY CHARACTERISTICS								
I_+	+25°C			13			13	mA
	Full		8.5	15		8.0	15	mA
I_-	+25°C			13			13	mA
	Full		6.5	15		6.0	15	mA
Power Supply Rejection Ratio, V+	Full	76	90		70	90		dB
Power Supply Rejection Ratio, V-	Full	80	100		80	100		dB

NOTES:
1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Acquisition Time is defined for a change of channel (+10V on chan. 1 to 0V on chan.16) with simultaneous change from HOLD to TRACK mode. Gain = 1.

HARRIS

HI-DAC 80I

12-Bit High Speed Monolithic Digital-to-Analog Converter

FEATURES

- DAC 80 CONFIGURATION
- MONOLITHIC CONSTRUCTION
- FAST SETTLING 260ns (TYP) TO 0.01%
- GUARANTEED MONOTONIC 0°C TO 75°C
- WAFER LASER TRIMMED
- APPLICATION RESISTORS ON CHIP
- ACCEPTS 6.2V OR 10.24V REFERENCE
- DIELECTRIC ISOLATION (DI) PROCESSING

APPLICATIONS

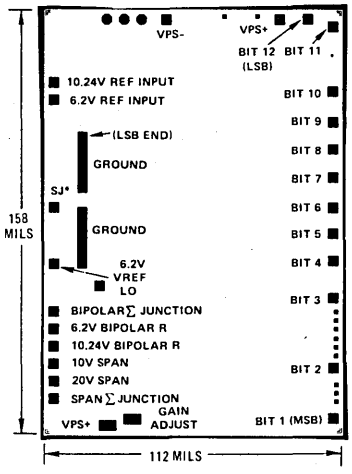
- HYBRID DAC 80 BY ADDING REFERENCE
- HIGH SPEED, SUCCESSIVE APPROXIMATION TYPE ADC'S
- HYBRID DATA ACQUISITION SYSTEMS

DESCRIPTION

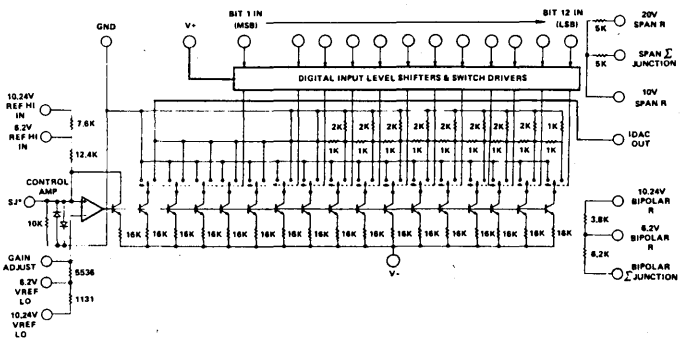
The Harris HI-DAC 80I is a 12-bit, monolithic digital to analog converter. Available in dice form, it is suitable as a component in hybrid or compound monolithic circuits. The HI-DAC 80I is a current output device, and the addition of a precision voltage reference makes it the functional equivalent of the popular DAC 80CBI-I. Two versions are available–DAC 80I-A, laser trimmed to accept a +6.2V reference; and DAC 80I-B, laser trimmed to accept a +10.24V reference. Both versions are guaranteed monotonic over the 0°C to 75°C temperature range. Digital input code may be complementary binary, complementary offset binary, or complementary two's complement binary logic.

Fast output current settling of 260ns is achieved using Dielectric Isolation (DI) processing to reduce internal parasitics. The speed of the HI-DAC 80I combined with its guaranteed monotonicity and maximum 1/2 LSB linearity error (@+25°C) make it an ideal choice for high speed successive approximation analog-to-digital converters. Laser trimmed application resistors are provided on-chip for use with an external output amplifier. They allow bipolar operation as well as +5V, +10V and +20V output ranges.

PAD CONFIGURATION/CHIP



FUNCTIONAL DIAGRAM



* A Summing Junction (normally an inverting input) is formed at the control amplifier's noninverting input, since the amplifier's feedback is inverted by an external transistor.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Referred to Ground) (Note 1).

Power Supply Inputs	V_{ps+}	+18V	Operating Temperature Range	-55°C to +125°C
	Vps-	-18V		
Reference Inputs	V_{REF} (Hi)	$+V_{ps}$	Storage Temperature Range	-65°C to +150°C
Digital Inputs	Bits 1-12	0V TO +10V		

ELECTRICAL CHARACTERISTICS (Note 5)

(@ +25°C, V_{ps+} = +15V, V_{ps-} = -15V, V_{REF} = 6.2V, Unless otherwise noted)

PARAMETER	CONDITION	HI-DAC 80I MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
Digital Inputs (TTL Compatible)					
Input Voltage	Bit ON = "Logic 0"				
Logic "1"	Bit OFF = "Logic 1"	2.0			V
Logic "0"				0.8	V
Input Current					
Logic "1"				10	μA
Logic "0"	Guaranteed, not tested			-100	μA
Reference Inputs (Note 2)					
Input Voltage					
HI-DAC 80I-A			6.2		V
HI-DAC 80I-B			10.24		V
Input Resistance					
HI-DAC 80I-A			12.4K		Ω
HI-DAC 80I-B			20K		Ω
TRANSFER CHARACTERISTICS					
Resolution				12	Bits
Linearity (Note 2)					
Integral				±½	LSB
Differential				±½	LSB
Monotonicity	0°C to +75°C GUARANTEED				
Offset (Note 5)	All bits OFF				
Unipolar			0.005	0.01	% FSR
Bipolar				0.1	% FSR
Gain Error	All bits OFF		0.05	0.1	% FSR
Temperature Stability					
Offset Drift (Note 2)	All bits OFF				
Unipolar			0.2		ppm
Bipolar			2		FSR/°C
Differential Nonlinearity (Note 2)			0.5		
Gain Drift (Note 2)	All bits ON		2		
Settling Time (Note 2), ± 1/2 LSB	All bits ON to OFF or OFF to ON		260	400	ns

SPECIFICATIONS (Continued)

PARAMETER	CONDITION	HI-DAC 80I			
		MIN	TYP	MAX	UNITS
Power Supply Sensitivity (Note 2)					
Offset					
Unipolar					
$+V_{ps}$	$-V_{ps}$ = -15V			0.05	% FSR/
$-V_{ps}$	$+V_{ps}$ = +15V			0.05	$\%\Delta V_{ps}$
Bipolar					
$+V_{ps}$	$-V_{ps}$ = -15V			0.05	
$-V_{ps}$	$+V_{ps}$ = +15V			0.05	
Gain					
$+V_{ps}$	$-V_{ps}$ = -15V			10	
$-V_{ps}$	$+V_{ps}$ = +15V			10	
OUTPUT CHARACTERISTICS					
Output Current					
Unipolar		1.6	2	2.4	mA
Bipolar		±0.8	± 1	± 1.2	mA
Output Resistance	Not including	1.6	2	2.4	KΩ
Output Capacitance	Feedback Resistor			10	pF
Compliance Limit (Note 2)		-3		+10	V
Glitch (Note 2)			1600		mV-ns
POWER SUPPLY REQUIREMENTS					
$V_{ps}+$		4.5	15	16.5	V
$V_{ps}-$		-16.5	-15	-11.4	V
$I_{ps}+$ (Note 4)			5		mA
$I_{ps}-$ (Note 4)			-10		mA

NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. See Definitions.
3. FSR is "full scale range" and is 2mA (±20%) for current output.
4. After 30 seconds warm-up.
5. Parameters may vary according to die bonding scheme used. See recommended bonding diagram.

DEFINITIONS OF SPECIFICATIONS

DIGITAL INPUTS

The HI-DAC 80I accepts digital input codes in complementary binary, complementary offset binary, and complementary two's complement binary.

DIGITAL INPUT	ANALOG OUTPUT		
	Complementary Binary	Complementary Offset Binary	Complementary Two's Complement*
MSB LSB			
000...000	+Full Scale	+Full Scale	-LSB
100...000	Mid Scale-1LSB	-1LSB	+Full Scale
111...111	Zero	-Full Scale	Zero
011...111	+½ Full Scale	Zero	-Full Scale

*Invert MSB with external inverter to obtain CTC Coding

ACCURACY

NONLINEARITY – Nonlinearity of a D/A converter is an important measure of its accuracy. It describes the deviation from an ideal straight line drawn between zero (all bits OFF) and full scale (all bits ON).

DIFFERENTIAL NONLINEARITY – For a D/A converter, it is the difference between the actual output voltage change and the ideal (1 LSB) voltage change for a one bit change in code. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity; i.e., the output always increases and never decreases for an increasing input.

DEFINITIONS OF SPECIFICATIONS (Continued)

SETTLING TIME

Settling time is the time required for the output to settle to within the specified error band for any input code transition. It is usually specified for a full scale or major carry transition.

DRIFT

GAIN DRIFT - The change in full scale analog output over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H -25°C) and low ranges (+25°C -T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT - The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Offset error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H-25°C) and low (+25°C -T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in -15V, or +15V supplies. It is specified under DC conditions and expressed as parts per million of fullscale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE

Compliance voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance limit implies functional operation only and makes no claims to accuracy.

GLITCH

A glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than turn OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably.

OPERATING INSTRUCTIONS

BONDING AND GROUNDING

In order to ensure proper operation of the HI-DAC 801, care must be taken to bond it correctly. Primary in these considerations is the selection of a grounding scheme. The best approach is to distinguish between a general power ground and a reference, or precision ground. Figure 1 shows the recommended connections in a system using an operational amplifier (such as the Harris HA-2600) to achieve voltage output. Notice that a ground plane extends along the chip, and all currents on the device flow through this plane. Any errors which arise along this plane are most significant at the MSB end. It is best then to choose this end as the reference point for the output. The opposite, or LSB end of the plane, is bonded to the general system or power ground. Varying currents through this point will give rise to voltages above those defined as reference; however, the only current flowing into precision ground is the constant current drawn by the reference plus the negligible bias current of the op-amp. Remember that the magnitude of the reference current changes when switching from unipolar to bipolar operation and requires readjustment of offset and gain. The finite resistance of the bond wires themselves introduce an error at both ends of the ground plane, and this effect is reduced by double bonding of the ground pads. For effective bypassing tie the bypass capacitors close to the pads of the chip.

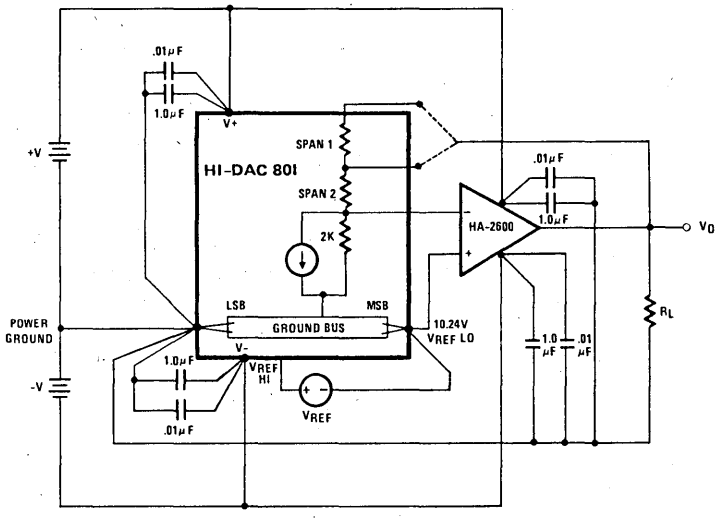
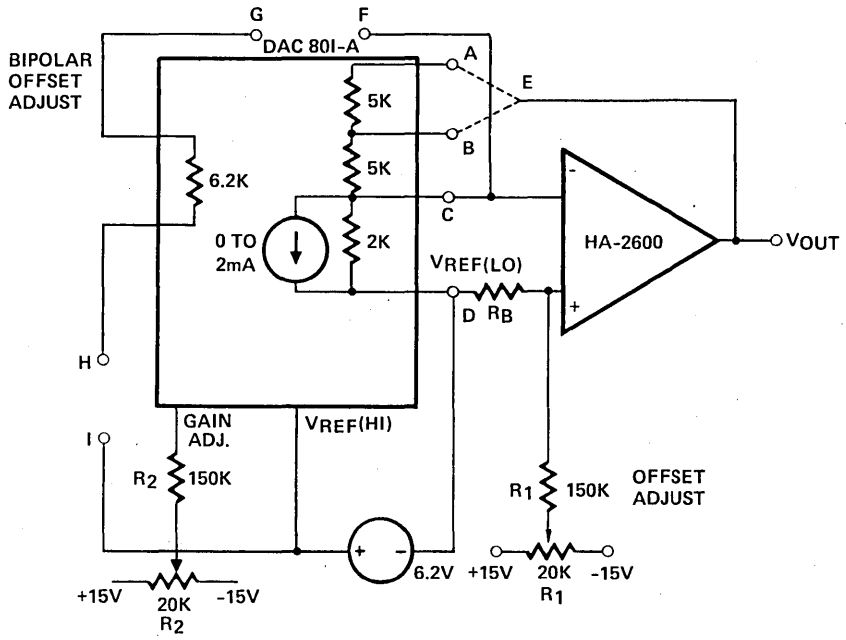


FIGURE 1. SYSTEM GROUNDING AND SUPPLY BYPASSING

OFFSET GAIN ADJUSTMENT

The offset and gain of the HI-DAC 80I may be externally adjusted via potentiometers. With the device mounted in a suitable package (see Packaging the HI-DAC 80I) connect the potentiometers as indicated in Figure 2.



	OUTPUT RANGE	CONNECTIONS	BIAS RESISTOR (R_B)
UNIPOLAR MODE	0 TO +10V 0 TO +5V	B TO E ; B TO E ; A TO C	1.43KΩ 1.11KΩ
BIPOLAR MODE	±10V ±5V 2.5V	F TO G ; H TO I ; A TO E F TO G ; H TO I ; B TO E F TO G ; H TO I ; B TO E A TO C	1.31K Ω 1.16KΩ .94KΩ

FIGURE 2. OFFSET GAIN ADJUSTMENT

UNIPOLAR CALIBRATION

Step 1: Unipolar Offset
- Turn all bits OFF
- Adjust R_1 for zero volts output

Step 2: Gain
- Turn all Bits ON
- Adjust R2 for an output of FS-1 LSB
- That is, adjust for:
- 9.9976V for 0V to +10V Range
- 4.9988V for 0V to +5V Range

BIPOLAR CALIBRATION

Step 1: Bipolar Offset
- Turn all bits OFF
- Adjust R1 for an output of:
- -10V for ±10V Range
- -5V for ±5V Range
- -2.5V for ±2.5V Range

Step 2: Gain
- Turn Bit 1 (MSB) ON; all other bits OFF
- Adjust R2 for zero volts output

HARRIS

HI-DAC16B/C

16-Bit D to A Converter

FEATURES

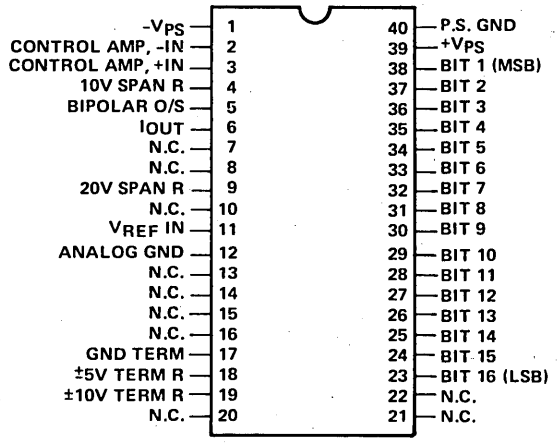
- 16 BIT RESOLUTION
- MONOLITHIC DI BIPOLAR CONSTRUCTION
- FAST SETTLING TIME — 1 μs TO .003%FS
- LOW DIFF. NONLIN. DRIFT — ± 0.3ppm/°C
- LOW GAIN DRIFT — ± 1ppm/°C
- ON-CHIP SPAN & OFFSET RESISTORS
- TTL/5V-CMOS COMPATIBLE
- LOW UNIPOLAR OFFSET — ≤ 1/2LSB@ +25°C
- LOW UNIPOLAR OFFSET T.C. — ± 0.2ppm/°C
- EXCELLENT STABILITY

APPLICATIONS

- HIGH RESOLUTION CONTROL SYSTEMS
- HIGH FIDELITY AUDIO RECONSTRUCTION
- PRECISION FUNCTION GENERATION AND INSTRUMENTATION

PINOUT

TOP VIEW



DESCRIPTION

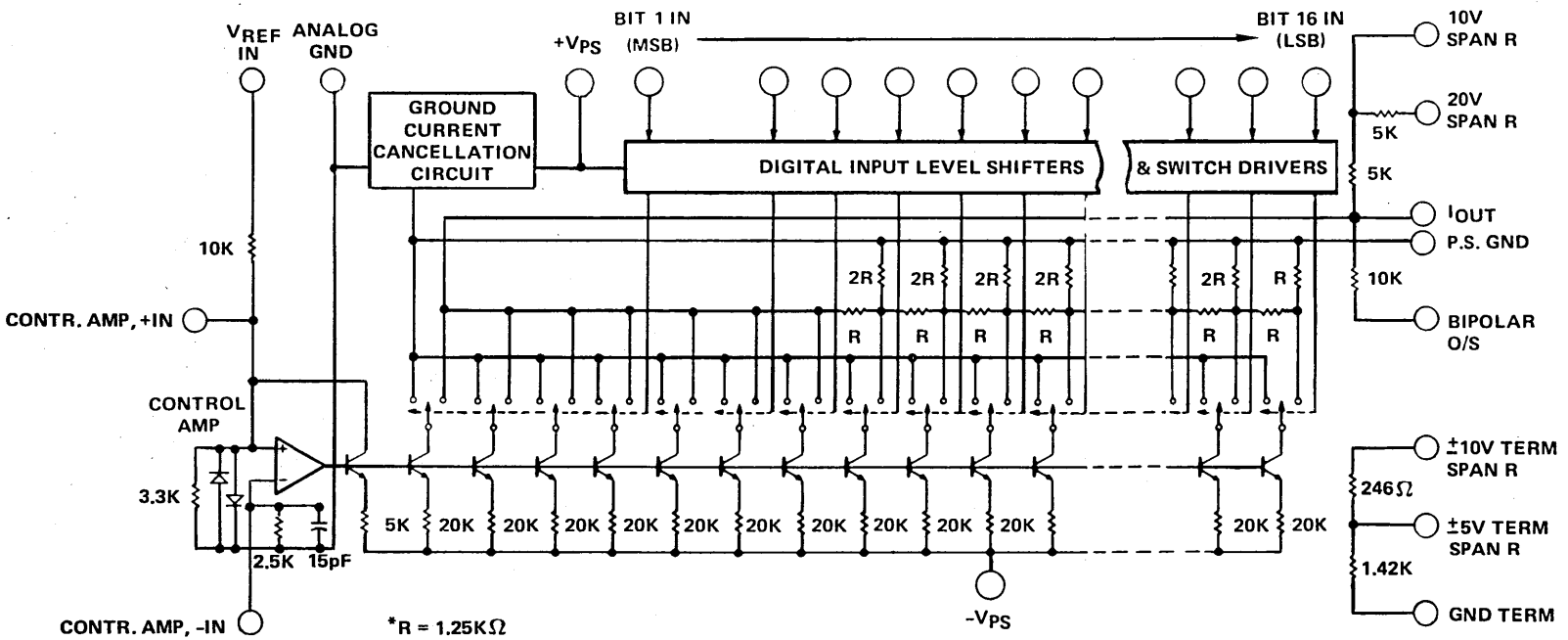
The HARRIS HI-DAC16 is a 16-bit, current output D/A converter. Single chip construction includes thin-film application resistors for use with an external op amp. These permit standard output voltage ranges of 0 to +5V, 0 to +10V, ±2.5V, ±5V and ±10V.

Reference and span resistors have adjacent placement on the chip for optimum match and thermal tracking. Futhermore, this layout feature helps minimize the superposition error caused by self-heating of the span resistor, reducing it to less than 1/10LSB. This and other design innovations have produced exceptionally stable operation over temperature. Typical temperature coefficients are ± 1ppm/°C for gain error and 0.3ppm/°C for differential non-linearity error.

The internal architecture is an extension of the earlier HI-562 with several major improvements. All code dependent ground currents are steered to a separate non-critical path, namely, power supply ground. This feature allows the precision ground of the converter to be sensed with virtually zero voltage drop referred to system ground. The result is the complete elimination of non-linearities due to code dependent ground currents while yielding an extremely low unipolar offset of less than 1/2LSB. Because of this separation, the user may route the precision ground some distance to the system ground without degrading converter accuracy.

The HARRIS HI-DAC16 delivers a stable, accurate output without sacrifice in speed. Settling time to within ±0.003% is one microsecond. Overall performance of this monolithic device should be attractive for applications such as high fidelity audio and high-resolution control systems.

Typical power requirement is 450 MW, from the +15V and -15V supplies combined. The package is a 40 pin ceramic DIP. Two accuracy grades are offered.



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Referred to Ground)

Power Supply Inputs	$V_{ps}+$	+20V	Power Dissipation Pd, Package	1000 mW
	$V_{ps}-$	−20V	Operating Temperature Range	
Reference Inputs	V_{REF} (Hi)	$\pm V_{ps}$		
Digital Inputs	Bits 1 to 16	−1V, +12V	HI-DAC 16B/C	0°C to +75°C
Outputs		$\pm V_{ps}$	Storage Temperature Range	−65°C to +150°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{ps} = ±15V, V_{ref} = +10V, unless otherwise specified)

PARAMETER	CONDITIONS	HI-DAC 16B MIN	HI-DAC 16B TYP	HI-DAC 16B MAX	HI-DAC 16C MIN	HI-DAC 16C TYP	HI-DAC 16C MAX	UNITS
INPUT CHARACTERISTICS								
Digital Inputs	Bit ON "Logic 1" Bit OFF "Logic 0"							
Input Voltage								
Logic "1"	Over full temp. range	2.0			2.0			V
Logic "0"				0.8			0.8	V
Input Current								
Logic "1"			20	500		20	500	nA
Logic "0"		−50			−50			μA
Reference Input								
Input Resistance			10			10		KΩ
Input Voltage			10			10		V
TRANSFER CHARACTERISTICS								
Resolution	Over full temp. range		16			16		Bits
Nonlinearity	@+25°C		±.0023			±.0045		%FSR(3)
	Over full temp. range			±.0045			±.009	
Differential Nonlinearity	@+25°C		±.0015			±.003		%FSR
	Over full temp. range			±.003			±.006	
Relative Accuracy (5)	With 100Ω (1%) Trim Resistors							
Gain Error	All Bits ON		±.1			±.1		%FSR
Bipolar Offset Error	All Bits OFF		±.5			±.5		
Unipolar Offset Error			±.002			±.002		
Adjustment Range	See Operating Instructions							
Gain	Using trim potentiometers as shown in Figure 1		.02			.02		%FSR
Bipolar Offset			2			2		
Temperature Stability	Drift specified with internal span resistors for voltage output							
Gain Drift (2)	Over full temp. range		±1	± 5		±1	± 5	ppm of FSR/°C
Offset Drift (2)								
Unipolar Offset	All Bits OFF		±.2			±.2		
Bipolar Offset			±.5			±.5		
Differential Nonlinearity	Over full temp. range		±0.3			±0.3		
Settling Time (2) to ±.003%FS	All Bits ON-to-OFF or OFF-to-ON		1.0			1.0		μs

PARAMETER	CONDITIONS	HI-DAC 16B			HI-DAC 16C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Glitch (2)	From 011 ... 1 to 100 ... 0 or 100 ... 0 to 011... 1 (R_O = 2.5KΩ)		0.52			0.52		mA-ns
Power Supply (2) Rejection Ratio, PSRR (3)								
V_{ps}+			1.5			1.5		ppm of FSR/% V_{ps}
V_{ps}−			1.5			1.5		
OUTPUT CHARACTERISTICS								
Output Current								
Unipolar			−2			−2		mA
Bipolar			±1			±1		
Resistance			2.5K			2.5K		ohms
Capacitance			10			10		pF
Output Voltage Ranges								
Unipolar	Using external op amp and internal scaling resistors. See Figure 1 and Table 1 for connections		0 to +5 0 to +10			0 to +5 0 to +10		V
Bipolar			±2.5 ±5 ±10			±2.5 ±5 ±10		
Compliance Limit (2)		−3		+10	−3		+10	V
Compliance Voltage (2)	Over full temp. range		±1			±1		V
Output Noise	0.1 to 5MHz (All Bits ON)		30			30		μVRMS
POWER REQUIREMENTS								
V_{ps}+ (7)	Over full temp. range	13.5	+15	16.5	13.5	+15	16.5	V
V_{ps}−		−13.5	−15	−16.5	−13.5	−15	−16.5	
I_{ps}+(4)	All Bits ON or OFF full temp. range		+13	+18		+13	+18	mA
I_{ps}−(4)		−25	−18		−25	−18		
Power Dissipation			465			465		mW

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impared. Functional operation under any of these conditions is not necessarily implied.
2. See Definitions.
3. FSR is "full scale range" and is 20V for ±10V range, 10V for ±5V range, etc., or 2mA (±20%) for current output.
4. After 30 seconds warm-up.
5. Using an external op amp with internal span resistors and specified external trim resistors in place of potentiometers R_1 and R_2. Errors are adjustable to zero using R_1 and R_2 potentiometers. (See Operating Instructions Figure 2.)

DEFINITIONS OF SPECIFICATIONS

DIGITAL INPUTS

The HI-DAC 16B/C accepts digital input codes in binary format and may be user connected for any one of three binary codes. Straight Binary, Two's Complement, or Offset Binary. (See Operation Instructions).

DIGITAL INPUT	ANALOG OUTPUT		
	Straight Binary	Offset Binary	Two's Complement *
MSB LSB			
000...000	Zero	-FS 9(Full Scale)	Zero
100...000	½FS	Zero	−FS
111...111	+FS − 1 LSB	+FS − 1 LSB	½FS − 1 LSB
011...111	½FS − 1 LSB	Zero − 1 LSB	+FS − 1 LSB
*Invert MSB with external inverter to obtain Two's Complement Coding			

ACCURACY

NONLINEARITY – Nonlinearity of a D/A converter is an important measure of its accuracy. It describes the deviation from an ideal straight line transfer curve drawn between zero (all bits OFF) and full scale (all bits ON).

DIFFERENTIAL NONLINEARITY – For a D/A converter, it is the difference between the actual output voltage change and the ideal (1 LSB) voltage change for a one bit change in code. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity; i.e., the output always increases and never decreases for an increasing input.

SETTLING TIME

Settling time is the time required for the output to settle to within the specified error band for any input code transition. It is usually specified for a full scale or major carry transition.

DRIFT

GAIN DRIFT – The change in full scale analog output over the specified temperature range expressed in parts per million of full scale per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H −25°C) and low ranges (+25°C−T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT – The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Offset error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H −25°C) and low (+25°C −T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in −15V, or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE

Compliance voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance limit implies functional operation only and makes no claims to accuracy.

GLITCH

A glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON−OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than turn OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably. (Calculated as the product of duration and amplitude.)

UNIPOLAR AND BIPOLAR VOLTAGE OUTPUT CONNECTIONS

FIGURE 1

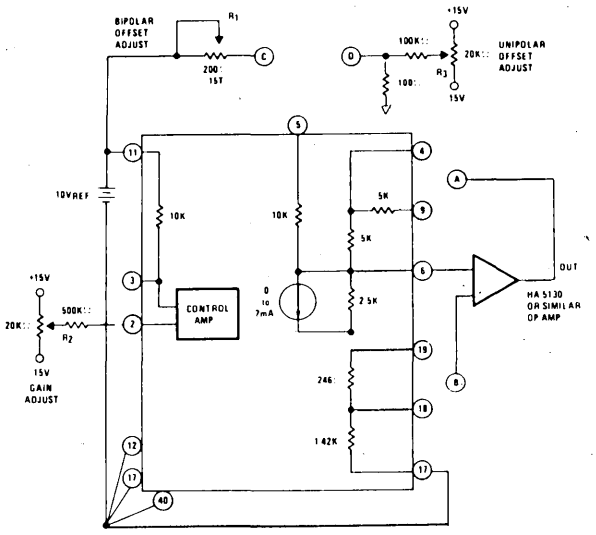


TABLE 1

	OUTPUT RANGE	CONNECTIONS PIN5 to	PIN4 to	PIN9 to	PIN B to
UNIPOLAR MODE	0 to +10V	D	A	N.C.	19
	0 to +5V	D	A	PIN6	*
BIPOLAR MODE	±10V	C	N.C.	A	19
	±5V	C	A	N.C.	18
	±2.5V	C	A	6	*

*Connect an external 1.1K ohm resistor to ground.

GAIN AND ZERO CALIBRATION

The HI-DAC16B/C input reference resistor, bipolar offset resistor and span resistors are optimized for excellent tracking over temperature. LASER trimming of the reference circuit resistors corrects the unipolar Gain and Offset errors to high accuracy. The remaining error can be adjusted with trimming potentiometers. The bipolar Gain and Offset errors are greater since the LASER correction is done in the unipolar mode, however these too are easily adjusted. Figure 1 illustrates the connections for unipolar and bipolar operation. Trimming potentiometers R_1, R_2, and R_3 are required for adjustment.

UNIPOLAR CALIBRATION

Step 1: Offset
- Turn all bits OFF (00..0)
- Adjust R_3 for zero volts output

Step 2: Gain
- Turn all bits ON (11..1)
- Adjust R_2 for an output of FS-1LSB
  That is, adjust for:

  9.999847 for +10V range
  4.999924 for +5V range

BIPOLAR CALIBRATION

Step 1: Offset
Turn all bits OFF (00..0)
Adjust R_1 for an output of
−10V for ± 10V range
−5V for ± 5V range
−2.5V for ± 2.5V range

Step 2: Gain
Turn all bits ON (11..1)
Adjust R_2 for FS-1LSB output
That is, adjust for:

9.999695 for ±10V range
4.999847 for ± 5V range
2.499924 for ± 2.5V range

OTHER CONSIDERATIONS

GROUNDS

The HI-DAC16 has two ground terminals, pin 12 (REF GND) and pin 40 (PWR GND). These should not be tied together near the package unless that point is also the system signal ground to which all returns are connected. (If such a point exists, then separate paths are required to pins 12 and 40).

The current through pin 12 is near-zero DC*, but pin 40 carries up to 1.75mA of code - dependent current from bits 1, 2, and 3. The general rule is to connect pin 12 directly to the system signal, or analog ground. Connect pin 40 to the local digital or power ground. Then, of course, a single path must connect the analog/signal and digital/power grounds.

OTHER CONSIDERATIONS (continued)

*Current cancellation is a two-step process in which code-dependent variations are eliminated, then the resulting DC current is supplied internally. First, an auxiliary 13-bit R-2R Ladder is driven by the complement of the DAC's input code. Together the main and auxiliary ladders draw a continuous 3.25mA from the internal ground node, regardless of input code. Part of this DC current is supplied by the zener voltage reference, and the remainder is sourced from the positive supply via a current mirror which is laser trimmed for zero current through the external terminal (pin 12).

LAYOUT

Connections to pin 6 (I_{OUT}) on the HI–DAC16 are most critical for high speed performance. Output capacitance of the DAC is only 10pF, so a small additional capacitance will alter the op amp's stability and affect settling time. Connections to pin 6 should be short and few. Component leads should be short on the side connecting to pin 6.

BYPASS CAPACITORS

Power supply bypass capacitors on the op amp will serve the HI–DAC16 also. If no op amp is used, a 0.01uF ceramic capacitor from each supply terminal to pin 40 is sufficient, since supply current variations are small.

SELECTING AN OPERATIONAL AMPLIFIER

The HI-DAC16 is a high resolution, high accuracy DAC. Many applications will require an OP-Amp used as a current-to-voltage converter at the DAC output. (Careful consideration should be given the choice of this amplifier as a poor selection can seriously degrade the inherent qualities of the DAC.)

The HA-5130 is an excellent choice to maintain high accuracy with an average Offset Drift of only 0.4μV/°C leading to an error over temperature of 30μV (.0003% FSR for a 10V FS). Inital offset and bias current are 10μV and 3nA respectively, while input noise current of 0.2pA/$\sqrt{Hz}$. Settling time is adequate for most audio applications. (11μs typ. to 0.1%).

COMPOSITE AMPLIFIER

It is desirable at times to have an output amplifier which combines the qualities of those op-amps available to the designer. For instance one may wish to combine the excellent front-end characteristics of the HA-5130 with the speed of a device such as the HA-2540 (t_{settle} =250ns to 0.1%). In these instances there is the option of the composite amplifier. The basic configuration is shown in Figure 2.

COMPOSITE AMPLIFIER

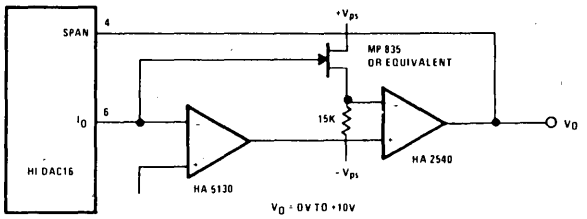


FIGURE 2

The composite amplifier may be used to achieve a compromise depending on the requirements of a design. Trade-offs in performance can be made and the following equations apply:

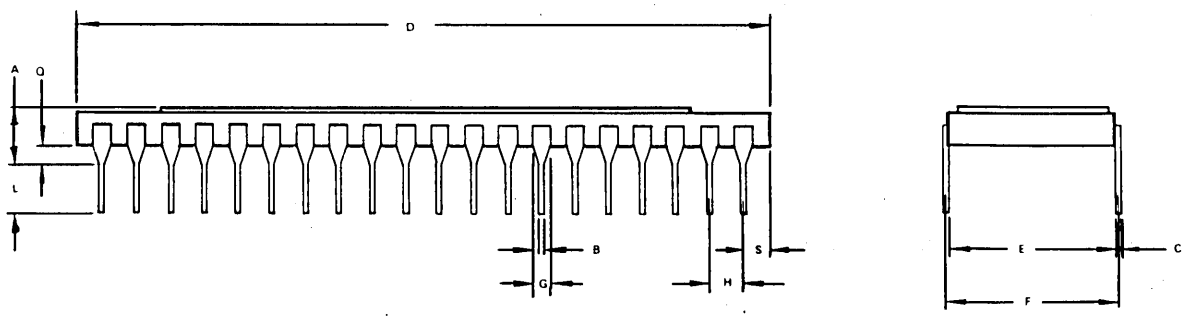
Offset; $$V_{OFF} = \frac{V_{OFF2}}{A_{01}} + V_{OFF1}$$

Bias; $$I_{BIAS} = I_{BIAS2} + I_{BIAS1}$$

Gain; $$\frac{V_0}{V_1} = A_V(S) = A_{V2}(S)\,[1 + A_{V1}(S)]$$

The amplifier A_2 should be of wide bandwidth and fast settling time.

PACKAGE DIMENSIONS



LEAD COUNT	DIM. A	DIM. B	DIM. C	DIM. D	DIM. E	DIM. F	DIM. G	DIM. H	DIM. L	DIM. Q	DIM. S
40	— / .225	.014 / .023	.008 / .015	— / 1.990	.500 / .610	.590 / .620	.030 / .070	.100 BSC	.120 / .200	.015 / .075	— / .098

NOTE: MIN. / MAX.

ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE	NONLINEARITY
HI-DAC16B-5	0°C to +75°C	±.003% FSR
HI-DAC16C-5	0°C to +75°C	±.006% FSR

HARRIS

HI-5660

ADVANCE

High Speed Monolithic Digital-to-Analog Converter

FEATURES

- VERY HIGH SPEED: SETTLES TO 1/2 LSB IN 350ns
  FULL SCALE SWITCHING TIME 30ns
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- 1/2 LSB MAX NONLINEARITY GUARANTEED OVER TEMPERATURE
- LOW GAIN DRIFT 10ppm/°C
- LOW POWER DISSIPATION 230mW
- LOW COST
- LOW PSR 1ppm/%PS

APPLICATIONS

- CRT DISPLAYS
- HIGH SPEED A/D CONVERTERS
- VIDEO SIGNAL RECONSTRUCTION
- WAVEFORM SYNTHESIS

DESCRIPTION

The HI-5660 12-bit digital-to-analog converter is a similar second source to the AD566, yet offers improved power dissipation performance.

Twelve high speed bipolar switches route the current from each bit cell either to ground or to the laser trimmed thin film R-2R ladder network, depending on the logic level of the bit input.

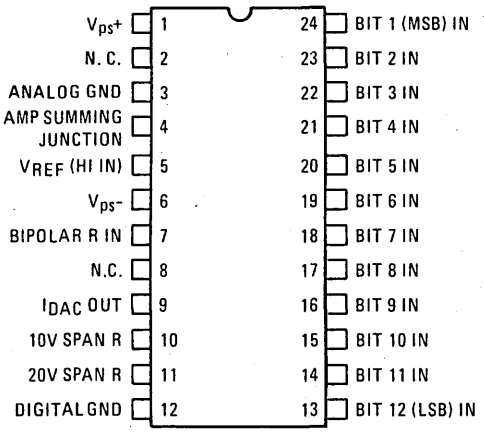
The Harris dielectric isolation process is used to fabricate the HI-5660, providing minimal stray capacitance and latch-free operation. The chips are trimmed at the wafer level to a maximum linearity error of 1/4 LSB at 25°C, making the HI-5660 an ideal choice when both high speed and high accuracy are essential.

For a +10V reference, Harris recommends using the HA-1610. This highly stable precision reference is laser trimmed to an absolute accuracy of ± 0.05% and a temperature coefficient of ± 3ppm/°C. For designs where an external reference is impractical, the HI-565A DAC is recommended.

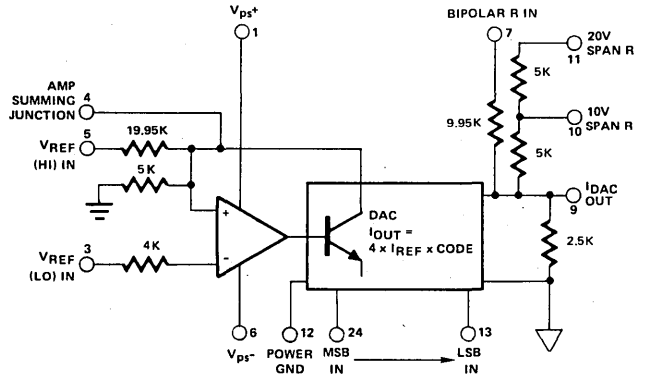
The HI-5660 is available in both commercial and military temperature grades, and is packaged in a ceramic 24 pin DIP. Power requirement is +5V, -15V.

PINOUT

TOP VIEW
24 LEAD DIP



FUNCTIONAL DIAGRAM



HARRIS

HI-7541

12-BIT MULTIPLYING MONOLITHIC DIGITAL TO ANALOG CONVERTER

FEATURES

- FULL FOUR QUADRANT MULTIPLICATION
- .01% RELATIVE ACCURACY OVER TEMPERATURE
- LOW OUTPUT CAPACITANCE 100pF MAX
- TTL/CMOS COMPATIBLE
- MONOLITHIC CONSTRUCTION
- VERY LOW OUTPUT LEAKAGE CURRENT ±100nA MAX
- LOW GAIN ERROR 0.1%

APPLICATIONS

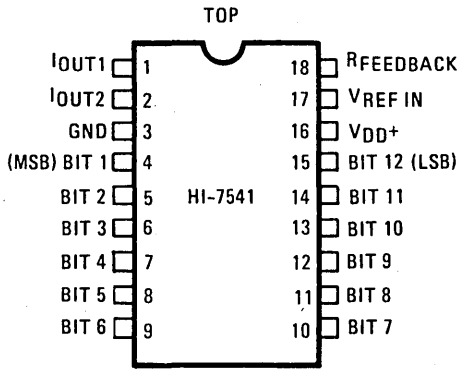
- PROGRAMMABLE GAIN AMPLIFIERS
- PROGRAMMABLE FUNCTION GENERATION

DESCRIPTION

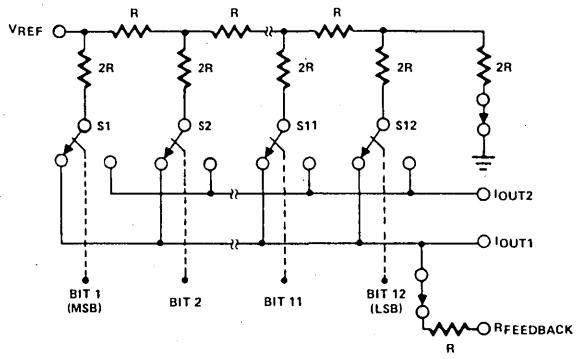
The Harris HI-7541 is a 12-Bit Monolithic Digital to Analog converter, offering full four quadrant multiplying capability. The chip features dielectrically isolated CMOS technology to assure fast settling time and freedom from latch-up. Included are thin film ladder and applications resistors, laser trimmed for accuracy over the full operating temperature range.

The HI-7541 is recommended as a high performance direct replacement for the AD7541 device. It operates on a single +15V supply and is available in an 18-pin ceramic package as well as in dice form. Screening to MIL-STD-883 method 5004 class B is available.

PINOUT



FUNCTIONAL DIAGRAM



DIGITAL INPUTS (DTL, TTL, CMOS COMPATIBLE)
LOGIC: A SWITCH IS CLOSED TO I_{OUT1} FOR ITS DIGITAL INPUT IN A HIGH (LOGIC 1) STATE.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Referred to Ground)1

Power Supply Inputs V_{DD}	+17V
Reference Inputs VREF (Hi)	±25V
Digital Input Range Bits 1-12	V_{DD} to GND
Output Voltage (Pins 1 and 2)	-100mV to V_{DD}

Power Dissipation (Package) up to +75°C Derate above +75°C by 6mW/°C.	450mW
Operating Temperature Range	
HI-7541SD/TD/SO	-55°C to +125°C
HI-7541AD/BD	-25°C to +85°C
HI-7541JN/KN/JO	0°C to +75°C
HI-7541SD/883 AND TD/883.	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS (@25°C, V_{DD} = +15V, V_{REF} = +10V Unless otherwise noted)

PARAMETER	CONDITIONS	HI-7541KN/BD/TD MIN	HI-7541KN/BD/TD TYP	HI-7541KN/BD/TD MAX	HI-7541JN/AD/SD/JO/SO MIN	HI-7541JN/AD/SD/JO/SO TYP	HI-7541JN/AD/SD/JO/SO MAX	UNITS
INPUT CHARACTERISTICS								
Digital Inputs	Bit ON = "Logic 1" Bit OFF = " Logic 0"							
Input Voltage								
Logic 1		2.4			2.4			V
Logic 0				0.8			0.8	V
Input Current								
Logic 1	V_{IN}=15V			1			1	µA
Logic 0	V_{IN}=0V			-1			-1	µA
Reference Input								
Input Resistance		5	9	20	5	9	20	KΩ
Input Voltage		-10		+10	-10		+10	V
TRANSFER CHARACTERISTICS								
Resolution	Over Full Temp. Range	12			12			Bits
Integral (2) Nonlinearity	@+25°C Over Full Temp Range			±.01			±.02	%FSR
Differential (2) Nonlinearity	@ +25°C Over Full Temp Range			±.01			±.02	%FSR
Gain Error (2)	@ +25°C Over Full Temp. Range			±.01 ±0.15			±0.2 ±0.25	%FSR
Gain Tempco (2)(5)	Over Full Temp. Range			±5			±5	PPM/°C
Settling Time (2) (5) to ±1/2 LSB				1			1	µs
PSRR (2)	14.5V≤V_{DD}≤15.5V;25°C Over Full Temp. Range		.01	±.01 ±.02		.01	±.01 ±.02	%FSR/ %ΔV_{DD}
OUTPUT CHARACTERISTICS								
Output (2) Leakage Current	V_{REF} = ±10V @ +25°C Over Full Temp. Range			±50 ±100			±50 ±100	nA nA
Capacitance (2) (5)				100			100	pF
Feed Through (2)(5)	V_{REF} = 20 V_{pp} @ 10kHz			±1			±1	mVpp
POWER REQUIREMENTS								
V_{DD}		+5	+15	+16	+5	+15	+16	V
I_{DD} (3)				2			2	mA

HARRIS

HD-0165

Keyboard Encoder

FEATURES

- STROBE OUTPUT
- KEY ROLLOVER OUTPUT
- EXPANDABLE: 2 PACKAGES REQUIRED FOR FULL TELETYPEWRITER, EIGHT-BIT ENCODING
- SINGLE +5.0V SUPPLY REQUIRED
- DTL/TTL OUTPUTS
- MONOLITHIC RELIABILITY

APPLICATIONS

- MICROPROCESSOR DATA ENTRY (16 KEY TO HEX CODE)
- BCD DATA ENTRY
- TYPEWRITER TYPE KEYBOARDS
- CONTROL PANELS

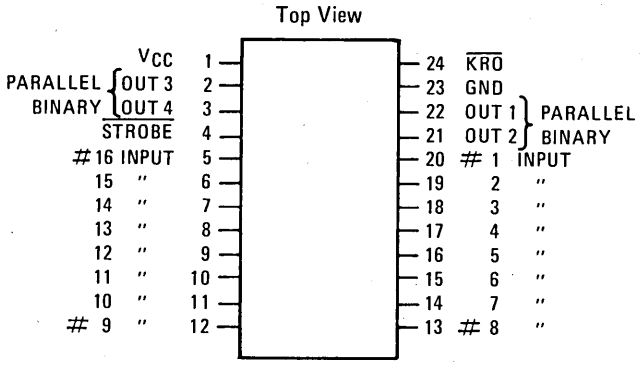
DESCRIPTION

The HD-0165 Keyboard Encoder is a 16 line to four-bit parallel encoder intended for use with manual data entry devices such as calculator or typewriter keyboards. In addition to the encoding function, there is a Strobe output and a Key Rollover output which energizes whenever two or more inputs are energized simultaneously. Any four-bit code can be implemented by proper wiring of the input lines. Inputs are normally wired through the key switches to the +5.0V power supply. Full typewriter keyboard encoding up to eight bits can be accomplished with two Encoder circuits by the use of double pole key switches or single pole switches with two isolation diodes per key. Outputs will interface with all popular DTL and TTL logic families. The circuit is packaged in a hermetic 24-pin dual-in-line package and operates over the temperature range of 0°C to +75°C.

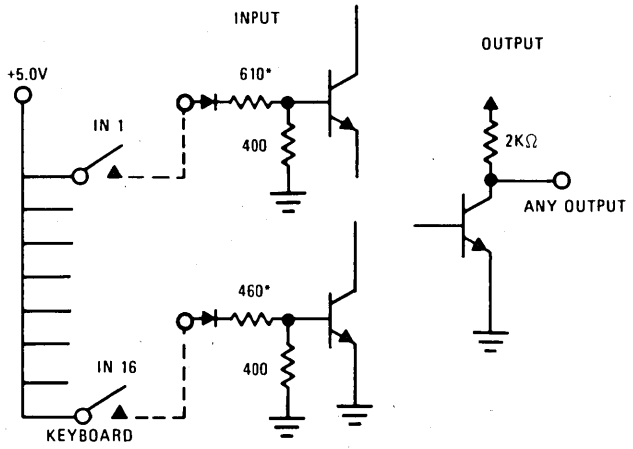
PINOUT

Section 11 for Packaging

Top View



EQUIVALENT CIRCUITS



* EQUIVALENT RESISTORS FOR OTHER INPUTS ARE BETWEEN THESE TWO VALUES

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7.0V	Output Current	30mA
Input Voltage	+5.5V	Storage Temperature	-65^{o} to $+150^{o}C$
Output Voltage	+5.5V	Operating Temperature (Case)	$0^{o}C$ to $+75^{o}C$

ELECTRICAL CHARACTERISTICS

Test Conditions: $V_{CC} = +5.0V \pm 5\%$
$T_{Case} = 0^{o}C$ to $+75^{o}C$
Unless otherwise specified

	PARAMETER	SYM.	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS
D.C.	Input Current "1"	I_{IH}			17	mA	$V_{IN} = +5.0V$
D.C.	Output Voltage "0"	V_{OL}		+0.2	+0.4	V	$V_{IH} = +4.5V$ $I_{OL} = 10mA$
D.C.	Output Voltage "0"	V_{OL}			+0.4	V	$V_{IH} = +3.5V$ $I_{OL} = 3.2mA$
D.C.	Output Voltage "1"	V_{OH}	+2.4	+4.0		V	V_{IL} = Open Circuit, $I_{OH} = -240\mu A$
D.C.	Power Supply Current Operating	I_{CC}			52	mA	One Input at +5.25V
D.C.	Power Supply Current Maximum	I_{CCM}			88	mA	All Inputs at +5.25V
A.C.	Skew Time (Note 1)	T_{SK}		80	200	ns	$T_{Case} = 25^{o}C$, $V_{CC} = V_{IN} = +5.0V$, $C_L < 50pF$

NOTE: (1) Skew time is the maximum time differential between propagation delay times of any outputs including strobe and $\overline{K_{RO}}$.

TRUTH TABLE

INPUTS 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	OUTPUTS 1	2	3	4	$\overline{St.}$	$\overline{K_{RO}}$
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H
H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L	H
L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	L	H
L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	H	H	L	H
L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	L	H
L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	L	H	L	H
L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	H	L	H	L	H
L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	H	L	L	H	L	H
L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	H	L	H
L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	H	H	H	L	L	H
L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	H	H	L	L	H
L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	H	L	H	L	L	H
L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	H	L	L	H
L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	H	H	L	L	L	H
L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	H	L	L	L	H
L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	H	L	L	L	L	H
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	H
ANY TWO OR MORE HIGH																X	X	X	X	L	L

INPUTS: L = Open Circuit or < +1.0V H = > +4.5V Current Source
OUTPUTS: L = < +0.4V H = > +2.4V X = Erroneous Data

HARRIS

HC-5502

SLIC-LC Subscriber Line Interface Circuit

Preliminary

FEATURES

- MONOLITHIC INTEGRATED DEVICE
- UNIQUE DI HIGH VOLTAGE PROCESS
- COMPATIBLE WITH WORLDWIDE PABX PERFORMANCE REQUIREMENTS
- CONTROLLED SUPPLY OF BATTERY FEED CURRENT FOR SHORT LOOPS
- INTERNAL RING RELAY DRIVER
- LOW POWER CONSUMPTION DURING STANDBY
- SWITCH HOOK, GROUND KEY AND RING TRIP DETECTION FUNCTIONS
- SELECTIVE DENIAL OF POWER TO SUBSCRIBER LOOPS

APPLICATIONS

- SOLID STATE LINE INTERFACE CIRCUIT FOR DIGITAL PBX SYSTEMS

DESCRIPTION

The HARRIS SLIC-LC incorporates many of the BORSHT functions on a single IC chip. This includes DC battery feed, a ring relay driver, supervisory and hybrid functions. Using the unique HARRIS dielectric isolation process, the SLIC-LC can operate directly with a wide range of station battery voltagees.

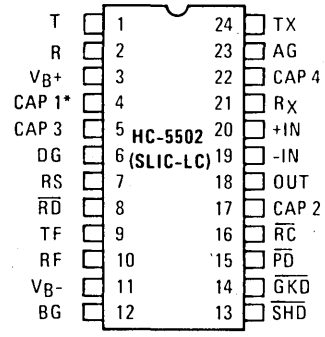
The SLIC-LC also provides selective denial of power. If the PABX system becomes overloaded during an emergency, the SLIC-LC will provide system protection by denying power to selected subscriber loops.

The HARRIS SLIC-LC is ideally suited in the design of new digital PABX systems, by eliminating bulky, expensive hybrid transformers.

SLIC-LC is available in either a 24 pin dual-in-line plastic or ceramic package.

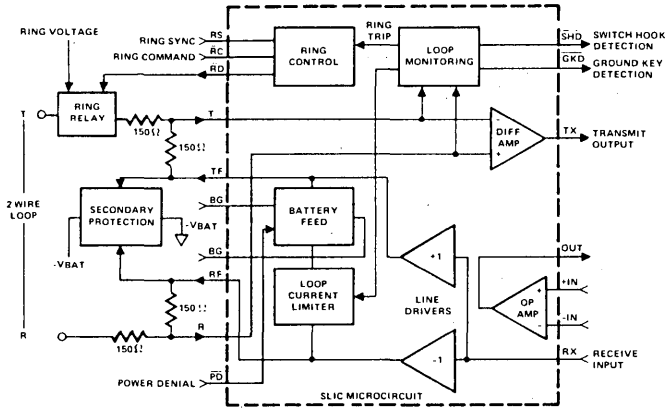
PINOUT

TOP VIEW



*Optional

FUNCTIONAL DIAGRAM



HARRIS

HC-5504

SLIC-LC Subscriber Line Interface Circuit

Preliminary

FEATURES

- MONOLITHIC INTEGRATED DEVICE
- UNIQUE DI HIGH VOLTAGE PROCESS
- COMPATIBLE WITH WORLDWIDE PABX PERFORMANCE REQUIREMENTS
- CONTROLLED SUPPLY OF BATTERY FEED CURRENT FOR SHORT LOOPS
- INTERNAL RING RELAY DRIVER
- ALLOWS INTERFACING WITH NEGATIVE SUPERIMPOSED RINGING SYSTEMS
- LOW POWER CONSUMPTION DURING STANDBY
- SWITCH HOOK, GROUND KEY AND RING TRIP DETECTION FUNCTIONS
- SELECTIVE DENIAL OF POWER TO SUBSCRIBER LOOPS

APPLICATIONS

- SOLID STATE LINE INTERFACE CIRCUIT FOR DIGITAL PBX SYSTEMS

DESCRIPTION

The HARRIS SLIC-LC incorporates many of the BORSHT functions on a single IC chip. This includes DC battery feed, a ring relay driver, supervisory and hybrid functions. Using the unique HARRIS dielectric isolation process, the SLIC-LC can operate directly with a wide range of station battery voltages.

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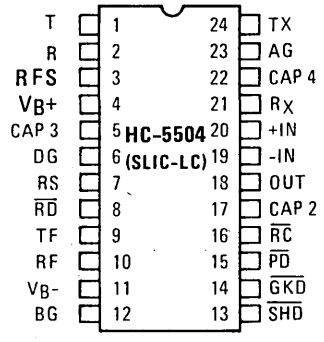
The HARRIS SLIC-LC is ideally suited in the design of new digital PABX systems, by eliminating bulky, expensive hybrid transformers.

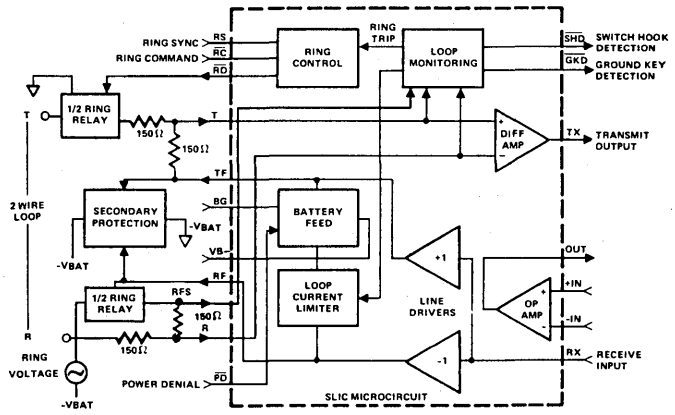
SLIC-LC is available in either a 24 pin dual-in-line plastic or ceramic package. The SLIC-LC is also available in die form.

PINOUT

TOP VIEW



FUNCTIONAL DIAGRAM



HARRIS

HC-5116A/5117A /5156A

ADVANCE

Monolithic CODECs

FEATURES

- LOW OPERATION POWER 50mW TYP.
- +5V OPERATION
- TTL COMPATIBLE DIGITAL INTERFACE
- INTERNAL PRECISION REFERENCE ON HC-5116A, HC-5117A and HC-5156A
- INTERNAL SAMPLE AND HOLD CAPACITORS
- INTERNAL AUTO-ZERO CIRCUIT
- HC-5116A–μ-LAW CODING (SIGN PLUS MAGNITUDE FORMAT)
- HC-5117A–μ-LAW, D3 COMPATIBLE FORMAT
- HC-5156A– A-LAW CODING
- SYNCHRONOUS OR ASYNCHRONOUS OPERATION

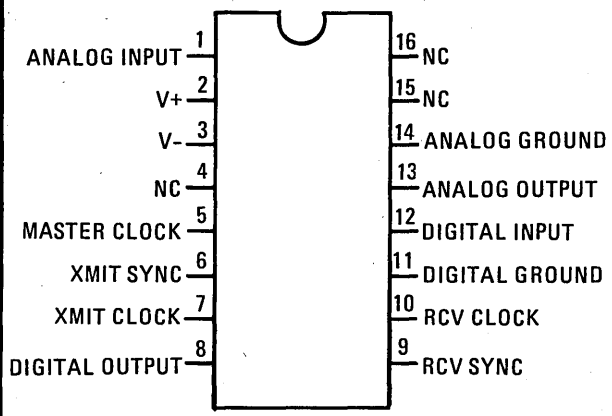
DESCRIPTION

The HC-5116A, HC-5117A and HC-5156A are monolithic PCM CODECs implemented with double-poly CMOS technology. The HC-5116A and HC-5117A are intended for μ-law applications. The HC-5117A has a D3 compatible format for line card compatibility with the HC-5156A.

Each device contains separate D/A and A/D circuitry, all necessary sample and hold capacitors, and internal auto-zero circuits. Each device also contains a precision internal voltage reference, eliminating the need for an external reference. There are no internal connections to pins 15 or 16, making them directly interchangeable with CODECs using external reference components.

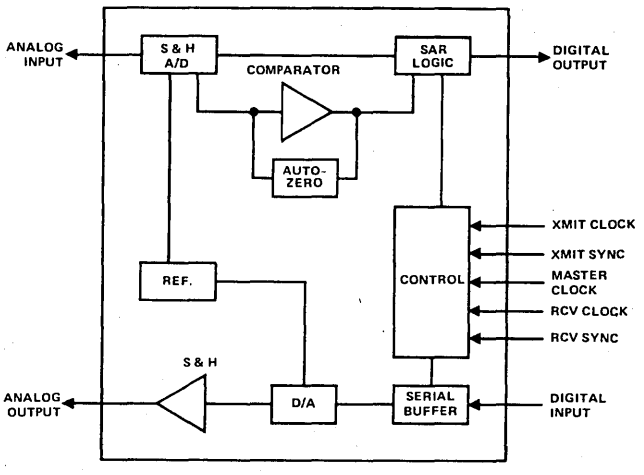
All devices are intended to be used with the HC-5512 monolithic PCM filter which provides the input anti-aliasing function for the encoder and smooths the output of the decoder and corrects for the sin x/x distortion introduced by the decoder sample and hold output.

PINOUT



TOP VIEW

FUNCTIONAL DIAGRAM



HARRIS

HC-5512/5512A

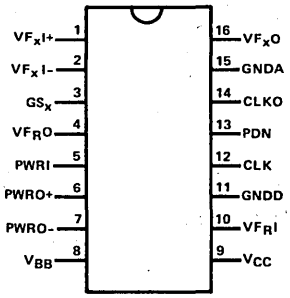
PCM Monolithic Filter

FEATURES

- EXCEEDS ALL D3/D4 AND CCITT SPECIFICATIONS
- +5V, -5V POWER SUPPLIES
- LOW POWER CONSUMPTION:
  45mW (600Ω 0dBm LOAD)
  30mW (POWER AMPS DISABLED)
- POWER DOWN MODE: 0.5mW
- 20dB GAIN ADJUST RANGE
- NO EXTERNAL ANTI-ALIASING COMPONENTS
- SIN x/x CORRECTION IN RECEIVE FILTER
- 50/60Hz REJECTION IN TRANSMIT FILTER
- TTL AND CMOS COMPATIBLE LOGIC
- ALL INPUT PROTECTED AGAINST STATIC DISCHARGE DUE TO HANDLING

PINOUT

DUAL-IN-LINE PACKAGE
TOP VIEW



DESCRIPTION

The HC-5512/HC-5512A filter is a monolithic circuit containing both transmit and receive filters specifically designed for PCM CODEC filtering applications in 8kHz sampled systems.

The filter is manufactured using double-poly silicon gate CMOS technology. Switched capacitor integrators are used to simulate classical LC ladder filters which exhibit low component sensitivity.

TRANSMIT FILTER STAGE

The transmit filter is a fifth order elliptic low pass filter in series with a fourth order Chebyshev high pass filter. It provides a flat response in the passband and rejection of signals below 200Hz and above 3.4kHz.

RECEIVE FILTER STAGE

The receive filter is a fifth order elliptic low pass filter designed to reconstruct the voice signal from the decoded/demultiplexed signal which, as a result of the sampling process, is a stair-step signal having the inherent sin x/x frequency response. The receive filter approximates the function required to compensate for the degraded frequency response and restore the flat passband response.

FUNCTIONAL DIAGRAM

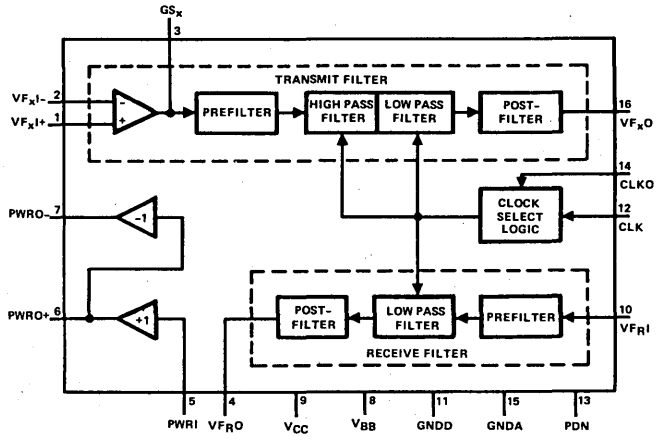


FIGURE 1

HARRIS

HC-55516

All-Digital Continuously Variable Slope Delta Modulator (CVSD)

FEATURES

- REQUIRES FEWER EXTERNAL PARTS
- LOW POWER DRAIN: 6mW FROM SINGLE 5V-7V SUPPLY
- TIME CONSTANTS DETERMINED BY CLOCK FREQUENCY; NO CALIBRATION OR DRIFT PROBLEMS; AUTOMATIC OFFSET ADJUSTMENT
- HALF DUPLEX OPERATION BY DIGITAL CONTROL
- FILTER RESET BY DIGITAL CONTROL
- AUTOMATIC OVERLOAD RECOVERY
- AUTOMATIC "QUIET" PATTERN GENERATION
- AGC CONTROL SIGNAL AVAILABLE

APPLICATIONS

- VOICE TRANSMISSION OVER DATA CHANNELS
- VOICE ENCRYPTION/SCRAMBLING
- VOICE I/O FOR DIGITAL SYSTEMS AND SPEECH SYNTHESIS
- AUDIO MANIPULATIONS: DELAY LINES, TIME COMPRESSION, ECHO GENERATION/ SUPPRESSION, SPECIAL EFFECTS, ETC.

The HC-55516 is a half duplex modulator/demodulator CMOS integrated circuit used to convert voice signals into serial NRZ digital data, and to reconvert that data into voice. The conversion is by delta modulation, using the continuously variable slope (CVSD) method of companding.

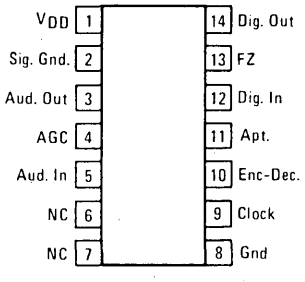
While signals are compatible with other CVSD circuits, internal design is unique. The analog loop filters have been replaced by digital filters, using very low power, and requiring no external timing components. This approach allows inclusion of many desirable features which would be difficult to implement using other approaches.

The HC-55516 has internal time constants optimized for a 16K bits/sec data rate and is usable from 9K bits/sec to above 64K bits/sec. The unit is available in 14 pin DIP (HC1) packages in two temperature ranges: -55°C to +125°C (-2 or -8), and -40°C to +85°C (-9). It is also available in chip form.

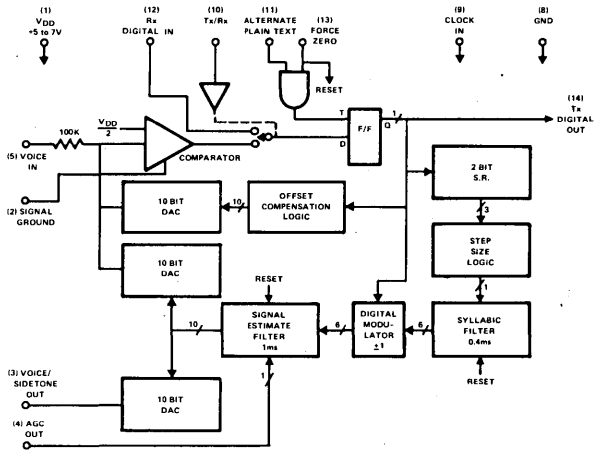
PINOUT

Section 11 for Packaging

Top View



FUNCTIONAL DIAGRAM



HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HC-5541

Pulse/Tone Dialer

Preliminary

FEATURES

- GENERATES EITHER DTMF TONES OR DIAL PULSES
- INTERFACES WITH STANDARD KEYPADS (FORM A CONTACT OR 2 OF 8) OR 4 BIT CMOS μP BUS.
- 17 DIGIT LAST NUMBER REDIAL
- 1mA PEAK OUTPUT DRIVE
- USES INEXPENSIVE 3.5795 MHz TV COLOR BURST CRYSTAL
- REGULATED TONE OUTPUT AMPLITUDES
- 2.5 TO 6V OPERATION
- TONE FREQUENCIES WITHIN 1%
- SINGLE TONE CAPABILITY
- MEETS INTERNATIONAL STANDARDS FOR TONE LEVELS AND DISTORTION
- AUTOMATIC RECEIVER MUTE OUTPUT DURING SIGNALING
- MUTE, PAUSE AND CANCEL SPECIAL FUNCTIONS

DESCRIPTION

The HC-5541 is a CMOS monolithic integrated circuit telephone dialer designed for applications where it is needed to produce either dial pulses or dial tones at will.

OUTPUTS

The HC-5541 outputs dial pulses or dial tones on separate pins. Sixteen standard DTMF frequency pairs are provided, accurate to ±1%. For pulse outputs, the make/break ratio can be selected with a single pin to conform to either US or European standards. A mute output is provided to mute the receiver while output signals are being generated.

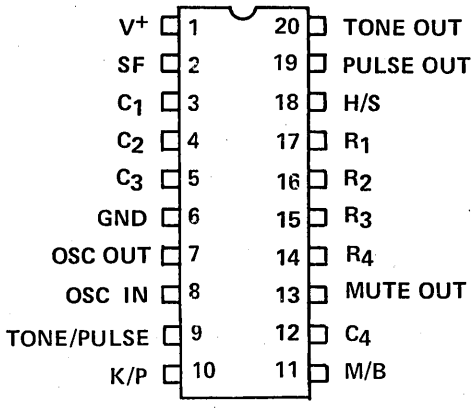
INPUTS

Data can be entered from a 4x4 keypad or a 4 bit microprocessor bus. In addition, the circuit can be driven from a standard 3x4 keypad plus one additional switch to select tones or pulses. Selection of keypad or microprocessor entry is controlled from a single pin.

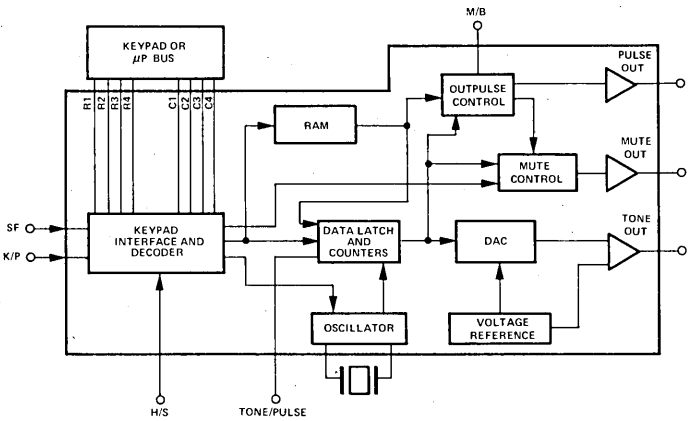
The pulse/tone dialer is available in either a 20 pin dual-in-line plastic or ceramic package.

PINOUT

TOP VIEW



FUNCTIONAL DIAGRAM



FUNCTIONAL DIAGRAM

HARRIS

SEMICONDUCTOR ANALOG PRODUCTS DIVISION

HV-1000/1005/1010

Induction Motor Energy Saver

Preliminary

FEATURES

- OPERATES DIRECTLY OFF 110/220V AC LINE – NO POWER SUPPLY REQUIRED
- PRODUCES POWER SAVINGS OFF FROM 10% TO 50% FOR MOTORS WITH LIGHT OR VARIABLE LOADS
- SCR OUTPUT STAGE TRIGGERS TRIAC DIRECTLY
- LOAD ANTICIPATOR SENSES SHOCK LOADS AND RESPONDS INSTANTLY WITH FULL POWER
- WITHSTANDS LINE SURGES TO 2000V
- CAUSES MOTOR TO RUN QUIETER, COOLER
- CAN BE MOUNTED INSIDE MOTOR
- NEEDS ONLY 3 RESISTORS, 2 CAPACITORS AND A TRIAC TO ASSEMBLE COMPLETE CONTROLLER

DESCRIPTION

The HV-1000/1005/1010 are energy saving induction motor controller circuits specifically designed for use with 110/220 volt AC single phase induction motors to reduce power consumption.

The controller circuit senses the load on the motor and then controls a TRIAC to apply reduced voltage to lightly loaded motors, full voltage to heavily loaded motors.

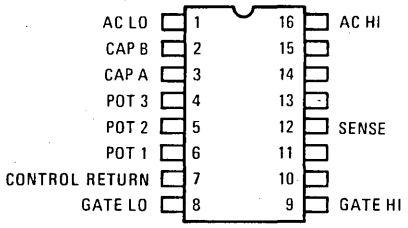
The HV-1000/1005/1010 is available in a 16 lead DIP. Ideal for mounting inside induction motors, it can also be mounted in a heat sunk circuit box for external, after market application.

APPLICATIONS

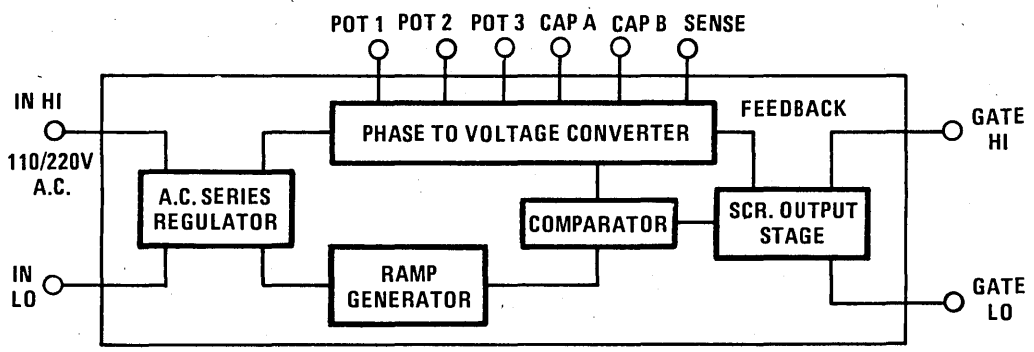
- POWER TOOLS
- WATER PUMPS
- HEAT PUMPS
- PRESSES
- CONVEYORS
- COMPRESSORS
  - ► ANY APPLICATION WHERE FOR SOME OF THE TIME THE MOTOR IS DRIVING LESS THAN ITS RATED LOAD

PINOUT

TOP VIEW



FUNCTIONAL DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Input Voltage (With Input Resistor)	±2000V
Input Voltage (Without Input Resistor)	±600V
Power Dissipation	500mW
Operating Temperature Range	-25°C to +85°C
Storage Temperature	-40°C to +100°C
Lead Temperature (Soldering, 10 seconds)	300°C
Output Current (10 microsecond pulse)	500mA

ELECTRICAL CHARACTERISTICS

These characteristics apply to the HV-1000/1005/1010 operating off 60Hz AC line power. HV-1000/1005/1010 respectively should be selected so that the full load power factor of the controller approximately matches that of the motor. The motor power factor $= \frac{\text{Watts}}{\text{Volt Amperes}}$ at full load, which should be measured experimentally.

FULL LOAD POWER FACTOR		
HV-1000	HV-1005	HV-1010
.86	.78	.68

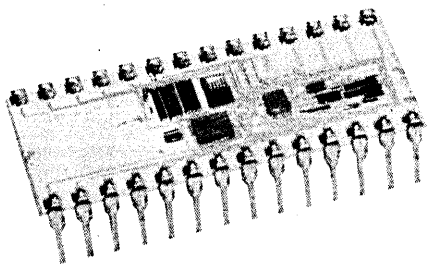
PARAMETER	MINIMUM	MAXIMUM	UNITS
Difference Between Positive and Negative Triggering Times, Measured from Line Voltage Zero Crossing		75	μsec
Output Stage Breakover Voltage	±600		V

NOTES:

1. Selection of HV-1000/1005/1010 by matching the full load power factor of the motor to that of the controller ensures that the controller will apply full voltage to the motor at its full rated load. At reduced loads, the controller will then apply appropriately reduced voltage to the motor so that its power consumption is reduced.

2. No guarantee of power savings can be given since the savings achievable depend entirely on the motor and its application. For a motor driving only a flywheel (e.g. a circular saw or a bench grinder) a power reduction of 50% may often be observed when the tool is switched on but not in use. For typical variable load applications, an overall power reduction of 10% is likely to be observed.

The Contender's Winning Combination



When you're The Contender, you have to have technological superiority and strength to go the distance. Most of all, you have to deliver.

We've rolled these key factors into a hard-hitting combination punch that scores technical knockouts over the competition every time.

FIRST WE NAIL'EM WITH THE RIGHT. We're the only converter manufacturer with a **patented** commercial package **guaranteed** to be leak-proof! We're on the leading edge of A/D and D/A technology. Our products feature innovative, state-of-the-art circuit design, and we've incorporated the most advanced manufacturing techniques available.

THEN WE PUT'EM AWAY WITH THE LEFT. No one else goes to the extremes we do to assure quality. We **full power burn-in** every product at +85° C. That's 15° C higher than the maximum specified operating temperature range. We have to, because every commercial data conversion product we build must meet an **Acceptable Quality Level (AQL) of 0.4%.** This commits us to guarantee that there will be no rejects in a sample of 100 pieces. That's more than twice as tough as it has to be—even for military applications.

Hybrid Systems not only makes the products shown here but hundreds of other data acquisition components . . . including custom hybrids. **Call for details.**

Industry Standard 574 $34.50(100's)

12-Bit, 25μSec Hybrid ADC

FEATURES

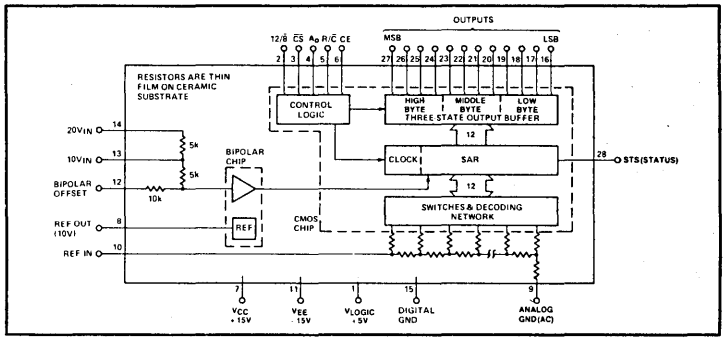
- Complete 12-Bit A/D Converter
- 25μSec Conversion Time
- Power 600mW
- No Missing Codes
- 150nSec Bus Access Time
- μP BUS Compatible
- Commercial and MIL-STD-883B Processing
- Hermetic, 28 pin DIP, Metal Package

SPECIFICATIONS

Resolution	12-Bits
Linearity Error	
Differential	No Missing Codes
Integral	±0.013% F.S.R.
End Point Error[1]	
Offset Bipolar	±0.25% F.S.R.
Unipolar	±0.05% F.S.R.
Full Scale	±0.3% F.S.R.
Conversion Time	25μSec
Temperature Stability	
Linearity	5ppm/°C F.S.R.
Offset	5ppm/°C F.S.R.
Full Scale	25ppm/°C F.S.R.
Power	±15V, +5V/600mW
Package	28 pin DIP

[1]Adjustable to zero

FUNCTIONAL DIAGRAM



ORDERING GUIDE

MODEL	RESOLUTION	LINEARITY ERROR MAX OVER TEMP	TEMP RANGE	PROCESSING	PRICE(100'S)
HS 574J	12 Bits	±1 LSB	0°C to +70°C	0.4% AQL*	$ 34.50
HS 574K	12 Bits	±½ LSB	0°C to +70°C	0.4% AQL*	$ 44.50
HS 574L	12 Bits	±½ LSB	0°C to +70°C	0.4% AQL*	$ 65.50
HS 574S	12 Bits	±1 LSB	−55°C to +125°C	0.4% AQL*	$ 95.00
HS 574T	12 Bits	±1 LSB[1]	−55°C to +125°C	0.4% AQL*	$130.00
HS 574U	12 Bits	±1 LSB[1]	−55°C to +125°C	0.4% AQL*	$190.00
HS 74S/B	12 Bits	±1 LSB[1]	−55°C to +125°C	MIL-STD-883B	$115.00
HS 574T/B	12 Bits	±1 LSB[1]	−55°C to +125°C	MIL-STD-883B	$160.00
HS 574U/B	12 Bits	±1 LSB[1]	−55°C to +125°C	MIL-STD-883B	$230.00

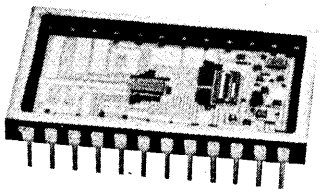
[1]Note: ±½ LSB max error from −25°C to −85°C

0.4% A.Q.L.* All units have full power burn-in at +85°C. Acceptable quality level (AQL) of 0.4% means that Hybrid Systems guarantees that there will be no rejects in a sample lot of 100 pieces. That's more than twice as tough as it has to be—even for military applications.

Hybrid Systems CORPORATION
22 Linnell Circle, Billerica, MA 01821
(617)667-8700, TWX 710-347-1575

12-Bit Adjustment Free ADC's

HS 5200 Series

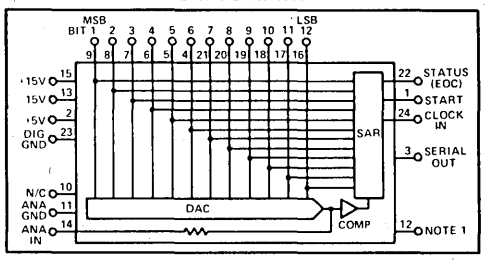


$160.00 (1-9)

FEATURES

- 12-Bit Conversion in 10μSec (Typical)
- Adjustment-Free (±0.0125%) Linearity
- Low Power 670mW (Typical)
- Hermetic, 24-pin DIP, Metal Package
- MIL-STD-883B Processing
- Pin Compatible to MN5200

FUNCTIONAL DIAGRAM



SPECIFICATIONS

Resolution	12 Bits
Linearity	±½ LSB
Absolute Accuracy[1]	±0.4%
Conversion Time	13μSec
Temperature Range	
C-versions	0°C to +70°C
B-versions	−55°C to +125°C
Power	+15V, +5V/870mW
Package	24-pin DIP, Metal

[1] Includes all errors, gain, zero, and linearity over temperature.

0.4% A.Q.L.* **All units have full power burn-in at +85°C. Acceptable quality level (AQL) of 0.4% means that Hybrid Systems guarantees that there will be no rejects in a sample lot of 100 pieces. That's more than twice as tough as it has to be-even for military applications.**

ORDERING GUIDE

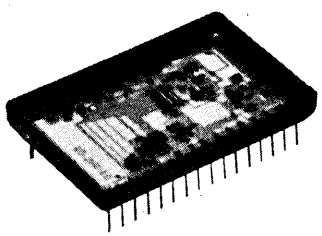
MODEL	RESOLUTION / CONVERSION TIME	INPUT RANGE	TEMP RANGE	PROCESSING	PRICE (1-9)
HS 5210C-12	12 Bits, 13μSec	0 to −10V	0°C to +70°C	0.4% AQL*	$160.00
HS 5211C-12	12 Bits, 13μSec	± 5V	0°C to +70°C	0.4% AQL*	$160.00
HS 5212C-12	12 Bits, 13μSec	±10V	0°C to +70°C	0.4% AQL*	$160.00
HS 5213C-12	12 Bits, 13μSec	0 to −10V	0°C to +70°C	0.4% AQL*	$160.00[1]
HS 5214C-12	12 Bits, 13μSec	± 5V	0°C to +70°C	0.4% AQL*	$160.00[1]
HS 5215C-12	12 Bits, 13μSec	±10V	0°C to +70°C	0.4% AQL*	$160.00[1]
HS 5216C-12	12 Bits, 13μSec	0 to +10V	0°C to +70°C	0.4% AQL*	$160.00
HS 5210B-12	12 Bits, 13μSec	0 to −10V	−55°C to +125°C	MIL-STD-883B	$190.00
HS 5211B-12	12 Bits, 13μSec	± 5V	−55°C to +125°C	MIL-STD-883B	$190.00
HS 5212B-12	12 Bits, 13μSec	±10V	−55°C to +125°C	MIL-STD-883B	$190.00
HS 5213B-12	12 Bits, 13μSec	0 to −10V	−55°C to +125°C	MIL-STD-883B	$190.00[1]
HS 5214B-12	12 Bits, 13μSec	± 5V	−55°C to +125°C	MIL-STD-883B	$190.00[1]
HS 5215B-12	12 Bits, 13μSec	±10V	−55°C to +125°C	MIL-STD-883B	$190.00[1]
HS 5216B-12	12 Bits, 13μSec	0 to +10V	−55°C to +125°C	MIL-STD-883B	$190.00

[1] 10V external reference user supplied

Technical knockouts from the Contenders!

12-Bit 10μSec Hi Rel ADC

ADC85 Series

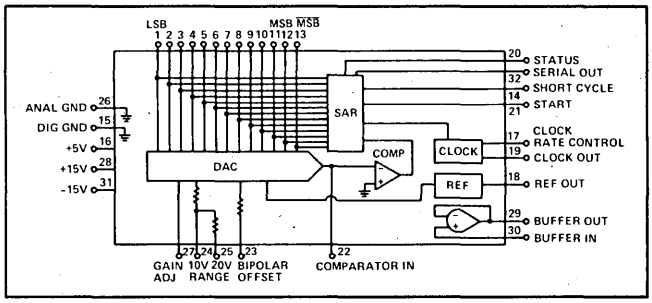


$134.00 (1-9)

FEATURES

- −55°C to+125°C Operation
- No Missing Codes
- Replaces ADC84/85, HX12B, HZ12B
- Low Power 1.2W (maximum)

FUNCTIONAL DIAGRAM



SPECIFICATIONS

Resolution	12 Bits
Analog Inputs	
Unipolar	0 to +5V, 0 to +10V
Bipolar	±2.5V, ±5V, ±10V
Outputs	Parallel, Serial/TTL
Coding	CBIN/COBIN
Linearity	±0.012% F.S.R. (maximum)
Conversion Time	8.8μSec, 10μSec (maximum)
Scale Factor Drift	15ppm/°C (maximum)
Linearity Drift	2ppm/°C (maximum)
Temperature Range	−55°C to +125°C
Power	±15V, +5V/1.2W (maximum)
Package	32-pin DIP

ORDERING GUIDE

MODEL	RESOLUTION	ACCURACY	TEMP RANGE	PROCESSING	PRICE
HS ADC85B	12 Bits	12 Bits	−55°C to +125°C	MIL-STD-883B	$205.00
HS ADC85C	12 Bits	12 Bits	0°C to +70°C	0.4% AQL*	$134.00

Hybrid Systems CORPORATION
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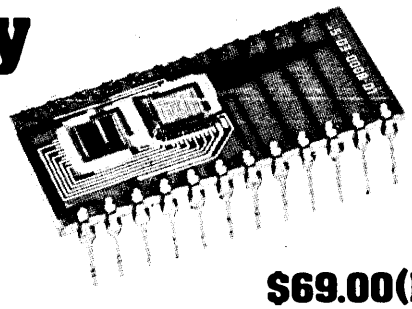
(617)667-8700, TWX 710-347-1575

14, 15 and 16 Bit Linearity Latched MDAC's

DAC9331-16 Series



$69.00(1-9)

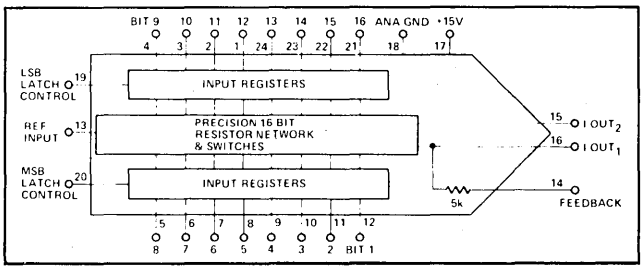
FEATURES

- Up to 16-Bit (0.0008%) Linearity
- Two-Chip Construction
- Input Registers
- 24-pin DIP, Metal Package
- 2 and 4-Quadrant Multiplication
- Single Supply Operation
- Low Power 60mW

SPECIFICATIONS

Resolution	16 Bits
Coding	BIN, OBIN
Logic	CMOS, TTL
Reference Input	0 to ±25V
Output	200μA/V_{REF}
Linearity	
DAC9331-16-4	±0.003% F.S.R.
DAC9331-16-5	±0.0015% F.S.R.
DAC9331-16-6	±0.0008% F.S.R.
Settling Time	2μSec
Scale Factor Drift	2ppm/°C
Temperature Range	0°C to +70°C
Power	+15V/60mW
Package	24-pin DIP

FUNCTIONAL DIAGRAM



ORDERING GUIDE

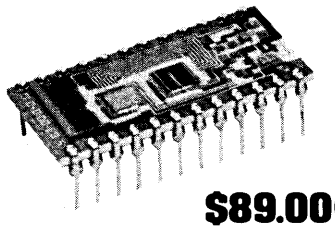
MODEL	RESOLUTION	LINEARITY	TEMP RANGE	PROCESSING	PRICE (1-9)
DAC9331-16-4	16 Bits	14 Bits	0°C to +70°C	0.4% AQL*	$ 69.00
DAC9331-16-5	16 Bits	15 Bits	0°C to +70°C	0.4% AQL*	$109.00
DAC9331-16-6	16 Bits	16 Bits	0°C to +70°C	0.4% AQL*	$169.00*

*$99.00 (100's)

Technical knockouts from the Contenders!

Complete Buffered 16 and 18 Bit DAC's

DAC9377, 377 Series



$89.00(1-9)

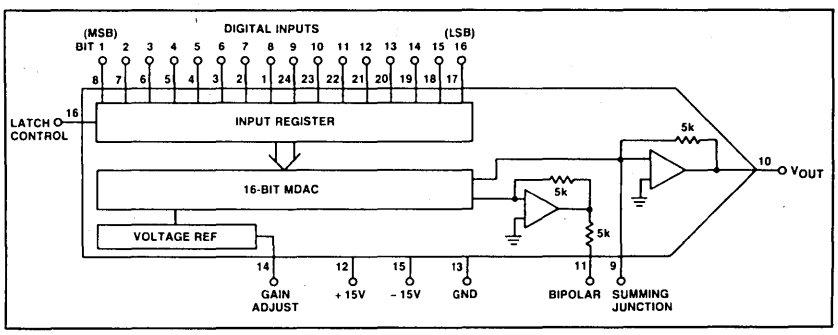
FEATURES

- True 16-Bit (0.0008%) Linearity
- μP Compatible
- Complete DAC
- 24-pin DIP, Metal Package
- Low Power 450mW

SPECIFICATIONS

Resolution	16 Bits, 18 Bits
Coding	BIN, OBIN
Logic	CMOS, TTL
Output	0 to +10V, ±10V
Linearity	
DAC377-18	±0.0008% F.S.R.
DAC9337-16-6	±0.0008% F.S.R.
DAC9337-16-5	±0.0015% F.S.R.
DAC9337-16-4	±0.003% F.S.R.
DAC9377-4D	±0.002% F.S.R.
Settling Time	20μSec
Scale Factor Drift	5ppm/°C
Temperature Range	0°C to +70°C
Power	+15V/450mW
Package	24-pin DIP (9377) 28-pin DIP, Metal (377)

FUNCTIONAL DIAGRAM



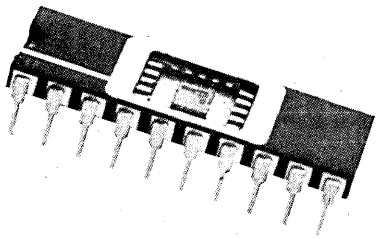
ORDERING GUIDE

MODEL	RESOLUTION	LINEARITY	TEMP RANGE	PROCESSING	PRICE (1-9)
DAC9377-4D	4 BCD	±0.002%	0°C to +70°C	0.4% AQL*	$ 99.00
DAC9377-16-4	16 Bits	14 Bits	0°C to +70°C	0.4% AQL*	$ 89.00
DAC9377-16-5	16 Bits	16 Bits	0°C to +70°C	0.4% AQL*	$129.00
DAC9377-16-6	16 Bits	16 Bits	0°C to +70°C	0.4% AQL*	$199.00
DAC377B-18	18 Bits	16 Bits	-55°C to +125°C	MIL-STD-883B	$395.00
DAC377C-18	18 Bits	16 Bits	0°C to +70°C	0.4% AQL*	$205.00

Hybrid Systems CORPORATION
22 Linnell Circle, Billerica, MA 01821
(617)667-8700, TWX 710-347-1575

Monolithic 14-Bit MDAC

HS 3140 Series



$29.00 (100's)

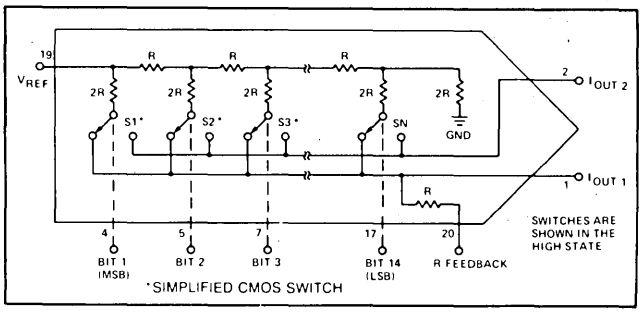
FEATURES

- Monolithic CMOS Circuit
- On-Chip Resistors
- Linearity ±0.003%
- Monotonic Over Temperature
- Latch-Up Protected
- 20-pin DIP, Metal Package
- Pin Compatible to DAC-HA 14B
- Commercial and MIL-STD-883B Processing

SPECIFICATIONS

Resolution	14 Bits
Coding	BIN, OBIN
Logic	CMOS, TTL
Reference Input	0 to ±25V
Output	200μA/V_{REF}
Linearity	
HS 3140-4	±0.003%
HS 3140-3	±0.006%
Settling Time	1.5μSec
Scale Factor Drift	2ppm/°C
Temperature Range	
C-versions	0°C to +70°C
B-versions	−55°C to +125°C
Power	+15V/@1mA
Package	20-pin DIP

FUNCTIONAL DIAGRAM



ORDERING GUIDE

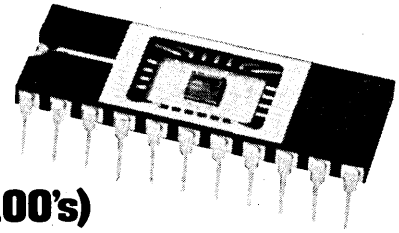
MODEL	RESOLUTION	LINEARITY	TEMP RANGE	PROCESSING	PRICE (1-9)
HS 3140C-3	14 Bits	13 Bits	0°C to +70°C	0.4% AQL*	$ 35.00¹
HS 3140C-4	14 Bits	14 Bits	0°C to +70°C	0.4% AQL*	$ 39.00
HS 3140B-3	14 Bits	13 Bits	−55°C to +125°C	MIL-STD-883B	$ 80.00
HS 3140B-4	14 Bits	14 Bits	−55°C to +125°C	MIL-STD-883B	$108.00

¹$29.00 (100's)

Technical knockouts from the Contenders!

Monolithic 16-Bit MDAC

HS 3160



$39.00 (100's)

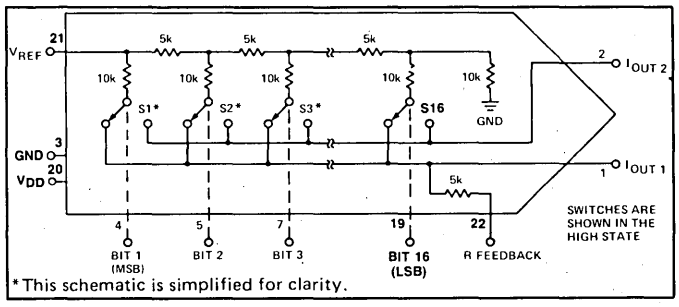
FEATURES

- Monolithic CMOS Circuit
- On-Chip Resistors
- Linearity ±0.003% (14-Bits)
- Monotonic Over Temperature
- Latch-Up Protected
- Small Size, 22 pin DIP
- Commercial and MIL-STD-883B Processing

SPECIFICATIONS

Resolution	16-Bits
Coding	BIN, OBIN
Logic	CMOS, TTL
Reference Input	0 to ±25V
Output	200μA/V REF
Integral Linearity (Accuracy)	
HS 3160-4	±0.006% F.S.R. Max
HS 3160-3	±0.012% F.S.R. Max
Differential Linearity	
HS 3160-4	±0.006% F.S.R. Max
HS 3160-3	±0.012% F.S.R. Max
Settling Time	1.5μSec
Scale Factor Drift	2ppm/°C
Temperature Range	
C-versions	0°C to +70°C
B-versions	−55°C to +125°C
Power	+15V@1mA
Package	22 pin DIP Ceramic

FUNCTIONAL DIAGRAM



ORDERING GUIDE

MODEL	RESOLUTION	LINEARITY	TEMP RANGE	PROCESSING	PRICE (1-9)
HS 3160C-3	16 Bits	13 Bits	0°C to +70°C	0.4% AQL*	$ 45.00¹
HS 3160C-4	16 Bits	14 Bits¹	0°C to +70°C	0.4% AQL*	$ 49.00
HS 3160B-3	16 Bits	13 Bits	−55°C to +125°C	MIL-STD-883B	$ 90.00
HS 3160B-4	16 Bits	14 Bits¹	−55°C to +125°C	MIL-STD-883B	$119.00

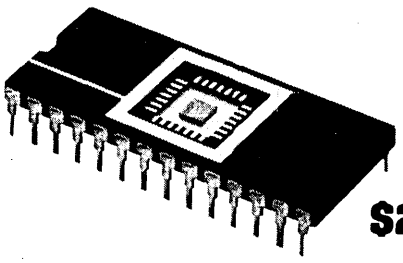
¹Integral Linearity (Accuracy): 0.006% F.S.R. Max
Differential Linearity: 0.006% F.S.R. Max

¹$39.00 (100's)

Hybrid Systems CORPORATION
22 Linnell Circle, Billerica, MA 01821
(617)667-8700, TWX 710-347-1575

Double Buffered 12-Bit MDAC

HS 3120 Series



$29.00(1-9)

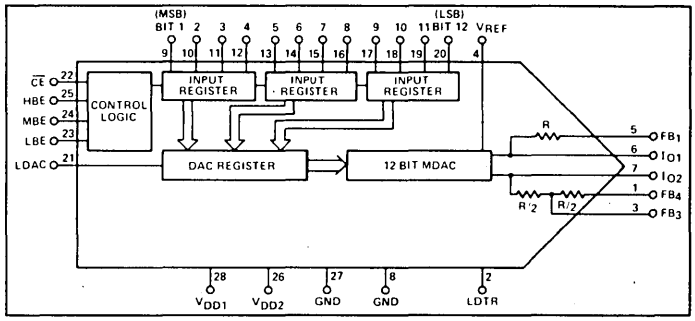
FEATURES

- Monolithic Construction
- 12-Bit Resolution
- Linearity 0.01%
- µP Compatible
- 4-Quadrant Multiplication
- Latch-Up Protected

SPECIFICATIONS

Resolution	12 Bits
Coding	BIN, OBIN
Logic	CMOS, TTL
Reference Input	0 to ±25V
Output	200µA/V_{REF}
Linearity	
HS 3120-0	±0.05%
HS 3120-2	±0.01%
Settling Time	1µSec
Scale Factor Drift	2ppm/°C
Temperature Range	
C-versions	0°C to +70°C
B-versions	−55°C to +125°C
Power	+15V/@2.5mA
Package	28-pin DIP

FUNCTIONAL DIAGRAM

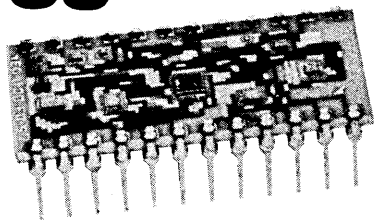


ORDERING GUIDE

MODEL	RESOLUTION	LINEARITY	TEMP RANGE	PROCESSING	PRICE (1-9)
HS 3120C-0	12 Bits	10 Bits	0°C to +70°C	0.4% AQL*	$29.00
HS 3120C-2	12 Bits	12 Bits	0°C to +70°C	0.4% AQL*	$36.00
HS 3120E-0	12 Bits	10 Bits	−25°C to +85°C	0.4% AQL*	$33.00
HS 3120E-2	12 Bits	12 Bits	−25°C to +85°C	0.4% AQL*	$42.00
HS 3120B-0	12 Bits	10 Bits	−55°C to +125°C	MIL-STD-883B	$72.00
HS 3120B-2	12 Bits	12 Bits	−55°C to +125°C	MIL-STD-883B	$82.00

Technical knockouts from the Contenders!

Industry Standard DAC 80



$15.95 ANY QTY.

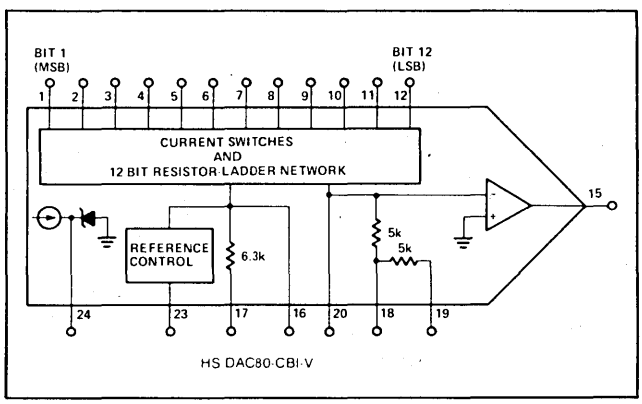
FEATURES

- 12-Bit Resolution
- Fast Output Settling
- ±½ LSB Linearity
- Voltage or Current Output
- TTL and CMOS Compatible
- Wide Operating Supply Range

SPECIFICATIONS

Resolution	12 Bits
Coding	CBIN, COBIN
Logic	CMOS, TTL
Output	
Current	±1mA, 0 to −2mA
Voltage	±2.5V, ±5V, ±10V, 0 to +5V
Total Error	
Unipolar	±0.08% F.S.R.
Bipolar	±0.06% F.S.R.
Settling Time	300nSec (−I)
	3µSec (−V)
Power	±15V/750mW
Temperature Range	0°C to +70°C
Package	24-pin DIP

FUNCTIONAL DIAGRAM



HS DAC80-CBI-V

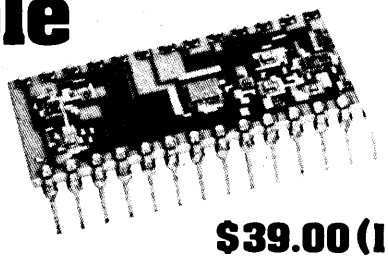
ORDERING GUIDE

MODEL	DESCRIPTION	PROCESSING	PRICE (1 up)
HS DAC80-CBI-I	Current Output	0.4% AQL*	$15.95
HS DAC80-CBI-V	Voltage Output	0.4% AQL*	$16.95

Hybrid Systems CORPORATION
22 Linnell Circle, Billerica, MA 01821
(617)667-8700, TWX 710-347-1575

Complete μP Compatible 12 Bit DAC

DAC338, HS 9338 Series



$39.00 (1-9)

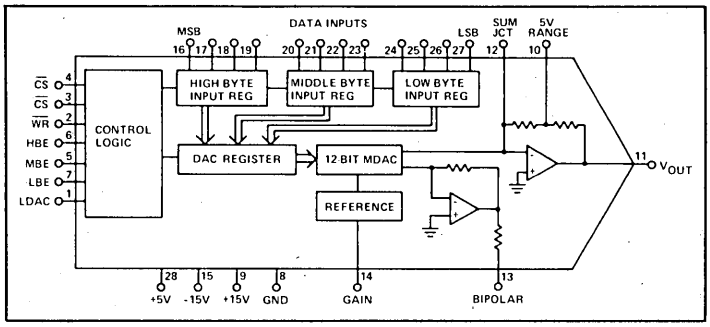
FEATURES

- μP BUS Compatible
- 0 to +10V, 0 to +5V, ±10V, ±5V Output Ranges
- Binary Coding
- Linearity ±0.01%
- 2.5μSec Settling Time

SPECIFICATIONS

Resolution	12 Bits
Coding	BIN, OBIN
Logic	CMOS, TTL
Output	0 to +10V, ±10V, ±5V
Linearity	
−0	±0.05% F.S.R.
−1	±0.02% F.S.R.
−2	±0.01% F.S.R.
Settling Time	20μSec
Scale Factor Drift	15ppm/°C
Temperature Range	0°C to +70°C
Power	+15V/450mW
Package	28-pin DIP

FUNCTIONAL DIAGRAM



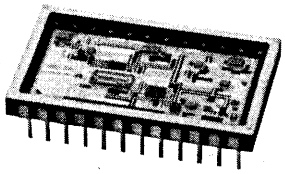
ORDERING GUIDE

MODEL	RESOLUTION	LINEARITY	TEMP RANGE	PROCESSING	PRICE (1-9)
DAC338B-12-0	12 Bits	10 Bits	−55°C to +125°C	MIL-STD-883B	$118.00
DAC338B-12-1	12 Bits	11 Bits	−55°C to +125°C	MIL-STD-883B	$126.00
DAC338B-12-2	12 Bits	12 Bits	−55°C to +125°C	MIL-STD-883B	$137.00
HS 9338-0	12 Bits	10 Bits	0°C to +70°C	0.4% AQL*	$ 39.00
HS 9338-1	12 Bits	11 Bits	0°C to +70°C	0.4% AQL*	$ 44.00
HS 9338-2	12 Bits	12 Bits	0°C to +70°C	0.4% AQL*	$ 49.00

Technical knockouts from the Contenders!

Complete Buffered 12-Bit DAC's

HS 3860 Series



$140.00 (1-9)

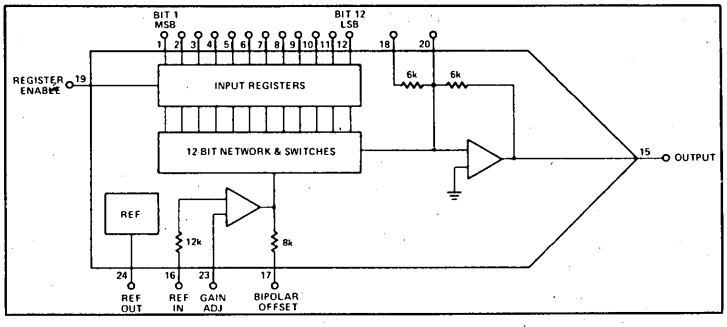
FEATURES

- ±½ LSB Linearity (maximum)
- ±0.3% Absolute Accuracy Over Temperature
- 3μSec Settling Time
- MIL-STD-883B Processing
- Superior Replacement for MN3860

SPECIFICATIONS

Resolution	12 Bits
Coding	CBIN, COBIN
Logic	CMOS, TTL
Output	0 to +10V, ±5V, ±10V
Linearity Error	
0°C to +70°C	±¼ LSB (typical)
	±½ LSB (maximum)
−55°C to +125°C	±½ LSB (maximum)
Monotonicity	Guaranteed Over Temp.
Full Scale Absolute Error	
+25°C	±0.05% F.S.R. (typical)
	±0.1% F.S.R. (maximum)
−55°C to +125°C	±0.15% F.S.R. (typical)
(B-version)	±0.3% F.S.R. (maximum)
Zero Error	
+25°C	±0.025% F.S.R. (typical)
	±0.05% F.S.R. (maximum)
−55°C to 125°C	±0.05% F.S.R. (typical)
(B-version)	±0.1% F.S.R. (maximum)
Gain Error	±0.1%
Gain Drift	±10ppm/°C
Settling Time	3μSec
Temperature Range	
C-version	0°C to +70°C
B-version	−55°C to +125°C
Power	±15V, +5V/1000mW
Package	24-pin DIP, Ceramic

FUNCTIONAL DIAGRAM



ORDERING GUIDE

MODEL	RESOLUTION	LINEARITY	TEMP RANGE	PROCESSING	PRICE (1-9)
HS 3860B	12 Bits	12 Bits	−55°C to +125°C	MIL-STD-883B	$225.00
HS 3860C	12 Bits	12 Bits	0°C to +70°C	0.4% AQL*	$140.00

Hybrid Systems CORPORATION
22 Linnell Circle, Billerica, MA 01821
(617)667-8700, TWX 710-347-1575

DAC's, ADC's, Mux's & Switches

Note: See other MPS parts in Linear and Military Sections.

Analog Multiplexers

- ☐ Second source to Analog Devices, Harris and Siliconix
- ☐ Low leakage; dielectric isolation
- ☐ 25 volt over-voltage protection
- ☐ Low ON resistance

Model	Type	R_{ON} (max, full temp) ohm	Access Time [1] nsec	Off Output Leakage (max, full temp)	Replaces
MP7501	8 Channel	375	800	250 nA	AD7501
MP7502	4 Channel Diff.	375	800	125 nA	AD7502
MP7503	8 Channel (Inv. Enable)	375	800	250 nA	AD7503
MP7506	16 Channel	500	800	500 nA	AD7506 DG506
MP7507	8 Channel Diff.	500	800	250 nA	AD7507 DG507
MP7508DI	8 Channel	350	500	500 nA	HI508A DG508
MP7509DI	4 Channel Diff.	350	500	500 nA	HI509A DG509

[1](typ, 25°C)

Analog-to-Digital Converters

- ☐ Second source to Analog Devices
- ☐ Bright display digital panel meter
- ☐ Microprocessor compatible

Model	Type CMOS	Resolution	Accuracy	Replaces
MP7138	3½ Digit Panel Meter	100 μV	±.05%	—
MP7550	Quadslope, 2's Complement	13 Bit	±1 L.S.B.	AD7550
MP7570	Successive Approximation	10 Bit	±.05%	AD7570
MP7574	Successive Approximation	8 Bit	±.75 L.S.B.	AD7574
MP7581	8 Channel, 8 Bit	8 Bit	± .5 L.S.B.	AD7581

Dielectrically isolated multiplexers and switches are indicated by "DI" suffix.

Digital-to Analog Converters

- ☐ Second source to Analog Devices and PMI
- ☐ Improved temperature drift characteristics
- ☐ Superior stability—no laser trimming
- ☐ .5 ppm gain tempco for MP7621

Model	Type	Resolution	Accuracy	Replaces
MP370	CMOS, High Resolution	18 Bit	±.0008%	DAC-370-18
MP377-18	CMOS, Buffered	18 Bit	±.0008%	DAC-377-18
MP562	Bipolar, Low Power	12 Bit	±.006%	AD562
MP3140	CMOS, Multiplying	14 Bit	±.006%	HS3140
MP5520	CMOS and Bipolar	6 Bit	±.2%	DAC01
MP5560	Bipolar, Low Noise	10 Bit	±.05%	DAC100
MP7520	CMOS, Multiplying	10 Bit	±.05%	AD7520
MP7521	CMOS, Multiplying	12 Bit	±.05%	AD7521
MP7522	CMOS, μP Compatible	10 Bit	±.05%	AD7522
MP7523	CMOS, Multiplying	8 Bit	±.05%	AD7523
MP7524	CMOS, μP Compatible	8 Bit	±.05%	AD7524
MP7530	CMOS, Multiplying	10 Bit	±.05%	AD7530
MP7531	CMOS, Multiplying	12 Bit	±.05%	AD7531
MP7533	CMOS, Multiplying	10 Bit	±.05%	AD7533
MP7541	CMOS, Multiplying	12 Bit	±.012%	AD7541
MP7614	CMOS, Multiplying	14 Bit	±.012%	AD7546
MP7616	CMOS, Multiplying	16 Bit	±.006%	AD7546
MP7621	CMOS, Untrimmed	12 Bit	±.012%	AD7541
MP7622	CMOS, Multiplying	12 Bit	±.012%	HS3120
MP7623	CMOS, Multiplying	12 Bit	±.012%	AD7541
MP9331	CMOS, High Resolution	16 Bit	±.0008%	DAC-9331-16
MP9377-16	CMOS, Buffered	16 Bit	±.0008%	DAC-9377-16

Analog Switches

- ☐ Second source to Analog Devices, Harris and Siliconix
- ☐ Low ON resistance

Model	Type	Off Output Leakage (max, full temp)	R_{ON} (max, full temp)	Switch ON Time (typ, 25°C)	Replaces
MP200DI	Dual, SPST	500 nA	100 ohm	240 nsec	DG200 HI200
MP201DI	Quad, SPST	500 nA	125 ohm	185 nsec	DG201 HI201
MP7510DI	Quad, SPST	500 nA	175 ohm	180 nsec	AD7510DI
MP7511DI	Quad, SPST	500 nA	175 ohm	180 nsec	AD7511DI
MP7512DI	Dual, SPDT	500 nA	175 ohm	180 nsec	AD7512DI

All Micro Power System's IC's are available with 883B processing, in dice form, or to customer's specifications.

MICRO POWER SYSTEMS
3100 Alfred Street
Santa Clara, CA 95050
(408) 727-5350

MOTOROLA
SEMICONDUCTORS
P.O. BOX 20912 • PHOENIX, ARIZONA 85036

FLOPPY DISK SUPPORT

MC3470P
MC3470AP

Specifications and Applications Information

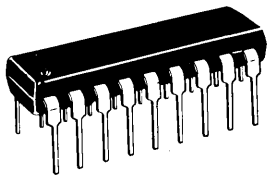
FLOPPY DISK READ AMPLIFIER SYSTEM

SILICON MONOLITHIC
INTEGRATED CIRCUIT

FLOPPY DISK READ AMPLIFIER

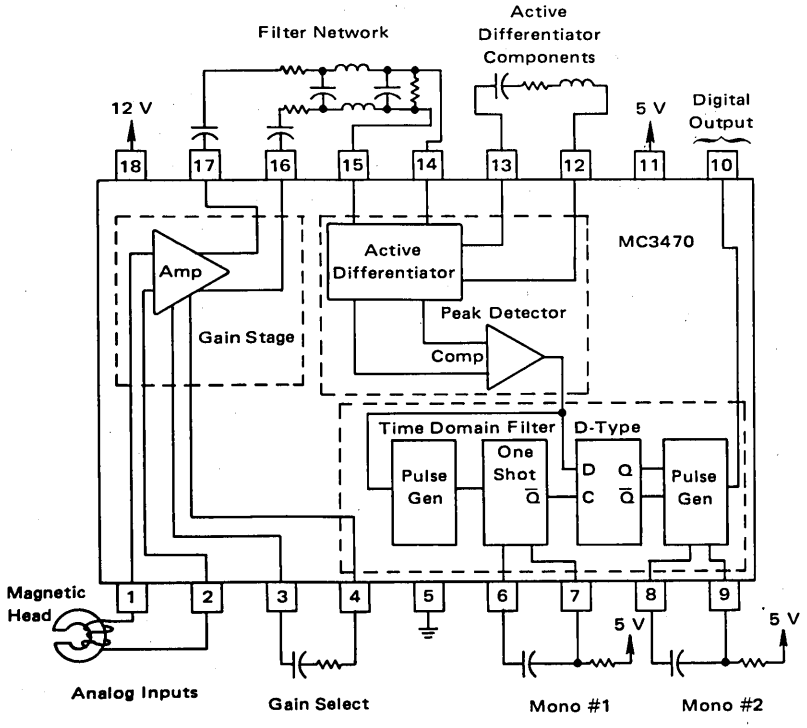
The MC3470 is a monolithic READ Amplifier System for obtaining digital information from floppy disk storage. It is designed to accept the differential ac signal produced by the magnetic head and produce a digital output pulse that corresponds to each peak of the input signal. The gain stage amplifies the input waveform and applies it to an external filter network, enabling the active differentiator and time domain filter to produce the desired output.

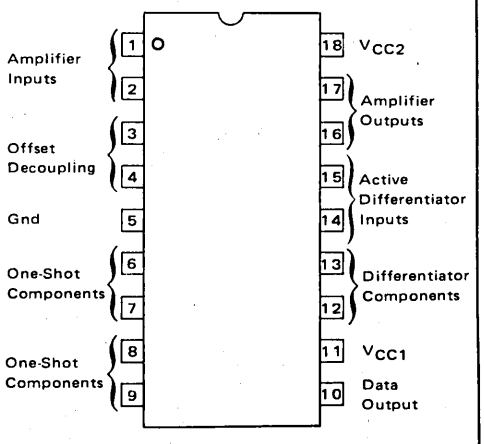
- Combines All the Active Circuitry To Perform the Floppy Disk Read Amplifier Function in One Circuit
- Guaranteed Maximum Peak Shift of 2.0% — MC3470A
- Improved (Positive) Gain T_C and Tolerance
- Improved Input Common Mode



P SUFFIX
PLASTIC PACKAGE
CASE 701-01

TYPICAL APPLICATION





DS9588
(Replaces ADI-512)

MOTOROLA
SEMICONDUCTORS
P.O. BOX 20912 • PHOENIX, ARIZONA 85036

FLOPPY DISK SUPPORT

MC3469P
MC3471P

Specifications and Applications Information

FLOPPY DISK
WRITE CONTROLLERS

SILICON MONOLITHIC
INTEGRATED CIRCUIT

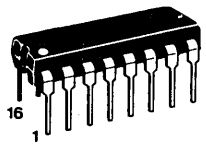
FLOPPY DISK WRITE CONTROLLER

The MC3469 and MC3471 are monolithic WRITE Current Controllers designed to provide the entire interface between floppy disk heads and the head control and write data signals for straddle-erase or tunnel-erase heads.

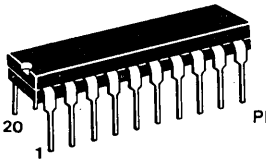
Provisions are made for selecting a range of accurately controlled write currents and for head selection during both read and write operation. Additionally, provisions are included for externally adjusting degauss period and inner/outer trace compensation.

The MC3471 provides the erase delay and inhibit functions required to interface with tunnel-erase heads.

- Head Selection — Current Steering Through Write Head and Erase Coil in Write Mode
- Provides High Impedance (Read Data Enable) during Read Mode
- Head Current (Write) Guaranteed Using Laser Trimmed Internal Resistor (3.0 mA using R_{ext} = 10 kΩ)
- IRW Select Input Provides for Inner/Outer Track Compensation
- Degauss Period Externally Adjustable
- Specified with ±10% Logic Supply and Head Supply (V_{BB}) from 10.8 V to 26.4 V
- Minimizes External Components
- MC3471 Provides On-Chip Adjustable Erase Delays

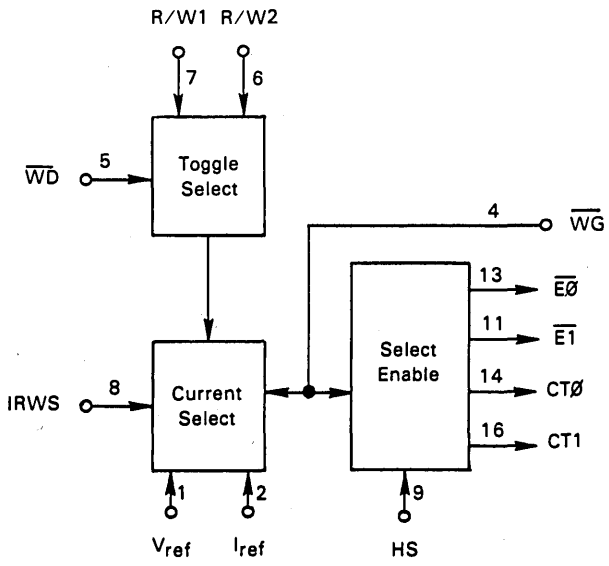


MC3469 only
P SUFFIX
PLASTIC PACKAGE
CASE 648

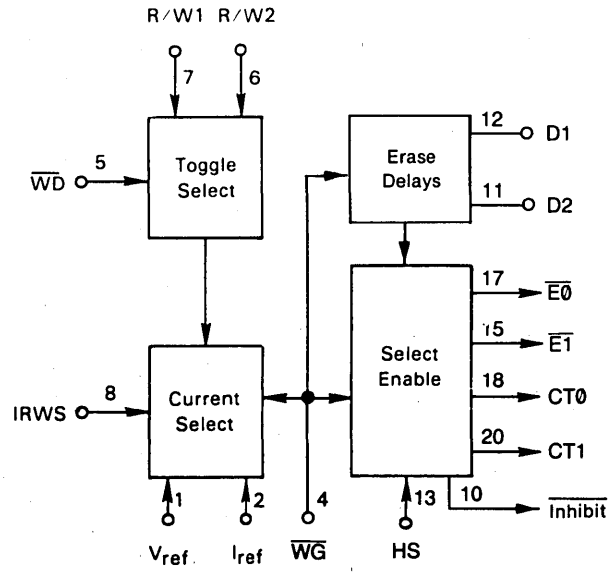


MC3471 only
P SUFFIX
PLASTIC PACKAGE
CASE 738

MC3469
BLOCK DIAGRAM



MC3471
BLOCK DIAGRAM



DS9577

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MC3482A/MC6882A
MC3482B/MC6882B

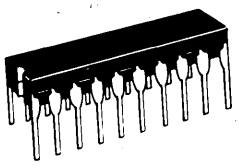
This device may be ordered under either of the above type numbers.

OCTAL THREE-STATE BUFFER/LATCH

This series of devices combines four features usually found desirable in bus-oriented systems: 1) High impedance logic inputs insure that these devices do not seriously load the bus; 2) Three-state logic configuration allows buffers not being utilized to be effectively removed from the bus; 3) Schottky technology allows for high-speed operation; 4) 48 mA drive capability.

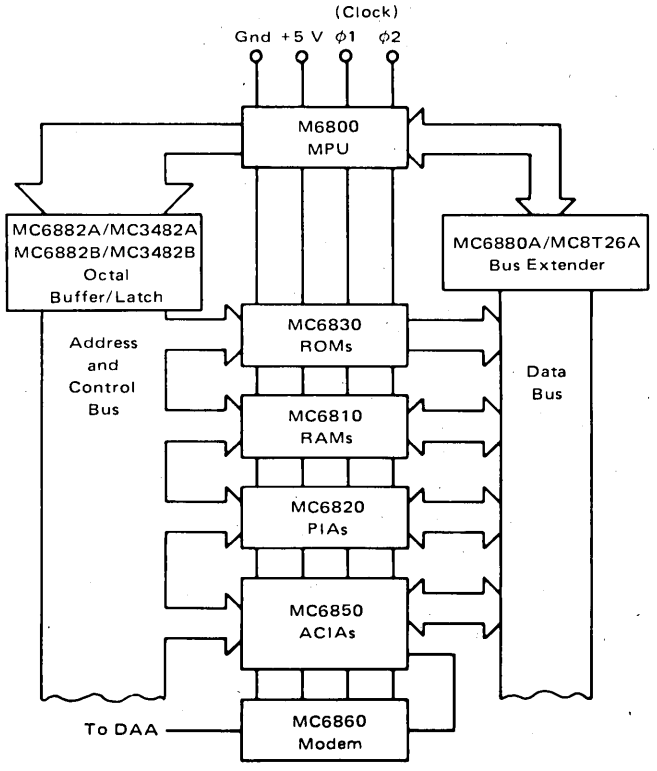
- Inverting and Non-Inverting Options of Data
- SN74S373 Function Pinouts
- Eight Transparent Latches/Buffers in a Single Package
- Full Parallel-Access for Loading and Reloading
- Buffered Control Inputs
- All Inputs Have Hysteresis to Improve Noise Rejection
- High Speed — 8.0 ns (Typ)
- Three-State Logic Configuration
- Single +5 V Power Supply Requirement
- Compatible with 74S Logic or M6800 Microprocessor Systems
- High Impedance PNP Inputs Assure Minimal Loading of the Bus

OCTAL THREE-STATE BUFFER/LATCH

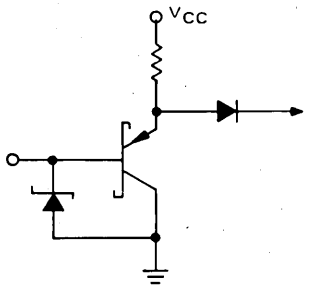


L SUFFIX
CASE 732

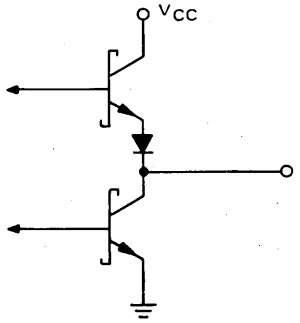
MICROPROCESSOR BUS EXTENDER APPLICATION



INPUT EQUIVALENT CIRCUIT



OUTPUT EQUIVALENT CIRCUIT



ORDERING INFORMATION

(Temperature Range for the following devices = 0 to +75°C.)

Device	Alternate	Package
MC6882AL	MC3482AL	Ceramic DIP
MC6882BL	MC3482BL	Ceramic DIP

MOTOROLA BROADLINE

BUS STANDARD LINE DRIVERS & RECEIVERS

STANDARD	INTRODUCED	1982 INTRODUCTION	1983 INTRODUCTION
RS232C	MC1488 DR MC1489 REC		
RS422	MC3486 REC MC3487 DR AM26LS31 DR	AM26LS32 REC	
RS423	MC3487 DR	μA9636A (MC3488A)	
RS-aaa (PARTY LINE)		SN75172 REC SN75174 REC	SN75173 DR SN75175 DR SN75176-8
IEEE 488-1978	MC3440-43A MC3446A MC3448A MC3447		
IBM GA-22-6974-3	MC3481 MC3485 MC75125-9		

PERIPHERAL DRIVERS

PART NUMBER	DESCRIPTION	INPUT COMPATIBILITY
MC1411P (ULN2001A) MC1412P (ULN2002A) MC1413P (ULN2003A) MC1416P (ULN2004A)	Seven Element Darlington Array (0.5 A Max)	General PMOS TTL/CMOS NMOS
MC1472U/P1	Dual Positive NAND	H1 Z(1)
ULN2801A ULN2802A ULN2803A ULN2804A	Octal Darlington Array (0.5 A Max)	General PMOS TTL/CMOS CMOS/PMOS
ULN2068B	Quad 1.5 A Darlington(2)	TTL/CMOS/DTL
ULN2074B	Quad 1.5 A Darlington(3)	General

(1) PNP Bufferer for TTL/MOS Compatibility
(2) Open Collector — Diode Clamped
(3) Open Collector — Open Emitter

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MICROPROCESSOR/COMPUTER INTERFACE
MC3481
MC3485

QUAD SINGLE-ENDED LINE DRIVER

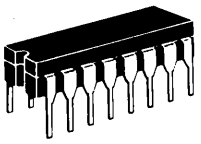
The MC3481 and MC3485 are quad single-ended line drivers specifically designed to meet the IBM 360/370 I/O specification (GA22-6974-3).

Output levels are guaranteed over the full range of output load and fault conditions. Compliance with the IBM requirements for fault protection, flagging, and power up/power down protection for the bus make this an ideal line driver for party line operations.

- Separate Enable and Fault Flags — MC3481
- Common Enable and Fault Flag — MC3485
- Power Up/Down Does Not Disturb Bus
- Schottky Circuitry for High-Speed — PNP Inputs
- Internal Bootstraps for Faster Rise Times
- Driver Output Current Foldback Protection
- MC3485 has LS Totem Pole Driver Output

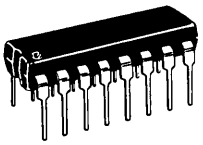
IBM 360/370 QUAD LINE DRIVER

SILICON MONOLITHIC
INTEGRATED CIRCUIT

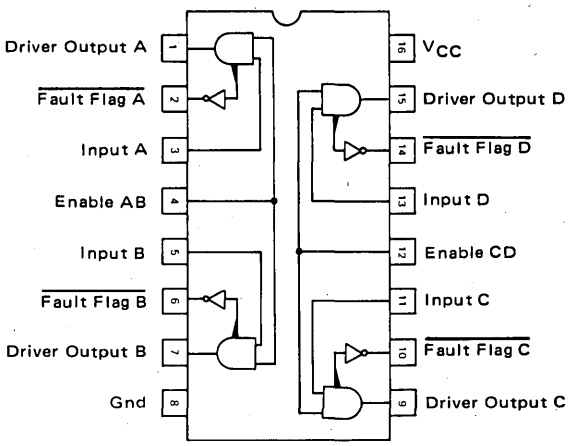


L SUFFIX
CERAMIC PACKAGE
CASE 620

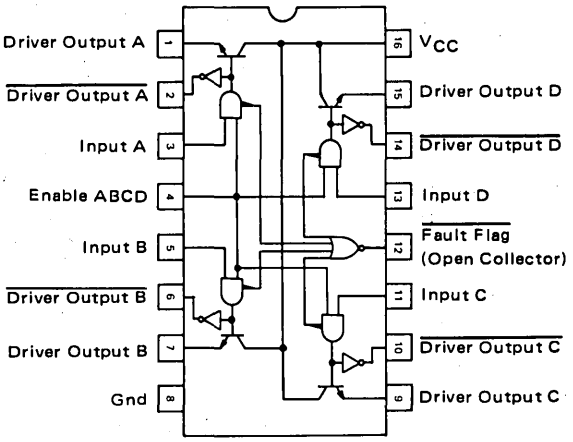
P SUFFIX
PLASTIC PACKAGE
CASE 648



MC3481
DUAL ENABLE
INDIVIDUAL FAULT FLAG



MC3485
COMMON ENABLE
COMMON FAULT FLAG



SUPPORTING IBM 360/370 LINE RECEIVERS

Device Number	No. of Channels	Input Resistance kΩ Min/Max	$I_{IH(R)}$ @V_{IH}=3.11 V mA Max	t_{PLH} @C_L=50 pF ns Max
MC75125/75127	Seven	7.4/20	0.42	25
MC75128/75129	Eight	7.4/20	0.42	25

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GPIB INSTRUMENTATION BUS INTERFACE MC3447

BIDIRECTIONAL INSTRUMENTATION BUS (GPIB) TRANSCEIVER

This bidirectional bus transceiver is intended as the interface between TTL or MOS logic and the IEEE Standard Instrumentation Bus (488-1978, often referred to as GPIB). The required bus termination is internally provided.

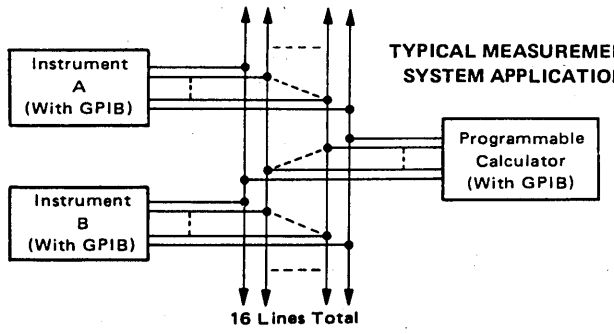
Low power consumption has been achieved by trading a minimum of speed for low current drain on non-critical channels. A fast channel is provided for critical ATN and EOI paths.

Each driver/receiver pair forms the complete interface between the bus and an instrument. Either the driver or the receiver of each channel is enabled by a Send/Receive input with the disabled output of the pair forced to a high impedance state. The receivers have input hysteresis to improve noise margin, and their input loading follows the bus standard specifications.

- Low Power — Average Power Supply Current = 30 mA Listening
  75 mA Talking
- Eight Driver/Receiver Pairs
- Three-State Outputs
- High Impedance Inputs
- Receiver Hysteresis — 600 mV (Typ)
- Fast Propagation Times — 15–20 ns (Typ)
- TTL Compatible Receiver Outputs
- Single +5 Volt Supply
- Open Collector Driver Output with Terminations
- Power Up/Power Down Protection (No Invalid Information Transmitted to Bus)
- No Bus Loading When Power is Removed From Device
- Required Termination Characteristics Provided

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

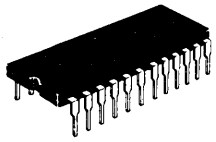
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	5.5	Vdc
Driver Output Current	$I_{O(D)}$	150	mA
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

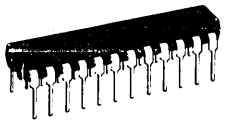


TYPICAL MEASUREMENT SYSTEM APPLICATION

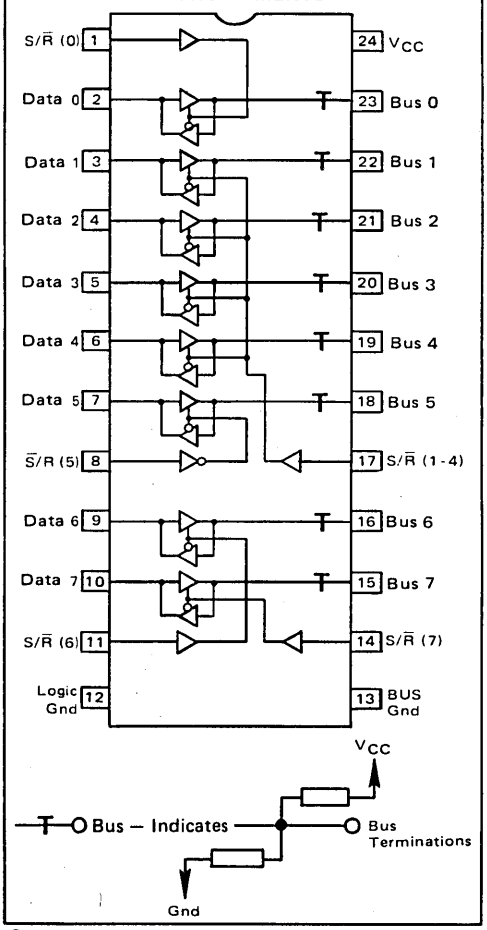
OCTAL BIDIRECTIONAL BUS TRANSCEIVER WITH TERMINATION NETWORKS

SILICON MONOLITHIC INTEGRATED CIRCUIT


L SUFFIX
CERAMIC PACKAGE
CASE 623


P3 SUFFIX
PLASTIC PACKAGE
CASE 724

PIN ASSIGNMENTS



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MC3419
MC3419A
MC3419C

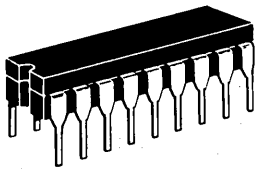
TELEPHONE LINE FEED AND 2- TO 4-WIRE CONVERSION CIRCUIT

. . . designed to replace the hybrid transformer circuit in Central Office, PABX and Subscriber carrier equipment, providing signal separation for two-wire differential to four-wire single-ended conversions and suppression of longitudinal signals at the two-wire input. It provides dc line current for powering the telset, operating from up to a 56 V supply

- All Key Parameters Externally Programmable
- Current Sensing Outputs Monitor Status of Both Tip and Ring Leads
- On-Hook Power Below 5.0 mW
- Digital Hook Status Output
- Power Down Input
- Ground Fault Protection
- Size and Weight Reduction Over Conventional Approaches
- The sale of this product is licensed under patent No. 4,004,109. All royalties related to this patent are included in the unit price.

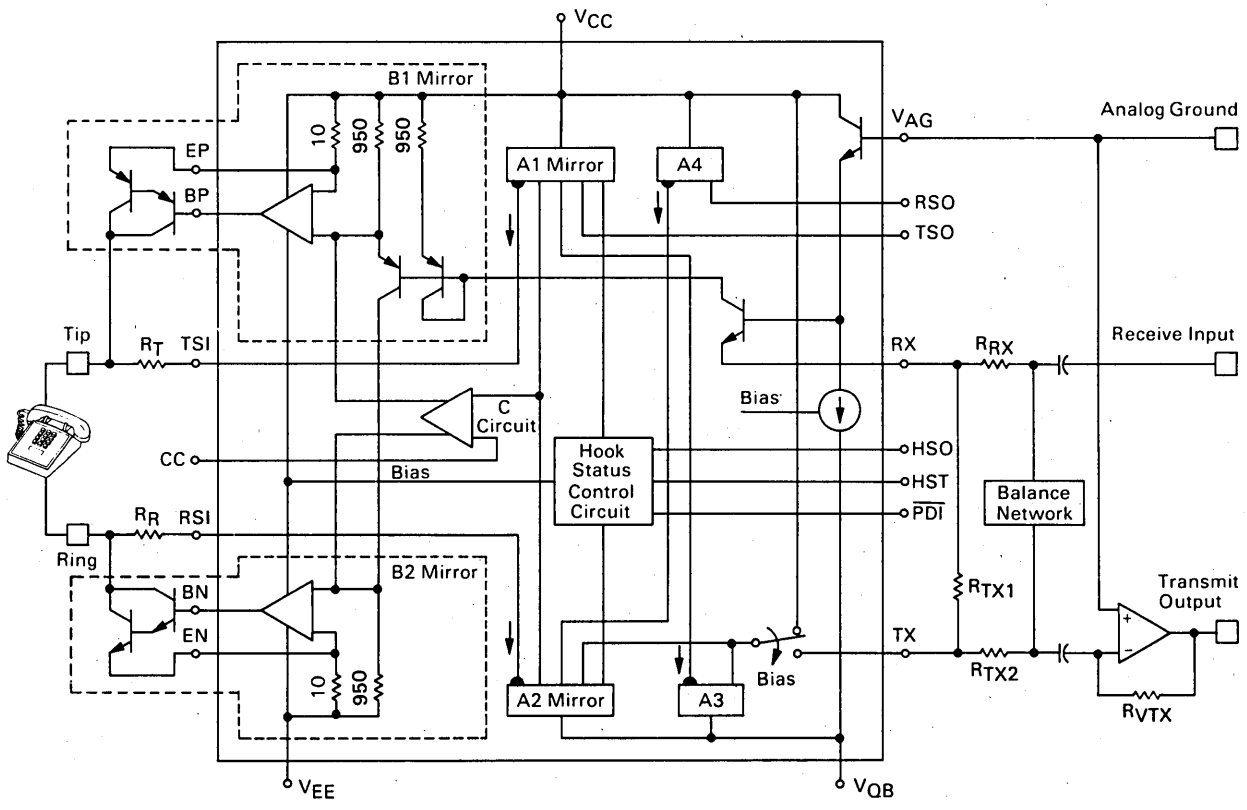
SUBSCRIBER LOOP INTERFACE CIRCUIT (SLIC)

BIPOLAR LASER-TRIMMED INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 726

FUNCTIONAL BLOCK DIAGRAM



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DATA CONVERSION
MC3412
MC3512

Advance Information

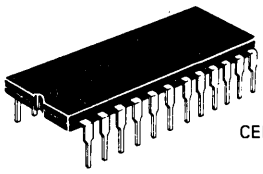
LASER TRIMMED HIGH-SPEED 12-BIT D/A CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT

COMPLETE 12-BIT HIGH-SPEED MONOLITHIC D/A CONVERTER

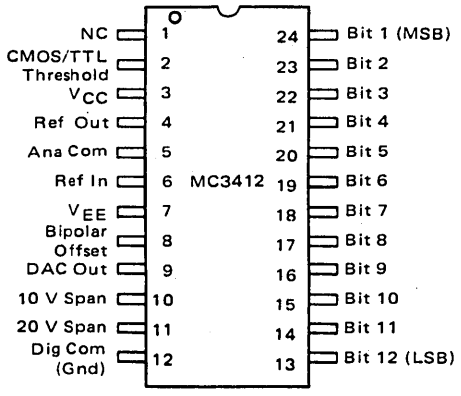
The MC3412/3512 is a monolithic 12-bit resolution D/A converter. It contains a high stability bandgap reference capable of supplying 1.5 mA externally, trimmed to ±0.25% maximum error. Active laser trimming of thin film ladder network, reference, span, bipolar offset, and bandgap resistors at wafer level provide accuracy and linearity of better than ±½ LSB. An innovative bit switching scheme provide fast settling time yet enables selection of CMOS or TTL thresholds. TTL threshold levels are retained over a wide V_{CC} range from 13.5 to 16.5 volts. Precision internal span resistors allow output voltage options of 0 to 5.0 V, 0 to 10 V, ±2.5 V, ±5.0 V, and ±10 V. 12-bit accuracy and a fast settling time of typically 200 ns (to ±½ LSB) make this converter ideal for applications such as a fast A/D building block or display driver.

- True 12-Bit Linearity: ±½ LSB Max
- Fast Settling Time: ±½ LSB in 200 ns Typ
- Fully Monotonic Over Temperature Range
- High-Stability Bandgap Voltage Reference On Chip
- Linearity Guaranteed Over Temperature
- Low Power Consumption: 210 mW
- Pinout Compatible with AD563 and AD565
- Selectable Digital Thresholds
- Internal Span Resistors for Generating Output Voltage

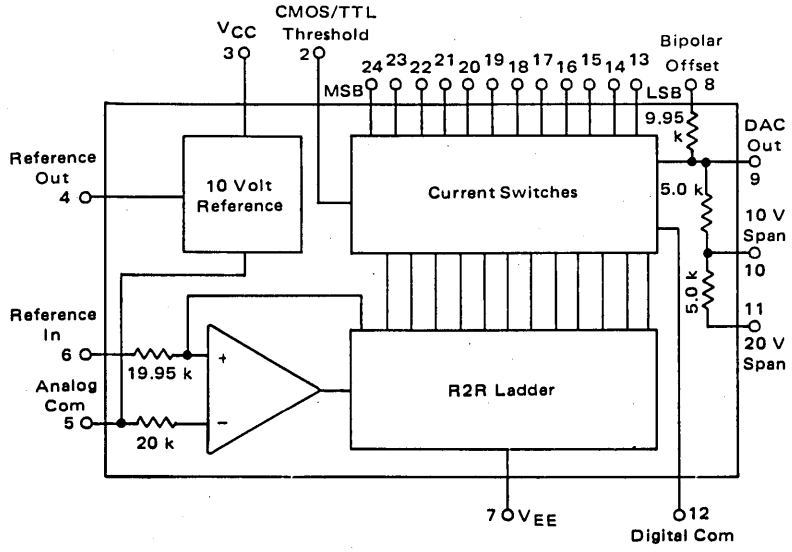


L SUFFIX
CERAMIC PACKAGE
CASE 623

PIN CONNECTIONS



BLOCK DIAGRAM



ORDERING INFORMATION

Device	Temperature Range	Package
MC3412L	0°C to +70°C	Ceramic DIP
MC3512L	−55°C to +125°C	Ceramic DIP

This is advance information and specifications are subject to change without notice.

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DATA CONVERSION

MC6890

Advance Information

MPU-BUS-COMPATIBLE 8-BIT D-TO-A CONVERTER

The MC6890 is a self-contained, bus-compatible, 8 bit (±0.19% accuracy) D-to-A converter system capable of interfacing directly with 8-bit microprocessors.

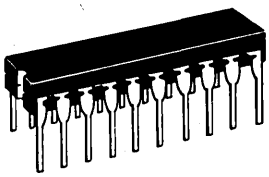
Available in both commercial and military temperature ranges, this monolithic converter contains master/slave registers to prevent transparency to data transitions during active enable; a laser-trimmed, low-TC, 2.5 V precision bandgap reference; and high stability, laser-trimmed, thin-film resistors for both reference input and output span and bipolar offset control.

A reset pin provides for overriding stored data and forcing I_{out} to zero.

- Direct Data Bus Link with All Popular TTL Level MPU's
- ±1/2 LSB Nonlinearity Over Temperature
- Fast Settling Time: 200 ns Typ
- Internal 2.5-V Precision Laser-Trimmed Voltage Reference (May Also Be Used Externally)
- Minimum $\overline{\text{Enable}}$ Pulse Width: 70 ns
- Fast $\overline{\text{Enable}}$: 10 ns Maximum Data Hold Time
- $\overline{\text{Reset}}$ Pin to Override Data
- Output Voltage Ranges: +5, +10, +20, or ±2.5, ±5, ±10 Volts
- Low Power: 90 mW Typ
- +5 V and -5 V to -15 V Supplies

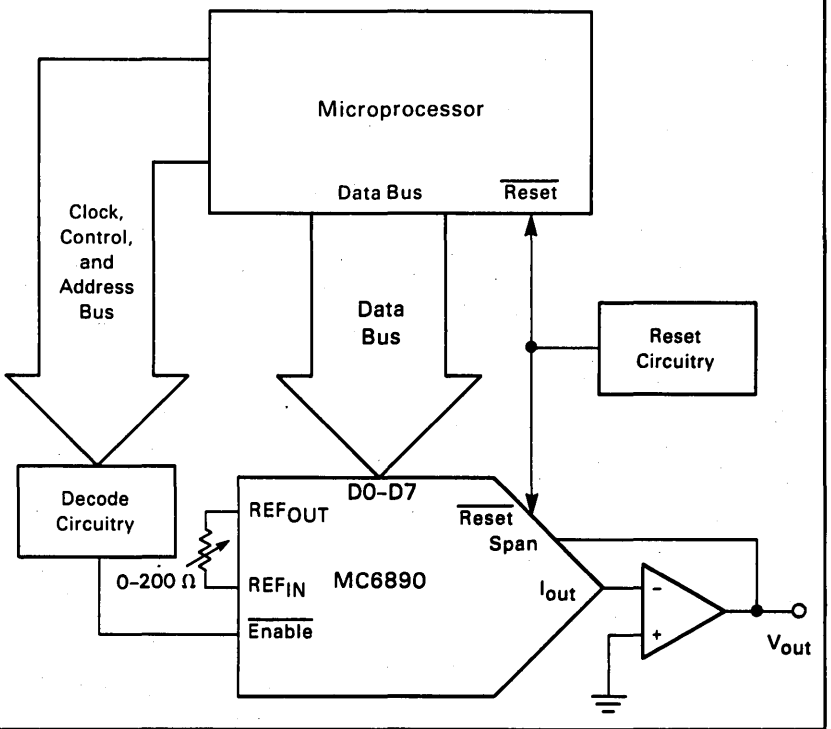
8-BIT MPU-BUS-COMPATIBLE DAC

SILICON MONOLITHIC INTEGRATED CIRCUIT

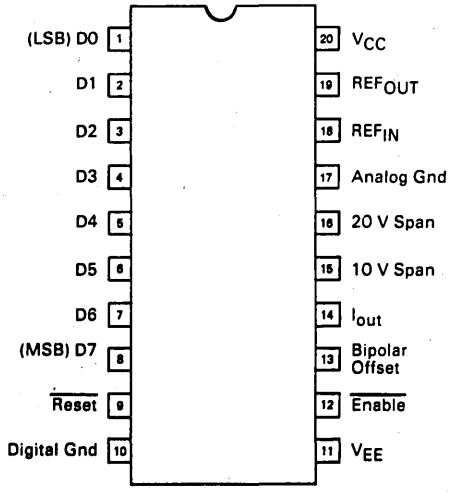


L SUFFIX
CASE 732

OPERATION WITH AN MPU



PIN CONNECTIONS



ORDERING INFORMATION

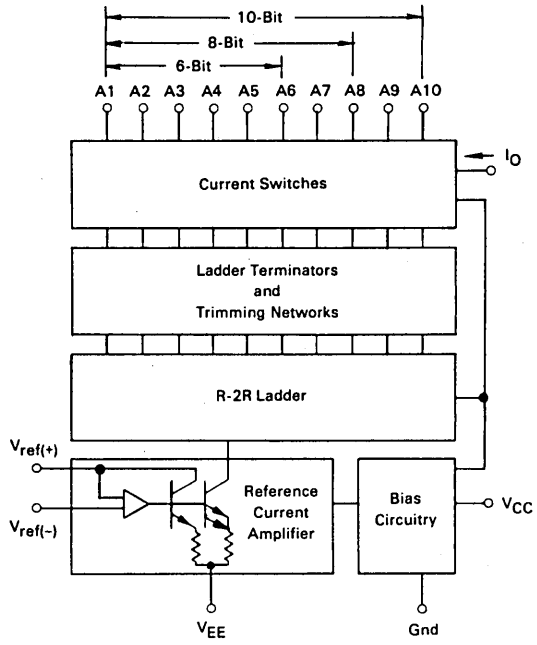
Device	Temperature Range	Package
MC6890L	0° to +70°C	Ceramic DIP
MC6890AL	-55° to +125°C	Ceramic DIP

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ADI-592R2

ADDITIONAL D-A CONVERTERS

General Purpose



Device Number	Error (%Max)	P_D @ V_{EE} = -5 V (mW Max)	$t_{Settling}$ (ns Typ)	I_O (mA)	Suffix	Case
6-Bit						
MC1506* MC1406	±0.78	120	150	1.9 to 2.1	L	632
8-Bit						
DAC-08A	±0.1	48	85	2.984 to 2.880	Q	620
DAC-08*	±0.19					
DAC-08H	±0.1			1.940 to 2.040	P, Q	648,620
DAC-08E	±0.19					
DAC-08C	±0.39					
MC1508L8* MC1408L8	±0.19	170	300	1.9 to 2.1	L	620
MC1408L7	±0.39				L, P	620, 648
MC1408L6	±0.78					
MC3408	±0.5				L	620
10-Bit						
MC3510* MC3410	±0.05	220	250	3.8 to 4.2	L	690
MC3410C	±0.1				L, P	690, 648
12-Bit						
AD562SD*	±0.006	210	200	1.6 to 2.4	D	716
AD562AD # **AD562KD**	±0.01					
AD563TD* **AD563SD*** **AD563KD**	±0.006	210	200	1.6 to 2.4	D	716
AD563JD	±0.01					

*T_A = -55 to +125°C #T_A = -25 to +85°C Devices without symbol: T_A = 0 to +70°C

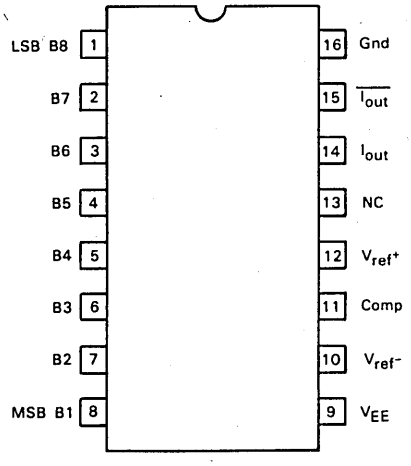
Bold Part Numbers Indicate New Products.

D-A CONVERTERS — HIGH SPEED

MC10318 series — A high speed 8-bit D/A converter capable of data conversion rates in excess of 25 MHz. It is intended for applications in high speed instrumentation and communication equipment, graphics displays, storage oscilloscopes, radar processing, and TV broadcast systems. The inputs are compatible with MECL 10,000 series logic, while the complementary current outputs have 51 mA full scale capability. Monotonic over the full temperature range, the outputs typically settle in 10 ns.

T_A = 0 to 70°C

Packages:
L Suffix — Case 620/690



Device Number	Error % Max	P_D @ V_{EE} = -5.2 V mW Max	$t_{Settling}$ ns Typ (to ½ LSB)	I_O & $\overline{I_O}$ @V_{Ref} = 10.56 V mA Typ
MC10318CL6	±0.78	675	10	51
MC10318CL7	±0.39	675	10	51
MC10318L	±0.19	675	10	51
MC10318L9	±0.10	675	10	51

Bold Part Numbers Indicate New Products.

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DATA CONVERSION

MC10315L
MC10317L

Advance Information

SEVEN-BIT PARALLEL HIGH SPEED A/D CONVERTER (WITH OVERRANGE)

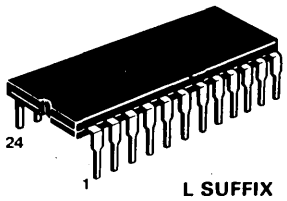
The MC10315L/MC10317L is a 7-bit high speed parallel A/D converter which employs ECL processing. The device consists of 128 parallel latched comparators across a high quality input reference network. The 128 comparator outputs are then fed to a 128-to-7 encoder and latched to the outputs which are ECL compatible. An overrange bit is provided to allow overrange sensing, or to facilitate the connection of an MC10315L and MC10317L in parallel to produce an 8-bit A/D converter. The MC10315L and MC10317L are identical devices except for the method of overranging used, which simplifies the utilization of two 7-bit converters to produce an 8-bit conversion. (See ordering information and technical description.)

Applications include video display and radar signal processing, high speed instrumentation, and TV broadcast video encoding.

- 7-Bit Resolution/8-Bit Accuracy Plus Overrange
- Direct Interconnection for 8-Bit Conversion
- 15 MHz Sampling Rate
- Wide Range of Input Voltage: ±2.0 Volts
- Low Input Capacitance: ≤70 pF
- 1.2 Watt Power Dissipation
- No Sample and Hold Required for Video Bandwidth Signals
- Standard 24-Pin Package

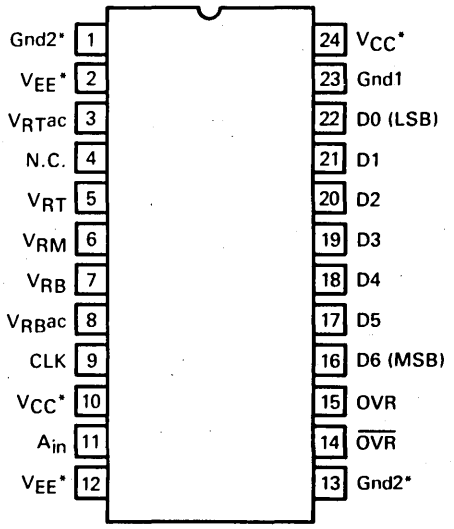
HIGH SPEED 7-BIT ANALOG-TO-DIGITAL FLASH CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT



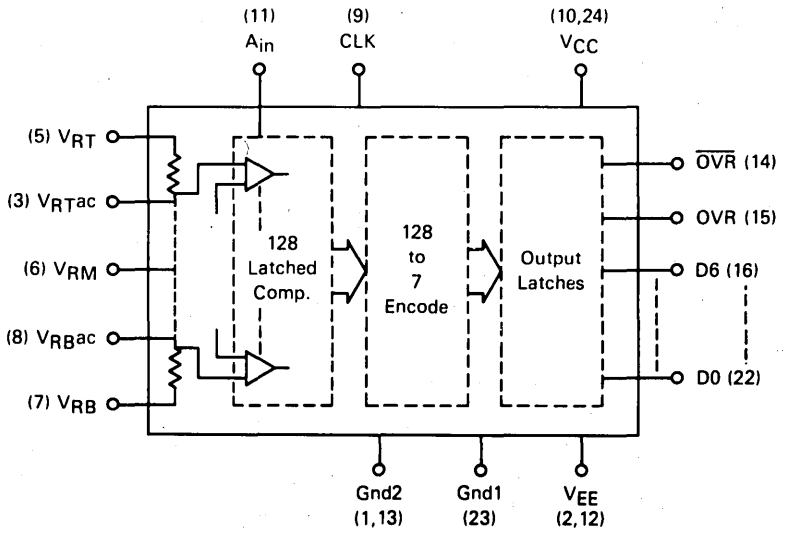
L SUFFIX
CERAMIC PACKAGE
CASE 623

PIN DIAGRAM



*V_{CC}, V_{EE} and Gnd2 are each available on two pins. Interconnections for the respective function are made on chip. To minimize I•R drops on chip and in the bonding wires, utilization of both pins for each function is recommended.

MC10315L/MC10317L DEVICE/APPLICATION CONFIGURATION



ORDERING INFORMATION**

Device	Overrange Function		
	Analog Input Condition	Logic Levels	
		OVR Bit	D0-D6 Bits
MC10315L	Overranged	High	High
MC10317L	Overranged	High	Low

**For information regarding an evaluation board, contact Linear Marketing.

ADI-654R1

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MOTOROLA
SEMICONDUCTORS
P.O. BOX 20912 • PHOENIX, ARIZONA 85036

PRECISION CIRCUITS
MC1400 MC1400A MC1500 MC1500A

Advance Information

Tight-Tolerance, Low-Drift Voltage Reference Family

The MC1400 series of ICs is a family of temperature-compensated voltage references for precision data conversion and instrumentation applications. Advances in thin-film resistors, laser-trimming techniques, ion-implanted devices, and monolithic fabrication techniques make this reference both temperature and time stable in applications demanding accuracy to the 12-bit level.

PRECISION VOLTAGE REFERENCES

2.5, 5.0, 6.25 and 10-VOLT

LASER-TRIMMED SILICON MONOLITHIC INTEGRATED CIRCUIT

Features

- Four Different Output Voltages: 2.5, 5.0, 6.25, 10 V
- Tight Absolute Accuracy: ±0.2% Maximum Initial Tolerance
- Single-Component Output Trimming Without Degrading Temperature Coefficient
- Wide Input Voltage Range: $(V_{out} + 1.0\,V) \leq V_{in} \leq 40\,V$
- Three-Terminal Operation: Positive References That Can Source and Sink Current
- Two-Terminal Operation: Positive or Negative References Floating References
- Low Current Consumption: 1.0 mA Typical
- Very Low Temperature Coefficient
- Low Output Noise Voltage
- Excellent Ripple Rejection: 87 dB Typical at 120 Hz
- Excellent Long Term Stability: 25 ppm/1000 Hrs Typical

Device Selection Table

Vout Volts Typ	IO mA Max	ΔVout/ΔT ppm/°C Max	Device Number	Regline mV Max	Regload mV Max	TA °C
2.5 ± 5.0 mV	±10	25	MC1400U2	3.0	10	0 to +70
		10	MC1400AU2			
		40	MC1500U2	(Note 1)	(Note 4)	−55 to +125
		10	MC1500AU2			
2.5 ± 25 mV	10	40	MC1403	3.0/4.5	10	0 to +70
		25	MC1403A			
		55	MC1503	(Note 2)	(Note 5)	−55 to +125
		25	MC1503A			
5.0 ± 10 mV	±10	25	MC1400U5	4.0	20	0 to +70
		10	MC1400AU5			
		40	MC1500U5	(Note 1)	(Note 4)	−55 to +125
		10	MC1500AU5			
5.0 ± 50 mV	10	40	MC1404U5	6.0	10	0 to +70
		25	MC1404AU5			
		55	MC1504U5	(Note 3)	(Note 5)	−55 to +125
		25	MC1504AU5			
6.25 ± 10 mV	±10	25	MC1400U6	4.0	20	0 to +70
		10	MC1400AU6			
		40	MC1500U6	(Note 1)	(Note 4)	−55 to +125
		10	MC1500AU6			
6.25 ± 60 mV	10	40	MC1404U6	6.0	10	0 to +70
		25	MC1404AU6			
		55	MC1504U6	(Note 3)	(Note 5)	−55 to +125
		25	MC1504AU6			
10 ± 20 mV	±10	25	MC1400U10	4.0	20	0 to +70
		10	MC1400AU10			
		40	MC1500U10	(Note 1)	(Note 4)	−55 to +125
		10	MC1500AU10			
10 ± 100 mV	10	40	MC1404U10	6.0	10	0 to +70
		25	MC1404AU10			
		55	MC1504U10	(Note 3)	(Note 5)	−55 to +125
		25	MC1504AU10			

Notes:
1. $(V_{out} + IV) \leq V_{in} \leq 40$ V
2. $4.5\,V \leq V_{in} \leq 15$ V
   $15\,V \leq V_{in} \leq 40$ V
3. $(V_{out} + 2.5\,V) \leq V_{in} \leq 40$ V
4. $-10\,mA \leq I_L \leq +10\,mA$
5. $0\,mA \leq I_L \leq 10\,mA$

This is advance information and specifications are subject to change without notice.

National Semiconductor

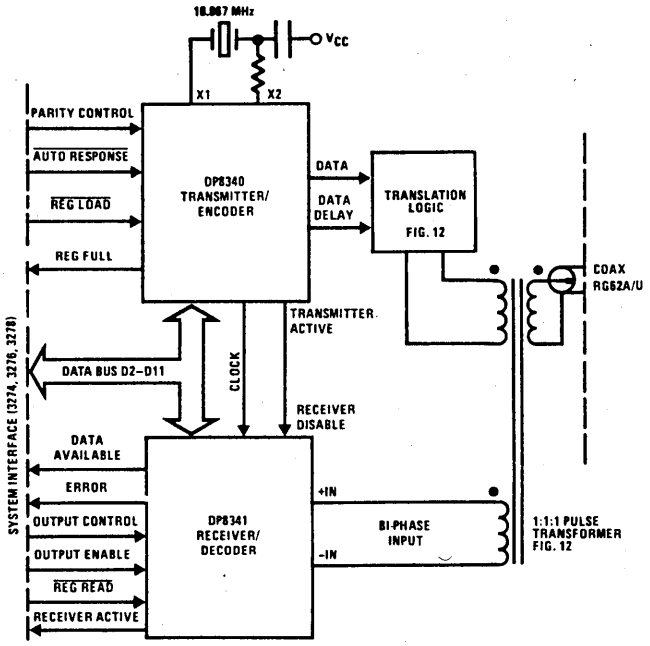
DP8340 Serial Bi-Phase Transmitter/Encoder
DP8341 Serial Bi-Phase Receiver/Decoder

General Description

The DP8340 generates a complete encoding of parallel data for high speed serial transmission which conforms to the protocol as defined by the IBM 3270 information display system standard. The DP8340 converts parallel input data into a serial data stream. Although the IBM standard covers bi-phase serial data transmission over a coax line, the DP8340 also adapts to general high speed serial data transmission over other than coax lines, at frequencies either higher or lower than the IBM standard.

The DP8341 provides complete decoding of data for high speed serial data communications. In specific, the DP8341 recognizes serial data that conforms to the IBM 3270 Information Display System Standard and converts it into ten (10) bits of parallel data. Although this standard covers Bi-Phase serial data transmission over a coax line, this device easily adapts to generalized high speed serial data transmission on other than coax lines at frequencies either higher or lower than the IBM 3270 standard.

The DP8341 receiver and its complementary chip, the DP8340 transmitter, are designed to provide maximum flexibility in system designs. The separation of transmitter and receiver functions allows addition of more receivers at one end of the Bi-Phase line without the necessity of adding unused transmitters. This is advantageous specifically in control units where typically Bi-Phase data is multiplexed over many Bi-Phase lines and the number of receivers generally outnumber the number of transmitters. The separation of transmitter and receiver function provides an additional advantage in flexibility of data bus organization. The data bus outputs of the receiver are TRI-STATE®, thus enabling the bus configuration to be organized as either a common transmit/receive (bi-directional) bus or as separate transmit and receive busses for higher speed.



Typical Application for IBM 3270 Interface

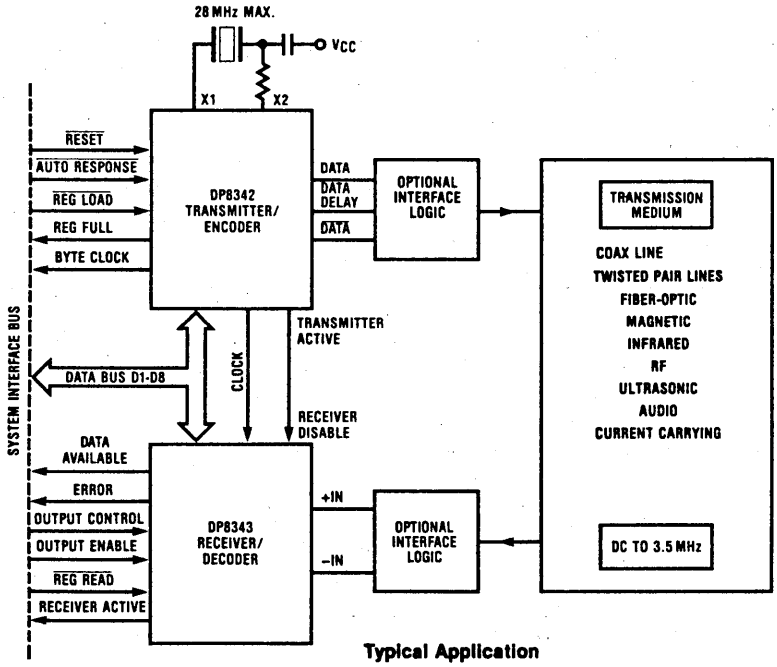
DP8342 High Speed Serial Transmitter/Encoder
DP8343 High Speed Serial Receiver/Decoder

General Description

The DP8342 generates a complete encoding of parallel data for high speed serial transmission. It generates a five bit starting sequence, three bit code violation, followed by a syn bit and eight bit per byte of data plus a parity bit. A three-bit ending code signals the termination of the transmission.

The DP8343 provides complete decoding of data for high speed serial data communications. In specific, the DP8343 receiver recognizes Bi-Phase serial data sent from its complementary chip, the DP8342 transmitter, and converts it into eight (8) bits of parallel data. These devices are easily adapted to generalized high speed serial data transmission systems that operate at bit rates up to 3.5 MHz.

The DP8342 and its complementary chip, the DP8343 (receiver/decoder) have been designed to provide maximum flexibility in system designs. The separation of the transmitter/receiver functions provides convenient addition of more receivers at one end of a bi-phase line without the need of unused transmitters. This is specifically advantageous in control units where typical bi-phase data is multiplexed over many bi-phase lines and the number of receivers generally exceeds the number of transmitters.



Typical Application

National Semiconductor

JUNE 1981

DP8350 Series CRT Controllers

General Description

The DP8350 Series of CRT Controllers are single-chip bipolar (I^2L technology) circuits in a 40-pin package. They are designed to be dedicated CRT display refresh circuits. Three standard products are available, designated DP8350, DP8352, DP8353. Custom devices, however, are available in a broad range of mask programmable options.

The CRT Controller (CRTC) provides an internal dot rate crystal controlled oscillator for ease of system design. For systems where a dot rate clock is already provided, an external clock may be inputted to the CRTC. In either case system synchronization is made possible with the use of the buffered Dot Rate Clock Output.

The DP8350 Series has 11 character generation related timing outputs. These outputs are compatible for systems with or without line buffers, using character ROMs, or DM86S64-type latch/ROM/shift register circuits.

12 bits (4k) of bidirectional TRI-STATE® character memory addresses are provided by the CRTC for direct interface to character memory.

Three on-chip registers provide for external loading of the row starting address, cursor address, and top-of-page address.

A complete set of video outputs is available including cursor enable, vertical blanking, horizontal sync, and vertical sync.

The DP8350 Series CRTC provides for a wide range of programmability using internal mask programmable ROMs:

- Character Field (both number of dots/character and number of scan lines/character)
- Characters per Row
- Character Rows per Video Frame
- Format of Video Outputs

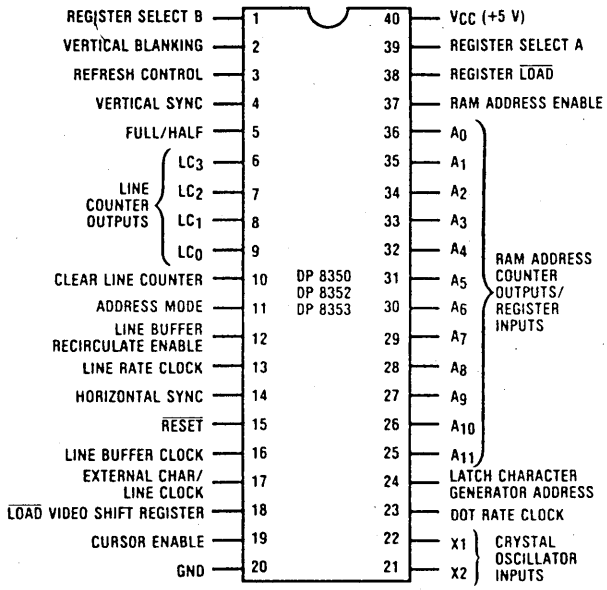
The CRTC also provides system sync and program inputs including Refresh Control, Reset, and Address Mode.

TRI-STATE is a registered trademark of National Semiconductor Corp.

Features

- Internal crystal controlled dot rate oscillator
- External dot rate clock input
- Buffered dot rate clock output
- Timing pulses for character generation
- Character memory address outputs (12 bits)
- Internal cursor address register
- Internal row starting address register
- Internal top-of-page address register (for scrolling)
- Programmable horizontal and vertical sync outputs
- Programmable cursor enable output
- Programmable vertical blanking output
- 2 programmable refresh rates, pin selectable
- Programmable characters/row (128 max.)
- Progammable character field size (up to 16 dots × 16 scan line field size)
- Programmable scan lines/frame (512 max.)
- Programmable character rows/frame
- Single +5V power supply
- Inputs and outputs TTL compatible
- Direct interface with DM86S64 character generator
- Ease of system design/application

Connection Diagram



Ordering Information:

DP8350N
DP8352N
DP8353N

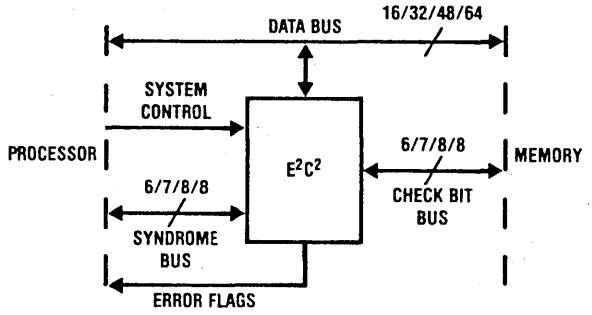
National Semiconductor

September 1982

DP8400 — E^2C^2 Expandable Error Checker and Corrector

General Description

The DP8400 Expandable Error Checker and Corrector (E^2C^2) aids system reliability and integrity by detecting errors in memory data and correcting single or double-bit errors. The E^2C^2 data I/O port sits across the processor-memory data bus as shown, and the check bit I/O port connects to the memory check bits. Error flags are provided, and a syndrome I/O port is available. Fabricated using high speed Schottky technology in a 48-pin dual-in-line package, the DP8400 has been designed such that its internal delay times are minimal, maintaining maximum memory performance.



For a 16-bit word, the DP8400 monitors data between the processor and memory, with its 16-bit bidirectional data bus connected to the memory data bus. The DP8400 uses an encoding matrix to generate 6 check bits from the 16 bits of data. In a WRITE cycle, the data word and the corresponding check bits are written into memory. When the same location of memory is subsequently read, the E^2C^2 generates 6 new check bits from the memory data and compares them with the 6 check bits read from memory to create 6 syndrome bits. If there is a difference (causing some syndrome bits to go high), then that memory location contains an error and the DP8400 indicates the type of error with 3 error flags. If the error is a single-bit error, the DP8400 will automatically correct it.

The DP8400 is easily expandable to other data configurations. For a 32-bit data bus with 7 check bits, two DP8400s can be used in cascade with no other ICs. Three DP8400s can be used for 48 bits, and four DP8400s for 64 data bits, both with 8 check bits. In all these configurations, single and double-error detection and single-error correction are easy to implement.

When the memory is more unreliable, or better system integrity is preferred, then in any of these configurations, double-error correction can be performed. One approach requires a further memory WRITE-READ cycle using complemented data and check bits from the DP8400. If at least one of the two errors is a hard error, the DP8400 will correct both errors. This implementation requires no more memory check bits or DP8400s than the single-error correct configurations.

The DP8400 has a separate syndrome I/O bus which can be used for error logging or error management. In addition, the DP8400 can be used in BYTE-WRITE applications (for up to 72 data bits) because it has separate byte controls for the data buffers. In 16 or 32-bit systems, the DP8400 will generate and check system byte parity, if required, for integrity of the data supplied from or to the processor. There are three latch controls to enable latching of data in various modes and configurations.

Operational Features

- Fast single and double-error detection
- Fast single-error correction
- Double-error correction after catastrophic failure with no additional ICs or check bits
- Functionally expandable to 100% double-error correct capability
- Functionally expandable to triple-error detect
- Directly expandable to 32 bits using 2 DP8400s only
- Directly expandable to 48 bits using 3 DP8400s only
- Directly expandable to 64 bits using 4 DP8400s only
- Expandable to and beyond 64 bits in fast configuration with extra ICs
- 3 error flags for complete error recording
- 3 latch enable inputs for versatile control
- Byte parity generating and checking
- Separate byte controls for outputting data in BYTE-WRITE operation
- Separate syndrome I/O port accessible for error logging and management
- On-chip input and output latches for data bus, check bit bus and syndrome bus
- Diagnostic capability for simulating check bits
- Memory check bit bus, syndrome bus, error flags and internally generated syndromes available on the data bus
- Self-test of E^2C^2 on the memory card under processor control
- Full diagnostic check of memory with the E^2C^2
- Complete memory failure detectable
- Power-on clears data and syndrome input latches

Timing Features

16-BIT CONFIGURATION

WRITE Time: 35 ns from data-in to check bits valid
DETECT Time: 30 ns from data-in to Any Error (AE) flag set
CORRECT Time: 65 ns from data-in to correct data out

 BF/2183

IM-B2.5M92/Printed in U.S.A.

National Semiconductor

ADVANCED INFORMATION
JUNE 1981

DP8409 Multi-Mode Dynamic RAM Controller/Driver

General Description

Dynamic memory system designs which formerly required several support chips to drive the memory array can now be implemented with a single DP8409 Multi-Mode Dynamic RAM Controller/Driver. The DP8409 is capable of driving all 4k, 16k, and 64k Dynamic RAMs (DRAMs) as well as all announced 256k DRAMs. Since the DP8409 is a one chip solution (including capacitive drivers), it minimizes propagation delay skews, the major performance disadvantage of multiple chip memory drive and control.

The DP8409's 8 modes of operation offers a wide selection of DRAM control capabilities. System access may be controlled externally or on-chip automatically; an on-chip refresh counter makes refreshing (either externally or automatically controlled) less complicated; and automatic memory initialization is both simple and fast.

The DP8409 is a 48-pin, Dynamic RAM Controller-Driver with 9 multiplexed address outputs and control signals. It consists of two 9 bit address latches, a 9 bit refresh counter and control logic. All output drivers are capable of driving 500pF loads with propagation delays of 20ns. 500pF is the typical capacitance of a line with 70 Dynamic RAMs (DRAMs), including trace capacitance.

The DP8409 has 3 mode pins M0, M1 and M2, where M0 is in general $\overline{\text{REFRESH}}$. These 3 pins allow 8 modes of operation, as shown in Table 1. The inputs B0 and B1 in the access modes (M0 = 1), are bank select inputs which select one of the four $\overline{\text{RAS}}$ outputs. The 9 address outputs can be selected from the Row Address Latch or the Column Address Latch, during normal access. During refresh, the on-chip 9 bit refresh counter can be enabled onto the address bus and in this mode all $\overline{\text{RAS}}$ outputs are selected.

The DP8409 can drive up to 4 banks of DRAMs, either 16ks, 64ks, or 256ks, but totalling less than 70 for speed-drive capability reasons. Control signal outputs $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ are provided with the same drive capability. Each $\overline{\text{RAS}}$ output drives one bank of DRAMs so that the four $\overline{\text{RAS}}$ outputs are used to select the banks, while $\overline{\text{CAS}}$, $\overline{\text{WE}}$ and the multiplexed addresses can be connected to all the banks of DRAMs. This leaves the non-selected banks in the standby mode (less than one tenth of operating power) with the data outputs in TRI-STATE®. Only the bank with its associated $\overline{\text{RAS}}$ low will be written to or read from.

Operational Features

- All DRAM drive functions on one chip — minimizes skew on outputs, maximizes AC performance
- Drives directly all 16k, 64k and 256k DRAMS
- Capable of addressing 64k, 256k or 1M words
- Address propagation delays of 20ns at 500pF
- Column address valid on output bus 20ns after R/C goes low
- $\overline{\text{CAS}}$ goes low 12ns after column addresses are valid
- $\overline{\text{WE}}$ goes low 15ns after $\overline{\text{WIN}}$ goes low
- On-chip 9 bit refresh counter with selectable End of Count (127, 255, or 511)
- End of Count indicated by RF I/O pin, going low at 127, 255 or 511
- Low Input on RF I/O resets 9 bit refresh counter
- $\overline{\text{CAS}}$ inhibited during refresh cycle
- Fall through latches on address inputs controlled by ADS
- TRI-STATE Outputs allow multi-controller addressing of the memory
- Control output signals go high impedance logic "1" when disabled
- Power up: counter reset, control signals high and address outputs TRI-STATE, and End of Count set to 127
- Pinout allows reversal of device in socket without part damage

Mode Features

- 8 modes of operation — 3 access, 3 refresh, and 2 set-up
- 2 external control modes — 1 access and 1 refresh (Modes 0, 4)
- 2 auto-access modes $\overline{\text{RAS}} \rightarrow \text{R}/\overline{\text{C}} \rightarrow \overline{\text{CAS}}$ automatic, with t_{RAH} = 20 or 30ns (Modes 5, 6)
- Slow auto-access mode allows Hidden Refreshing (Mode 5)
- Forced Refresh requested on RF I/O if no Hidden Refresh (Mode 5)
- Forced Refresh performed after System acknowledge of request (Mode 1)
- Internal Auto-Burst Refresh mode stops at End of Count of 127, 255, or 511 (Mode 2)
- Internal Auto-Burst mode used before and after DMA transfer (Mode 2)
- 2 All-$\overline{\text{RAS}}$ Access modes, external control or internal control (Mode 3a, 3b)
- External All-$\overline{\text{RAS}}$ mode with $\overline{\text{WE}}$ useful for memory initialization (Mode 3b)
- Internal All-$\overline{\text{RAS}}$ mode with $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ allows fast memory initialization (Mode 3a)
- Internal All-$\overline{\text{RAS}}$ mode with external 8-bit counter frees system for other set-up routines (Mode 3a)
- End of Count value of Refresh Counter set by B0, B1 (Mode 7)

National Semiconductor

June 1982

DP8460 MFM Data Separator

General Description

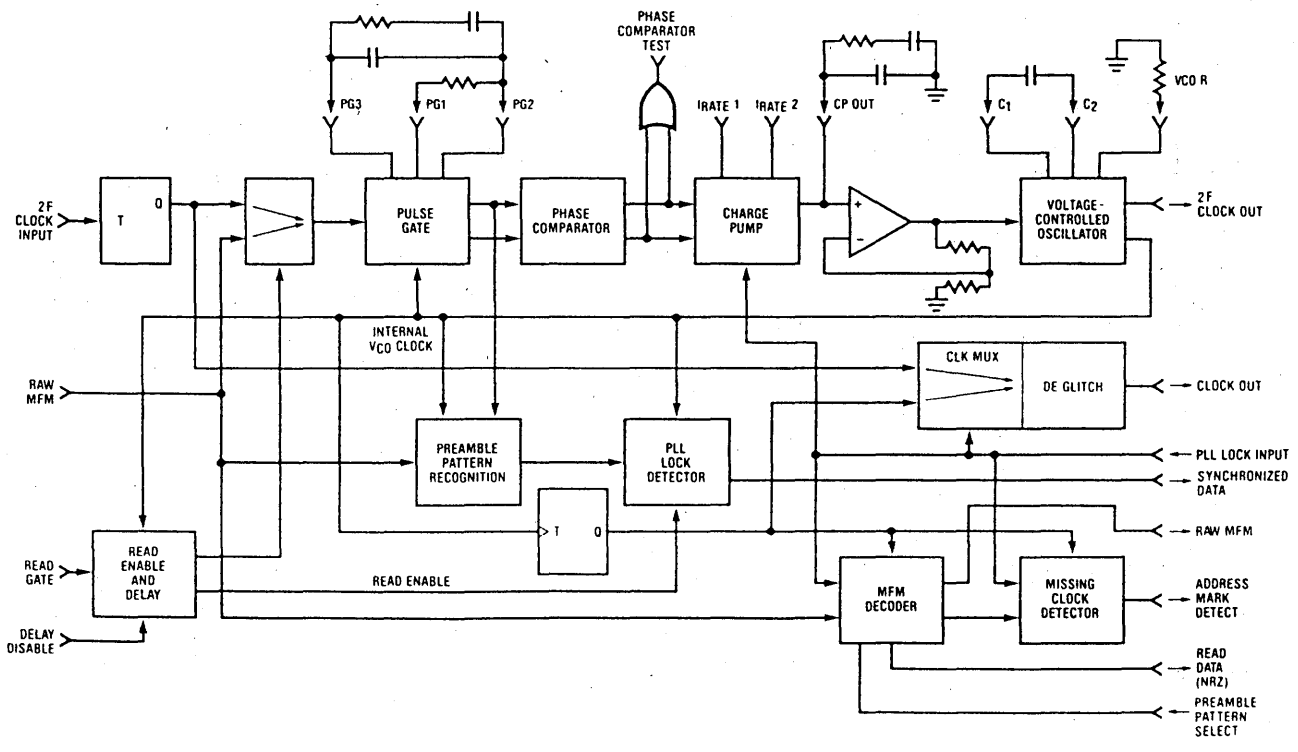
National Semiconductor Corporation's DP8460 MFM Data Separator Chip (Modified Frequency Modulation Decoder) is a monolithic bipolar integrated circuit used in disk drive systems. It receives raw MFM pulses from pulse detection logic and outputs both NRZ data and raw MFM synchronized to the on-chip VCO. The user may choose either of these outputs to apply to the controller depending on the type of system. All digital signals are at TTL logic levels and a single +5V power supply is required. The DP8460-2 will operate with data rates between 2 and 25 megabits per second. The DP8460-4 will operate with data rates between 2 and 12.5 megabits per second, and the DP8460-8 will operate from 2 to 6.25 megabits per second.

The read circuit features an internal phase-locked loop consisting of a pulse gate, phase comparator, charge pump, op-amp, and voltage-controlled oscillator. In addition to the DATA and CLOCK outputs, ADDRESS MARK DETECT, LOCK DETECT, PHASE COMPARATOR TEST, SYNCHRONOUS MFM, and 2F-CLOCK outputs are provided. The functional description will provide details concerning these outputs as well as circuit input requirements.

Features

- Fabricated on the same advanced oxide-isolated process as the ALS family.
- Decodes MFM data up to 25MBits/second.
- On-chip data and clock separation.
- PLL incorporates dual tracking rate (user-determined).
- Phase-lock indicator with external control of switchover from high-to-low track rate.
- Undecoded Input Data (synchronized with VCO) provided as an output.
- Decodes MFM with All Ones or All Zeros data preamble.
- ADDRESS MARK DETECT output.
- "OR-ed" outputs of phase comparator provided to aid in the testing of disk media.
- READ DELAY DISABLE input provided to reduce time required from READ GATE Command until beginning of PLL Lock sequence.
- Single +5V supply.

Block Diagram



National Semiconductor

PRELIMINARY
September 1982

DP84240/DP84244 Octal TRI-STATE® MOS Drivers

General Description

The DP84240 and DP84244 are octal TRI-STATE® drivers which are ideally suited as fast data buffers or as memory address drivers. The DP84240 is an inverting driver which is pin-compatible with both the 74S240 and AM2965. The DP84244 is a non-inverting driver which is pin-compatible with the 74S244 and AM2966. These parts are fabricated using an oxide isolation process, for much faster speeds, and are specified for 50 pF and 500 pF load capacitances.

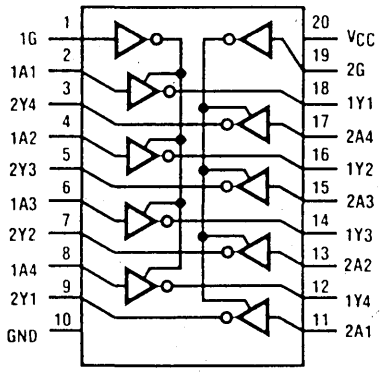
Features

- t_{pd} specified with 50 pF and 500 pF loads
- Output specified from 0.8V to 2.7V
- Designed for symmetric rise and fall times at 500 pF
- Outputs glitch free at power up and power down
- PNP inputs reduce DC loading on bus lines
- Low static and dynamic input capacitance
- Low skew times between edges and pins
- AC parameters fully tested

TRI-STATE is a registered trademark of National Semiconductor Corporation

Connection Diagrams

TOP VIEW



Truth Tables

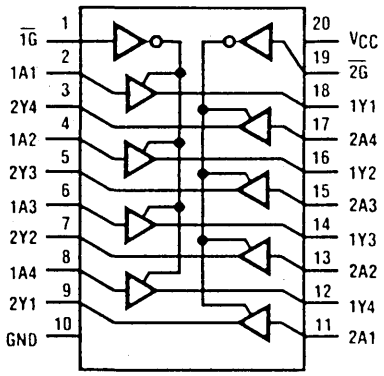
DP84240

Inputs $\overline{G}$	A	Outputs Y
H	X	Z
L	L	H
L	H	L

H = High Level
L = Low Level
X = Don't Care
Z = High Impedance

DP84244

TOP VIEW



Inputs $\overline{G}$	A	Outputs Y
H	X	Z
L	L	L
L	H	H

National Semiconductor

DS75160A/DS75161A/DS75162A/DS3666 IEEE-488 GPIB Transceivers

General Description

This family of high-speed-Schottky 8-channel bi-directional transceivers is designed to interface TTL/MOS logic to the IEEE Standard 488-1978 General Purpose Interface Bus (GPIB). PNP inputs are used at all driver inputs for minimum loading, and hysteresis is provided at all receiver inputs for added noise margin. The IEEE-488 required bus termination is provided internally with an active turn-off feature which disconnects the termination from the bus when V_{CC} is removed. A power up/down protection circuit is included at all bus outputs to provide glitch-free operation during V_{CC} power up or down.

The General Purpose Interface Bus is comprised of 16 signal lines—8 for data and 8 for interface management. The data lines are always implemented with DS75160A, and the management lines are either implemented with DS75161A in a single-controller system, or with DS75162A in a multi-controller system.

Features

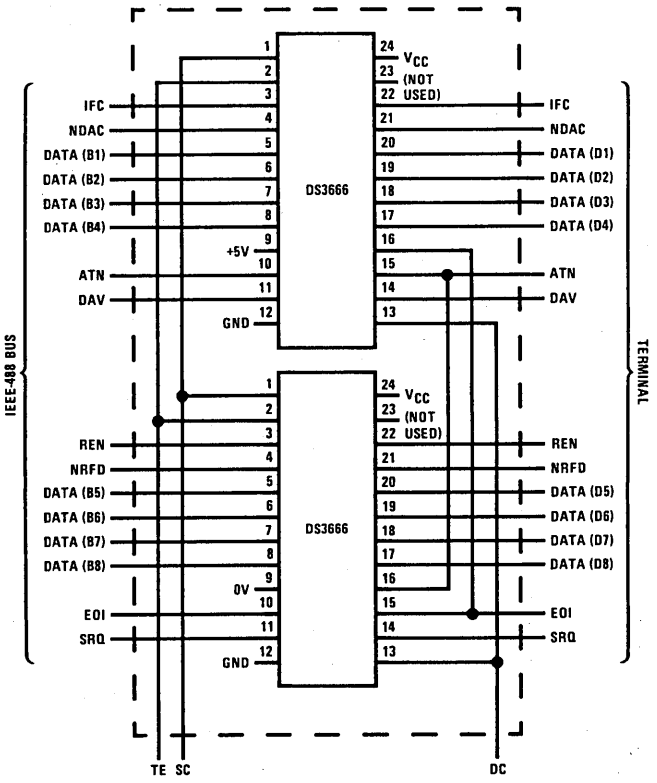
- 8-channel bi-directional non-inverting transceivers
- Bi-directional control implemented with TRI-STATE® output design
- Meets IEEE Standard 488-1978
- High-speed Schottky design
- Low power consumption
- High impedance PNP inputs (drivers)
- 500 mV (typ) input hysteresis (receivers)
- On-chip bus terminators
- No bus loading when V_{CC} is removed
- Power up/down protection (glitch-free)

DS3666 Functional Description

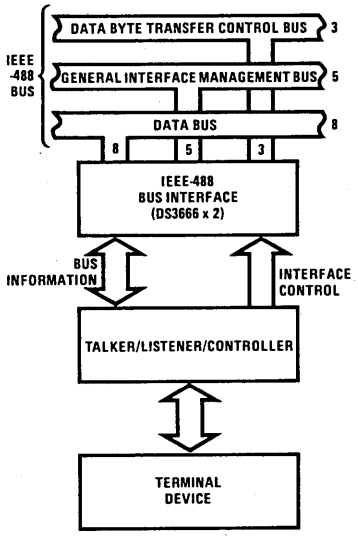
The DS3666 is a high-speed-Schottky 8-channel bi-directional transceiver designed to interface TTL/MOS logic to the IEEE Standard 488-1978 General Purpose Interface Bus.

Implementing the IEEE-488 bus interface is accomplished by connecting two DS3666 devices together using the expansion control inputs provided. Each device is assigned to 4 data channels and 4 management signal channels to achieve the 16-line format.

IEEE-488 Interface Configuration Implementation Using the DS3666



Terminal Interface Block Diagram



National Semiconductor

PRELIMINARY
April 1982

DS3658 Quad High Current Peripheral Driver

General Description

The DS3658 quad peripheral driver is designed for those applications where low operating power, high breakdown voltage, high output current and low output ON voltage are required. A unique input circuit combines TTL compatibility with high impedance. In fact, its extreme low input current allows it to be driven directly by a CMOS device. Output clamp diodes are provided for protection when driving inductive loads. An on-chip protection circuit guarantees glitch-free operation during power up or down, and a fail safe feature is provided which puts the output in high impedance state when the input is open.

Applications

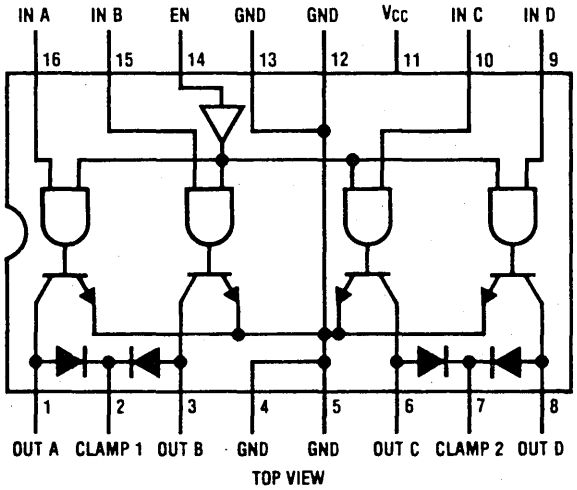
- Relay drivers
- Lamp drivers
- Solenoid drivers
- Hammer drivers
- Stepping motor drivers
- Triac drivers
- LED drivers
- High current, high voltage drivers
- Level translators
- Fiber optic LED drivers

Features

- Single saturated transistor outputs
- Low standby power, 10 mW typical
- High impedance TTL compatible inputs
- Outputs may be tied together for increased current capacity
- High output current
  - 600 mA per output
  - 2.4A per package
- No output latch-up at 35V
- Low output ON voltage (350 mV typ @ 600 mA)
- High breakdown voltage (70V)
- Open collector outputs
- Output clamp diodes for inductive fly back protection
- NPN inputs for minimal input currents (1 μA typical)
- Low operating power
- Standard 5V power supply
- Power up/down protection
- Fail safe operation
- 2W power package
- Pin-for-pin compatible with SN75437

Connection Diagram

Dual-In-Line Package



TOP VIEW

Truth Table

IN	EN	OUT
H	H	L
L	H	Z
H	L	Z
L	L	Z

H = High state
L = Low state
Z = High impedance state

National Semiconductor

PRELIMINARY
August 1982

DS3695/DS3696/DS3697/DS3698 Differential TRI-STATE® Bus/Line Transceivers/Repeaters

General Description

The DS3695, DS3696, DS3697 and DS3698 are high speed differential TRI-STATE bus/line transceivers/repeaters designed to meet the requirements of proposed new EIA standard RS485 with extended common mode range (+12V to −7V), for multipoint data transmission.

The driver and receiver outputs feature TRI-STATE capability, for the driver outputs over the entire common mode range of +12V to −7V. Bus contention or fault situations that cause excessive power dissipation within the device are handled by a thermal shutdown circuit, which forces the driver outputs into the high impedance state. The DS3696 and DS3698 provide an output pin which reports the occurrence of a line fault causing thermal shutdown of the device. This is an "open collector" pin with an internal 10kΩ pull-up resistor. This allows the line fault outputs of several devices to be wire OR-ed.

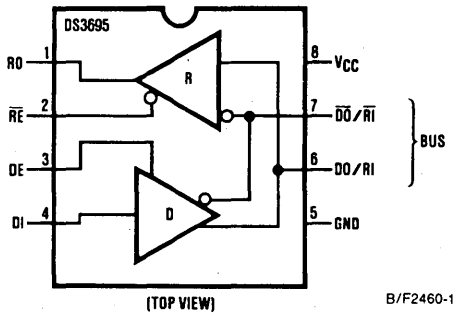
Both AC and DC specifications are guaranteed over the 0 to 70°C temperature and 4.75V to 5.25V supply voltage range.

*TRI-STATE is a registered trademark of National Semiconductor Corp.

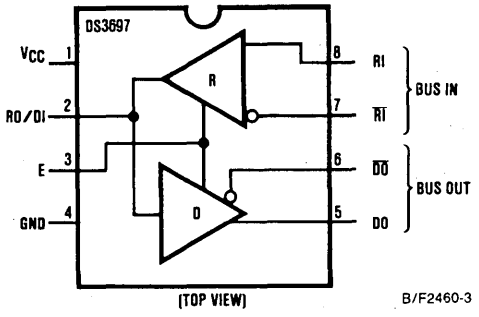
Features

- Meets new EIA standard RS485, for multipoint bus transmission.
- 15ns driver propagation delays with 2ns skew (typical).
- Single channel per package isolates faulty channels (from shutting down good channels).
- Single +5V supply.
- −7V to +12V bus common mode range permits ±7V ground difference between devices on the bus.
- Thermal shutdown protection.
- Power-up down glitch-free driver outputs permit live insertion or removal of transceivers.
- High impedance to bus with driver in TRI-STATE or with power off, over the entire common mode range allows the unused devices on the bus to be powered down.
- Line fault reporting capability on DS3696 and DS3698 allows automated fault location and re-routing under processor control.
- 12kΩ Minimum receiver input impedance.
- 70mV typical receiver hysteresis.

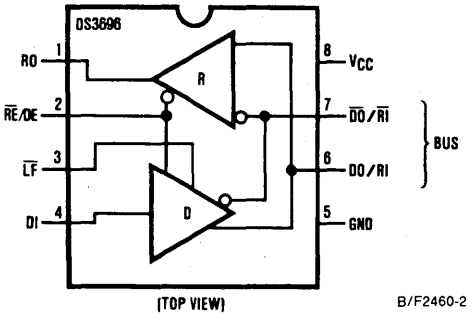
Connection and Logic Diagrams



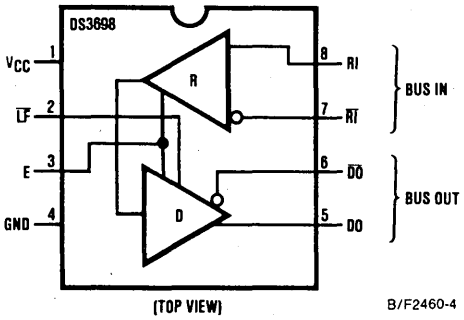
B/F2460-1



B/F2460-3



B/F2460-2



B/F2460-4

National Semiconductor

February 1982
PRELIMINARY

DS8614, DS8615, DS8616, DS8617 225 MHz Low Power Dual Modulus Prescalers

General Description

The DS8614 series products are low power dual modulus prescalers which divide by 20/21, 32/33, 40/41, and 64/65, respectively. The modulus control (MC) input selects division by N when at a high TTL level and division by N + 1 when at a low TTL level. The clock inputs are buffered, providing 40 mVrms input sensitivity. The two outputs provide the user the option to wire either a totem-pole or open-collector output structure. Additionally, the user can wire a resistor between the two output pins to minimize edge transition emissions. The outputs are designed to drive positive edge triggered PLLs. These products can be operated from either an unregulated 6.8V to 13.5V source or regulated 5V ± 10% source. Unregulated operation is obtained by connecting V_S to the source and V_{REG} to a 0.1 μF capacitor to ground. Regulated operation is obtained by connecting both V_S and V_{REG} to the supply source.

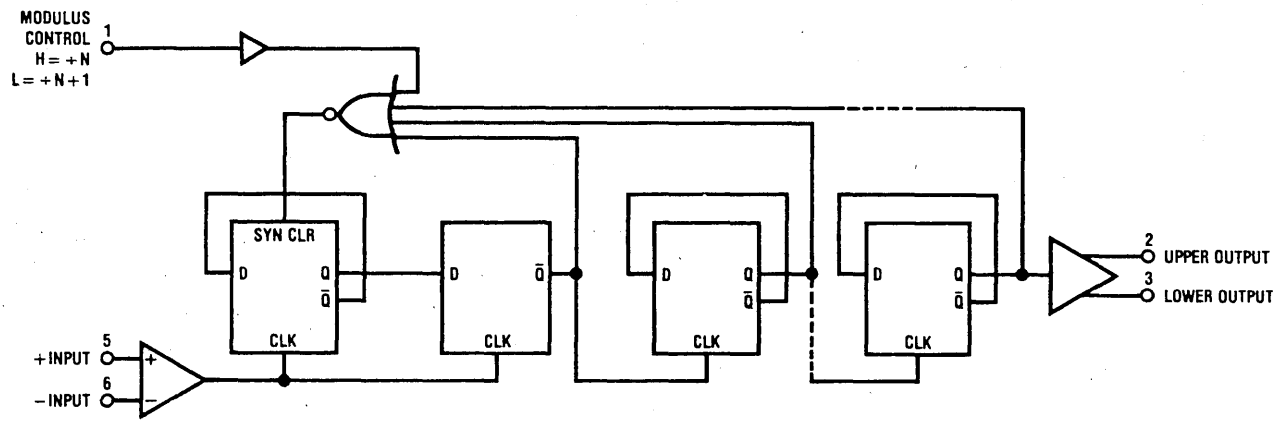
The device can be used in phase-locked loop applications such as FM radio or other communications bands to prescale the input frequency down to a more usable level. A digital frequency display system can also be derived separately or in conjunction with a phase-locked loop, and it can extend the useful range of many inexpensive frequency counters to 225 MHz.

Features

- Low power, 7 mA max
- 225 MHz toggle frequency
- 40 mVrms input sensitivity
- Pin compatible with Motorola MC12015-17 prescalers
- Unregulated/regulated power supply option

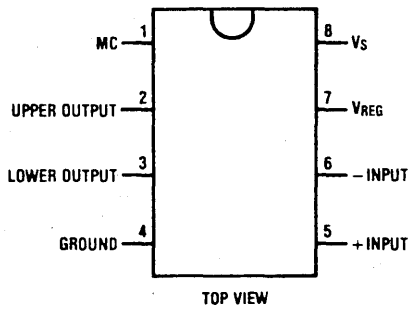
Logic Diagram

Generalized ÷ N/N + 1



Connection Diagram

Dual-In-Line Package



TOP VIEW

TRANSCEIVERS 54/74LS641, LS642, 74LS641-1, LS642-1

Octal Bus Transceiver (Open Collector)

- Octal bidirectional bus interface
- Open Collector Outputs
  - — 'LS641, non-inverting
  - — 'LS642, inverting
- PNP inputs for reduced loading
- Hysteresis on all Data inputs
- 48mA sink capability ('LS641-1, LS642-1)

TYPE	TYPICAL PROPAGATION DELAY (A to B)	TYPICAL SUPPLY CURRENT (Total)
74LS641 & -1	17ns	58mA
74LS642 & -1	17ns	58mA

FUNCTION TABLE, 'LS641

INPUTS		INPUTS/OUTPUTS	
$\overline{CE}$	S/$\overline{R}$	A_n	B_n
L	L	A = B	INPUTS
L	H	INPUTS	B = A
H	X	(Z)	(Z)

FUNCTION TABLE, 'LS642

INPUTS		INPUTS/OUTPUTS	
$\overline{CE}$	S/$\overline{R}$	A_n	B_n
L	L	A = $\overline{B}$	INPUTS
L	H	INPUTS	B = $\overline{A}$
H	X	(Z)	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance "off" state

ORDERING CODE

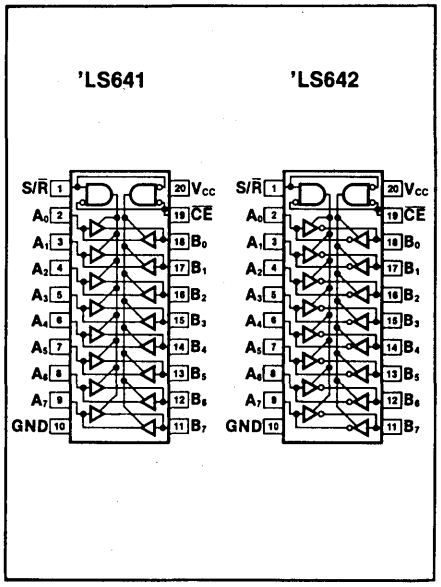
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS641N N74LS641-1N N74LS642N N74LS642-1N	
Ceramic DIP	N74LS641F N74LS641-1F N74LS642F N74LS642-1F	S54LS641F S54LS642F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

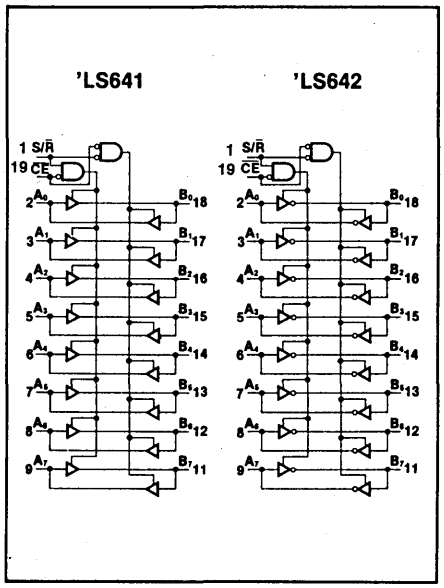
PINS	DESCRIPTION	54/74LS & -1
All	Inputs	1LSul
All	Outputs	30LSul

NOTE
A 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

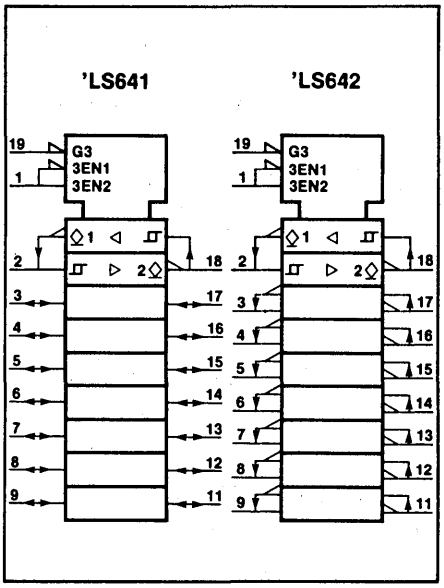
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS & -1	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

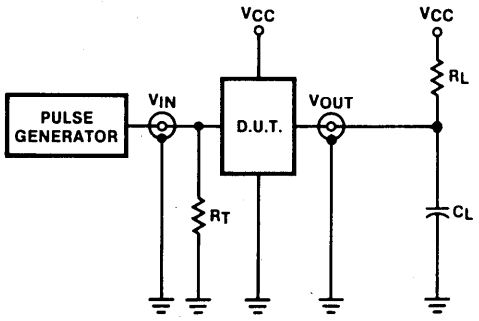
NOTE
V_{IN} limited to 5.5V on A and B inputs only.

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS & -1			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.5	V
		Com'l			+0.6	V
I_{IK}	Input clamp current				−18	mA
V_{OH}	HIGH-level output voltage				5.5	V
I_{OL}	LOW-level output current	Mil			12	mA
		Com'l			24	mA
		74LS-1 only			48	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

TEST CIRCUITS AND WAVEFORMS

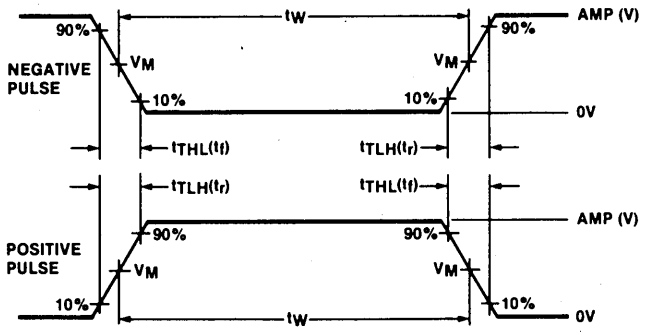
TEST CIRCUIT FOR 54/74 OPEN COLLECTOR OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

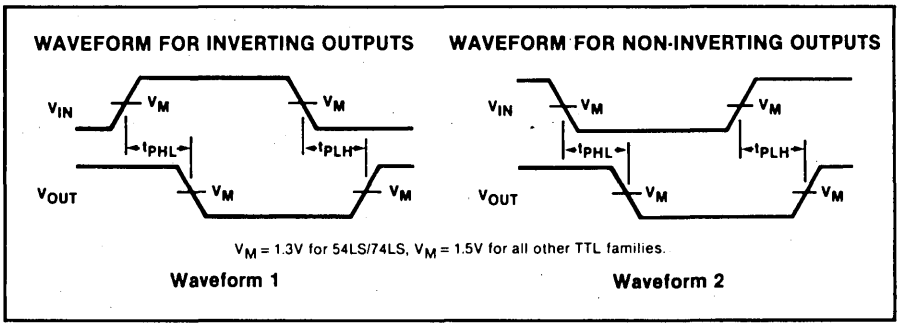
TRANSCEIVERS 54/74LS641, LS642, 74LS641-1, LS642-1

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature unless range otherwise noted)

PARAMETER		TEST CONDITIONS[1]			54/74LS641 54/74LS642			74LS641-1 74LS642-1			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
ΔV_T	Hysteresis (V_{T+}-T_{T-})	V_{CC} = MIN, A or B input		Mil	0.1	0.4					V
				Com'l	0.2	0.4		0.2	0.4		V
I_{OH}	HIGH-level output current	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, V_{OH} = 5.5V					100			100	μA
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = 12mA	Mil		0.25	0.4				V
				Com'l		0.25	0.4		0.25	0.4	V
			I_{OL} = 24mA	74LS		0.35	0.5		0.35	0.5	V
			I_{OL} = 48mA						0.4	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					-1.5			-1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V	A or B input			0.1			0.1	mA
			V_I = 7.0V	S/$\overline{R}$ or $\overline{CE}$ input			0.1			0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20			20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					-0.4			-0.4	mA
I_{CC}	Supply current[3] (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH		48	70		48	70	mA
			I_{CCL}	Outputs LOW		62	90		62	90	mA
			I_{CCZ}	Outputs OFF		64	95		64	95	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C
3. Measure I_{CC} with outputs open.

AC WAVEFORMS



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74LS641 & -1 C_L = 45pF, R_L = 667Ω		54/74LS642 & -1 C_L = 45pF, R_L = 667Ω		UNIT
			Min	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 2, 'LS641		25		25	ns
t_{PHL}	A input to B output	Waveform 1, 'LS642		25		25	
t_{PLH}	Propagation delay	Waveform 2, 'LS641		25		25	ns
t_{PHL}	B input to A output	Waveform 1, 'LS642		25		25	
t_{PLH}	Propagation delay						
	$\overline{CE}$, S/$\overline{R}$ inputs to A output	Waveform 1		40		40	
	$\overline{CE}$ input to B output	Waveform 1		40		40	ns
	S/$\overline{R}$ input to B output	Waveform 2		40		40	
t_{PHL}	Propagation delay						
	$\overline{CE}$, S/$\overline{R}$ inputs to A output	Waveform 2		50		60	
	$\overline{CE}$ input to B output	Waveform 2		50		60	ns
	S/$\overline{R}$ input to B output	Waveform 1		50		60	

Octal Buffer/Line Driver (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS540	9ns	22mA
74LS541	10ns	23mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS540N • N74LS541N	
Ceramic DIP	N74LS540F • N74LS541F	S54LS540F • S54LS541F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

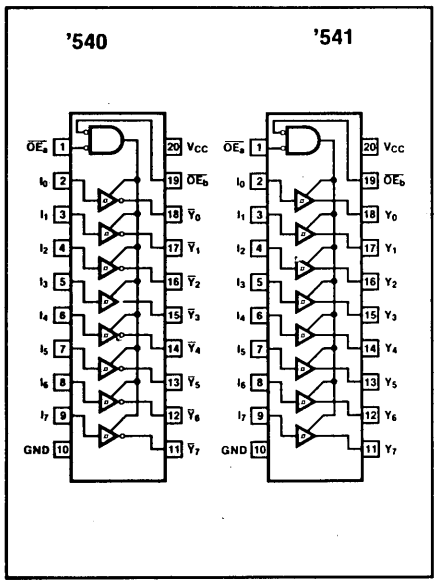
PINS	DESCRIPTION	54/74LS
All	Inputs	1LSul
All	Outputs	30LSul

NOTE
A 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

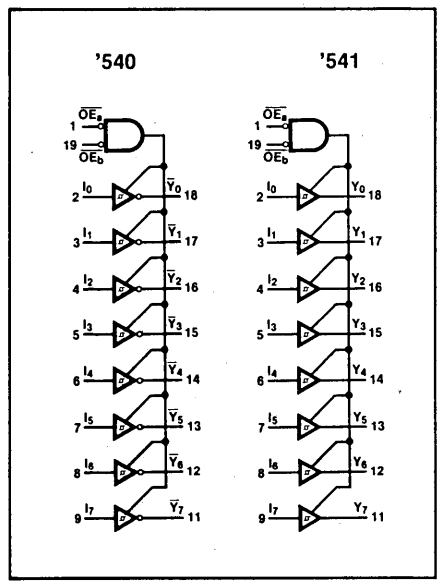
FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{OE}_1$	$\overline{OE}_2$	I	Y	$\overline{Y}$
L	L	L	L	H
L	L	H	H	L
X	H	X	(Z)	(Z)
H	X	X	(Z)	(Z)

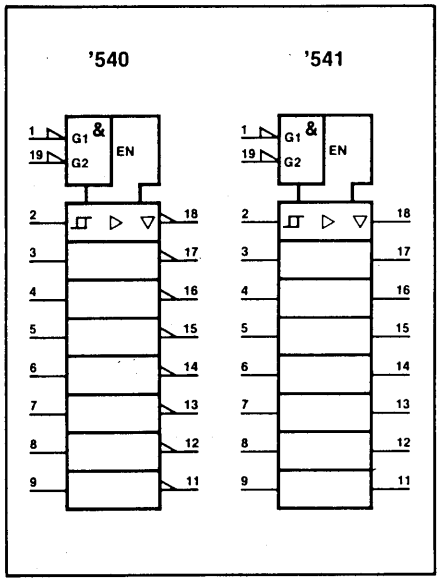
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Signetics

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

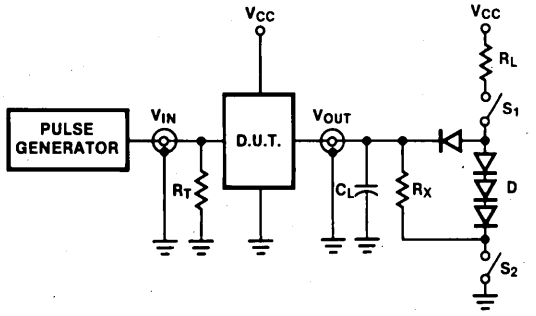
PARAMETER		54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	Mil			−12	mA
		Com'l			−15	mA
I_{OL}	LOW-level output current	Mil			12	mA
		Com'l			24	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



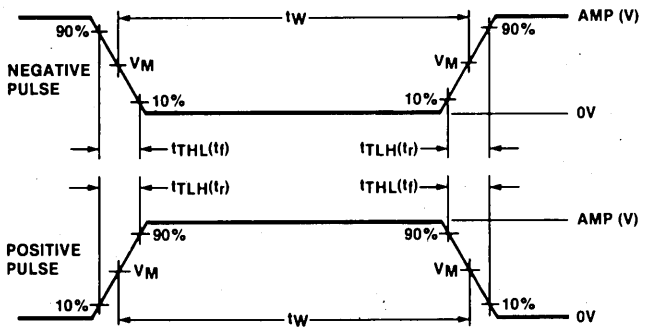
SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS540, 541			UNIT
					Min	Typ[2]	Max	
ΔV_T	Hysteresis ($V_{T+}-V_{T-}$)	V_{CC} = MIN			0.2	0.4		V
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = 0.5V, I_{OH} = MAX			2.0			V
		V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = −3mA			2.4	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4	V
				Com'l		0.35	0.5	V
			I_{OL} = 12mA	74LS		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					−1.5	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_H = MIN, V_{IL} = MAX, V_O = 2.7V					20	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{IL} = MAX, V_O = 0.4V					−20	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					−0.2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−40		−130	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH		16	25	mA
			I_{CCL}	Outputs LOW		27	45	mA
			I_{CCZ}	Outputs OFF		31	52	mA

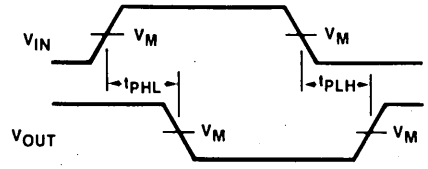
NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74LS540		54/74LS541		UNIT
			C_L = 45pF, R_L = 667Ω		C_L = 45pF, R_L = 667Ω		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveforms 1 & 2		15 15		15 18	ns
t_{PZH}	Output enable time to HIGH level	Waveform 3		25		32	ns
t_{PZL}	Output enable time to LOW level	Waveform 4		38		38	ns
t_{PHZ}	Output disable time from HIGH level	Waveform 3, C_L = 5pF		18		18	ns
t_{PLZ}	Output disable time from LOW level	Waveform 4, C_L = 5pF		25		29	ns

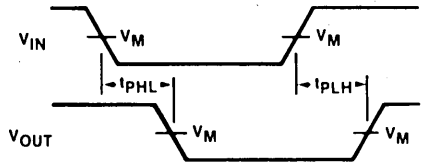
AC WAVEFORMS

WAVEFORM FOR INVERTING OUTPUTS



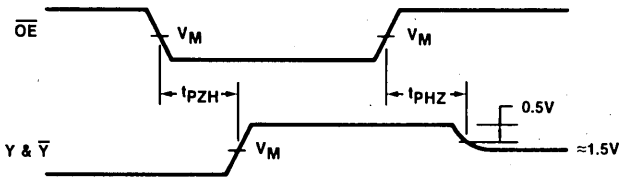
Waveform 1

WAVEFORM FOR NON-INVERTING OUTPUTS



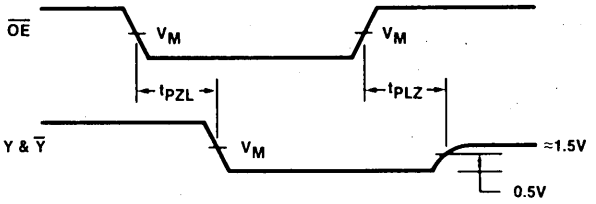
Waveform 2

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 3

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 4

V_M = 1.5V for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS.

Analog Switches

Basic Part No. (Note 1)	Switch Type	Analog Voltage Range (V) (Note 4)	$r_{DS(on)}$ Max (Ω) (Note 4)	$I_{D(off)}$ (nA)	Switching Time (μsec) t_{ON}	t_{OFF}	Logic Levels (V) V_{INL}	V_{INH}	Opt. Supply Voltage (V) (+) Sup. V+	(−) Sup. V−	Logic Sup. V_L	Ref. Sup. V_R	Comments	Switch Configuration
SINGLE CHANNEL SPST														
DG5040	Plus 40 CMOS	+15 to −15	50	1	1.0	0.5	0.8	2	15	−15	5	—	TTL Compatible	1 SPST Switch per Package
TWO CHANNEL SPST														
DG180	N-JFET	+10 to −12.5	10	10	0.3	0.25	0.8	2.0	10	−20	5	0	Break-Before-Make	
		+10 to −7.5	10	10	0.3	0.26	0.8	2.0	15	−15	5	0	15 V Supplies	
DG181	N-JFET	+10 to −12.5	30	1	0.15	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make	
		+10 to −7.5	30	1	0.15	0.13	0.8	2.0	15	−15	5	0	15 V Supplies JAN/11101	
DG182	N-JFET	+10 to −15	75	1	0.25	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make	
		+10 to −10	75	1	0.25	0.13	0.8	2.0	15	−15	5	0	15 V Supplies JAN/11102	**2 SPST Switches per Package**
DG200	CMOS	+15 to −15	70	2	1.0	0.5	0.8	2.4	15	−15	—	(Note 3)	JAN/12303	
DG200A	Plus 40 CMOS	+15 to −15	70	2	1.0	0.5	0.8	2.4	15	−15	—	—	TTL In	
DG281	N-JFET	+15 to −15	300	0.2	0.15	0.13	0.8	2.0	15	−15	5	0	Low Charge Injection	
DG300	CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	—	—	Low Power, TTL In JAN/11601	
DG300A	Plus 40 CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	—	—	Low Power, TTL In	
DG304	CMOS	+15 to −15	50	1	0.25	0.15	3.5	11.0	15	−15	—	—	Low Power, CMOS In JAN/11605	
DG304A	Plus 40 CMOS	+15 to −15	50	1	0.25	0.15	3.5	11.0	15	−15	—	—	Low Power, CMOS In	
DG381	CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	—	—	Low Power, DG181 Pin Out	
DG381A	Plus 40 CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	—	—	Low Power, DG181 Pin Out	
DG5041	Plus 40 CMOS	+15 to −15	50	1	1.0	0.5	0.8	2.0	15	−15	5	—	TTL Compatible	
FOUR CHANNEL SPST														
DG201	CMOS	+15 to −15	175	1	1.0	0.5	0.8	2.4	15	−15	—	(Note 3)	JAN/12304	**4 SPST Switches per Package**
DG201A	Plus 40 CMOS	+15 to −15	175	1	1.0	0.5	0.8	2.4	15	−15	—	—	TTL In	
DG202	Plus 40 CMOS	+15 to −15	175	1	1.0	0.5	0.8	2.4	15	−15	—	—	TTL In	
DG211	Plus 40 CMOS	+15 to −15	175	5	0.5	0.4	0.8	2.4	15	−15	5	—	Low Cost, TTL In	
DG212	Plus 40 CMOS	+15 to −15	175	5	0.6	0.45	0.8	2.4	15	−15	5	—	Low Cost, TTL In	
DG308A	Plus 40 CMOS	+15 to −15	100	1	0.2	0.15	3.5	11.0	15	−15	—	—	Low Cost CMOS In	
DG309	Plus 40 CMOS	+15 to −15	100	5	0.2	0.15	3.5	11.0	15	−15	—	—	Low Cost CMOS In	
ONE CHANNEL SPDT														
DG186	N-JFET	+10 to −12.5	10	10	0.3	0.25	0.8	2.0	10	−20	5	0	Break-Before-Make	
	N-JFET	+15 to −7.5	10	10	0.3	0.25	0.8	2.0	15	−15	5	0	15 V Supplies	
DG187	N-JFET	+10 to −12.5	30	1	0.15	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make	
	N-JFET	+15 to −7.5	30	1	0.15	0.13	0.8	2.0	15	−15	5	0	15 V Supplies JAN/11105	
DG188	N-JFET	+10 to −15	75	1	0.25	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make	**1 SPST Switch per Package**
	N-JFET	+15 to −10	75	1	0.25	0.13	0.8	2.0	15	−15	5	0	15 V Supplies JAN/11106	
DG287	N-JFET	+15 to −7.5	300	0.2	0.15	0.13	0.8	2.0	15	−15	5	0	Break-Before-Make	
DG301	CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	—	—	Low Power, TTL In JAN/11602	
DG301A	Plus 40 CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	—	—	Low Power, TTL In	
DG305	CMOS	+15 to −15	50	1	0.25	0.15	3.5	11.0	15	−15	—	—	Low Power, CMOS In JAN/11605	
DG305A	Plus 40 CMOS	+15 to −15	50	1	0.25	0.15	3.5	11.0	15	−15	—	—	Low Power, CMOS In	
DG387	CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	—	—	Low Power, DG187 Pin Out	
DG387A	Plus 40 CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	—	—	Low Power, DG187 Pin Out	
DG5042	Plus 40 CMOS	+15 to −15	50	1	1.0	0.5	0.8	4.0	15	−15	5	—	TTL Compatible	

NOTES:

1. The devices shown in **boldface** are recommended parts for new designs.
2. The appropriate switching characteristic for multiplexers is $t_{TRANSITION}$, not t_{ON}, t_{OFF}.
3. $V_{REF} = 1.5$ V is used when supply voltages < ± 15 V are used. Not needed when supply voltages of ± 15 are used.
4. Analog voltage range is a function of supply voltages. Where a FET switch is PMOS or CMOS, r_{DS} is also a function of Supply Voltage and Analog Voltage. See individual data sheets for more detail. Values shown are for temperature suffix A.
5. Device normally operates with resistor to + 10 V.

Analog Switches (Cont'd)

Basic Part No. (Note 1)	Switch Type	Analog Voltage Range (V) (Note 4)	$r_{DS(on)}$ Max (Ω) (Note 4)	$I_{D(off)}$ (nA)	Switching Time (μsec) t_{ON}	t_{OFF}	Logic Levels (V) V_{INL}	V_{INH}	Opt. Supply Voltage (V) (+) Sup. V+	(−) Sup. V−	Logic Sup. V_L	Ref. Sup. V_R	Comments	Switch Configuration
TWO CHANNEL SPDT														
DG189	N-JFET	+10 to −12.5	10	10	0.3	0.25	0.8	2.0	10	−20	5	0	Break-Before-Make	
	N-JFET	+15 to −7.5	10	10	0.3	0.25	0.8	2.0	15	−15	5	0	15 V Supplies	
DG190	N-JFET	+10 to −12.5	30	1	0.15	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make JAN/11107	
	N-JFET	+15 to −7.5	30	1	0.15	0.13	0.8	2.0	15	−15	5	0	15 V Supplies	
DG191	N-JFET	+10 to −15	75	1	0.25	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make JAN/11108	**2 SPDT Switches per Package**
	N-JFET	+15 to −10	75	1	0.25	0.13	0.8	2.0	15	−15	5	0	15 V Supplies	
DG243	Plus 40 CMOS	+15 to −15	50	1	0.5	1.0	0.8	2.0	15	−15	5	–	Make-Before-Break (DG191 Pin Out)	
DG290	N-JFET	+15 to −7.5	300	0.2	0.15	0.13	0.8	2.0	15	−15	5	0	Break-Before-Make	
DG303	CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	–	–	Low Power, TTL In JAN/11604	
DG303A	Plus 40 CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	–	–	Low Power, TTL In	
DG307	CMOS	+15 to −15	50	1	0.25	0.15	3.5	11.0	15	−15	–	–	Low Power, CMOS In JAN/11608	
DG307A	Plus 40 CMOS	+15 to −15	50	1	0.25	0.15	3.5	11.0	15	−15	–	–	Low Power, CMOS In	
DG390	CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	–	–	Low Power, DG190 Pin Out	
DG390A	Plus 40 CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	–	–	Low Power, DG190 Pin Out	
DG5043	Plus 40 CMOS	+15 to −15	50	1	1.0	0.5	0.8	2.0	15	−15	5	–		
ONE CHANNEL DPST														
DG5044	Plus 40 CMOS	+15 to −15	50	1	1.0	0.5	0.8	2	15	−15	5	–	TTL Compatible	1 DPST Switch per Package
TWO CHANNEL DPST														
DG183	N-JFET	+10 to −12.5	10	10	0.3	0.25	0.8	2.0	10	−20	5	0	Break-Before-Make	
	N-JFET	+15 to −7.5	10	10	0.3	0.25	0.8	2.0	15	−15	5	0	15 V Supplies	
DG184	N-JFET	+10 to −12.5	30	1	0.15	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make	
	N-JFET	+15 to −7.5	30	1	0.15	0.13	0.8	2.0	15	−15	5	0	15 V Supplies	
DG185	N-JFET	+10 to −15	75	1	0.25	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make	**2 DPST Switches per Package**
	N-JFET	+15 to −10	75	1	0.25	0.13	0.8	2.0	15	−15	5	0	15 V Supplies	
DG284	N-JFET	+15 to −7.5	300	0.2	0.15	0.13	0.8	2.0	15	−15	5	0	Break-Before-Make	
DG302	CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	–	–	Low Power, TTL In	
DG302A	Plus 40 CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	–	–	Low Power, TTL In	
DG306	CMOS	+15 to −15	50	1	0.25	0.15	3.5	11.0	15	−15	–	–	Low Power, CMOS In	
DG306A	Plus 40 CMOS	+15 to −15	50	1	0.25	0.15	3.5	11.0	15	−15	–	–	Low Power, CMOS In	
DG384	CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	–	–	Low Power, DG184 Pin Out	
DG384A	Plus 40 CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	–	–	Low Power, DG184 Pin Out	
DG5045	Plus 40 CMOS	+15 to −15	50	1	1.0	0.5	0.8	2.0	15	−15	5	–		

NOTES:

1. The devices shown in **boldface** are recommended parts for new designs.
2. The appropriate switching characteristic for multiplexers is $t_{TRANSITION}$, not t_{ON}, t_{OFF}.
3. V_{REF} = 1.5 V is used when supply voltages < ±15 V are used. Not needed when supply voltages of ±15 are used.
4. Analog voltage range is a function of supply voltages. Where a FET switch is PMOS or CMOS, r_{DS} is also a function of Supply Voltage and Analog Voltage: See individual data sheets for more detail. Values shown are for temperature suffix A.
5. Device normally operates with resistor to +10 V.

Analog Switches Selector Guide

Application	Feature of Application	Important Parameters	Major Tradeoffs	Suggested Switches
Battery Operated or Battery Back-Up Supply	1) Low Power	Low Supply Current		**CMOS DG304-DG308, DG304A, DG307A, DG309** DG300-DG303, DG381-DG390, DG300A-DG303A, DG381A-DG390A
	2) Minimum Number of Power Supplies	Only One or Two Supplies Needed		**CMOS DG300-DG308A, DG300A-DG307A, DG309** (Can Also Be Used As Single Supply) CMOS DG200, DG201, DG211, DG200A, DG201A, DG202, DG212 (For MUX: DG506-DG509, DG506A-DG509A, DG528, DG529)
	3) Low Standby Power	Low Standby Current		**CMOS DG304-DG308A, DG211, DG304A-DG307A, DG309, DG212**
Audio	1) Low Signal Distortion	Low $r_{DS(on)}$; Constant $r_{DS(on)}$	JFET is Constant, $r_{DS(on)}$; Signal Range Limited Toward Negative Supply; CMOS Slight $r_{DS(on)}$ Variation, Full Signal Range	**JFET DG180-DG191** CMOS DG300-DG308A, DG381-DG390, DG300A-DG307A, DG309, DG381A-DG390A, DG5040-DG5045 DG243 (Make-Before-Break)
	2) Low Noise (Channel)	Low $r_{DS(on)}$		CMOS DG300-DG308A, DG381-DG390, DG300A-DG307A, DG309, DG381A-DG390A, DG5040-DG5045, DG243 JFET DG180-DG191
	3) Wide Signal Range	±15V Signal Range		**CMOS DG300-DG308, DG381-DG390, DG300A-DG307A, DG309, DG381A-DG390A, DG5040-DG5045, DG243** CMOS DG200, DG200A, DG201, DG201A, DG202, DG211, DG212 (MUX: DG506-DG509, DG506A-DG509A, DG528, DG529)
		Signal Range is From the Positive Supply to Above the Negative Supply	Higher $r_{DS(on)}$ (Must Stay Above Negative Supply By 5V to 7.5V)	**JFET (75Ω) DG182, DG185, DG188, DG191** (10Ω, 30Ω) Remainder of DG181-DG190 Family
	4) Large Dynamic Range	Wide Signal Range and Low Thermocouple Noise		**CMOS DG304-DG308A, DG304A-DG307A, DG309** DG300-DG303, DG381-DG390, DG211, DG300A-DG303A, DG381A-DG390A, DG212
Video (High Frequency)	1) High OFF Impedance, Small Feedthrough of Signal	High OFF Isolation	Higher $r_{DS(on)}$	**JFET (30Ω, 75Ω) DG181, DG182, DG184, DG185, DG187, DG188, DG190, DG191** CMOS DG200, DG201, DG211, DG200A, DG201A, DG202, DG212 CMOS DG300-DG308A, DG381-DG390, DG300A-DG307A, DG309, DG381A-DG390A, DG5040-DG5045, DG243
	2) Good Impedance Matching, Minimum Signal Drop Across Switch	Low $r_{DS(on)}$	Lower OFF Isolation	**JFET (10Ω) DG180, DG183, DG186, DG189** (30Ω) DG181, DG184, DG187, DG190 CMOS DG300-DG308A, DG211 DG300A-DG307A, DG309, DG212

Bold Print = Recommended for the application

Analog Switches Selector Guide (Cont'd)

Application	Feature of Application	Important Parameters	Major Tradeoffs	Suggested Switches
Sample and Hold	1) Low Droop Rate	Low Leakage	Higher ON Resistance	**CMOS DG300A-DG307A, DG300, DG309 DG381A-DG390A** **CMOS DG300-DG308A, DG381-DG390, DG5040-DG5045** JFET DG180-DG191 CMOS DG200, DG201, DG211, DG200A, DG201A, DG202, DG212
	2) Low Sample to Hold Offset	Low Charge Coupling	Higher ON Resistance	**CMOS DG200A, DG201A, DG202, DG212** **CMOS DG200, DG201, DG211** JFET DG181, DG182 (30Ω, 75Ω) DG184, DG185, DG187, DG188, DG190, DG191 CMOS DG300-DG308A, DG300A-DG307A, DG309
	3) Fast Acquisition Speed	Low ON Resistance	Higher Leakage Higher Charge Coupling	**JFET (10Ω) DG180, DG183, DG186, DG189** (30Ω, 75Ω) Remainder of DG181-DG191 Family CMOS DG300-DG307, DG381-DG390, DG300A-DG307A CMOS DG200, DG201, DG211, DG212 CMOS DG381A-DG390A, DG200A, DG201A, DG202
Switching to High Impedance Inputs	1) Low Error Voltage	Low Leakage		**CMOS DG300A-DG307A, DG381A-DG390A** **CMOS DG300-DG307, DG381-DG390, DG5040-DG5045, DG200-DG201, DG211, DG200A, DG201A, DG212**
	2) Low Switching Transient Error Voltage	Low Charge Coupling		**CMOS DG200A, DG201A, DG202, DG212** **CMOS DG200, DG201, DG211** DG300-DG307, DG381-DG390, DG300A-DG307A, DG381A-DG390A
Low Cost	1) Best Performance for Lowest Cost	Monolithic Good Switch Performance		**CMOS DG211, DG212, DG303, DG309, DG308A, DG300-DG307, DG5040-DG5045** DG200, DG201, DG381-DG390, DG200A, DG201A, DG202, DG300A-DG307A, DG243, DG381A-DG390A
Military System	1) Hi-Rel Specified			**BS9000** **JM38510/XXXXX**
Differential Signal Switching	1) Good Matching of Switch Parameters	Monolithic Switch		**CMOS DG300, DG302, DG303, DG304, DG243, DG306, DG307, DG308A, DG381, DG384, DG390, DG309** CMOS DG200, DG201, DG211, DG5040-DG5045, DG300A, DG302A, DG303A, DG304A, DG306A, DG307A, DG309, DG381A, DG384A, DG390A, DG200A, DG207A, DG202, DG212
	2) Low Thermo-couple Offset Voltage	Drain and Source of FET Switch in Close Proximity on *Small Chip*	JFET Switches Not Monolithic	**JFET DG183, DG184, DG185**
		Low Power Dissipation on Switch Driver		**CMOS DG304, DG306, DG307, DG308A DG304A, DG309** DG300-DG303, DG300A-DG303A, DG306A, DG307A, DG381-DG390, DG381A-DG390A, DG309

Bold Print = Recommended for the application

Analog Switches Selector Guide (Cont'd)

Application	Feature of Application	Important Parameters	Major Tradeoffs	Suggested Switches
Small Signal (<1V)	1) Low Noise (Channel)	Low $r_{DS(on)}$	Higher Leakages	**JFET (10Ω) DG180, DG183, DG186, DG189** (30Ω, 75Ω) Remainder of DG181-DG191 Family
	2) Low Charge Coupling			**CMOS DG300A-DG307A, DG309, DG381A-DG390A, DG212, DG308A** CMOS DG300-DG308, DG381-DG390, DG211
	3) High Impedance Inputs of Load	Low Leakage	Higher $r_{DS(on)}$	**CMOS DG300-DG308A, DG381-DG390, DG211, DG5040-DG5045, DG243, DG309** DG200-DG201 JFET DG181, DG182, DG184, DG185, DG187, DG188, DG190, DG191 CMOS DG300A-DG307A, DG309, DG381A-DG390A, DG212
	4) Low Thermo-couple Offset Voltage	Low Power Switch		**CMOS DG304-DG307, DG304A-DG307A, DG381A-DG390A** DG300-DG303, DG381-DG390, DG300A-DG303A
		Drain and Source of FET Switch in Close Proximity on *Small Chip*		**JFET DG180-DG190 Family**
Multiplexing	1) Break-Before-Make Switching	t_{on} is Greater Than t_{off}		**CMOS DG506, DG506A, DG507, DG507A, DG508, DG508A, DG509, DG509A, DG528, DG529 (Latchable)**
	2) Binary Controlled Logic Inputs	Binary Decoding Stage on Chip		PMOS DG501, DG503
	3) Differential Multi-plexing	Dual Switching Action		CMOS DG507, DG509, DG507A, DG509A, DG529
	4) D/A Conversion	Binary Weighted ON Resistance and Channel Resistance to Minimize Error		NMOS DG515, DG516

Bold Print = Recommended for the application

DG200A

Dual Monolithic SPST CMOS Analog Switch

Siliconix

designed for . . .

- **Analog Multiplexing**
- **Servo Control Switching**
- **Video Signal Switching**
- **Remove Switching under TTL Logic Control**

BENEFITS

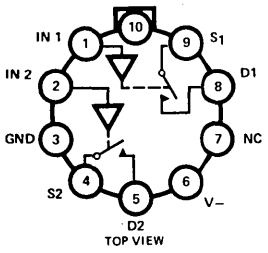
- **Environmentally Rugged**
  - 44V Power Supply Maximum Rating
  - Static Protected Logic Inputs
  - Latchproof
- **Easily Interfaced**
  - TTL and CMOS Compatible without Pull-Up Resistors
- **Pin for Pin Compatible with**
  - Analog Devices ADG200
  - Harris HI200
  - Intersil DG200
  - Siliconix DG200

DESCRIPTION

The DG200A designed on the Siliconix PLUS-40 CMOS process provides solid state switch action with 70 ohms contact (ON) resistance and very high OFF resistance. True switch action takes place over the full analog signal range of ±15 V, with Break-Before-Make operation to prevent momentary shorting of signal inputs.

PIN CONFIGURATIONS

Metal Can Package
V+ (SUBSTRATE AND CASE)



TOP VIEW

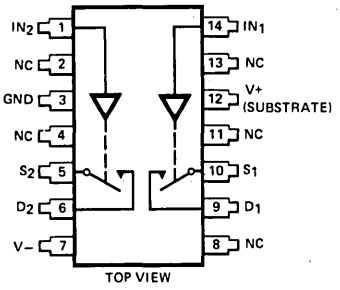
LOGIC	SWITCH
0	ON
1	OFF

ORDER NUMBERS:
DG200AAA OR DG200ABA
SEE PACKAGE 2

ORDER NUMBERS:
DG200AAK OR DG200ABK
OR DG200ACK
SEE PACKAGE 9

DG200ACJ
SEE PACKAGE 7

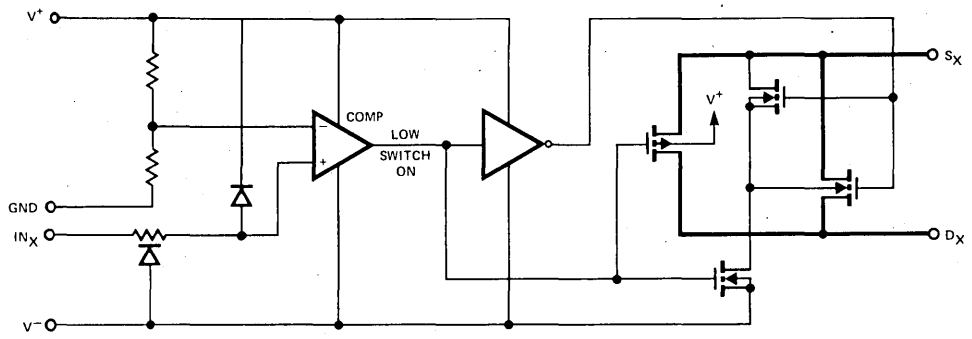
Dual-In-Line Package



TOP VIEW

SWITCH STATES ARE FOR LOGIC "1" INPUT (POSITIVE LOGIC)

SCHEMATIC DIAGRAM (typical channel)



ABSOLUTE MAXIMUM RATINGS

Voltages referenced to V–

V+ . . . . . 44 V
GND . . . . . 25 V
Digital inputs[4], V_S, V_D . . . . . –2 V to (V^+ +2 V) or 20 mA, whichever occurs first.
Current, Any Terminal Except S or D . . . . 30 mA
Current, S or D . . . . . 20 mA
Current, S or D Pulsed
(1 msec, 10% Duty Cycle Max) . . . . . 100 mA
Operating Temp. (A Suffix) . . . . . –55 to 125°C
(B Suffix) . . . . . –20 to 85°C
(C Suffix) . . . . . 0 to 70°C
Storage Temp. (A & B Suffix) . . . . –65 to 150°C
(C Suffix) . . . . . –65 to +125°C
Power Dissipation (Package)*
Metal Can** . . . . . 450 mW
14 Pin DIP*** . . . . . 825 mW
14 Pin Plastic DIP**** . . . . . 470 mW

*Device mounted with all leads welded or soldered to PC board.
**Derate 6 mW/°C above 75°C
***Derate 11 mW/°C above 75°C
****Derate 6.5 mW/°C above 25°C

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		CHARACTERISTIC		TYP[1] 25°C	MAX LIMITS A SUFFIX -55°C	A SUFFIX 25°C	A SUFFIX 125°C	B/C SUFFIX -20/0°C	B/C SUFFIX 25°C	B/C SUFFIX 85/70°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V– = –15 V, Gnd = 0,	
1		V_{ANALOG}	Minimum Analog Signal Handling Capability	±15		±15	±15		±15	±15	V		
2	SWITCH	$r_{DS(on)}$	Drain Source ON Resistance	45	70	70	100	80	80	100	Ω	V_D = 10 V	V_{IN} = 0.8 V, I_S = –1 mA
3				45	70	70	100	80	80	100		V_D = –10 V	
4		$I_{S(off)}$	Source OFF Leakage Current	+0.01		2	100		5	100	nA	V_S = +14 V, V_D = –14 V	V_{IN} = 2.4 V
5				–0.02		–2	–100		–5	–100		V_S = –14 V, V_D = 14 V	
6		$I_{D(off)}$	Drain OFF Leakage Current	+0.01		2	100		5	100		V_D = 14 V, V_S = –14 V	
7				–0.02		–2	–100		–5	–100		V_D = –14 V, V_S = 14 V	
8		$I_{D(on)}$[2]	Channel ON Leakage Current	+0.1		2	200		–5	200		V_D = V_S = 14 V	V_{IN} = 0.8 V
9				–0.1		–2	–200		–5	–200		V_D = V_S = –14 V	
10	INPUT	I_{INH}	Input Current Input Voltage High	0.0009		–1	–10		–1	–10	μA	V_{IN} = 2.4 V	
11				0.005		1	10		1	10		V_{IN} = 15 V	
12		I_{INL}	Input Current Input Voltage Low	–.0015		–1	–10		–1	–10		V_{IN} = 0 V	
13	DYNAMIC	t_{on}	Turn-ON Time	440		1000			1000		ns	See Switching Time Test Circuit	
14		t_{off}	Turn-OFF Time	370		500			500				
15		Q	Charge Injection	–10							pC	C_L = 1000pF, V_{GEN} = 0V, R_{GEN} = 0Ω	
16		$C_{S(off)}$	Source OFF Capacitance	9.0							pF	V_S = 0, V_{IN} = 5 V	f = 140 kHz
17		$C_{D(off)}$	Drain OFF Capacitance	9.0								V_D = 0, V_{IN} = 5V	
18		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance	25								V_D = V_S = 0, V_{IN} = 0	
19		OIRR[3]	OFF Isolation	75								V_{IN} = 5 V	
20		CCRR	Channel to Channel Crosstalk	90								V_S = 2 Vpp	Z_L = 75Ω, f = 1 MHz
21	SUP	I+	Positive Supply Current	0.8		2			2		mA	Both Channels "ON", or "OFF" V_{IN} = 0 or 2.4 V	
22		I–	Negative Supply Current	–.23		–1			–1				

NOTES:
1. Typical Values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
2. $I_{D(on)}$ is leakage from driver into "ON" switch.
3. "OFF" isolation $\triangleq$ 20 log V_S/V_D, V_S = input to OFF switch, V_D = output
4. Signals on S_X, D_X or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

ICME

See Product Selector Guides on Pages 2779-2783.

Quad Monolithic SPST CMOS Analog Switch

Siliconix

designed for . . .

- **Analog Multiplexing**
- **Remote Switching under TTL Logic Control**
- **Servo Control Switching**
- **Sampled Data Systems**
- **Programmable Gain Amplifiers**

BENEFITS

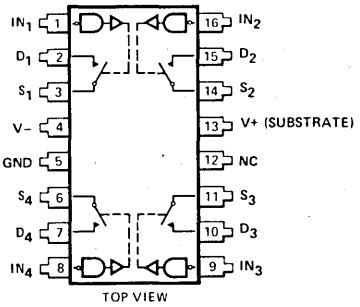
- **Environmentally Rugged**
  - 44V Power Supply Maximum Rating
  - Static Protected Logic Inputs
  - Latchproof
- **Easily Interfaced**
  - TTL and CMOS Compatible without Pull-Up Resistors
  - Logic Inputs Accept ± Comparator Transitions without Series Current Limiting Resistors
- **Pin for Pin Compatible with**
  - Analog Devices ADG201
  - Harris HI201
  - Intersil DG201
  - Siliconix DG201

DESCRIPTION

The DG201A designed on the Siliconix PLUS-40 CMOS process provides solid state switch action with 175 ohms contact resistance and very high OFF resistance. True switch action takes place over the full analog signal range of ±15V, with Break-Before-Make operation to prevent momentary shorting of signal inputs. Charge injection has been reduced by design to minimize spikes during switching transitions.

PIN CONFIGURATION

Dual-In-Line Package



TOP VIEW

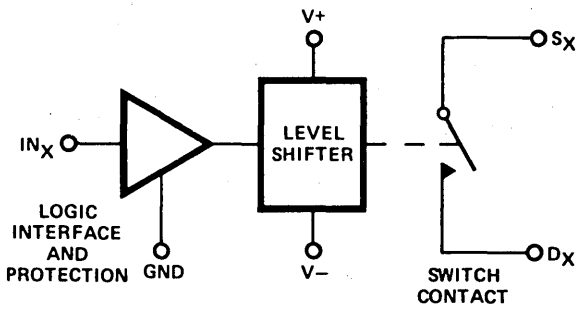
LOGIC	SWITCH
0	ON
1	OFF

ORDER NUMBERS:
DG201AAK, DG201ABK OR DG201ACK
SEE PACKAGE 10

DG201ACJ
SEE PACKAGE 8

SWITCH OPEN FOR LOGIC "1" INPUT (POSITIVE LOGIC)

FUNCTIONAL DIAGRAM (typical channel)



ABSOLUTE MAXIMUM RATINGS

Voltages referenced to V–

V+ . . . . . 44 V
GND . . . . . 25 V
Digital inputs[3] V_S, V_D . . . . . –2 V to (V^+ +2 V) or 20 mA, whichever occurs first.
Current, Any Terminal Except S or D . . . . 30 mA
Continuous Current, S or D . . . . . 20 mA
Peak Current, S or D
(pulsed at 1 msec, 10% duty cycle max) . . 70 mA
Storage Temperature (A & B Suffix) . . –65 to 150°C
(C Suffix) . . . . –65 to 125°C
Operating Temperature (A Suffix) . . . –55 to 125°C
(B Suffix) . . . –20 to 85°C
(C Suffix) . . . 0 to 70°C

Power Dissipation (Package)*
16 Pin DIP** . . . . . 900 mW
16 Pin Plastic DIP*** . . . . . 470 mW

*Device mounted with all leads soldered or welded to PC board.
**Derate 12 mW/°C above 75°C
***Derate 6.5 mW/°C above 25°C

Stresses listed under "Absolute Maximum Ratings" may be applied (one at a time) to devices without resulting in permanent damage. This is a stress rating only and not subject to production testing. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		CHARACTERISTIC		TYP 25°C	MAX LIMITS A SUFFIX –55°C	A SUFFIX 25°C	A SUFFIX 125°C	B/C SUFFIX –20°C/0°C	B/C SUFFIX 25°C	B/C SUFFIX 85°C/70°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V– = –15 V, Gnd = 0	
1		V_{ANALOG}	Minimum Analog Signal Handling Capability	±15		±15	±15		±15	±15	V		
2	SWITCH	$r_{DS(on)}$	Drain Source ON Resistance	105	175	175	250	200	200	250	Ω	V_D = 10 V	V_{IN} = 0.8 V, I_S = –1 mA
3				115	175	175	250	200	200	250		V_D = –10 V	
4		$I_{S(off)}$	Source OFF Leakage Current	0.01		1	100		5	100	nA	V_S =14 V, V_D = – 14 V	V_{IN} = 2.4 V
5				–0.02		–1	–100		–5	–100		V_S = –14 V, V_D = 14 V	
6		$I_{D(off)}$	Drain OFF Leakage Current	0.01		1	100		5	100		V_D = 14 V, V_S = – 14 V	
7				–0.02		–1	–100		–5	–100		V_D = –14 V, V_S = 14 V	
8		$I_{D(on)}$[2]	Drain ON Leakage Current	0.1		1	200		5	200	μA	V_D = V_S = 14 V	V_{IN} = 0.8 V
9				–0.15		–1	–200		–5	–200		V_D = V_S = –14 V	
10	INPUT	I_{INH}	Input Current Input Voltage High	–.0004		–1	–10		–1	–10		V_{IN} = 2.4 V	
11				.003		1	10		1	10		V_{IN} = 15 V	
12		I_{INL}	Input Current Input Voltage Low	–.0004		–1	–10		–1	–10		V_{IN} = 0 V	
13	DYNAMIC	t_{on}	Turn-ON Time	480		1000			1000		ns	See Switching Time Test Circuit	
14		t_{off}	Turn-OFF Time	370		500			500				
15		Q	Charge Injection	20							pC	C_L = 1000pF V_{GEN} = 0V R_{GEN} = 0Ω	
16		$C_{S(off)}$	Source OFF Capacitance	5							pF	V_S = 0, V_{IN} = 5 V	f = 140 kHz
17		$C_{D(off)}$	Drain OFF Capacitance	5								V_D = 0, V_{IN} = 5V	
18		$C_{D(on)}$ + $C_{S(on)}$	Channel ON Capacitance	16								V_D = V_S = 0, V_{IN} = 0	
19		OIRR	OFF Isolation	70							dB	V_{IN} = 5 V	
20		CCRR	Channel to Channel Crosstalk	90								V_S = 2 Vpp, f = 100 KHz Z_L = 75Ω	
21	SUP	I+	Positive Supply Current	.9		2			2		mA	All Channels "ON" or "OFF", V_{IN} = 0 or 2.4 V	
22		I–	Negative Supply Current	–.3		–1			–1				

NOTES:
1. Typical Values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
2. $I_{D(on)}$ is leakage from driver into "ON" switch.
3. Signals on S_X, D_X or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

ICMC-B

See Product Selector Guides on Pages 2779-2783.

Quad Monolithic SPST CMOS Analog Switch

designed for . . .

- **Analog Multiplexing**
- **Remote Switching under TTL Logic Control**
- **Servo Control Switching**
- **Sampled Data Systems**
- **Programmable Gain Amplifiers**

Siliconix

BENEFITS

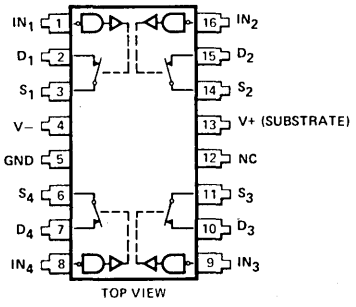
- **Environmentally Rugged**
  - 44 V Power Supply Max Rating
  - Static Protected Logic Inputs
  - Latch Proof
- **Easily Interfaced**
  - TTL and CMOS Compatible Without Pullup Resistors
  - Logic Inputs Accept ± Comparator Transitions Without Series Current Limiting Resistors
- **Pin for Pin Compatible**
  - Intersil IH202
  - National LF11202

DESCRIPTION

The DG202 designed on the Siliconix PLUS-40 CMOS process provides solid state switch action with 175 ohms contact resistance and very high OFF resistance. True switch action takes place over the full analog signal range of ±15 V, with BREAK-BEFORE-MAKE operation to prevent momentary shorting of signals inputs. Charge injection has been reduced by design to minimize spikes during switching transitions.

PIN CONFIGURATION

Dual In-Line Package



TOP VIEW

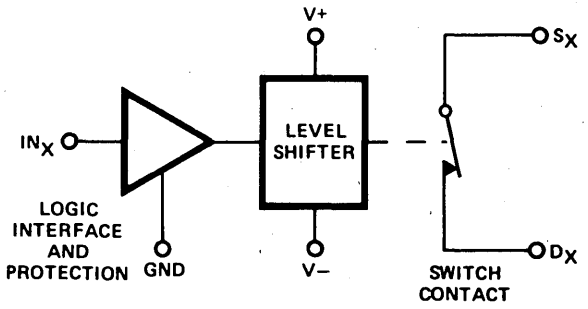
LOGIC	SWITCH
0	OFF
1	ON

ORDER NUMBERS:
DG202AK, DG202BK OR DG202CK
SEE PACKAGE 10

ORDER NUMBER:
DG202CJ
SEE PACKAGE 8

SWITCH CLOSED FOR LOGIC "1" INPUT (POSITIVE LOGIC)

FUNCTIONAL DIAGRAM (typical switch)



ABSOLUTE MAXIMUM RATINGS

Voltages referenced to V –

V+ ..... 44 V
GND ..... 25 V
Digital inputs[3], V_S, V_D ..... –2 V to (V^+ +2 V) or 20 mA, whichever occurs first
Current, Any Terminal Except S or D ..... 30 mA
Continuous Current, S or D ..... 20 mA
Peak Current S or D
(pulsed at 1 msec, 10% duty cycle max) ..... 70 mA
Storage Temperature (A & B Suffix) ..... –65 to 150°C
(C Suffix) ..... –65 to 125°C
Operating Temperature (A Suffix) ..... –55 to 125°C
(B Suffix) ..... –20 to 85°C
(C Suffix) ..... 0 to 70°C

Power Dissipation (Package)*
16-Pin DIP** ..... 900 mW
16-Pin Plastic DIP*** ..... 470 mW

*Device mounted with all leads soldered or welded to PC board.
**Derate 12 mW/°C above 75°C.
***Derate 6.5 mW/°C above 25°C.

Stresses listed under "Absolute Maximum Ratings" may be applied (one at a time) to devices without resulting in permanent damage. This is a stress rating only and not subject to production testing. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		CHARACTERISTIC		TYP[1] 25°C	MAX LIMITS A SUFFIX –55°C	A SUFFIX 25°C	A SUFFIX 125°C	B/C SUFFIX –20°C/0°C	B/C SUFFIX 25°C	B/C SUFFIX 85°C/70°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V– = –15 V, GND = 0	
1		V_{ANALOG}	Minimum Analog Signal Handling Capability	±15		±15	±15		±15	±15	V		
2	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	105	175	175	250	200	200	250	Ω	V_D = 10 V	V_{IN} = 2.4 V, I_S = –1 mA
3				115	175	175	250	200	200	250		V_D = –10 V	
4		$I_{S(off)}$	Source OFF Leakage Current	0.01		1	100		5	100	nA	V_S = 14 V, V_D = –14 V	V_{IN} = 0.8 V
5				–0.02		–1	–100		–5	–100		V_S = –14 V, V_D = 14 V	
6		$I_{D(off)}$	Drain OFF Leakage Current	0.01		1	100		5	100		V_D = 14 V, V_S = –14 V	
7				–0.02		–1	–100		–5	–100		V_D = –14 V, V_S = 14 V	
8		$I_{D(on)}$[2]	Drain ON Leakage Current	0.1		1	200		5	200		V_D V_S = 14 V	V_{IN} = 2.4 V
9				–0.15		–1	–200		–5	–200		V_D = V_S = –14 V	
10	INPUT	I_{INH}	Input Current, Input Voltage High	–.0004		–1	–10		–1	–10	μA	V_{IN} = 2.4 V	
11				.003		1	10		1	10		V_{IN} = 15 V	
12		I_{INL}	Input Current, Input Voltage Low	–.0004		–1	–10		–1	–10		V_{IN} = 0	
13	DYNAMIC	t_{on}	Turn-ON Time	480		1000			1000		ns	See Switching Time Test Circuit	
14		t_{off}	Turn-OFF Time	370		500			500				
15		Q	Charge Injection	20							pC	C_L = 1000pF, V_{GEN} = 0 V, R_{GEN} = 0Ω	
16		$C_{S(off)}$	Source OFF Capacitance	5							pF	V_S = 0, V_{IN} = 0 V	f = 140 KHz
17		$C_{D(off)}$	Drain OFF Capacitance	5								V_D = 0, V_{IN} = 0 V	
18		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance	16								V_D = V_S = 0, V_{IN} = 5 V	
19		OIRR	Off Isolation	70							dB	V_{IN} = 0 V	
20		CCRR	Channel to Channel Crosstalk	90								V_S = 2 Vpp, f = 100 KHz, Z_L = 75Ω	
21	SUPPLY	I+	Positive Supply Current	.9		2			2		mA	All Channels "ON" or "OFF," V_{IN} = 0 or 2.4 V	
22		I–	Negative Supply Current	–.3		–1			–1				

NOTES:

1. Typical Values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
2. $I_{D(on)}$ is leakage from driver into "ON" switch.
3. Signals on S_X, D_X or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

ICMC-D

See Product Selector Guides on Pages 2779-2783.

Quad Monolithic SPST CMOS Analog Switch

Siliconix

designed for . . .

- **Low Transient Switching i.e., Sample and Hold Circuits**
- **Switching Multiple Signals such as Multiplexing Inputs**
- **High Frequency Signal Switching e.g., Computer Peripheral Equipment**
- **TTL Compatible Systems Including Microprocessor Systems**

BENEFITS

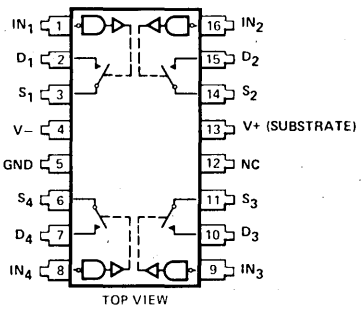
- **Environmentally Rugged**
  - Latchproof
  - Power Supply Overvoltage to 40V Max
- **Reduced Switching Error**
  - Low Charge Coupling
- **Easily Interfaced**
  - TTL, DTL and CMOS Compatible without Pull Up Resistors
- **Reduces External Component Requirements**
  - ±15 V Analog Signal Range with ±15 V Supplies
- **Reduced System Cross-Talk**
  - Break-Before-Make Switching
- **Eliminates Signal Error**
  - 0.01 nA Typical Leakage From Source Or Drain
- **Pin for Pin Compatible with**
  - Intersil IH5052, IH201
- **Low Cost**

DESCRIPTION

The DG211 designed on the Siliconix PLUS-40 CMOS process is a 4-channel single pole single throw analog switch with low and nearly constant ON resistance over the entire analog signal range. The switch will conduct current in either direction with no offset voltage in the ON condition, and block voltages up to 30 V peak-to-peak in the OFF condition. The ON-OFF state of each switch is controlled by a driver. With a logic "0" at the input to the driver (– 15 V to 0.8 V) thw switch will be ON, and a logic "1" (2.4 V to 15 V) will turn the switch OFF. The input can thus be directly interfaced with TTL, DTL, RTL, CMOS and certain PMOS circuits. Switch action is break-before-make. Logic inputs can directly connect to op-amp output swings.

PIN CONFIGURATION

Dual-In-Line Package



TOP VIEW

LOGIC	SWITCH
0	ON
1	OFF

ORDER NUMBER:
DG211CJ
SEE PACKAGE 8

SWITCH OPEN FOR LOGIC "1" INPUT (POSITIVE LOGIC)

ABSOLUTE MAXIMUM RATINGS

V+ to V−	40 V
V_{IN} to Ground	V−, V+
V_L to Ground	−0.3 V, 25 V
V_S or V_D to V+	0, −40 V
V_S or V_D to V−	0, 40 V
V+ to Ground	25 V
V− to Ground	−25 V
Current, Any Terminal Except S or D	30 mA
Continuous Current, S or D	20 mA
Peak Current, S or D (pulsed at 1 msec, 10% duty cycle max)	70 mA
Storage Temperature	−65 to 125°C
Operating Temperature	0 to 70°C
Power Dissipation (Package)*	
16 Pin Plastic DIP**	470 mW

*Device mounted with all leads soldered or welded to PC board.

**Derate 6.5 mW/°C above 25°C

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

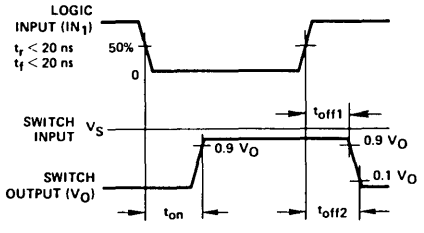
		CHARACTERISTIC		TYP[1] 25°C	MAX LIMITS C SUFFIX 25°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V− = −15 V, Gnd = 0, V_L = 5 V	
1		V_{ANALOG}	Min. Analog Signal Handling Capability	±15	±15	V		
2	SWITCH	$r_{DS(on)}$	Drain Source ON Resistance	105	175	Ω	V_D = 10 V	V_{IN} = 0.8 V, I_S = −1 mA
3				115	175		V_D = −10 V	
4		$I_{S(off)}$	Source OFF Leakage Current	0.01	5	nA	V_S = 14 V, V_D = −14 V	V_{IN} = 2.4 V
5				−0.02	−5		V_S = −14 V, V_D = 14 V	
6		$I_{D(off)}$	Drain OFF Leakage Current	0.01	5		V_D = 14 V, V_S = 14 V	
7				−0.02	−5		V_D = −14 V, V_S = 14 V	
8		$I_{D(on)}$[2]	Drain ON Leakage Current	0.1	5		V_D = V_S = 14 V	V_{IN} = 0.8 V
9				−0.15	−5		V_D = V_S = 14 V	
10	INPUT	I_{INH}	Input Current, Input Voltage High	−0.0004	1	μA	V_{IN} = 2.4 V	
11				0.003	1		V_{IN} = 15 V	
12		I_{INL}	Input Current, Input Voltage Low	−0.0004	1		V_{IN} = 0	
13	DYNAMIC	t_{on}	Turn-ON Time	460	1000	ns	V_S = 2 V, R_L = 1K Ω, C_L = 35 pF	See Switching Time Test Circuit
14		t_{off1}	Turn-OFF Time	360	500			
15		t_{off2}	Turn-OFF Time	450				
16		$C_{S(off)}$	Source OFF Capacitance	5		pF	V_S = 0, V_{IN} = 5 V	f = 1 MHz
17		$C_{D(off)}$	Drain OFF Capacitance	5			V_D = 0, V_{IN} = 5 V	
18		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance	16			V_D = V_S = 0, V_{IN} = 0	
19		OFF Isolation[3]		70		dB	V_{IN} = 5 V, R_L = 1K Ω, C_L = 15 pF, V_S = 1 VRMS, f = 100 kHz	
20		Interchannel Crosstalk Isolation		90				
21	SUP	I+	Positive Supply Current	0.35	0.48	mA	V_{IN} = 0 or 2.4 V	
22		I−	Negative Supply Current	0.30	0.48			
23		I_L	Logic Supply Current	0.5	1.2			

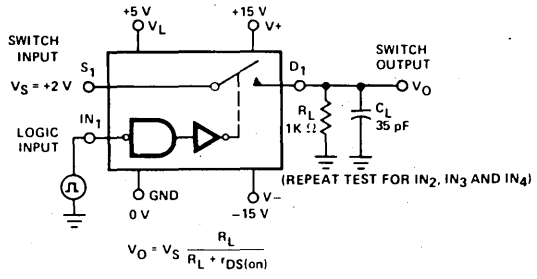
1. Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
2. $I_{D(on)}$ is leakage from driver into ON switch.
3. OFF Isolation = $20 \log \frac{|V_S|}{|V_D|}$, V_S = input to OFF switch, V_D = output.

ICMC-A

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.





See Product Selector Guides on Pages 2779-2783.

Quad Monolithic SPST CMOS Analog Switch

Siliconix

designed for . . .

- **Low Transient Switching i.e., Sample and Hold Circuits**
- **Switching Multiple Signals such as Multiplexing Inputs**
- **High Frequency Signal Switching e.g., Computer Peripheral Equipment**
- **TTL Compatible Systems Including Microprocessor Systems**

BENEFITS

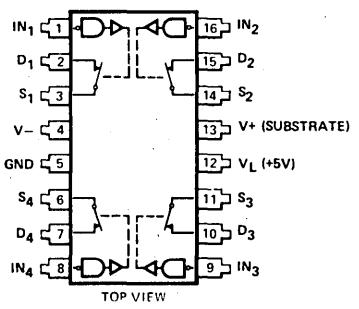
- **Environmentally Rugged**
  - Latchproof
  - 40 V Power Supply Max Rating
- **Reduced Switching Error**
  - Low Charge Coupling
- **Easily Interfaced**
  - TTL, DTL and CMOS Compatible without Pull Up Resistors
- **Reduces External Component Requirements**
  - ±15 V Analog Signal Range with ±15 V Supplies
- **Reduced System Cross-Talk**
  - Break-Before-Make Switching
- **Eliminates Signal Error**
  - 0.01 nA Typical Leakage From Source or Drain
- **Pin for Pin Compatible with Intersil IH5053, IH202**
- **Opposite Logic Control of DG211**
- **Low Cost**

DESCRIPTION

The DG212 designed on the Siliconix PLUS-40 CMOS process is a 4-channel single pole single throw analog switch with low and nearly constant ON resistance over the entire analog signal range. The switch will conduct current in either direction with no offset voltage in the ON condition, and block voltages up to 30 V peak-to-peak in the OFF condition. The ON-OFF state of each switch is controlled by a driver. With a logic "0" at the input to the driver (–15 V to 0.8 V) the switch will be OFF, and a logic "1" (2.4 V to 15 V) will turn the switch ON. The input can thus be directly interfaced with TTL, DTL, RTL, CMOS and certain PMOS circuits. Switch action is break-before-make. Logic inputs can directly connect to op-amp output swings.

PIN CONFIGURATION

Dual-In-Line Package



LOGIC	SWITCH
0	OFF
1	ON

ORDER NUMBER:
DG212CJ
SEE PACKAGE 8

SWITCH CLOSED FOR LOGIC "1" INPUT (POSITIVE LOGIC)

ABSOLUTE MAXIMUM RATINGS

Voltages referenced to V–

V+ . . . . . 44 V
GND . . . . . 25 V
Digital inputs[4] V_S, V_D . . . . . −2 V to (V^+ +2 V) or 20 mA, whichever occurs first.

Current, Any Terminal Except S or D . . . . . 30 mA
Continuous Current, S or D . . . . . 20 mA
Peak Current, S or D
(pulsed at 1 msec, 10% duty cycle max) . . . . . 70 mA
Storage Temperature . . . . . −65 to 125°C
Operating Temperature . . . . . 0 to 70°C

Power Dissipation (Package)*
16 Pin Plastic DIP** . . . . . 470 mW

*Device mounted with all leads soldered or welded to PC board.
**Derate 6.5 mW/°C above 25°C

Stresses listed under "Absolute Maximum Ratings" may be applied (one at a time) to devices without resulting in permanent damage. This is a stress rating only and not subject to production testing. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		CHARACTERISTIC		TYP[1] 25°C	MAX LIMITS C SUFFIX 25°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V– = –15 V, Gnd = 0, V_L = 5 V	
1	SWITCH	V_{ANALOG}	Min. Analog Signal Handling Capability	±15	±15	V		
2		$r_{DS(on)}$	Drain Source ON Resistance	105	175	Ω	V_D = 10 V	V_{IN} = 2.4 V, I_S = –1 mA
3				115	175		V_D = –10 V	
4		$I_{S(off)}$	Source OFF Leakage Current	0.01	5	nA	V_S = 14 V, V_D = 14 V	V_{IN} = 0.8 V
5				0.02	–5		V_S = –14 V, V_D = 14 V	
6		$I_{D(off)}$	Drain OFF Leakage Current	0.01	5		V_D = 14 V, V_S = 14 V	
7				0.02	–5		V_D = –14 V, V_S = 14 V	
8		$I_{D(on)}$[2]	Drain ON Leakage Current	0.1	5		V_D = V_S = 14 V	V_{IN} = 2.4 V
9				0.15	–5		V_D = V_S = –14 V	
10	INPUT	I_{INH}	Input Current, Input Voltage High	0.0004	1	µA	V_{IN} = 2.4 V	
11				0.003	1		V_{IN} = 15 V	
12		I_{INL}	Input Current, Input Voltage Low	0.0004	1		V_{IN} = 0	
13	DYNAMIC	t_{on}	Turn-ON Time	460	600	ns	V_S = 2 V, R_L = 1K Ω, C_L = 35 pF	See Switching Time Test Circuit
14		t_{off1}	Turn-OFF Time	360	450			
15		t_{off2}	Turn-OFF Time	450				
16		$C_{S(off)}$	Source OFF Capacitance	5		pF	V_S = 0, V_{IN} = 0 V	f = 1 MHz
17		$C_{D(off)}$	Drain OFF Capacitance	5			V_D = 0, V_{IN} = 0 V	
18		$C_{D(on)}$ + $C_{S(on)}$	Channel ON Capacitance	16			V_D = V_S = 0, V_{IN} = 5 V	
19		OFF Isolation[3]		70		dB	V_{IN} = 0 V, R_L = 1K Ω, C_L = 15 pF, V_S = 1 VRMS, f = 100 kHz	
20		Interchannel Crosstalk Isolation		90				
21	SUP	I+	Positive Supply Current	0.35	0.48	mA	V_{IN} = 0 or 2.4 V	
22		I–	Negative Supply Current	0.30	0.48			
23		I_L	Logic Supply Current	0.5	1.2			

1. Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
2. $I_{D(on)}$ is leakage from driver into ON switch.
3. OFF Isolation = $20 \log \frac{|V_S|}{|V_D|}$, V_S = input to OFF switch, V_D = output.
4. Signals on S_X, D_X or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

ICMC-C

See Product Selector Guides on Pages 2779-2783.

Quad Monolithic SPST CMOS Analog Switch with Data Latches

Siliconix

designed for . . .

- **Data Acquisition Systems**
- **Automatic Test Equipment**
- **Communication Systems**
- **Microprocessor Controlled Systems**

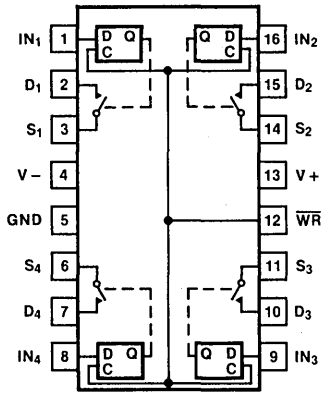
BENEFITS

- **Environmentally Rugged**
  - 44V Power Supply Max Rating
  - Static Protected
  - Latchproof CMOS Process
  - Improved Input Protection
- **Easily Interfaced**
  - TTL Compatible Without Pullup Resistor
  - On-Chip Regulator Allows Wide Tolerance of Supplies Without Affecting TTL Switching Levels
- **Microprocessor Bus Compatible**
  - Accepts 230 ns Write Plus Width
  - Guaranteed Break-Before-Make
- **Improved System Accuracy**
  - $V_{ERROR} = 0.45\ \mu V$ max
    $= I_{D(on)} \times R_{DS(on)}$

DESCRIPTION

The DG221 is designed on the SILICONIX PLUS-40 CMOS PROCESS providing solid state switch action with 60 ohms (typical) contact resistance and very high OFF resistance. True switch action takes place over the full analog signal range of ± 15V with guaranteed break-before-make switch action to prevent momentary shorting of input signals. The input protection circuitry protects inputs from static damage and gives high noise immunity. Charge injection has been reduced by design to minimize switching transients. Latches on all four switches result in μP bus compatibility.

PIN CONFIGURATION



IN_X	$\overline{WR}$	SWITCH
0	0	ON
1	0	OFF
X	1	Maintains Previous State

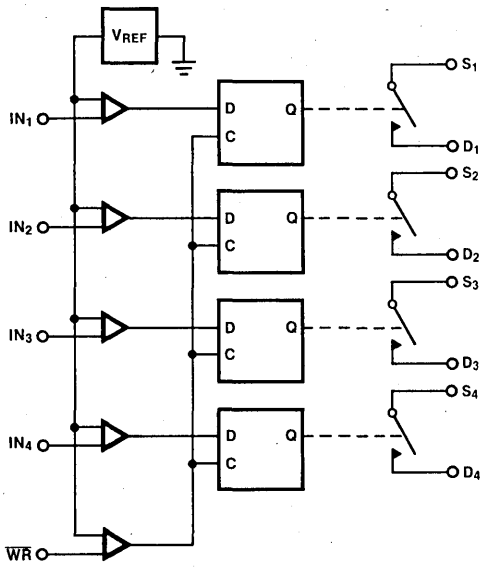
Logic "1" $V_{IN} \geq 2.4V$
Logic "0" $V_{IN} \leq 0.8V$
$\overline{WR}$ input is level sensitive (not edge-triggered)

ORDER NUMBERS:
DG221AK, DG221BK or DG221CK
SEE PACKAGE 10

DG221CJ
SEE PACKAGE 8

SWITCHES ARE SHOWN IN THE LOGIC "1" INPUT STATE

FUNCTIONAL DIAGRAM (typical switch)



ABSOLUTE MAXIMUM RATINGS

Voltages referenced to V–

V+ 44V
GND 25V
Digital inputs $\overline{WR}$, V_S, V_D[3] ..... – 2V to (V+ + 2V) or 20 mA, whichever occurs first
Current, Any Terminal Except S or D ..... 30 mA
Continuous Current, S or D ..... 20 mA
Peak Current S or D
(pulsed at 1 msec, 10% duty cycle max) ..... 70 mA
Storage Temperature (A & B Suffix) .... – 65 to +150°C
(C Suffix) ..... – 65 to +125°C
Operating Temperature (A Suffix) ..... – 55 to +125°C
(B Suffix) ..... – 20 to +85°C
(C Suffix) ..... 0 to +70°C

Power Dissipation (Package)*
16-Pin DIP** ..... 900 mW
16-Pin Plastic DIP*** ..... 470 mW

*Device mounted with all leads soldered or welded to PC board.
**Derate 12 mW/°C above 75°C.
***Derate 6.5 mW/°C above 25°C.

Stresses listed under "Absolute Maximum Ratings" may be applied (one at a time) to devices without resulting in permanent damage. This is a stress rating only and not subject to production testing. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS All DC parameters are 100% tested at 25°C. Sample parts are tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		CHARACTERISTIC		TYP[1] 25°C	MAX LIMITS A SUFFIX -55°C	A SUFFIX 25°C	A SUFFIX 125°C	B/C SUFFIX -20°C/ 0°C	B/C SUFFIX 25°C	B/C SUFFIX 85°C/ 70°C	UNIT	TEST CONDITIONS, UNLESS NOTED V+ = 15V, V– = + 15V, GND = 0	
1	SWITCH	V_{ANALOG}	Analog Signal Handling Capability	±15		±15	±15		±15	±15	V		
2	SWITCH	$r_{DS(on)}$[4]	Drain-Source ON Resistance	60	90	90	135	90	90	135	Ω	V_D = 10V	V_{IN} = 0.8V, I_S = – 1 mA
3	SWITCH	$r_{DS(on)}$[4]	Drain-Source ON Resistance	70	90	90	135	90	90	135	Ω	V_D = – 10V	V_{IN} = 0.8V, I_S = – 1 mA
4	SWITCH	$I_{S(off)}$	Source OFF Leakage Current	0.01		1	100		5	100	nA	V_S = 14V, V_D = – 14V	V_{IN} = 2.4V
5	SWITCH	$I_{S(off)}$	Source OFF Leakage Current	-0.02		-1	-100		-5	-100	nA	V_S = – 14V, V_D = 14V	V_{IN} = 2.4V
6	SWITCH	$I_{D(off)}$	Drain OFF Leakage Current	0.01		1	100		5	100	nA	V_D = 14V, V_S = – 14V	V_{IN} = 2.4V
7	SWITCH	$I_{D(off)}$	Drain OFF Leakage Current	-0.02		-1	-100		-5	-100	nA	V_D = – 14V, V_S = 14V	V_{IN} = 2.4V
8	SWITCH	$I_{D(on)}$[2]	Drain ON Leakage Current	0.1		1	200		5	200	nA	V_D = V_S = 14V	V_{IN} = 0.8V
9	SWITCH	$I_{D(on)}$[2]	Drain ON Leakage Current	-0.15		-1	-200		-5	-200	nA	V_D = V_S = – 14V	V_{IN} = 0.8V
10	INPUT	I_{INH}, $I_{\overline{WR}\ H}$	Input Current, Input Voltage High	-.0004		-1	-10		-1	-10	μA	V_{IN} = 2.4V	
11	INPUT	I_{INH}, $I_{\overline{WR}\ H}$	Input Current, Input Voltage High	.003		1	10		1	10	μA	V_{IN} = 15V	
12	INPUT	I_{INL}, $I_{\overline{WR}\ L}$	Input Current, Input Voltage Low	-.0004		-1	-10		-1	-10	μA	V_{IN} = 0V	
13	SUP	I+	Positive Supply Current	0.8		1.5			1.5		mA	All Channels "ON" or "OFF", V_{IN} = 0 or 2.4V	
14	SUP	I–	Negative Supply Current	-.4		-1.0			-1.0		mA	All Channels "ON" or "OFF", V_{IN} = 0 or 2.4V	
15	DYNAMIC	Q	Charge Injection	20							pC	C_L = 1000 pF, V_{GEN} = 0V, R_{GEN} = 0Ω	
16	DYNAMIC	$C_{S(off)}$	Source Off Capacitance	8							pF	V_S = 0, V_{IN} = 5V	f = 1 MHz
17	DYNAMIC	$C_{D(off)}$	Drain OFF Capacitance	9							pF	V_D = 0, V_{IN} = 5V	f = 1 MHz
18	DYNAMIC	$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance	29							pF	V_D = V_S = 0, V_{IN} = 0	f = 1 MHz
19	DYNAMIC	OIRR	Off isolation	70							dB	V_{IN} = 5V	
20	DYNAMIC	CCRR	Channel to Channel Crosstalk	90							dB	V_S = 1 V_{pp}, f = 100 kHz, R_L = 1 kΩ, C_L = 15 pF	
21	DYNAMIC	t_{on}	Turn-ON Time			550			550		nS	See Switching Time Test Circuit, Fig. 1	
22	DYNAMIC	t_{off}	Turn-OFF Time			340			340		nS	See Switching Time Test Circuit, Fig. 1	
23	DYNAMIC	t_{on}, $\overline{WR}$	Turn-ON Time Write			550			550		nS	See Switching Time Test Circuit, Fig. 2	
24	DYNAMIC	t_{off}, $\overline{WR}$	Turn-OFF Time Write			340			340		nS	See Switching Time Test Circuit, Fig. 2	

ICMM-A

NOTES:
1. Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
2. $I_{D(on)}$ is leakage from driver into "ON" switch.
3. Signals on S_X, D_X, $\overline{WR}$ or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
4. $\Delta r_{DS(on)}$ is guaranteed to be within ±5% switch to switch within a package (not a tested parameter).

See Product Selector Guides on Pages 2779-2783.

Monolithic General Purpose CMOS Analog Switch

Siliconix

designed for . . .

- **Programmable Gain Amplifiers**
- **Analog Multiplexing**
- **Servo Control Switching**

BENEFITS

- **Transient Suppression**
  - Make-Before-Break Switch Operation
- **Environmentally Rugged**
  - 40V Power Supply Rating
  - Static Protected Logic Inputs
  - Latchproof
- **Easily Interfaced**
  - TTL and CMOS Compatible without Pull Up Resistors
- **Reduces External Component Requirements**
  - Full Rail to Rail Analog Signal Range
  - No Diode Protection Required Between V_L and V+ for Power Supply Sequencing
- **Pin for Pin Compatible with**
  - IH5043
  - HI5043
  - DG5043, DG191, DG390

DESCRIPTION

The DG243 designed on the Siliconix PLUS-40 CMOS process provides solid state switch action with 50 ohms contact resistance and very high OFF resistance. True switch action takes place over the full analog signal range of ±15 volts, with Make-Before-Break operation improving transient response in programmable gain amplifiers.

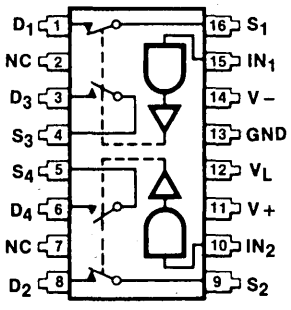
PIN CONFIGURATIONS

DUAL SPDT

LOGIC	SW 1 SW 2	SW 3 SW 4
0	OFF	ON
1	ON	OFF

ALL SWITCHES SHOWN IN THE LOGIC "1" SWITCH STATE

Dual-In-Line Package

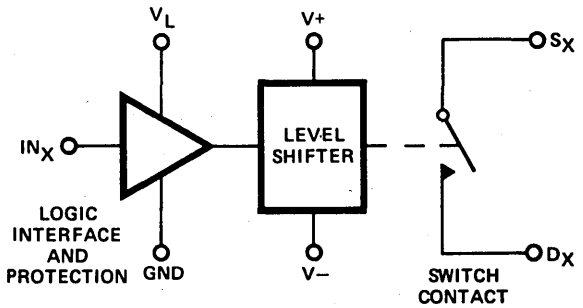


TOP VIEW

ORDER NUMBER:
DG243AK or DG243CK
SEE PACKAGE 10

DG243CJ
SEE PACKAGE 8

FUNCTIONAL DIAGRAM (typical channel)



ABSOLUTE MAXIMUM RATINGS

Voltages referenced to V–

V+ . . . . . 44 V
V_L . . . . . (GND –0.3 V) to 44 V
GND . . . . . 25 V
Digital inputs[5] V_S, V_D . . . . . –2 V to (V^+ +2 V) or 30 mA, whichever occurs first.

Current, Any Terminal Except S or D . . . . 30 mA
Continuous Current, S or D . . . . . 30 mA
Peak Current, S or D
(pulsed at 1 msec, 10% duty cycle max) . . . . 100 mA
Storage Temperature (A Suffix) . . . . . -65 to 150°C
(C Suffix) . . . . . -65 to 125°C
Operating Temperature (A Suffix) . . . . -55 to 125°C
(C Suffix) . . . . . 0 to 70°C
Power Dissipation*
Metal Can and Plastic DIP** . . . . . 450 mW
16 Pin DIP**** . . . . . 900 mW
Flat Pack***** . . . . . 900 mW

*All leads welded or soldered to PC board.
**Derate 6 mW/°C above 75°C
****Derate 12 mW/°C above 75°C
*****Derate 10 mW/°C above 75°C

Stresses listed under "Absolute Maximum Ratings" may be applied (one at a time) to devices without resulting in permanent damage. This is a stress rating only and not subject to production testing. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25° C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		CHARACTERISTICS		MAX LIMITS A SUFFIX –55°C	A SUFFIX 25°C	A SUFFIX 125°C	C SUFFIX 0°C	C SUFFIX 25°C	C SUFFIX 70°C	UNIT	TEST CONDITIONS V+ = 15V, V– = –15V, V_L = 5V, GND = 0V	
1		V_{ANALOG}	Minimum Analog Signal Handling Capability		±15	±15		±15	±15	V		
2	SWITCH	$r_{DS(on)}$[3]	Drain Source ON Resistance	50	50	75	50	50	75	Ω	V_D = 10 V, I_S = –10 mA	Note 1
3				50	50	75	50	50	75		V_D = –10 V, I_S = –10 mA	
4		$I_{S(off)}$[3]	Source OFF Leakage Current		1	100		1	100	nA	V_S = 14 V, V_D = –14 V	
5					–1	–100		–1	–100		V_S = –14 V, V_D = 14 V	
6		$I_{D(off)}$[3]	Drain OFF Leakage Current		1	100		1	100		V_S = –14 V, V_D = 14 V	
7					–1	–100		–1	–100		V_S = 14 V, V_D = –14 V	
8		$I_{D(on)}$[3]	Drain ON Leakage Current		2	200		2	200		V_S = V_D = 14 V	
9					–2	–200		–2	–200		V_S = V_D = –14 V	
10	INPUT	I_{INH}[3]	Input Current Input Voltage High		±1	±1		±1	±1	μA	V_{INH} = 2.0 V	
11		I_{INL}[3]	Input Current Input Voltage Low		±1	±1		±1	±1		V_{INL} = 0.8 V	
12	DYNAMIC	t_{on}[4]	Turn-ON Time		500			700		ns	V_S = ±10 V, R_L = 1KΩ	Note 2
13		t_{off}[4]	Turn-OFF Time		1000			1200			C_L = 35 pF	
14		Q	Charge Injection	60 Typical						pC	C_L = 1000pF, R_{GEN} = 0Ω, V_{GEN} = 0 V	
15		$C_{S(off)}$	Source OFF Capacitance	15 Typical						pF	V_S = V_D = 0 V, f = 1 MHz	Note 1
16		$C_{D(off)}$	Drain OFF Capacitance	17 Typical								
17		$C_{D(on)}$ + $C_{S(on)}$	Channel ON Capacitance	45 Typical								
18		OIRR	OFF Isolation	75 Typical						dB	Z_L = 75Ω, V_S = 2 Vpp, f = 1 MHz	
19		CCRR	Interchannel Crosstalk Isolation	89 Typical								
20	SUPPLY	$I+$[3]	Positive Supply Current	300	300	300	300	300	300	μA	V_{IN} = 0 V or 2.4 V	
21		$I-$[3]	Negative Supply Current	–300	–300	–300	–300	–300	–300			
22		I_L[3]	Logic Supply Current	300	300	300	300	300	300			
23		I_{GND}	Ground Supply Current	–300	–300	–300	–300	–300	–300			

ICMK-C

NOTES:

1: V_{IN} = Input voltage to perform proper function.
For Logic "1" — V_{INH} = 2.0 V
For Logic "0" — V_{INL} = 0.8 V

2: See Switching Time Test Circuit.

3: Limits of these paramaters are tested 100% at 25 °C and 125°C for "/883" devices.

4: For "/883" devices these parameters are 100% tested at 25°C.

5: Signals on S_X, D_X or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

See Product Selector Guides on Pages 2779-2783.

Quad Monolithic SPST CMOS Analog Switch

Siliconix

designed for . . .

- **Portable, Battery Powered Instrumentation**
- **Automotive Applications**
- **Computer Peripherals**
- **Communication Systems**
- **High Speed Multiplexing**
- **Low Leakage Switching**
- **Sample and Hold**
- **Data Acquisition Systems**
- **Single or Dual Supply Systems**

BENEFITS

- **High Speed Switching with Break-Before-Make**
  - t_{on} = 130 nsec Typical
  - t_{off} = 90 nsec Typical
- **Single Supply Operation**
  - +5V to +30V
- **CMOS Compatible (positive logic)**
  - For TTL Logic Compatibility Use DG202
- **Wide Signal Range ±15V**
- **Low Standby Power**
  - 300 μW Max
- **Minimizes Signal Error**
  - r_{DS} < 60Ω Typical
  - $I_{D(off)}$ < 100 pA Typical
  - Minimized Switching Transients
- **Environmentally Rugged**
  - Latchproof CMOS Process

DESCRIPTION:

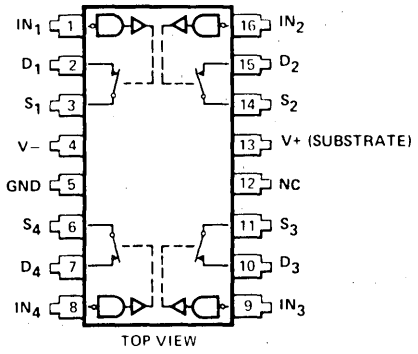
The DG308A is a monolithic quad single-pole single-throw analog switch fabricated in complementary MOS technology. In the ON condition, each switch will conduct current in either direction and in the OFF condition each switch will block voltages up to 30 volts peak to peak. The ON-OFF State of each switch is controlled by a driver. With CMOS logic '1' at the input the switch will be ON, with logic '0' at the input the switch will be OFF.

PIN CONFIGURATION

ORDER NUMBERS:
DG308AAK, DG308ABK, DG308ACK
SEE PACKAGE 10
(CERDIP)

DG308ACJ
SEE PACKAGE 8
(PLASTIC)

Dual-In-Line Package



TOP VIEW

LOGIC	SWITCH
0	OFF
1	ON

SWITCH CLOSED FOR LOGIC "1" (POSITIVE LOGIC)

ABSOLUTE MAXIMUM RATINGS

Voltages referenced to V–
V+ 44V
GND 25V
Digital inputs, V_S, V_D[4] ..... – 2V to (V^+ + 2V) or 20 mA, whichever occurs first
Current, Any Terminal Except S or D ..... 30 mA
Continuous Current, S or D ..... 20 mA
Peak Current S or D
(pulsed at 1 msec, 10% duty cycle max) ..... 70 mA
Storage Temperature (A & B Suffix) ..... – 65 to + 150°C
(C Suffix) ..... – 65 to + 125°C
Operating Temperature (A Suffix) ..... – 55 to + 125°C
(B Suffix) ..... – 20 to + 85°C
(C Suffix) ..... 0 to + 70°C
Power Dissipation (Package)*
16-Pin DIP** ..... 900 mW
16-Pin Plastic DIP*** ..... 470 mW

*Device mounted with all leads soldered or welded to PC board.
**Derate 12 mW/°C above 75°C.
***Derate 6.5 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

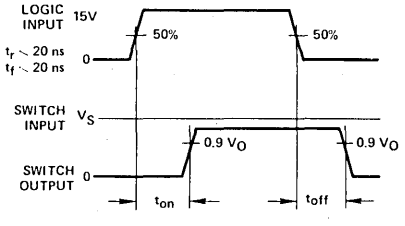
		CHARACTERISTIC		TYP[1] 25°C	MAX LIMITS A SUFFIX -55°C	A SUFFIX 25°C	A SUFFIX 125°C	B/C SUFFIX -20°C/ 0°C	B/C SUFFIX 25°C	B/C SUFFIX 85°C/ 70°C	UNIT	TEST CONDITIONS, UNLESS NOTED V+ = 15V, V– = + 15V, GND = 0	
1	SWITCH	V_{ANALOG}	Analog Signal Handling Capability	± 15							V	V+ = + 15V, V– = – 15V	GND = 0V
2	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	60	100	100	150	100	100	125	Ω	V_D = 10V, I_S = – 1 mA	V_{IN} = 11V
3	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	60	100	100	150	100	100	125	Ω	V_D = – 10V, I_S = 1 mA	V_{IN} = 11V
4	SWITCH	$I_{S(off)}$	Source OFF Leakage Current	0.1		1	100		5	100	nA	V_S = 14V, V_D = – 14V	V_{IN} = 3.5V
5	SWITCH	$I_{S(off)}$	Source OFF Leakage Current	-0.1		-1	-100		-5	-100	nA	V_S = – 14V, V_D = 14V	V_{IN} = 3.5V
6	SWITCH	$I_{D(off)}$	Drain OFF Leakage Current	0.1		1	100		5	100	nA	V_D = 14V, V_S = – 14V	V_{IN} = 3.5V
7	SWITCH	$I_{D(off)}$	Drain OFF Leakage Current	-0.1		-1	-100		-5	-100	nA	V_D = – 14V, V_S = 14V	V_{IN} = 3.5V
8	SWITCH	$I_{D(on)}$[2]	Drain ON Leakage Current	0.1		1	100		5	200	nA	V_D = V_S = 14V	V_{IN} = 11V
9	SWITCH	$I_{D(on)}$[2]	Drain ON Leakage Current	-0.1		-2	-200		-5	-200	nA	V_D = V_S = – 14V	V_{IN} = 11V
10	INPUT	I_{INH}	Input Current, Input Voltage High	0.001		1	1		1		μA	V_{IN} = 15V	
11	INPUT	I_{INH}	Input Current, Input Voltage High	0.001		1	1		1		μA	V_{IN} = 15V	
12	INPUT	I_{INL}	Input Current, Input Voltage Low	-0.001		-1	-1		-1		μA	V_{IN} = 0	
13	DYNAMIC	t_{on}	Turn ON Time	130		200			200		ns	See Switching Time Test Circuit	
14	DYNAMIC	t_{off}	Turn OFF Time	90		150			150		ns	See Switching Time Test Circuit	
15	DYNAMIC	Q	Charge Injection	-10							pC	C_L = 1000 pF, V_{GEN} = 0V, R_{GEN} = 0Ω	
16	DYNAMIC	$C_{S(off)}$	Source OFF Capacitance	11							pF	V_S = 0, V_{IN} = 0V	f = 140 kHz
17	DYNAMIC	$C_{D(off)}$	Drain OFF Capacitance	8							pF	V_D = 0, V_{IN} = 0V	f = 140 kHz
18	DYNAMIC	$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance	27							pF	V_D = V_S = 0, V_{IN} = 15V	f = 140 kHz
19	DYNAMIC	OIRR[3]	Off isolation	78							dB	V_{IN} = 0V, Z_L = 75Ω, V_S = 2 Vpp, f = 500 kHz	
20	DYNAMIC	CCRR	Channel to Channel Crosstalk	TBD							dB	V_{IN} = 0V, Z_L = 75Ω, V_S = 2 Vpp, f = 500 kHz	
21	SUP	I+	Positive Supply Current	0.001	10	10	100		100		μA	All Channels "ON" or "OFF", V_{IN} = 0V or 15V	
22	SUP	I–	Negative Supply Current	-0.001	-10	-10	-100		-100		μA	All Channels "ON" or "OFF", V_{IN} = 0V or 15V	

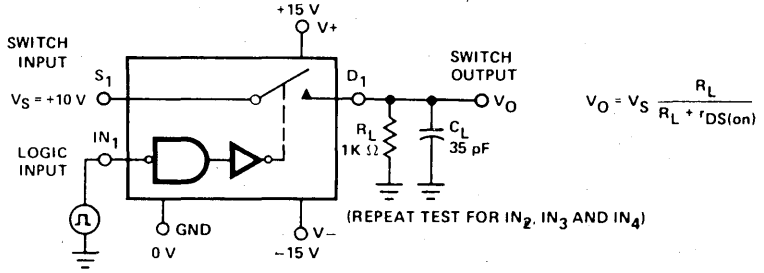
NOTES: ICMF-A

1. Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
2. V_{IN} = Input Voltage to perform proper function for logic '1' = 11V, for logic '0' = 3.5V.
3. OFF Isolation = $20 \log_{10} \frac{V_D}{V_S}$ V_D = Output, V_S = Input to OFF Switch
4. Signals on S_X, D_X or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current rating.

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or – as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.





See Product Selector Guides on Pages 2779-2783.

Quad Monolithic SPST CMOS Analog Switch

Siliconix

designed for . . .

- **Portable, Battery Instrumentation**
- **Computer Peripherals**
- **Communication Systems**
- **High Speed Multiplexing**
- **Sample and Hold**
- **Single or Dual Supply Systems**

BENEFITS

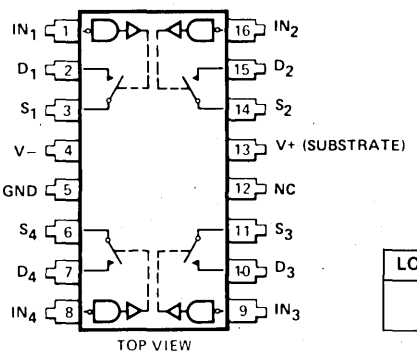
- **Environmentally Rugged**
  - 44V Power Supply Max Rating
  - Static Protected Logic Inputs
  - Latchproof
- **Minimizes System Power Requirements**
  - Operates Off Single Supply When V– Tied to GND
  - Low Quiescent Power <30 μW Typ
- **Fast t_{on} < 200 ns**
  t_{off} < 150 ns
- **Minimizes Signal Error**
  - $r_{DS(ON)}$ < 100Ω
  - $I_{D(OFF)}$ < 5 nA
  - Full Rail-to-Rail Analog Signal Range
- **Easily Interfaced**
  CMOS Logic Compatible
  For TTL Logic Compatibility Use DG201A

DESCRIPTION:

The DG309 designed on the Siliconix PLUS-40 CMOS process provides solid state switch action with 100 ohms contact (ON) resistance and very high OFF resistance. True bidirectional switch action occurs over the full analog signal range of ±15V, with Break-Before-Make operation to prevent momentary shorting of signal inputs.

PIN CONFIGURATION

Dual-In-Line Package



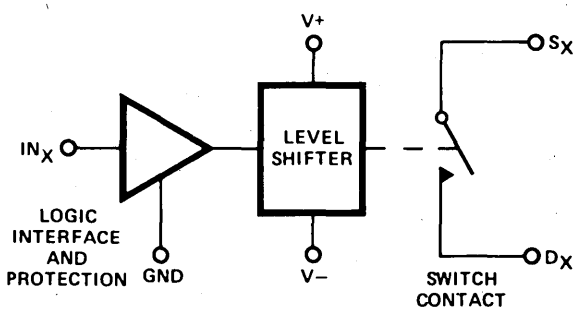
TOP VIEW

LOGIC	SWITCH
0	ON
1	OFF

ORDER NUMBERS:
DG309CJ
SEE PACKAGE 8 (PLASTIC)
DG309AK, DG309BK, DG309CK
SEE PACKAGE 10 (CERDIP)

SWITCHES ARE SHOWN IN THE LOGIC "1" INPUT STATE

FUNCTIONAL DIAGRAM (typical switch)



ABSOLUTE MAXIMUM RATINGS

Voltages referenced to V–

V+ 44V
GND 25V
Digital inputs, V_S, V_D[4] ..... – 2V to (V^+ +2V) or 20 mA, whichever occurs first
Current, Any Terminal Except S or D ..... 30 mA
Continuous Current, S or D ..... 20 mA
Peak Current S or D
(pulsed at 1 msec, 10% duty cycle max) ..... 70 mA
Storage Temperature (A & B Suffix) ..... – 65 to +150°C
(C Suffix) ..... – 65 to +125°C
Operating Temperature (A Suffix) ..... – 55 to +125°C
(B Suffix) ..... – 20 to +85°C
(C Suffix) ..... 0 to +70°C
Power Dissipation (Package)*
16-Pin DIP** ..... 900 mW
16-Pin Plastic DIP*** ..... 470 mW

*Device mounted with all leads soldered or welded to PC board.
**Derate 12 mW/°C above 75°C.
***Derate 6.5 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

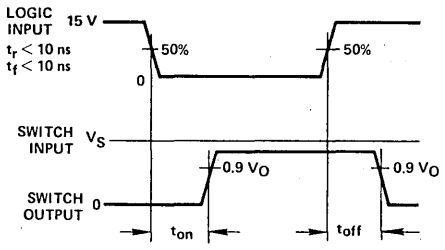
		CHARACTERISTIC		TYP[1] 25°C	MAX LIMITS A SUFFIX -55°C	A SUFFIX 25°C	A SUFFIX 125°C	B/C SUFFIX -20°C/ 0°C	B/C SUFFIX 25°C	B/C SUFFIX 85°C/ 70°C	UNIT	TEST CONDITIONS, UNLESS NOTED V+ = 15V, V– = +15V, GND = 0	
1	SWITCH	V_{ANALOG}	Analog Signal Handling Capability	±15							V	V+ = +15V, V– = –15V	GND = 0V
2	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	60	100	100	150	100	100	125	Ω	V_D = 10V, I_S = –1 mA	V_{IN} = 3.5V
3	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	60	100	100	150	100	100	125	Ω	V_D = –10V, I_S = 1 mA	V_{IN} = 3.5V
4	SWITCH	$I_{S(off)}$	Source OFF Leakage Current	0.1		1	100		5	100	nA	V_S = 14V, V_D = –14V	V_{IN} = 11V
5	SWITCH	$I_{S(off)}$	Source OFF Leakage Current	-0.1		-1	-100		-5	-100	nA	V_S = –14V, V_D = 14V	V_{IN} = 11V
6	SWITCH	$I_{D(off)}$	Drain OFF Leakage Current	0.1		1	100		5	100	nA	V_D = 14V, V_S = –14V	V_{IN} = 11V
7	SWITCH	$I_{D(off)}$	Drain OFF Leakage Current	-0.1		-1	-100		-5	-100	nA	V_D = –14V, V_S = 14V	V_{IN} = 11V
8	SWITCH	$I_{D(on)}$[2]	Drain ON Leakage Current	0.1		1	100		5	200	nA	V_D = V_S = 14V	V_{IN} = 3.5V
9	SWITCH	$I_{D(on)}$[2]	Drain ON Leakage Current	-0.1		-2	-200		-5	-200	nA	V_D = V_S = –14V	V_{IN} = 3.5V
10	INPUT	I_{INH}	Input Current, Input Voltage High	0.001		1	1		1		μA	V_{IN} = 15V	
11	INPUT	I_{INH}	Input Current, Input Voltage High	0.001		1	1		1		μA	V_{IN} = 15V	
12	INPUT	I_{INL}	Input Current, Input Voltage Low	-0.001		-1	-1		-1		μA	V_{IN} = 0	
13	DYNAMIC	t_{on}	Turn ON Time	130		200			200		ns	See Switching Time Test Circuit	
14	DYNAMIC	t_{off}	Turn OFF Time	90		150			150		ns	See Switching Time Test Circuit	
15	DYNAMIC	Q	Charge Injection	-10							pC	C_L = 1000 pF, V_{GEN} = 0V, R_{GEN} = 0Ω	
16	DYNAMIC	$C_{S(off)}$	Source OFF Capacitance	11							pF	V_S = 0, V_{IN} = 15V	f = 140 kHz
17	DYNAMIC	$C_{D(off)}$	Drain OFF Capacitance	8							pF	V_D = 0, V_{IN} = 15V	f = 140 kHz
18	DYNAMIC	$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance	27							pF	V_D = V_S = 0, V_{IN} = 0V	f = 140 kHz
19	DYNAMIC	OIRR[3]	Off isolation	78							dB	V_{IN} = 15V, Z_L = 75Ω, V_S = 2 Vpp, f = 500 kHz	
20	DYNAMIC	CCRR	Channel to Channel Crosstalk								dB	V_{IN} = 15V, Z_L = 75Ω, V_S = 2 Vpp, f = 500 kHz	
21	SUP	I+	Positive Supply Current	0.001	10	10	100		100		μA	All Channels "ON" or "OFF", V_{IN} = 0V or 15V	
22	SUP	I–	Negative Supply Current	-0.001	-10	-10	-100		-100		μA	All Channels "ON" or "OFF", V_{IN} = 0V or 15V	

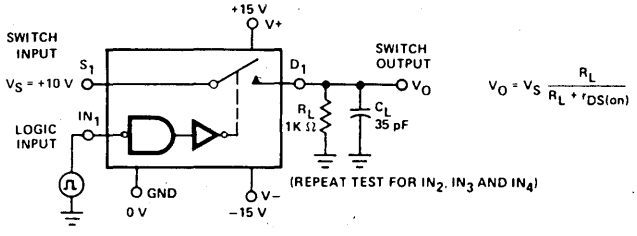
ICMF-B

NOTES:
1. Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
2. V_{IN} = Input Voltage to perform proper function for logic '1' = 11V, for logic '0' = 3.5V.
3. OFF Isolation = $20 \log_{10} \frac{V_D}{V_S}$ V_D = Output, V_S = Input to OFF Switch
4. Signals on S_X, D_X or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current rating.

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or – as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.





See Product Selector Guides on Pages 2779-2783.

16-Channel and Dual 8-Channel Analog Multiplexers

designed for . . .

- **Data Acquisition Systems**
- **Multiplexing Reference Signals**
- **Communication Systems**

Siliconix

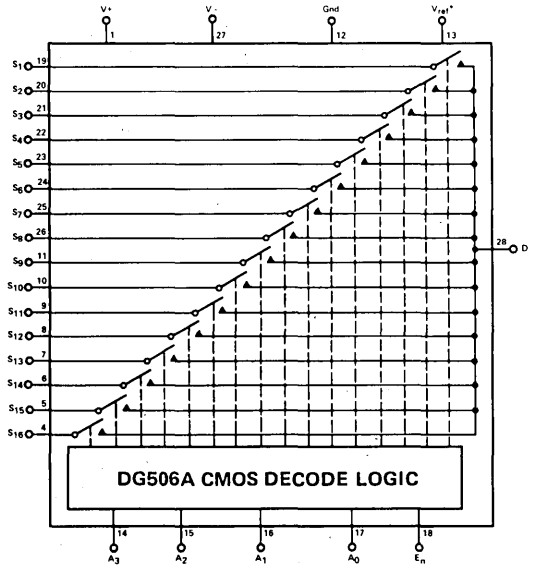
BENEFITS

- **Environmentally Rugged**
  - 40V Power Supply Max Rating
  - Static Protected Logic Inputs
  - Latchproof
- Easily Interfaced
  - TTL Compatible without Pull-Up Resistors
- **Improved System Accuracy**
  - $r_{DS(on)} < 400\Omega$
  - V_{ERROR} = 150 Microvolts at 125°C
    $= I_{D(on)} \times r_{DS(on)}$
  - $\Delta r_{DS(on)} < 6\%$
    for $-10V < V_{ANA} < +10V$
- **Pin for Pin Compatible with Intersil IH6116, Harris HI506 and Analog Devices AD7506**

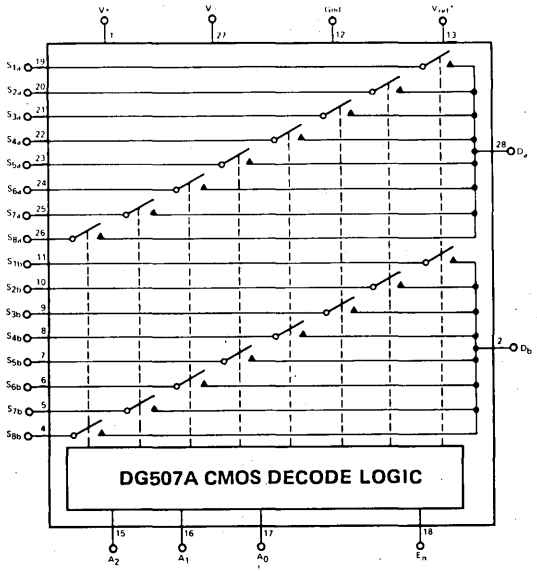
DESCRIPTION

The DG506A and DG507A designed on the Siliconix PLUS-40 CMOS process provides solid state switch action with 400 ohms contact (ON) resistance and very high OFF resistance. True bidirectional switch action takes place over the full analog signal range of ±15 volts, with Break-Before-Make operation to prevent momentary shorting of signal inputs. The DG506A provides 16 channel single ended multiplexing and demultiplexing of ±15 volt analog signals. The DG507A provides 8 channel differential multiplexing and demultiplexing of ±15 volt common mode plus differential signals.

FUNCTIONAL DIAGRAMS



DG506A
16 CHANNEL SINGLE ENDED MULTIPLEXER



DG507A
DIFFERENTIAL 8 CHANNEL MULTIPLEXER

ABSOLUTE MAXIMUM RATINGS

Voltages referenced to V–

V+ . . . . . 44 V
GND . . . . . 25 V
Digital inputs[5] V_S, V_D . . . . . −2 V to (V^+ +2 V) or 20 mA, whichever occurs first.
Current (Any Terminal, Except S or D) . . . . . 30 mA
Continuous Current, S or D . . . . . 20 mA
Peak Current, S or D
(Pulsed at 1 msec, 10% Duty Cycle Max) . . . . 40 mA
Storage Temperature (A & B Suffix) . . . . . −65 to 150°C
(C Suffix) . . . . . −65 to 125°C
Operating Temperature (A Suffix) . . . . . −55 to 125°C
(B Suffix) . . . . . −20 to 85°C
(C Suffix) . . . . . 0 to 70°C
Power Dissipation (Package)*
28 Pin DIP** . . . . . 1200 mW
28 Pin Plastic DIP*** . . . . . 625 mW

*All leads soldered or welded to PC board.
**Derate 16 mW/°C above 75°C.
***Derate 8.3 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		CHARACTERISTIC			MEASURED TERMINAL	NO. TESTS PER TEMP.	(Note 1) TYP 25°C	MAX LIMITS A SUFFIX −55°C	A SUFFIX 25°C	A SUFFIX 125°C	B/C SUFFIX −20/0°C	B/C SUFFIX 25°C	B/C SUFFIX 85/70°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V− = −15 V, Ground = 0, (Note 4)	
1		V_{ANALOG}	Minimum Analog Signal Handling Capability				±15		±15	±15		±15	±15	V		
2		$r_{DS(on)}$	Drain Source ON Resistance		S to D	16	270	400	400	500	450	450	550	Ω	V_D = 10 V, I_S = −200 μA	Sequence each switch on V_{AL} = 0.8 V, V_{AH} = 2.4 V V_{EN} = 2.4 V
3						16	230	400	400	500	450	450	550		V_D = −10 V, I_S = −200 μA	
4		$\Delta r_{DS(on)}$	Greatest Change in Drain-Source ON Resistance Between Channels		S to D	16	6							%	$\Delta r_{DS(on)} = \left(\frac{r_{DS(on)\ MAX} - r_{DS(on)\ MIN}}{r_{DS(on)\ AVE}}\right)$ −10 V ≤ V_S ≤ 10 V	
5	SWITCH	$I_{S(off)}$	Source OFF Leakage Current		S	16	0.002		±1	±50		±5	±50	nA	V_S = 10 V, V_D = −10 V	V_{EN} = 0
6						16	−0.005		±1	±50		±5	±50		V_S = −10 V, V_D = 10 V	
7		$I_{D(off)}$	Drain OFF Leakage Current	DG506A	D	1	0.020		±10	±300		±20	±300		V_D = 10 V, V_S = −10 V	
8						1	−0.03		±10	±300		±20	±300		V_D = −10 V, V_S = 10 V	
9				DG507A		2	0.007		±5	±200		±10	±200		V_D = 10 V, V_S = −10 V	
10						2	−0.015		±5	±200		±10	±200		V_D = −10 V, V_S = 10 V	
11		$I_{D(on)}$[2]	Channel ON Leakage Current	DG506A	D	16	0.03		±10	±300		±20	±300		$V_{S(all)}$ = V_D = 10 V	Sequence each switch on V_{AL} = 0.8 V, V_{AH} = 2.4 V V_{EN} = 2.4 V
12						16	−0.06		±10	±300		±20	±300		$V_{S(all)}$ = V_D = −10 V	
13				DG507A		16	0.015		±5	±200		±10	±200		$V_{S(all)}$ = V_D = 10 V	
14						16	−0.03		±5	±200		±10	±200		$V_{S(all)}$ = V_D = −10 V	
15	INPUT	I_{AH}	Address Input Current, Input Voltage High		A_0, A_1, A_2, (A_3) EN	(5) 4	−0.002		−10	−30		−10	−30	μA	V_A = 2.4 V	
16						(5) 4	0.006		10	30		10	30		V_A = 15 V	
17		I_{AL}	Address Input Current, Input Voltage Low			3	−0.002		−10	−30		−10	−30		V_{EN} = 2.4 V	All V_A = 0
18						1	−0.002		−10	−30		−10	−30		V_{EN} = 0	
19	DYNAMIC	$t_{transition}$	Switching Time of Multiplexer		D	1	0.6		1					μs	See Figure 1	
20		t_{open}	Break-Before-Make Interval		D		0.2								See Figure 3	
21		$t_{on(EN)}$	Enable Turn-ON Time		D	1	1.0		1.5						See Figure 2	
22		$t_{off(EN)}$	Enable Turn-OFF Time		D	1	0.4		1							
23		OIRR	OFF Isolation (Note 3)		D		68							dB	V_{EN} = 0, R_L = 1K Ω, C_L = 15 pF, V_S = 7 VRMS, f = 500 KHz	
24		$C_{S(off)}$	Source OFF Capacitance		S	16	6								V_S = 0	V_{EN} = 0, f = 140 KHz
25		$C_{D(off)}$	Drain OFF Capacitance	DG506A	D	1	45							pF	V_D = 0	
26				DG507A		2	23									
27	SUP	I_+	Positive Supply Current		V+		1.3		2.4			2.4		mA	V_{EN} = 0 V or 5 V	All V_A = 0
28		I_-	Negative Supply Current		V−		−0.7		−1.5			−1.5				

DG506A ICMH-A
DG507A ICMH-B

NOTES:

1. Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
2. $I_{D(on)}$ is leakage from driver into "ON" switch.
3. OFF position = 20 log $\frac{V_D}{V_S}$, V_S = input to "OFF" switch, V_D = output due to V_S.
4. Functional operation is possible for supply voltages less than 15 V, but the input logic threshold will shift.
5. Signals on S_X, D_X or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

See Product Selector Guides on Pages 2779-2783.

8-Channel/Dual 4-Channel CMOS Analog Multiplexer

Siliconix

designed for...

- **Data Acquisition Systems**
- **Multiplexing Reference Signals**
- **Communication Systems**

BENEFITS

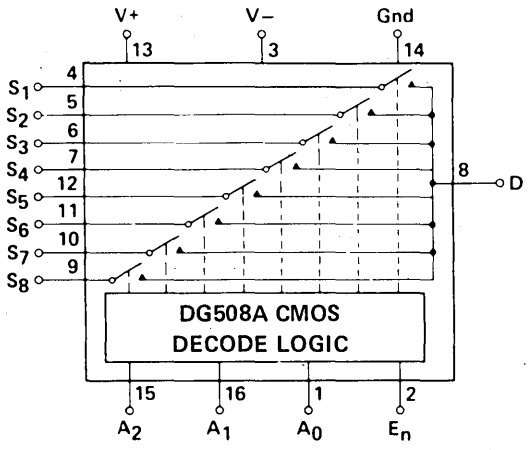
- **Easily Interfaced**
  - TTL, DTL and CMOS Direct Control Over Military Temperature Range
- **Low Power**
  - 30 mW Typical Quiescent Power
- **Reduces System Cross-Talk**
  - Break-Before-Make Switching Action
- **Environmentally Rugged**
  - Latchproof PLUS-40 CMOS
  - 44V Power Supply Maximum Rating
  - Static Protection Circuitry on all Inputs

DESCRIPTION

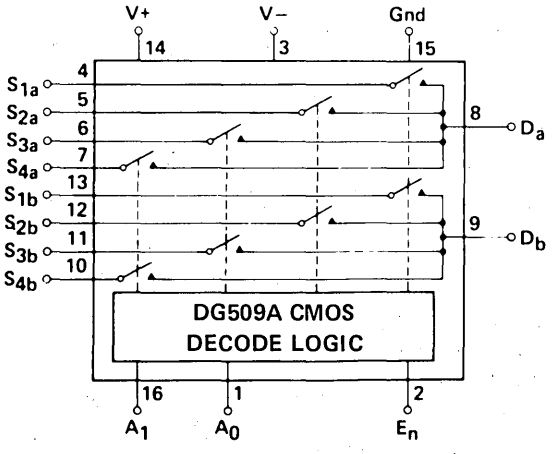
The DG508A a single ended 8 channel analog multiplexer connects 1 of 8 inputs to a common output decoded from 3 binary inputs (A_0, A_1, A_2).

The DG509A a differential input 4 channel analog multiplexer connects 1 of 4 differential inputs to a common differential output decoded from 2 binary inputs (A_0, A_1). In the ON state each switch conducts current in either direction, and in the OFF state blocks voltage up to the power supply rails, generally 30 volts peak-to-peak. Bidirectional current switching also insures equal operation as a demultiplexer. An enable (E_n) input provides a package select function. All control inputs address (A_x) and enable (E_n) are TTL or CMOS compatible over the full operating temperature range of the product. The multiplexers operate in a Break-Before-Make (BBM) switch action between any two decoded switch selections protecting against momentary shorting of the input transducers. Additionally BBM action occurs between package selection. See the DG528 and DG529 for the same function plus latches on the A_2, A_1, A_0, E_n inputs.

FUNCTIONAL DIAGRAMS



DG508A
8 Channel Single Ended Multiplexer



DG509A
Differential 4 Channel Multiplexer

ABSOLUTE MAXIMUM RATINGS

Voltages referenced to V–

V+ . . . . . 44 V
GND . . . . . 25 V
Digital inputs[4], V_S, V_D . . . . . –2 V to (V^+ +2 V) or 20 mA, whichever occurs first.

Current (Any Terminal, Except S or D) . . . 30 mA
Continuous Current, S or D . . . . . 20 mA
Peak Current, S or D
(Pulsed at 1 msec, 10% Duty Cycle Max) . . 40 mA
Operating Temperature (A Suffix) . . . –55 to 125°C
(B Suffix) . . . –20 to 85°C
(C Suffix) . . . 0 to 70°C

Storage Temperature (A & B Suffix) . . –65 to 150°C
(C Suffix) . . . –65 to 125°C
Power Dissipation (Package)*
16 Pin DIP** . . . . . 900 mW
16 Pin Plastic DIP*** . . . . . 470 mW
Flat Package**** . . . . . 750 mW

*All leads soldered or welded to PC board.
**Derate 12 mW/°C above 75°C
***Derate 6.3 mW/°C above 25°C
****Derate 10 mW/°C above 75°C

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		CHARACTERISTIC		MEASURED TERMINAL	NO. TESTS PER TEMP.	TYP[1] 25°C	MAX LIMITS A SUFFIX –55°C	A SUFFIX 25°C	A SUFFIX 125°C	B/C SUFFIXES –20/0 C	B/C SUFFIXES 25°C	B/C SUFFIXES 85/70°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V– = 15 V, Ground = 0	
1		V_{ANALOG}	Minimum Analog Signal Handling Capability			±15		±15	±15		±15	±15	V		
2		$r_{DS(on)}$	Drain-Source ON-Resistance	S to D	8	270	400	400	500	450	450	550	Ω	V_D = 10 V, I_S = –200 µA	Sequence each switch on V_{AL} = 0.8 V, V_{AH} = 2.4 V
3					8	230	400	400	500	450	450	500		V_D = –10 V, I_S = –200 µA	
4		$\Delta r_{DS(on)}$	Greatest Change in Drain Source ON Resistance Between Channels	S to D	8	6							%	$\Delta r_{DS(on)} = \left(\frac{r_{DS(on)\ MAX} - r_{DS(on)\ MIN}}{r_{DS(on)\ AVE}}\right)$ –10 V ≤ V_S ≤ 10 V	
5	SWITCH	$I_{S(off)}$	Source OFF Leakage Current	S	8	0.002		±1	±50		±5	±50	nA	V_S = 10 V, V_D = –10 V	V_{EN} = 0
6					8	–0.005		±1	±50		±5	±50		V_S = –10 V, V_D = 10 V	
7		$I_{D(off)}$	Drain OFF Leakage Current DG508A	D	1	0.010		±10	±200		±20	±200		V_D = 10 V, V_S = –10 V	
8					1	–0.015		±10	±200		±20	±200		V_D = –10V, V_S = 10 V	
9			DG509A		2	0.005		±10	±100		±20	±100		V_D = 10 V, V_S = –10 V	
10					2	–0.008		±10	±100		±20	±100		V_D = –10 V, V_S = 10 V	
11		$I_{D(on)}$[2]	Drain ON Leakage Current DG508A	D	8	0.015		±10	±200		±20	±200		$V_{S(all)}$ = V_D = 10 V	Sequence each switch on V_{AL} = 0.8 V, V_{AH} = 2.4 V
12					8	–0.030		±10	±200		±20	±200		$V_{S(all)}$ = V_D = –10 V	
13			DG509A		8	0.007		±10	±100		±20	±100		$V_{S(all)}$ = V_D = 10 V	
14					8	–0.015		±10	±100		±20	±100		$V_{S(all)}$ = V_D = –10 V	
15	INPUT	I_{AH}	Address Input Current Input Voltage High	A_0, A_1, (A_2), EN	(4) 3	–0.002		±10	–30		–10	–30	µA	V_A = 2.4 V	
16					(4) 3	0.006		10	30		10	30		V_A = 15 V	
17		I_{AL}	Address Input Current Input Voltage Low		(3) 2	–0.002		–10	–30		–10	–30		V_{EN} = 2.4 V	All V_A = 0
18					1	–0.002		–10	–30		–10	–30		V_{EN} = 0	
19	DYNAMIC	$t_{transition}$	Switching Time of Multiplexer	D	1	0.6		1					µs	See Figure 1	
20		t_{open}	Break-Before-Make Interval	D		0.2								See Figure 3	
21		$t_{on(EN)}$	Enable Turn-ON Time	D	1	1.0		1.5						See Figure 2	
22		$t_{off(EN)}$	Enable Turn-OFF Time	D	1	0.4		1							
23		OIRR	OFF Isolation (Note 3)	D	8	68							dB	V_{EN} = 0, R_L = 1K Ω, C_L = 15 pF V_S = 7 VRMS, f = 500 kHz	
24		$C_{S(off)}$	Source OFF Capacitance	S	8	5							pF	V_S = 0	V_{EN} = 0, f = 140 kHz
25		$C_{D(off)}$	Drain OFF Capacitance DG508A	D	1	25								V_D = 0	
26			DG509A	D	2	12									
27	SUPPLY	I+	Positive Supply Current	V+	1	1.3		2.4			2.4		mA	V_{EN} = 2.4 V	All V_A = 0, or 2.4 V
28		I–	Negative Supply Current	V–	1	–0.7		–1.5			–1.5				
29		I+ Standby	Positive Supply Current	V+	1	1.3		2.4			2.4			V_{EN} = 0 V	
30		I– Standby	Negative Supply Current	V–	1	–0.7		–1.5			–1.5				

NOTES:

1. Typical Values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
2. $I_{D(on)}$ is leakage from driver into "ON" switch.
3. OFF isolation = 20 log $\frac{|V_S|}{|V_D|}$, V_S = input to "OFF" switch, V_D = output due to V_S.
4. Signals on S_X, D_X or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

ICMG-A DG508A
ICMG-B DG509A

8-Channel and Dual 4-Channel Latchable Multiplexers

designed for . . .

- **Data Acquisition Systems**
- **Automatic Test Equipment**
- **Communication Systems**
- **Microprocessor Controlled Systems**

BENEFITS

Siliconix

- **Microprocessor Bus Compatible**
  - Accepts 300 nsec WRITE Pulse Width
  - Direct RESET
- **Environmentally Rugged**
  - 44V Power Supply Rating
  - Static Protected Logic Inputs
  - Latch-Proof
- **Easily Interfaced**
  - TTL Compatible Without Pullup Resistors V_{INH} = 2.4V
- **Improved System Accuracy**
  - $r_{DS(on)}$ <400Ω
  - V_{error} = 80 μ V Max at 125°C = $I_{D(on)} \times r_{DS(on)}$
  - $\Delta r_{DS(on)}$ Channel to Channel is Less Than 6%

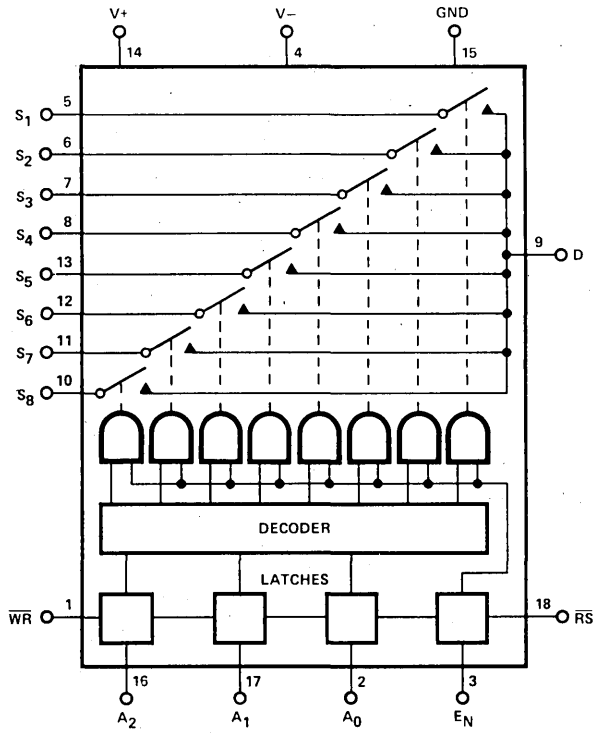
DESCRIPTION

The DG528 and DG529 designed on the Siliconix PLUS-40 CMOS Process provides solid state switch action with 400 ohms contact (ON) resistance and very high OFF resistance. True bidirectional switch action takes place over the full analog signal range of ±15 volts, with break-before-make operation to prevent momentary shorting of signal inputs. The DG528 provides 8-channel single-ended multiplexing and demultiplexing of ±15 volt analog signals. The DG529 provides 4-channel differential multiplexing and demultiplexing of ±15 volt common mode plus differential mode signals.

Four input latches on the binary coded switch-state inputs (A_0, A_1, A_2, E_n) result in microprocessor bus compatibility. Two control lines, $\overline{WR}$ and $\overline{RS}$, store or clear the the switch-state input (A_0, A_1, A_2, E_n) latches. Programming the enable input (E_n) latch with a logic zero turns all analog switches OFF. The direct chip reset $\overline{RS}$ simplifies switch turn OFF during system power up or system reset.

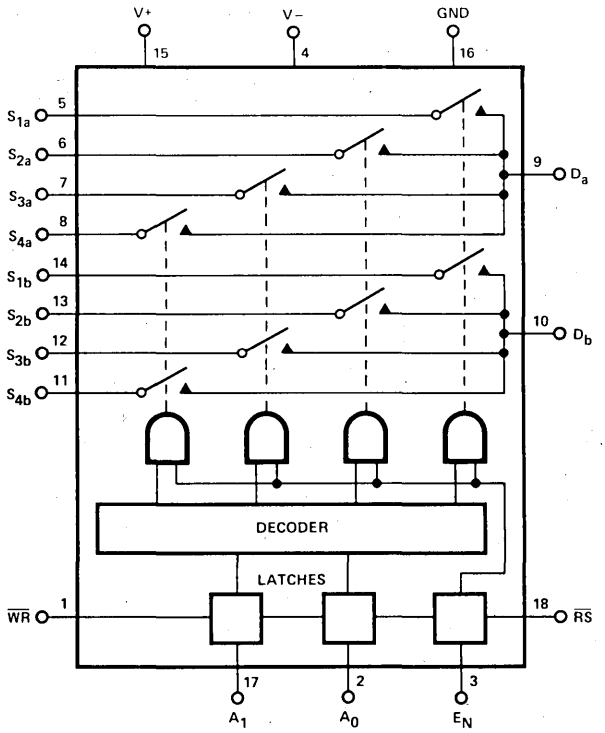
FUNCTIONAL DIAGRAMS

DG528



8 Channel Single Ended Multiplexer

DG529

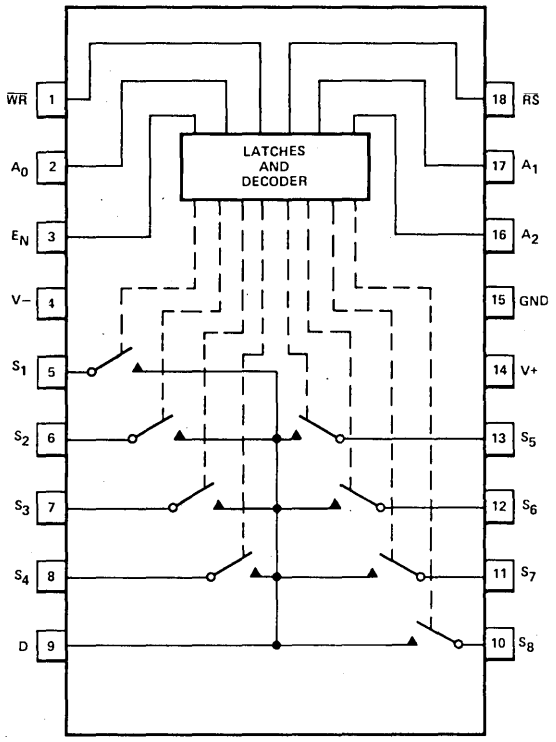


Differential 4 Channel Multiplexer

PIN CONFIGURATIONS

DG528

Dual–In–Line Package

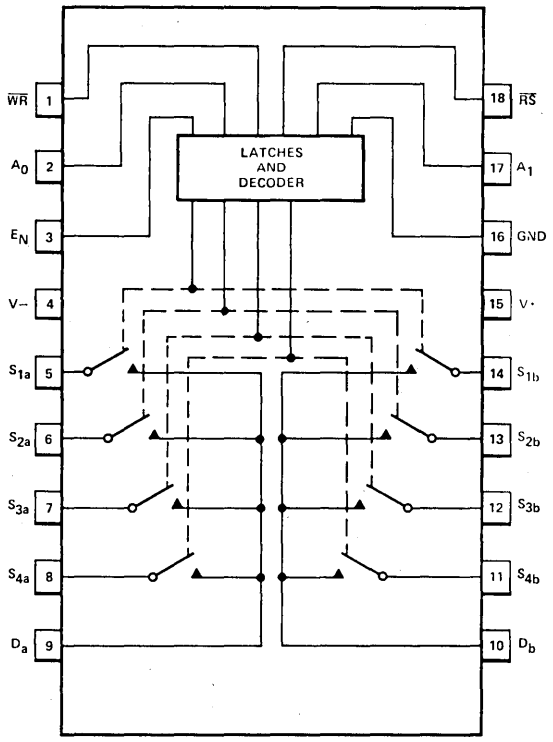


Top View

ORDER NUMBERS:
DG528AK OR DG528BK
SEE PACKAGE 23
DG528CJ
SEE PACKAGE 19

DG529

Dual–In–Line Package



Top View

ORDER NUMBERS:
DG529AK OR DG529BK
SEE PACKAGE 23
DG529CJ
SEE PACKAGE 19

TRUTH TABLES

DG528

A_2	A_1	A_0	E_n	$\overline{WR}$	$\overline{RS}$	On Switch
X	X	X	X	↓	1	Maintains previous switch condition
X	X	X	X	X	0	NONE (latches cleared)
X	X	X	0	0	1	NONE
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

DG529

A_1	A_0	E_n	$\overline{WR}$	$\overline{RS}$	On Switch
X	X	X	↓	1	Maintains previous switch condition
X	X	X	X	0	NONE (latches cleared)
X	X	0	0	1	NONE
0	0	1	0	1	1
0	1	1	0	1	2
1	0	1	0	1	3
1	1	1	0	1	4

Logic "1": $V_{AH} \geq 2.4V$
Logic "0": $V_{AL} \leq 0.8V$

See Product Selector Guides on Pages 2779-2783.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Voltages referenced to V–

V+ . . . . . 44 V
GND . . . . . 25 V
Digital inputs[5], V_S, V_D . . . . . –2 V to (V^+ +2 V) or 20 mA, whichever occurs first.

Current (Any Terminal Except S or D) . . . . 30 mA
Continuous Current, S or D . . . . . 20 mA
Peak Current, S or D
(Pulsed at 1 msec, 10% Duty Cycle Max) . 40 mA

Operating Temperature (A Suffix) –55 to 125°C
(B Suffix) –20 to 85°C
(C Suffix) 0 to 70°C
Storage Temperature (A & B Suffix) –65 to 150°C
(C Suffix) –65 to 125°C
Power Dissipation (Package)*
18 Pin DIP** . . . . . 900 mW
18 Pin Plastic DIP*** . . . . . 470 mW

*All leads soldered or welded to PC board.
**Derate 12 mW/°C above 75°C.
***Derate 6.3 mW/°C above 50°C

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample–tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		Characteristic		Measured Terminal	No. Tests Per Temp.	Typ 25°C Note 1	Max Limits A Suffix -55°C	A Suffix 25°C	A Suffix 125°C	B/C Suffixes -20°C 0°C	B/C Suffixes 25°C	B/C Suffixes 85°C	Unit	Test Conditions, Unless Noted: V+ = 15, V– = –15, Ground = 0, $\overline{WR}$ = 0, $\overline{RS}$ = 2.4V
1		V_{ANALOG}	Minimum Analog Signal Handling Capability			±15		±15	±15		±15	±15	V	
2	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	S to D	8	270	400	400	500	450	450	550	Ω	V_D = 10V, I_S = -200 µA; Sequence each switch on, V_{AL} = 0.8V, V_{AH} = 2.4V
3					8	230	400	400	500	450	450	500		V_D = -10V, I_S = -200 µA
4		$\Delta r_{DS(on)}$	Greatest Change in Drain Source ON Resistance Between Channels	S to D	8	6							%	$\Delta r_{DS(on)} = \left(\frac{r_{DS(on)}^{MAX} - r_{DS(on)}^{MIN}}{r_{DS(on)}^{AVE}}\right)$, -10V ≤ V_S ≤ 10V
5		$I_{S(off)}$	Source OFF Leakage Current	S	8	-0.005		±1	±50		±5	±50	nA	V_S = 10V, V_D = -10V
6					8	-0.005		±1	±50		±5	±50		V_S = -10V, V_D = 10V
7		$I_{D(off)}$	Drain OFF Leakage Current, DG528	D	1	-0.015		±10	±200		±20	±200		V_D = 10V, V_S = -10V; V_{EN} = 0
8					1	-0.015		±10	±200		±20	±200		V_D = -10V, V_S = 10V
9			DG529		2	-0.008		±10	±100		±20	±100		V_D = 10V, V_S = -10V
10					2	-0.008		±10	±100		±20	±100		V_D = -10, V_S = 10V
11		$I_{D(on)}$	Drain ON Leakage Current Note 2, DG528	D	8	-0.03		±10	±200		±20	±200		$V_{S(all)}$ = V_D = 10V; Sequence each switch on, V_{AL} = 0.8V, V_{AH} = 2.4V
12					8	-0.03		±10	±200		±20	±200		$V_{S(all)}$ = V_D = -10V
13			DG529		8	-0.015		±10	±100		±20	±100		$V_{S(all)}$ = V_D = 10V
14					8	-0.015		±10	±100		±20	±100		$V_{S(all)}$ = V_D = -10V
15	INPUT	I_{AH}	Logic Input Current, Input Voltage High	A_0, A_1, (A_2), E_n, $\overline{WR}$, $\overline{RS}$	5 (6)	-0.002		±10	-30		-10	-30	µA	V_A = 2.4V
16					5 (6)	0.006		10	30		10	30		V_A = 15V
17		I_{AL}	Logic Input Current, Input Voltage Low		5 (6)	-0.002		-10	-30		-10	-30		V_{EN} = 0; All V_A = 0, $\overline{WR}$ = 0, $\overline{RS}$ = 0
18		$t_{transition}$	Switching Time of Multiplexer	D	1	0.6		1					µs	See Figure 3
19		t_{open}	Break-Before-Make Interval	D		0.2								See Figure 5
20	DYNAMIC	t_{on}(EN, $\overline{WR}$)	Enable Turn-ON Time	D	1	1.0		1						See Figures 4 and 6
21		t_{off}(EN, $\overline{RS}$)	Enable and RS Reset Turn-OFF Time	D	1	0.4		1						See Figure 4 and 7
22		Q	Charge Coupling	D		4.0							pC	See Figure 8
23		OFF Isolation	Note 3	D	8	68							dB	V_{EN} = 0, R_L = 1KΩ, C_L = 15 pF, V_S = 7 VRMS, f = 500 kHz
24		C_{in}	Logic Input Capacitance	A_0, A_1, (A_2) E_n, $\overline{WR}$, $\overline{RS}$		2.5							pF	f = 1 MHz
25	SUPPLY	$C_{S(off)}$	Source OFF Capacitance	S	8	5								V_S = 0; V_{EN} = 0, f = 140 kHz
26		$C_{D(off)}$	Drain OFF Capacitance, DG528	D	1	25								V_D = 0
27			DG529	D	2	12								
28		I+	Positive Supply Current	V+	1			2.5			2.5		mA	V_{EN} = 0V; All V_A = 0
29		I-	Negative Supply Current	V-	1			-1.5			-1.5			

NOTES:
1. Typical Values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
2. $I_{D(on)}$ is leakage from driver into "ON" switch.
3. OFF isolation=20 log $\frac{V_S}{V_D}$, V_S=input to "OFF" switch, V_D= output due to V_S.
4. Period of Reset ($\overline{RS}$) pulse must be at least 50 µsec during or after power ON.
5. Signals on S_X, D_X or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

ICML–A DG528
ICML–B DG529

TIMING DIAGRAMS

Minimum Input Timing Requirements

	Parameter	Measured Terminal	Min Limits over full temp range	Unit	Test Circuit
30	t_{WW} WRITE Pulse Width	$\overline{WR}$	300	ns	See Figure 1
31	t_{DW} A, E_n Data Valid to WRITE (Stabilization Time)	A_0, A_1, (A_2), E_n $\overline{WR}$	180		
32	t_{WD} A, E_n Data Valid after WRITE (Hold Time)	$\overline{WR}$ A_0, A_1, (A_2), E_n	30		
33	$t_{\overline{RS}}$ RESET Pulse Width Note 4	$\overline{RS}$	500		See Figure 2 V_S = 5V

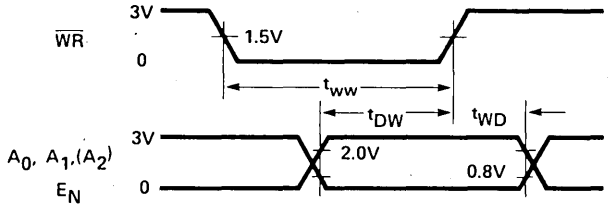


Figure 1.

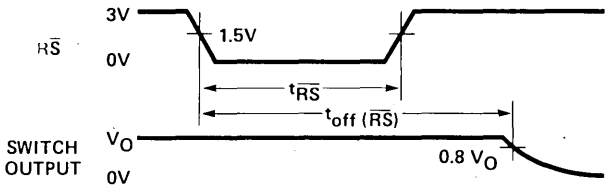
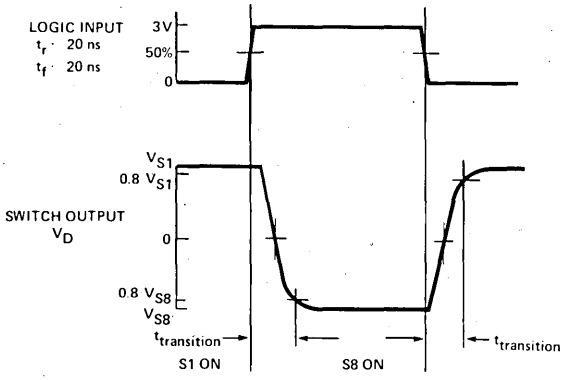
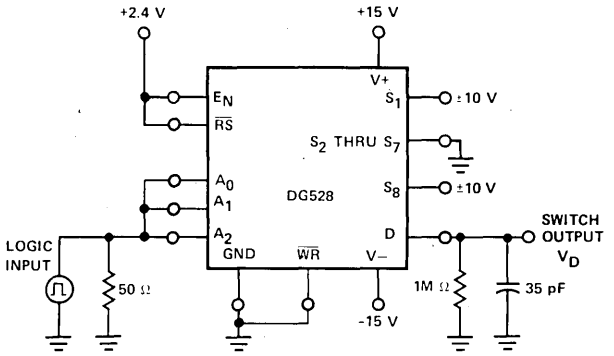


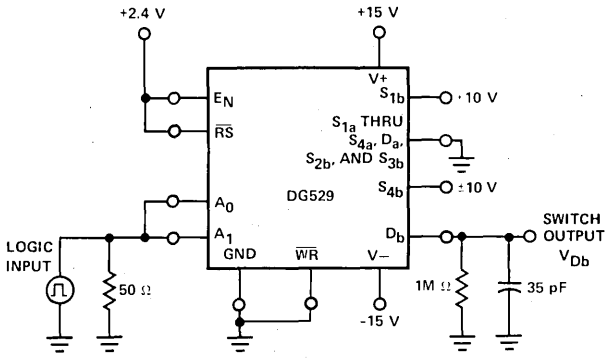
Figure 2.

SWITCHING TIME TEST CIRCUITS





(a)

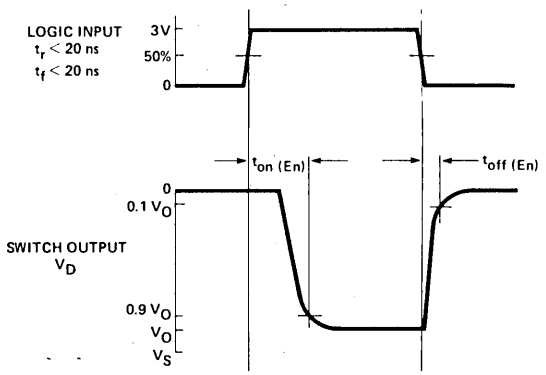


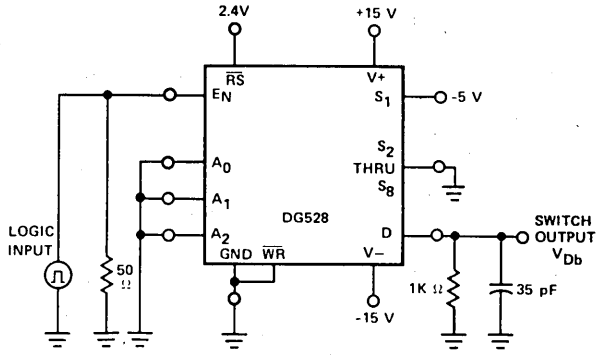
(b)

Figure 3. Transition Time Test Circuit

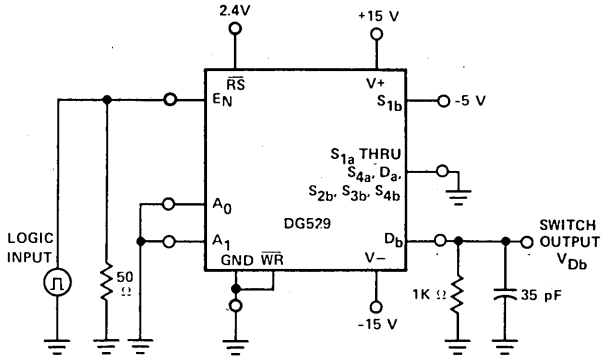
See Product Selector Guides on Pages 2779-2783.

SWITCHING TIME TEST CIRCUITS (Cont'd)



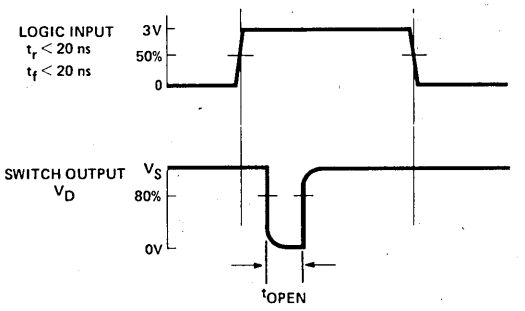


(a)



(b)

Figure 4. Enable t_{on}/t_{off} Time



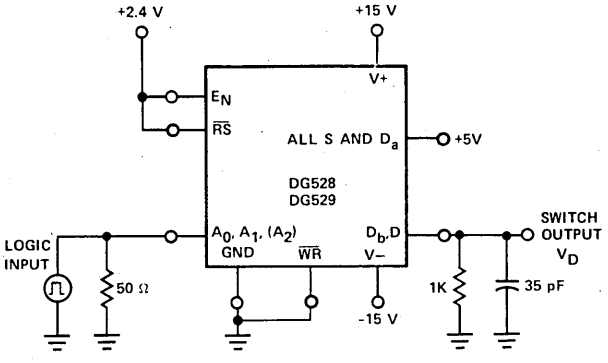


Figure 5. Open Time (B.B.M. Interval)

SWITCHING TIME TEST CIRCUITS (Cont'd)

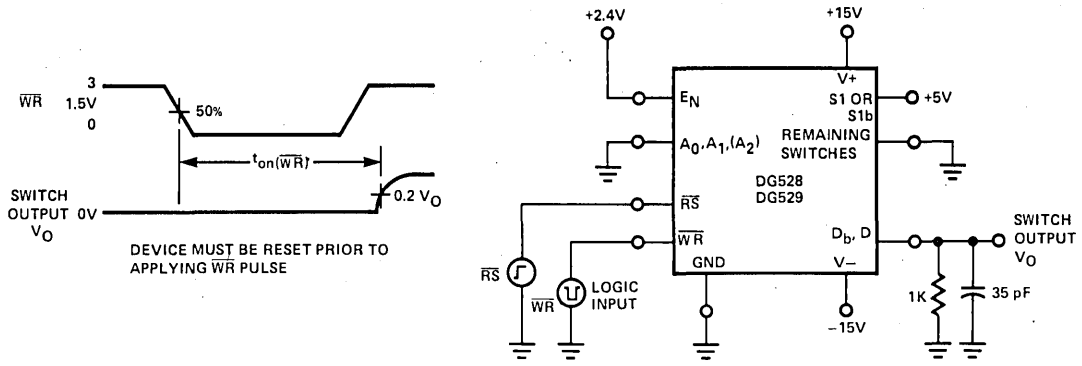


Figure 6. Write Turn-On Time $t_{on(\overline{WR})}$

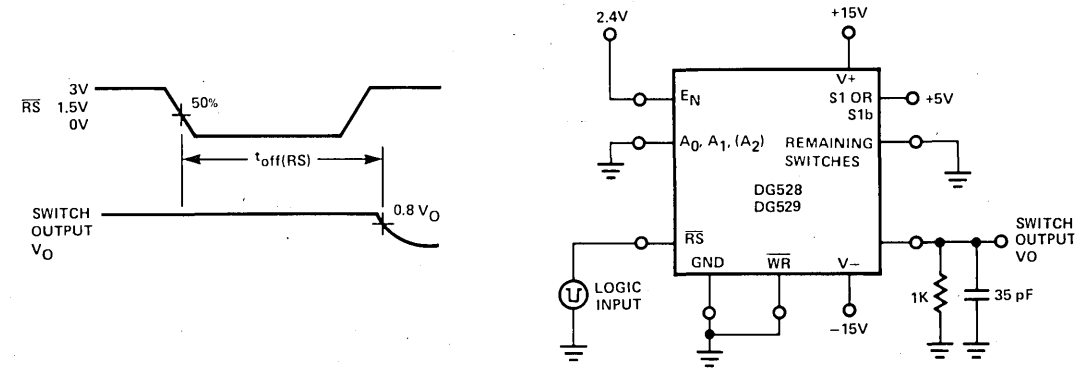


Figure 7. Reset Turn-Off Time $t_{off(\overline{RS})}$

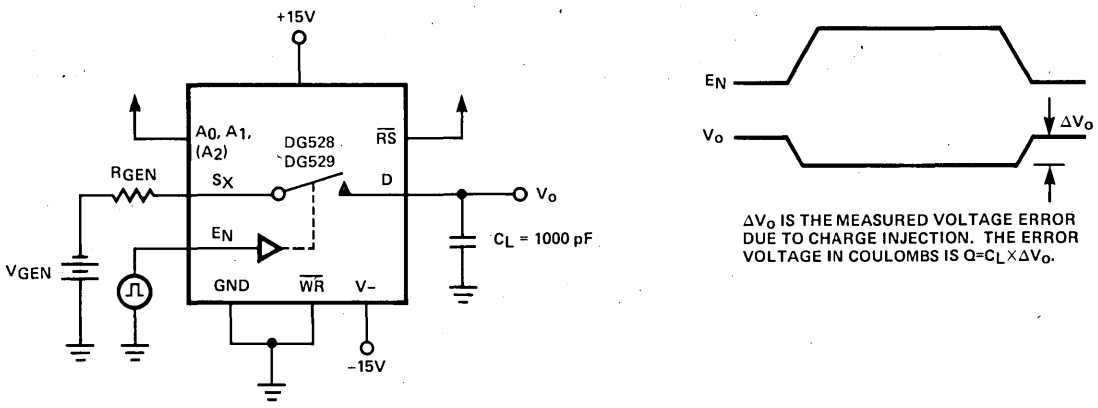


Figure 8. Charge Injection Test Circuit

See Product Selector Guides on Pages 2779-2783.

DETAILED DESCRIPTION

The internal structure of the DG528 and DG529 provides a 5 volt logic interface with input protection circuitry followed by a latch, level shifter, decoder and finally the switch constructed with parallel N and P channel MOSFETs (see figure 9).

Looking at figure 9, the input protection on the logic lines A_0, A_1, A_2, E_n and control lines $\overline{WR}$, $\overline{RS}$ minimize susceptibility to static encountered during handling and operational transients.

The logic interface circuit compares the TTL input signal against a TTL threshold reference voltage. The output of the comparator feeds the data input of a D-type latch. The level sensitive D latch continuously places the D_X input signal on the Q_X output when the CLK ($\overline{WR}$) input is low, resulting in transparent operation. As soon as CLK ($\overline{WR}$) returns high the latch holds the data last present on the D_X input at the Q_X output, subject to the "Minimum Input Timing Requirements" table.

Following the latches the Q_X signals are level shifted and decoded to provide proper drive levels for the CMOS switches. This level shifting insures full ON/OFF switch operation for any analog signal present between the V+ and V- supply pins.

Power Supplies

The final data sheet will provide graphs showing the effect on power supply sensitive parameters.

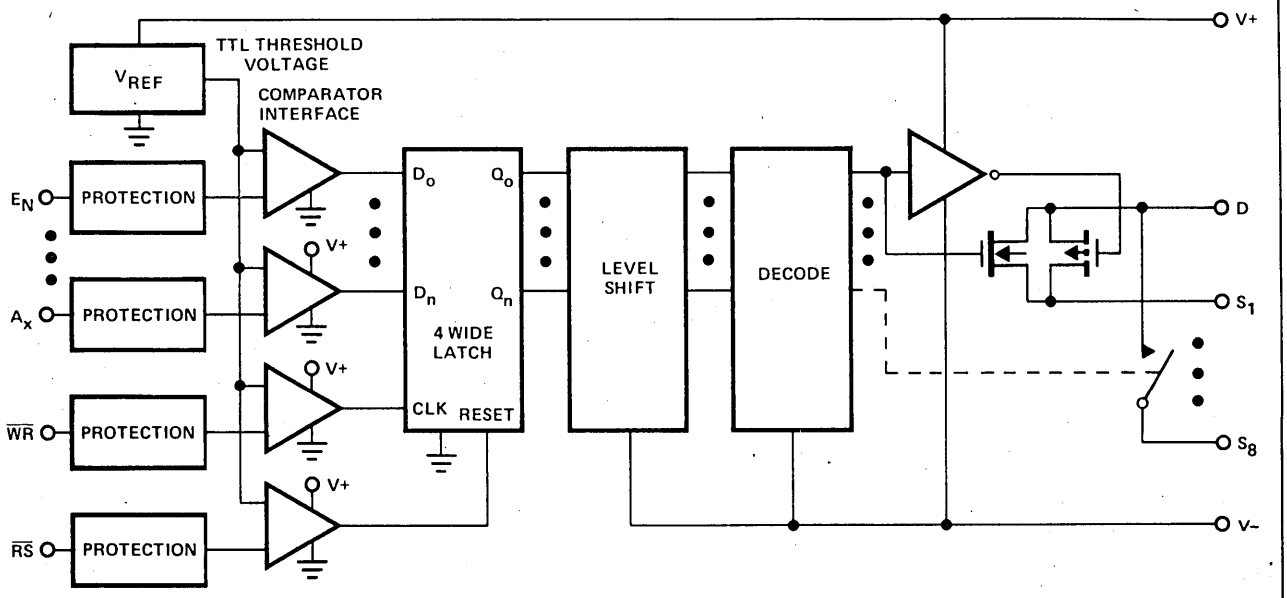


Figure 9. DG528 Simplified Internal Structure

DG5040–45 Series General Purpose CMOS Analog Switches

Siliconix
Revised 3/82

designed for . . .

- **Programmable Gain Amplifiers**
- **Analog Multiplexing**
- **Servo Control Switching**
- **Sampled Data Systems**
- **Synchronous Demodulators**

BENEFITS

- **Environmentally Rugged**
  - 44V Power Supply Rating
  - Static Protected Logic Inputs
  - Latchproof
- **Easily Interfaced**
  - TTL and CMOS Compatible without Pull Up Resistors
- **Reduces External Component Requirements**
  - Full Rail to Rail Analog Signal Range
  - No Diode Protection Required Between V_L and V+ for Power Supply Sequencing
- **Pin for Pin Compatible with**
  - IH5040 Family
  - HI5040 Family

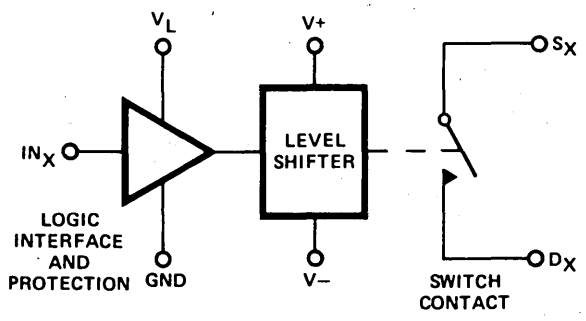
DESCRIPTION

The DG5040 through DG4045 series designed on the Siliconix PLUS-40 CMOS process provides solid state switch action with 50 ohms contact resistance and very high OFF resistance. True switch action takes place over the full analog signal range of ±15 volts, with Break-Before-Make operation to prevent momentary shorting of signal inputs.

FUNCTIONAL DESCRIPTION

PART NUMBER	TYPE	
DG5040		SPST
DG5041	Dual	SPST
DG5042		SPDT
DG5043	Dual	SPDT
DG5044		DPST
DG5045	Dual	DPST

FUNCTIONAL DIAGRAM (typical channel)



See Product Selector Guides on Pages 2779-2783.

ABSOLUTE MAXIMUM RATINGS (T_A = 25° unless otherwise noted)

Voltages referenced to V–

V+ . . . . . 44 V
V_L . . . . . (GND –0.3 V) to 44 V
GND . . . . . 25 V
Digital inputs[5], V_S, V_D . . . . . –2 V to (V^+ +2 V) or 30 mA, whichever occurs first.
Current, Any Terminal Except S or D . . . . . 30 mA
Continuous Current, S or D . . . . . 30 mA
Peak Current, S or D (pulsed at 1 msec, 10% duty cycle max) . . . . . 100 mA
Storage Temperature (A Suffix) –65 to 150°C
(C Suffix) –65 to 125°C
Operating Temperature (A Suffix) –55 to 125°C
(C Suffix) 0 to 70°C
Power Dissipation*
Metal Can and Plastic DIP** . . . . . 450 mW
16 Pin DIP**** . . . . . 900 mW
Flat Pak***** . . . . . 900 mW

*All leads welded or soldered to PC board.
**Derate 6 mW/°C above 75°C.
****Derate 12 mW/°C above 75°C.
*****Derate 10 mW/°C above 75°C.

Stresses listed under "Absolute Maximum Ratings" may be applied (one at a time) to devices without resulting in permanent damage. This is a stress rating only and not subject to production testing. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		Characteristics		Max Limits A Suffix –55°C	25°C	125°C	C Suffix 0°C	25°C	70°C	Unit	Test Conditions V+ = 15V, V– = –15V, V_L = 5V, GND = 0V	
1		V_{ANALOG}	Min. Analog Signal Handling Capability		±15	±15		±15	±15	V		
2	SWITCH	$r_{DS(on)}$[3]	Drain Source ON Resistance	50	50	75	50	50	75	Ω	V_D = 10V, I_S = –10 mA	Note 1
3				50	50	75	50	50	75		V_D = –10V, I_S = –10 mA	
4		$I_{S(off)}$[3]	Source OFF Leakage Current		1	100		1	100	nA	V_S = 14V, V_D = –14V	
5					–1	–100		–1	–100		V_S = –14V, V_D = 14V	
6		$I_{D(off)}$[3]	Drain OFF Leakage Current		1	100		1	100		V_S = –14V, V_D = 14V	
7					–1	–100		–1	–100		V_S = 14V, V_D = –14V	
8		$I_{D(on)}$[3]	Drain ON Leakage Current		2	200		2	200		V_S = V_D = 14V	
9					–2	–200		–2	–200		V_S = V_D = –14V	
10	INPUT	I_{INH}[3]	Input Current, Input Voltage High		±1	±1		±1	±1	µA	V_{INH} = 2.0V	
11		I_{INL}[3]	Input Current, Input Voltage Low		±1	±1		±1	±1		V_{INL} = 0.8V	
12	DYNAMIC	t_{on}[4]	Turn-ON Time		1000			1200		ns	V_S = ±10V, R_L = 1KΩ, C_L = 35 pF	Note 2
13		t_{off}[4]	Turn-OFF Time		500			700				
14		Q	Charge Injection	3 Typical						mV	C_L = 10,000 pF, R_{GEN} = 0Ω, V_{GEN} = 0V	
15		$C_{S(off)}$	Source OFF Capacitance	15 Typical						pF	V_S = V_D = 0V, f = 1 MHz	Note 1
16		$C_{D(off)}$	Drain OFF Capacitance	17 Typical								
17		$C_{D(on)}$ + $C_{S(on)}$	Channel ON Capacitance	45 Typical								
18		OIRR	OFF Isolation	75 Typical						dB	Z_L = 75Ω, V_S = 2 Vpp, f = 1 MHz	
19		CCRR	Interchannel Crosstalk Isolation	89 Typical								
20	SUPPLY	I_+[3]	Positive Supply Current	300	300	300	300	300	300	µA	V_{IN} = 0V or 2.4V	
21		I_-[3]	Negative Supply Current	–300	–300	–300	–300	–300	–300			
22		I_L[3]	Logic Supply Current	300	300	300	300	300	300			
23		I_{GND}	Ground Current	–300	–300	–300	–300	–300	–300			

ICMK–A, B

NOTES:

1: V_{IN} = Input voltage to perform proper function.
For Logic "1" — V_{INH} = 2.0 V
For Logic "0" — V_{INL} = 0.8 V

2: See Switching Time Test Circuit.

3: Limits of these paramaters are tested 100% at 25 °C and 125 °C for "883" devices.

4: For "883" devices these parameters are 100% tested at 25 °C.

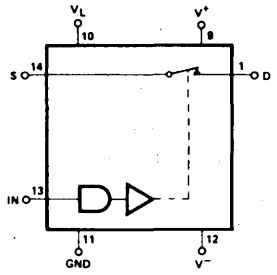
5: Signals on S_X, D_X or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

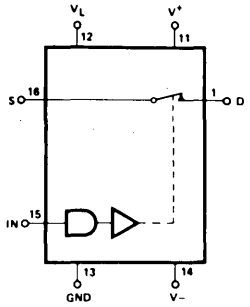
PIN CONFIGURATIONS

ALL SWITCHES SHOWN IN THE LOGIC "1" SWITCH STATE	FLAT PACK (L) SEE PACKAGE 5	CERDIP (K) OR PLASTIC (J) SEE PACKAGE 8 or 10	METAL CAN (A) SEE PACKAGE 2

SPST
DG5040

LOGIC	SWITCH
0	OFF
1	ON

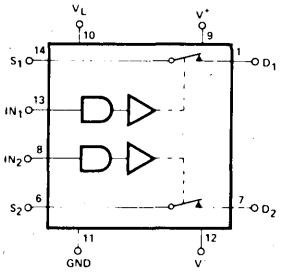


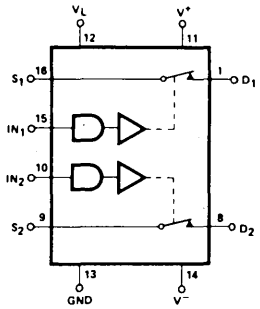


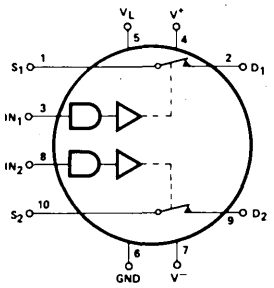
ORDER NUMBER: DG5040AL | DG5040AK or DG5040CK or DG5040CJ

DUAL SPST
DG5041

LOGIC	SWITCH
0	OFF
1	ON



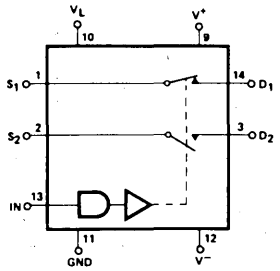


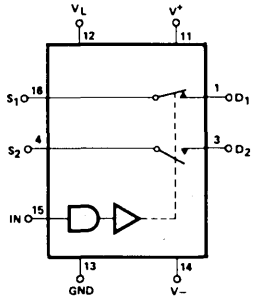


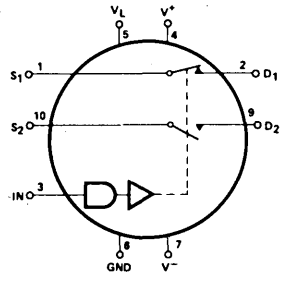
ORDER NUMBER: DG5041AL | DG5041AK or DG5041CK or DG5041CJ | DG5041AA

SPDT
DG5042

LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF







ORDER NUMBER: DG5042AL | DG5042AK or DG5042CK or DG5042CJ | DG5042AA

See Product Selector Guides on Pages 2779-2783.

PIN CONFIGURATIONS Continued

ALL SWITCHES SHOWN IN THE LOGIC "1" SWITCH STATE

FLAT PACK (L) SEE PACKAGE 5

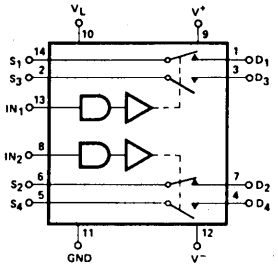
CERDIP (K) OR PLASTIC (J) SEE PACKAGE 8 or 10

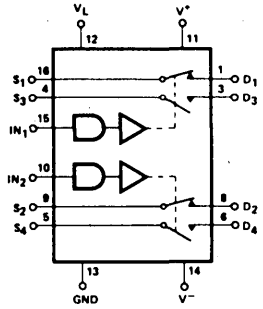
METAL CAN (A) SEE PACKAGE 2

DUAL SPDT DG5043

LOGIC	SW 1 SW 2	SW 3 SW 4
0	OFF	ON
1	ON	OFF

(DG191 EQUIVALENT)



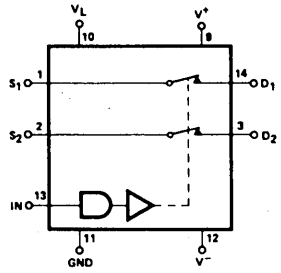


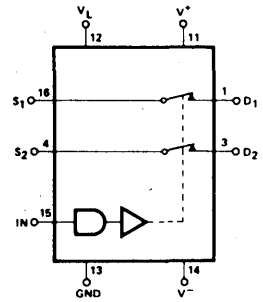
ORDER NUMBER: DG5043AL

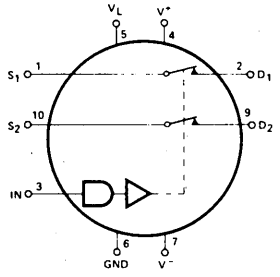
DG5043AK or DG5043CK or DG5043CJ

DPST DG5044

LOGIC	SWITCH
0	OFF
1	ON







ORDER NUMBER: DG5044AL

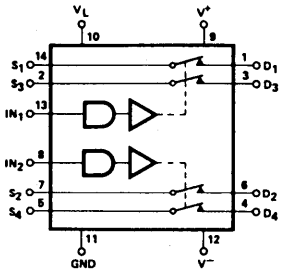
DG5044AK or DG5044CK or DG5044CJ

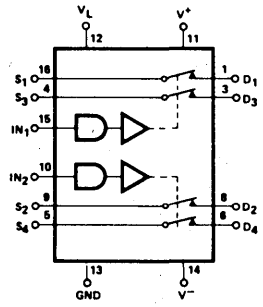
DG5044AA

DUAL DPST DG5045

LOGIC	SWITCH
0	OFF
1	ON

(DG185 EQUIVALENT)





ORDER NUMBER: DG5045AL

DG5045AK or DG5045CK or DG5045CJ

4½ digit A/D converter set *designed for . . .*

Siliconix

- **High Accuracy and High Resolution Digital Voltmeters, Panel Meters**
- **Digital Scales, Thermometers**
- **Microprocessor Data Acquisition Systems**
- **Scientific Instrumentation**

BENEFITS

- 0.005% ±1 Count Accuracy, Ensures High System Performance
- 1 μV Resolution for 20 mV Full Scale
- 28,500 Count Maximum for 142% Overrange
- Sample Rate from One to Five/Second
- Auto-Zero Cycle Nulls Out Internal and External Amplifier Offsets
- Auto-Polarity Operation with One Reference
- Multiplexed BCD Output for Easy Interface to Displays
- Two Overrange Outputs, Underrange Output, Blink Inhibit, and Convert-On-Command Capabilities Allow Easy Interface to External Circuitry and Microprocessors

DESCRIPTION

Replace LD121 with LD121A for New Designs

The LD122/LD121A 4½ digit A/D system uses Siliconix's proprietary "Quantized Feedback" (patent pending) conversion technique. Intrinsic features of this system are Auto-Polarity. Auto-zero and ratiometric operation. No critical components are required except for a stable voltage reference and a low noise op amp. The technique offers superior linearity, normal mode rejection, and stability due to the simultaneous integration of the unknown input and the reference voltages. Unlike other conversion techniques, the integrator output voltage never represents more than 100 counts, thus critical, high resolution performance is not required of either the integrator or comparator.

The LD122/LD121A combination extends system resolution beyond the 10 μV maximum available from the LD120/121A system. By adding a user selected low noise input gain amplifier, and appropriate input filter, any input resolution can be achieved. Otherwise functional operation is identical to the LD120/LD121A. Complete LD122/LD121A functional information may be obtained by consulting the LD120/LD121A data sheet. Also see AN80-8 and AN77-1 application notes.

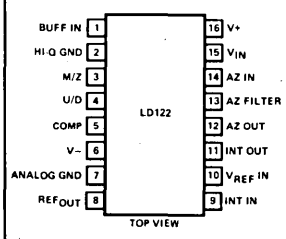
The LD122 analog processor is fabricated with a unique combined PMOS/Bipolar process. It contains all the necessary amplifiers, MOSFET switches, and switch driver circuits for the system. The reference voltage input is fully buffered on the LD122 to eliminate the reference switch resistance as a source of error. All the amplifiers are internally compensated. The LD122 directly interfaces the LD121A digital processor with no additional active components required.

The LD121A synchronous processor contains all the digital circuitry for the quantized feedback system. Device outputs supply two overrange signals, underrange, sign and 4½ digits of multiplexed BCD data. (All outputs are TTL compatible.) Overrange is also indicated by blinking digit strobes above 20,000 counts. An input is provided to inhibit this feature at user option. Microprocessor controlled operation is simplified by a start conversion input that allows conversion-on-command.

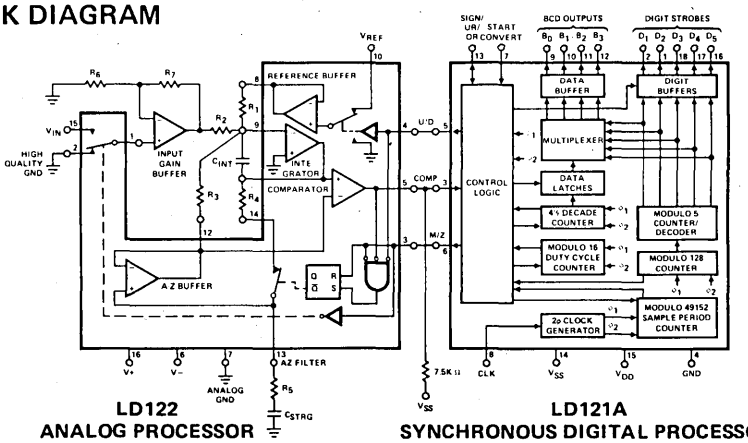
Both devices are supplied in space saving 300 mil dual-in-line packages. The LD122 has 16 pins and the LD121A has 18 pins.

FUNCTIONAL BLOCK DIAGRAM

Dual-In-Line Package



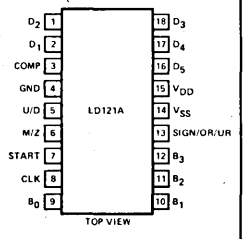
ORDER NO. LD122CJ
SEE PACKAGE 8



LD122
ANALOG PROCESSOR

LD121A
SYNCHRONOUS DIGITAL PROCESSOR

Dual-In-Line Package



ORDER NO. LD121ACJ
SEE PACKAGE 19

SWITCH STATES ARE FOR A LOGIC "O" AT U/D AND M/Z INPUTS

See Product Selector Guides on Pages 2779-2783.

ABSOLUTE MAXIMUM RATINGS

V_{IN} (Pin 15, 2 LD122) . . . . . $V- < V_{IN} < V+$
$V+ - V^-$ (LD122) . . . . . 32 V
$V_{SS} - V_{DD}$ (LD121A) . . . . . 20 V
Any Pin (LD121A) . . . . . V_{DD} to V_{SS} ±0.3
V_{REF} . . . . . +V

Operating Temperature . . . . . 0 to 70°C
Storage Temperature . . . . . −65 to 125°C
Power Dissipation (Package)* . . . . . 750 mW

* Device mounted with all leads welded or soldered to PC Board. Derated 6.3 mW/°C above 25°C.

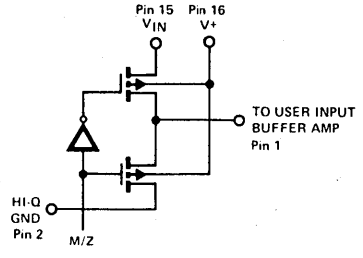
Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristic define the functional operating limits.

ELECTRICAL CHARACTERISTICS

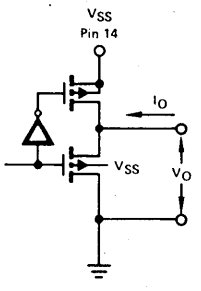
All DC parameters are 100% tested at 25°C. Lots are sample tested for AC parameters and high and low temperature limits to assure conformance with specifications.

				CHARACTERISTIC	MIN	TYP	MAX	UNITS	TEST CONDITIONS UNLESS NOTED OTHERWISE V+ = 12 V; V− = V_{DD} = −12 V, V_{SS} = 5 V, T_A = 25°C
1	SYSTEM (Notes 2 and 3)			Linearity	1	1/4	1	Count	2 V Scale
					2	1/2	2		200 mV Scale
2				Noise (Note 1)		1/3	1	Count	2 V Scale
						1/2	2		200 mV Scale
3			NMRR			40		dB	f_L = 50 or 60 Hz
			PSRR			80			
4				Gain T.C.		5	15	ppm/°C	
5				Zero Drift		1	5	Count	T_A = 25 to 75 °C, C_{STRG} = 1 µF, $R_{IN} \leq$ 100K Ω
6	LD121ACJ DIGITAL	POWER	V_{SS}		4.5	5	5.5	V	Range Over Which Functionality is Guaranteed
7			V_{DD}		−10.8	12	−13.2		
8			I_{SS}	(Note 4)		14	25	mA	
9			I_{DD}			−14	−25		
10		INPUTS	V_{INH}	Comparator Input, Sign/UR/OR/ Blink (Note 5), Start, CLK IN	4.0			V	Guaranteed Input Threshold Voltages
11			V_{INL}				0.5		
12			I_{INH}	Sign/OR/UR (Note 5)		170	300	µA	V_{IN} = 5 V
13			I_{INL}	Start Convert, Clock		−150	−400		V_{IN} = 0 V
14		OUTPUTS	V_{OH}	Bit Lines, Sign/OR/UR Digit Strobes	2.4			V	I_{OH} = −40 µA
15			V_{OL}				0.6		I_{OL} = 1.6 mA
16			V_{OH}	M/Z	4.0				I_{OH} = −150 µA
17			V_{OL}				0.6		I_{OL} = 0.8 mA
18			V_{OH}	U/D	4.0				I_{OH} = −0.5 mA
19			V_{OL}				0.6		I_{OL} = 0.8 mA
20		DYN	tp	Start Convert (Note 6)	20			µs	
21			f_{CLK}		50		250	kHz	50% Duty Cycle
22				Rep Rate (Strobes)	78		470	Hz	f_{CLK} : 640

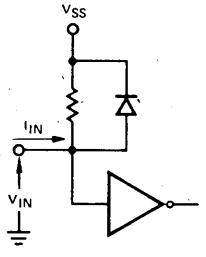
INPUT/OUTPUT SCHEMATICS



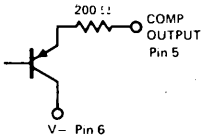
LD122 Input



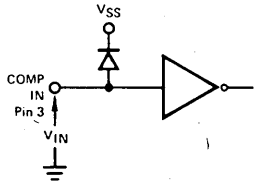
LD121A Output Buffers (Digits, Bits, Sign, M/Z U/D)



LD121A Clock Input Start Convert



LD122 Comparator Output



LD121A Comparator Input

ELECTRICAL CHARACTERISTICS (Cont'd)

			CHARACTERISTIC		MIN	TYP	MAX	UNITS	TEST CONDITIONS UNLESS NOTED OTHERWISE V+ = 12 V; V− = V_{DD} = −12 V, V_{SS} = 5 V, T_A = 25°C
23	LD122CJ LINEAR	POWER	V+		9	12	15	V	
24			V−		−9	−12	−15		
25			I+				3.5	mA	
26			I−				−3		
27			I_{GND}		0		−2	mA	M/Z, U/D = 2.4 V
28		INPUT SWITCH	V_A	(Note 7)	−3		+3	V	
29			$r_{DS(on)}$	On Resistance, V_{IN} or Hi-Q Switches			5.5	kΩ	V_A = +1 V
30							8.0		V_A = −1 V
31			$I_{LEAKAGE}$	Leakage Current, Switch ON or OFF		2		pA	V_A = ±2.8 V
32									
33									
34		AZ BUFF	I_{SOURCE}			−100		μA	
35			I_{SINK}			800			
36			I_{STRG}			100		pA	T_A = 70 C
37			V_{OFFSET}		−50		50	mV	V_{OUT} = 0 V
38				Switch Resistance (on) (Note 8)		6	20	kΩ	V_{STRG} = −4 V, I_{DS} = 30 μA
39		REF BUF	I_{SOURCE}	Pin 8	−400	−800		μA	V_{IL} (U/D IN), = 0.8 V, V_O = 0 V
40			I_{SINK}	Pin 8		100			V_{IH} (U/D IN) = 2.0 V, V_O = 2 V
41		INT	I_{SOURCE}	(Note 9)	−50	−100		μA	V_{IN} (Int. IN) = −100 mV, V_O = 0 V
42			I_{SINK}		400	800			V_{IN} (Int. IN) = 100 mV, V_O = 0 V
43				Output Swing	−10		10	V	
44		COMP	V_{OUT}		−5			V	R_L = 10k to +5 V, AZ FILTER IN = 100 mV
45			V_{OFFSET}			5		mV	INTEGRATOR OUT = 0 V
46			I_{IH}	M/Z, U/D Inputs			20	μA	V_{IH} = 2.0 V
47			I_{IL}				−100	μA	V_{IL} = 0.8 V

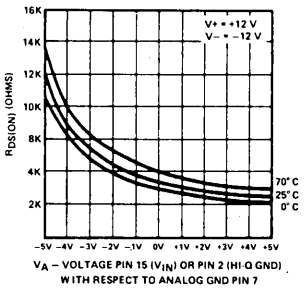
Typical values are for Design Aid Only, not guaranteed and not subject to production testing. LD122 - CMAM-C LD121A - IPDC VI

NOTES:

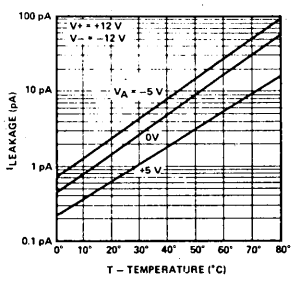
1. Bit width over which reading is stable 95% of the time.
2. System Parameters are not directly tested.
3. f_{CLK} = 163.84 kHz, V_{REF} = 6.8 V.
4. All outputs disconnected.
5. Pin characteristic only during D_4 strobe time.
6. Minimum positive going pulse width to initiate a conversion.
7. Maximum voltage range for V_{INPUT} (pin 1) or hi-quality GND (pin 2).
8. V_{STRG} must be more positive than −4 volts.
9. Reference Source Impedance must be less than 10K Ω.

TYPICAL CHARACTERISTICS

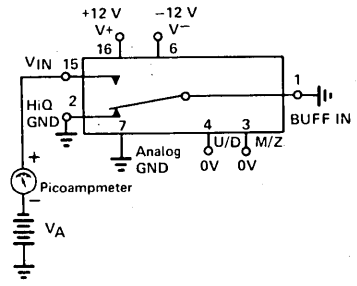
V_{IN} and $V_{Hi\text{-}Q}$ GND Switches Typical $r_{DS(on)}$ vs V_A and Temp



Typical Input Leakage vs Temp and V_A



Input Leakage Test Set-up



See Product Selector Guides on Pages 2779-2783.

Regulating Pulse Width Modulators

designed for . . .

■ Switched Mode Power Supplies (SMPS)

Designed to Optimize SMPS Using "State of the Art" MOSPOWER FETs

Siliconix
May 1982

BENEFITS

- **Improved Performance Over SG2525A/2527A**
  - Greatly Reduced Output Crossover Current
  - Greatly Reduced Transients with Separated Ground System
  - Fully Operational Up to 500 KHz
- **Wide Versatility**
  - 100 Hz to 500 KHz Oscillator Range
  - Separate Oscillator Sync Terminal
  - Adjustable Deadtime Control
  - Internal Soft-Start
  - Input Undervoltage Lockout
  - Latching PWM to Prevent Multiple Pulses
  - 8 to 35 Volts Operation

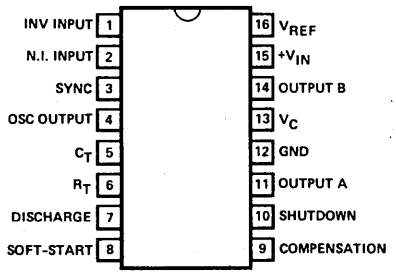
  Lower Overall Parts Count
  - 5.1 Volt Onboard Reference Trimmed to ±1%
  - Dual 100mA source/Sink Output Drivers
- **Pin Compatible with SG2525A/2527A**

DESCRIPTION

The PWM25/27 series of pulse width modulator integrated circuits are designed to offer improved performance and lowered external parts count when used to implement all types of switching power supplies. In addition to being pin compatible with the SG2525A/2527A the PWM25/27 features low crossover current through the output transistors and will maintain typical 10% pulse width up to 200KHz. The on-chip +5.1 volt reference is trimmed to ±1% initial accuracy and the input common-mode range of the error amplifier includes the reference voltage, eliminating external potentiometers and divider resistors. A Sync input to the oscillator allows multiple units to be slaved together, or a single unit to be synchronized to an external system clock. A single resistor between the C_T pin and the Discharge pin provides deadtime adjustment. These devices also feature built-in soft-start circuitry with only a timing capacitor required externally. A Shutdown pin controls both the soft-start circuitry and the output stages, providing instantaneous turn-off with soft-start recycle for slow turn-on. These functions are also controlled by an undervoltage lockout which keeps the outputs off and the soft-start capacitor discharged for input voltages less than that required for normal operation. Another unique feature of these PWM circuits is a latch following the comparator. Once a PWM pulse has been terminated for any reason, the outputs will remain off for the duration of the period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking 100 mA. The PWM25 output stage features NOR logic, giving a LOW output for an OFF state. The PWM27 utilizes OR logic which results in a HIGH output level when OFF.

PIN CONFIGURATION

Dual-In-Line Package

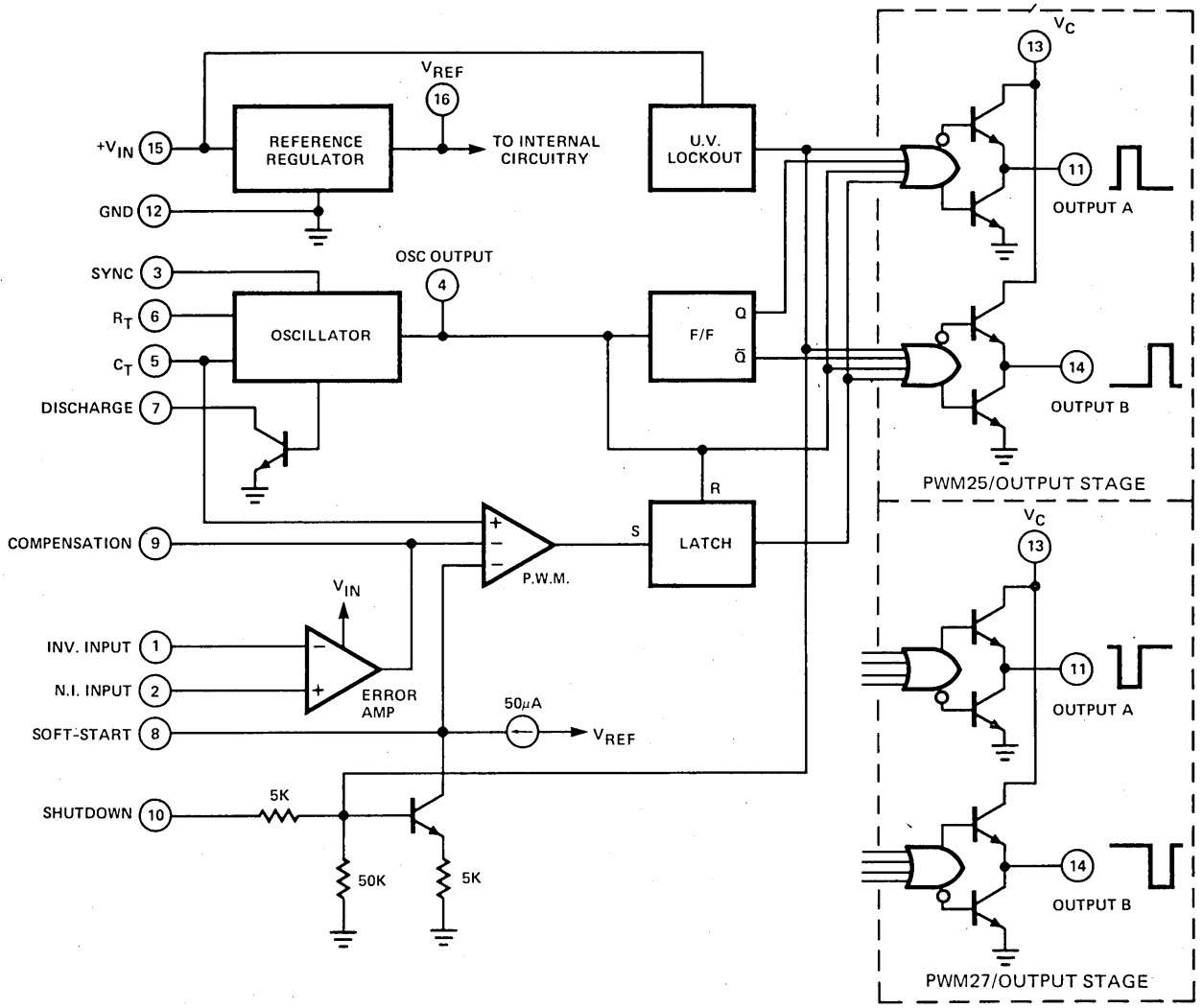


Top View

ORDER NUMBERS:

PWM25BK	PWM27BK
PWM25CK	PWM27CK

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS * (T_A = 25°C unless noted otherwise)

Supply Voltage (+V_{IN})	+40V
Collector Supply Voltage (V_C)	+40V
Logic Inputs	-0.3V to +5.5V
Analog Inputs	-0.3V to +V_{IN}
Output Current, Source or Sink	500 mA
Reference Output Current	50 mA
Oscillator Charging Current	5 mA
Power Dissipation at T_A = +25°C**	1000 mW
Thermal Resistance: junction to ambient	100°C/W
Power Dissipation at T_C = +25°C***	2000 mW
Thermal Resistance: junction to case	60°C/W
Operating Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

*Values beyond which damage may occur.
**Derate at 10 mW/°C for ambient temperatures above +50°C.
***Derate at 16 mW/°C for case temperatures above +25°C.

See Product Selector Guides on Pages 2779-2783.

RECOMMENDED OPERATING CONDITIONS [1]

Input Voltage ($+V_{IN}$) . . . . . +8V to +35V
Collector Supply Voltage (V_C) . . . +4.5V to +35V
Sink/Source Load Current
(each output) Steady State . . . . . 0 to 100 mA
Peak Current . . . . . 0 to 400 mA
Reference Load Current . . . . . 0 to 20 mA
Oscillator Frequency Range . . . 100 Hz to 500 kHz
Oscillator Timing Resistor. . . . . 1.5K to 210kΩ
Oscillator Timing Capacitor. . . . .820 pF to 0.1 μF

Operating Ambient Temperature Range
PWM25C, PWM27C . . . . . 0°C to +70°C
PWM25B, PWM27B . . . . . −25°C to +85°C

[1] Range over which the device is functional.

ELECTRICAL CHARACTERISTICS ($+V_{IN}$ = 20V, and over operating temperature, unless otherwise noted)

	Parameter	Conditions	PWM25B PWM27B			PWM25C PWM27C			Units
			Min	Typ	Max	Min	Typ	Max	
	Reference Section								
1	Output Voltage	T_j = 25°C	5.05	5.10	5.15	5.00	5.10	5.20	V
2	Line Regulation	V_{IN} = 8 to 35V		4	20		4	20	mV
3	Load Regulation	I_L = 0 to 20 mA		20	50		20	50	mV
4	Temperature Stability [2]	Over Operating Range		20	50		20	50	mV
5	Total Output Variation [2]	Line, Load, and Temp	5.00		5.20	4.95		5.25	V
6	Short Circuit Current	V_{REF} = 0, T_j = 25°C		80	110		80	110	mA
7	Output Noise Voltage [2]	10 Hz ≤ f ≤ 10 kHz, T_j = 25°C		40	200		40	200	μVrms
8	Long Term Stability [2]	T_j = 125°C		20	50		20	50	mV/khr
	Oscillator Section [3]								
9	Initial Accuracy [2,3]	T_j = 25°C		±2	±6		±2	±6	%
10	Voltage Stability [2,3]	V_{IN} = 8 to 35V		±0.1	±1		±0.1	±2	%
11	Temperature Stability [2]	Over Operating Range		±3	±6		±3	±6	%
12	Minimum Frequency				100			100	Hz
13	Maximum Frequency		400	500		400	500		kHz
14	Current Mirror	I_{RT} = 2 mA	1.7	2.0	2.2	1.7	2.0	2.2	mA
15	Clock Amplitude [2,3]		3.0	3.5		3.0	3.5		V
16	Clock Width [2,3]	T_j = 25°C	0.3	0.5	1.3	0.3	0.5	1.3	μsec
17	Sync Threshold		1.2	2.0	2.8	1.2	2.0	2.8	V
18	Sync Input Current	Sync Voltage = 3.5V		1.0	2.5		1.0	2.5	mA
	Error Amplifier Section (V_{CM} = 5.1 Volts)								
19	Input Offset Voltage			0.5	5		2	10	mV
20	Input Bias Current			1	10		1	10	μA
21	Input Offset Current				1			1	μA
22	DC Open Loop Gain	RL ≥ 10 MegΩ	60	80		60	80		dB
23	Gain-Bandwidth Product [4]	A_V = 0 dB, T_j = 25°C		3.5			3.5		MHz
24	Output Low Level			.02	0.5		.02	0.5	V
25	Output High Level		3.8	7		3.8	7		V
26	Common Mode Rejection	V_{CM} = 1.5 to 5.2V	60	85		60	85		dB
27	Supply Voltage Rejection	V_{IN} = 8 to 35V	50	85		50	85		dB

[2] These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
[3] Tested at f_{OSC} = 40 kHz (R_T = 3.6 kΩ, C_T = .01 μF, R_D = 0Ω).

PWM25 CMCD-A
PWM27 CMCD-B

TENTATIVE DATA SHEET. *This page provides tentative information on a new product. Siliconix reserves the right to change specifications for this product in any manner without notice.*

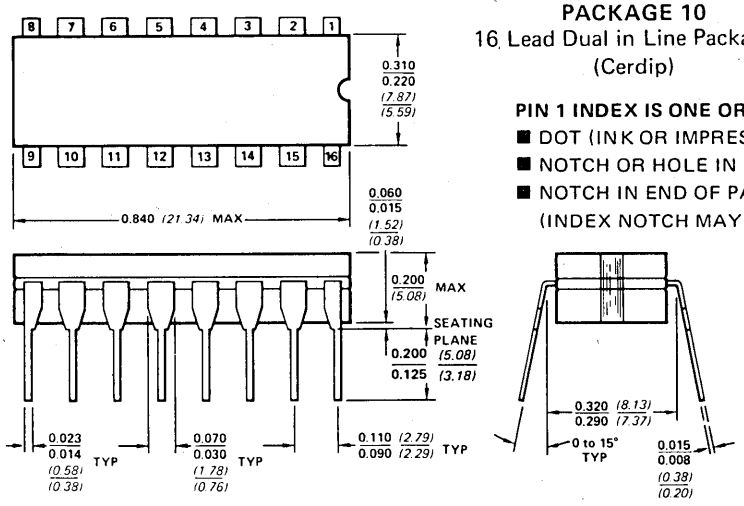
ELECTRICAL CHARACTERISTICS (CONT)

	Parameter	Conditions	PWM25B PWM27B			PWM25C PWM27C			Units
			Min	Typ	Max	Min	Typ	Max	
	P.W.M. Comparator								
28	Minimum Duty Cycle				0			0	%
29	Maximum Duty Cycle		45	49		45	49		%
30	Input Threshold[5]	Zero Duty Cycle	0.6	0.9		0.6	0.9		V
31	Input Threshold[5]	Max Duty Cycle		3.3	3.6		3.3	3.6	V
32	Input Bias Current[4]			.05			.05		μA
	Soft–Start Section								
33	Soft Start Current	$V_{SHUTDOWN}$ = 0V	25	50	100	25	50	100	μA
34	Soft Start Voltage	$V_{SHUTDOWN}$ = 2V		0.4	0.6		0.4	0.6	V
35	Shutdown Input Current	$V_{SHUTDOWN}$ = 2.5V		0.4	1.0		0.4	1.0	mA
	Output Drivers (Each Output) (V_C = 20 Volts)								
36	Output Low Level	I_{SINK} = 20 mA		0.2	0.4		0.2	0.4	V
37		I_{SINK} = 100 mA		1.0	2.5		1.0	2.5	V
38	Output High Level	I_{SOURCE} = 20 mA	18	19		18	19		V
39		I_{SOURCE} = 100 mA	17	18		17	18		V
40	Undervoltage Lockout	V_{Comp} and V_{SS} = high	6	7	8	6	7	8	V
41	Crossover Current	V_C = 35V		120			120		mA
42	Rise Time[4]	C_L = 1 nF, T_j = 25°C		100	600		100	600	nsec
43	Fall Time[4]	C_L = 1 nF, T_j = 25°C		50	300		50	300	nsec
44	Shutdown Delay[4]	V_{SH} = 3V, C_S = 0, T_j = 25°C		0.2	0.5		0.2	0.5	μsec
	Total Standby Current								
45	Supply Current	V_{IN} = 35V		14	20		14	20	mA

[4] These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production. PWM25 CMCD-A PWM27 CMCD-B

[5] Tested at f_{OSC} = 40 kHz (R_T = 3.6 kΩ, C_T = .01 μF, R_D = 0Ω).

PACKAGE DIMENSIONS



PACKAGE 10
16 Lead Dual in Line Package (K)
(Cerdip)

PIN 1 INDEX IS ONE OR MORE OF THE FOLLOWING:
- DOT (INK OR IMPRESSION) ON TOP OF PACKAGE
- NOTCH OR HOLE IN PIN 1 VISIBLE FROM TOP AND/OR SIDE
- NOTCH IN END OF PACKAGE VISIBLE FROM TOP AND/OR BOTTOM (INDEX NOTCH MAY BE PARTIALLY FILLED WITH GLASS)

ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

TOLERANCE
NON-ACCUMULATIVE

TENTATIVE DATA SHEET. *This page provides tentative information on a new product. Siliconix reserves the right to change specifications for this product in any manner without notice.*

See Product Selector Guides on Pages 2779-2783.

D-MOS FET QUAD ANALOG SWITCH ARRAYS AND DRIVER

designed for...

Siliconix
August 1982

SD5000 SERIES APPLICATIONS

- Analog Switching (up to very high frequencies)
- Audio Routing
- Choppers
- Crosspoint Switches
- Sample and Hold

SD5200 Applications

- Switch Drivers

FEATURES

- Low Input Capacitance - 2.4pF
- Low Feedback Capacitance - 0.3pF
- Low Output Capacitance - 1.3pF
- ±10V Analog Signal Range
- Low Propagation Delay Time - 600ps
- Low On Resistance - 30Ω
- Low Feedthrough And Feedback Transients
- Ion Implanted For Greater Reliability
- High Channel-To-Channel Isolation - 107dB
- Transient Protection For Gates

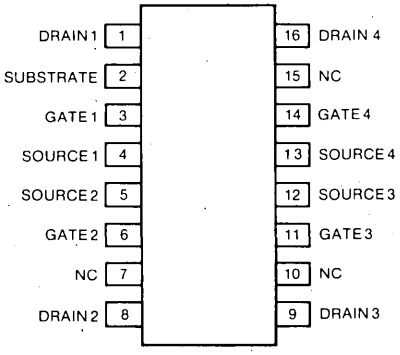
DESCRIPTION

The SILICONIX D-MOS SD5000, and 5200 series are monolithic arrays of silicon, insulated-gate, field-effect transistors using the N-channel enchancement mode technology.

This family of devices is designed to handle a wide variety of analog switching and driver applications. They are capable of high speed operation where excellent transient response, and wide voltage range are required. The SD5000 quad switch array can handle high voltage analog signals (± 10V), whereas the SD5001 and SD5002 are designed for lower voltage applications. The SD5200 is intended for use as a 30V driver to complement the other switch products.

PIN CONFIGURATIONS

I, N PACKAGE
(TOP VIEW)



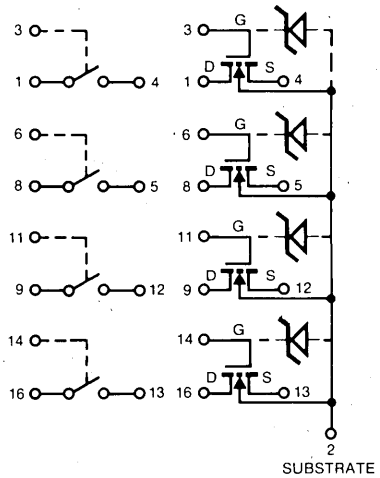
ORDER PART NO.

SD5000N SD5001N SD5002N SD5200N
(PLASTIC)

SD5000I SD5001I SD5002I SD5200I
(SIDE BRAZE)

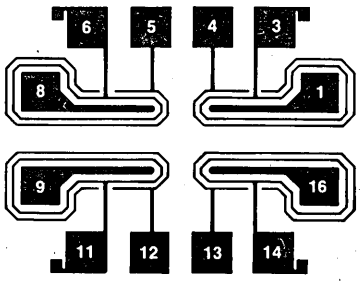
FUNCTIONAL AND SCHEMATIC DIAGRAM

SD5000, 5001, 5002, 5200



CHIP DIAGRAM

SD5000, 5001, 5002, 5200
SWITCH ARRAYS



Die Size 35 x 43

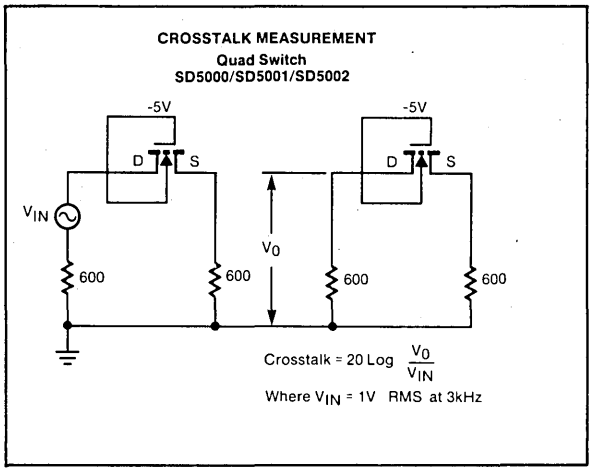
TENTATIVE DATA SHEET. *This page provides tentative information on a new product. Siliconix reserves the right to change specifications for this product in any manner without notice.*

ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise specified.

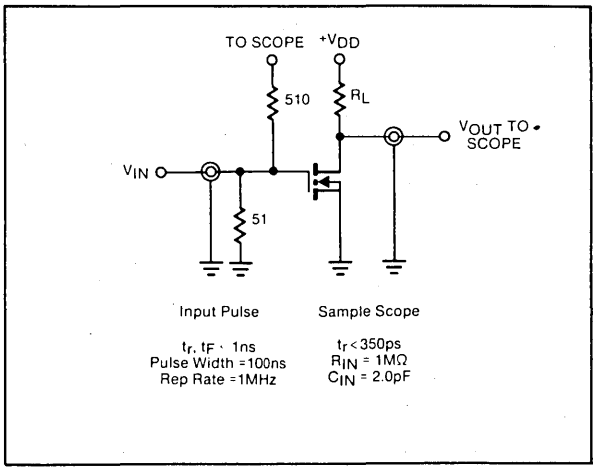
PARAMETERS		SD5000	SD5001	SD5002	SD5200	UNIT
V_{DS}	Drain-to-source	+20	+10	+15	+30	Vdc
V_{SD}	Source-to-drain [1]	+20	+10	+15	+0.5	
V_{DB}	Drain-to-Substrate	+25	+15	+22.5	+30	
V_{SB}	Source-to-Substrate	+25	+15	+22.5	+0.5	
V_{GS}	Gate-to-source	+30	+25	+30	+20	
		-25	-15	-22.5		
V_{GB}	Gate-to-substrate	+30	+25	+30	+20	
		-0.3	-0.3	-0.3	-0.3	
V_{GD}	Gate-to-drain	+30	+25	+30	+20	
		-25	-15	-22.5		
I_D	Drain current	50	50	50	50	mA
Ambient temperature range	Storage	-55 to +150				°C
	Operating	0 to +85				
Power Dissipation	Total package dissipation[2]	640				mW
	Individual transistor dissipation	300				

NOTES
1. Refer to test conditions specified in Electrical Characteristics Table.
2. Derated 5mW per degree centigrade.

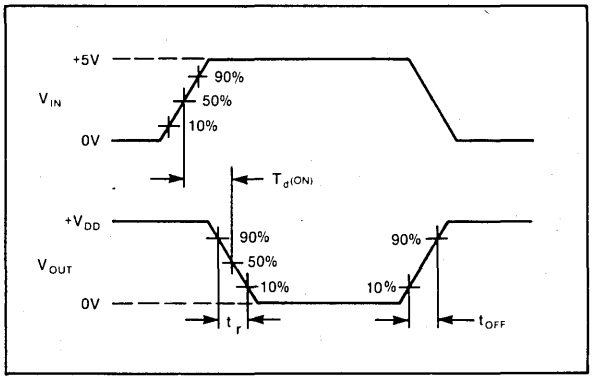
TEST CIRCUIT



SWITCHING TEST CIRCUIT



SWITCHING WAVEFORMS



SWITCHING CHARACTERISTICS

		$t_{d(ON)}$(ns)		t_{r}(ns)		* t_{OFF}(ns)	
V_{DD}	R_L	TYP	MAX	TYP	MAX	TYP	MAX
5	680	0.6	1.0	0.7	1.0	9.0	
10	680	0.7		0.8		9.0	
15	1k	0.9		1.0		14.0	

*t_{OFF} is dependent on R_L and does not depend on the device characteristics.

TENTATIVE DATA SHEET. *This page provides tentative information on a new product. Siliconix reserves the right to change specifications for this product in any manner without notice.*

See Product Selector Guides on Pages 2779-2783.

DC ELECTRICAL CHARACTERISTICS T_A = +25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	SD5000			SD5001			UNIT
			Min	Typ	Max	Min	Typ	Max	
BREAKDOWN VOLTAGE BV_{DS}	Drain-to-source	$V_{GS} = V_{BS} = -5V$, $I_S = 10nA$	20	25		10	25		V
BV_{SD}	Source-to-drain	$V_{GD} = V_{BD} = -5V$, $I_D = 10nA$	20			10			V
BV_{DB}	Drain-to-substrate	$V_{GB} = 0V$, source Open $I_D = 10nA$	25			15			V
BV_{SB}	Source-to-substrate	$V_{GB} = 0V$, drain Open $I_S = 10\mu A$	25			15			V
LEAKAGE CURRENT $I_{DS}(OFF)$	Drain-to-source	$V_{GS} = V_{BS} = -5V$, $V_{DS} = +20V$		1	10				nA
		$V_{GS} = V_{BS} = -5V$, $V_{DS} = +10V$					1	10	
$I_{SD}(OFF)$	Source-to-drain	$V_{GD} = V_{BD} = -5V$, $V_{SD} = +20V$		1	10				nA
		$V_{GD} = V_{BD} = -5V$, $V_{SD} = +10V$					1	10	
I_{GBS}	Gate	$V_{DB} = V_{SB} = 0V$, $V_{GB} = 30V$			1				μA
		$V_{DB} = V_{SB} = 0V$, $V_{GB} = 25V$						1	
V_T	Threshold voltage	$V_{DS} = V_{GS} = V_T$, $I_S = 1\mu A$ $V_{SB} = 0V$	0.1	1.0	2.0	0.1	1.0	2.0	V
$r_{DS}(On)$	Drain-to-source resistance	$I_D = 1.0mA$, $V_{SB} = 0$, $V_{GS} = +5V$		50	70		50	70	Ω
		$I_D = 1.0mA$, $V_{SB} = 0$, $V_{GS} = +10V$		30			30		
		$I_D = 1.0mA$, $V_{SB} = 0$, $V_{GS} = +15V$		23			23		
		$I_D = 1.0mA$, $V_{SB} = 0$, $V_{GS} = +20V$		19			19		
$r_{DS}(On)$	Resistance match (Note 1)	$I_D = 1.0mA$, $V_{SB} = 0$ $V_{GS} = +5V$		1	5		1	5	Ω

PARAMETER		TEST CONDITIONS	SD5002			SD5200			UNIT
			Min	Typ	Max	Min	Typ	Max	
BREAKDOWN VOLTAGE BV_{DS}	Drain-to-source	$V_{GS} = V_{BS} = 0V$, $I_D = 10\mu A$				30	35		V
		$V_{GS} = V_{BS} = -5V$, $I_S = 10nA$	15	25					
BV_{SD}	Source-to-drain	$V_{GD} = V_{BD} = -5V$, $I_D = 10nA$	15						V
BV_{DB}	Drain-to-substrate	$V_{GB} = 0V$, source Open $I_D = 10nA$	22.5						V
BV_{SB}	Source-to-substrate	$V_{GB} = 0V$, drain Open $I_S = 10\mu A$	22.5						V
LEAKAGE CURRENT $I_{DS}(OFF)$	Drain-to-source	$V_{GS} = V_{BS} = -5V$ $V_{DS} = +15V$ $V_{DS} = +10V$		1	10				nA
$I_{SD}(OFF)$	Source-to-drain	$V_{GD} = V_{BD} = -5V$ $V_{SD} = +15V$ $V_{SD} = +10V$		1	10				nA
I_{GBS}	Gate	$V_{DB} = V_{SB} = 0V$ $V_{GB} = 30V$			1				μA
V_T	Threshold voltage	$V_{DS} = V_{GS} = V_T$, $I_S = 1\mu A$ $V_{SB} = 0V$	0.1	1.0	2.0	0.5	1.0	2.0	V
$r_{DS}(On)$	Drain-to-source resistance	$I_D = 1.0mA$, $V_{SB} = 0$, $V_{GS} = +5V$		50	70		50	80	Ω
		$I_D = 1.0mA$, $V_{SB} = 0$, $V_{GS} = +10V$		30			30		
		$I_D = 1.0mA$, $V_{SB} = 0$, $V_{GS} = +15V$		23			23		
		$I_D = 1.0mA$, $V_{SB} = 0$, $V_{GS} = +20V$		19			19		
$r_{DS}(On)$	Resistance match (Note 1)	$I_D = 1.0mA$, $V_{SB} = 0$ $V_{GS} = +5V$		1	5				Ω

DMAC

NOTE:
1. This untested parameter is guaranteed by design.

TENTATIVE DATA SHEET. *This page provides tentative information on a new product. Siliconix reserves the right to change specifications for this product in any manner without notice.*

AC ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	SD5000			SD5001			UNIT
			Min	Typ	Max	Min	Typ	Max	
gfs	Forward transconductance	V_{DS} = 10V, V_{SB} = 0V I_D = 20mA, f = 1kHz	10	15		10	15		mmhos
$C_{(GS+GD+GB)}$	Gate node capacitances	V_{DS} = 10V, f = 1MHz V_{GS} = V_{BS} = -15V See capacitance model in Figure 1		2.4	3.5		2.4	3.5	pf
$C_{(GD+DB)}$	Drain node capacitances			1.3	1.5		1.3	1.5	
$C_{(GS+SB)}$	Source node capacitances			3.5	4.0		3.5	4.0	
C_{DG}	Reverse transfer capacitances			0.3	0.5		0.3	0.5	
C_T	Cross talk	See test circuits no.1 and 2, f = 3kHz		-107			-107		dB

PARAMETER		TEST CONDITIONS	SD5002			SD5200			UNIT
			Min	Typ	Max	Min	Typ	Max	
gfs	Forward transconductance	V_{DS} = 10V, V_{SB} = 0V I_D = 20mA, f = 1kHz	10	15		10	15		mmhos
$C_{(GS+GD+GB)}$	Gate node capacitances	V_{DS} = 10V, f = 1MHz V_{GS} = V_{BS} = -15V See capacitance model in Figure 1		2.4	3.5		2.4	3.5	pf
$C_{(GD+DB)}$	Drain node capacitances			1.3	1.5		1.3	1.5	
$C_{(GS+SB)}$	Source node capacitances			3.5	4.0				
C_{DG}	Reverse transfer capacitances			0.3	0.5		0.3	0.5	
C_T	Cross talk	See test circuits no.1 and 2, f = 3kHz		-107			-107		dB

THEORY OF OPERATION

The SD5000 series consists of four SPST switches with analog signal capability of up to ±10 volts for the SD5000 and ±7.5 volts for the SD5002. Each switch of the array is a D-MOS N-channel field-effect transistor of the enhancement-mode type; that is, the device is normally off when gate-to-source voltage (V_{GS}) is zero volts. When V_{GS} exceeds the threshold voltage, V_T, the FET switch starts to turn ON with V_{GS} in excess of +10 volts, a low resistance path (typically 30Ω) exists between input and output of the switch. Figure 1 shows the normal mode of operation of a single switch of the array for±5 volt analog signal processing. Note that the source is recommended for the input since feedback or reverse transfer capacitance is lower when drain is used as the output. When analog signals are routed from one point to another the important factors are isolation, crosstalk between switches, feedthrough and feedback transients, insertion loss and speed of operation. The SD5000 series offers superior performance in all these areas (Figure 1).

Isolation. ON resistance is typically 30Ω and OFF resistance is typically 10^{10}Ω, which results in an OFF to On resistance ratio in excess of 10^9. Isolation from output to input from 3kHz analog signals is typically -107dB.

Feedback and feedthrough transients. These are kept to a minimum because of the very low feedback and feedthrough capacitances. This means that "glitchless" or "clean" signals appear at the output.

Insertion loss. This depends upon the source and load impedances involved. As an example, for 600Ω source impedance the insertion loss for voice signals (1V RMS at 3kHz) is less than 0.3dB. This indicates that the SD5000 series would make good telephone cross-point switches.

Speed. Because of the low ON resistance and low input capacitance, the SD5000 switches ON at sub-nanoseconds speeds. They are also capable of handling very high frequency analog signals and still maintain excellent isolation (20-30dB-at 1GHz).

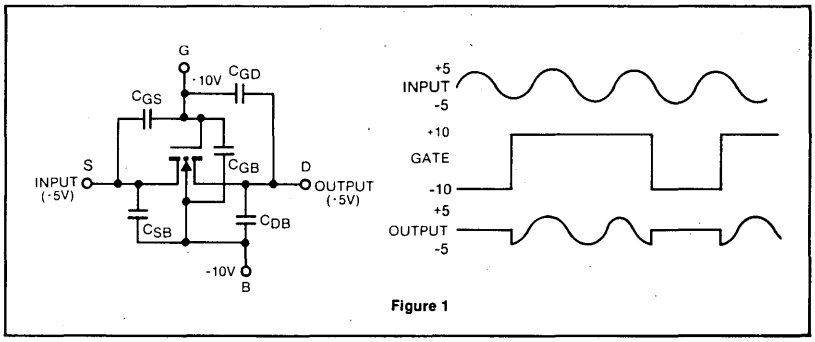


Figure 1

Note that the body (B) is biased to the most negative voltage in the circuit.

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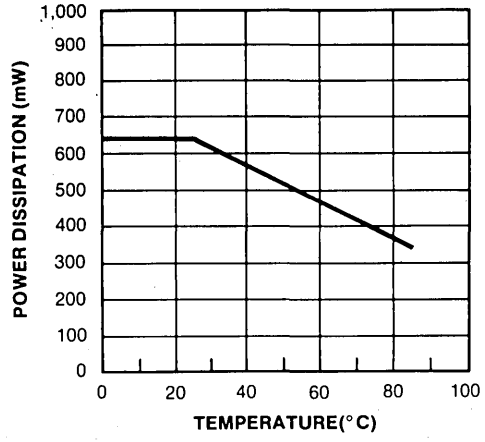
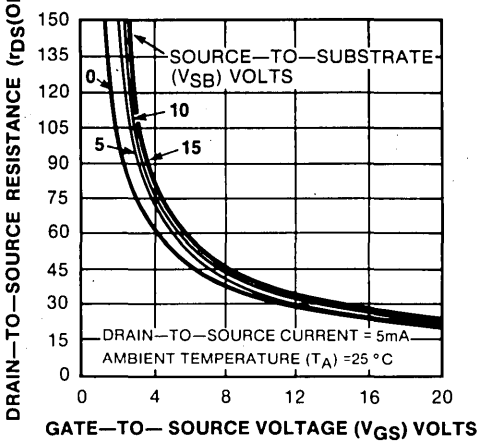
See Product Selector Guides on Pages 2779-2783.

TYPICAL PERFORMANCE CHARACTERISTICS

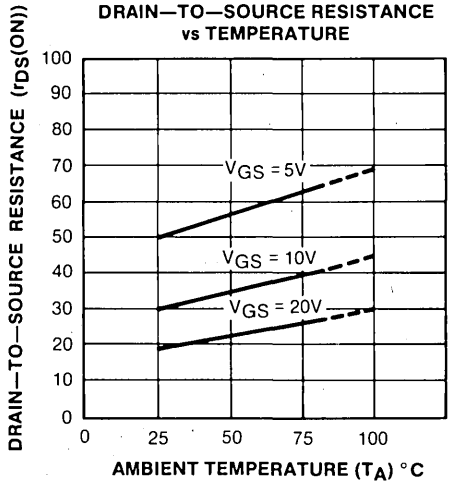
MAXIMUM POWER DISSIPATION vs TEMPERATURE



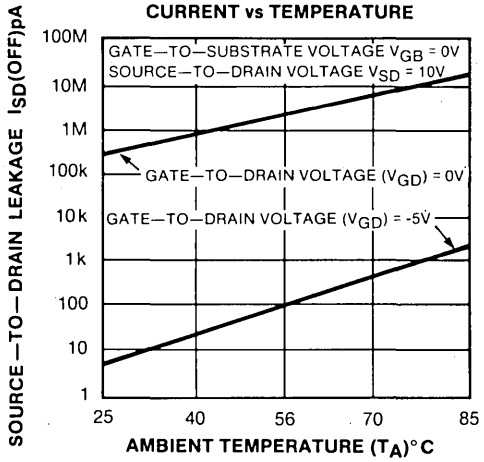
DRAIN—TO—SOURCE RESISTANCE vs SOURCE—TO—SUBSTRATE AND GATE—TO—SOURCE VOLTAGE



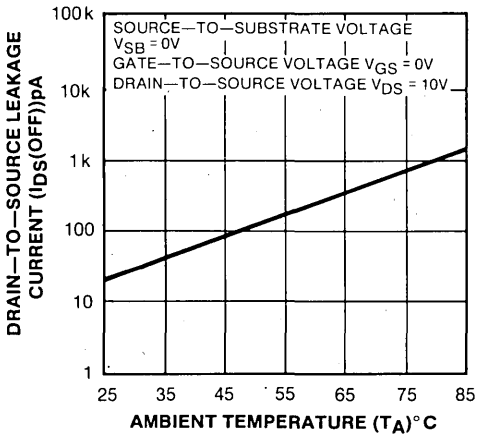
DRAIN—TO—SOURCE RESISTANCE vs TEMPERATURE



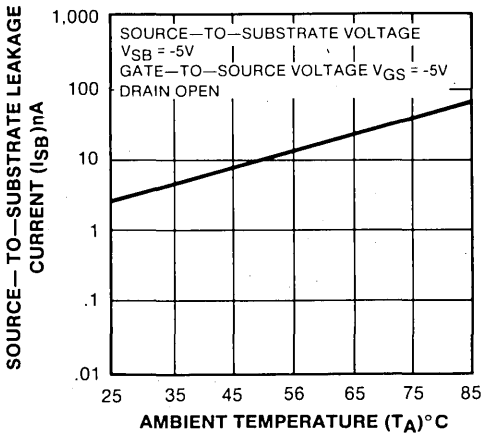
SOURCE—TO—DRAIN LEAKAGE CURRENT vs TEMPERATURE



DRAIN—TO—SOURCE LEAKAGE CURRENT vs TEMPERATURE



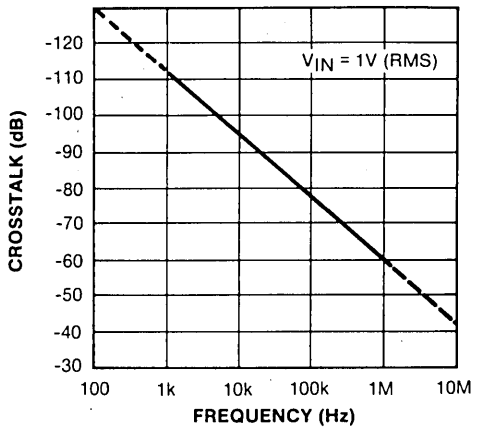
SOURCE—TO—SUBSTRATE LEAKAGE CURRENT vs TEMPERATURE



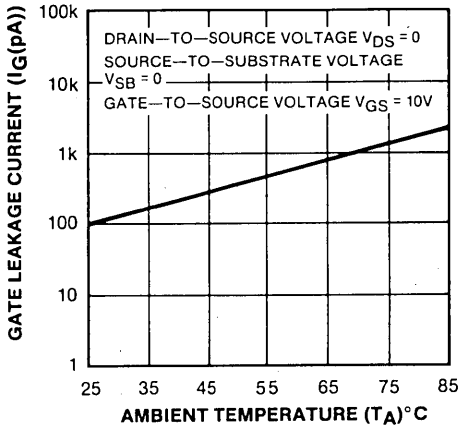
TENTATIVE DATA SHEET. *This page provides tentative information on a new product. Siliconix reserves the right to change specifications for this product in any manner without notice.*

TYPICAL PERFORMANCE CHARACTERISTICS (Cont.)

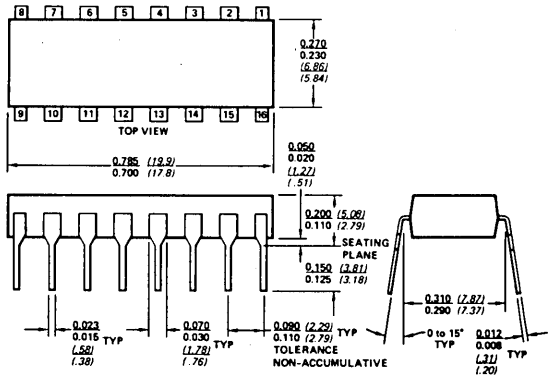
CROSSTALK vs FREQUENCY



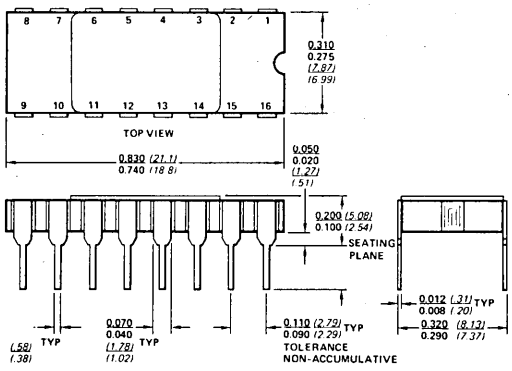
GATE LEAKAGE CURRENT vs TEMPERATURE



PACKAGE OUTLINES



16 LEAD DUAL IN LINE PACKAGE **(N)**
(PLASTIC)



16 LEAD DUAL IN LINE PACKAGE **(I)**
(SIDE BRAZE)

PIN 1 INDEX IS ONE OR MORE OF THE FOLLOWING

- DOT (INK OR IMPRESSION) ON TOP OF PACKAGE
- NOTCH OR HOLE IN PIN 1 VISIBLE FROM TOP AND/OR SIDE
- NOTCH IN END OF PACKAGE VISIBLE FROM TOP AND/OR BOTTOM

ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

TENTATIVE DATA SHEET. *This page provides tentative information on a new product. Siliconix reserves the right to change specifications for this product in any manner without notice.*

Siliconix
2201 Laurelwood Road Santa Clara, CA 95054
(408) 988-8000 TWX: 910-338-0227

Si7250

High Current Power Driver

Siliconix

Revised April 1982

Designed as Coil Pre-Driver for Bubble Memories

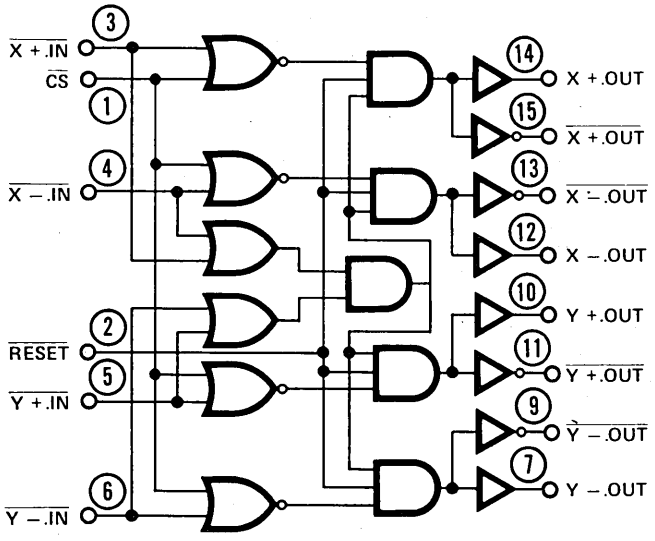
FEATURES

- Capable of Driving a 500 pf Load With Less Than 25 ns Transitions
- Very Low Standby Power Consumption
- TTL Compatible Inputs
- Single 12V Power Supply
- CMOS Technology
- Ideal for use in Magnetic Bubble Memory Systems
- Power Fail Reset for Maximum Protection of Bubble Memories
- Standard 16 Pin Dual-In-Line Package.

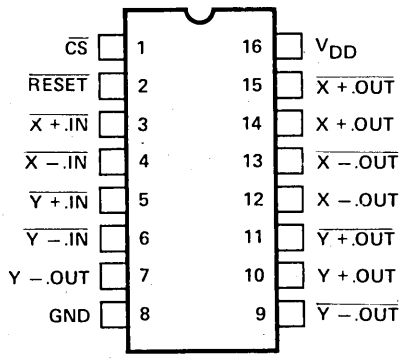
DESCRIPTION

The Si7250 is a low power coil pre-driver for direct use with the Siliconix VQ7254 to drive magnetic bubble memory coils. The Si7250 has TTL compatible inputs and complimentary outputs designed to drive high capacitance, low on resistance MOS-POWER® devices.

LOGIC DIAGRAM



PIN CONFIGURATION



ORDER NUMBER: Si7250CK

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C unless otherwise noted)

Ambient Temperature Under Bias . . . . . −20°C to +80°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin with Respect to Ground . . . . . −0.5 to V_{DD} + 0.5V
Supply Voltage, V_{DD} . . . . . −0.5 to +14V
Output Current . . . . . 250 mA
(One Output @ 100% Duty Cycle)

Maximum Operating Junction Temperature 150°C
θ_{JC} = 25°C/W
θ_{JA} = 75°C/W (No Airflow)

Stresses listed under "Absolute Maximum Ratings" may be applied (one at a time) to devices without resulting in permanent damage. This is a stress rating only and not subject to production testing. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure performance with specifications.

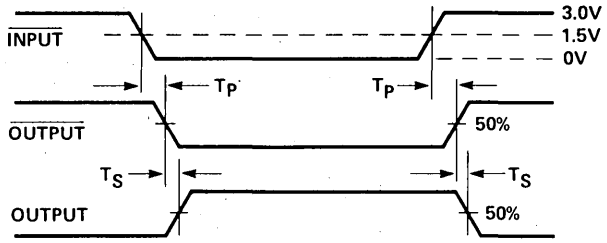
		Characteristic		Limits			Unit	Test Conditions Unless otherwise noted: T_A = 0°C to 70°C, V_{DD} = 12V ±10%
				Min	Typ[2]	Max		
1	INPUT	$\|I_{IN}\|$	Input Current			10	µA	V_I = 0.8V
2	INPUT	V_{IL}	Low Level Input Voltage			0.8	V	
3	INPUT	V_{IH}	High Level Input Volage	2.2			V	
4	OUTPUT	V_{OL1}	Output Low Voltage		1.45	2.0	V	I_{OL} = 200 mA
5	OUTPUT	V_{OL2}	Output Low Voltage		0.1	0.2	V	I_{OL} = 10 mA
6	OUTPUT	V_{OH1}	Output High Voltage	V_{DD}−2.0	V_{DD}−1.4		V	I_{OH} = −200 mA
7	OUTPUT	V_{OH2}	Output High Voltage	V_{DD}−0.2	V_{DD}−0.1		V	I_{OH} = −10 mA
8	OUTPUT	I_{OL}	Output Sink Current	200			mA	V_{OL} = 2.0V, 30% Duty Cycle
9	OUTPUT	$\|I_{OH}\|$	Output Source Current	200			mA	V_{OH} = V_{DD}−2.0V, 30% Duty Cycle
10	DYNAMIC	t_{p1}	Propagation Delay from $\overline{X+.IN}$, $\overline{X-.IN}$, $\overline{Y+.IN}$, $\overline{Y-.IN}$		55	100	ns	500 pF Load
11	DYNAMIC	t_{p2}	Propagation Delay from $\overline{CS}$ or $\overline{RESET}$		90	150	ns	500 pF Load
12	DYNAMIC	t_r	Rise Time (10% to 90%)		25	45	ns	500 pF Load
13	DYNAMIC	t_f	Fall Time (90% to 10%)		25	45	ns	500 pF Load
14	DYNAMIC	t_s	Skew Between an Output and its Complement		10	20	ns	500 pF Load
15	DYNAMIC	C_{IN}[1]	Input Capacitance			10	pF	
16	SUPPLY	I_{DD0}	Supply Current		1.0	4.5	mA	Chip Deselected: $\overline{CS}$ = V_{IH}, V_{DD} = 12.6V
17	SUPPLY	I_{DD1}	Supply Current			75	mA	f = 100 kHz, V_{DD} = 12.6V, Outputs Unloaded
18	SUPPLY	I_{DD2}	Supply Current			90	mA	f = 200 kHz, V_{DD} = 12.6V, Output Unloaded

Note 1: This parameter is periodically sampled and is not 100% tested. Condition of measurement is f= 1 MHz, V_{BIAS}= 2V, V_{DD}= 0V, and T_A= 25°.

Note 2: Typical Values are for DESIGN AID ONLY, not guaranteed and not subject to production testing (Typical values at T_A= 25°C and V_{DD}= 12V)

See Product Selector Guides on Pages 2779-2783.

AC TEST CONDITIONS



PIN DESCRIPTION

$\overline{CS}$ (Pin 1)

Chip select is active low. When high, chip is de-selected and I_{DD} is significantly reduced. Chip Select is most commonly used for system expansion.

$\overline{RESET}$ (Pin 2)

Active low input from $\overline{RESET.OUT}$ of the Controller results in removal of power from the chip so that bubble memory is protected in the event of power supply failure.

$\overline{X+.IN}$, $\overline{X-.IN}$ (Pins 3, 4)

Active low inputs from controller which turn on the high current X outputs.

X–.OUT, $\overline{X-.OUT}$, $\overline{X+.OUT}$, X+.OUT(Pins 12-15)

High current outputs and their complements for driving the gates of the 7254 QUAD MOSPOWER® FETs which in turn drive the X coils of the bubble memory.

$\overline{Y+.IN}$, $\overline{Y-.IN}$ (Pins 5, 6)

Active low inputs from controller which turn on the high current Y outputs.

$\overline{Y-.OUT}$, Y+.OUT, $\overline{Y+.OUT}$, Y–.OUT (Pins 9–11 and 7)

High current outputs and their complements for driving the gates of the 7254 QUAD MOSPOWER® FETs which in turn drive the Y coils of the bubble memory.

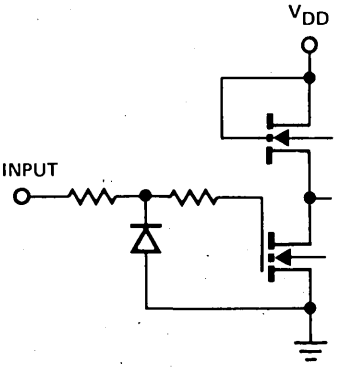
TRUTH TABLE

INPUT PINS						OUTPUT PINS							
1 $\overline{CS}$	2 $\overline{R}$	3 $\overline{X+.}$	4 $\overline{X-.}$	5 $\overline{Y+.}$	6 $\overline{Y-.}$	7 Y–.	9 $\overline{Y-.}$	10 Y+.	11 $\overline{Y+.}$	12 X–.	13 $\overline{X-.}$	14 X+.	15 $\overline{X+.}$
1	X	X	X	X	X	0	1	0	1	0	1	0	1
X	0	X	X	X	X	0	1	0	1	0	1	0	1
8 INPUT STATES DECODED													
0	1	0	1	0	1	0	1	1	0	0	1	1	0
0	1	0	1	1	0	1	0	0	1	0	1	1	0
0	1	0	1	1	1	0	1	0	1	0	1	1	0
0	1	1	0	0	1	0	1	1	0	1	0	0	1
0	1	1	0	1	0	1	0	0	1	1	0	0	1
0	1	1	0	1	1	0	1	0	1	1	0	0	1
0	1	1	1	0	1	0	1	1	0	0	1	0	1
0	1	1	1	1	0	1	0	0	1	0	1	0	1

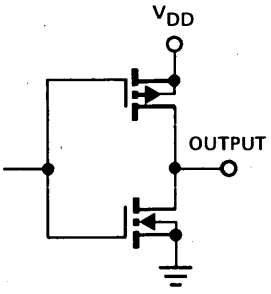
The 8 remaining input states are **not** decoded resulting in a reset output condition This is to prevent the inadvertent shorting of any power drivers directly across the supplies in a standard bubble memory configuration

0	1	0	0	0	0	0	1	0	1	0	1	0	1
0	1	0	0	0	1	0	1	0	1	0	1	0	1
0	1	0	0	1	0	0	1	0	1	0	1	0	1
0	1	0	0	1	1	0	1	0	1	0	1	0	1
0	1	0	1	0	0	0	1	0	1	0	1	0	1
0	1	1	0	0	0	0	1	0	1	0	1	0	1
0	1	1	1	0	0	0	1	0	1	0	1	0	1
0	1	1	1	1	1	0	1	0	1	0	1	0	1

INPUT STRUCTURE



OUTPUT STRUCTURE



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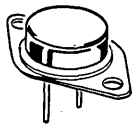
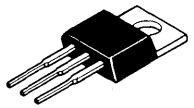
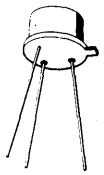
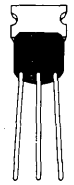
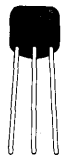
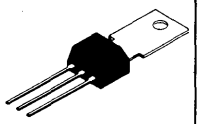
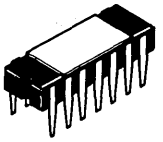
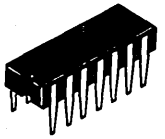
* 200°C RATING

Packages:								
BV_{DSS} (Volts)	**TO-3**	**TO-220**	**TO-39**	**TO-237**	**TO-92**	**TO-202**	**Quad Side Braze**	**Quad Plastic**
450-500	IRF450 13A, 0.4Ω	IRF840 8A, 0.85Ω						
	IRF440 8A, 0.85Ω	VN5001D/IRF830 4A, 1.5Ω						
	VNP002A* 6.5A, 1.5Ω	IRF820 2.5A, 3Ω						
	VN5001A/IRF430 4A, 1.5Ω							
350-400	IRF350 15A, 0.3Ω	IRF740 10A, 0.55Ω						
	IRF340 10A, 0.55Ω	VN4000D/IRF730 6A, 1.0Ω						
	VNM001A* 8A, 1.0Ω	IRF720 3A, 1.8Ω						
	VN4000A/IRF330 6A, 1.0Ω							
150-240	IRF250 30A, 0.085Ω	IRF640 18A, 0.18Ω	VN2406B 0.8A, 6Ω	VN2406M 0.3A, 6Ω	VN2406L 0.21A, 6Ω			
	IRF240 18A, 0.18Ω	IRF630 9A, 0.4Ω		VN2410M 0.25A, 10Ω	VN2410L 0.16A, 10Ω			
	IRF230 9A, 0.4Ω	IRF620 5A, 0.8Ω						
	IRF220 5A, 0.8Ω	VN2406D 1.4A, 6Ω						

P-CHANNEL

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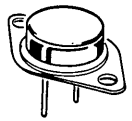
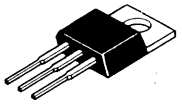
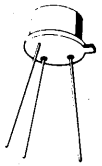
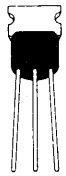
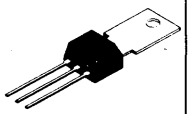
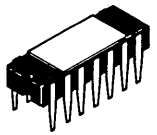
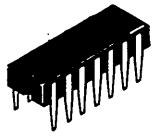
Packages:								
BV_{DSS} (Volts)	**TO-3**	**TO-220**	**TO-39**	**TO-237**	**TO-92**	**TO-202**	**Quad Side Braze**	**Quad Plastic**
100-120	IRF150 40A, 0.055Ω	IRF540 27A, 0.085Ω	IRFF120 6A, 0.30Ω	VN1206M 0.3A, 6Ω	VN1206L 0.21A, 6Ω			
	IRF140 27A, 0.085Ω	VN1200D/IRF530 12A, 0.18Ω	IRFF122 5A, 0.40Ω	VN1210M 0.25A, 10Ω	VN1210L 0.16A, 10Ω			
	VN1200A/IRF130 12A, 0.18Ω	IRF520 8A, 0.30Ω	VN1206B 0.8A, 6Ω	VP1008M 0.37A, 5Ω	VP1008L 0.4A, 5Ω			
		VN1206D 1.4A, 6Ω	VP1008B 0.9A, 5Ω					
80-90	VN0800A 12A, 0.18Ω	VN0800D 12A, 0.18Ω	2N6661 0.9A, 4Ω	VN0808M 0.35A, 4Ω	VP0808L 0.37A, 5Ω	VN88AF 1.5A, 4Ω	VQ1006P 0.40A, 4.5Ω	VQ1006J 0.40A, 4.5Ω
	2N6658 1.9A, 4Ω	VN88AD 1.7A, 4Ω	VP0808B 0.9A, 5Ω	VP0808M 0.37A, 5Ω		VN80AF 1.3A, 5Ω	VQ2006P 1.3A, 5Ω	VQ2006J 1.3A, 5Ω
60	**IRF151** **40A, 0.055Ω**	IRF541 27A, 0.085Ω	IRFF121 6A, 0.30Ω	VN0606M 0.4, 3Ω	VN0610L 0.2A, 5Ω	VN66AF 1.7A, 3Ω	VQ1004P 0.46A, 5.5Ω	VQ1004J 0.46A, 5.5Ω
	IRF141 27A, 0.085Ω	VN0600D 16A, 0.12Ω	IRFF123 5A, 0.40Ω	VN10KM 0.3A, 5Ω	VN2222L 0.15A, 7.5Ω	VN67AF 1.6A, 3.5Ω	VQ1000P 0.225A, 3.5Ω	VQ1000J 0.225A, 3.5Ω
	VN0600A 16A, 0.12Ω	IRF531 14A, 0.18Ω	2N6660 1.1A, 3Ω	VN2222KM 0.25A, 7.5Ω			VQ2004P 1.3A, 5Ω	VQ2004J 1.3A, 5Ω
	IRF131 14A, 0.18Ω	IRF521 8A, 0.30Ω	VN67AB 1A, 3.5Ω					
	2N6657 2A, 3Ω	VN66AD 1.9A, 3Ω						
30-40	VN0400A 16A, 0.12Ω	VN0400D 16A, 0.12Ω	2N6659 1.4A, 1.8Ω	VN0300M 0.7A, 1.2Ω		VN46AF 1.6A, 3Ω	VQ1001P 0.85A, 1.0Ω	VQ1001J 0.85A, 1.0Ω
	2N6656 2A, 1.8Ω	VN0300D 2.5A, 1.5Ω	VP0300B 1.3A, 2.5Ω	VP0300M 0.48A, 2.5Ω		VN40AF 1.3A, 5Ω	VQ2001P 1.3A, 2Ω	VQ2001J 1.3A, 2Ω
Specialty Products (N- and P-Channel Quad Arrays)							VQ3001P 30V, 3Ω Total	VQ3001J 30V, 3Ω Total
							VQ7254P 20V, 3Ω Total	VQ7254J 20V, 3Ω Total

VQ1000P ■ VQ1000J

Siliconix

60V N-Channel Enhancement Mode Quad MOSPOWER Array

This power FET is designed especially for low power high frequency inverters, interface to CMOS and TTL logic, line drivers and Analog Switching.

FEATURES

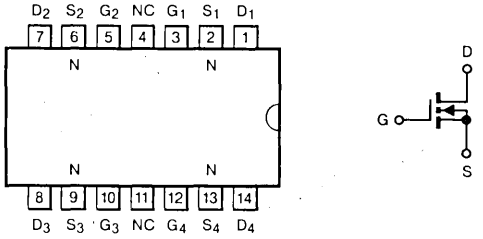
- **High Input Impedance**
- **Extremely Fast Switching**
- **Rugged**
- **Internal Drain-Source Diode**
- **Dual-In-Line Package for Packing Density and Automatic Insertion**

BENEFITS

- **Reduced Component Count**
- **Simpler Designs**
  - **— Directly Interfaces CMOS & TTL**
- **Improved Circuit Performance**
- **Increased Reliability**

Product Summary

Part Number	BV_{DSS} (Volts)	$R_{DS(ON)}$ (Ohms)	Package
VQ1000P	60	5.5	Side Braze
VQ1000J	60	5.5	Plastic



TOP VIEW
ORDER NUMBER: VQ1000P, VQ1000J

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Drain-Source Voltage 60V

Drain-Gate Voltage 60V

Drain Current
- Continuous[1] . . . . . ±225mA
- Pulsed[1,2] . . . . . ±1A

Gate-Source Voltage . . . . . ±30V

Gate Current Peak . . . . . ±1A

Power Dissipation
- Single 1.30W
- Quad 2W

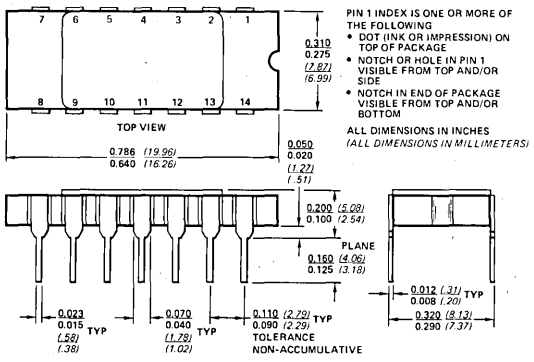
Linear Derating Factor
- Single . . . . . 10.4mW/°C
- Quad . . . . . 16mW/°C

Operating and Storage Temperature . . . . . −55°C to +150°C

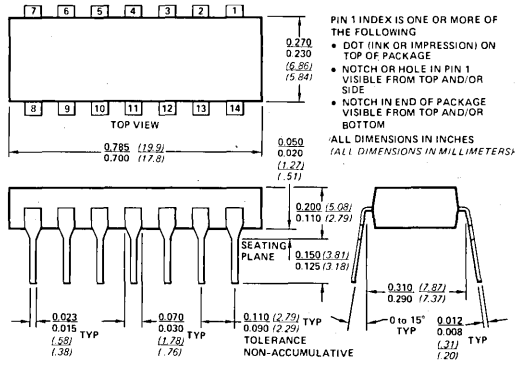
Lead Temperature (1/16″ from case for 10 secs) . . . . . +300°C

Note: 1: Single device alone. Package limited.
Note: 2: Pulse test: 80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



14-LEAD DUAL-IN-LINE PACKAGE (P)
(SIDE BRAZE)



14-LEAD DUAL-IN-LINE PACKAGE (J)
(PLASTIC)

See Product Selector Guides on Pages 2833-2834.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Parameter		Min	Max	Unit	Test Conditions
Static					
BV_{DSS}	Drain-Source Breakdown	60		V	V_{GS} = 0, I_D = 100μA
$V_{GS(th)}$	Gate Threshold Voltage	0.8	2.5	V	V_{DS} = V_{GS}, I_D = 1mA
I_{GSS}	Gate Body Leakage		100	nA	V_{GS} = 10V, V_{DS} = 0
			500		V_{GS} = 10V, V_{DS} = 0, T_A = 125°C
I_{DSS}	Zero Gate Voltage Drain Current		10	μA	V_{GS} = 0, V_{DS} = 48V
			500		V_{GS} = 0, V_{DS} = 48V, T_A = 125°C
$V_{DS(on)}$	Drain-Source Saturation Voltage[1]		1.5	V	V_{GS} = 5V, I_D = 0.2A
			1.65		V_{GS} = 10V, I_D = 0.3A
$r_{DS(on)}$	Drain-Source On Resistance[1]		7.5	Ω	V_{GS} = 5V, I_D = 0.2A
			5.5		V_{GS} = 10V, I_D = 0.3A
$I_{D(on)}$	On-State Drain Current[1]	0.2		A	V_{DS} = 15V, V_{GS} = 5V
		0.5			V_{DS} = 15V, V_{GS} = 10V
Dynamic					
g_{fs}	Forward Transconductance[1]	100		mS	V_{DS} = 15V, I_D = 0.5A
C_{iss}	Input Capacitance		60	pF	V_{DS} = 25V, V_{GS} = 0, f = 1MHz
C_{rss}	Reverse Transfer Capacitance		5		
C_{oss}	Common-Source Output Capacitance		25		
t_{ON}	Turn-ON Time		10	ns	V_{DD} = 15V, R_L = 23Ω, R_g = 25Ω, I_D ≈ 0.6A (Figure 1)
t_{OFF}	Turn-OFF Time		10		
Drain-Source Diode Characteristics					
		Typ			
V_{SD}	Forward ON Voltage[1]	−0.85		V	I_S = −0.5A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	165		ns	I_F = I_R = 0.3A, V_{GS} = 0 (Figure 2)

Note 1: Pulse test — 80μs to 300μs, 1% duty cycle

VNML

TEST CIRCUITS

FIGURE 1. Switching Test Circuit

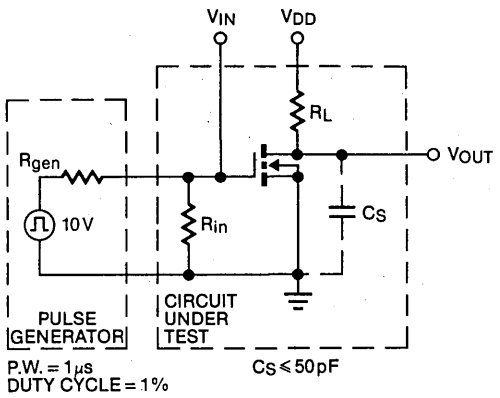
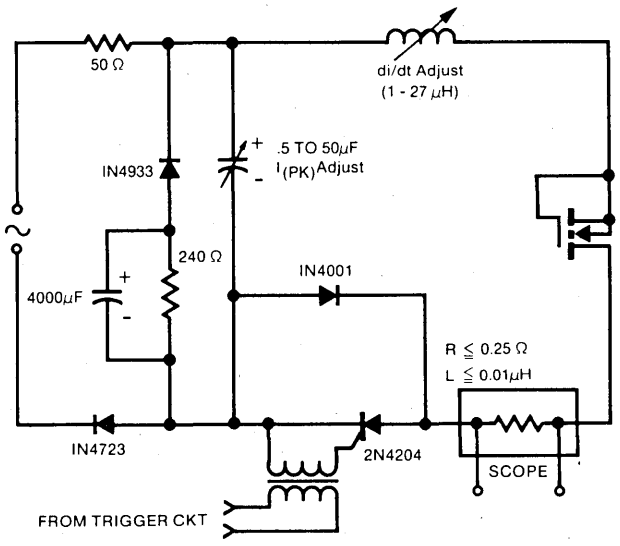


FIGURE 2. JEDEC Reverse Recovery Circuit



VQ1004P ■ VQ1004J ■ VQ1006P ■ VQ1006J

Siliconix

90V N-Channel Enhancement Mode Quad MOSPOWER Array

This power FET is designed especially for low power high frequency inverters, interface to CMOS and TTL logic, line drivers and Analog Switching.

FEATURES

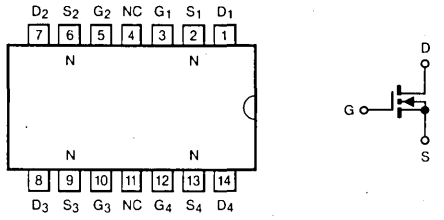
- **High Input Impedance**
- **Extremely Fast Switching**
- **Rugged—Dissipation Limited SOA**
- **Internal Drain-Source Diode**
- **Dual-In-Line Package for Packing Density and Automatic Insertion**

BENEFITS

- **Reduced Component Count**
- **Simpler Designs — Directly Interfaces CMOS & TTL**
- **Improved Circuit Performance**
- **Increased Reliability**

Product Summary

Part Number	Package	$R_{DS(on)}$	I_D	BV_{DSS}
VQ1004P	14 Pin DIP, Side Braze	3.5Ω	0.46A	60V
VQ1004J	14 Pin DIP, Plastic			
VQ1006P	14 Pin DIP, Side Braze	4.5Ω	0.40A	90V
VQ1006J	14 Pin DIP, Plastic			



TOP VIEW

ORDER NUMBER: VQ1004P, VQ1004J, VQ1006P, VQ1006J

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Drain-Source Voltage
- VQ1004P, J 60V
- VQ1006P, J 90V

Drain-Gate Voltage
- VQ1004P, J 60V
- VQ1006P, J 90V

Gate Current (Peak) ..... ±1A

Gate-Source Voltage ..... ±30V

Drain Current Continuous[1]
- VQ1004P, J ..... ±0.46A
- VQ1006P, J ..... ±0.40A

Drain Current
- Pulsed[2] ..... ±2A

Note 1: Single device alone. Package limited.
Note 2: Pulse test: 80μs to 300μs, 1% duty cycle.

Power Dissipation
- Single 1.30W
- Quad 2W

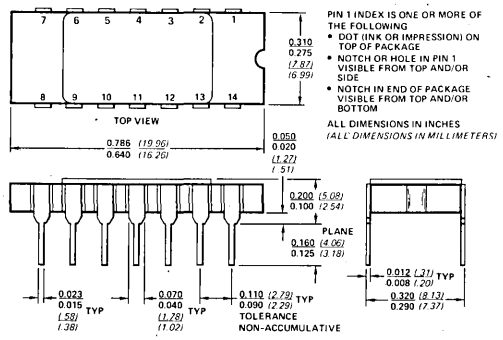
Linear Derating Factor
- Single ..... 10.4mW/°C
- Quad ..... 16mW/°C

Thermal Resistance
- Single ..... 96.2°C/W
- Quad ..... 62.5°C/W

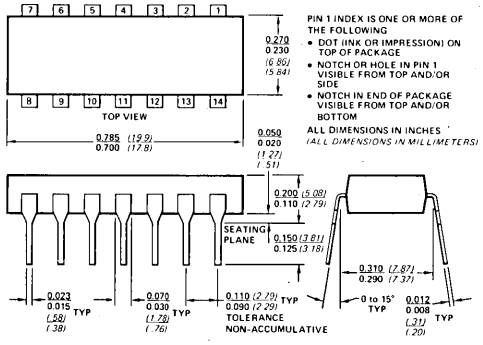
Operating and Storage Temperature ..... −55°C to +150°C

Lead Temperature (1/16″ from case for 10 secs) ..... +300°C

PACKAGE DIMENSIONS



14-LEAD DUAL-IN-LINE PACKAGE (P)
(SIDE BRAZE)



14-LEAD DUAL-IN-LINE PACKAGE (J)
(PLASTIC)

See Product Selector Guides on Pages 2833-2834.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Parameter		Part Number	Min	Max	Unit	Test Conditions
Static						
BV_{DSS}	Drain-Source Breakdown	VQ1004	60		V	V_{GS} = 0, I_D = 10μA
		VQ1006	90			
$V_{GS(th)}$	Gate-Source Threshold Voltage	All	0.8	2.5	V	V_{DS} = V_{GS}, I_D = 1mA
I_{GSS}	Gate Body Leakage	All		100	nA	V_{GS} = 15V, V_{DS} = 0
				500		V_{GS} = 15V, V_{DS} = 0, T_A = 125°C
I_{DSS}	Zero Gate Voltage Drain Current	All		1	μA	V_{GS} = 0, V_{DS} = 0.8 Max Rating
				500		V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$V_{DS(on)}$	Drain-Source Saturation Voltage[1]	All		1.5	V	V_{GS} = 5V, I_D = 0.3A
		VQ1004		3.5		V_{GS} = 10V, I_D = 1A
		VQ1006		4.5		
$r_{DS(on)}$	Drain-Source On Resistance[1]	All		5	Ω	V_{GS} = 5V, I_D = 0.3A
		VQ1004		3.5		V_{GS} = 10V, I_D = 1A
		VQ1006		4.5		
$I_{D(on)}$	On-State Drain Current[1]	All	1.5		A	V_{GS} = 10V, V_{DS} = 25V
Dynamic						
g_{fs}	Forward Transconductance[1]	All	170		mS	V_{DS} = 25V, I_D = 0.5A
C_{iss}	Input Capacitance	All		60	pF	V_{DS} = 25V, V_{GS} = 0, f = 1MHz
C_{rss}	Reverse Transfer Capacitance	All		10		
C_{oss}	Common-Source Output Capacitance	All		50		
t_{ON}	Turn-ON Time	All		10	ns	V_{DD} = 25V, R_L = 23Ω, R_g = 25Ω, I_D ≈ 1A
t_{OFF}	Turn-OFF Time	All		10		
Drain-Source Diode Characteristics						
			Typ			
V_{SD}	Forward ON Voltage[1]	All	−0.9		V	V_{GS} = 0, I_S = −1A
t_{rr}	Reverse Recovery Time	All	35		ns	V_{GS} = 0, I_F = I_R = 1A

Note 1: Pulse test — 80μs to 300μs, 1% duty cycle

TEST CIRCUITS

FIGURE 1. Switching Test Circuit

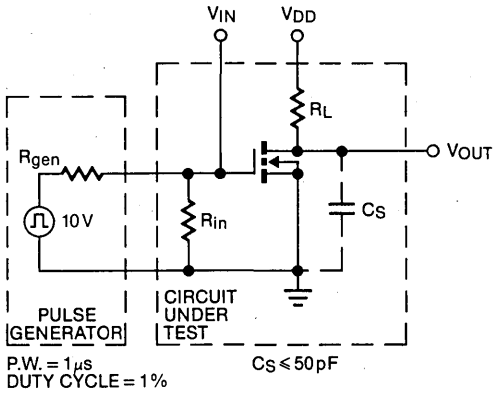
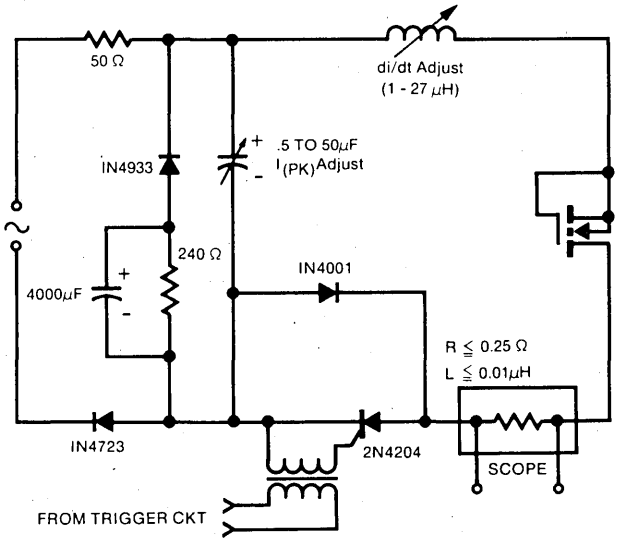


FIGURE 2. JEDEC Reverse Recovery Circuit



VQ2006P ■ VQ2006J

Siliconix

90V P-Channel Enhancement Mode Quad MOSPOWER Array

This power FET is designed especially for low power high frequency inverters, interface to CMOS and TTL logic, line drivers and Analog Switching.

FEATURES

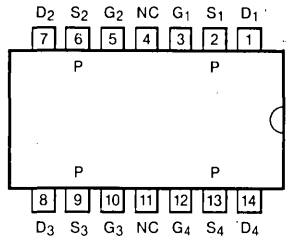
- **High Input Impedance**
- **Extremely Fast Switching**
- **Rugged**
- **Internal Drain-Source Diode**
- **Dual-In-Line Package for Packing Density and Automatic Insertion**

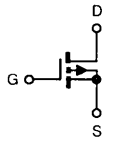
BENEFITS

- **Reduced Component Count**
- **Simpler Designs**
  - **— Directly Interfaces CMOS & TTL**
- **Improved Circuit Performance**
- **Increased Reliability**

Product Summary

Part Number	BV_{DSS} (Volts)	$R_{DS(ON)}$ (Ohms)	Package
VQ2006P	−90	5	Side Braze
VQ2006J	−90	5	Plastic





TOP VIEW
ORDER NUMBER: VQ2006P, VQ2006J

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Drain-Source Voltage ..... −90V

Drain-Gate Voltage ..... −90V

Drain Current
- Continuous[1] ..... ±410mA
- Pulsed[1,2] ..... ±3.0A

Gate-Source Voltage ..... ±20V

Gate Current Peak ..... ±1A

Power Dissipation
- Single 1.30W
- Quad 2W

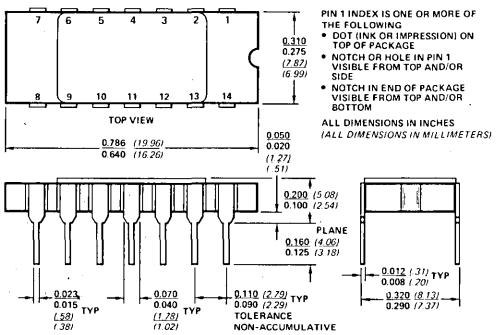
Linear Derating Factor
- Single ..... 10.4mW/°C
- Quad ..... 16mW/°C

Operating and Storage Temperature ..... −55°C to +150°C

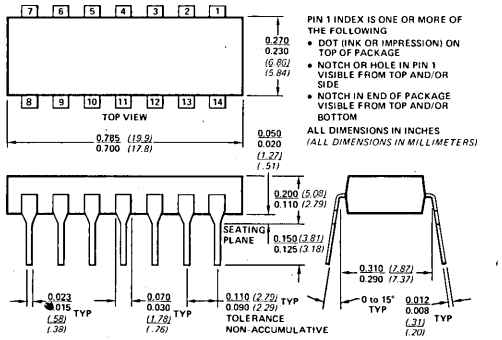
Lead Temperature (1/16" from case for 10 secs) ..... +300°C

Note 1: Single device alone. Package limited.
Note 2: Pulse test: 80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



14-LEAD DUAL-IN-LINE PACKAGE (P)
(SIDE BRAZE)



14-LEAD DUAL-IN-LINE PACKAGE (J)
(PLASTIC)

See Product Selector Guides on Pages 2833-2834.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Parameter		Min	Max	Unit	Test Conditions
Static					
BV_{DSS}	Drain-Source Breakdown	−90		V	V_{GS} = 0, I_D = −10μA
$V_{GS(th)}$	Gate Threshold Voltage	−2.0	−4.5	V	V_{DS} = V_{GS}, I_D = −1mA
I_{GSS}	Gate Body Leakage		−100	nA	V_{GS} = −30V, V_{DS} = 0
			−500		V_{GS} = −30V, V_{DS} = 0, T_A = 125°C
I_{DSS}	Zero Gate Voltage Drain Current		−10	μA	V_{GS} = 0, V_{DS} = −90V
			−500		V_{GS} = 0, V_{DS} = −90V, T_A = 125°C
$V_{DS(on)}$	Drain-Source Saturation Voltage[1]		−5.0	V	V_{GS} = −10V, I_D = −1A
$r_{DS(on)}$	Drain-Source On Resistance[1]		5.0	Ω	V_{GS} = −10V, I_D = −1A
$I_{D(on)}$	On-State Drain Current[1]	−1.0		A	V_{GS} = −10V, V_{DS} = −15V
Dynamic					
g_{fs}	Forward Transconductance[1]	200		mS	V_{DS} = −25V, I_D = −500mA
C_{iss}	Input Capacitance		150	pF	V_{DS} = −25V, V_{GS} = 0, f = 1MHz
C_{rss}	Reverse Transfer Capacitance		20		
C_{oss}	Common-Source Output Capacitance		60		
t_{ON}	Turn-ON Time		15	ns	V_{DD} = −25V, R_L = 23Ω, R_g = 25Ω, I_D ≈ −1A (Figure 1)
t_{OFF}	Turn-OFF Time		15		
Drain-Source Diode Characteristics					
		Typ			
V_{SD}	Forward ON Voltage[1]	0.9		V	V_{GS} = 0, I_S = 0.5A
t_{rr}	Reverse Recovery Time	65		ns	V_{GS} = 0, I_F = I_R = −0.5A (Figure 2)

Note 1: Pulse test — 80μs to 300μs, 1% duty cycle

VPMH10

TEST CIRCUITS

FIGURE 1. Switching Test Circuit

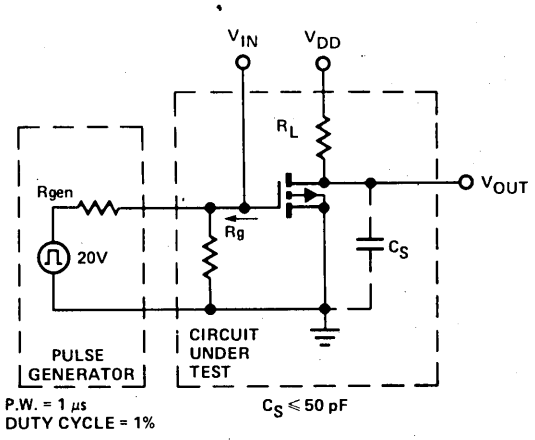
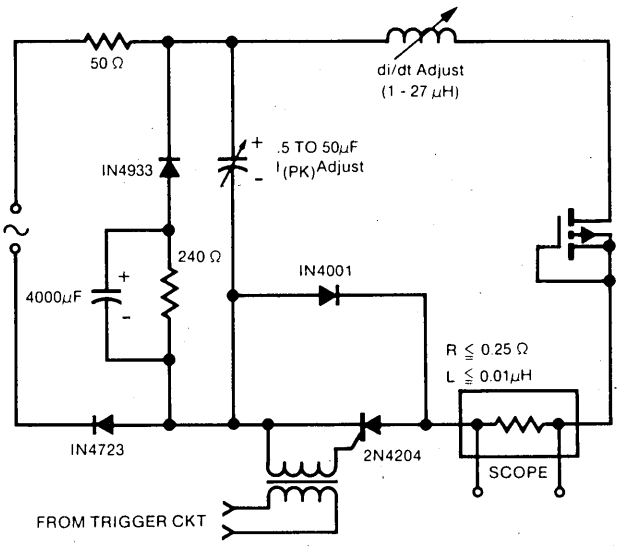


FIGURE 2. JEDEC Reverse Recovery Circuit



VQ3001P ■ VQ3001J

Siliconix
August 1982

30V Quad N-and P-Channel Enhancement Mode MOSPOWER

These power FETs are designed especially for low power high frequency inverters, interface to CMOS and TTL logic, line drivers and Analog Switching.

FEATURES

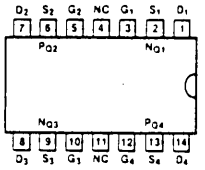
- **High Input Impedance**
- **Extremely Fast Switching**
- **Rugged**
- **Internal Drain-Source Diode**

BENEFITS

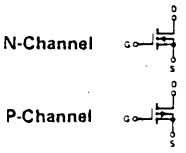
- **Reduced Component Count**
- **Simpler Designs**
  - **— Directly Interfaces CMOS & TTL**
- **Improved Circuit Performance**
- **Increased Reliability**

Product Summary

Part Number	BV_{DSS} Volts	$r_{DS(ON)}$ (ohms)	Package
VQ3001P	30	1 & 2	Side Braze
VQ3001J	30	1 & 2	Plastic



TOP VIEW

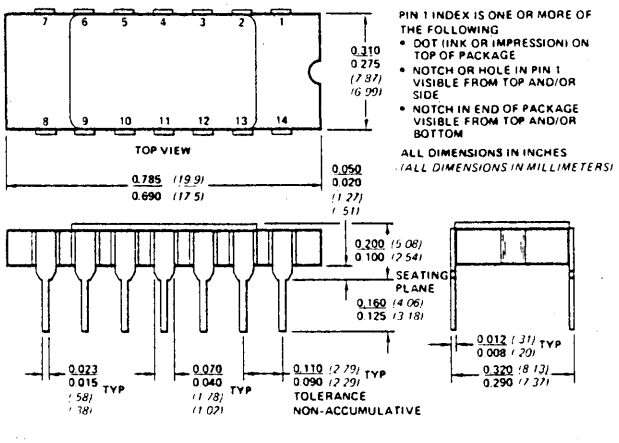


ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

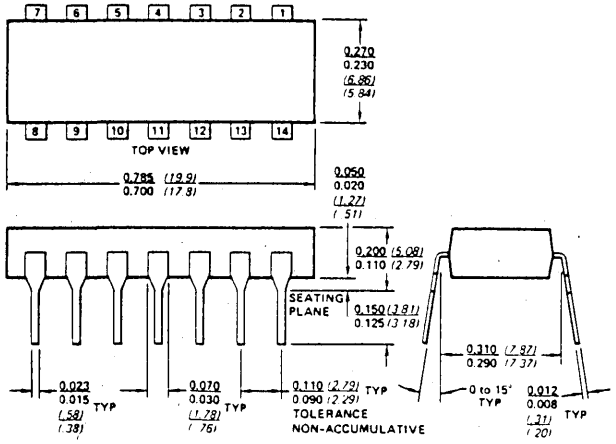
Drain-Source Voltage	30V
Drain-Gate Voltage	30V
Drain Current	
Continuous[1]	
P-Channel	±600 mA
N-Channel	±850 mA
Pulsed[2]	
P-Channel	±2.0A
N-Channel	±3.0A
Gate Source Voltage	±20V
Power Dissipation	
Single	1.30W
Quad	2W
Linear Derating Factor	
Single	10.4mW/°C
Quad	16m W/°C
Operating and Storage	
Temperature	−55°C to +150°C
Lead Temperature	
(1/16" from Case for 10 secs)	+300°C

Note: 1. Single device alone. Limited by package dissipation.
2. Pulse Test: 80 μs - 300 μs, 1% Duty Cycle.

PACKAGE DIMENSIONS



14-LEAD DUAL-IN-LINE PACKAGE (P)
(SIZE-BRAZE)



14-LEAD DUAL-IN-LINE PACKAGE (J)
(PLASTIC)

ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise noted)

Symbol	Parameter	N-Channel		P-Channel		Unit	Test Conditions
		Min	Max	Min	Max		(Reverse Polarity for P-Channel)
Static							
BV_{DSS}	Drain Source Breakdown	30		-30		V	V_{GS}=0, I_D=10μA
$V_{GS(th)}$	Gate Threshold Voltage	0.8	2.5	-2.0	-4.5	V	V_{DS}=V_{GS}, I_D=1 mA
I_{GSS}	Gate Body Leakage		100		-100	nA	V_{DS}=0, V_{GS}=16V
			500		-500		V_{DS}=0, V_{GS}=16V, T_A=125 °C
I_{DSS}	Zero Gate Voltage Drain Current		10		-10	μA	V_{DS}=24V, V_{GS}=0
			500		-500		V_{DS}=24V, V_{GS}=0, T_A=125°C, Note 2
$I_{D(ON)}$	ON-State Drain Current[1]	2.0		-1.5		A	V_{GS}=12V, V_{DS}=15V
V_{DS}	Drain-Source On-State Voltage [1]		0.35			V	V_{GS}=5.V, I_D=200 mA
			1.0		-2.0		V_{GS}=12V, I_D=1 A
Dynamic							
g_{fs}	Forward Transconductance[1]	250		200		mS	V_{DS}= ±15V, I_D=±500mA
C_{iss}	Input Capacitance		100		150	pF	V_{GS}=0, V_{DS}=15V, f=1 MHz
C_{oss}	Output Capacitance		80		100		
C_{rss}	Reverse Transfer Capacitance		55		60		
t_{on}	Turn-On Time		30		30	ns	V_{DD}=15V, R_L=23Ω, R_g=25Ω ID ≈ 0.6A (Figure 1)
t_{off}	Turn-Off Time		30		30		
Drain-Source Diode Characteristics							
		Typ		Typ		Unit	
V_{SD}	Forward On Voltage	.72		.72		V	I_F=50 mA, V_{GS}=0
t_{rr}	Reverse Recovery Time	50		65		ns	I_F=I_R=0.5A, V_{GS}=0 (Figure 2)

Note 1: Pulse test — 80 μs to 300 μs, 1% duty cycle.

TEST CIRCUITS (Reverse Polarity for P-Channel)

FIGURE 1 Switching Test Circuit

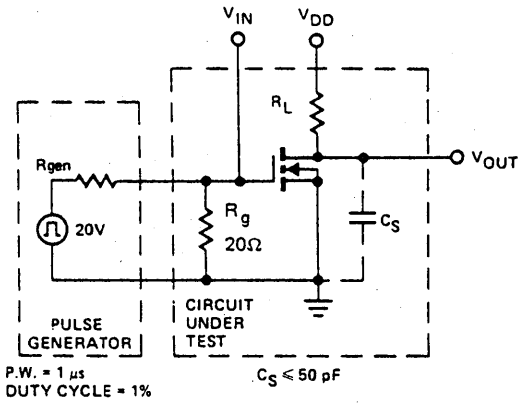
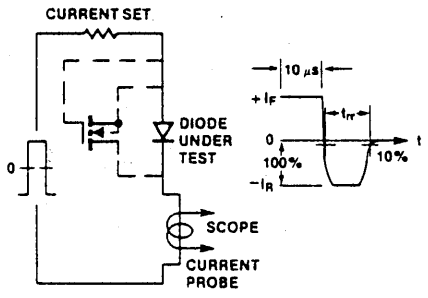


FIGURE 2 Reverse Recovery Test Circuit



SPRAGUE® THE MARK OF RELIABILITY

PERIPHERAL/DISPLAY DRIVER IC REFERENCE

Sink or Source in order of (1) output current rating, (2) output voltage rating, (3) number of drivers

TYPICAL DRIVING APPLICATIONS								OUTPUTS*			SPRAGUE PART NUMBER	EXTENDED TEMP. MILITARY HERM. AVAILABLE
DISPLAYS				INDUCTIVE		PRINTERS						
LED	V. FLUOR.	GAS DIS.	INCAND.	SOLENOID	MOTOR	THERMAL	ELECTRO. SENS.	mA	V	#		
SINK DRIVERS												
–	–	✓	–	–	–	–	–	5	130	5	UHP-480	✓
–	–	✓	–	–	–	–	–		130	7	UHP-481	✓
–	–	✓	–	–	–	–	–		130	8	UHP-482	✓
–	–	✓	–	–	–	–	–	20	−115	8	SERIES UDN-7180A	–
✓	–	–	✓	–	–	–	–	100	20	8	UDN-2595A	✓
✓	–	–	✓	✓	✓	✓	–	250	70	4	SERIES UHP-400	✓
✓	–	–	✓	✓	✓	✓	–		100	4	SERIES UHP-500	✓
SCR ARRAY			✓	✓	–	–	–	275	35	6†	UTN-2886B	–
SCR ARRAY			✓	✓	–	–	–		35	8†	UTN-2888A	–
✓	–	–	✓	✓	✓	✓	–	300	80	2	SERIES UDN-3610M	✓
✓	–	–	✓	✓	✓	✓	–		80	2	SERIES UDN-5710M	✓
✓	–	–	✓	✓	✓	✓	–		80	4	SERIES UDN-5700A	✓
✓	–	–	✓	✓	✓	✓	–		80	4	UDN-5733A	✓
PIN DIODE DRIVER				–	–	–	–		120	4	UDN-5790/91A	✓
✓	–	–	✓	✓	✓	✓	–	350	50	4†	UCN-4401A	✓
✓	–	–	✓	✓	✓	–	–		50	7	SERIES ULN-2000A	✓
✓	–	–	✓	✓	✓	–	–		50	8	SERIES ULN-2800A	✓
✓	–	–	✓	✓	✓	✓	–		50	8†	UCN-4801A	✓
✓	–	–	✓	✓	–	✓	✓		50	8†	UCN-4821A	✓
✓	–	–	✓	✓	–	✓	✓		80	8†	UCN-4822A	✓
✓	–	–	✓	✓	✓	–	–		95	7	SERIES ULN-2020A	✓
✓	–	–	✓	✓	✓	–	–		95	8	SERIES ULN-2820A	✓
✓	–	–	✓	✓	–	✓	✓		100	8†	UCN-4823A	✓
STEPPER MOTOR DRIVER				–	✓	–	–	500	35	4	UCN-4202/03A	–
✓	–	–	✓	✓	✓	–	–		50	7	SERIES ULN-2010A	✓
✓	–	–	✓	✓	✓	–	–		50	8	SERIES ULN-2810A	✓
✓	✓	–	✓	✓	–	–	–		50	8†	UCN-4807/08A	✓
FULL-BRIDGE				–	✓	–	–	±1000	36	1	UDN-2952B	–
✓	–	–	✓	✓	✓	✓	–	1250	60	4	UDN-2540B	–
✓	–	–	✓	✓	✓	–	–	1500	50	2	ULN-2061M	–
✓	–	–	✓	✓	✓	–	–		50	4	SERIES ULN-2064B	✓
✓	–	–	–	✓	✓	–	✓		−50	4	SERIES UDN-2840B	–
✓	–	–	✓	✓	✓	–	–		80	2	ULN-2062M	–
✓	–	–	✓	✓	✓	–	–		80	4	SERIES ULN-2065B	✓
HALF-BRIDGE				–	✓	–	–	±2000	30	1	UDN-2949Z	–
FULL-BRIDGE				–	✓	–	–		36	1	UDN-2952W	–
SOURCE DRIVERS												
–	✓	✓	–	–	–	–	–	−15	−80	5	UHP-490	✓
–	✓	✓	–	–	–	–	–		−80	6	UHP-491	✓
–	✓	✓	–	–	–	–	–		−80	6	UHP-495	✓
–	✓	–	–	–	–	–	–	−25	±40	8	SERIES UDN-6138A	–
–	✓	–	–	–	–	–	–		60	8†	UCN-4815A	✓
✓	✓	–	✓	–	–	–	–		60	10†	UCN-4810A	✓
–	–	✓	–	–	–	–	–		115	6	SERIES UDN-6116A	–
–	✓	✓	–	–	–	–	–		115	6	UDN-6164A	–
–	–	✓	–	–	–	–	–		115	8	SERIES UDN-6118A	–
–	✓	✓	–	–	–	–	–		115	8	UDN-6184A	–
–	–	✓	–	–	–	–	–		140	8	UDN-6514A	–
–	–	✓	–	–	–	–	–		200	8	UDN-6510A	–
✓	–	–	✓	✓	–	–	–	−350	20	8	UDN-2585A	✓
✓	–	–	✓	✓	✓	✓	✓		50	8	UDN-2981/82A	✓
–	–	–	–	✓	–	–	–		−80	5	UDN-2956/57A	–
✓	✓	–	✓	✓	–	–	–		80	8	SERIES UDN-2580A	✓
✓	–	–	✓	✓	–	–	–		80	8	SERIES UDN-2588A	✓
✓	✓	–	✓	✓	✓	✓	✓		80	8	UDN-2983/84A	✓
FULL-BRIDGE				–	✓	–	–	±1000	36	1	UDN-2952B	–
✓	–	–	✓	✓	✓	–	–	−1500	50	2	ULN-2061M	–
✓	–	–	✓	✓	✓	–	–		50	4	SERIES ULN-2074B	✓
✓	–	–	–	✓	✓	–	✓		−50	4	SERIES UDN-2840B	–
✓	–	–	✓	✓	✓	–	–		80	2	ULN-2062M	–
✓	–	–	✓	✓	✓	–	–		80	4	SERIES ULN-2075B	✓
HALF-BRIDGE				–	✓	–	–	±2000	30	1	UDN-2949Z	–
FULL-BRIDGE				–	✓	–	–		36	1	UDN-2952W	–

*Current is maximum tested condition, voltage is absolute maximum rating. † Latched Driver.

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TELEDYNE SEMICONDUCTOR

TSC450 Dual Power MOSFET Driver

General Description

The TSC450 is a low cost dual driver with TTL compatible inputs and high voltage outputs. Each device may be configured in an inverting or non-inverting configuration. The active pullup, high voltage outputs will drive power MOSFET gates.

The TSC450 also serves as a logic level translator and discrete analog switch driver.

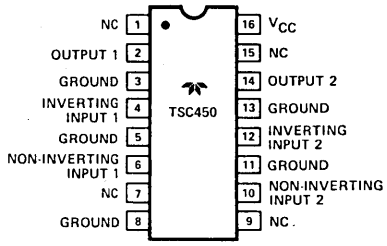
Features

- Dual Device for High Packing Density
- User Selectable Inverting or Non-Inverting Operation
- Single Supply Operation
- TTL Compatible Inputs
- High Output Sink Current ..... 12 mA
- High Output Source Current ..... 6 mA
- Fast Switching ..... 125 ns
- Available with Mil-STD-883B Processing

Ordering Information

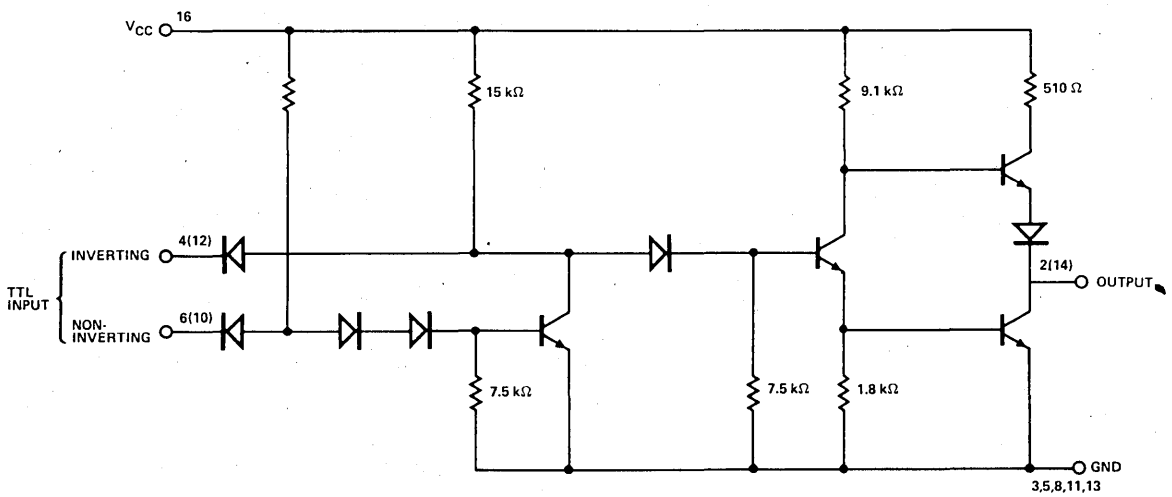
Part No.	Supply Voltage	Temp. Range	Package
TSC450AIJE	15 V	-25°C to +85°C	16 Pin CerDIP
TSC450ACPE	15 V	0°C to +70°C	16 Pin Epoxy
TSC450BIJE	12 V	-25°C to +85°C	16 Pin CerDIP
TSC450BCPE	12 V	0°C to +70°C	16 Pin Epoxy
TSC450AMJE	15 V	-55°C to +125°C	16 Pin CerDIP
TSC450BMJE	12 V	-55°C to +125°C	16 Pin CerDIP
TSC450 AMJE/883	15 V	MIL-STD-883B Processing -55°C to +125°C	16 Pin CerDIP
TSC450 BMJE/883	12 V	MIL-STD-883B Processing -55°C to +125°C	16 Pin CerDIP

Pin Configuration



NC = No Connection

Functional Diagram (1/2 Circuit)



TELEDYNE SEMICONDUCTOR

TELEDYNE SEMICONDUCTOR

TSC 700A

Four Digit LED Display Decoder and Driver High Segment Drive Current

General Description

The TSC700A drives common anode LED displays with 28 high current, open-drain N channel output transistors. Four seven segment LED displays may be driven. Drive current is guaranteed to be 11 mA minimum. This is twice the minimum drive current available from comparable devices and will provide high LED luminance. High luminous intensity is an important factor when a dark contrasting background is unavailable or the LED is viewed at a distance. The TSC700A current capability makes it an ideal large character LED driver.

Four data bit inputs and four digit select signals permit interfacing to multiplexed BCD or binary output devices. The four bit data input is decoded into the seven segment alphanumeric code known as "Code B". A 0 to 9, —, E, H, L, P or "blank" reading may be displayed.

An added feature includes a brightness control input that adjusts segment drive current. The control pin may also be used as a digital display enable. The TSC700A is an improved pin compatible and functional equivalent to the ICM7212A.

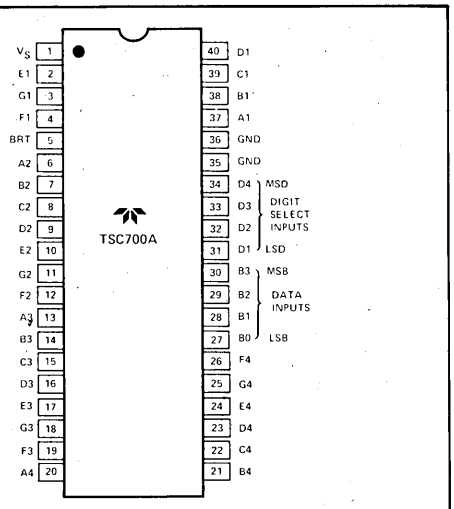
Features

- High Drive Current for High Luminance LED Display
- Guaranteed High LED Segment Current 11 mA Minimum
- 28 Common Anode LED Drivers (4 Digits)
- Code B Output Format ... 0 to 9, —, E, H, L, P, "blank"
- BCD/Binary Input to 7 Segment LED Code
- Four Separate Digit Selects for Multiplexed Input
- Digital or Analog Brightness Control
- Digital Display Enable
- Low Thermal Resistance Package
- Military Temperature Range Devices Available
- Pin Compatible With TSC7212A, ICM7212A

Ordering Information

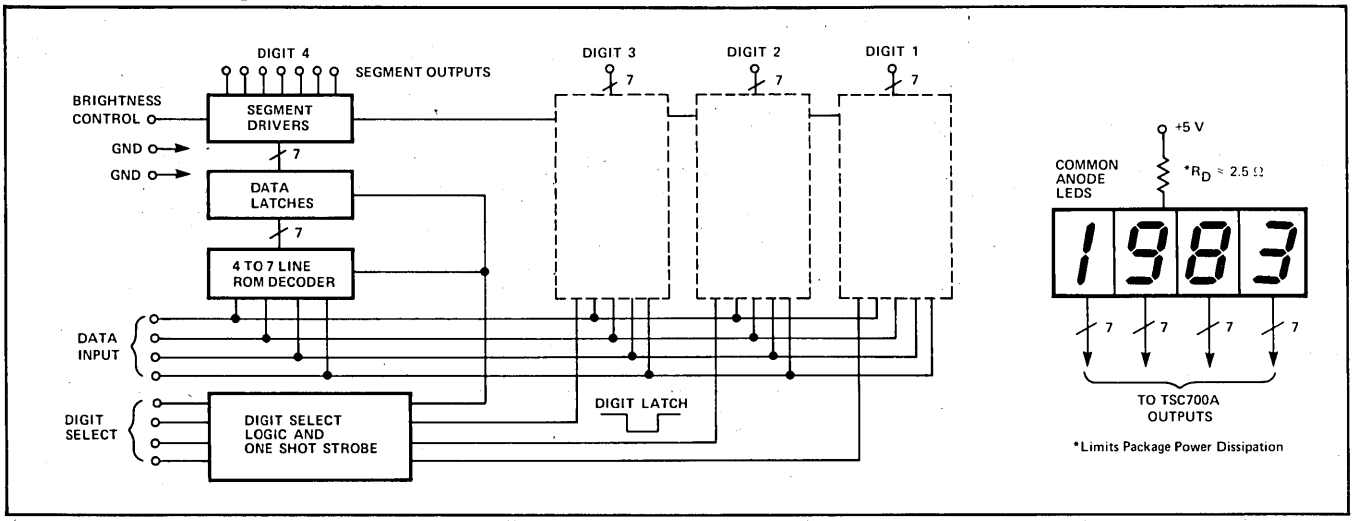
Part No.	Package	Temp. Range	LED Segment Current	Output Code
TSC700AMJL	40 Pin CerDIP	-55°C to +125°C	14 mA	Code B
TSC700AIJL	40 Pin CerDIP	-25°C to +85°C	14 mA	Code B
TSC700 AMJL/883	40 Pin CerDIP	-55°C to +125°C	14 mA	Code B
TSC700A/Y	CHIP	25°C	14 mA	Code B

Pin Configuration



If Brightness Control is not needed, connect BRT (pin 5) to V_S.

Functional Diagram



TELEDYNE SEMICONDUCTOR

TELEDYNE SEMICONDUCTOR

TSC7109

12-Bit Plus Sign CMOS A/D Converter – Microprocessor/UART Interface

General Description

The TSC7109 is a 12-bit plus sign CMOS low power A/D converter. The single CMOS IC contains all the necessary active devices to interface with microprocessors.

In direct mode, Chip Select and High/Low Byte Enables control parallel bus interface. In the handshake mode the TSC7109 will operate with industry standard UARTs in controlling serial data transmission, ideal for remote data logging. Control and monitoring of conversion timing is provided by the RUN/$\overline{\text{HOLD}}$ and STATUS outputs. The TSC7109 requires only the addition of 8 passive components plus a crystal to operate as a dual slope integrating A/D converter. The TSC7109 has features that make it an attractive per-channel alternative to analog multiplexing for many data acquisition applications. These features include typical input bias current of 1 pA, drift of less than 1 μV/°C, input noise typically 15 μV p-p, and auto-zero. True differential input and reference allows the measurement of bridge-type transducers such as load cells, strain gauges and temperature transducers.

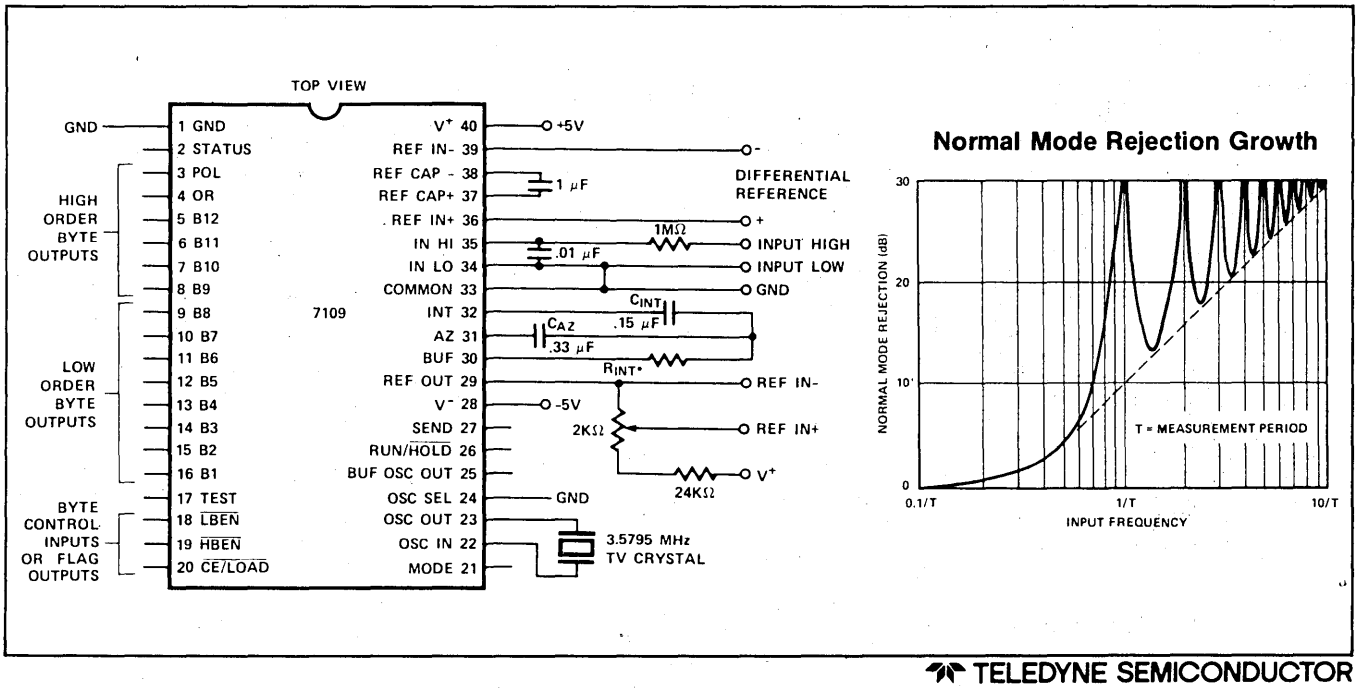
Ordering Information

Part No.	Temp. Range	Package
TSC7109MDL	-55°C to +125°C	40 Pin CerDIP
TSC7109IDL	-25°C to +85°C	40 Pin CerDIP
TSC7109CPL	0°C to +70°C	40 Pin Plastic
TSC7109IJL	0°C to +70°C	40 Pin CerDIP

Features

- 12-bit plus sign integrating analog-to-digital converter with overrange indication
- Sign magnitude coding format
- True differential signal input and differential reference input
- Low noise — typically 15 μV p-p
- High normal mode noise and line frequency rejection
- 1 pA typical input current
- No zero adjustment potentiometer needed
- TTL compatible byte organized Tri-State outputs
- UART handshake mode for simple serial data transmission
- Direct bus connection to 8 or 16-bit bus
- Dual mode on-chip oscillator
  - 3.58 MHz crystal provides 7.5 conversions per second for 60 Hz rejection
  - External RC network provides up to 30 conversions per second
- Power dissipation typically less than 20 mW

Pin Configuration



TELEDYNE SEMICONDUCTOR

TELEDYNE SEMICONDUCTOR

TSC7126
Low Power 3 1/2 Digit CMOS A/D Converter
— 50 Microamp Supply Current

General Information

The TSC7126 is designed to operate from a 9 volt battery drawing 50 μA typical, 100 μA maximum supply current. The single CMOS IC 3-1/2 digit A/D converter contains all the necessary active devices including seven segment decoders, liquid crystal display drivers, backplane drive, clock and reference.

With an auto zero less than 10 μV, zero drift less than 1 μV/° C, input bias current of 10 pA max and rollover error of less than one count, the TSC7126 brings exceptional value to the portable battery powered field.

In addition, the differential input and reference allows the measurement of load cells, strain gauges and other bridge type transducers. The TSC7126 can be used as a plug-in replacement for the TSC7106 changing only the values of the seven passive components.

Ordering Information

Part Number	Temp. Range	Package
TSC7126CDL	0-70° C	40 pin Ceramic DIP
TSC7126CPL	0-70° C	40 pin Plastic DIP

Features

- 8000 hours typical 9 volt battery life
- Pin compatible with TSC7126
- Auto-zero, auto-polarity
- True polarity at zero for precise null detection
- True differential input and reference
- 1 pA input current
- Direct LCD Display drive — no external components required
- Low noise — less than 15 μV p-p
- On-chip clock and reference
- Power dissipation typically less than 1 mW
- No other active circuits required

Applications

- Portable Instruments
- Multimeters
- Digital Voltmeters
- Digital Thermometers
- Digital Bridges (strain gauges, load cells)
- Ph meters

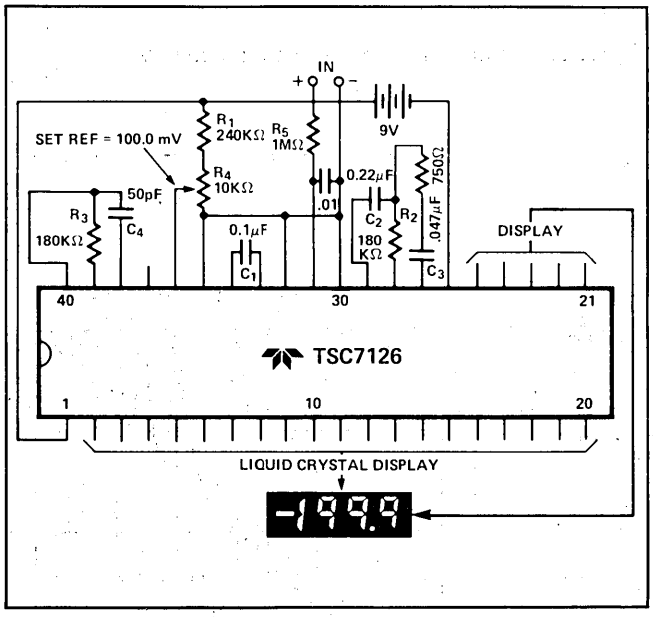


Figure 1: Typical Circuit Configuration for 3 readings/second

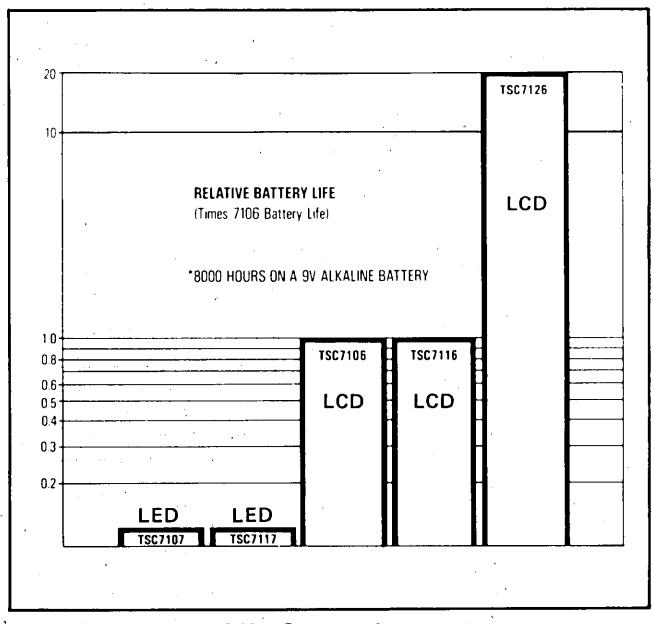


Figure 2: Battery Life Comparisons

TSC7126

Low Power 3 1/2 Digit CMOS A/D Converter
— 50 Microamp Supply Current

Absolute Maximum Ratings*

Supply Voltage (V^+ to V^-) 15V
Analog Input Voltage (either input)[1] ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... Test to V^+

Power Dissipation[2]
Ceramic Package ..... 1000 mW
Plastic Package ..... 800 mW
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... —65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

Electrical Characteristics[3]

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V Full Scale = 200.0 mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ V_{REF} = 100 mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN} = +V_{IN} \simeq$ 200.0 mV	-1	±0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full Scale = 200 mV or Full Scale = 2.000 V	-1	±0.2	+1	Counts
Common Mode Rejection Ratio[4]	V_{CM} = ±1V, V_{IN} = 0V. Full Scale = 200.0 mV		50		μV/V
Noise (Pk - Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0 mV		15		μV
Leakage Current @ Input	V_{IN} = 0V		1	10	pA
Zero Reading Drift	V_{IN} = 0 0° < T_A < 70°C		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0 mV 0 < T_A < 70°C (Ext. Ref. 0 ppm/°C)		1	5	ppm/°C
Supply Current (Does not include Common current)	V_{IN} = 0 (Note 6)		50	100	μA
Analog Common Voltage (with respect to positive supply)	250KΩ between Common and positive supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog Common (with respect to positive supply)	250KΩ between Common and positive supply		80		ppm/°C
Pk-Pk Segment Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
Pk-Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
Power Dissipation Capacitance	vs. Clock Frequency		40		pF

Notes:
1. Input voltages may exceed the supply voltages provided the input current is limited to ±100 μA.
2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3. Unless otherwise noted, specifications apply at T_A = 25°C, f_{clock} = 16kHz and are tested in the circuit of Figure 1.
4. Refer to "Differential Input" discussion on page 4.
5. Backplane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50 mV.
6. During auto zero phase, current is 10-20 μA higher. 48 kHz oscillator, Figure 2, increases current by 8 μA (typ.)

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

3-1/2 Digit ADC Family Comparison

Part No.	10 μV Resolution	Low Power ($I_S \leq$ 100 μA)	Single Supply	Internal Reference	Differential Input	Differential Reference	Display "Hold" Feature	LCD Drive	LED Drive
TSC7106	X		X	X	X	X		X	
TSC7126	X	X	X	X	X	X		X	
TSC7116	X		X	X	X		X	X	
TSC7107	X			X	X	X			X
TSC7117	X			X	X		X		X

TELEDYNE SEMICONDUCTOR

TELEDYNE SEMICONDUCTOR

TSC7135
4 1/2 Digit Precision Analog-to-Digital Converter

General Description

The TSC7135 4 1/2 digit analog converter offers 50 ppm (1 part in 20,000) resolution with a maximum linearity error of 1 count. An auto-zero cycle reduces the zero error to below 10 μV and zero drift to 0.5 μV/°C. Source impedance error sources are minimized by a 10 pA maximum input current. Rollover error is limited to ± 1 count.

By combining the TSC7135 with a TSC7211A (LCD), TSC7212A (LED) or TSC700A (High LED Segment Current) driver a 4 1/2 digit display DVM or DPM can be constructed. Overrange and underrange signals support automatic range switching and special display blanking/flashing applications.

Micro-processor based measurement systems are supported by the TSC7135 Busy, Strobe and Run/HOLD control signals. Remote data acquisition systems with data transfer via UART are also possible. The additional control pins and multiplexed BCD outputs make the TSC7135 the ideal converter for display or μ-processor based measurement systems.

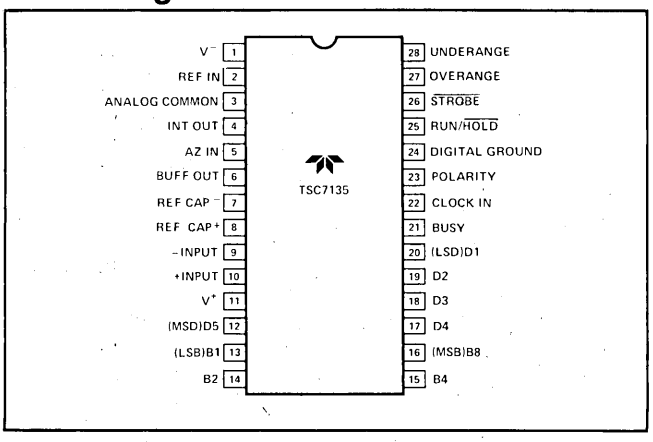
Features

- Low Rollover Error ..... ± 1 Count Maximum
- Guaranteed ± 1 Count Maximum Error
- Guaranteed Zero Reading for 0 V Input
- True Polarity Indication at Zero for Null Detection
- Multiplexed BCD Data Output
- TTL Compatible Outputs
- Differential Input
- Control Signals Permit Interface to UARTS and μ-Processors
- Auto-ranging Supported with Over and Underrange Signals
- Blinking Display Visually Indicates Overrange Condition
- Low Input Current ..... 1 pA
- Low Zero Reading Drift ..... 2 μV/°C
- Interface to TSC7211A, TSC7212A, and TSC700A Display Drivers

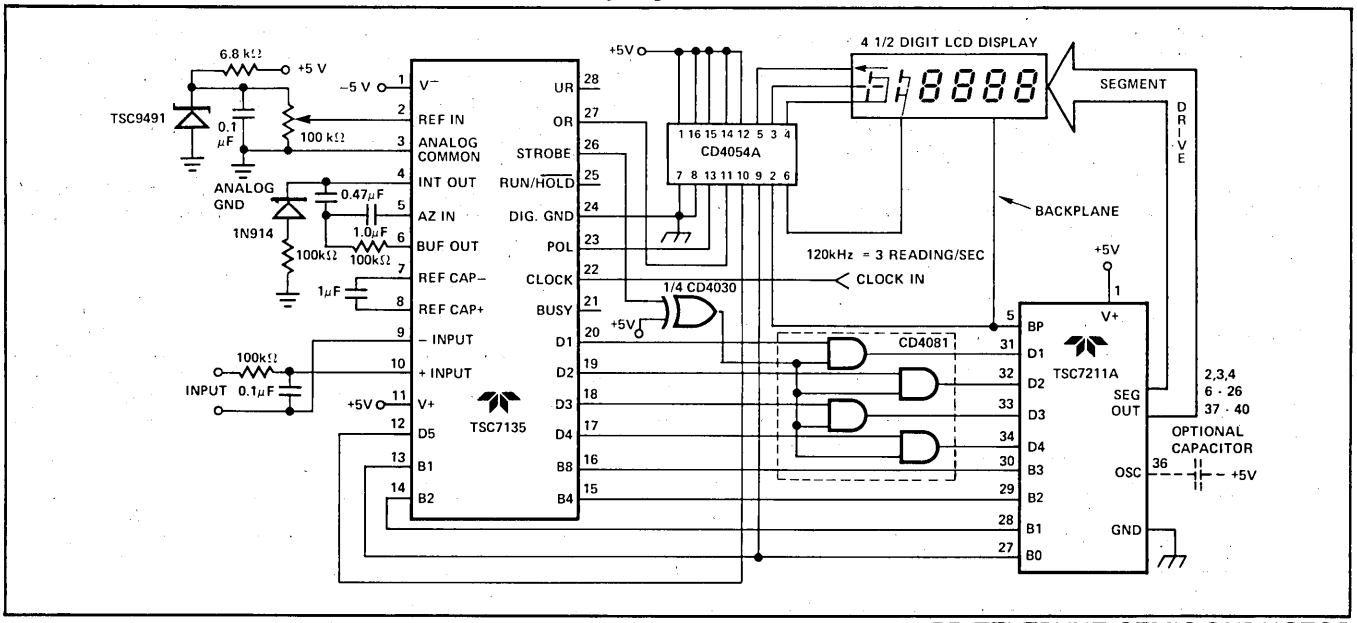
Ordering Information

Part No.	Package	Temperature Range
TSC7135CJI	28 Pin CerDIP	0°C to +70°C
TSC7135CPI	28 Pin Plastic	0°C to +70°C

Pin Configuration



Typical 4 1/2 Digit DVM with LCD Display



TELEDYNE SEMICONDUCTOR

Absolute Maximum Ratings (Note 1)

Positive Supply Voltage ..... +6 V
Negative Supply voltage ..... -9 V
Analog Input Voltage (Pin 9 or 10) ..... V^+ to V^- (Note 2)
Reference Input Voltage (Pin 2) ..... V^+ to V^-
Clock Input Voltage ..... 0 V to V^+

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +160°C
Soldering Lead Temperature (10 Seconds) ..... 300°C
CerDIP(J) Package Power Dissipation ..... 1 W
Plastic(P) Package Power Dissipation ..... 0.8 W

Electrical Specifications: T_A = 25°C, f_{CLOCK} = 120 kHz, V^+ = 5.0 V, V^- = -5 V

TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC7135 MIN	TYP	MAX	UNIT
ANALOG SECTION	1		Display Reading with Zero Volt Input	Note 3,4	-0.0000	±0.0000	+0.0000	Display Reading
	2	TC_Z	Zero Reading Temperature Coefficient	V_{IN} = 0 V Note 5	—	0.5	2	μV/°C
	3	TC_{FS}	Full Scale Temperature Coefficient	V_{IN} = 2 V Notes 5,6	—	—	5	ppm/°C
	4	NL	Nonlinearity Error	Note 7	—	0.5	1	count
	5	DNL	Differential Linearity Error	Note 7	—	0.01	—	LSB
	6		Display Reading In Ratiometric Operation	V_{IN} = V_{REF} Note 3	+0.9998	+0.9999	+1.0000	Display Reading
	7	±FSE	± Full Scale Symmetry Error (Rollover Error)	-V_{IN} = +V_{IN} Note 8	—	0.5	1	count
	8	I_{IN}	Input Leakage Current	Note 4	—	1	10	pA
	9	V_N	Noise	Peak-to-Peak Value not exceed 95% of time	—	15	—	μV_{p-p}
DIGITAL SECTION	10	I_{NL}	Input Low Current	V_{IN} = 0 V	—	10	100	μA
	11	I_{NH}	Input High Current	V_{IN} = +5 V	—	0.08	10	μA
	12	V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA	—	0.20	0.40	V
	13	V_{OH}	Output High Voltage (B_1, B_2, B_4, B_8, D_1 - D_5)	I_{OH} = 1 mA	2.4	4.4	5.0	V
	14	V_{OH}	Output High Voltage (Busy, Polarity, Overrange, Underrange, Strobe)	I_{OH} = 10 μA	4.9	4.99	5.0	V
	15	f_{CLK}	Clock Frequency		0	120	200	kHz
POWER SUPPLY	16	V^+	Positive Supply Voltage		4	5	6	V
	17	V^-	Negative Supply Voltage		-3	-5	-8	V
	18	I^+	Positive Supply Current	f_{CLK} = 0 Hz	—	1.0	3.0	mA
	19	I^-	Negative Supply Current	f_{CLK} = 0 Hz	—	0.7	3.0	mA
	20	Pd	Power Dissipation	f_{CLK} = 0 Hz	—	8.5	30	mW

Notes:
1. Functional operation is not implied.
2. Limit input current to under 100 μA if input voltages exceed supply voltage.
3. Full Scale Voltage = 2.000 V.
4. V_{IN} = 0.0000 V.
5. 0°C ≤ T_A ≤ +70°C.
6. External Reference Temperature Coefficient less than 0.01 ppm/°C.
7. -2 V ≤ V_{IN} ≤ +2 V.
8. |V_{IN}| = 1.959 V.
9. Test Circuit shown in Figure 1.

TELEDYNE SEMICONDUCTOR

TSC7211A (LCD)
TSC7212A (LED)
Four Digit CMOS Display Decoder and Driver

General Description

The TSC7211A (LCD Decoder/Driver) and TSC7212A (LED Decoder/Driver) are direct drive, four digit, seven segment display decoder and drivers.

The TSC7211A drives conventional LCD displays. An RC oscillator, divider chain, backplane driver, and 28 segment outputs are provided on a single CMOS chip. The segment drivers supply square waves of the same frequency as the backplane but in phase for an OFF segment and out of phase for an ON segment. The net d.c. voltage applied between driver segment and backplane is zero.

The TSC7212A drives common anode LED displays with 28 current controlled, low leakage, open drain, N-Channel output transistors. The brightness control input can be used as a digital display enable. A varying voltage at the control input will allow continuous display brightness control.

The TSC7211A (LCD) and TSC7212A (LED) require only four data bit inputs and four digit select signals to interface with multiplexed BCD or binary output devices such as the ICM7217, ICM7226, ICL7103 and TSC7135. The four bit binary input code is decoded into the seven segment alphanumeric code known as "Code B."

The "Code B" output format results in a 0 to 9, —, E, H, L, P or blank display. True BCD or binary inputs will be correctly decoded to the seven segment display format.

The CMOS TSC7211A and TSC7212A are available in a 40 pin epoxy dual-in-line package. All inputs are protected against static discharge.

Ordering Information

Part No.	Driver Type	Package	Output Code	Input Config.
TSC7211AIPL	LCD	40 Pin Epoxy DIP	Code B	Multiplexed 4 Bit Binary or BCD
TSC7212AIPL	LED	40 Pin Epoxy DIP	Code B	Multiplexed 4 Bit Binary or BCD
TSC7211A/Y	LCD	DICE	Code B	Multiplexed 4 Bit Binary or BCD
TSC7212A/Y	LED	DICE	Code B	Multiplexed 4 Bit Binary or BCD

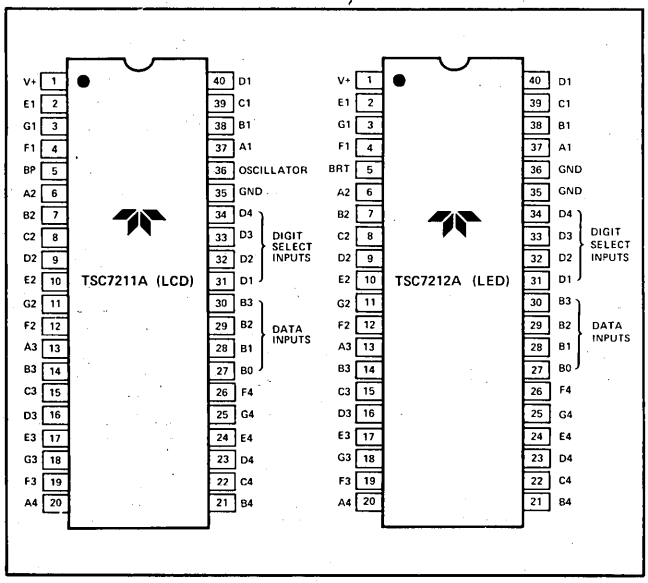
TSC7211A Features (LCD Driver)

- Four digit non-multiplexed 7 segment LCD display outputs with backplane driver.
- RC oscillator on chip generated backplane drive signal.
- Eliminates d.c. bias which degrade LCD display life.
- Backplane input/output pin permits synchronization of cascaded slave device to a master backplane signal.
- Separate digit select inputs to accept multiplexed BCD/binary inputs.
- Binary and BCD inputs decoded to code B (0 to 9, —, E, H, L, P, blank).
- Pin compatible and functionally equivalent to ICM7211A and DF411.

TSC7212A Features (LED Driver)

- 28 current limited outputs drive common anode LEDs at greater than 5 mA per segment.
- Brightness input allows potentiometer control of LED segment current. Pin also serves as digital display enable.
- Same input configuration and output decoding as the TSC7211A.
- Pin compatible and functionally equivalent to ICM7212A.

Pin Configuration



TELEDYNE SEMICONDUCTOR

TSC800
15 Bit Plus Sign Integrating Analog to Digital Converter
– 8/16 Bit μ-Processor Interface
– UART Interface

General Description

The TSC800 is a 15 bit plus sign integrating analog to digital converter. The TSC800 improves the conventional two phase dual slope conversion cycle by incorporating system zero and integrator output zero phases.

External zero nulling potentiometers are unneeded and over-range recovery time is enhanced. Conversion speed may be set to reject the 50, 60 and 400 Hz line frequency interference signals common in industrial environments.
Interface control signals support either single byte (16 bits) or two byte (8 bits) parallel data transfer to processor data busses. A "handshake" operating mode permits serial data transmission with a UART.

The high impedance differential inputs, 16 bit dynamic range and bus interface ease make the TSC800 the ideal converter in precision process control, data logging and "intelligent" measurement applications.

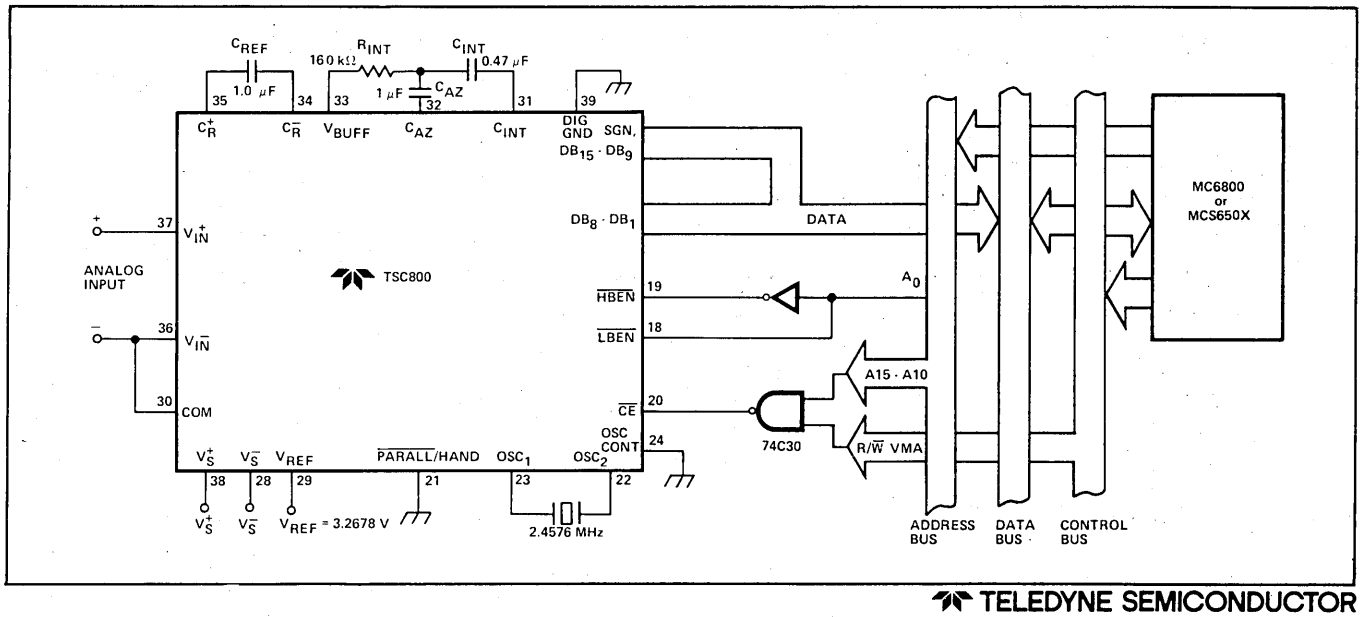
Ordering Information

Part No.	Package	Temp. Range	Max Linearity Error
TSC800AMJL	40 Pin CerDIP	MIL	2LSB
TSC800AIJL	40 Pin CerDIP	IND	2LSB
TSC800ACPL	40 Pin Plastic	COM	2LSB
TSC800BMJL	40 Pin CerDIP	MIL	4LSB
TSC800BIJL	40 Pin CerDIP	IND	4LSB
TSC800BCPL	40 Pin Plastic	COM	4LSB

Features

- 15 Bit Resolution Plus Sign Bit
  - 96 dB Dynamic Range
- Integrating Dual Slope Converter
  - Monotonic
  - Eliminate 50/60 Hz "Line" Interference
  - High Noise Immunity
  - Auto Zero Cycle Eliminates Trimming
  - Incorporates Integrator Zero Cycle for Fast Overload Recovery
- Three State Data Bit/Sign Bit Outputs
  - 8 or 16 Bit Parallel Data Transfer to μ-Processor Bus
- UART Control Signals
  - Serial Data Transmission
  - "Handshake" Data Transfer
  - Distributed Control Systems
  - Fiber Optic Transmission Systems
- Easy Conversion Cycle Monitoring and Control
  - Data Valid Output Signal
  - Continuous or Convert on Command Operation
- High Impedance Differential Input
  - 15 pA Maximum Input Current
- Low Input Noise
  - 15 μ V_{p-p}
- On Chip Crystal Oscillator for 2.5 Conversions/ Sec.
  - f_{xtal} = 2.4576 MHz
  - 100 mSEC Integration Period Rejects 50, 60, 400 Hz Interference Signals
- Convenient ±5 V Supply Operation
  - Low Power Dissipation ..... 20 mW

Typical μ-Processor Interface



TELEDYNE SEMICONDUCTOR

TELEDYNE SEMICONDUCTOR

TSC9403
TSC9404
Serial Input/16 Bit Parallel Output Peripheral Driver — High Voltage, High Current Outputs

General Description

The Teledyne Semiconductor TSC 9403 and TSC 9404 are serial input, 16 bit parallel output shift registers. High output power MOS switching transistors make the TSC 9403 and TSC 9404 ideal interface circuits between microprocessor I/O ports and high current/voltage peripherals. The MOS construction limits quiescent power dissipation to 20 mW.

The TSC 9403 common source, open drain MOS outputs sustain 20V in the OFF state and maintain leakage currents under 100 μA. The TSC 9404 outputs are rated at 15V. The 16 parallel outputs will continuously sink 60 mA. ($V_{SAT} \leq 0.5V$).

Successive connection of serial data outputs to serial data inputs make longer length serial to parallel conversions possible. Device cascading makes the TSC 9403 and TSC 9404 ideal thermal printhead or high resolution LED bar graph drivers.

Features

- High Voltage Outputs: 20V (TSC 9403), 15V (TSC 9404)
- High Output Current Sink Capability: 60 mA
- Low Standby Power: 20 mW
- High Speed Operation: 3.0 MHz
- 16 Parallel Outputs
- Cascading Possible for Longer Data Words

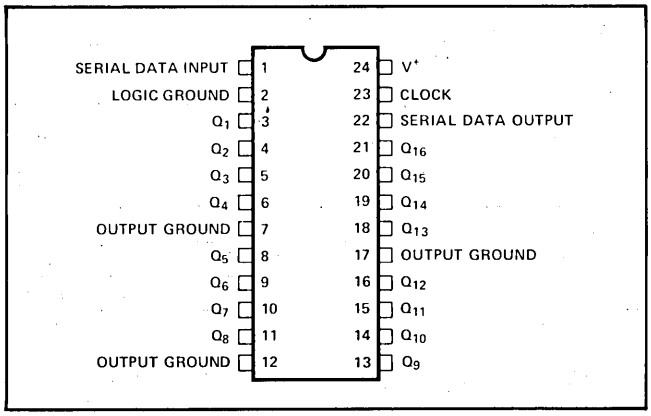
Applications

- Thermal Printhead Driver
- LED Bar Graph Driver
- High Current, Microprocessor Serial Port Expander
- Relay/Solenoid Driver
- Tungsten Lamp Driver
- SCR Gate Driver

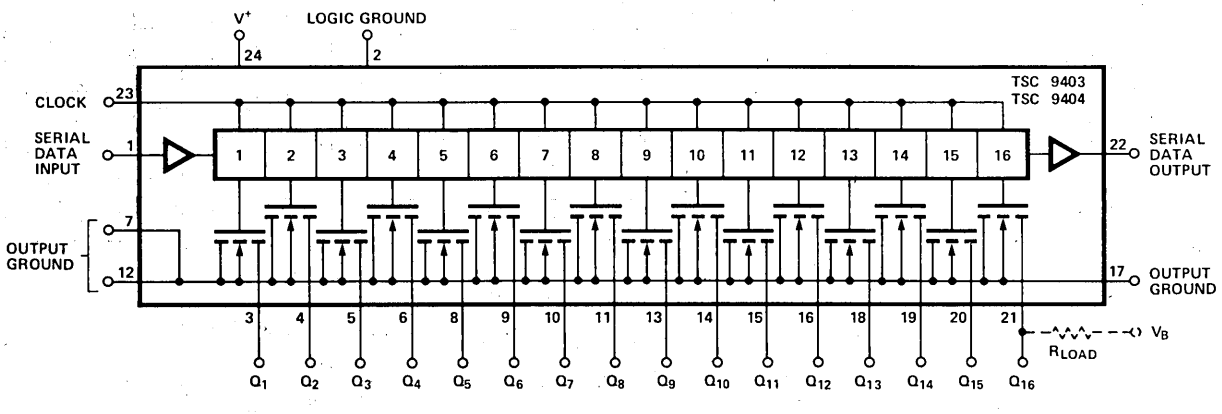
Ordering Information

Part	Package	Temperature Range	Output Voltage	Order Part #
TSC 9403	24 Pin Epoxy DIP	0° C to 70° C	20V	TSC 9403CJ
TSC 9403	24 Pin Cerdip	-25° C to 85° C	20V	TSC 9403IL
TSC 9404	24 Pin Epoxy DIP	0° C to 70° C	15V	TSC 9404CJ
TSC 9404	24 Pin Cerdip	-25° C to 85° C	15V	TSC 9404IL

Pin Configuration



Simplified Schematic



NOTE: LOGIC 1 SERIAL DATA INPUT BIT TURNS OUTPUT NMOS ON.

TELEDYNE SEMICONDUCTOR

Peripheral Drivers
from Texas Instruments

Dual, high current, peripheral drivers
Types SN75407, SN75408

Features
- Very low quiescent power ... 100 mW typical
- Very low input current ... 1 μA typical
- No output latch-up at 50 V
- Characterized for use to 500 mA
- Output clamp diodes
- TTL OR MOS compatible-diode clamped inputs
- Standard 5-V supply voltage

Applications
- Logic buffers
- Hammer drivers
- DC motor drivers
- DC relay/solenoid drivers

Logic Functions
SN75407 — NAND
SN75408 — OR

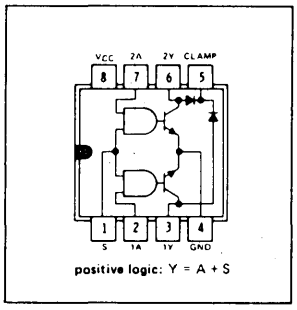
Description
The SN75407 and SN75408 series of dual peripheral drivers are designed for use in systems that require high current, high voltage, and fast switching outputs. These devices have diode-clamped inputs as well as high-current, high-voltage inductive-clamp diodes on the outputs. Use of PNP circuitry enables this series to feature very low quiescent power and minimal input current requirements.

Absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

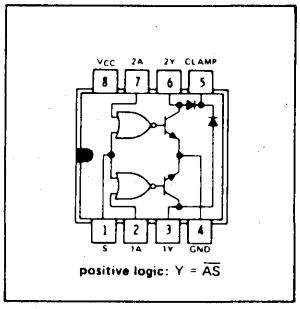
Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Output current (see Note 2)	500 mA
Output clamp diode current	500 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3)	
P (copper)	1380 mW
Operating free-air temperature	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 10 seconds:	260°C

Notes: 1. Voltage values are with respect to network ground terminal.
2. Both halves of this dual circuit may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation ratings.
3. PG package for operation above 25°C free-air temperature, derate at 11.1 mW/°C

SN75407
DUAL-IN-LINE
PACKAGE (TOP VIEW)



SN75408
DUAL-IN-LINE
PACKAGE (TOP VIEW)

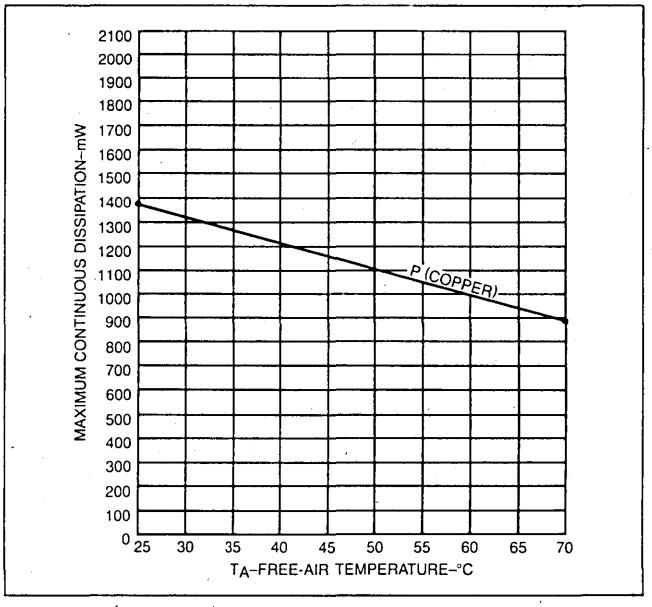


SN75407
function table
(each driver)

INPUTS		OUTPUT
A	S	Y
L	L	H
L	H	H
H	L	H
H	H	L

SN75408
function table
(each driver)

INPUTS		OUTPUT
A	S	Y
L	L	L
L	H	H
H	L	H
H	H	H



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225612 • DALLAS, TEXAS 75265

Peripheral Drivers
from Texas Instruments

Quadruple, hi-current, peripheral drivers
Types SN75436, SN75437A, SN75438

Features
- Saturating outputs with low on-resistance
- Very low standby power ... 26mW max
- High voltage outputs ... 70 V min
- High impedance MOS or TTL compatible inputs
- Standard 5 V supply voltage
- No output glitch during power up or power down
- Output clamp diodes for transient suppression
- 2W power pkg ... 60°C W $R_{\theta JA}$
  10°C W $R_{\theta JC}$

Applications
- Relay drivers
- DC and stepping motor drivers
- Solenoid drivers
- Land drivers
- Hammer drivers
- Memory drivers

Logic Functions
- All 3 devices — NAND

Description
The SN75436, SN75437A, and SN75438 quad peripheral drivers are designed for use in systems requiring high current, high voltage, and high load power. Each features four inverting open collector drivers with a common enable input which, when taken low, disables all four outputs.

Absolute maximum ratings over free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage	5.5 V
Output voltage	70 V
Output current	1.0 A
Output clamp diode current	1.0 A
Continuous total dissipation, $T_A \leq 25°C$ (free-air) Note 1	2075 mW
Operating free-air temperature	0°C to 70°C

Note 1: For operating above 25°C ambient temperature derate at 16.6 mW/°C

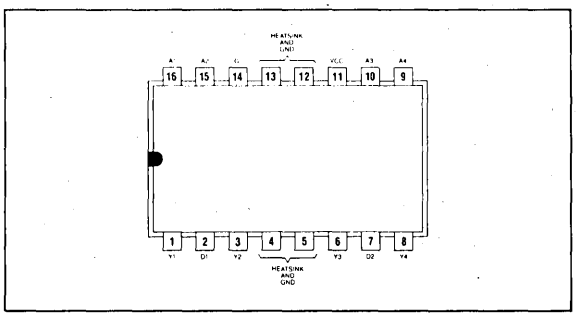
Recommended operating conditions

	MIN	NOM	MAX
Supply voltage, V_{CC}	4.75 V	5.0 V	5.25 V
Output current SN75436, SN75437 SN75438			500 mA 1.0 A
Output voltage SN75436 SN75437, SN75438			50 V 35 V

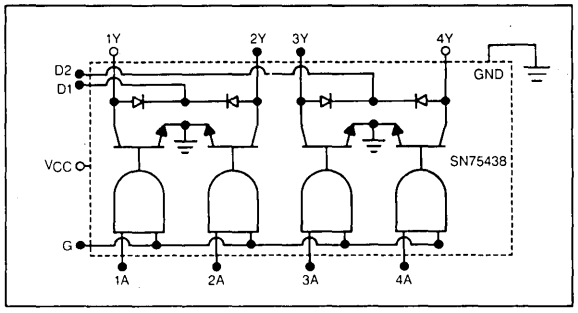
Selection guide

FEATURE	75436	75437A	75438
Output current	500 mA	500 mA	1000 mA
Max VSAT	0.5 V	0.5 V	1.0 V
Max switching volt.	50 V	35 V	35 V

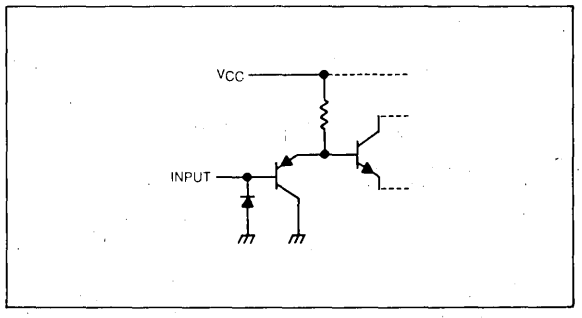
NE
DUAL-IN-LINE
PACKAGE (TOP-VIEW)



Logic diagram



Equivalent of each input



Function table (each nand driver)

INPUTS		OUTPUT
A	G	Y
L	X	H
X	L	H
H	H	L

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225612 • DALLAS, TEXAS 75265

Peripheral Drivers
from Texas Instruments

2 Amp Half-H motor driver
Types SN75603, SN75604

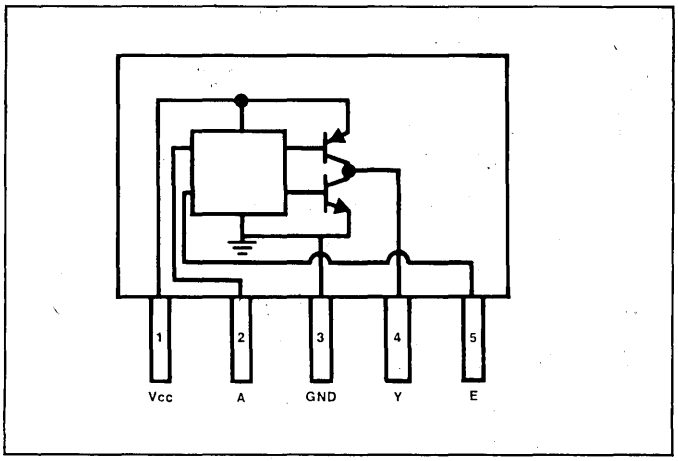
Features
- ±2 Amp Continuous Output Current
- ±5 Amp Peak Output Current
- Vcc Operating Range from 8V to 40V
- Sink-Source Interlock Protection
- Transient Suppression Diodes
- Thermal Shutdown
- High Impedance
- TTL or MOS Compatible Inputs
- 5 Lead TO220 Power Package

Description
The SN75603 and SN75604 are designed for H-drive motor applications. A full-H driver can be implemented using 1-75603 and 1-75604 without adding any additional gates or inverters, thereby achieving easy interface between a microprocessor or stepper motor controller.

The "A" input determines direction of current flow through the motor coil by activating either the sink or source output. The "E" input is an enable, which when taken low, provides a high impedance output of the driver and shuts off current to the motor. This also provides for chopper mode operation and pulse width modulation to achieve lower power dissipation and speed control.

These drivers offer desirable protection features such as thermal shutdown if the junction temperature exceeds 150°C, sink-source interlock to prevent the sink and source outputs from conducting simultaneously, and transient suppression diodes.

SN75603, 75604 KC



Truth Tables

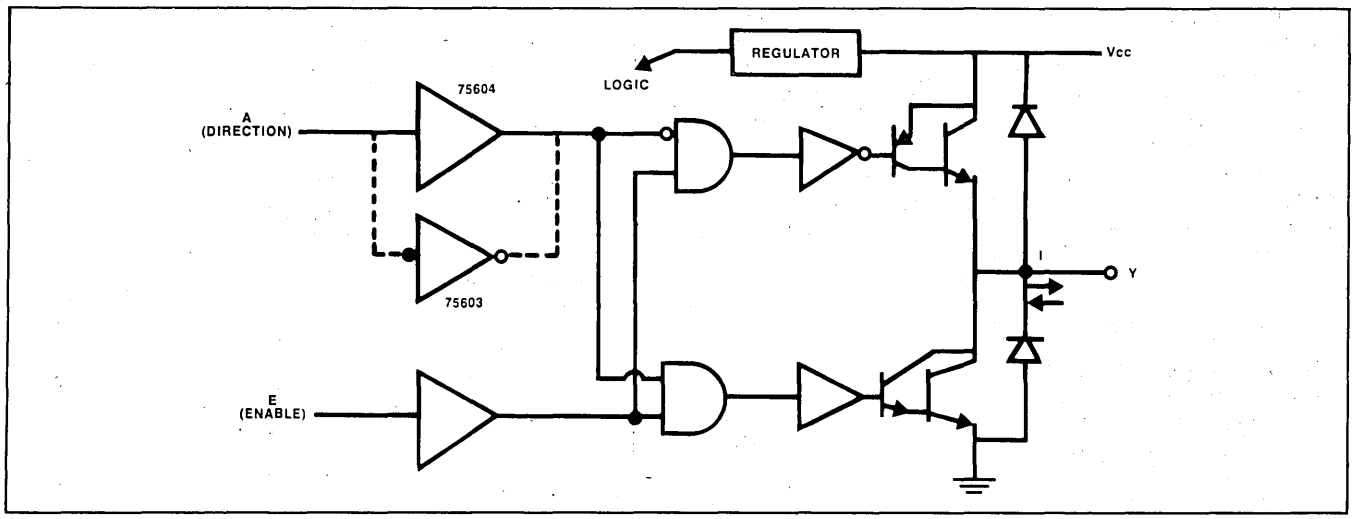
75604

A	E	Y	I
X	0	Z	off
0	1	1	→
1	1	0	←

75603

A	E	Y	I
X	0	Z	off
0	1	0	←
1	1	1	→

FUNCTION DIAGRAM



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225612 • DALLAS, TEXAS 75265

Line Circuits for EIA Industry Standards from Texas Instruments

SN75176, SN75177, SN75178 differential bus transceivers/repeaters

Features:

- Meets EIA standard RS422A
- Designed for multipoint bus transmission
- −7V to +12V bus common mode range
- Single +5V supply
- Low power requirements . . . 35 mA max.
- High impedance to bus with driver in 3-state or with power off over entire common mode range
- Driver thermal shutdown protection
- Positive and negative current limiting on driver outputs
- 60mA driver output capability
- ±200mV receiver sensitivity
- 12kΩ minimum receiver input impedance
- 50mV typical receiver hysteresis

Description

The SN75176, SN75177, and SN75178 transceivers are designed to meet EIA standard RS422 with extended positive and negative common mode range for bus applications. These transceivers are capable of transmitting and receiving data at rates up to 4M bits and over distances up to 4000 ft. If distances greater than 4000 ft. are required, the SN75177 and SN75178 repeaters can be used as a pair for bi-directional communication, or individually for one way communication.

With the SN75176 transceiver, the RE and DE inputs can be connected together to use as a direction control input, or used individually for independent control of the driver and receiver.

The SN75177 and SN75178 enable inputs are complementary such that when paired and connected together, this pin serves as a direction control for bi-directional communication.

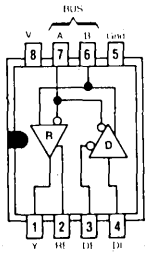
Absolute maximum ratings

Supply voltage, Vcc	7 V
Enable input voltage	5.5 V
Common mode bus voltage	+15 V/−10 V
Differential bus voltage	±25 V
Continuous total power dissipation at 25°C	830 mW

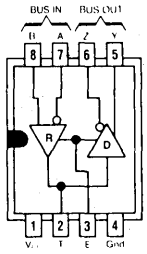
Recommended operating conditions

	MIN	MAX
Supply voltage	4.75 V	5.25 V
Common mode bus voltage	−7 V	+12 V
Driver output current		±60 mA
Receiver high-level output current		−400 μA
Receiver low-level output current		+16 mA
Operating free air temperature	0°C	+70°C

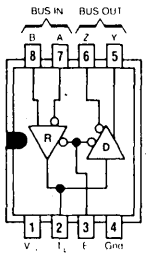
SN75176
JG OR P PACKAGE
(TOP VIEW)



SN75177
JG OR P PACKAGE
(TOP VIEW)



SN75178
JG OR P PACKAGE
(TOP VIEW)



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225612 • DALLAS, TEXAS 75265

Display Drivers
from Texas Instruments

TL4810A BIDFET
10-Bit Serial-Input Latched Driver with Active Pull-Down

Features

- High-voltage outputs 60V
- CMOS compatible inputs
- Low power CMOS logic and latches
- Active totem-pole outputs
- Wide supply voltage range
- Directly interchangeable with UCN4810A

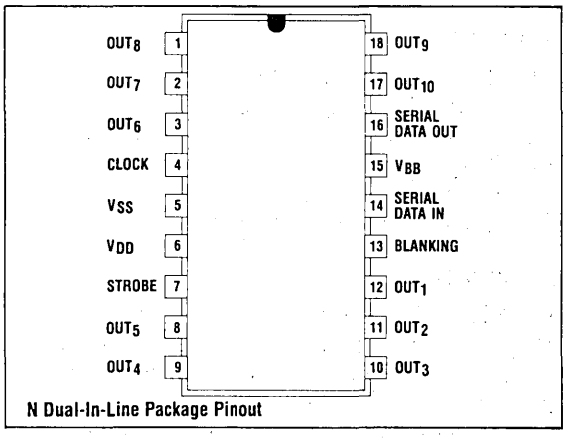
Description

The TL4810A is a monolithic BIDFET integrated circuit designed to drive a segmented, dot character, or full dot matrix vacuum fluorescent display (VFD).

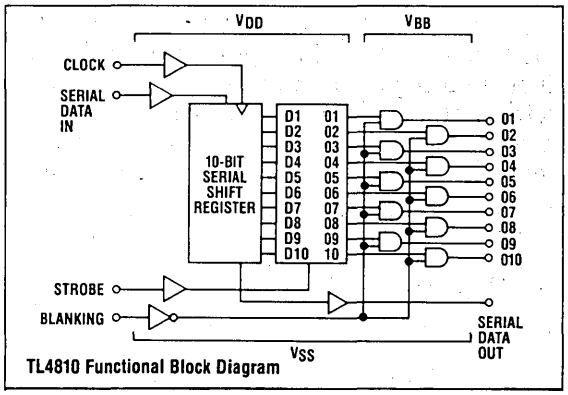
The primary feature of the TL4810A 10-bit VFD driver is its unique output structure. The TL4810A utilizes an active totem-pole output to improve the sink current capability without sacrificing the resulting power consumption as conventionally experienced in a passive pull-down structure. The totem-pole output decreases the inter-digit-blanking time required and the overall device power consumption.

Unlike most VFD drivers which are limited to an 85% duty cycle at 50°C the TL4810A will sustain a 25 mA per output load at 100% duty cycle over its entire operating temperature range of 70°C.

Designed to control 10 VFD inputs, the TL4810A contains a positive edge triggered 10-bit serial shift register with a serial data output for serial transmission and registration of the display information. A 10-bit D-type latch accepts parallel data from the serial shift register when the strobe input is high. The data stored in the latch circuitry when the strobe input is taken low remains un-altered regardless of subsequent changes in the data present in the serial shift register. The latched information is then transferred to the outputs through the gated output buffers when the blanking input is low. A logic high on the blanking input causes all outputs to go low. All outputs are capable of sourcing 40mA each at a supply voltage of 60V, providing the maximum allowable package power limitation is not exceeded. All device inputs are diode-clamped and compatible with standard MOS, CMOS and DMOS logic. The addition of a pull-up resistor to V_{DD} is required when driven by standard TTL logic.



N Dual-In-Line Package Pinout



TL4810 Functional Block Diagram

FUNCTIONAL TABLE

Function	Control Inputs*			Shift Register Contents R1 Thru R10	Latches Contents L1 Thru L10	Outputs	
	Clock	Strobe	Blanking			Serial	0-1 Thru 010
Load	⎍			Load and Shift	Determined by Strobe & R1/R10	R10	Determined By Blanking & L1/L10
	⎏			No Change			
Latch	X	High		As Determined Above	L1 = R1; L2 = R2; ETC	R10	Determined By Blanking & L1/L10
	X	Low			Stored Data		
Blanking			High	As Determined Above	As Determined Above	R10	All Low
			Low				10 = L1; 02 = L2; ETC

*All control inputs are independent of each other.

TEXAS INSTRUMENTS
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Display Drivers
from Texas Instruments

SN75512A
12-Bit Serial-Input Display Driver with Latches

Features

- Each device drives 12 lines
- 60V output voltage swing capability
- 25mA output source current capability
- High-speed serially-shifted data input
- TTL compatible inputs
- Latches on all driver outputs.

Description

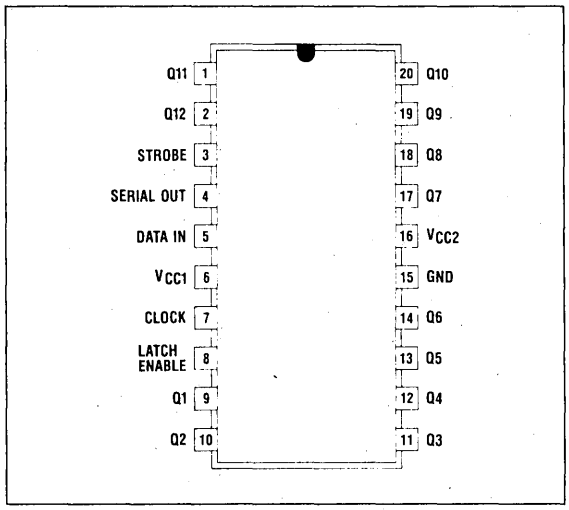
The SN75512A is a monolithic BIDFET integrated circuit (bipolar, double diffused, n-channel MOS and p-channel MOS transistors on same chip) designed to drive a dot matrix or segmented vacuum fluorescent display.

All device inputs are diode-clamped p-n-p inputs and will assume a high logic level when open-circuited. The nominal input threshold is 1.5 V. Outputs are totem-pole structures formed by n-p-n emitter follower and double-diffused MOS (DMOS) transistors.

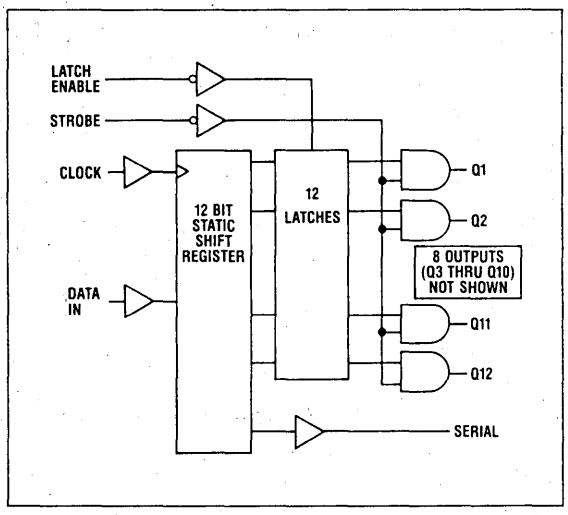
Input data is stored in the 12-bit serial shift register on the positive transition of the clock input. Parallel data is presented to the output buffers through a 12-bit-type latch. Data at the respective output of the serial shift register is transferred through the 12-bit latch while the latch input is high. Data present at the latches, inputs during the negative transition of the latch is stored regardless of subsequent changes providing the latch input remains low. The active low strobe input enables all output gates.

Each output is capable of sourcing 25mA at a supply voltage of 60V providing the maximum package power dissipation is not exceeded. Based on the maximum allowable voltage drop across the output at 25mA source current, the total package capabilities are as shown. (Table). All inputs of the SN75512A are TTL compatible. A serial data out is also available for cascading additional drivers.

The SN75512A is characterized for operation from 0°C to 70°C.



N Dual-In-Line Package Pinout



SN75512A Functional Block Diagram

SN75512A OPERATIONAL DUTY CYCLE (%)					
NUMBER OF OUTPUTS ON I_O = 25mA	MAX RECOMMENDED DUTY CYCLE AT AMBIENT TEMPERATURE OF 25°C	40°C	50°C	60°C	70°C
12	77	68	62	55	48
11	84	75	67	60	52
10	92	82	74	66	58
9	100	91	82	73	61
8	|	100	93	83	73
7	|	|	100	94	82
6	|	|	|	100	96
5	|	|	|	|	100
1	100	100	100	100	100

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225612 • DALLAS, TEXAS 75265

SN75513A
12-Bit Serial-Input Display Driver with Reset

Features

- Each device drives 12 lines
- 60V output voltage swing capability
- 25mA output source current capability
- High-speed serially-shifted data input
- TTL compatible inputs
- Reset input

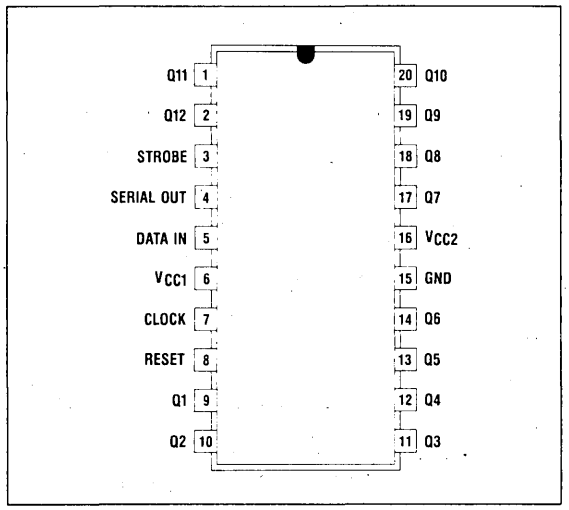
Description

The SN75513A is a monolithic BIDFET integrated circuit (bipolar, double-diffused, n-channel MOS, and P-channel MOS transistors on the same chip), designed to drive a dot matrix or segmented vacuum fluorescent display.

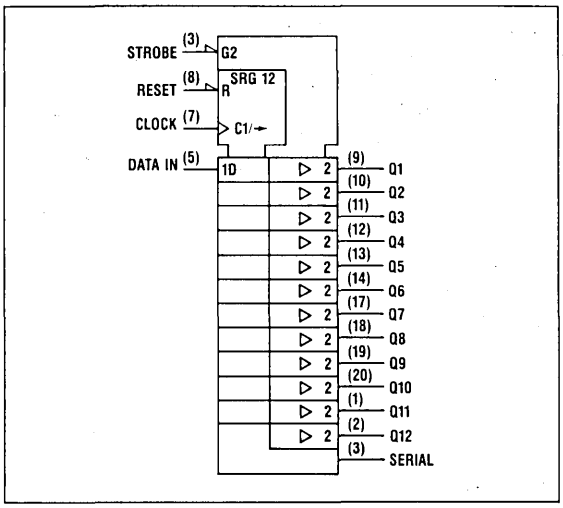
All device inputs are diode-clamped p-n-p inputs and will assume a high logic level when open-circuited. The nominal input threshold is 1.5V. Outputs are totem-pole structures formed by n-p-n emitter follower and diffused MOS (DMOS) transistors.

Input data is shifted into a 12-bit serial shift register on the positive transition of the clock. Data appearing at the corresponding outputs of the shift register is presented directly to the output gates and is reflected at the output, when the strobe input is low. Data in the shift register can be cleared with the reset input. A logic 0 on the reset input clears the shift register contents to a logic 0. All outputs are capable of supplying 25mA of source current at a supply voltage of 60V providing the absolute maximum package power limitation is not exceeded. Table I reflects the derating resulting from this consideration. All inputs are TTL compatible and assume a logic high if left open. A serial data output allows cascading of several devices without additional circuitry.

The SN75513A is characterized for operation from 0°C to 70°C.



N Dual-In-Line Package Pinout



SN75513A Functional Block Diagram

SN75513A OPERATIONAL DUTY CYCLE (%)					
NUMBER OF OUTPUTS ON I_O = 25mA	MAX RECOMMENDED DUTY CYCLE AT AMBIENT TEMPERATURE OF				
	25°C	40°C	50°C	60°C	70°C
12	77	68	62	55	48
11	84	75	67	60	52
10	92	82	74	66	58
9	100	91	82	73	61
8	|	100	93	83	73
7	|	|	100	94	82
6	|	|	|	100	96
5	|	|	|	|	100
1	100	100	100	100	100

TEXAS INSTRUMENTS
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Display Drivers
from Texas Instruments

Vacuum fluorescent display driver Type SN75518

Features

- Each Device Drives 32 Lines
- 60V Output Voltage Swing Capability
- 25 mA Output Source Current Capability
- High-Speed Serially-Shifted Data Input
- Totem Pole Outputs
- Latches on All Driver Outputs

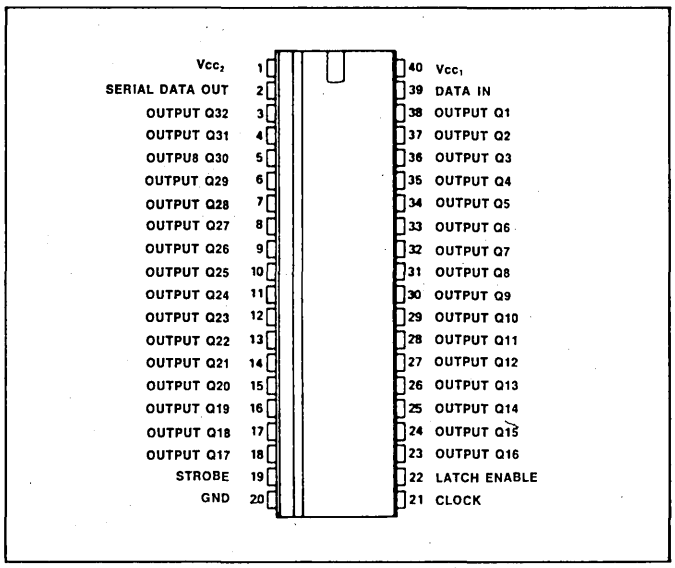
Description

The SN75518 is a monolithic BIDFET integrated circuit (bipolar, double-diffused, n-channel MOS and p-channel MOS transistors on same chipt) designed to drive a dot matrix or segmented vacuum fluorescent display.

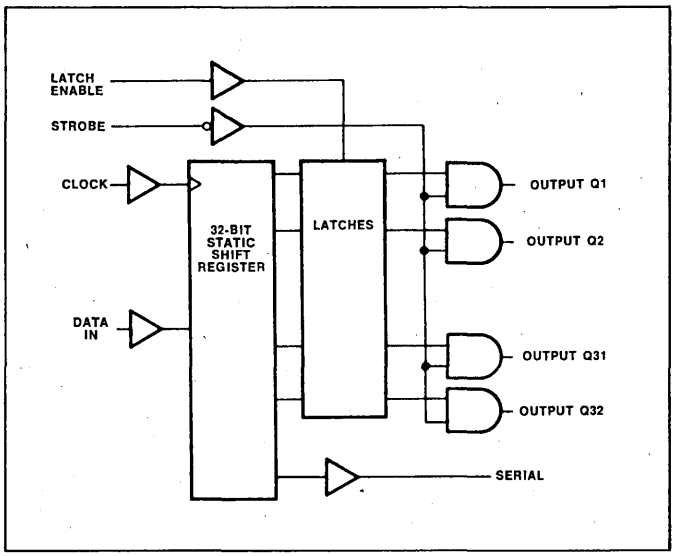
The device consists of a 32-bit shift register, 32 latches and 32 output AND gates. Serial data is entered into the shift register on the low-to-high transition of the clock. When high, the latch enable input transfers the shift register contents to the outputs of the 32 latches. The active-low strobe input enables all Q outputs. Serial data output from the shift register may be used to cascade shift registers. This output is not affected by the latch enable or strobe inputs.

The SN75518 is characterized for operation from 0°C to 70°C.

N DUAL-IN-LINE PACKAGE (Top view)



FUNCTIONAL BLOCK DIAGRAM



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Gas discharge display driver Type SN75581

Features

- Each Device Drives 7 Lines
- 150V Output Voltage Swing Capability
- TTL Compatible Inputs
- Latches on All Driver Outputs
- High Speed Serially-Shifted Data Input
- Output Enable/Disable Function
- Serial Data Output for Cascade Operation
- Shift Register Has Synchronous Clear Function

Description

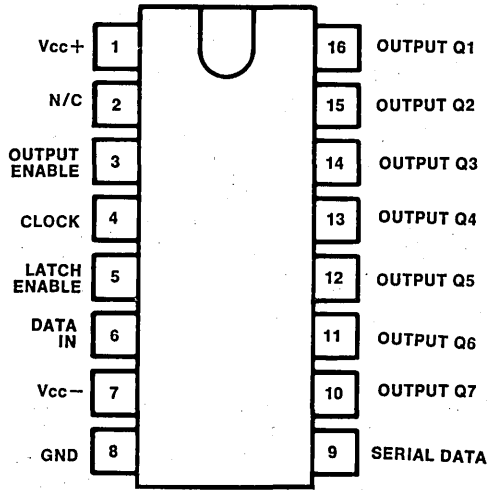
The SN75581 is a monolithic BIDFET integrated circuit designed to drive a dot matrix or segmented display. The output characteristics of this driver make it compatible to several display types including VF and DC Plasma displays.

All device inputs are diode clamped PNP inputs and will assume a high logic level when open circuited. The nominal input threshold is 1.5 volts. Outputs are open source DMOS transistors for excellent high voltage characteristics and reliability.

The device consists of a 7-bit shift register, 7 latches and 7 output gates. Serial data is entered into the shift register on the low-to-high transition of the clock. When high, the latch enable transfers the shift register contents to the latch outputs. When latch enable is pulled low from a high state, the shift register is cleared. The output enable input enables all outputs. Serial data output is not affected by the output enable function.

The SN 75581 is characterized for operation over the industrial temperature range of 0°C to 70°C.

N, J DUAL-IN-LINE PACKAGE (Top view)



TEXAS INSTRUMENTS
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Display Drivers
from Texas Instruments

High-voltage 7-segment latch/ decoder/cathode driver Type SN75584

Features

- Output Current Adjustable From 0.1 mA to 4 mA
- DMOS Outputs for High Breakdown Voltage
  Segment Outputs — 100V Min
  Decimal Point Output — 100V Min
- Input Data Latches
- Blanking Input Provided
- P-N-P Inputs for Minimal Input Loading
- Low Power Requirements
- Thermal Protection Circuitry
- Supply Voltage Variable Over Wide Range — 4.75V to 15V
- Decimal Point Output Provided
- Suitable for Multiplex Operation

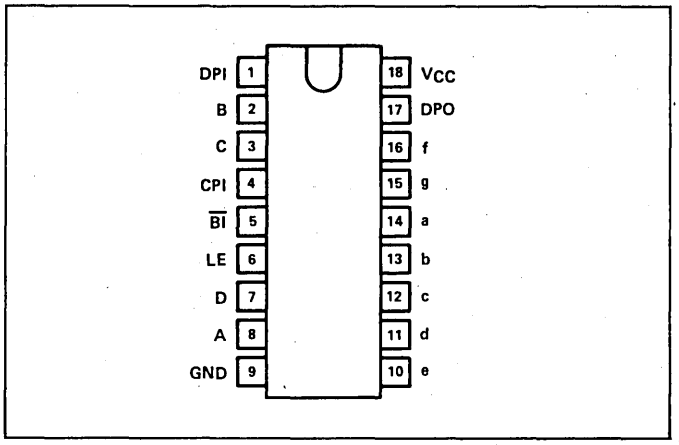
Description

The SN75584A is designed to decode four lines of BCD data and drive a gas-filled seven-segment display tube such as Beckman and Panaplex II† displays. Latches are provided to store the BCD and decimal point data while the enable input is at a low-level voltage.

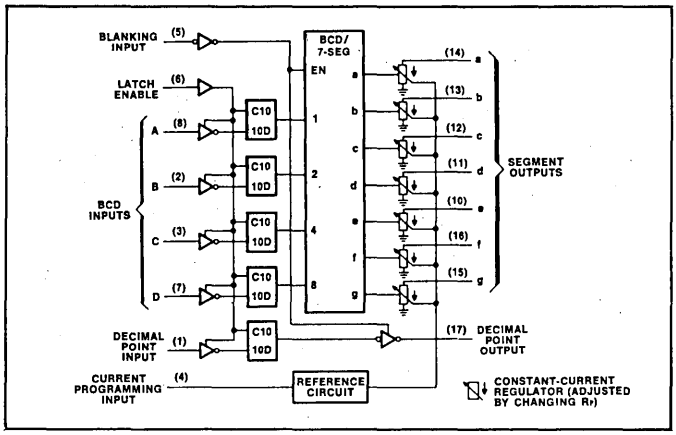
The design employs a read-only memory to provide output decoding for the BCD digits 0 to 9. For input data greater than BCD 9, the segment outputs are blanked. Each sink output is regulated to ensure a constant brightness of the display even with a fluctuating supply voltage. The on-state output current is essentially constant over the output voltage range of 4 volts to 100 volts. Each current sink is ratioed to the "b" segment output current as required for even illumination of all segments.

† Trademark or Burroughs Corporation.

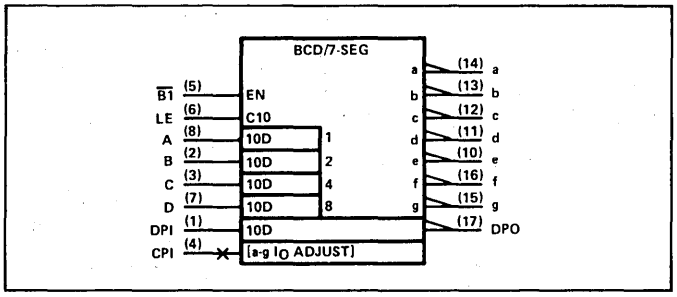
N DUAL-IN-LINE PACKAGE (Top view)



FUNCTIONAL BLOCK DIAGRAM



LOGIC SYMBOL†



† This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and current discussions in IEC and IEEE.

TEXAS INSTRUMENTS
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Data Acquisition Circuits
from Texas Instruments

8-Bit analog-to-digital converter with 15-analog and 12-digital input channels Type TL530N

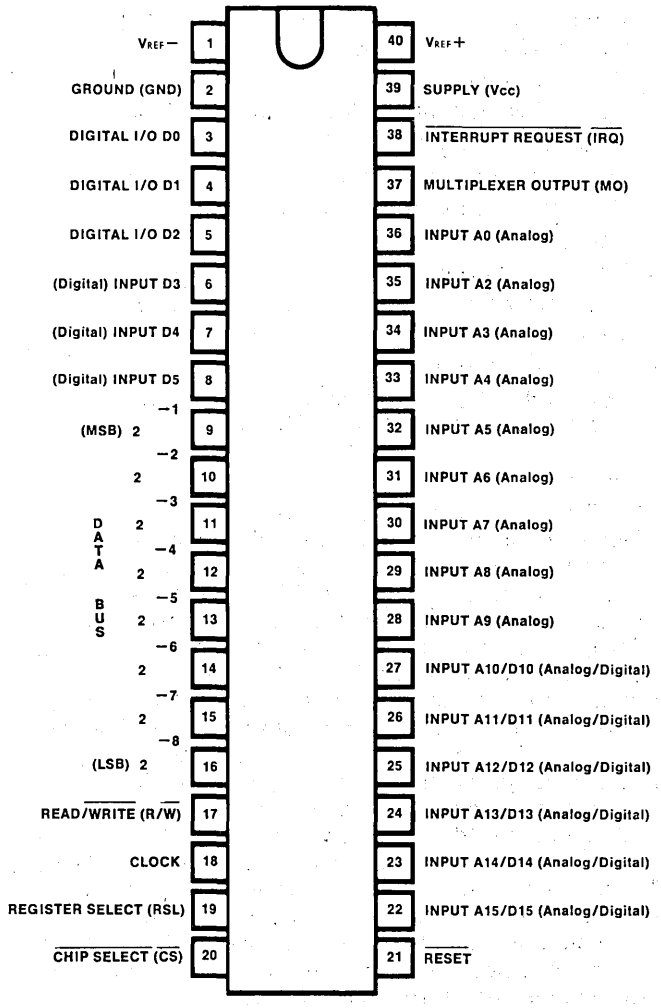
Features

- 8 Bit Resolution
- Total Unadjusted Error: ±½ LSB Max for TL530 (±1 LSB Max for TL531)
- Up to 15 Analog Inputs
- Up to 12 Digital Inputs, Including 3 I/O Pins
- Three-state, Bidirectional Data Bus
- Access & Conversion in 300 μSec @ 85°C
- 16-Channel On-Chip Analog Multiplexer
- Ratiometric Conversion
- Single 5-Volt Supply
- Low Power Consumption of 15 mW, Typical
- Three 16-Bit On-Chip Data Registers
- Polled or Interrupt Driven
- Designed to be a Pin-Compatible, Functional Replacement for MC144444
- Pin-For-Pin replacement for 74C924

Description

The TL530 is a monolithic CMOS device with 16-channel analog multiplexer, 8-bit ratiometric analog-to-digital (A/D) converter, a register to store digital data from 9 inputs and 3 input/outputs, bus-compatible 8-pin input/output data ports and microprocessor-compatible control logic. Three on-chip data registers store control, conversion-results, and digital data that can be accessed via the IC's data port in two 8-bit bytes (most-significant-byte first). The A/D conversion is accomplished using successive-approximation technique and employing a high-impedance chopper-stabilized comparator, a 256R end-compensated voltage divider with analog switch tree, and a successive-approximation register (SAR). These methods eliminate the possibility of missing codes, nonmonotonicity, and a need for zero or full-scale adjustment. Positive and negative reference inputs make possible ratiometric conversion and reference isolation from supply noise.

N DUAL-IN-LINE PACKAGE (Top view)



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225612 • DALLAS, TEXAS 75265

Data Acquisition Circuits from Texas Instruments

8-Bit analog-to-digital converter with 15-analog and 12-digital input channels Type TL531N

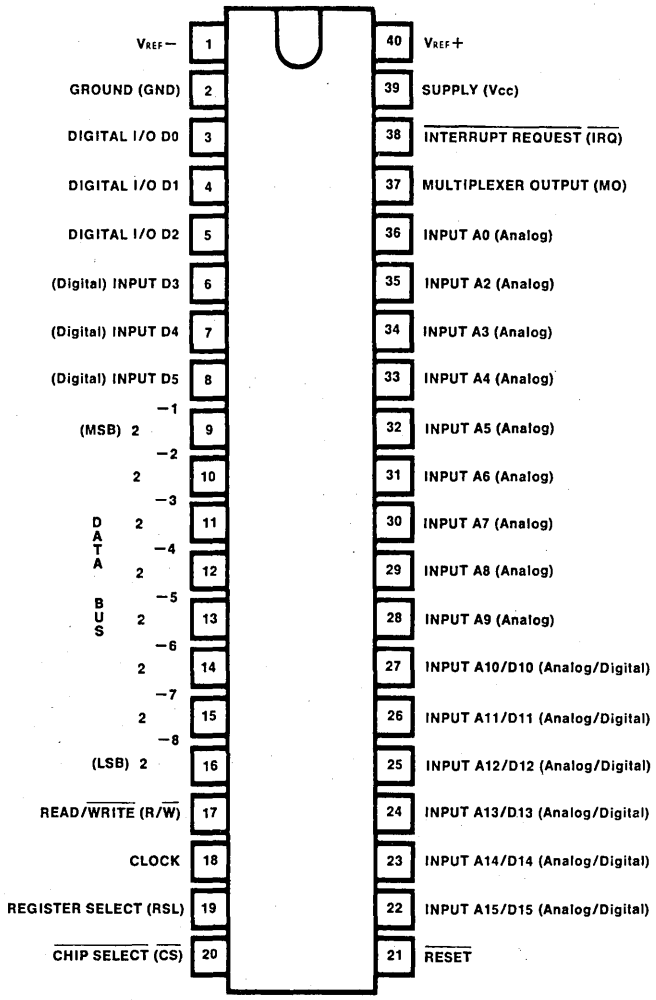
Features

- 8 Bit Resolution
- Total Unadjusted Error: ±1 LSB Max for TL531 (±½ LSB Max for TL530)
- Up to 15 Analog Inputs
- Up to 12 Digital Inputs, Including 3 I/O Pins
- Three-state, Bidirectional Data Bus
- Access & Conversion in 300 μSec @ 85°C
- 16-Channel On-Chip Analog Multiplexer
- Ratiometric Conversion
- Single 5-Volt Supply
- Low Power Consumption of 15 mW, Typical
- Three 16-Bit On-Chip Data Registers
- Polled or Interrupt Driven
- Designed to be a Pin-Compatible Functional Replacement for 74C924 & MC144444

Description

The TL531 is a monolithic CMOS device with 16-channel analog multiplexer, 8-bit ratiometric analog-to-digital (A/D) converter, a register to store digital data from 9 inputs and 3 input/outputs, bus-compatible 8-pin input/output data ports and microprocessor-compatible control logic. Three on-chip data registers store control, conversion-results, and digital data that can be accessed via the IC's data port in two 8-bit bytes (most-significant-byte first). The A/D conversion is accomplished using successive-approximation technique and employing a high-impedance chopper-stabilized comparator, a 256R end-compensated voltage divider with analog switch tree, and a successive-approximation register (SAR). These methods eliminate the possibility of missing codes, nonmonotonicity, and a need for zero or full-scale adjustment. Positive and negative reference inputs make possible ratiometric conversion and reference isolation from supply noise.

N DUAL-IN-LINE PACKAGE (Top view)



TEXAS INSTRUMENTS
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8-Bit analog-to-digital converter with 5 analog and 6 multipurpose inputs Type TL532N

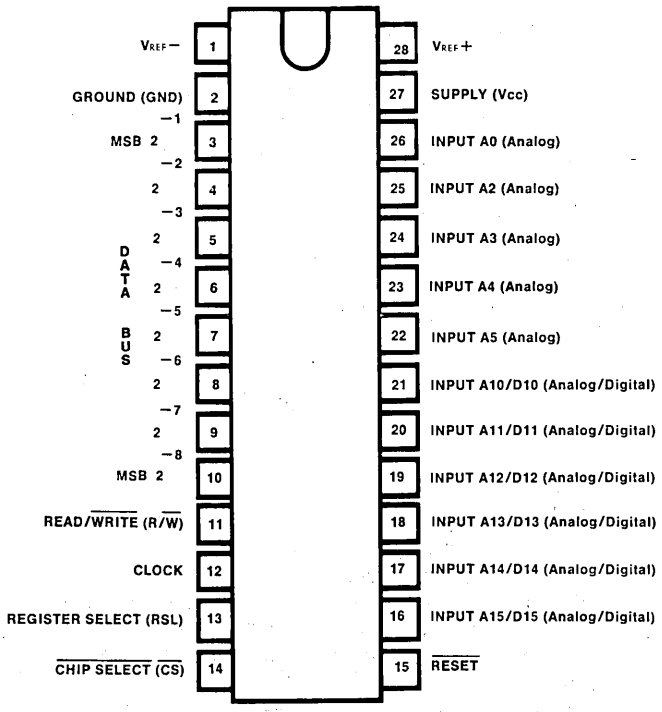
Features

- 8 Bit Resolution
- Total Unadjusted Error: ±½ LSB Max for TL532 (±1 LSB Max for TL533)
- 5 Analog Inputs
- 6 Multipurpose Analog or Digital Inputs
- Three-state, Bidirectional Data Bus
- Access & Conversion in 300 μSec @ 85°C
- 12-Channel On-Chip Analog Multiplexer
- Ratiometric Conversion
- Single 5-Volt Supply
- Low Power Consumption of 15 mW, Typical
- Three 16-Bit Data Registers
- Software Compatible with Larger 21-Input Version, TL530
- Pin-for-Pin Replacement for 74C934

Description

The TL532 is a monolithic CMOS device with 12-channel analog multiplexer, 8-Bit ratiometric analog-to-digital (A/D) converter, a register to store digital data from 6 multipurpose inputs, a TTL-Compatible 8-pin input/output data port, and microprocessor-compatible control logic. Three on-chip data registers store control, conversion-results, and digital data that can be accessed via the IC's data port in two 8-bit bytes (most-significant-byte first). The A/D conversion is accomplished using successive-approximation technique and employing a high-impedance chopper-stabilized comparator, a 256R end-compensated voltage divider with analog switch tree, and a successive-approxImation register (SAR). These methods eliminate the possibility of missing codes, nonmonotonicity, and a need for zero or full-scale adjustment. Positive and negative reference inputs make possible ratiometric conversion and reference isolation from supply noise.

N DUAL-IN-LINE PACKAGE (Top view)



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225612 • DALLAS, TEXAS 75265

Data Acquisition Circuits from Texas Instruments

8-Bit analog-to-digital converter with 5 analog and 6 multipurpose inputs Type TL533N

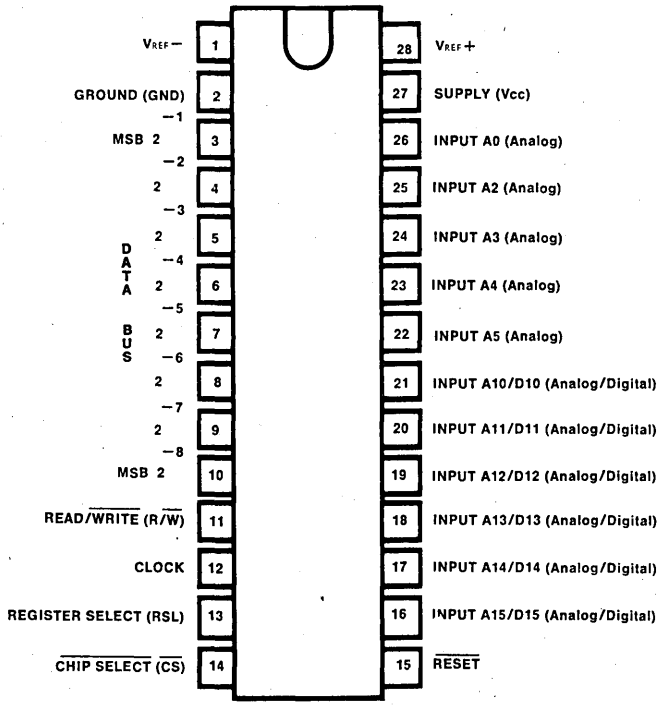
Features

- 8 Bit Resolution
- Total Unadjusted Error: ±1 LSB Max for TL533 (±½ LSB Max for TL532)
- 5 Analog Inputs
- 6 Multipurpose Analog or Digital Inputs
- Three-state, Bidirectional Data Bus
- Access & Conversion in 300 μSec @ 85°C
- 12-Channel On-Chip Analog Multiplexer
- Ratiometric Conversion
- Single 5-Volt Supply
- Low Power Consumption of 15 mW, Typical
- Three 16-Bit Data Registers
- Software Compatible with Larger 21-Input Versions, TL531
- TL533 is a Pin-Compatible, Functional Replacement for 74C934

Description

The TL533 is a monolithic CMOS device with 12-channel analog multiplexer, 8-Bit ratiometric analog-to-digital (A/D) converter, a register to store digital data from 6 multipurpose inputs, a TTL-Compatible 8-pin input/output data port, and microprocessor-compatible control logic. Three on-chip data registers store control, conversion-results, and digital data that can be accessed via the IC's data port in two 8-bit bytes (most-significant-byte first). The A/D conversion is accomplished using successive-approximation technique and employing a high-impedance chopper-stabilized comparator, a 256R end-compensated voltage divider with analog switch tree, and a successive-approximation register (SAR). These methods eliminate the possibility of missing codes, nonmonotonicity, and a need for zero or full-scale adjustment. Positive and negative reference inputs make possible ratiometric conversion and reference isolation from supply noise.

N DUAL-IN-LINE PACKAGE (Top view)



TEXAS INSTRUMENTS
INCORPORATED
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WD2501/2511 Packet Network Interface (LAP/LAPB)

FEATURES

- Packet switching controller, compatible with CCITT recommendation X.25, level 2, LAP (2501) or LAPB (2511)
- Programmable primary timer (T1) and retransmission counter (N2)
- Programmable A-field which provides a wider range of applications than defined by X.25. These include: DTE-to-DTE connection, multipoint and loop-back testing
- Direct memory access (DMA) transfer: two channels; one for transmit and one for receive. Send/receive data accessed by indirect addressing method. Sixteen output address lines.
- Zero bit insert and delete
- Automatic appending and testing of FCS field
- Computer bus interface structure: 8 bit bi-directional data bus. CS, WE, RE and four input address lines
- DC to 1.1 MBPS data rate
- TTL compatible
- 48 pin dual in-line packages
- Higher bit rates available by special order

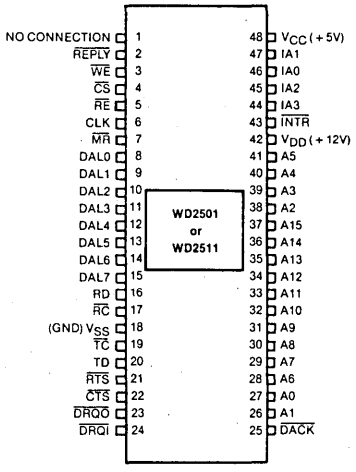
APPLICATIONS

X.25 PACKET SWITCHING CONTROLLER
PART OF DTE OR DCE
PRIVATE PACKET NETWORKS
LINK LEVEL CONTROLLER

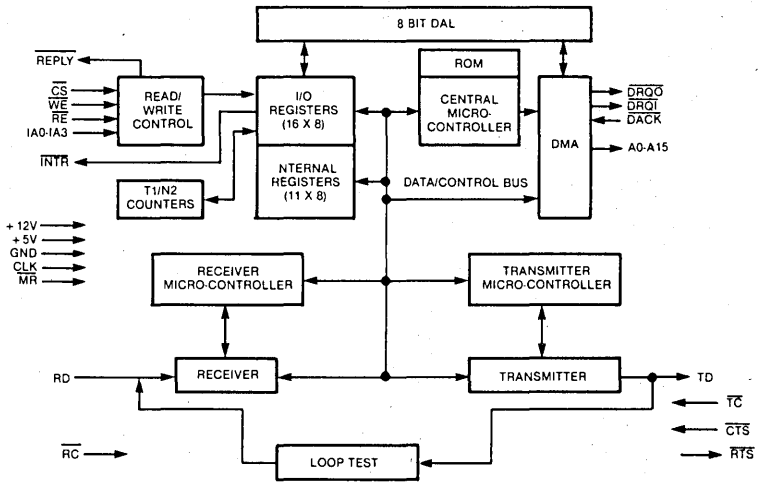
GENERAL DESCRIPTION

The WD2501/2511 is a MOS/LSI device which handles bit-oriented, full-duplex serial data communications with DMA, which conforms to CCITT X.25 with programmable enhancements.

The device is fabricated in N-Channel silicon gate MOS technology and is TTL compatible on all inputs and outputs.



PIN DESIGNATION



BLOCK DIAGRAM

WESTERN DIGITAL
CORPORATION

WD2520 CCITT #7 Data Link Controller

FEATURES

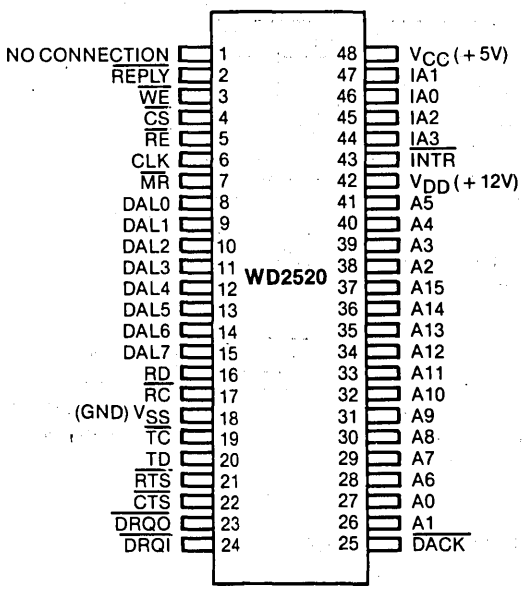
- Performs the controls of the Message Transfer part of CCITT #7.
- Dual Channel DMA for full-duplex operation.
- Unique memory access method for buffer management.
- All formatting of bit-oriented control included: zero bit insertion and deletion. Automatic appending and testing of flags and FCS Fields.
- Automatic control of sequence numbers FSN and BSN, and of control bits FIB and BIB.
- Optional selection of either "Basic" error correction method or the preventive cyclic retransmission error correction method.
- Computer bus interface structure: 8-bit bi-directional data bus. 16-bit address bus for DMA. 4-bit input address bus (may be tied to lower 4 bits of 16 bit address). CS, RE, WE.
- TTL compatible.
- Speeds to 1MBit/Sec Transmit-Receive Rate.

GENERAL DESCRIPTION

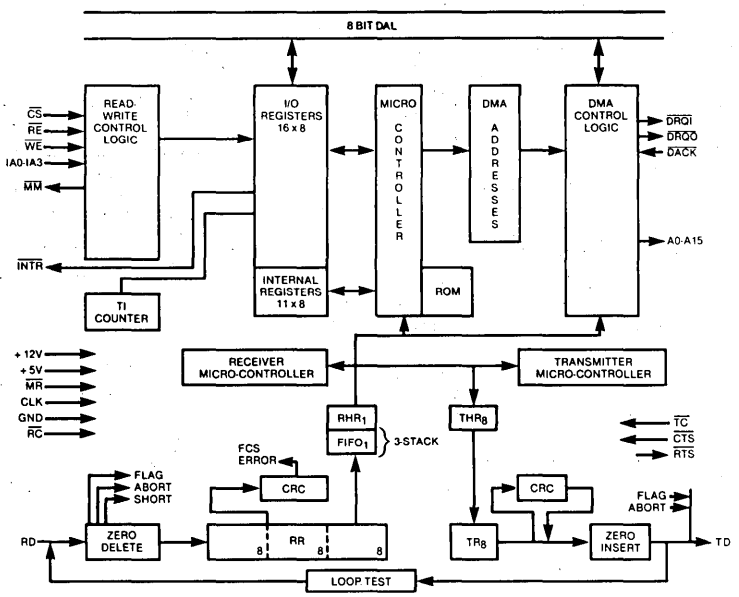
The WD2520 is a MOS LSI device which is compatible with the CCITT Recommendation #7 (Signalling System Number 7). The overall objective of Signalling System #7 is to provide one internationally standardized general purpose common channel signalling system for information transfer within telecommunications networks. (i.e. signalling from one central office switch to another).

The WD2520 performs most of the controls of the Message Transfer Part of CCITT#7. The device includes a unique buffer management scheme with dual channel DMA.

The WD2520 is pin-for-pin compatible with the WD2501/2511 popular Level 2 X.25 controller.



PIN DESIGNATION



BLOCK DIAGRAM

UC1671 ASTRO

FEATURES

SYNCHRONOUS AND ASYNCHRONOUS
- Full Duplex Operations

SYNCHRONOUS MODE
- Selectable 5-8 Bit Characters
- Two Successive SYN Characters Sets Synchronization
- Programmable SYN and DLE Character Stripping
- Programmable SYN and DLE-SYN Fill

ASYNCHRONOUS MODE
- Selectable 5-8 Bit Characters
- Line Break Detection and Generation
- 1-, 1½-, or 2-Stop Bit Selection
- False Start Bit Detection Automatic Serial Echo Mode

SYSTEM COMPATIBILITY
- Double Buffering of Data
- 8-Bit Bi-Directional Bus For Data, Status, and Control Words
- All Inputs and Outputs TTL Compatible
- Up to 32 ASTROS Can Be Addressed On Bus
- On-Line Diagnostic Capability

TRANSMISSION ERROR DETECTION-PARITY
- Overrun and Framing

BAUD RATE — DC TO 1M BIT/SEC

8 SELECTABLE CLOCK RATES
- Accepts 1X Clock and Up to 4 Different 32X Baud Rate Clock Inputs
- Up to 47% Distortion Allowance with 32X Clock

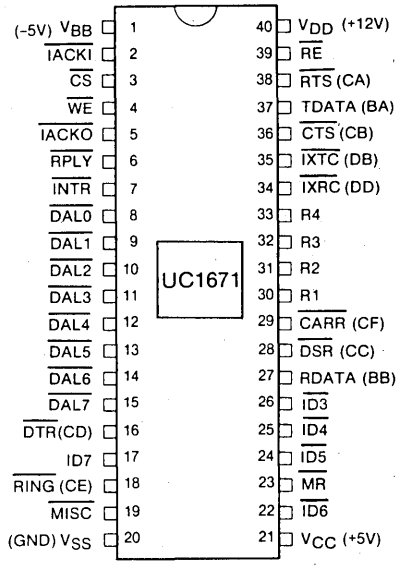
APPLICATIONS

SYNCHRONOUS COMMUNICATIONS
ASYNCHRONOUS COMMUNICATIONS
SERIAL/PARALLEL COMMUNICATIONS

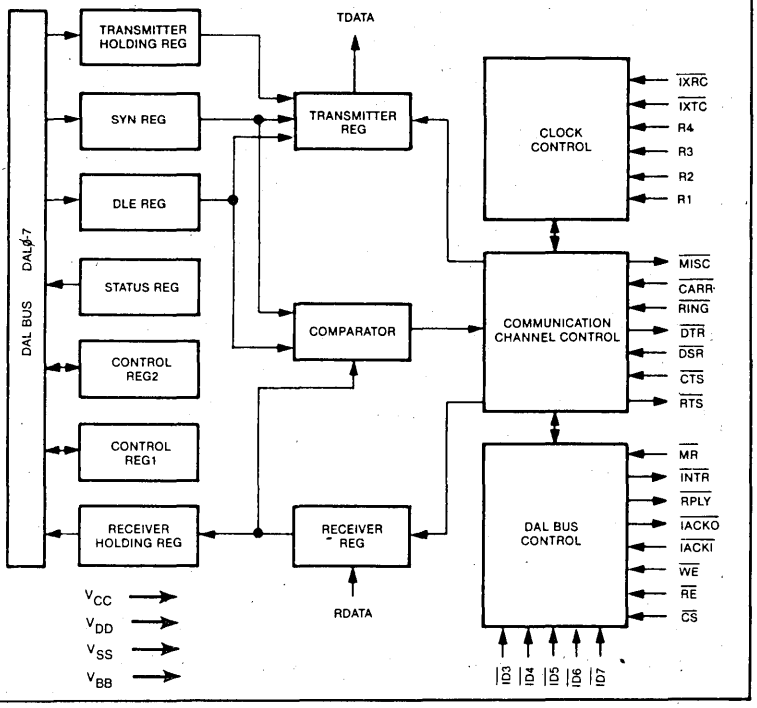
GENERAL DESCRIPTION

The UC1671 (ASTRO) is a MOS/LSI device which performs the functions of interfacing a serial data communication channel to a parallel digital system. The device is capable of full duplex communications (receiving and transmitting) with synchronous or asynchronous systems. The ASTRO is designed to operate on a multiplexed bus with other bus-oriented devices. Its operation is programmed by a processor or controller via the bus and all parallel data transfers with these machines are accomplished over the bus lines.

The ASTRO is fabricated in n-channel silicon gate MOS technology and is TTL compatible on all inputs and outputs.



PIN DESIGNATION



WESTERN DIGITAL
CORPORATION

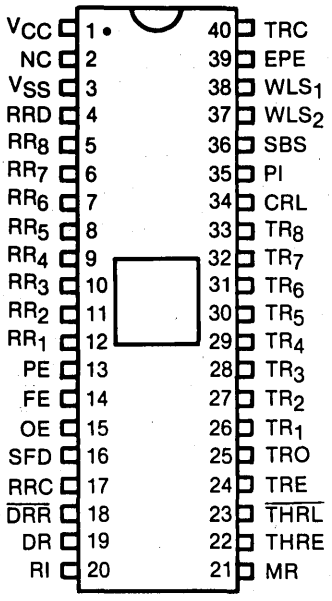
TR1863/TR1865
Universal Asynchronous Receiver/Transmitter (UART)

FEATURES

- SINGLE POWER SUPPLY — +5VDC
- D.C. TO 1 MHZ (64 KB) (STANDARD PART) TR1863/5
- FULL DUPLEX OR HALF DUPLEX OPERATION
- AUTOMATIC INTERNAL SYNCHRONIZATION OF DATA AND CLOCK
- AUTOMATIC START BIT GENERATION
- EXTERNALLY SELECTABLE
  Word Length
  Baud Rate
  Even/Odd Parity (Receiver/Verification — Transmitter/Generation)
  Parity Inhibit
  One, One and One-Half, or Two Stop Bit Generation (1½ at 5 Bit Level)
- AUTOMATIC DATA RECEIVED/TRANSMITTED STATUS GENERATION
  Transmission Complete
  Buffer Register Transfer Complete
  Received Data Available
  Parity Error
  Framing Error
  Overrun Error
- BUFFERED RECEIVER AND TRANSMITTER REGISTERS
- THREE-STATE OUTPUTS
  Receiver Register Outputs
  Status Flags
- TTL COMPATIBLE
- TR1865 HAS PULL-UP RESISTORS ON ALL INPUTS

APPLICATIONS

PERIPHERALS
TERMINALS
MINI COMPUTERS
FACSIMILE TRANSMISSION
MODEMS
CONCENTRATORS
ASYNCHRONOUS DATA MULTIPLEXERS
CARD AND TAPE READERS
PRINTERS
DATA SETS
CONTROLLERS
KEYBOARD ENCODERS
REMOTE DATA ACQUISITION SYSTEMS
ASYNCHRONOUS DATA CASSETTES



PIN DESIGNATION

BLOCK DIAGRAM

WD8250 Asynchronous Communications Element

FEATURES

- Designed to be Easily Interfaced to Most Popular Microprocessors (Z-80, 8080A, 6800, etc.)
- Full Double Buffering
- Independently Controlled Transmit, Receive, Line Status, and Data Set Interrupts
- Programmable Baud Rate Generator Allows Division of Any Input Clock by 1 to (2^{16} - 1) and Generates the Internal 16x Clock
- Independent Receiver Clock Input
- Fully Programmable Serial-Interface Characteristics
  - —5-, 6-, 7-, or 8-Bit Characters
  - —Even, Odd, or No-Parity Bit Generation and Detection
  - —1-, 1½-, or 2-Stop Bit Generation
  - —Baud Rate Generation (DC to 56K Baud)
- False Start Bit Detector
- Complete Status Reporting Capabilities
- THREE-STATE TTL Drive Capabilities for Bi-directional Data Bus and Control Bus
- Line Break Generation and Detection
- Internal Diagnostic Capabilities
  - —Loopback Controls for Communications Link Fault Isolation
  - —Break, Parity, Overrun, Framing Error Simulation
- Full Prioritized Interrupt System Controls
- Single +5-Volt Power Supply

GENERAL DESCRIPTION

The WD8250 is a programmable Asynchronous Communication Element (ACE) in a 40-pin package. The device is fabricated in N/MOS silicon gate technology.

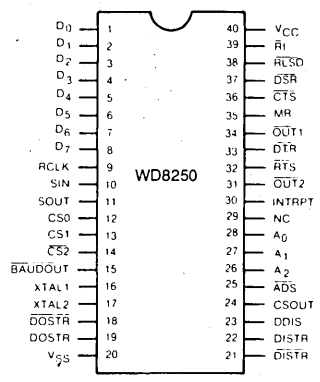
The ACE is a software-oriented device using a three-state 8-bit bi-directional data bus.

The ACE is used to convert parallel data to a serial format on the transmit side, and convert serial data to parallel on the receiver side. The serial format, in order of transmission and reception, is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, one and one half (five bit format only) or two stop bits. The maximum recommended data rate is 56K baud.

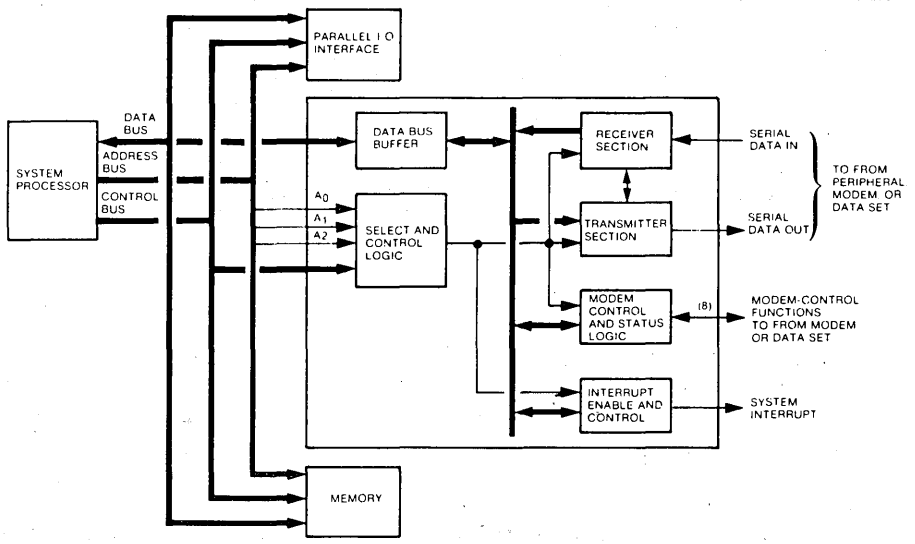
Internal registers enable the user to program various types of interrupts, modem controls, and character formats. The user can read the status of the ACE at any time monitoring word conditions, interrupts and modem status.

An additional feature of the ACE is a programmable baud rate generator that is capable of dividing an internal XTAL or TTL signal clock by a division of 1 to 2^{16} – 1.

The ACE is designed to work in either a polling or interrupt driven system, which is programmable by users software controlling an internal register.



PIN DESIGNATION



BLOCK DIAGRAM

WESTERN DIGITAL
CORPORATION

WD1943(8116)/WD1945(8136) Dual Baud Rate Clock

FEATURES

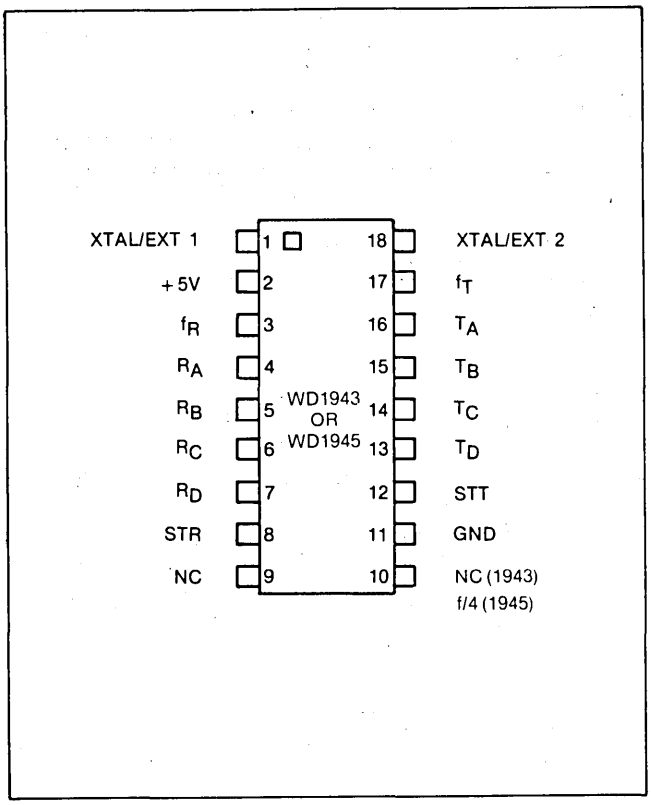
- 16 SELECTABLE BAUD RATE CLOCK FREQUENCIES
- OPERATES WITH CRYSTAL OSCILLATOR OR EXTERNALLY GENERATED FREQUENCY INPUT
- ROM MASKABLE FOR NON-STANDARD FREQUENCY SELECTIONS
- INTERFACES EASILY WITH MICROCOMPUTERS
- OUTPUTS A 50% DUTY CYCLE CLOCK WITH 0.01% ACCURACY
- 6 DIFFERENT FREQUENCY/DIVISOR PAIRS AVAILABLE
- SINGLE +5V POWER SUPPLY
- COMPATIBLE WITH BR1941
- TTL, MOS COMPATIBILITY
- WD1943 IS PIN COMPATIBLE TO THE COM8116
- WD1945 IS PIN COMPATIBLE TO THE COM8136 AND COM5036 (PIN 9 ON WD1945 IS A NO CONNECT)

GENERAL DESCRIPTION

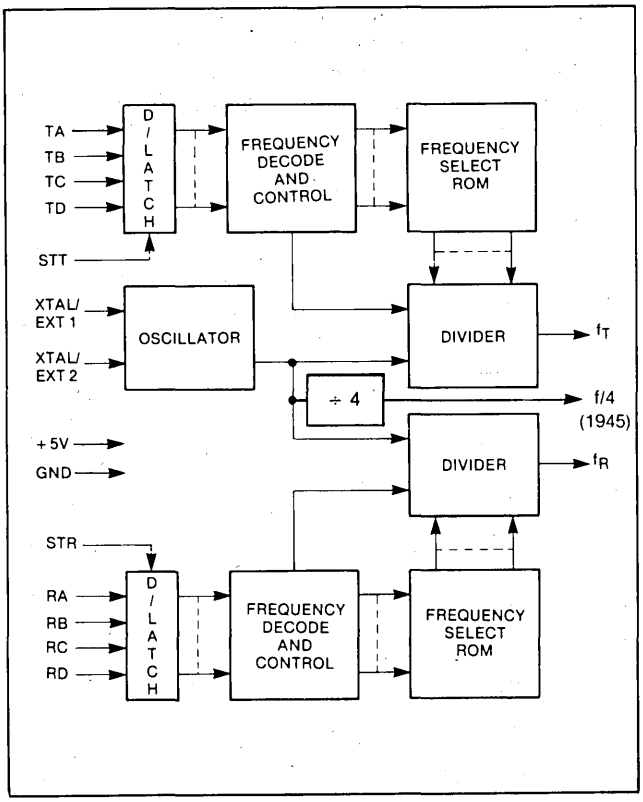
The WD1943/45 is an enhanced version of the BR1941 Dual Baud Rate Clock. The WD1943/45 is a combination Baud Rate Clock Generator and Programmable Divider. It is manufactured in N-channel MOS using silicon gate technology. This device is capable of generating 16 externally selected clock rates whose frequency is determined by either a single crystal or an externally generated input clock. The WD1943/45 is a programmable counter capable of generating a division by any integer from 4 to $2^{15} - 1$, inclusive.

The WD1943/45 is available programmed with the most used frequencies in data communication. Each frequency is selectable by strobing or hard wiring each of the two sets of four Rate Select inputs. Other frequencies/division rates can be generated by reprogramming the internal ROM coding through a MOS mask change. Additionally, further clock division may be accomplished through cascading of devices. The frequency output is fed into the XTAL/EXT input on a subsequent device.

The WD1943/45 can be driven by an external crystal or by TTL logic.



PIN DESIGNATION



BLOCK DIAGRAM

WESTERN DIGITAL
CORPORATION

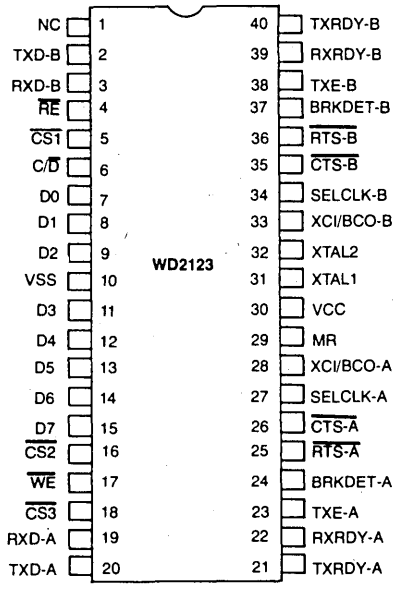
WD2123 DEUCE
Dual Enhanced Universal Communications Element

FEATURES

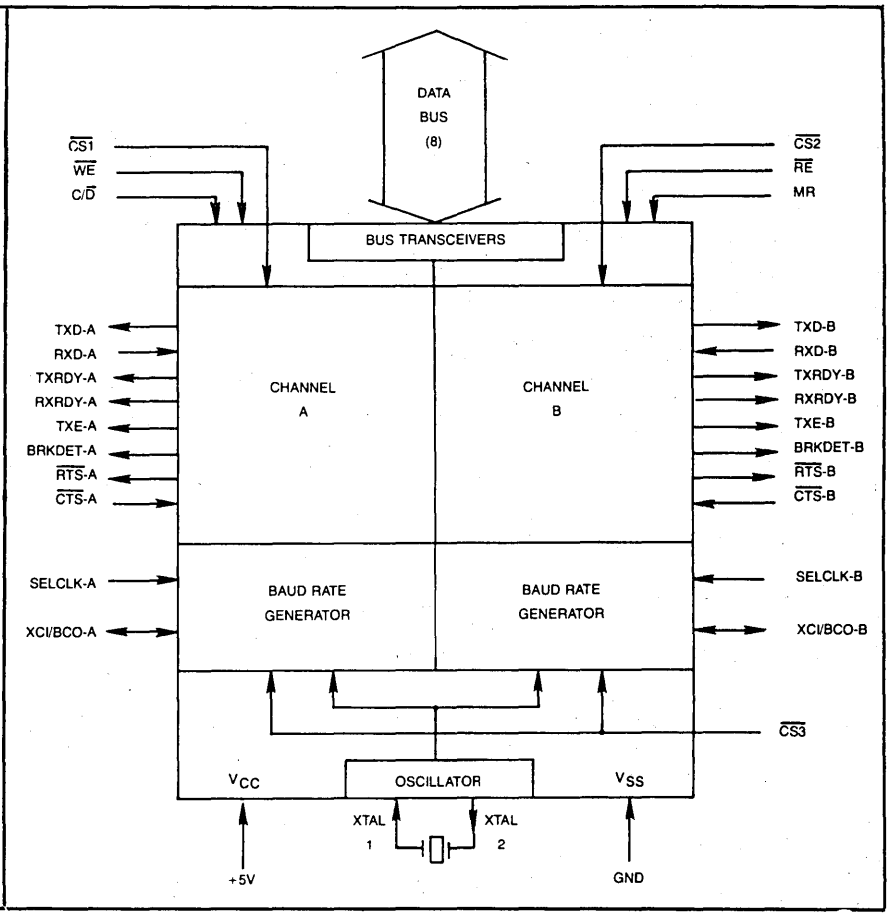
- TWO INDEPENDENT ASYNCHRONOUS FULL DUPLEX DATA COMMUNICATION CHANNELS (2 BOARTS)
- TWO INDEPENDENT BAUD RATE GENERATORS (ONE PER CHANNEL)
- EACH CHANNEL WITH FOLLOWING FEATURES:
- SELECTABLE 5 TO 8 BIT CHARACTERS
- 1X, 16X, 64X CLOCK RATES
- 16 SELECTABLE BAUD RATE CLOCK FREQUENCIES (INTERNAL)
- LINE BREAK DETECTION AND GENERATION
- 1, 1½, OR 2 STOP BIT SELECTION
- FALSE START BIT DETECTION
- ODD OR EVEN PARITY GENERATE AND DETECTION
- OVERRUN AND FRAMING DETECTION
- DOUBLE BUFFERING OF DATA
- TTL COMPATIBLE INPUTS AND OUTPUTS
- COMPATIBLE WITH 8251A (ASYNC ONLY) AND WD1983 DEVICES
- DIAGNOSTIC LOCAL LOOP-BACK MODE
- RXD INITIALIZATION UPON MASTER RESET
- ON-BOARD OSCILLATOR FOR EASE OF USE WITH A CRYSTAL
- VERSATILE CLOCK SELECT OPTIONS FOR INDEPENDENT TRANSMIT AND RECEIVE RATES

INTRODUCTION

The Western Digital WD2123 Dual Enhanced Universal Communications Element (DEUCE) is a single chip MOS/LSI Data Communications Controller Circuit that contains two independent full-duplex asynchronous RECEIVER/TRANSMITTER CHANNELS and two independent BAUD RATE GENERATORS. The WD2123 is fabricated in N-Channel silicon gate technology and is packaged in a 40 pin plastic or ceramic package. All inputs and outputs are TTL compatible.



PIN DESIGNATION



BLOCK DIAGRAM

WESTERN DIGITAL
CORPORATION

WD2001/WD2002 Data Encryption Devices

FEATURES

- CERTIFIED BY NATIONAL BUREAU OF STANDARDS.
- TRANSFER RATE:
  WD2001/2-05 300Kbs with 500KHz clock
  WD2001/2-20 1.3 Mbs with 2MHz clock
  WD2001/2-30 1.8 Mbs with 3MHz clock
- ENCRYPTS/DECRYPTS 64 BIT DATA WORDS USING 56 BIT KEY WORD
- SINGLE PORT 28 PIN PACKAGE WD2001 OR DUAL PORT 40 PIN PACKAGE WD2002
- COMMAND BIT PROGRAMMING VIA DAL BUS OR INPUT PINS
- DMA COMPATIBLE (SEE WESTERN DIGITAL DM1883)
- PARITY CHECK ON KEY WORD LOADING
- STANDARD 8 BIT MICROPROCESSOR INTERFACE
- INPUTS AND OUTPUTS TTL COMPATIBLE
- KEY STORED ON CHIP IS NOT EXTERNALLY ACCESSIBLE

  SEPARATE CLEAR AND CIPHER BUS STRUCTURE ON WD2002

APPLICATIONS

SECURE BROKERAGE TRANSACTIONS

ELECTRONIC FUNDS TRANSFERS

SECURE BANKING/BUSINESS ACCOUNTING

MAINFRAME COMMUNICATIONS

REMOTE AND HOST COMPUTER COMMUNICATIONS

SECURE A/D

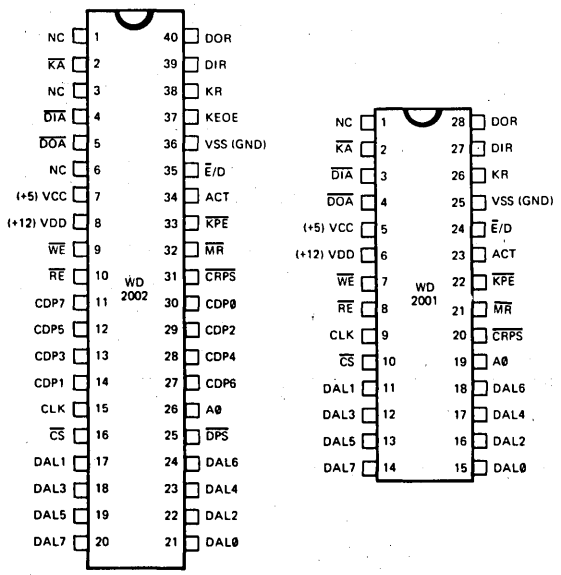
SECURE DISK OR MAG TAPE DATA STORAGE

SECURE PACKET SWITCHING TRANSMISSION

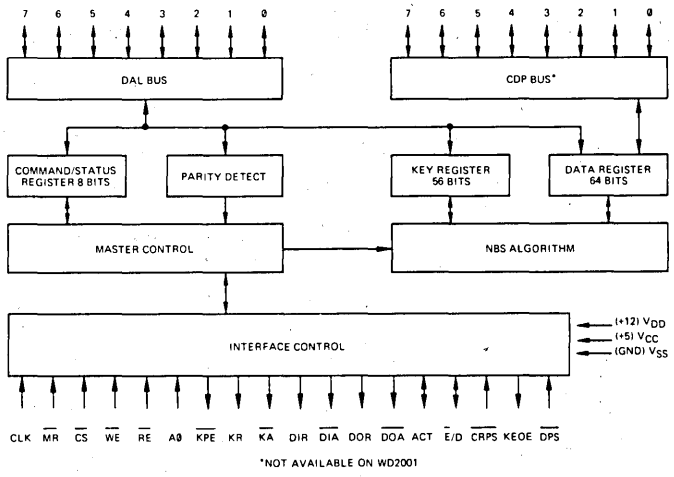
GENERAL DESCRIPTION

The Western Digital WD2001 and WD2002 Data Encryption/Decryption devices are designed to encrypt and decrypt 64-bit blocks of data using the algorithm specified in the Federal Information Processing Data Encryption Standard (#46). These devices encrypt a 64-Bit clear text word using a 56-Bit user-specified key to produce a 64-Bit cipher text word. When reversed, the cipher text word is decrypted to produce the original clear text word.

The DE2001/2 are fabricated in N-channel silicon gate MOS technology and are TTL compatible on all inputs and outputs.



PIN DESIGNATION



BLOCK DIAGRAM

WESTERN DIGITAL
CORPORATION

WD1993 Arinc 429 Receiver/Transmitter and Multi-Character Receiver/Transmitter

FEATURES

- PRESENT UPON MASTER RESET FOR ARINC 429 PROTOCOL
- PROGRAMMABLE WORD LENGTH FROM 1 CHARACTER TO 8 CHARACTERS
- PROGRAMMABLE CHARACTER LENGTH, 5, 6, 7, OR 8 BITS
- RETURN TO ZERO (RZ) OUTPUT
- AUTO SPACE GENERATION
- DOUBLE BUFFERED RECEIVER AND TRANSMITTER
- UNDERRUN ERROR DETECTION FOR TRANSMISSION
- OVERRUN, FRAMING AND PARITY ERROR DETECTION ON RECEIVER
- WORD ERROR FLAG FOR COMPREHENSIVE ERROR REPORTING
- FIRST CHARACTER OF WORD FLAG FOR SINGLE INTERRUPT APPLICATIONS
- DIAGNOSTIC LOCAL LOOP-BACK TEST MODE
- DC TO 200 KILOBITS PER SECOND OPERATION
- TTL COMPATIBLE INPUTS AND OUTPUTS
- SINGLE +5 VOLT SUPPLY
- TEMPERATURE RANGES 0°C to 70°C, — 1993-03, −40°C to +85°C — 1993-02, −55°C to +125°C — 1993-01

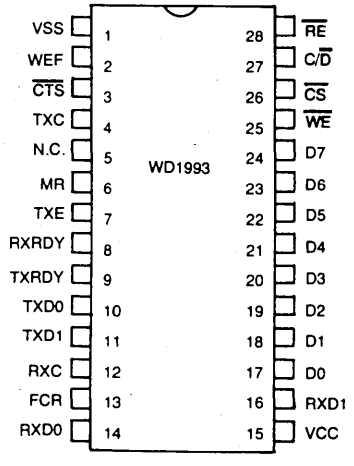
INTRODUCTION

The Western Digital WD1993 Avionic Receiver/Transmitter is designed to handle digital data transmission, according to the Avionic Arinc 429 protocol. Also, the word length is programmable from one to eight characters of 5, 6, 7, or 8 bits. Parallel data is converted into a serial data stream during transmission and serial to parallel during reception. The WD1993 is packaged in a 28 pin plastic or ceramic package and is available in three temperature ranges: Commercial, Industrial and Military.

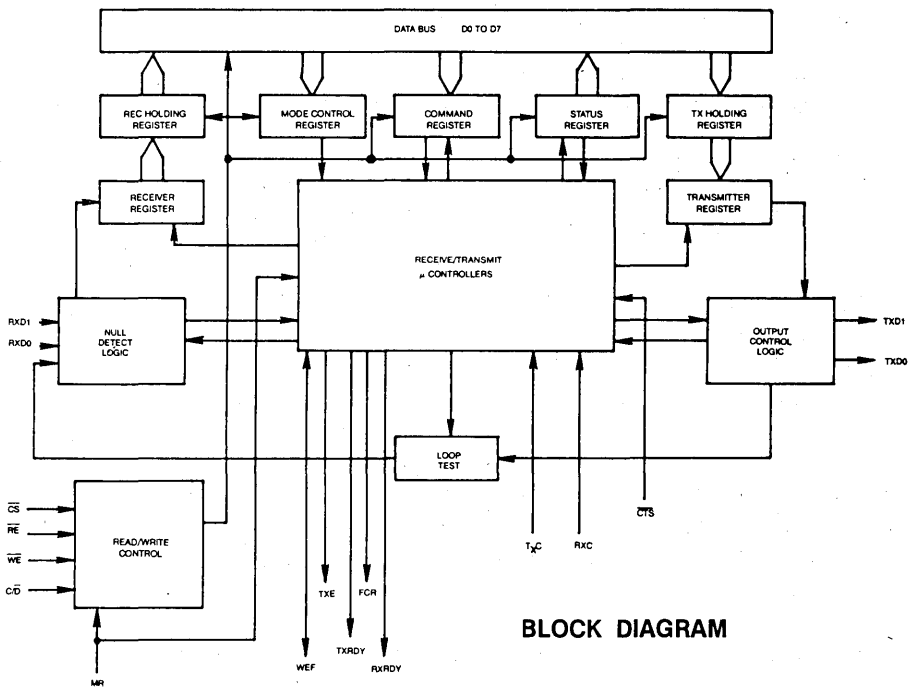
GENERAL DESCRIPTION

The WD1993 is a bus-orientated MOS/LSI device designed to provide the Avionics Arinc 429 Data Communication Protocol, along with programmable character length capabilities.

Also, the WD1993 contains a local loop-back test mode of operation, which is controlled by the Loop Test Enable (LTE) bit in the command register. In this diagnostic mode, the transmitter output is "looped-back" into the receiver input. The REN and TEN control bits must also be active ("1") and the CTS input must be low. The status and output flags operate normally.



PIN DESIGNATION



BLOCK DIAGRAM

WESTERN DIGITAL
CORPORATION

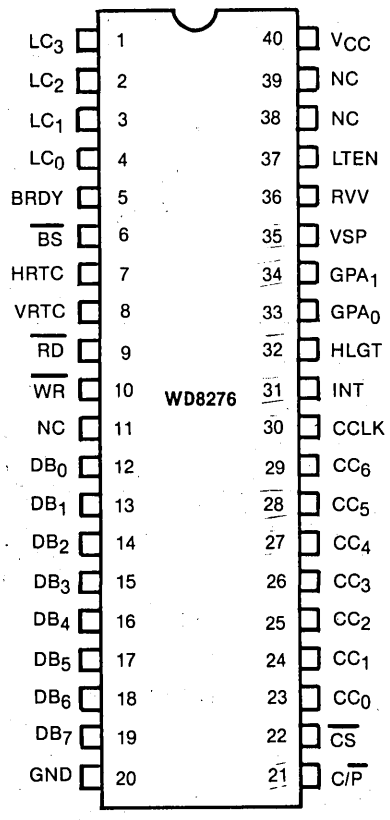
WD8276 Small System CRT Controller

FEATURES

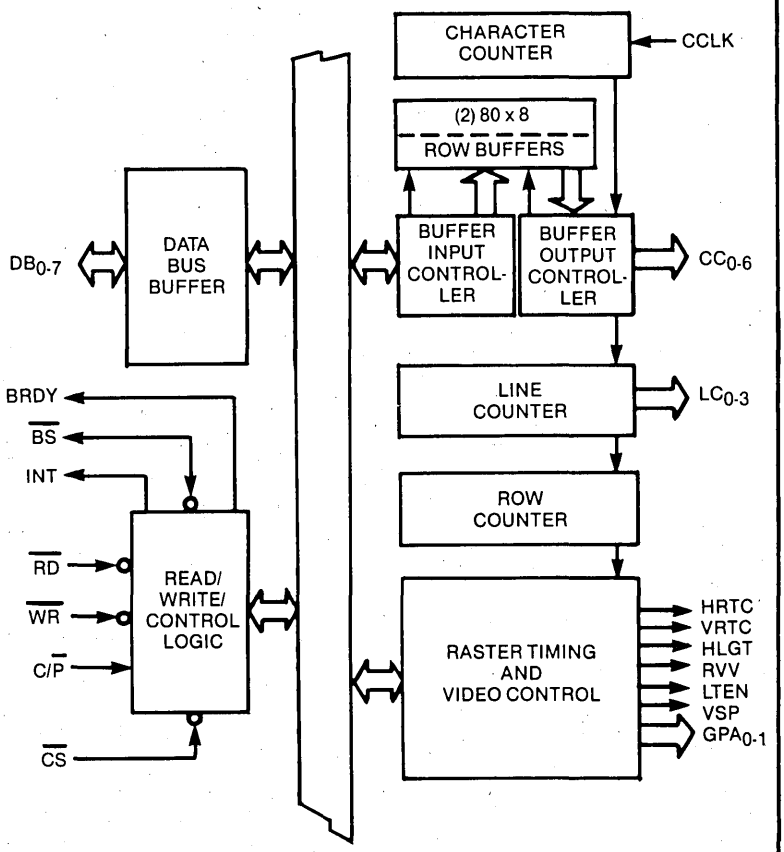
- PROGRAMMABLE SCREEN AND CHARACTER FORMAT
- 6 INDEPENDENT VISUAL FIELD ATTRIBUTES
- CURSOR CONTROL (4 TYPES)
- DUAL ROW BUFFERS
- SINGLE +5V SUPPLY
- 40-PIN PACKAGE

GENERAL DESCRIPTION

The WD8276 Small System CRT Controller is a single chip device intended to interface CRT raster scan displays with Intel microcomputers in minimum device-count systems. Its primary function is to refresh the display by buffering character information from main memory and keeping track of the display position of the screen. The flexibility designed into the WD8276 will allow simple interface to almost any raster scan CRT display with a minimum system IC count.



PIN DESIGNATION



BLOCK DIAGRAM

WESTERN DIGITAL
CORPORATION

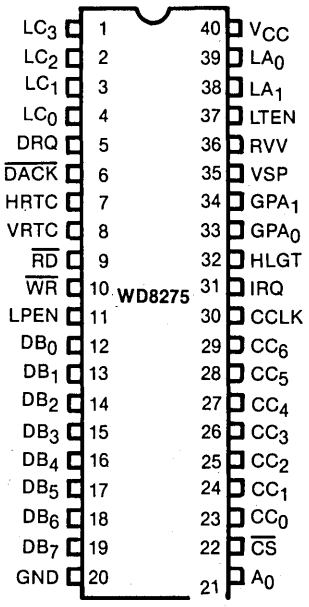
WD8275 Programmable CRT Controller

FEATURES

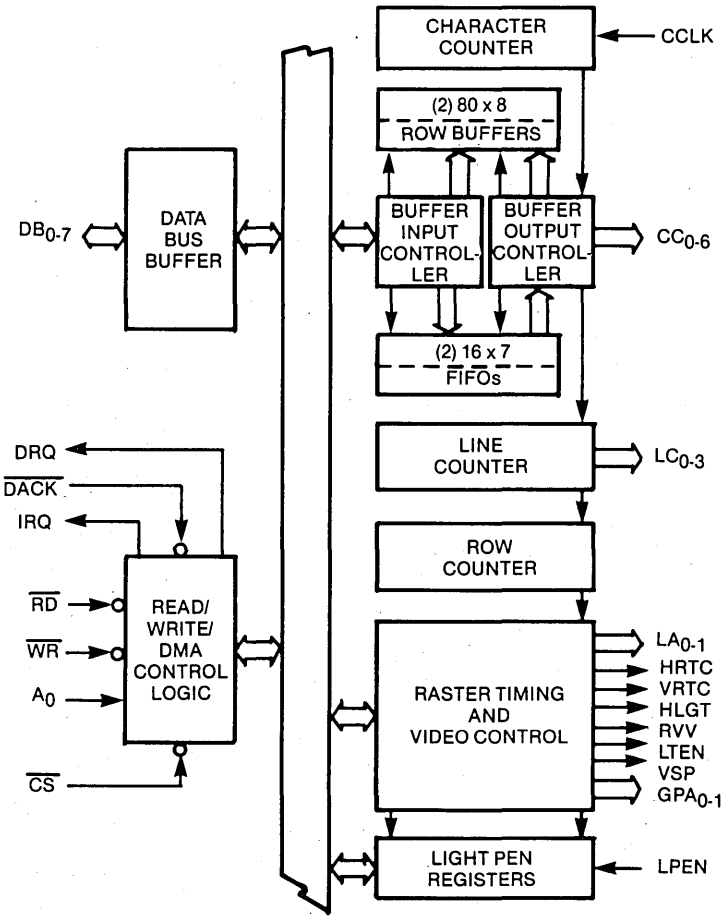
- PROGRAMMABLE SCREEN AND CHARACTER FORMAT
- 6 INDEPENDENT VISUAL FIELD ATTRIBUTES
- 11 VISUAL CHARACTER ATTRIBUTES (GRAPHIC CAPABILITY)
- CURSOR CONTROL (4 TYPES)
- LIGHT PEN DETECTION AND REGISTERS
- DUAL ROW BUFFERS
- PROGRAMMABLE DMA BURST MODE
- SINGLE +5V SUPPLY
- 40-PIN PACKAGE

GENERAL DESCRIPTION

The WD8275 Programmable CRT Controller is a single chip device to Interface CRT raster scan displays with microcomputer systems. Its primary function is to refresh the display by buffering the information from main memory and keeping track of the display position of the screen. The flexibility designed into the WD8275 will allow simple interface to almost any raster scan CRT display with a minimum of external hardware and software overhead.



PIN DESIGNATION



BLOCK DIAGRAM

WESTERN DIGITAL
CORPORATION

WD193X
Synchronous Data Link Controller

FEATURES

- HDLC, SDLC, ADCCP AND CCITT X.25 COMPATIBLE
- SDLC LOOP CAPABILITY
- DC TO 2.0 MBITS/SEC DATA RATE
- PROGRAMMABLE/AUTOMATIC FCS (CRC GENERATION AND CHECKING
- PROGRAMMABLE NRZI ENCODE/DECODE
- FULL SET OF MODEM CONTROL SIGNALS
- DIGITAL PHASE LOCKED LOOP
- MINIMUM CPU OVERHEAD
- ASYNCHRONOUS/SYNCHRONOUS MULTI-PROTOCOL BOARD CAPABILITY (PIN COMPATIBLE WITH WD 1931)
- SINGLE +5V SUPPLY
- DMA COMPATABILITY
- RESIDUAL CHARACTER CAPABILITY
- ADDRESS COMPARE
- GLOBAL ADDRESS RECOGNITION
- EXTENDABLE ADDRESS FIELD
- EXTENDABLE CONTROL FIELD
- MAINTENANCE MODE FOR SELF-TESTING

APPLICATIONS

FRONT END COMMUNICATIONS

PACKET SWITCHING

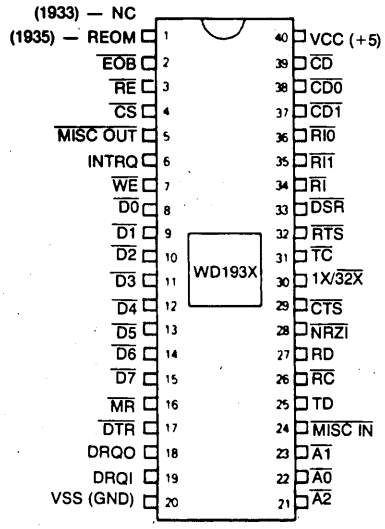
MULTIPLEXING SYSTEMS

LOCAL NETWORKS

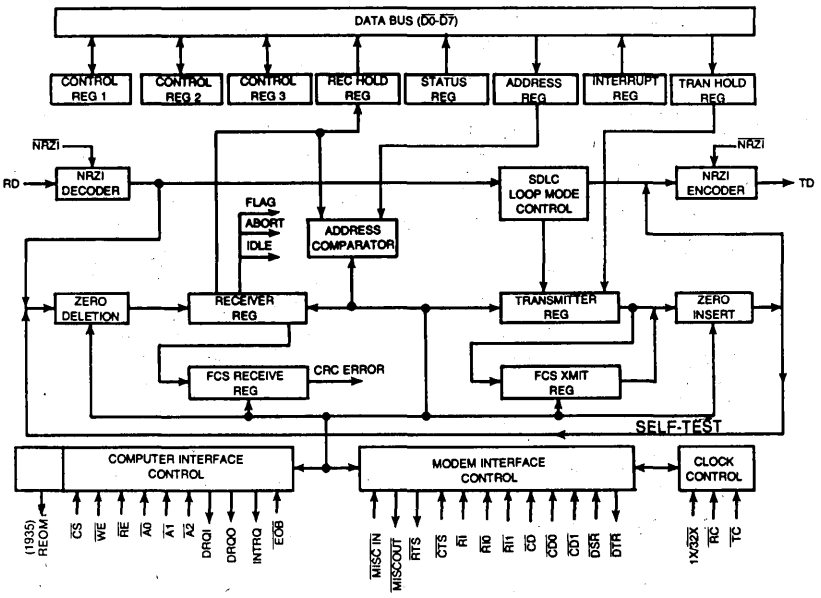
GENERAL DESCRIPTION

The WD193X is a MOS/LSI device which interfaces a parallel digital system to a synchronous serial data communication channel employing ISO's HDLC, IBM's SDLC or ANSI's ADCCP line protocol.

The WD193X is fabricated in N-channel depletion load MOS technology and is TTL compatible on all inputs and outputs. This controller requires a minimum of CPU software by supporting a comprehensive frame-level instruction set and by hardware implementation of the low level tasks associated with frame assembly/disassembly and data integrity. It can be programmed to encode/decode NRZI data. The internal clock is then derived from the NRZI data using a digital phase locked loop.



PIN DESIGNATION



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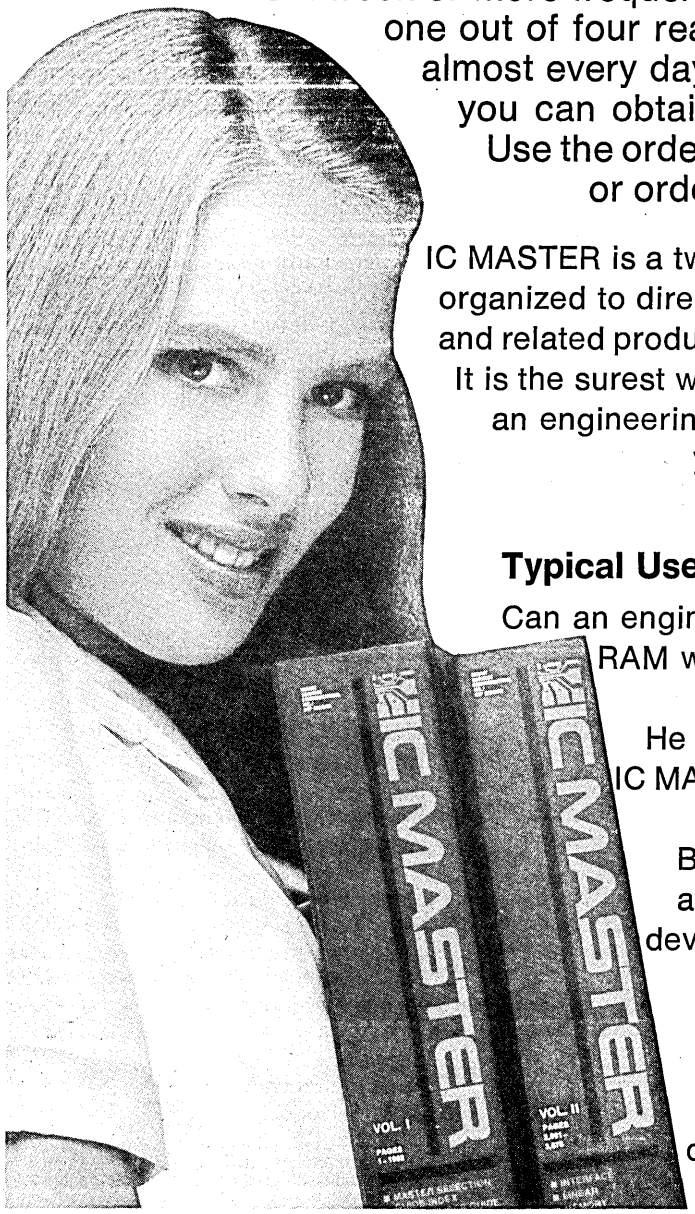

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INTRODUCTION TO LINEAR

The Master Selection Guide provides sufficient information to make initial product selections. All devices that appear in this section, both in the initial selection guide and the data pages, are included in all indexes. These index listings lead to the page and the line on that page where each device appears.

In the Linear section over 1100 operational amplifiers are covered. Since there are so many devices, the operational amplifier entries have been given special consideration. Separate lists are provided for those which have High Speed, High Voltage capability, Wide bandwidth, etc. Under General Purpose, four amplifier types are listed; these are the ones that the high volume manufacturers indicate are the most widely used; however, quad amplifiers should also be considered when appropriate. If you have located an op amp in a specialized category, you can review its characteristics by finding it in the Part Number or Product Indexes and looking it up in the Operational Amplifier Characteristics and in the Data Sections.

Following the special lists, the "Operational Amplifier Characteristics" listings categorize amplifiers by input parameters. They are arranged in order of increasing offset voltage, bias current, offset current and then voltage drift. The other parameters listed do not affect the sequence in which the devices are presented. The column labeled "Comp" indicates the number of external components normally used for compensation; for example "0" means no compensation is required.

Consumer circuits such as audio amplifiers, AM, FM, and TV circuits as well as some digital devices (watches, calculators, etc.) are covered by model number in the Consumer Circuit Section. Linear devices and unusual circuits which do not fit elsewhere are listed under the heading "Other Linear Devices."

Detailed Product Information provided by:

The manufacturers listed above have provided detailed information on their latest and most significant products.

EINFÜHRUNG LINEAR-SCHALTUNGEN

Der Master Selection Guide für Linearschaltungen enthält alle Informationen, die Sie für die Erstauswahl Ihres Produkts benötigen. Die Bauteile, die in diesem Abschnitt erscheinen, sowohl im Selection Guide als auch auf den Datenblättern, sind in allen Master Indexes enthalten. Diese Register verweisen auf die Seite und Zeile, auf der das entsprechende Bauelement vorkommt.

Der Linear-Teil enthält über 1100 Operationsverstärker. Da es hier sehr viele Bausteine gibt, haben die Eintragungen über Operationsverstärker besondere Beachtung gefunden. Es gibt getrennte Listen für solche mit hoher Geschwindigkeit, hoher Spannung, großer Bandbreite usw. Unter "Allgemeine Verwendung" (General Purpose) finden sich vier Verstärkertypen. Laut Aussage der großen Hersteller sind dies die Gebräuchlichsten. Jedoch sollten auch Vierfach-Verstärker auf ihre Verwendbarkeit hin untersucht werden. Haben Sie einen Operationsverstärker in einer bestimmten Kategorie gefunden, so schlagen Sie ihn im numerishen Typenverzeichnis oder im Produktverzeichnis nach und überprüfen seine Eigenschaften unter der Rubrik "Operational Amplifier Characteristics" und in den Datenblättern.

Der Abschnitt "Eigenschaften von Operationsverstärkern" (Operational Amplifier Characteristics) bestimmt die Verstärker nach Eingangs-Parametern. Sie sind nach steigender Offsetspannung, Bias-Strom, offsetstrom und Spannungsdrift angeordnet. Die übrigen aufgeführten Parameter haben keinen Einfluß auf die Reihenfolge, in der die Bauteile genannt werden. Die Spalte "Comp" nennt die Anzahl externer Bausteine, die normalerweise für die Kompensation verwendet werden. "O" z.B. bedeutet, daß keine externe Kompensation erforderlich ist.

Consumer-Schaltkreise wie Audio-Verstärker, AM, FM und TV-Schaltungen sowie einige Digital-Bauteile (Uhren, Rechner usw.) erscheinen nach Typennummer im Abschnitt "Consumer Circuit Section." Solche Linear-Bauelemente und Schaltungen, die in keine entsprechende Rubrik passen, werden unter der Uberschrift "Sonstige Linear-Bauelmente" (Other Linear Devices) aufgeführt.

Neu in diesem Jahr sind erweiterte Listen von Sample/Hold Verstärkern und von festen und einstellbaren Spannungsreferenzen (Fixed and Adjustable Voltage References). Zusätzlich zu der Auflistung unter "Other Linear Devices" finden Sie wichtige Leistungsparameter für diese Produkte am Schluß des Linear-Hauptteils.

INTRODUCTION AUX SYSTEMES LINEAIRES

Le Guide Général de Sélection fournit suffisamment de renseignements pour permettre des sélections initiales de produits. Tous les appareils mentionés dans cette Section, à la fois das le Premier Guide de Selection et dans les feuilles de données, sont inclus dans tous les index. Ces index indiquent à quelle page et à quelle ligne il a été fait mention de tel ou tel appareil.

La Section "Linéaire" décrit plus de 1100 amplificateurs opérationnels. Du fait du nombre considérable d'appareils entrant dans cette catégorie, une attention toute spéciale a été apportée lors de leur classification. Des listes énumèrent séparément les appareils à grande vitesse, à capacité de haut voltage, à grande plage de fréquence, etc. Dans la rubrique "Applications Générales" (General Purpose), quatre types d'amplificateurs sont cités. Ce sont, d'après les gros fabricants, ceux qui sont le plus couramment usités. Les amplificateurs "QUAD" sont également dignes d'attention dans certains cas. Si vous recherchez un amplificateur opérationnel dans une categorie bien definie, vous pourrez en obtenir les caractéristiques en consultant les index des Numéros de Pièces ou de Produits, ainsi que la Section "Caractéristiques des Amplificateurs Opérationels" et les feuilles de données.

La Section "Caractéristiques des Amplificateurs Opérationnels", offre une liste d'amplificateurs classes par paramètre d'entrée. Ces derniers font apparaître dans l'ordre : la tension de compensation, l'ajustement intensité/courant, la compensation du courant, et enfin le changement de tension. Les autres paramètres indiqués n'affectent pas l'ordre dans lequel les appareils sont presentés. La colonne intitulee "COMP" indique le nombre de composants externes également utilisés dans un but de compensation, exemple : "0" signifie qu'aucune compensation n'est nécessaire.

Les circuits de grande consommation tels que les amplificateurs radio AM, FM, les amplificateurs télévision, ainsi que les appareils digitaux (montres, calculatrices, etc.) sont regroupés par numero de modèle dans la Section "Circuits de Grande Consommation" (Consumer Circuit Section). Les appareils linéaires et autres circuits de moins grande utilisation qui n'entrent pas dans les autres catégories, sont énumérés dans la Section "Autres Appareils Linéaires" (Other Linear Devices).

Un additif nouveau à l'édition de cette année : des références sur les amplificateurs partiels/continus, et avec voltage fixe ou ajustable. En plus des listes fournies dans la Section "Autres Appareils Linéaires", d'autres paramètres de performance relativement importants pour ces produits, apparaîssent à la fin du Guide Général de Sélection Linéaire.

INTRODUCCIÓN A LINEAL

La Guía Maestra de Selección provee suficiente información para hacer selecciones iniciales del producto. Todas las componentes que aparecen en esta sección, ya sea en la guía de selección inicial o en las páginas de datos, están incluídas en todos los otros índices. Estas listas de índices los refiere a la página y linea de aquella página donde se encuentra cada componente.

En la sección bajo Lineal, aparecen más de 1,100 amplificadores operacionales. Debido a que hay tantas componentes, se les ha dado consideración especial a los amplificadores operacionales. Listas apartes son provistas para equellos con Alta Velocidad, Capacidad de Alto Voltaje, Banda Ancha, etc. Bajo Propósito General, aparecen cuatro tipos de amplificadores, éstos son los que los fabricantes mayores piensan son los más usados; sin embargo, los amplificadores cuadrangulares deben también ser considerados cuando sea necesario. Si usted ha localizado un amp. op. en una categoría especializada, puede usted estudiar sus características encontrándolo en el Indice de Producto o Número de Pieza y buscándolo en la Sección de Datos de las Características de los Amplificadores Operacionales.

Siguiendo las listas especiales, la lista de "Características del Amplificador Operacional" categoriza los amplificadores por parámetros de entrada. Estos están arreglados por orden ascendente de tensión contrapuesta corriente de polarización, corriente contrapuesta, y también deslizamiento de voltaje o tensión. Los otros parametros mencionados no afectan la secuencia en que las componentes aparecen. La columna titulada "Comp" indica el número de componentes externas que normalmente se emplean para compensación; por ejemplo "O" significa que no requiere compensación.

Circuitos del Consumidor como audioamplificadores, AM, FM, y circuitos de TV así como también algunas componentes digitales (relojes, calculadoras, etc.) aparecen por número de modelo en la Sección de Circuitos del Consumidor. Componentes Lineales y circuitos poco comunes que no corresponden en otras secciones aparecen bajo el título "Otras Componentes Lineales."

Listas expandidas para Amplificadores de Muestra/Retención y Referencias de Voltaje Fijas y Ajustables son nuevas para este año. Además de las listas bajo Otras Componentes Lineales, parámetros de redimiento significantes para estos productos aparecen al final de la Guúa Maestra de Selección.

リニアへの案内

マスターセレクションガイドは素子選択にとりかかる充分な資料を揃えています。最初のセレクションガイド並にデータ掲載ページとこのセクションに記載されている製品はどのインデックスにも入っていて，そのページ数と行数がすぐ分ります。

ここでは1,100種以上のオペアンプが収録されています。余りに多品種のため，特別の配慮をしました。それはオペアンプを高速，高耐圧，高域巾他と別々に掲載しました。搬用オペアンプには4種のアンプをのせてあります。大量生産している会社が最も巾広く使用されていると云う品種です。がクオドアンプももし適当なものがあれば考慮すべきかも知れません。
あるカテゴリーでオペアンプを見つけられたらその特性をパーツナンバーインデックスかプロダクトインデックスで探し検討し，オペアンプ特性表やデータセクションを良く調べて下さい。

特殊品種リストに続きオペアンプ特性表があり入出パラメーター毎にオペアンプが分類されています。製品はオフセット電圧，バイアス電流，オフセット電流，電圧ドリフト等小さな順に記載されています。"Comp"と表示されている項目の下の数字は0調整をする為に外付部品が何個必要かを示しています。例えば"0"となっていれば0調整不要を意味します。

民生用製品 - オーディオアンプ，AM，FM，TV素子，ディジタル素子（時計用，電卓用等）は"コンシューマーサーキットセクション"に掲載されています。他のどのカテゴリーにも入らないリニアや特異な素子は"アザーリニアデバイス"の見出しに載っています。

本年新たに加わったものとしてサンプル／ホールドアンプと固定，調整可能なボルティジリファレンスが広くのっています。"アザーリニアデバイス"欄にのっている製品中顕著な性能パラメーターはリニアマスターセレクションガイドの最後に掲載されています。

LINEAR–Amplifiers, Special Purpose

Function	Device	Source	Line
Special Purpose			
AC Amplifier, Quad, Single Supply	CA3048	† RCA	
	CA3052	RCA	
AGC Amplifier, 20 Hz to 10 MHz, 6 dB Dynamic Range	MY108	Analog Sys	
AGC Generator, for SSB Receivers	SL621C	Plessey	
AGC Generator (voice operated gain adjusting device)	SL620C	Plessey	
	SL6270	Plessey	
Amplifier, CATV. See Linear—Consumer Circuits, TV			
Amplifier for IR Remote Control (1300 dB gain, 8 kHz bandwidth)	U250	Telefunken	
	U3043M	Telefunken	
	U3083M	Telefunken	10
Amplifier with Photodiode	TFA1001	Siemens	
Amplifier, Triple for Active Filters (see also linear—other devices, active filters)	TAA960	Signetics	
Audio Amplifier with Three NPN Transistors	**LM389**	**National (3326,3328)**	
Current Amplifier (unity gain, 100 mA output)	LH0002	† Harris	
	LH0002C	Harris	
	LH0002	**† National (3342)**	
	LH0002C	**National (3342)**	
Current Amplifier (unity gain, 200 mA output)	3553	† Burr-Brown	
	9963	**† OEI (3346)**	
Current Amplifier (unity gain, 300 mA output)	MC1438	Motorola	20
	MC1538	† Motorola	
	2003	Teledyne P	
	2003-01	† Teledyne P	
Current Amplifier (unity gain, 500 mA output)	**9910**	**† OEI (3346)**	
	9911	**† OEI (3346)**	
Current Amplifier (unity gain, 600 mA output)	**HA-2630**	**† Harris (3230,3287)**	
	HA-2635	**Harris (3230,3287)**	
Current Amplifier (wideband, 100 mA output)	**HOS-100AH**	**AD (3155)**	
	HOS-199SH	† AD	
Current Amplifiers, See also Linear-Followers			30
Current Booster, 100 mA Output (for op amp)	2035	† Teledyne P	
Differential/Cascode Amplifier (dc to rf)	MC3330	Motorola	
	CA3028A	† RCA	
	CA3028B	† RCA	
	CA3053	† RCA	
Differential Input/Differential Output Amplifier (bandwidth less than 2 MHz)	MC1590G	† Motorola	
	CA3000	† RCA	
	CA3007	† RCA	
Differential/Video Amplifier	μPC754	NEC-Electron	
Fiber Optic Receiver Amplifier	LH0082	† National	40
	LH0082C	National	
Floppy Disc Read Amplifier System	**XR3470**	**Exar (3189)**	
	MC3470	**Motorola (2750)**	
	MC3470	TI	
Floppy Disc Write Amplifier	**SN75251C**	**TI (3437)**	
Front End Amplifier (for ultrasonic or infrared remote control systems)	TDA4180	Telefunken	
Hearing Aid Amplifiers. See Linear-Consumer Circuits			
Instrumentation Amplifier	INA101AM	† Burr-Brown	
	INA101BM	† Burr-Brown	
	INA101CM	† Burr-Brown	50
	INA101SM	† Burr-Brown	
Instrumentation (commutating auto zero)	ICL7605C	Intersil	
	ICL7605M	† Intersil	
	ICL7606C	Intersil	
	ICL7606M	† Intersil	
Instrumentation, (differential input, independent gain adjustment)	**AD522A**	**AD (3158)**	
	AD522B	**AD (3158)**	
	AD522S	**† AD (3158)**	
	AD612A	**AD (3158)**	
	AD612B	**AD (3158)**	60
	AD612C	**AD (3158)**	
	AD614A	**AD (3158)**	
	AD614B	**AD (3158)**	
	HC3020	HyComp	
	LM163A	† National	
	LM363	National	
	LM363A	† National	
	AD521J	**AD (3158)**	
	AD521K	**AD (3158)**	
	AD521L	**AD (3158)**	70
	AD521S	**† AD (3158)**	
	3626A	Burr-Brown	
	3626B	Burr-Brown	
	3626C	Burr-Brown	
	3629	† Burr-Brown	
	3630A	Burr-Brown	
	3630B	Burr-Brown	
	3630C	Burr-Brown	
	3630S	Burr-Brown	
	3660J	Burr-Brown	80
	3662	Burr-Brown	
	MN2200	Micro Net	
	MN2200H	† Micro Net	
	MN2201	Micro Net	
	MN2201H	† Micro Net	
	LH0036	**† National (3343)**	
	LH0036C	**National (3343)**	
	LH0037	**† National (3343)**	
	LH0037C	**National (3343)**	
	LH0038	**† National (3343)**	90
	LH0038C	**National (3343)**	
Instrumentation, Digitally Programmable Gain	**AM-542MC**	**Datel (2623)**	
	AM-542MM	**† Datel (2620)**	
	AM-542MR	Datel	
	AM-543MC	**Datel (2623)**	
	AM-543MM	**† Datel (2620)**	
	AM-543MR	Datel	
	PGA100AG	Burr-Brown	
	PGA100BG	Burr-Brown	
	LH0084	**† National (3343)**	100
	LH0084C	**National (3343)**	
	LH0086	**† National (3343)**	
	LH0086C	**National (3343)**	
Instrumentation, Pin Programmable Gain	AD624A	AD	
	AD624B	AD	
	AD624C	AD	
	AD624S	† AD	
Instrumentation, (unity gain)	3627	Burr-Brown	
Isolation Amplifier, Optically Coupled	3650HG	Burr-Brown	
	3650MG	Burr-Brown	110
	3652HG	Burr-Brown	
	3652MG	Burr-Brown	
	3656BG	Burr-Brown	
	3656HG	Burr-Brown	
	ISO100AP	Burr-Brown	
	ISO100BP	Burr-Brown	
	ISO100CP	Burr-Brown	
Isolation Amplifier, Transformer Coupled	3456	Burr-Brown	
	3656AG	Burr-Brown	
	3656BG	Burr-Brown	120
Limiting Amplifier/Detector	SAB1009B	Signetics	
Linear-Antilog Amplifier (current in, current out)	SSM2010	SSM	
	SSM2012	SSM	
Linear-Antilog Amplifier, Dual (differential input, separate control inputs)	SSM2000	SSM	
	SSM2020	SSM	
	SSM2022	SSM	
Log Amplifier, Bipolar (module)	**2531A**	**OEI (3347)**	
	2540	OEI	
Log/Antilog Amplifier, (antilog)	ICL8049C	Intersil	
	2910	**† OEI (3347)**	130
	SSM2100	SSM	
Log/Antilog Amplifier, (log)	4127	Burr-Brown	
	ICL8048C	Intersil	
	2910	† OEI	
	TL441C	TI	
	TL441M	† TI	
Log/Log Ratio Amplifier	LOG100	Burr-Brown	
Microphone Amplifier, Electret	PBL3721	RIFA	
Microphone Amplifier (for microphones in telephones)	TAA970	Signetics	
	TCA980	Signetics	140
	TDD0246	Telefunken	
Microphone/Headphone Amplifier	SL6310	Plessey	
Mixer (to 200 MHz)	S042	Siemens	
MOS Amplifier, MOS and NPN Transistors, 3 Terminal	TAA320	Signetics	
	TAA320A	Signetics	
Operational Amplifier, Band-Select Switch, AFT Mode Switch (for frequency-synthesizer TV systems)	CA3166	RCA	
Operational Amplifier/Comparator with Shutdown Control and Isolated Transistor	CA3177	RCA	
Operational Amplifier/Voltage Comparator, Dual	LM192	† National	
	LM292	National	
	LM392	National	150

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Amplifiers, Special Purpose (Cont'd)

Function	Device	Source	Line
Special Purpose (Cont'd)			
Operational Amplifier/Voltage Comparator, Dual (Cont'd)			
	LM2924	National	
	LM3924	National	
Operational Amplifier, Dual with Dual Voltage Comparator			
	MC3405	Motorola	
	MC3505	† Motorola	
Operational Transconductance Amplifier, Dual			
	LM13600	Raytheon	
	LM13600A	Raytheon	
Power Amplifier, Motor and Actuator Driver, to 12 V, 1.5 A			
	ICH8515I	Intersil	
	ICH8515M	† Intersil	
Power Amplifier, Motor and Actuator Driver, to 24 V, 3 A			
	ICH8510I	Intersil	
	ICH8510M	† Intersil	10
	ICH8520I	Intersil	
	ICH8520M	† Intersil	
	ICH8530I	Intersil	
	ICH8530M	† Intersil	
Power Transistor Driver/Amplifier, Biases External MOSFET Devices			
	MA500	Analog Sys	
Preamplifier, for Ultrasonic Remote Control			
	TDA3047	Signetics	
	TDB2033	Signetics	
Preamplifier, Infrared (74 dB gain, 100 kHz bandwidth)			
	TDA4050B	Siemens	
Preamplifier, Low Noise (35 dB gain, 100 MHz bandwidth)			
	AH0013CA	**OEI (3346)**	
	AH0013CB	**OEI (3346)**	20
	AH0013MA	**† OEI (3346)**	
Preamplifier, Low Noise (40 dB gain, 20 MHz bandwidth)			
	9913	OEI	
Preamplifier, Low Noise (100 dB gain, 50 MHz bandwidth)			
	9923	OEI	
Preamplifier, Precision (to precede operational amplifiers)			
	LM121	† National	
	LM121A	† National	
	LM221	National	
	LM221A	National	
	LM321	National	
	LM321A	National	
Preamplifier, Temperature Controlled			
	μA727C	Fairchild	30
	μA727M	† Fairchild	
Programmable Channel Op Amp (one of 4 input stages can be connected to single output)			
	HA-2400	**† Harris (3212,3287)**	
	HA-2404	**Harris (3212,3287)**	
	HA-2405	**Harris (3212,3287)**	
Programmable Gain Amplifier (digitally controlled gain)			
	3606	Burr-Brown	
	3607	Burr-Brown	
	HS2020	Hybrid Sys	
	MN2020	Micro Net	
Read Amplifier/Preamplifier (for magnetic tape memory systems)	MC3467	Motorola	
	MC3468	Motorola	40
RF Amplifier, Gated			
	MC1445	Motorola	
	MC1545	† Motorola	
	MC1445	TI	

Function	Device	Source	Line
RF Amplifiers, Hybrids			
	MHW401	Motorola	
	MHW590	Motorola	
	MHW591	Motorola	
	MHW592	Motorola	
	MHW593	Motorola	
	MHW601	Motorola	
	MHW602	Motorola	50
	MHW603	Motorola	
	MHW709	Motorola	
	MHW710	Motorola	
	CA2800	TRW	
	CA2810	TRW	
	CA2820	TRW	
	CA2830	TRW	
	CA2840	TRW	
	CA2842	TRW	
	CA2850	TRW	60
	CA2851	TRW	
	CA2870	TRW	
	CA2871	TRW	
	CA2875	TRW	
	CA2876	TRW	
	CA2880	TRW	
Signal Sources Switch, (buffer amplifiers with input switches)	TDA1028	Signetics	
	TDA1029	Signetics	
Video, IF and RF Amplifiers			
	CLC100	Comlinear	
	CLC102	Comlinear	70
	μA733C	Fairchild	
	μA733M	† Fairchild	
	μA733	† Intersil	
	μA733C	Intersil	
	MC1550	† Motorola	
	MC1552	† Motorola	
	MC1553	† Motorola	
	MC1733	† Motorola	
	MC1733C	Motorola	
	NE592	Motorola	80
	SE592	† Motorola	
	LM733	† National	
	AN606	Panasonic	
	AN607	Panasonic	
	AN608	Panasonic	
	SL1550	Plessey	
	SL541	Plessey	
	SL550	Plessey	
	SL560	Plessey	
	SL610C	Plessey	90
	SL611C	Plessey	
	SL612C	Plessey	
	CA3001	† RCA	
	CA3004	† RCA	
	CA3011	† RCA	
	CA3020A	RCA	
	CA3021	† RCA	
	CA3022	† RCA	
	CA3023	† RCA	
	CA3040	† RCA	100
	NE592	Signetics	
	SE592	† Signetics	
	TDA3541	Signetics	
	μA733	† Signetics	
	μA733C	Signetics	
	SG1401	† Silicon G	
	SG2401	Silicon G	
	SG3001	† Silicon G	
	SG3401	Silicon G	
	SG733	† Silicon G	110
	SG733C	Silicon G	
	NE592	TI	
	TL592	**TI (3435)**	

(Continued)

Function	Device	Source	Line
Video, IF and RF Amplifiers (Cont'd)			
	μA733C	TI	
	μA733M	† TI	
	TA7061A	Toshiba	
Voltage Controlled Amplifier: See also Compander under: Linear—Telecommunication Circuits			
Wide Band Amplifier/÷32/33 Divider			
	SAA1058	Signetics	
Wideband Amplifier, Logarithmic Limiting (4 to 500 MHz)			
	SL1531	Plessey	
	SL1532	Plessey	120
	SL531C	Plessey	
	SL532C	Plessey	
Wideband Amplifier with Low Level Video Detection (7 to 200 MHz for log IF amplifiers)			
	SL1521	† Plessey	
	SL1522	Plessey	
	SL1523	Plessey	
	SL1524	Plessey	
	SL1525	Plessey	
	SL521	Plessey	
	SL523	Plessey	
Single-Ended Input/Output Amplifier, Triple			
	CA3035	RCA	130
Hex Analog CMOS Amplifier			
	MA113	Analog Sys	
Two Wire Transmitter (Sends current signal over same two lines from which it is powered.)			
	XTR100AM	† Burr-Brown	
	XTR100AP	Burr-Brown	
	XTR100BM	† Burr-Brown	
	XTR100BP	Burr-Brown	
	LH0045	† National	
	LH0045C	National	

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Arrays

Transistor Arrays

Function	Device	Source	Line
Darlington Pair and Two Matched NPN Transistors			
	CA3018	† RCA	
	CA3018A	† RCA	
	CA3118	† RCA	
	CA3118A	† RCA	
	SFC2018	† Thomson-CSF	
Differential Pair and Three NPN Transistors			
	μA3086M	Fairchild	
	MC3346	† Motorola	
	MC3386	† Motorola	
	LM3045	† National	
	LM3046	National	10
	LM3086	National	
	LM3146	National	
	SL3045	† Plessey	
	SL3046	Plessey	
	SL3086	Plessey	
	SL3145	† Plessey	
	SL3146	Plessey	
	CA3045	† RCA	
	CA3046	† RCA	
	CA3086	† RCA	20
	CA3146	RCA	
	CA3146A	RCA	
	TBA331	SGS	
	TCA671	Siemens	
	TCA871	Siemens	
	TCA971	Siemens	
	TCA991	Siemens	
	SG3045	Silicon G	
	SG3046	Silicon G	
	SG3086	† Silicon G	30
	SG3146	Silicon G	
	SG3821	Silicon G	
	SG3886	Silicon G	
	ULN-2046A	Sprague	
	ULN-2086A	Sprague	
	ULS-2045H	† Sprague	
	SFC2046	† Thomson-CSF	
Dual Darlington (NPN) and Two NPN Transistors			
	SG3823	Silicon G	
Dual Darlington (NPN)			
	CA3036	† RCA	
	SFC2036	† Thomson-CSF	40
Dual Darlington (NPN-PNP quasi complementary)			
	TDA1410	SGS	
	TDA1420	SGS	
Dual Darlington Switch			
	ULN-2061M	**Sprague (2843)**	
	ULN-2062M	**Sprague (2843)**	
Dual Differential Amplifiers (NPN), Biasing, to Above 100 MHz			
	NE510	Signetics	
	NE511	Signetics	
	SE510	† Signetics	
	SE511	† Signetics	
Dual Differential Amplifiers (NPN), to 120 MHz			
	CA3054	Motorola	
	CA3026	RCA	50
	CA3054	RCA	
	SG3822	Silicon G	
	ULN-2054A	Sprague	
Dual Differential Amplifiers (NPN), to 500 MHz			
	CA3049	† RCA	
	CA3102	† RCA	
Dual Differential Amplifiers (NPN) with Diode Bias String			
	CA3050	† RCA	
	CA3051	RCA	
Dual Matched Transistor Pairs, NPN			
	SL354	Plessey	
Dual Transistors (f4t>5 GHz)			
	SL2363C	Plessey	
	SL2364C	Plessey	60
Dual Transistors, Monolithic NPN, Logarithmic Conformance	MP318	Micro Pwr	
	MAT-01	† PMI	
	MAT-01A	† PMI	
	MAT-01F	† PMI	
	MAT-01G	† PMI	
	MAT-01H	PMI	
Dual Transistors, Monolithic NPN Tightly Matched			
	IT120	Intersil	
	IT120A	Intersil	
	IT121	Intersil	
	IT122	Intersil	70
	MP301	Micro Pwr	
	MP302	Micro Pwr	
	MP303	Micro Pwr	
	MP310	Micro Pwr	
	MP311	Micro Pwr	
	MP312	Micro Pwr	
	MP360	Micro Pwr	
	LM194	† National	
	LM394	National	
	SL360	Plessey	80
	SL362	Plessey	
Dual Transistors, Monolithic PNP, Logarithmic Conformance	MP358	Micro Pwr	
Dual Transistors, Monolithic PNP, Tightly Matched			
	IT130	Intersil	
	IT130A	Intersil	
	IT131	Intersil	
	IT132	Intersil	
	MP350	Micro Pwr	
	MP351	Micro Pwr	
	MP352	Micro Pwr	
Quad Darlington Switch			
	ULN2068	**Motorola (2753)**	90
	ULN2074	Motorola	
	L702	SGS	
	SG2064	Silicon G	
	SG2065	Silicon G	
	SG2066	Silicon G	
	SG2067	Silicon G	
	SG2068	Silicon G	
	SG2069	Silicon G	
	SG2070	Silicon G	
	SG2072	Silicon G	100
	SG2073	Silicon G	
	SG2074	Silicon G	
	SG2075	Silicon G	
	SG2076	Silicon G	
	SG2077	Silicon G	
	UDN-2841B	**Sprague (2843)**	
	UDN-2842B	**Sprague (2843)**	
	UDN-2843B	**Sprague (2843)**	
	UDN-2844B	**Sprague (2843)**	
	UDN-2845B	**Sprague (2843)**	110
	UDN-2846B	**Sprague (2843)**	
	ULN-2064B	**Sprague (2843)**	
	ULN-2065B	**Sprague (2843)**	
	ULN-2066B	**Sprague (2843)**	
	ULN-2067B	**Sprague (2843)**	
	ULN-2068B	**Sprague (2843)**	
	ULN-2069B	**Sprague (2843)**	
	ULN-2070B	**Sprague (2843)**	
	ULN-2071B	**Sprague (2843)**	
	ULN-2074B	**Sprague (2843)**	120
	ULN-2075B	**Sprague (2843)**	
	ULN-2076B	**Sprague (2843)**	
	ULN-2077B	**Sprague (2843)**	
	UDN2841	TI	

(Continued)

Function	Device	Source	Line
Quad Darlington Switch			
			(Cont'd)
	UDN2845	TI	
	ULN2064	TI	
	ULN2065	TI	
Hex NPN Darlington			
	LB1274	Sanyo	
One Darlington PNP Pair, and One Current Mirror Pair with Shared Diode, and Two PNP Transistors			
	CA3084	RCA	
Three Differential Amplifiers (NPN)			
	ULN-2047A	Sprague	130
Three NPN and two PNP Transistors			
	CA3096	† RCA	
	CA3096A	† RCA	
	CA3096C	† RCA	
Four High Current NPN Transistors (core driver)			
	FQ3724	Fairchild	
	FQ3725	Fairchild	
	MHQ4001A	Motorola	
	MHQ4002A	Motorola	
	MHQ4013	Motorola	
	MHQ4014	Motorola	
	MPQ3303	Motorola	140
	MPQ3725	Motorola	
	MPQ3725A	Motorola	
	MPQ4003	Motorola	
	MPQ4004	Motorola	
	DH3725C	National	
	DH6376C	National	
	CA1724G	† RCA	
	CA1725G	† RCA	
	CA3138	† RCA	
	CA3138A	† RCA	150
	TPQ3724	Sprague	
	TPQ3725	Sprague	
	TPQ3725A	Sprague	
Four High Current PNP Transistors (core driver)			
	FQ3467	Fairchild	
	FQ3468	Fairchild	
	MHQ3467	Motorola	
	DH3467C	National	
Five High Current NPN Transistors			
	SL3083	† Plessey	
	SL3183	† Plessey	
	CA3083	† RCA	160
	CA3183	† RCA	
	CA3183	† Signetics	
	SG3083	† Silicon G	
	SG3183	† Silicon G	
	SG3183A	† Silicon G	
	ULN-2083A	Sprague	
	ULS-2083H	† Sprague	
Five High Frequency NPN Transistors, (f4t>s GHz)			
	SL3127	Plessey	
	CA3127	RCA	
	CA3227	**RCA (3369)**	170
	CA3246	**RCA (3369)**	
Five High Voltage, High Current NPN Darlington Amplifiers			
	LB1287	Sanyo	
	LB1288	Sanyo	
Five High Voltage, High Current NPN Darlington Amplifiers, Source, for Load Connected to Negative Supply	**UDN-2956A**	**Sprague (2843)**	
	UDN-2957A	**Sprague (2843)**	
Five Low-Noise NPN Transistors			
	TDA3310	SGS	
Six NPN Darlingtons			
	LB1272	Sanyo	
	LB1273R	Sanyo	

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Arrays (Cont'd)

Transistor Arrays (Cont'd)

Function	Device	Source		Line
Seven High Current Darlingtons				
	ULN-2031A	Sprague		
	ULN-2032A	Sprague		
	ULN-2033A	Sprague		
Seven High Current, High Voltage, NPN Darlington Amplifiers, Open Collector, to 100 V, 500 mA				
	SN75465	TI		
	SN75468	TI		
	SN75469	TI		
Seven High Current, High Voltage, NPN Darlington Amplifiers, Open Collector, to 50 V, 500 mA				
	XR2001C	**Exar**	**(3199)**	
	XR2002C	**Exar**	**(3199)**	
	XR2003C	**Exar**	**(3199)**	
	XR2004C	**Exar**	**(3199)**	10
	XR2011C	**Exar**	**(3199)**	
	XR2012C	**Exar**	**(3199)**	
	XR2013C	**Exar**	**(3199)**	
	XR2014C	**Exar**	**(3199)**	
	XR2201	**Exar**	**(3200)**	
	XR2201M	**† Exar**	**(3200)**	
	XR2202	**Exar**	**(3200)**	
	XR2202M	**† Exar**	**(3200)**	
	XR2203	**Exar**	**(3200)**	
	XR2203M	**† Exar**	**(3200)**	20
	XR2204	**Exar**	**(3200)**	
	XR2204M	**† Exar**	**(3200)**	
	9665	Fairchild		
	9666	Fairchild		
	9666M	† Fairchild		
	9667	Fairchild		
	9667M	† Fairchild		
	9668	Fairchild		
	9668M	† Fairchild		
	MC1411	**Motorola**	**(2753)**	30
	MC1412	**Motorola**	**(2753)**	
	MC1413	**Motorola**	**(2753)**	
	MC1416	**Motorola**	**(2753)**	
	PBD352301	RIFA		
	PBD352302	RIFA		
	PBD352303	RIFA		
	RBD352301	RIFA		
	RBD352302	RIFA		
	RBD352303	RIFA		
	L201	SGS		40
	L202	SGS		
	L203	SGS		
	L204	SGS		
	ULN2001	Signetics		
	ULN2003	Signetics		
	ULN2004	Signetics		
	SG2001	Silicon G		
	SG2002	Silicon G		
	SG2003	Silicon G		
	SG3851	Silicon G		50
	SG3852	Silicon G		
	SG3853	Silicon G		
	ULN-2001A	**Sprague**	**(2843)**	
	ULN-2002A	**Sprague**	**(2843)**	
	ULN-2003A	**Sprague**	**(2843)**	
	ULN-2004A	**Sprague**	**(2843)**	
	ULN-2005A	**Sprague**	**(2843)**	
	ULS-2001H	† Sprague		
	ULS-2002H	† Sprague		
	ULS-2003H	† Sprague		60
	ULS-2004H	† Sprague		
	ULS-2005H	† Sprague		
	SN75466	TI		
	SN75467	TI		
	ULN2001A	TI		
	ULN2002A	TI		

(Continued)

Function	Device	Source		Line
Seven High Current, High Voltage, NPN Darlington Amplifiers, Open Collector, to 50 V, 500 mA				(Cont'd)
	ULN2003A	TI		
	ULN2004A	TI		
	ULN2005A	TI		
Seven High Current, High Voltage NPN Darlington Amplifiers, Open Collector, to 50 V, 600 mA				
	ULN-2011A	**Sprague**	**(2843)**	70
	ULN-2012A	**Sprague**	**(2843)**	
	ULN-2013A	**Sprague**	**(2843)**	
	ULN-2014A	**Sprague**	**(2843)**	
	ULN-2015A	**Sprague**	**(2843)**	
	ULS-2011H	† Sprague		
	ULS-2012H	† Sprague		
	ULS-2013H	† Sprague		
	ULS-2014H	† Sprague		
	ULS-2015H	† Sprague		
Seven High Current, High Voltage NPN Darlington Amplifiers, Open Collector, to 95 V, 500 mA				
	ULN-2021A	**Sprague**	**(2843)**	80
	ULN-2022A	**Sprague**	**(2843)**	
	ULN-2023A	**Sprague**	**(2843)**	
	ULN-2024A	**Sprague**	**(2843)**	
	ULN-2025A	**Sprague**	**(2843)**	
	ULS-2021H	† Sprague		
	ULS-2022H	† Sprague		
	ULS-2023H	† Sprague		
	ULS-2024H	† Sprague		
	ULS-2025H	† Sprague		
Seven High Current NPN Transistors, Common Collector				
	SL3082	Plessey		90
	CA3082	† RCA		
	CA3082	Signetics		
	SG3082	Silicon G		
	ULN-2082A	Sprague		
Seven NPN Darlingtons				
	LB1275	Sanyo		
Seven NPN Transistors, Common Emitter				
	SL3081	Plessey		
	CA3081	† RCA		
	CA3081	Signetics		
	SG3081	Silicon G		
	ULN-2081A	Sprague		100
Seven-Stage Driver Array				
	LB1260	Sanyo		
	LB1261	Sanyo		
	LB1264	Sanyo		
Eight High Current, High Voltage NPN Darlington Amplifiers, Current Source				
	UDN-2981A	**Sprague**	**(2843)**	
	UDN-2982A	**Sprague**	**(2843)**	
	UDN-2983A	**Sprague**	**(2843)**	
	UDN-2984A	**Sprague**	**(2843)**	
	UDS-2981H	† Sprague		
	UDS-2982H	† Sprague		
	UDS-2983H	† Sprague		110
	UDS-2984H	† Sprague		
Eight High Current, High Voltage NPN Darlington Amplifiers, Open Collector, to 50 V, 500 mA				
	ULN-2801A	**Sprague**	**(2843)**	
	ULN-2802A	**Sprague**	**(2843)**	
	ULN-2803A	**Sprague**	**(2843)**	
	ULN-2804A	**Sprague**	**(2843)**	
	ULN-2805A	**Sprague**	**(2843)**	
	ULS-2801H	† Sprague		
	ULS-2802H	† Sprague		
	ULS-2803H	† Sprague		
	ULS-2804H	† Sprague		120
	ULS-2805H	† Sprague		

Function	Device	Source		Line
Eight High Current, High Voltage NPN Darlington Amplifiers, Open Collector, to 50 V, 600 mA				
	ULN-2811A	**Sprague**	**(2843)**	
	ULN-2812A	**Sprague**	**(2843)**	
	ULN-2813A	**Sprague**	**(2843)**	
	ULN-2814A	**Sprague**	**(2843)**	
	ULN-2815A	**Sprague**	**(2843)**	
	ULS-2811A	Sprague		
	ULS-2811H	† Sprague		
	ULS-2812H	† Sprague		
	ULS-2813H	† Sprague		130
	ULS-2814H	† Sprague		
	ULS-2815H	† Sprague		
Eight High Current, High Voltage NPN Darlington Amplifiers, Open Collector, to 500 mA				
	L601	SGS		
	L602	SGS		
	L603	SGS		
	L604	SGS		
Eight High Current, High Voltage NPN Darlington Amplifiers, Open Collector, to 95 V, 500 mA				
	ULN-2821A	**Sprague**	**(2843)**	
	ULN-2822A	**Sprague**	**(2843)**	
	ULN-2823A	**Sprague**	**(2843)**	
	ULN-2824A	**Sprague**	**(2843)**	140
	ULN-2825A	**Sprague**	**(2843)**	
	ULS-2821H	† Sprague		
	ULS-2822H	† Sprague		
	ULS-2823H	† Sprague		
	ULS-2824H	† Sprague		
	ULS-2825H	† Sprague		

Special Arrays

CMOS (three p-channel and three n-channel enhancement MOS transistors tested for linear operation)			
	CA3600	† RCA	
Diode Array (one diode quad and two isolated)			
	CA3019	† RCA	
Diode Array (10 element)			
	CA3141	RCA	
Diode Array (16 element)			
	DN803	Panasonic	150
SCR Array (eight SCRs with current-limiting resistors)			
	UTN-2886B	**Sprague**	**(2843)**
	UTN-2888A	**Sprague**	**(2843)**
Thyristor/Transistor Array (SCR, programmable unjunction transistor, PNP/NPN transistor pair, NPN transistor and zener diode)			
	CA3097	† RCA	
Transistor/Diode Array (three NPN transistors two zener diodes and one diode)			
	CA3093	RCA	

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR-Comparators

Offset Voltage mV (25°C)	Bias Current (25°C)	Offset Current (25°C)	Response Time ns	Max. Differential Voltage	Gain	Fan Out	Supply Voltage, V	Device	Source	Line
Comparators-Single										
0.25	1.2 μA	80 nA	30	—	20K	—	5,−16	RC4805A	Raytheon	
								RM4805A	† Raytheon	
	1200 nA	80 nA	35 *	—	8000	—	5 to ±18	CMP-05A	† PMI	
								CMP-05E	PMI	
0.5 *	0.25 nA	0.1 nA	—	30	200K *	5	5, 0 to ±15	TL111	† TI	
0.6	1.8 μA	150 nA	30	—	20K	—	5,−16	RC4805	Raytheon	
								RM4805	† Raytheon	
	1800 nA	150 nA	35 *	—	7000	—	5 to ±18	CMP-05B	† PMI	
								CMP-05F	PMI	
0.7	0.1 μA	40 nA	200	—	200K	5	5	LF2111	† National	10
0.8	50 nA	3 nA	270	11	200K		5 to ±18	CMP-02	† PMI	
								CMP-02B	PMI	
								CMP-02E	PMI	
	600 nA	25 nA	180	11	200K		5 to ±18	CMP-01	† PMI	
								CMP-01B	PMI	
								CMP-01E	PMI	
1.0	6.0 μA	1.5 μA	45	15	—		±15,5	HA-4950	† Harris	
2.0	10 μA	1 μA	6.5	6			−5.2,6	685L	AMD	
								685M	† AMD	
			12	6		5	−6,5	686M	† AMD	20
	15 μA	3 μA	80	5	12.5K		−6,12	TL810M	† TI	
	20 μA	3 μA	40	5	40K *	10	−3 to -12,12	**LM106**	**† National (3317)**	
								LM206	**National (3317)**	
			40 *	5	1250	1	−6,12	μA710M	† Fairchild	
								MC1710	† Motorola	
								LM710	**† National (3317)**	
								SG710	† Silicon G	
								μA710M	† TI	
								SFC2710	† Thomson-CSF	
	45 μA	3 μA	40	5	40K	10	−3 to -12,12	LM106	† TI	30
								LM206	TI	
2.8	100 nA	15 nA	270	11	100K		5 to ±18	CMP-02C	PMI	
	900 nA	80 nA	180	11	200K		5 to ±18	CMP-01C	PMI	
3.0	5 μA	2 μA *	20	5	3K *	2	5,(−6, 5-±15)	**LM161**	**† National (3317)**	
								LM261	**National (3317)**	
	10 μA	1 μA	12	6			−6,5	686C	AMD	
	50 nA	10 nA	200	10	35K		±5 to ±18	μA734M	† Fairchild	
	100 nA	10 nA	165 *	30	200K *	5	5, 0 to ±15	LM111	† TI	
			200 *	30	200K *	5	5, 0 to ±15	AD111	† AD	
								AD211	AD	40
								μA111M	† Fairchild	
								LM111	† Intersil	
								LM111	† Motorola	
								LM211	Motorola	
								LM111	**† National (3317)**	
								LM211	**National (3317)**	
								LM111	† Raytheon	
								CA111	† RCA	
								CA211	RCA	
								LM111	† Signetics	50
								LM211	Signetics	
								SG111	† Silicon G	
								SG211	Silicon G	
								SFC2111	† Thomson-CSF	
								SFC2211	Thomson-CSF	
			250	30	200K *	5	5, 0 to ±15	LM111	† AMD	
								LM211	AMD	
		20 nA	250 *	15	15K		5-15, ±5-±15	ICL8001M	† Intersil	
3.5	20 μA	5 μA	80	5	10K		−6,12	TL810C	TI	

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Comparators (Cont'd)

Offset Voltage mV (25°C)	Bias Current (25°C)	Offset Current (25°C)	Response Time ns	Max. Differential Voltage	Gain	Fan Out	Supply Voltage, V	Device	Source	Line
Comparators-Single									**(Cont'd)**	
4.0	2 μA	0.5 μA	26	5	5K *		5,(−6, 5-± 10)	SE527	† Signetics	
	12 μA	3 μA	22	5	5K *		5,(−6, 5-± 10)	SE529	† Signetics	
	25 pA	50 pA	200	—	200K	2	36 *	**LF111**	**† National (3310,3317)**	
								LF211	**National (3310,3317)**	
	50 pA	25 pA	200 *	30	200K *	5	5, 0 to ± 15	LF111	† AMD	
								LF211	AMD	
5.0	6.0 μA	1.5 μA	55	15	—	—	± 15,5	HA-4955	Harris	
	10 μA	2 μA	20	5	3K *	2	(−6, 5 to ± 15)	**LM361**	**National (3317)**	
		5 μA	2.2	5	—	—	5,−5.2	**AD9685**	**AD (3157)**	
			2.7	5	—	—	5,−5.2	**AD9687**	**AD (3157)**	10
	20 μA	3 μA	14 *	5	3K *	4	± 5	**LM160**	**† National (3317)**	
								LM260	**National (3317)**	
								LM360	**National (3317)**	
	25 μA	5 μA	40	5	40K *	10	−3 to -12,12	**LM306**	**National (3317)**	
			40 *	5	1000	1	−6,12	μA710C	Fairchild	
								MC1710C	Motorola	
								LM710C	**National (3317)**	
								μPC71	NEC-Electron	
								SG710C	Silicon G	
	40 μA	5 μA	28 *	5	40K	10	−3 to -12,12	LM306	TI	20
	75 μA	10 μA	40 *	5	750		−6,12	TL710M	† TI	
	150 nA	25 nA	200 *	10	25K	2	± 5 to ± 15	μA734C	Fairchild	
			1300 *	36	200K *		2 to 36	TL331M	† TI	
		50 nA	1300 *	36	200K *		2 to 36	TL331C	TI	
	200 nA		50000	32	200K *		2	MK404	Analog Sys	
	250 nA	50 nA	250 *	15	15K		5-15, ±5-± 15	ICL8001C	Intersil	
6.0	2 μA	0.75 μA	26	5	5K *		5,(−6,5-± 10)	NE527	Signetics	
	20 μA	5 μA	22	5	5K *		5,(−6,5-± 10)	NE529	Signetics	
	60 μA	7.5 μA	25 *	5	5K *	2	± 4.5 to ± 6.5	μA760C	Fairchild	
								μA760M	† Fairchild	30
	250 nA	100 nA	250	10	15K		± 6 to ± 18	AD351J	AD	
								AD351K	AD	
								AD351S	† AD	
7.5	100 μA	15 μA	40 *	5	700		−6,12	TL710C	TI	
	250 nA	50 nA	200 *	30	200K *	5	5, 0 to ± 15	AD311	AD	
								μA311C	Fairchild	
								LM311	Intersil	
								LM311	Motorola	
								LM311	**National (3317)**	
								μPC271	NEC-Electron	40
								μPC311	NEC-Electron	
								LM311	Raytheon	
								CA311	RCA	
								LM311	Signetics	
								SG311	Silicon G	
								TL311M	**† TI (3426)**	
								SFC2311	Thomson-CSF	
	250 pA	50 pA	165 *	30	200K *	5	5, 0 to ± 15	LM211	TI	
								LM311	TI	
			250	30	200K *	5	5, 0 to ± 15	LM311	AMD	50
		100 pA	—	30	200K *	5	5, 0 to ± 15	**TL311A**	**TI (3426)**	
10	250 pA	100 pA	—	30	200K *	5	5, 0 to ± 15	**TL311**	**TI (3426)**	
10.0	75 pA	150 pA	200	—	200K	2	36 *	**LF311**	**National (3310,3317)**	
	150 pA	75 pA	200 *	30	200K *	5	5, 0 to ± 15	LF311	AMD	
20	500 nA	100 nA	1300 *	Vcc	2K	2	2 to 28	LM3302	TI	
20.0	50 μA	—	5	15	60 dB	—	5	**9050**	**OEI (3347)**	
30.0	50 μA	20 μA	55	5	100	6	5	**9915**	**OEI (3347)**	
Comparators-Dual										
2.0	10 μA	1 μA	8	6			−5.2, 5	687AM	† AMD	
			10	6			−5.2, 5	687M	† AMD	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Comparators (Cont'd)

Offset Voltage mV (25°C)	Bias Current (25°C)	Offset Current (25°C)	Response Time ns	Max. Differential Voltage	Gain	Fan Out	Supply Voltage, V	Device	Source	Line
Comparators-Dual									**(Cont'd)**	
2.0									(Cont'd)	
	15 μA	3 μA	80	5	12.5K		−6,12	TL514M	† TI	
								TL820M	† TI	
	20 μA	3 μA	30 *	5	1250	1	−6,12	**LM1514**	**† National (3317)**	
			40 *	5	1250		−6,12	MC1514	† Motorola	
	100 nA	25 nA	1300 *	36	50K		2 to 36	μA193A	† Fairchild	
								LM193A	**† National (3317)**	
								LM193A	† Signetics	
		250 nA	50 nA	1300 *	50K		2 to 36	μA293A	Fairchild	
								μA393A	Fairchild	
	250 nA	50 nA	1300 *	36	50K		2 to 36	**LM293A**	**National (3317)**	10
								LM393A	**National (3317)**	
3.0	10 μA	1 μA	8	6			−5.2, 5	687AL	AMD	
			10	6			−5.2, 5	687L	AMD	
	45 μA	7 μA	40	5	40K *	10	−3 to -12, 12	TL506M	† TI	
	100 nA	10 nA	200 *	30	200K *	5	5, 0 to ± 15	LH211	AMD	
								LH2111	† AMD	
								LH2211	AMD	
								LH2111	† Intersil	
								LH2111	**† National (3317)**	
								LH2211	**National (3317)**	20
								LH2111	Raytheon	
			250	30	200K *		5, 0 to ± 15	1500L	AMD	
								1500M	† AMD	
3.5	20 μA	3 μA	80	5	12.5K		−6, 12	TL811M	† TI	
		5 μA	80	5	10K		−6, 12	TL514C	TI	
								TL820C	TI	
	75 μA	10 μA	40 *	5	700	1	−6, 12	MC1711	† Motorola	
					750	1	−6, 12	μA711M	† Fairchild	
								LM711	**† National (3317)**	
			60	5	750	1	−6, 12	SG711	Silicon G	30
4.0	0.5 μA	75 nA	80	—	40K	2	± 15	LM119	† National	
	500 nA	75 nA	80 *	5	10K	2	5, 0 to ± 15	LM119	† AMD	
								LM219	AMD	
								LM119	**† National (3317)**	
								LM219	**National (3317)**	
								LM119	† Signetics	
								LM219	Signetics	
5.0	5 μA *	1 μA	2.7 *	30			−5.2,5	SP9685	Plessey	
								SP9687	Plessey	
	25 μA	5 μA	30 *	5	1000	1	−6,12	**LM1414**	**National (3317)**	40
			40 *	5	1000		−6,12	MC1414	Motorola	
	30 μA	5 μA	33 *	5	10K		−6,12	TL811C	TI	
	100 nA	25 nA	1300 *	36	50K		2 to 36	μA193	† Fairchild	
								LM193	**† National (3317)**	
								LM193	† Signetics	
								LM193	† TI	
	100 μA	15 μA	40 *	5	700	1	−6,12	μA711C	Fairchild	
								MC1711C	Motorola	
								LM711C	**National (3317)**	
								SG711C	Silicon G	50
								μA711C	TI	
								SFC2711	Thomson-CSF	
	250 nA	50 nA	1300 *	36	50K		2 to 36	μA293	Fairchild	
								μA393	Fairchild	
								LM293	**National (3317)**	
								LM393	**National (3317)**	
								LM293	Signetics	
								LM393A	Signetics	
								LM293	TI	
								LM393	TI	60
					200K *	2	2 to 36/± 1-± 18	μPC393	NEC-Electron	
	600 nA	150 nA	5000	30			4.5 to 20	μPC379	NEC-Electron	
6.0	30 pA	15 pA	200 *	36	50K	1	4 to 44	CA3290B	RCA	
6.5	40 pA	7.5 pA	28 *	5	40K *	10	−3 to -12, 12	TL506C	TI	

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Comparators (Cont'd)

Offset Voltage mV (25°C)	Bias Current (25°C)	Offset Current (25°C)	Response Time ns	Max. Differential Voltage	Gain	Fan Out	Supply Voltage, V	Device	Source	Line
Comparators-Dual									**(Cont'd)**	
7.0	250 nA	50 nA	1500 *	36	25K		2 to 36	μA2903	Fairchild	
								LM2903	**National (3317)**	
								LM2903	Signetics	
								LM2903	TI	
7.5	20 μA	5 μA	18	6	5K *	10	±5	NE521	Signetics	
								SE521	† Signetics	
			25	6	5K *	10	±5	NE522	Signetics	
								SE522	† Signetics	
	250 nA	50 nA	200 *	30	200K *	5	5, 0 to ± 15	LH2311	AMD	
								LH2311	Intersil	10
								LH2311	National	
			250	30	200K		5, 0 to ± 15	1500C	AMD	
8.0	1 μA	0.2 μA	80 *	5	8K	2	5, 0 to ± 15	LM319	AMD	
								LM319	**National (3317)**	
								μPC319	NEC-Electron	
								LM319	Signetics	
	250 nA	25 nA	600 *	40	—	1	4.5 to 40	MC3324A	Motorola	
								MC3424A	Motorola	
								MC3524A	Motorola	
10	40 pA	25 pA	200 *	36	50K	2	4 to 36	CA3290A	RCA	20
	100 nA	25 nA	300 *	38	—	1	4.5 to 40	MC3524	† Motorola	
	250 nA	50 nA	300 *	38	—	1	4.5 to 40	MC3324	Motorola	
								MC3424	Motorola	
20	50 pA	30 pA	200 *	36	25K	2	4 to 36	CA3290	RCA	
30	50 pA	100 pA	240	13	20K	1	± 1.5 to ±7.5	MC14575	Motorola	
			250	13	20K	1	± 1.5 to ±7.5	MC14575	Motorola	
Comparators-Quad										
0.8	100 nA	25 nA	1300	36	50K	2	2-36/± 1-± 18	CMP-04B	† PMI	
								CMP-04F	PMI	
2.0	100 nA	25 nA	1300 *	36	50K	2	2-36/± 1-± 18	LM139A	† AMD	
								μA139A	† Fairchild	30
								LM139A	† Intersil	
								LM139A	† Motorola	
								LM139A	**† National (3317)**	
								PM139A	† PMI	
								CA139A	† RCA	
								SG139A	† Silicon G	
								LM139A	† TI	
	250 nA	50 nA	1300 *	36	50K	2	2-36/± 1-± 18	LM239A	AMD	
								LM339A	AMD	
								μA239A	Fairchild	40
								μA339A	Fairchild	
								LM339A	Intersil	
								LM239A	Motorola	
								LM339A	Motorola	
								LM239A	**National (3317)**	
								LM339A	**National (3317)**	
								PM239A	PMI	
								PM339A	PMI	
								CA239A	RCA	
								CA339A	RCA	50
								SG239A	Silicon G	
								SG339A	Silicon G	
2.0 *	20 μA	1 μA *	55	5	1.2K *	10	±5	MC3430	Motorola	
								MC3431	Motorola	
			65	5	1.2K *	10	±5	MC3432	Motorola	
								MC3433	Motorola	
2.5	5 nA	0.5 nA	10 ms	36	25K		2 to 36	L161	Siliconix	
3.0	6 μA	1.5 μA	35 *	6	25k *	—	± 15,5	HA-4920	† Harris	
	75 nA	25 nA	130 *	15	400K *		5 to ± 15	**HA-4900-2**	**† Harris (3284,3287)**	
5.0	100 nA	25 nA	1300 *	36	200K *	2	2-36/± 1, ± 18	LM139	† AMD	60
								μA139	† Fairchild	
								LM139	† Intersil	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Comparators (Cont'd)

Offset Voltage mV (25°C)	Bias Current (25°C)	Offset Current (25°C)	Response Time ns	Max. Differential Voltage	Gain	Fan Out	Supply Voltage, V	Device	Source	Line
Comparators-Quad									**(Cont'd)**	
5.0	100 nA	25 nA	1300 *	36	200K *	2	2-36/±1,±18		(Cont'd)	
								LM139	† Motorola	
								LM139	**† National (3317)**	
								PM139	† PMI	
								LM139	† Raytheon	
								CA139	† RCA	
								LM139A	† Signetics	
								SG139	† Silicon G	
								LM139	† TI	
	150 nA	35 nA	200	15	400K *	—	5 to ±15	**HA-4902-2**	**† Harris (3284,3287)**	
	250 nA	50 nA	1300 *	15	200K *	1	3-15	MM54C909	† National	10
								MM74C909	National	
				36	200K *	2	2-36/±1,±18	LM239	AMD	
								LM339	AMD	
								μA239	Fairchild	
								μA339	Fairchild	
								LM339	Intersil	
								LM239	Motorola	
								LM339	Motorola	
								LM239	**National (3317)**	
								LM339	**National (3317)**	20
								μPC177	NEC-Electron	
								μPC339	NEC-Electron	
								AN6912	Panasonic	
								PM239	PMI	
								PM339	PMI	
								LM239	Raytheon	
								LM339	Raytheon	
								CA239	RCA	
								CA339	RCA	
								LM239A	Signetics	30
								LM339	Signetics	
								SG239	Silicon G	
								SG339	Silicon G	
								LM239	TI	
								LM339	TI	
5.0 (2 operational amplifiers, 2 comparators)										
	500 nA	75 nA	1300 *	36	200K *		3-36	MC3505	† Motorola	
6.0	8 μA	2 μA	35 *	6	25k *	—	±15,5	HA-4925	Harris	
7.0	250 nA	50 nA	1300 *	36	50K	2	2-36/±1-±18	LM2901	Motorola	
								LM2901	National	
								μPC2901	NEC-Electron	40
								LM2901	Raytheon	
								LM2901	Signetics	
								LM2901	TI	
7.5	150 nA	50 nA	130 *	15	400K *		5 to ±15	**HA-4905-5**	**Harris (3284,3287)**	
9.0 (2 operational amplifiers, 2 comparators)										
	10	500 nA	1300 *	36			3-36	MC3405	Motorola	
20	500 nA	3 nA *	2000 *	Vcc	2K	1	2 to 28	MC3302	Motorola	
								RV3302	Raytheon	
								MC3302	Signetics	
								SG3302	Silicon G	
		100 nA	1300 *	Vcc	2K	2	5 to ±15	LM3302	National	50
30 (2 operational amplifiers, 2 comparators)										
	50 pA	100 pA	250	13	20K	1	±1.5 to ±7.5	MC14574	Motorola	
Comparators-Hex										
5	100 nA	25 nA	1300	±36	200K	4	2-36/±1-±18	TL336C	TI	
	250 nA	25 nA	1300	±36	200K	4	3-36/±1-±18	TL336M	† TI	

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LINEAR–Consumer Circuits

Audio Circuits

Function	Device	Source	Line
Amplifier and Preamplifier, Low Power			
	TCA210	Signetics	
Amplifier, Headphone			
	LA4170	Sanyo	
	LA4175	Sanyo	
	LA4177	Sanyo	
Amplifier, Hearing Aid			
	CS263	Cherry	
	TCA1003	ITT	
	TCA1004	ITT	
	MPS5003	Micro Pwr	
	MPS5004	Micro Pwr	
	MPS5053	Micro Pwr	10
	μPC12	NEC-Electron	
	OM200	Panasonic	
	OM200	Signetics	
Amplifier, Low Power			
	TBA915	Signetics	
Amplifier, with AGC, for Recorders			
	HA1319	Hitachi	
	HA1361	Hitachi	
	TDA2054	Signetics	
	TDA7137	Toshiba	
	TDA7137-ST	Toshiba	
Attenuator, Digital			
	AD7115K	**AD (3163)**	20
Attenuator, Digital (logarithmic D/A converter)			
	AD7111K	**AD (3166)**	
	AD7111L	**AD (3166)**	
	AD7111T	**† AD (3166)**	
	AD7111U	**† AD (3166)**	
	AD7118T	**† AD (3166)**	
	AD7118U	**† AD (3166)**	
Attenuator, Digital (with loudness compensation switch), 0 to 88.5 dB Attenuation in 1.5 dB Steps			
	AD7110K	**AD (3166)**	
	AD7118K	**AD (3166)**	
	AD7118L	**AD (3166)**	
Attenuator, Dual			
	LA2600	Sanyo	30
	LC7500	Sanyo	
Audio Noise Reduction, Compander. See Linear-Telecommunications Circuits			
Controls (loudness, treble, bass)			
	TDA4290	Siemens	
Controls, Stereo, DC Operated			
	LM1035	**National (3326)**	
	TCA730A	Signetics	
	TCA740A	Signetics	
	TDA1074	Signetics	
	TDA1524	Signetics	
Digital Compact Disc			
	SAA7000	Signetics	
	SAA7010	Signetics	40
	SAA7020	Signetics	
Digital Noise Source			
	MM5437	National	
Equalizer, Switchable			
	TDA2000	Siemens	
Muting Circuit (switching noise suppressor)			
	TA7324	Toshiba	
Noise reduction, DNR			
	LM832	National	
Noise Reduction, Dolby			
	HA11226	Hitachi	
	LM1111	**National (3326,3328)**	
	LM1121A	**National (3326)**	
	LM1121B	**National (3326)**	

(Continued)

Function	Device	Source	Line
Noise Reduction, Dolby			
		(Cont'd)	
	LM1121C	**National (3326)**	50
	LM1131A	**National (3326)**	
	LM1131B	**National (3326)**	
	LM1131C	**National (3326)**	
	LM1894	**National (3326)**	
	NE545B	Signetics	
	NE645	Signetics	
	NE646	Signetics	
	NE648	Signetics	
	NE649	Signetics	
	NE650	Signetics	60
Pop Noise Canceller			
	AN6135	Panasonic	
Power Amplifier Controller			
	AN7071	Panasonic	
Power Amplifier Driver			
	ICL8063C	Intersil	
	ICL8063M	† Intersil	
	MC3221	Motorola	
	MC3320	Motorola	
	MC3321	Motorola	
	LM391	**National (3326,3328)**	
	AN7070	Panasonic	
	NE540	Signetics	70
	SE540	Signetics	
Power Amplifier Driver, Dual			
	STK3042	Sanyo	
	STK3062	Sanyo	
	STK3082	Sanyo	
Power Amplifier, Single, <5 Watts			
	CA3094	† RCA	
	TBA641	Fairchild	
	TBA820	Fairchild	
	HA1325	Hitachi	
	HA1329	Hitachi	
	MC1306	Motorola	80
	MC1384	Motorola	
	MC1454	Motorola	
	MC1554	† Motorola	
	MC3360	Motorola	
	LM1879	National	
	LM2001	National	
	LM2895	**National (3326)**	
	LM380	**National (3326)**	
	LM386	**National (3326,3328)**	
	LM388	**National (3326,3328)**	90
	LM389	National	
	LM390	**National (3326,3328)**	
	μPC1025	NEC-Electron	
	μPC41	NEC-Electron	
	AN124	Panasonic	
	AN214	Panasonic	
	AN252	Panasonic	
	AN374	Panasonic	
	AN7110	Panasonic	
	AN7114	Panasonic	100
	AN7115	Panasonic	
	AN7120	Panasonic	
	AN7130	Panasonic	
	CA3020	† RCA	
	LA4100	Sanyo	
	LA4101	Sanyo	
	LA4102	Sanyo	
	LA4110	Sanyo	
	LA4112	Sanyo	
	LA4126	Sanyo	110
	LA4137	Sanyo	

(Continued)

Function	Device	Source	Line
Power Amplifier, Single, <5 Watts			
		(Cont'd)	
	LA4138	Sanyo	
	LA4180	Sanyo	
	LA4182	Sanyo	
	LA4200	Sanyo	
	LA4201	Sanyo	
	LA4220	Sanyo	
	LA4430	Sanyo	
	TBA820	SGS	
	TBA820M	SGS	120
	TCA830S	SGS	
	TDA1012	Signetics	
	TDA1013	Signetics	
	ULN-2280B	Sprague	
	ULN-2283B	Sprague	
	ULN-3705M	Sprague	
	TCA830	Telefunken	
	U410	Telefunken	
	U411	Telefunken	
	LM388	TI	130
	SN16923	TI	
	SN76000	TI	
	SN76002	TI	
	SN76011	TI	
	SN76021	TI	
	SN76024	TI	
	TA7140	Toshiba	
	TA7207	Toshiba	
	TA7208	Toshiba	
Power Amplifier, Single, > 10 Watts			
	μA7332	Fairchild	140
	HA1388	Hitachi	
	HA1392	Hitachi	
	LM1875	**National (3330)**	
	CA2004	RCA	
	SI1020	Sanken	
	SI1030	Sanken	
	SI1050	Sanken	
	LA4460	Sanyo	
	LA4461	Sanyo	
	STK0030	Sanyo	150
	STK0040	Sanyo	
	STK0050	Sanyo	
	STK0055	Sanyo	
	STK0059	Sanyo	
	STK0060	Sanyo	
	STK0070	Sanyo	
	STK0080	Sanyo	
	STK0150	Sanyo	
	STK050	Sanyo	
	STK058	Sanyo	160
	STK070	Sanyo	
	STK075	Sanyo	
	STK077	Sanyo	
	STK078	Sanyo	
	STK080	Sanyo	
	STK082	Sanyo	
	STK083	Sanyo	
	STK084	Sanyo	
	STK086	Sanyo	
	STK4021	Sanyo	170
	STK4023	Sanyo	
	STK4025	Sanyo	
	STK4372	Sanyo	
	STK4392	Sanyo	
	TCA940	SGS	
	TDA2008	SGS	
	TDA2010	SGS	
	TDA2020	SGS	
	TDA2020D	SGS	
	TDA2030	SGS	180
	TDA2040	SGS	

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† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Consumer Circuits (Cont'd)

Audio Circuits (Cont'd)

Function	Device	Source	Line
Power Amplifier, Single, > 10 Watts (Cont'd)			
	TDA2030	Siemens	
	TDA3000	Siemens	
	TDA1512	Signetics	
	TDA1520	Signetics	
	TDA2030	Telefunken	
	ESM532	Thomson-CSF	
	TA7210	Toshiba	
Power Amplifier, Single, 5-10 Watts			
	HA1366	Hitachi	
	HA1368	Hitachi	
	HA1371	Hitachi	10
	HA1372	Hitachi	
	HA1389	Hitachi	
	TBA800	Hitachi	
	TBA810	Hitachi	
	TDA2002	Hitachi	
	TDA2002	Motorola	
	TDA2002A	Motorola	
	LM2002	**National (3326)**	
	LM383	**National (3326)**	
	LM383A	**National (3326)**	20
	LM384	**National (3326,3328)**	
	TDA2002	National	
	TDA2002A	National	
	µPC1020	NEC-Electron	
	µPC1155	NEC-Electron	
	µPC1156	NEC-Electron	
	µPC571	NEC-Electron	
	µPC578	NEC-Electron	
	AN272	Panasonic	
	AN315	Panasonic	30
	AN7150	Panasonic	
	AN7151	Panasonic	
	AN7152	Panasonic	
	AN7154	Panasonic	
	AN7155	Panasonic	
	CA2002	RCA	
	CA3131	RCA	
	CA3132	RCA	
	CA810	RCA	
	CA810A	RCA	40
	CA810AM	RCA	
	CA810M	RCA	
	SI1010	Sanken	
	LA4140	Sanyo	
	LA4230	Sanyo	
	LA4250	Sanyo	
	LA4420	Sanyo	
	LA4422	Sanyo	
	LA4440	Sanyo	
	STK4017	Sanyo	50
	STK4019	Sanyo	
	STK4332	Sanyo	
	STK4352	Sanyo	
	STK4362	Sanyo	
	L149	SGS	
	TBA800	SGS	
	TBA810	SGS	
	TCA940E	SGS	
	TDA1905	SGS	
	TDA1908	SGS	60
	TDA1910	SGS	
	TDA2002	SGS	
	TDA2002A	SGS	
	TDA2003	SGS	
	TDA2006	SGS	
	TDA1037	Siemens	
	TDA2003	Siemens	

(Continued)

Function	Device	Source	Line
Power Amplifier, Single, 5-10 Watts (Cont'd)			
	TDA1010A	Signetics	
	TDA1011	Signetics	
	TDA1011A	Signetics	70
	TDA1020	Signetics	
	TDA2611A	Signetics	
	TDA2002	Sprague	
	TDA2002A	Sprague	
	ULN-3701Z	Sprague	
	ULN-3702Z	Sprague	
	ULN-3703Z	Sprague	
	ULN-3784B	Sprague	
	ULX-3704B	Sprague	
	TBA800	Telefunken	80
	TBA810	Telefunken	
	TDA2002	Telefunken	
	TDA2002A	Telefunken	
	TDA2003	Telefunken	
	TDA2004	Telefunken	
	SN76005	TI	
	TA7205A	Toshiba	
	TA7217A	Toshiba	
	TA7222A	Toshiba	
	TA7238	Toshiba	90
Power Amplifier, Dual, <5 Watts			
	HA1374	Hitachi	
	LM1877	**National (3326,3328)**	
	LM1895	**National (3326)**	
	LM1896	**National (3326,3328)**	
	LM2877	**National (3326,3328)**	
	LM2896	**National (3326,3328)**	
	LM377	National	
	LM378	**National (3326)**	
	AN313	Panasonic	
	AN7145L	Panasonic	100
	AN7146M	Panasonic	
	LA4120	Sanyo	
	LA4125	Sanyo	
	LA4125T	Sanyo	
	ULX-3783M	Sprague	
	TA7203	Toshiba	
	TA7214	Toshiba	
	TA7215	Toshiba	
Power Amplifier, Dual, 5-10 Watts			
	HA1377	Hitachi	
	LM2878	**National (3326)**	110
	LM2879	National	
	LM379	**National (3326)**	
	AN7145M	Panasonic	
	AN7156	Panasonic	
	STK433	Sanyo	
	STK435	Sanyo	
	STK443	Sanyo	
	STK457	Sanyo	
	STK459	Sanyo	
	STK463	Sanyo	120
	STK465	Sanyo	
	TDA2004	SGS	
	TDA2005	SGS	
	TDA1510	Signetics	
	TDA1515	Signetics	
	ULX-3777W	Sprague	
	TDA2005	Telefunken	
	TA7227	Toshiba	
Power Amplifier, Dual, > 10 Watts			
	AN7145H	Panasonic	
	AN7146H	Panasonic	130
	AN7156N	Panasonic	

(Continued)

Function	Device	Source	Line
Power Amplifier, Dual, > 10 Watts (Cont'd)			
	STK437	Sanyo	
	STK439	Sanyo	
	STK441	Sanyo	
Preamplifier	CA3080	RCA	
	CA3080A	† RCA	
	MA106	Analog Sys	
	ZN459	† Ferranti	
	ZN459C	Ferranti	
	ZN459CP	Ferranti	140
	ZN460	† Ferranti	
	ZN460C	Ferranti	
	ZN460CP	Ferranti	
	HA12017	Hitachi	
	HA1406	Hitachi	
	HA1457	Hitachi	
	LM1837	**National (3325,3327)**	
	LM3080	National	
	LM3080A	National	
	µPC1023	NEC-Electron	150
	µPC1024	NEC-Electron	
	µPC1032	NEC-Electron	
	µPC566	NEC-Electron	
	µPC573	NEC-Electron	
	µPC592	NEC-Electron	
	AN127	Panasonic	
	AN360	Panasonic	
	AN370	Panasonic	
	SL561	Plessey	
	SL561B	Plessey	160
	SL561C	Plessey	
	LA3110	Sanyo	
	LA3120	Sanyo	
	LA3130	Sanyo	
	LA3150	Sanyo	
	LA3170	Sanyo	
	TDA2310	SGS	
	TDA3410	SGS	
	TDA3420	SGS	
	TAA263	Signetics	170
	TAA310A	Signetics	
	TA7063	Toshiba	
	TA7120	Toshiba	
	TA7122A	Toshiba	
	TA7122B	Toshiba	
	TA7129	Toshiba	
	TA7129A	Toshiba	
	TA7136A	Toshiba	
	TA7322	Toshiba	
Preamplifier for IR Remote Control			
	TDA2320	SGS	180
Preamplifier, Dual			
	XR4739	Exar	
	XR4739M	† Exar	
	UA739	Fairchild	
	µA739	Fairchild	
	µA749	† Fairchild	
	HA12012	Hitachi	
	HA1452W	Hitachi	
	LM1301	National	
	LM1303	**National (3325)**	
	LM1897	**National (3325,3327)**	190
	LM381	**National (3325,3328)**	
	LM382	**National (3325,3327)**	
	LM387	**National (3325,3327)**	
	AN264	Panasonic	
	AN7311	Panasonic	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Consumer Circuits (Cont'd)

Audio Circuits (Cont'd)

Function	Device	Source	Line
Preamplifier, Dual (Cont'd)			
	LA3115	Sanyo	
	LA3122	Sanyo	
	LA3133	Sanyo	
	LA3155	Sanyo	
	LA3160	Sanyo	
	LA3161	Sanyo	
	TDA2320A	SGS	
	LM381A	Signetics	
	LM387	Signetics	
	NE542	**Signetics (3393)**	10
	TDA1522	Signetics	
	ULN-2231A	Sprague	
	SN76130	TI	
	SN76131	TI	
	SN76149	TI	
	TA7312	Toshiba	
	TA7325	Toshiba	
	TA7685	Toshiba	
Preamplifier, Quad			
	XR4212	Exar	
Signal Delay	MN3001	Panasonic	20
	MN3010	Panasonic	
	MN3204	Panasonic	
	MN3207	Panasonic	
	TDA1096	Signetics	
	TDA2104	Signetics	
	TDA2105	Signetics	
	TDA2107	Signetics	
	TDA2108	Signetics	
Sound Generator			
	AY3-8910	GI	
	AY3-8912	GI	30
Sound Generator Controller for Microprocessor-Based Systems	SN76489	TI	
	SN76489A	TI	
	SN76493	TI	
	SN76494	TI	
	SN76495	TI	
Sound Generator w/Audio Amp			
	SN76487	TI	
	SN76488	TI	

Automotive Circuits

Function	Device	Source	Line
Clock	PCF1171	Signetics	
	PCF1172	Signetics	
Clock with Vacuum Fluorescent Display Drivers			
	S4003	AMI	40
	SCL5233	SSS	
Ignition Circuit	MC3333	Motorola	
Lamp Monitor	ULN-2401A	Sprague	
Low Coolant Detector			
	ULN-2429A	Sprague	
Speed Control Processor			
	MC14460	Motorola	
Speedometer and Mileage Indicator			
	SAY115	ITT	
Traffic Information Broadcast Decoders			
	UAA1009	ITT	
	S0280	Siemens	
	S0281	Siemens	
	S551	Siemens	50
	S552	Siemens	
Voltage Regulator			
	TCA700	ITT	
	MC3325	Motorola	

Calculator Circuits

Function	Device	Source	Line
Calculator	μPD1201	NEC-Electron	
	μPD1801	NEC-Electron	
	μPD276	NEC-Electron	
	μPD277	NEC-Electron	
	μPD278	NEC-Electron	
	μPD284	NEC-Electron	
	μPD286	NEC-Electron	60
	μPD299	NEC-Electron	
	μPD940	NEC-Electron	
	μPD941	NEC-Electron	
	μPD943	NEC-Electron	
	μPD946	NEC-Electron	
	μPD947	NEC-Electron	
	μPD950	NEC-Electron	
	μPD951	NEC-Electron	
	μPD952	NEC-Electron	
	MN5530	Panasonic	70
	MN5540	Panasonic	
	MN5550	Panasonic	
	MN5556	Panasonic	
	MN5701	Panasonic	
	MN5710	Panasonic	
	MN5750	Panasonic	
	MN5752	Panasonic	
	TMS1018	**TI (1559)**	
Calculator, Printing			
	HD38510	Hitachi	
	HD38513	Hitachi	80
	HD38546	Hitachi	
	HD38550	Hitachi	
	HD38560	Hitachi	
	HD38570	Hitachi	
	HD38580	Hitachi	
	HD38585	Hitachi	

Camera Circuits

Function	Device	Source	Line
Exposure Control			
	CS100	Cherry	
	CS102	Cherry	
	CS122	Cherry	
	CS127	Cherry	90
	CS129	Cherry	
	CS130	Cherry	
	CS131	Cherry	
	CS132	Cherry	
	CS137	Cherry	
	CS460	Cherry	
	CS461	Cherry	
	CS462	Cherry	
	CS463	Cherry	
	CS464	Cherry	100
	CS470	Cherry	
	CS480	Cherry	
	CS481	Cherry	
	CS482	Cherry	
	CS483	Cherry	
	CS484	Cherry	
	CS485	Cherry	
	CS486	Cherry	
	CS487	Cherry	
	CS488	Cherry	110
	CS489	Cherry	
	CS580	Cherry	
	μPC558	NEC-Electron	
	μPC589	NEC-Electron	
	S0258A	Siemens	
	S0289	Siemens	
Strobe Light Controller			
	CS139	Cherry	

CB Radio Circuits

Function	Device	Source	Line
AF Processing Circuit			
	AN6140	Panasonic	
Channel Selector/Display Driver			
	FCB8010	Fairchild	
	MN6080	Panasonic	120
	LC7181	Sanyo	
	LC7184	Sanyo	
	LC7191	Sanyo	
Programmer, for PLL			
	MP7156	Micro Pwr	
	LC7120	Sanyo	
Synthesizer Set, 40 Channel, BCD Channel Setting			
	MP7139	Micro Pwr	
	MP7149	Micro Pwr	
	MP7189	Micro Pwr	
Synthesizer Set, 40 Channel, Binary Channel Setting			
	SP8923	Plessey	
Synthesizer Set, 40 Channel, BCD Channel Setting			
	SP8921	Plessey	130
	SP8923	Plessey	
	LC7131	Sanyo	
	LC7135	Sanyo	
Synthesizer Set, 40 Channel, Binary Channel Setting			
	SP8922	Plessey	
Transceiver Receiver			
	TMS1022	TI	

Clock/Watch Circuits

Function	Device	Source	Line
Alarm Clock	HD38980	Hitachi	
	HD38991C	Hitachi	
	HD43115	Hitachi	
	HD43890	Hitachi	
	ICM1115	Intersil	140
	ICM1115A	Intersil	
	ICM1115B	Intersil	
	ICM7038A	Intersil	
	ICM7038B	Intersil	
	ICM7049A	Intersil	
	ICM7050	Intersil	
	MM53108	National	
	MM5316	**National (3327)**	
	MM5387	**National (3327)**	
	MM5402	**National (3327)**	150
	MM5405	National	
	MM58143	**National (3327)**	
	MM58144	National	
	μPD5388	NEC-Electron	
	μPD832	NEC-Electron	
	μPD833	NEC-Electron	
	MSM5550	**OKI (3873)**	
	MN6052	Panasonic	
	MN6053	Panasonic	
	MN6054	Panasonic	160
	MN6056	Panasonic	
	MN6075	Panasonic	
	MN6076	Panasonic	
	MN6091	Panasonic	
	MN6092	Panasonic	
	LM8360	Sanyo	
	LM8361	Sanyo	
	MB561	Signetics	
	MB562	Signetics	
	PCA1515	Signetics	170
	PCA1517	Signetics	
	PCA1564	Signetics	
	PCA1566	Signetics	
	TCA1516	Signetics	

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Consumer Circuits (Cont'd)

Clock/Watch Circuits (Cont'd)

Function	Device	Source		Line
Alarm Clock Radio				
	CK3300	GI		
	ICM7223	Intersil		
	ICM7223A	Intersil		
	ICM7223VF	Intersil		
	MM53113	National		
	MM53124	National		
	MM5455	National		
	MM5456	**National**	**(3327)**	
	MM5457	**National**	**(3327)**	
	MM5462	National		10
	MM5463	National		
	MM5464	**National**	**(3327)**	
	MM5465	National		
	MM5466	**National**	**(735)**	
	MSM5523	OKI		
	MSM5524	**OKI**	**(3873)**	
	MSM5549	OKI		
	MSM5550	OKI		
	LM8363	Sanyo		
	LM8364	Sanyo		20
Automotive Clock with LCD Display Drivers				
	PCF1171	Signetics		
	PCF1172	Signetics		
Clock Automotive, with Vacuum Fluorescent Display Drivers	**MSM5557**	**OKI**	**(3873)**	
	SCL5458	SSS		
Clock Circuits (See Also: Digital—CMOS Oscillators/ Dividers. Linear—Clock, Alarm Clock, Clock, Alarm Clock Radio. Other Linear Devices—Oscillator)				
	S4003	**AMI**	**(618)**	
	8640	Epson		
	8650	Epson		
	8651	Epson		
	HD44010	Hitachi		
	ICM7051A	Intersil		30
	ICM7051B	Intersil		
	ICM7052	Intersil		
	SAJ300	ITT		
	C1200	LSI Comp		
	MM5309	National		
	MM5311	National		
	MM53110	National		
	MM5312	National		
	MM5313	National		
	MM5314	National		40
	MM5315	National		
	MM5318	National		
	MM5378	National		
	μPD811	NEC-Electron		
	μPD815	NEC-Electron		
	μPD816	NEC-Electron		
	MSA750	OKI		
	MSM5509	**OKI**	**(3873)**	
	MSM5528	**OKI**	**(3873)**	
	MSM5529	OKI		50
	MSM5558	**OKI**	**(3873)**	
	MSM5559	OKI		
	MN6052	Panasonic		
	MN6053	Panasonic		
	MN6057	Panasonic		
	MN6058	Panasonic		
	MN6059	Panasonic		
	MN6070	Panasonic		
	MN6093	Panasonic		
	MN6200	Panasonic		60
	MN6250	Panasonic		
	MN6251	Panasonic		
	MN6252	Panasonic		
	CD22012	RCA		
	CD22014	RCA		

(Continued)

Function	Device	Source	Line
Clock Circuits (See Also: Digital—CMOS Oscillators/ Dividers. Linear—Clock, Alarm Clock, Clock, Alarm Clock Radio. Other Linear Devices—Oscillator) (Cont'd)			
	MB512	Signetics	
	MB513	Signetics	
	SCL5233	SSS	
	SCL5238	SSS	
	SCL5455	SSS	70
	SCL5463	SSS	
	SCL5474	SSS	
	SCL5601	SSS	
Clock Circuits (See Also: Digital—CMOS Oscillators/ Dividers. Linear—Clock, Alarm Clock, Clock, Alarm Clock Radio, Other Linear Devices—Oscillator)			
	ICM7045	Intersil	
	WD2412	Western	
Color Bar Generator			
	MM5322	National	
Color Control for VIR Broadcasts			
	HA11409	Hitachi	
Digital Clock, Channel and Time Display			
	MM58106	National	
Digital Tuner	MM58142	National	
Melody Circuit, for Clocks			
	7910	Epson	80
	7920	Epson	
	7930	Epson	
	SVM7940	Epson	
	SVM7950	Epson	
	SVM7960	Epson	
	SVM7970	Epson	
	SVM7990	Epson	
Melody Circuit, Westminister Chime			
	SVM5530	Epson	
	SVM7810	Epson	
Stopwatch/Clock (LCD)			
	ICM7045	Intersil	90
	WD2412	Western	
Stopwatch (LED)			
	ICM7205	Intersil	
	ICM7215	Intersil	
Watch, Analog (See also Digital—CMOS Oscillators/ Dividers)	HC43850	Hitachi	
	ICM7047	Intersil	
	ICM7245	Intersil	
	μPD810	NEC-Electron	
	MB101	Signetics	
	MB105	Signetics	
	MB125	Signetics	100
	MB126	Signetics	
	MB140	Signetics	
	SCL5484	SSS	
Watch (LCD), Digital			
	HC42022	Hitachi	
	HC42030	Hitachi	
	HC43032	Hitachi	
	HC43802	Hitachi	
	HC43803	Hitachi	
	ICM1424B	Intersil	
	ICM1424MB	Intersil	110
	ICM1424MC	Intersil	
	ICM7210	Intersil	
	ICM7210C	Intersil	
	ICM7210M	Intersil	
	ICM7210MC	Intersil	
	ICM7220	Intersil	
	ICM7220B	Intersil	
	ICM7220M	Intersil	
	ICM7220MA	Intersil	
	ICM7220MC	Intersil	120
	ICM7269	Intersil	

(Continued)

Function	Device	Source	Line
Watch (LCD), Digital (Cont'd)			
	ICM7270	Intersil	
	ICM7272	Intersil	
	μPD809	NEC-Electron	
	μPD819	NEC-Electron	
	μPD826	NEC-Electron	
	μPD828	NEC-Electron	
	μPD844	NEC-Electron	
	MSM5080	OKI	
	MSM5517	OKI	130
	MSM5803	**OKI**	**(3873)**
	MSM5977	OKI	
	MS680	RTC	
	MS681	RTC	
	MS682	RTC	
	MS683	RTC	
	LC5621	Sanyo	
	MJ11-2	Signetics	
	MJ121	Signetics	
	MJ123	Signetics	140
	PCA1122	Signetics	
	PCA1126	Signetics	
	SCL54301	SSS	
	SCL5450	SSS	
	SCL5478	SSS	
	SCL5482	SSS	
	SCL5483	SSS	
Watch (LCD), Digital Chronograph			
	ICM7220C	Intersil	
	MP7160	Micro Pwr	
	MSM5515	OKI	150
	MSM5970	OKI	
	MSM5976	OKI	
	LC5613	Sanyo	
	SW-604	Supertex	
Watch (LCD), Digital Chronograph/Alarm			
	HI7000	Holt	
	MP7216	Micro Pwr	
	MSM5016	OKI	
	MSM5081	OKI	
Watch (LCD), Digital with Alarm			
	HI7020	Holt	
	ICM7220A	Intersil	160
	ICM7220FA	Intersil	
	ICM7220MFA	Intersil	
	ICM7221	Intersil	
	ICM7222	Intersil	
	MP7150	Micro Pwr	
	MSM5518	OKI	
	MSM5519	OKI	
	MSM5972	OKI	
	MJ150	Signetics	
	SCL5481	SSS	170
	SCL5485	SSS	
	SCL5486	SSS	
Watch (LCD), Digital with Alarm and Music Enable			
	ICM7271	Intersil	
	ICM7273	Intersil	
Watch (LCD), Digital with Musical Alarm			
	SCL5470	SSS	
	SCL5471	SSS	
	SCL5472	SSS	
Watch (LED), Digital			
	ICM7214	Intersil	
	ICM7214A	Intersil	
	μPD824	NEC-Electron	180
	μPD829	NEC-Electron	

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Consumer Circuits (Cont'd)

Organ Circuits

Function	Device	Source
Delay Circuit, See also Analog Shift Registers under Linear-Other Devices.		
	SAD1024A	Reticon
	SAD512	Reticon
	TDA1022	Signetics
Digital Accompaniment Interface		
	M109	SGS
Electronic Attenuator		
	CA3080	RCA
	CA3080A	† RCA
	XR13600	Exar
	MC3340	Motorola
Frequency Divider, 6-Stage		
	S10129	AMI
	S10130	AMI
	S10131	AMI
	LM3216	Sanyo
Frequency Divider, 6-Stage, with Gating, Five Outputs		
	TDA1008	Signetics
Frequency Divider, 7-Stage		
	MC1302	Motorola
	M738	SGS
	M740	SGS
	M741	SGS
	M747	SGS
	SAJ410	Siemens
Frequency Divider, 8-Stage, with Staircase Generator		
	MN6004	Panasonic
Frequency Generator. See also Organ, Top Octave Generator	MN6005	Panasonic
Key Divider	S10430	AMI
Monophonic Synthesizer		
	M110	SGS
Noise Generator		
	S2688	AMI
	MM5837	National
Rhythm Circuit	S2567	AMI
	LM8372	Sanyo
	LM8471	Sanyo
	LM8972	Sanyo
	M258	SGS
	M259	SGS
	M268	SGS
	M269	SGS
Solo and Accompaniment		
	M108	SGS
Tone Generator		
	M082	SGS
	M082AA	SGS
	M083	SGS
	M083AA	SGS
	M086	SGS
	M086AA	SGS
Top Octave Generator		
	S50240	AMI
	S50241	AMI
	S50242	AMI
	S50243	AMI
	S50244	AMI
	S50245	AMI
	MK50240	Mostek
	MK50241	Mostek
	MK50242	Mostek
	LM8071	Sanyo
Toy Organ	SAA1900	ITT
Single Chip	M208	SGS
Dual Voltage Controlled Amplifier		
	SSM2020	SSM
	SSM2022	SSM

Radio Circuits, AM

Function	Device	Source
AM/SW Tuner	5054	Siemens
Amplifier with Demodulator and Volume Control		
	TDA1048	Siemens
Frequency Synthesizer		
	TC9131	Toshiba
Mixer, IF, AGC	ULN-2243A	Sprague
Receiver System		
	HA1151	Hitachi
	HA1197	Hitachi
	HA1199	Hitachi
	HA1199	Motorola
	μPC1215V	NEC-Electron
	AN259	Panasonic
	CA3088	† RCA
	CA3123	† RCA
	TCA440	Siemens
	TDA1046	Siemens
	TCA440	Signetics
	TDA1072	Signetics
	TEA5550	Signetics
	ULN-2249A	Sprague
	ULN-3838A	Sprague
	TDA1072	Telefunken
	SN76635	TI
	TA7306	Toshiba
	TA7615	Toshiba
RF, IF Detector	**LM3820**	**National (3325,3327)**
RF, IF, Detector, AGC		
	ZN414	Ferranti
RF, Mixer, IF	μPC1021	NEC-Electron
	μPC30	NEC-Electron
SSB Detector	SL623C	Plessey
Stereo Decoder	LM1981	National
Stereo Demodulator		
	HS3604	Harris
Tuner for Car Radio		
	TA7402	Toshiba
	TA7616	Toshiba
Tuner System	LA1130	Sanyo
	LA1240	Sanyo
	LA1245	Sanyo

Radio Circuits, AM/FM

Function	Device	Source
AM/FM Phase and Signal Locked Loop (PSL²) Tuner		
	LC7210	Sanyo
AM/FM PLL Synthesizer Tuner		
	LC7220	Sanyo
	LC7225	Sanyo
AM/FM/SW Frequency Counter		
	MSM5527	OKI
Display Driver for Receiving Frequency Digital Display		
	TD6301A	Toshiba
FM/SW/MW/LW Frequency Display		
	LC7253	Sanyo
	LC7257	Sanyo
	LC7258	Sanyo
Frequency Counter		
	MSM5525	**OKI (3873)**
Frequency Counter, Up to 130 MHz		
	SDA5680	Siemens
IF Amplifier	μA757	Fairchild
	LM1821	National
	LM1868	**National (3325)**
	μPC27	NEC-Electron
	μPC577	NEC-Electron
	AN203	Panasonic
	AN210	Panasonic
	AN7218	Panasonic
	AN7266	Panasonic
	LA1201	Sanyo
	TAA991	Siemens
Radio Frequency Display		
	MM5430	National
	MM5431	National
Radio Frequency Display Driver and Clock		
	HA12404	Hitachi
	HA12405	Hitachi
	T1400	Toshiba
Receiver System		
	HA11211	Hitachi
	HA11251	Hitachi
	HA12402	Hitachi
	LM1866	**National (3325)**
	AN217P	Panasonic
	AN253	Panasonic
	AN260	Panasonic
	AN277	Panasonic
	AN366	Panasonic
	AN7000	Panasonic
	SL624C	Plessey
	LA1210	Sanyo
	TDA1220A	SGS
	TBA570A	Signetics
	TDA5700	Signetics
	TDA5701	Signetics
	TDA1083	Sprague
	TDA1090	Sprague
	ULN-2204A	Sprague
	ULN-2240A	Sprague
	ULN-2241A	Sprague
	ULN-2242A	Sprague
	ULX-3840A	Sprague
	TDA1083	Telefunken
	U416	Telefunken
	U417	Telefunken
	U418	Telefunken
	TA7613	Toshiba
	TA7614	Toshiba
Search Tuning	TDA 1580	Signetics
Signal Processor		
	ULX-3804A	Sprague
Synthesizer (FM prescaler, preamplifier and reference oscillator)	AC5945	TI
Tuner Control	LC7200	Sanyo
	LC7201	Sanyo
	LC7203	Sanyo
	LC7207	Sanyo
Tuner, Radio Frequency Display and Clock		
	LC7250	Sanyo
TV Synthesizer	SAA1057	Signetics

Radio Circuits, FM

Function	Device	Source
Controller, for Voltage Synthesis Systems		
	SDA5690	Siemens
Detector. See Linear-Phase Locked Loop Circuits and IF Amplifier/Detector below.		
Front End	AN7213	Panasonic
	TDA1571	Signetics
	TDA1574	Signetics

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Consumer Circuits (Cont'd)

Radio Circuits, FM (Cont'd)

Function	Device	Source	Line
Front End Timer	TDA1094	Telefunken	
	TA7335	Toshiba	
IF Amplifier	HA1201	Hitachi	
	HA1211	Hitachi	
	MC1350	Motorola	
	MC1355	Motorola	
	MC3310	Motorola	
	AN278	Panasonic	
	AN377	Panasonic	
	CA3002	† RCA	10
	CA3005	† RCA	
	CA3006	† RCA	
	CA3012	† RCA	
	CA3028	† RCA	
	CA3076	† RCA	
	LA1111	Sanyo	
	LA1222	Sanyo	
	TDA4200	Siemens	
	TBA1576	Signetics	
	TEA5560	Signetics	20
	ULN-2243A	Sprague	
	SN76676	TI	
	SN76678	TI	
	TA7302	Toshiba	
	TA7303	Toshiba	
IF Amplifier/Detector	HA11225	Hitachi	
	HA1137	Hitachi	
	HA12411	Hitachi	
	MC1356	Motorola	
	LM1865	**National (3325,3327)**	30
	LM3011	**National (3325,3328)**	
	LM3075	**National (3325,3327)**	
	LM3089	**National (3325,3327)**	
	LM3189	**National (3325,3327)**	
	TBA120	**National (3325,3327)**	
	μPC1004	NEC-Electron	
	μPC1028	NEC-Electron	
	TAA661	Plessey	
	TBA120	Plessey	
	TBA750	Plessey	40
	CA2111A	† RCA	
	CA3013	RCA	
	CA3014	† RCA	
	CA3041	RCA	
	CA3042	RCA	
	CA3065	RCA	
	CA3075	† RCA	
	CA3089	† RCA	
	CA3189	RCA	
	CA3209	RCA	50
	CA3215	RCA	
	LA1140	Sanyo	
	LA1150	Sanyo	
	LA1230	Sanyo	
	LA1231N	Sanyo	
	TDA1200	SGS	
	S041	Siemens	
	TBA120S	Siemens	
	TDA1047	Siemens	
	CA3089	Signetics	60
	CA3089D2	Signetics	
	TBA120S	Signetics	
IF Amplifier Detector	TBA120U	Signetics	
IF Amplifier/Detector	TBA750C	Signetics	
	TCA420A	Signetics	
	TCA770	Signetics	
	ULN-2111A	Sprague	
	ULN-2136A	Sprague	
	ULN-3889A	Sprague	
	TBA120	Telefunken	70
	TDA1093	Telefunken	
	SN76642	TI	
	SN76643	TI	
	SN76669	TI	
	SN76675	TI	
	SN76689	TI	
IF Amplifier, Narrow Band	MC3359	Motorola	
	ULN-3859A	Sprague	
IF Amplifier, PLL, Squelch, Narrow Band	SL6640	Plessey	
	SL6650	Plessey	80
	SL6690	Plessey	
IF System	LA1235	Sanyo	
	LA2300	Sanyo	
Interference Absorption Circuit	TDA1001A	Signetics	
	TDA1001B	Signetics	
LED Tuning Indicator	LB1450	Sanyo	
	LB1473	Sanyo	
Mixer, IF, AGC System	LA1160	Sanyo	
Modulator Circuit (VCO/modulator, 1.4 to 14 MHz)	MC1376	Motorola	
Noise Canceller	HA11219	Hitachi	90
	AN101	Panasonic	
	LA2100	Sanyo	
	LA2101	Sanyo	
	LA2110	Sanyo	
Prescaler (for digital tuning)	TD6104	Toshiba	
Receiver System with Squelch and Scan Control	MP5071	Micro Pwr	
	MC3357	Motorola	
RF/IF Amplifier	CA3127	RCA	
	TBA120U	Signetics	
	TCA770	Signetics	100
Stereo Decoder	XR1310	Exar	
	HA11223	Hitachi	
	HA11227	Hitachi	
	HA1156	Hitachi	
	HA1196	Hitachi	
	MC1309	Motorola	
	MC1310	Motorola	
	TCA4500	Motorola	
	μA758A	Motorola	
	LM1310	**National (3325,3328)**	110
	LM1800	**National (3325,3328)**	
	LM1870	**National (3325,3328)**	
	LM4500A	**National (3325,3328)**	
	μPC1026	NEC-Electron	
	μPC554	NEC-Electron	
	μPC585	NEC-Electron	
	μPC587	NEC-Electron	
	AN115	Panasonic	

(Continued)

Function	Device	Source	Line
Stereo Decoder (Cont'd)	AN211	Panasonic	
	AN271	Panasonic	120
	AN362	Panasonic	
	AN363	Panasonic	
	CA1310A	RCA	
	CA1395	RCA	
	CA3090A	† RCA	
	CA3195	RCA	
	CA758	RCA	
	LA3301	Sanyo	
	LA3350	Sanyo	
	LA3361	Sanyo	130
	LA3365	Sanyo	
	LA3370	Sanyo	
	LA3375	Sanyo	
	LA3380	Sanyo	
	LA3381	Sanyo	
	LA3390	Sanyo	
	TCA4500	Siemens	
	TCA4510	Siemens	
	LM1870	Signetics	
	TDA1005A	Signetics	140
	TDA1578	Signetics	
	μA758	Signetics	
	ULN-2245A	Sprague	
	ULN-3809A	Sprague	
	ULN-3810A	Sprague	
	SN76104	TI	
	SN76105	TI	
	SN76110	TI	
	SN76111	TI	
	SN76113	TI	150
	SN76115	TI	
	SN76116	TI	
	TA7157A	Toshiba	
	TA7401A	Toshiba	
	TA7604A	Toshiba	
	TA7624	Toshiba	
Stereo Multiplexer (PLL)	TA7343	Toshiba	
Tuner	TUA1000	Siemens	
	TDA1062	Telefunken	
	TDA1062S	Telefunken	160

Remote Control Circuits

Function	Device	Source	Line
Remote Control, Infrared	SAA1082	Signetics	
	SAA3004	Signetics	
	SAA3027	Signetics	
	SAA3028	Signetics	
RF Amplifier/Mixer	CA3005	† RCA	
	CA3006	† RCA	
	CA3049	† RCA	
Transceiver (ultrasonic)	LM1812	National	
Transmitter, Infrared	MM53226	National	
	SN76881	TI	170
	SN76882	TI	
	SN76891	TI	

NOTE: In the following category ONLY, the dagger symbol in front of a company name indicates a transmitter/encoder. Absence of a dagger designates a receiver/decoder.

Function	Device	Source	Line
Transmitter/Receiver (encoder/decoder), 2 device sets	S2600	† AMI	
	S2601	AMI	
	S2602	† AMI	
	S2603	AMI	
	S2604	† AMI	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Consumer Circuits (Cont'd)

Remote Control Circuits (Cont'd)

Transmitter/Receiver (encoder/decoder), 2 device sets (Cont'd)

Function	Device	Source		Line
	S2605	AMI		
	S2742	AMI		
	S2743	† AMI		
	S2747	AMI		
	S2748	AMI		
	AY3-8470	† GI		
	AY3-8475	GI		
	SAA1250	† ITT		
	SAA1251	ITT		
	SAA1272	ITT		10
	SAA1350	† ITT		
	SAA1351	ITT		
	MC14457	† Motorola		
	MC14458	Motorola		
	MC145026	Motorola		
	MC145027	Motorola		
	MC145028	Motorola		
	LM1871	National		
	LM1872	National		
	MM5425	National		20
	MM58250	† National		
	MSL9362	**OKI**	**(3873)**	
	MSL9363	**OKI**	**(3873)**	
	MN6021	Panasonic		
	MN6025	Panasonic		
	ML920	Plessey		
	ML922	Plessey		
	ML926	Plessey		
	ML928	Plessey		
	ML929	Plessey		30
	SL470	Plessey		
	SL490	Plessey		
	SL491	Plessey		
	M1124	† SGS		
	SAB3209	Siemens		
	SAB3210	† Siemens		
	SAB3271	Siemens		
	SAB4209	Siemens		
	SDA2007	Siemens		
	SDA2008	† Siemens		40
	SDA3205	Siemens		
	SDA3206	† Siemens		
	SAA5000	† Signetics		
	SAA5012	Signetics		
	SAB3021	Signetics		
	SAB3023	Signetics		
	SAB3042	Signetics		
	SAF1032	Signetics		
	SAF1039	Signetics		
	U318	Telefunken		50
	U321	† Telefunken		
	U327	† Telefunken		
	U328	Telefunken		
	SN76605	† TI		
	SN76606	TI		
	SN76730	TI		
	SN76831	† TI		
	SN76832A	TI		
	TC9132	† Toshiba		
	TC9133	Toshiba		60
	TC9134	Toshiba		

Transmitter/Receiver, Preamplifier

	TEA1009	ITT	

Speech Circuits

Preprogrammed Vocabulary ROM

	VM61001	TI	
	VM61002	**TI**	**(1563)**
	VM61003	**TI**	**(1563)**

(Continued)

Preprogrammed Vocabulary ROM (Cont'd)

	VM61004	**TI**	**(1563)**
	VM61005	**TI**	**(1563)**
	VM71001	TI	
	VM71002	TI	
	VM71003	**TI**	**(1563)** 70

Speech Circuit for Electronic Telephones

TCM1705A	TI	
TCM1706	TI	

Speech Controller/Synthesizer

SP0200	GI	

Speech Evaluation Kit

DT1051	National	

Speech FIFO Buffer Memory and Control Logic

SPB512	GI	
SPB640	GI	

Speech Generator

UAA1003	ITT	
UAA1103	ITT	

Speech Interface Control Logic

	SPR000	**GI**	**(1324)**

Speech Snythesis Processor

	SP0256	**GI**	**(1320,1324)** 80
	DT1000	**National**	**(3338)**
	TMS5100	**TI**	**(1562)**
	TMS5110	**TI**	**(1562)**
	TMS5200	TI	
	TMS5220	**TI**	**(1562)**
	SC-01	Votrax	

Speech Synthesis Processor

SVM9300	Epson	
SP-0250	GI	
SP0230	GI	

Speech Synthesis System, Basic Numbers Kit

DT1052	National	90

Speech Synthesis System, Standard Vocabulary Kit

DT1050	National	
DT1056	**National**	**(3340)**
DT1057	**National**	**(3340)**

Speech Synthesizer, Linear Predictive Data Stored in ROM

S3610	AMI	
S3620	**AMI**	**(3149)**

Synthesized-Speech ROM

TMS6100	**TI**	**(1563)**
TMS6125	**TI**	**(1563)**

Tape Recorder Circuits, Audio

Amplifier System

TA7223	Toshiba	
TA7628	Toshiba	

Amplifier System (for cassette recorders)

TA7628H	Toshiba	100

Amplifier, with AGC, for Recorders

TDA2054	SGS	
TA7137	Toshiba	
TA7137-ST	Toshiba	

Audio System

HA12006	Hitachi	
LM1818	**National**	**(3325,3328)**
AN262	Panasonic	

Automatic Cuing Circuit

LC7510	Sanyo	
LC7512	Sanyo	

Automatic Leveling

S028-2	Siemens	

Automatic Program Search

TC9138	Toshiba	110
TC9139	Toshiba	

Automatic Reverse/Eject for car stereo

TD6304	Toshiba	
TD6308	Toshiba	

Broadband Compander

U401	Telefunken	

Controller (mode change, absence recording)

HA12001	Hitachi	
TC9121	Toshiba	

Head, Microphone, Headphone, Buffer, and Record Amplifiers

HA12005	Hitachi	
TA7617	Toshiba	

IC Switch (cassette)

TC9143	Toshiba	
TC9144	Toshiba	120

Motor Speed Control (automatic stop, dc manual stop, biasing and erasing oscillator)

TDA7770	SGS	

Motor Speed Control, Stop, Pause, Cassette Ejection

TDA7270	SGS	

Power Amp, Preamp with ALC, Meter Driver

TA7225	Toshiba	

Power Amp, Preamp with ALC, Meter Driver, Mute Control

TA7224	Toshiba	

Power Amplifier (cassette)

TA7229	Toshiba	

Power Amplifier (minicassette)

TA7331	Toshiba	

Preamplifier with ALC

LA3201	Sanyo	
LA3210	Sanyo	
SSM2011	SSM	

Preamplifier with ALC (cassette)

TDA1054M	SGS	130

Preamplifier with ALC (minicassette)

TA7330	Toshiba	

System (power amp, preamp with ALC, for minicassette recorders)

TA7625	Toshiba	

Tape Counter

LM8523	Sanyo	

Tape Deck Amplifier System

TA7663	Toshiba	

Tape Deck Amplifier, Dual Channel

TA7639	Toshiba	

Tape Deck Automatic Reverse

AN6249	Panasonic	
AN6250	Panasonic	

Tape Deck Key Controller

AN6251	Panasonic	

Tape Recorder Circuits, Video

Color Processing Circuit

HA11704	Hitachi	
HA11705	Hitachi	140
HA11706	Hitachi	
AN305	Panasonic	
AN306	Panasonic	
AN307	Panasonic	
AN337	Panasonic	
MN6061A	Panasonic	

Dropout Compensation Circuit

AN316	Panasonic	

FM Limiter

HA11703	Hitachi	
AN304	Panasonic	
TDA2730	Signetics	150

FM Recording Signal Processor

HA11701	Hitachi	
AN6321	Panasonic	
AN6331	Panasonic	

Head Amplifier

AN6320	Panasonic	
AN6330	Panasonic	

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Consumer Circuits (Cont'd)

Function	Device	Source	Line
Tape Recorder Circuits, Video (Cont'd)			
Luminance Processing			
	AN302	Panasonic	
	AN303	Panasonic	
Oscillator	TDA3700	Signetics	
Playback Signal Processor			
	HA11702	Hitachi	
Servo Signal Processing			
	HA11707	Hitachi	
	AN301	Panasonic	
	AN318	Panasonic	
	AN6341	Panasonic	
	AN6342	Panasonic	
	AN6344	Panasonic	10
Timer Controller			
	SND5027	SSS	
	SND5037	SSS	
Video Recording Processing			
	AN6300	Panasonic	
Television Circuits			
AFT System	HA1108	Hitachi	
	HA1126	Hitachi	
	CA3139	Motorola	
	MC1364	Motorola	
	MC6195	Motorola	
	LM3064	National	
	μPC423	NEC-Electron	20
	AN222	Panasonic	
	AN320	Panasonic	
	AN321	Panasonic	
	AN325	Panasonic	
	AN326	Panasonic	
	CA3064	† RCA	
	CA3139	RCA	
	LA1364	Sanyo	
	SDA4260	Siemens	
	SN76565	TI	30
	TA7070	Toshiba	
Cable TV Channel Processor			
	SDA2110	Siemens	
Camera	AN614	Panasonic	
	AN616	Panasonic	
Camera Sync. Generator			
	3262A	Fairchild	
	3262B	Fairchild	
	ZNA134E	Ferranti	
	ZNA134J	† Ferranti	
	HD44007	Hitachi	
	MM5321	National	40
	MN6060	Panasonic	
	MN6063	Panasonic	
	MN6064	Panasonic	
	S178A	Siemens	
CATV Amplifiers (hybrid)			
	MHW1121	Motorola	
	MHW1127	Motorola	
	MHW1171	Motorola	
	MHW1172	Motorola	
	MHW1182	Motorola	
	MHW1221	Motorola	50
	MHW1222	Motorola	
	MHW1341	Motorola	
	MHW1342	Motorola	
	MHW1343	Motorola	
	MHW1391	Motorola	
	MHW1392	Motorola	
	MHW5181	Motorola	
	MHW5182	Motorola	

(Continued)

Function	Device	Source	Line
CATV Amplifiers (hybrid) (Cont'd)			
	MHW559	Motorola	
	MHW560	Motorola	60
	MHW561	Motorola	
	MHW562	Motorola	
	MHW570	Motorola	
	MHW572	Motorola	
	MHW580	Motorola	
	MHW594	Motorola	
	MHW595	Motorola	
	CA2100	TRW	
	CA2300	TRW	
	CA2301	TRW	70
	CA2418	TRW	
	CA2600	TRW	
	CA2601	TRW	
Channel Display Driver/Decoder			
	LM1017	National	
	U143	Telefunken	
Channel Processor for Frequency Synthesis Tuning System	SDA2003	Siemens	
Channel Selection			
	μPC1009	NEC-Electron	
	AN5010	Panasonic	
	AN5011	Panasonic	
	LB1500	Sanyo	80
	LB1515	Sanyo	
	LB1550	Sanyo	
	SN76701	TI	
	SN76702	TI	
	SN76710	TI	
	SN76711	TI	
	SN76721	TI	
	SN76727	TI	
	TA7171	Toshiba	
	TA7172	Toshiba	90
	TA7177	Toshiba	
	TA7178	Toshiba	
Character Generator (indicates tuning voltage scale and band info on screen)			
	U191	Telefunken	
Chroma Circuits (demodulators, IF amplifiers, luminance control, signal processors, and various combinations)			
	HA11247	Hitachi	
	HA11412	Hitachi	
	HA11417	Hitachi	
	HA11580	Hitachi	
	MC1323	Motorola	
	MC1324	Motorola	
	MC1327	Motorola	100
	MC1398	Motorola	
	MC1399	Motorola	
	LM1828	National	
	LM1848	National	
	LM2887	National	
	LM3126	National	
	TBA510	National	
	TBA530	National	
	TBA540	National	
	TBA560	National	110
	TBA990	National	
	TDA2522	National	
	TDA2523	National	
	TDA2530	National	
	TDA2560	National	
	TDA3500	National	
	TDA3501	National	
	UPC580	NEC-Electron	
	μPC1380	NEC-Electron	
	μPC562	NEC-Electron	120
	AN223	Panasonic	
	AN224	Panasonic	

(Continued)

Function	Device	Source	Line
Chroma Circuits (demodulators, IF amplifiers, luminance control, signal processors, and various combinations) (Cont'd)			
	AN236	Panasonic	
	AN282	Panasonic	
	AN380	Panasonic	
	AN5310	Panasonic	
	AN5311	Panasonic	
	AN5320	Panasonic	
	AN5330	Panasonic	
	AN5620	Panasonic	130
	AN5630	Panasonic	
	TBA990	Plessey	
	TDA2522	Plessey	
	TDA2523	Plessey	
	TDA2530	Plessey	
	TDA2532	Plessey	
	TDA2560	Plessey	
	CA1398	RCA	
	CA3067	RCA	
	CA3070	RCA	140
	CA3071	RCA	
	CA3072	RCA	
	CA3121	RCA	
	CA3125	RCA	
	CA3126	RCA	
	CA3128	RCA	
	CA3135	RCA	
	CA3137	RCA	
	CA3143	RCA	
	CA3144	RCA	150
	CA3145	RCA	
	CA3151	RCA	
	CA3156	RCA	
	CA3158	RCA	
	CA3170	RCA	
	CA3172	RCA	
	CA3194	RCA	
	CA3201	RCA	
	CA3217	RCA	
	CA3221	RCA	160
	LA1368	Sanyo	
	LA1369	Sanyo	
	LA1390	Sanyo	
	LB1332	Sanyo	
	TDA2140	SGS	
	TDA2151	SGS	
	TDA2161	SGS	
	TDA2522	Siemens	
	TDA2530	Siemens	
	TDA2560	Siemens	170
	TBA540	Signetics	
	TCA640	Signetics	
	TCA650	Signetics	
	TCA660B	Signetics	
	TDA2522	Signetics	
	TDA2530	Signetics	
	TDA2532	Signetics	
	TDA2560	Signetics	
	TDA3500	Signetics	
	TDA3501	Signetics	180
	TDA3505	Signetics	
	TDA3510	Signetics	
	TDA3520	Signetics	
	TDA3560	Signetics	
	TDA3561	Signetics	
	TDA3562	Signetics	
	TDA3563	Signetics	
	TDA3570	Signetics	
	TDA3590	Signetics	
	TDA3600	Signetics	190
	TDA4550	Signetics	
	TDA4560	Signetics	

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† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Consumer Circuits (Cont'd)

Television Circuits (Cont'd)

Function	Device	Source	Line
Chroma Circuits (demodulators, IF amplifiers, luminance control, signal processors, and various combinations) (Cont'd)			
	ULN-2224A	Sprague	
	ULN-2260A	Sprague	
	ULN-2261A	Sprague	
	ULN-3914A	Sprague	
	TBA520	Telefunken	
	TBA530	Telefunken	
	TBA540	Telefunken	
	TBA560	Telefunken	
	TBA990	Telefunken	
	TDA2140	Telefunken	10
	TDA2150	Telefunken	
	TDA2151	Telefunken	
	TDA2160	Telefunken	
	TDA2161	Telefunken	
	SN76242	TI	
	SN76243	TI	
	SN76246	TI	
	SN76267	TI	
	SN76298	TI	
	SN76645	TI	20
	SN76889	TI	
	TA7141A	Toshiba	
	TA7148	Toshiba	
	TA7149	Toshiba	
	TA7150	Toshiba	
	TA7161	Toshiba	
	TA7167	Toshiba	
	TA7168	Toshiba	
	TA7169	Toshiba	
	TA7173	Toshiba	30
	TA7174	Toshiba	
	TA7192	Toshiba	
	TA7193	Toshiba	
	TA7607A	Toshiba	
	TA7611A	Toshiba	
	TA7621	Toshiba	
	TA7622A	Toshiba	
	TA7650	Toshiba	
	TA7659	Toshiba	
	TA7660	Toshiba	40
	TA7661	Toshiba	
	TA7675	Toshiba	
	TA7676	Toshiba	
	TA7678	Toshiba	
Chrome Circuits (demodulators, IF amplifiers, luminance control, signal processors, and various combinations)	HA11409	Hitachi	
D/A Converter (converts an input to coarse and fine tune outputs)	SAB3013	Signetics	
Decoder, 1 of 16			
	M054	SGS	
	M055	SGS	
Deflection Correction Circuit			
	TDA4610	Siemens	
Digital Tuner and Signal Detector			
	LM1019	National	50
	TDA4431	SGS	
Digital Tuning	SAB3035	Signetics	
	SAB3036	Signetics	
	SAB3037	Signetics	
Digital Tuning Device Set			
	SAA1075	ITT	
	SAA1274	ITT	
	SAA1276	ITT	
Digital Tuning System Memory Controller			
	TA7619A	Toshiba	
Digital Tuning System (PLL)			
	TC9136	Toshiba	
	TC9137	Toshiba	60
Frequency Synthesis Control (converts tuning data into frequency information for SDA100 system)			
	SM564	Siemens	
Frequency Synthesis Control (interface between synthesizer and varicap diode tuner)			
	MC2801	Motorola	
Frequency Synthesizer			
	SAB3035	Signetics	
Frequency Synthesizer, interfaces to MPU			
	MN6044	Panasonic	
	MN6049	Panasonic	
Games, See Consumer Circuits, Video Games			
Horizontal & Vertical Processor			
	HA11235	Hitachi	
	HA11244	Hitachi	
	LM1880	National	
	AN294	Panasonic	70
	AN295	Panasonic	
	AN5410	Panasonic	
	AN5411	Panasonic	
	AN5430	Panasonic	
	AN5431	Panasonic	
	AN5435	Panasonic	
	CA3157	RCA	
	CA3190	RCA	
	CA3223	RCA	
	LM1880	Signetics	80
	TDA2577	Signetics	
	TDA2578	Signetics	
Horizontal Processor			
	TBA940	ITT	
	TBA950	ITT	
	TDA1950	ITT	
	TDA9500	ITT	
	TDA9503	ITT	
	TDA9513	ITT	
	MC1391	Motorola	
	MC1394	Motorola	90
	LM1391	National	
	TBA920	National	
	TBA950-2	National	
	TDA2590	National	
	TDA2591	National	
	μPC570	NEC-Electron	
	AN5750	Panasonic	
	AN5760	Panasonic	
	TBA920	Plessey	
	TBA940	Plessey	100
	TBA950	Plessey	
	TDA2591	Plessey	
	CA1391	RCA	
	CA1394	RCA	
	CA3159	RCA	
	CA3210	RCA	
	CA920A	RCA	
	TDA1180	SGS	
	TBA920S	Signetics	
	TDA2571A	Signetics	110
	TDA2581	Signetics	
	TDA2591	Signetics	
	TDA2593	Signetics	
	TDA2594	Signetics	
	TDA2591	Telefunken	
	TDA2593	Telefunken	
	SN76525	TI	
	TA7151	Toshiba	
MATV Amplifiers (hybrid)			
	OM337	Amperex	
	OM339	Amperex	120
	OM345	Amperex	
	OM350	Amperex	
	OM360	Amperex	
	OM361	Amperex	
	OM370	Amperex	
Modulator Circuit for Video Tape Recorders and Disc Players	MC1374	Motorola	
Noise Reduction System			
	TA7652	Toshiba	
On Screen Channel Display			
	M191	SGS	
	M192	SGS	
On Screen Display			
	SDA2005	Siemens	130
On Screen Tuning Voltage Bargraph Display			
	UAA190	Siemens	
PAL Switch	AN387	Panasonic	
Picture Contrast/Brightness			
	TA7126	Toshiba	
	TA7134	Toshiba	
	TA7135	Toshiba	
Power Supply Controller			
	LA5112	Sanyo	
	TDA2582	Signetics	
Prescalers			
Program Memory (17x16)			
	M193	SGS	
Program Memory (20x12), D/A			
	SN76720	TI	140
Radio	M755	SGS	
	M756	SGS	
Signal Processor, Bilingual			
	MC1344	Motorola	
	AN228W	Panasonic	
	AN245	Panasonic	
	AN246	Panasonic	
	AN287	Panasonic	
	AN331	Panasonic	
	AN345	Panasonic	
	CA3120	RCA	150
	CA3142	RCA	
	CA3154	RCA	
	LA7751	Sanyo	
	LA7755	Sanyo	
	TBA890	Signetics	
	SN76524	TI	
	SN76544	TI	
	SN76545	TI	
Sound Circuits	HA11229	Hitachi	
	HA1124	Hitachi	160
	HA1125	Hitachi	
	HA1364	Hitachi	
	TDA1235	ITT	
	TDA1236	ITT	
	MC1351	Motorola	
	MC1357	Motorola	
	MC1358	Motorola	
	TDA1190	Motorola	
	TDA11902	Motorola	
	TDA1190P	Motorola	170
	TDA3190P	Motorola	
	TBA120S	**National (3325,3327)**	
	μPC575	NEC-Electron	
	μPC576	NEC-Electron	
	AN239	Panasonic	
	AN240P	Panasonic	
	AN241	Panasonic	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Consumer Circuits (Cont'd)

Television Circuits (Cont'd)

Function	Device	Source	Line
Sound Circuits (Cont'd)			
	AN255	Panasonic	
	AN340	Panasonic	
	AN355	Panasonic	
	AN5210	Panasonic	
	AN5220	Panasonic	
	AN5250	Panasonic	
	AN5260	Panasonic	
	AN5730	Panasonic	
	AN5820	Panasonic	
	AN5821	Panasonic	10
	TAA570	Plessey	
	TAA661	Plessey	
	TBA120	Plessey	
	TBA750	Plessey	
	CA1190	RCA	
	CA1191	RCA	
	CA3041	RCA	
	CA3042	RCA	
	CA3065	RCA	
	CA3075	† RCA	20
	CA3134	RCA	
	LA1320	Sanyo	
	LA1363	Sanyo	
	LA1365	Sanyo	
	TDA1190	SGS	
	TDA2190	SGS	
	TDA3190	SGS	
	TDA2840	Siemens	
	TDA2841	Siemens	
	TDA4280	Siemens	30
	TDA4281	Siemens	
	TBA120S	Signetics	
	TBA120U	Signetics	
	TBA750C	Signetics	
	TDA2791	Signetics	
	TDA3810	Signetics	
	TDA1190Z	Sprague	
	ULN-2111A	Sprague	
	ULN-2211B	Sprague	
	ULN-2290	Sprague	40
	TBA120	Telefunken	
	SN76643	TI	
	SN76651	TI	
	SN76660	TI	
	SN76665	TI	
	SN76666	TI	
	SN76688	TI	
	TA7051	Toshiba	
	TA7072	Toshiba	
	TA7073A	Toshiba	50
	TA7130	Toshiba	
	TA7146	Toshiba	
	TA7176A	Toshiba	
	TA7243	Toshiba	
	TA7314	Toshiba	
	TA7632	Toshiba	
	TA7633	Toshiba	
Stereo Matrix Circuit			
	AN5822	Panasonic	
Surface Acoustic Wave Filter, IF			
	SW203	Plessey	
	SW205	Plessey	60
	SW206	Plessey	
	SW303	Plessey	
	SW450	Plessey	
Synchronication and Deflection Circuit			
	LA7801	Sanyo	
	LA7802	Sanyo	
	LA7806	Sanyo	
	LA7810	Sanyo	
Synchronous Demodulator			
	TDA0820	Signetics	
T.V. Channel Selection—See also: Switches, Capacitance or Touch Sensing and T.V. Tuning, both this section			
Test Pattern Generator			
	ZNA234	Ferranti	70
Timer, Programmable			
	MM53100	National	
	MM53105	National	
Tone Control	TDA1524	Signetics	
	TA7125	Toshiba	
Touch Tuner: See Switches, Capacitance or touch sensing and T.V.			
Tuner Band Switching			
	AN5700	Panasonic	
	LA7900	Sanyo	
	TA7315	Toshiba	
Tuner Controller			
	SL952	Plessey	
Tuner Controller, Non-Volatile Storage for 16 Programs			
	U193	Telefunken	80
Tuner Controller (2 device set)			
	SAA1020	ITT	
	SAA1121	ITT	
	SAA1220	ITT	
Tuning System	SDA100	Siemens	
	SDA200	Siemens	
Universal Sync. Generator (NTSC)			
	SCN2622A	Signetics	
Universal Sync. Generator (PAL)			
	SCN2621A	Signetics	
Universal Video Interface			
	SCN2637A	Signetics	
Vertical Deflection			
	MC1393	Motorola	
	MC6190	Motorola	90
	MC6191	Motorola	
	MC6192	Motorola	
	MC6193	Motorola	
	MC6194	Motorola	
	μPC1031	NEC-Electron	
	AN5510	Panasonic	
	AN5512	Panasonic	
	AN5520	Panasonic	
	AN5560	Panasonic	
	LA1385	Sanyo	100
	LA1463	Sanyo	
	LA1464	Sanyo	
	LA7800	Sanyo	
	TDA1170	SGS	
	TDA1270	SGS	
	TDA1470	SGS	
	TDA1470A	SGS	
	TDA1670	SGS	
	TDA1770	SGS	
	TDA2653	Signetics	110
	TDA2653A	Signetics	
	TDA2654	Signetics	
	TDA3650	Signetics	
	TDA3651	Signetics	
	TDA3651A	Signetics	
	TDA1170	Sprague	
	ULN-2270	Sprague	
	U2170B	Telefunken	
	TA7152	Toshiba	
	TA7242	Toshiba	120
VHF Tuner	TUA2000	Siemens	
Video Circuits (IF amplifiers, detectors, AGC, AFC, and various combinations)			
	HA11215	Hitachi	
	HA11220	Hitachi	
	HA11221	Hitachi	
	HA11238	Hitachi	
	HA11405	Hitachi	
	MC13001	Motorola	
	MC13002	Motorola	
	MC1330A1	Motorola	
	MC1331	Motorola	130
	MC13330A2	Motorola	
	MC1349	Motorola	
	MC1350	Motorola	
	MC1352	Motorola	
	MC1372	Motorola	
	MC1373	Motorola	
	LM1822	**National** (3329)	
	LM1886	National	
	LM1889	National	
	TBA440	National	140
	TBA970	National	
	TDA2540	National	
	TDA2541	National	
	TDA440	National	
	μPC595	NEC-Electron	
	μPC596	NEC-Electron	
	AN247P	Panasonic	
	AN350	Panasonic	
	AN5111	Panasonic	
	AN5120	Panasonic	150
	AN5610	Panasonic	
	AN5710	Panasonic	
	AN5720	Panasonic	
	SL1430	Plessey	
	SL1431	Plessey	
	SL1432	Plessey	
	SL1440	Plessey	
	TCA270	Plessey	
	TDA2540	Plessey	
	TDA2541	Plessey	160
	TDA440	Plessey	
	CA1352	RCA	
	CA270	RCA	
	CA3068	RCA	
	CA3136	RCA	
	CA3191	RCA	
	CA3192	RCA	
	CA3216	RCA	
	LA1352	Sanyo	
	LA1353	Sanyo	170
	LA1354	Sanyo	
	LA1357N	Sanyo	
	TDA4420	SGS	
	TDA4433	SGS	
	SDA5500	Siemens	
	TBA1440G	Siemens	
	TBA1441	Siemens	
	TDA5500	Siemens	
	TDA5600	Siemens	
	TDA5610	Siemens	180
	TDA5611	Siemens	
	TBA1440G	Signetics	
	TBA1441G	Signetics	
	TDA2540	Signetics	
	TDA2541	Signetics	
	TDA3540	Signetics	
	TDA3541	Signetics	
	TDA440	Telefunken	
	TDA4400	Telefunken	
	TDA4410	Telefunken	190
	TDA4420	Telefunken	
	TDA4421	Telefunken	

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† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Consumer Circuits (Cont'd)

Television Circuits (Cont'd)

Function	Device	Source	Line
Video Circuits (IF amplifiers, detectors, AGC, AFC, and various combinations) (Cont'd)			
	TDA4422	Telefunken	
	TDA4430	Telefunken	
	TDA4431	Telefunken	
	TDA4432	Telefunken	
	TDA4440	Telefunken	
	TDA4450	Telefunken	
	SN76600	TI	
	SN76644	TI	
	SN76650	TI	
	TA7069	Toshiba	10
	TA7074	Toshiba	
	TA7075	Toshiba	
	TA7076	Toshiba	
	TA7124	Toshiba	
	TA7145	Toshiba	
	TA7147	Toshiba	
	TA7162	Toshiba	
	TC5003	Toshiba	
Video Disc Player/Microprocessor Interface (digital auxiliary information buffer)	CD3226	RCA	
Video Pulse Generator	S178	Siemens	20
Y Signal Recording Processor	TA7637	Toshiba	

Video Game Circuits

Function	Device	Source	Line
Character Generator	HS3819	Harris	
Clock Generator (for MM57100)	MM53104	National	
Color Circuit	MN6062	Panasonic	
Color Processor (generates single composite color signal from game chip input)	AY3-8915	GI	
Dedicated (some may be used in programmable systems also)	AY3-8500	GI	
	AY3-8500-1	GI	
	AY3-8603	GI	
	AY3-8603-1	GI	
	AY3-8605	GI	30
	AY3-8605-1	GI	
	AY3-8606	GI	
	AY3-8606-1	GI	
	AY3-8607-1	GI	
	AY3-8610	GI	
Interface (processes graphics data and generates video signals)	AY3-8900	GI	
	AY3-8900-1	GI	
Programmable Video Interface	SCN2636A	Signetics	
	SCN2637A	Signetics	
Sound Generator	**AY3-8910**	**GI** **(1325)**	40
	AY3-8912	**GI** **(1325)**	
	SN76477	TI	
TV/μP Interface	M106	SGS	
Video Display Generator	S68047	AMI	
	MC6847	**Motorola** **(1351)**	
Video Modulator (interfaces audio, color, difference, and luminance signals to TV antenna terminals)	MC1372	Motorola	
	MC1373	Motorola	
	LM1889	National	

Miscellaneous

Function	Device	Source	Line
Appliance Timer	FCM7040	Fairchild	
Digital Lock	**LS7220**	**LSI Comp** **(696)**	50
	LS7225	**LSI Comp** **(696)**	
Facsimile	LM1011	National	
	MN8023	Panasonic	
General-Purpose A/D Converter and Digital-Scale Circuit	S4036	AMI	
Ground Fault Interrupter	CS259	Cherry	
	MC3426	Motorola	
	LM1851	National	
Motor Positioning System (3-chip set), Tachometer Converter, D/A Converter and Switch-Mode Driver for dc Motor	SG290N	Silicon G	
	SG291N	Silicon G	
	SG2925	Silicon G	60
Motor Speed Regulator	MC212	Analog Sys	
	MC213	Analog Sys	
	CS140	Cherry	
	CS175	Cherry	
	CS2917	Cherry	
	MC2907	Cherry	
	LM1014	Fairchild	
	LM1014A	Fairchild	
	μA7392	Fairchild	
	LM1014	National	70
	MSM5819	**OKI** **(3873)**	
	SL440	Plessey	
	TDA1085A	Plessey	
	TDA2085A	Plessey	
	TCA900	SGS	
	TCA910	SGS	
	TDA1151	SGS	
	S572	Siemens	
	TCA955	Siemens	
	TDA1003A	Signetics	80
	TDA1059B	Signetics	
	TDA1506	Signetics	
	TDA1559	Signetics	
	SG1731	Silicon G	
	SG2731	Silicon G	
	SG3731	Silicon G	
Motor Speed Regulator, for Record Players, Tape Recorders	TDA1533	Signetics	
Motor Speed Regulator, PLL	TM4503	Toshiba	
Motor Speed Regulator, PLL, for Record Players, VTR	MSM5810	OKI	
	MSM5811	OKI	90
	MSM5814	OKI	
	MSM5815	OKI	
	MSM5816	**OKI** **(3873)**	
Motor Speed Regulator, with Tape End Indicator, for Tape Recorders	TDA1006A	Signetics	
Motor, Stepping Motor Drive	**S4521**	**AMI** **(2610)**	
	PBL3717	RIFA	
Motor, Stepping Motor Driver	SAA1027	Signetics	
	UDN-2949Z	Sprague	
Music Chimes	SAB0600	Siemens	
Music, Voltage Control Oscillator	SSM2030	SSM	100
	SSM2033	SSM	
Music, Voltage Controlled Filter, Four Stage	SSM2040	SSM	
	SSM2044	SSM	
Music, Voltage Controlled Transient Generator	SSM2050	SSM	
	SSM2055	SSM	
	SSM2056	SSM	
Optical Transceiver (intrusion alarm)	CS258A	Cherry	
Peak Power Meter Driver, Dual (for hi-fi stereo)	TA7318	Toshiba	
	TA7332	Toshiba	
Protector Circuit (overcurrent detection for OCL and speaker)	HA12002	Hitachi	110
	TA7317	Toshiba	
Revolution Counter Pulse Shaper	SAK215	ITT	
Servo Driver	NE544	Signetics	
	NE644	Signetics	
Smoke Detector	CS179	Cherry	
	MP7162	Micro Pwr	
	MC14466	Motorola	
	MC14467	Motorola	
	LM1801	National	
	NF5301	National	120
	CA3164	RCA	
	SCL5331-5	SSS	
	SCL5331-6	SSS	
	SCL5341	SSS	
	SD1	Supertex	
	SD2	Supertex	
	SD3	Supertex	
	SFF25309	Thomson-CSF	
Switch, Video	SAA1300	Signetics	
Switches	SAS560	Hitachi	130
	SAS570	Hitachi	
	MN1976	Panasonic	
	SAS560	Siemens	
	SAS570	Siemens	
	SAS580	Siemens	
	SAS5800	Siemens	
	SAS590	Siemens	
	SAS5900	Siemens	
	SAS6800	Siemens	
	SAS6810	Siemens	140
	SAS660	Telefunken	
	SAS6600	Telefunken	
	SAS6610	Telefunken	
	SAS670	Telefunken	
	SAS6700	Telefunken	
	SAS6710	Telefunken	
Switches, Capacitive Touch Input (keyboard encoder and prioritizer)	TMS1976	TI	
Switches, DC-Controlled, Audio	**LM1037**	**National** **(3326)**	
	LM1038	**National** **(3326)**	
	TDA1029	Signetics	150
	TDA1527	Signetics	
Switches, Proximity	SAS221	Siemens	
	TCA205AK	Siemens	
Switches, Touch-Sensitive Light Dimmer	LS7231	LSI Comp	
	LS7232	LSI Comp	
	LS7233	LSI Comp	
	LS7234	LSI Comp	
	LS7235	LSI Comp	
	LS7236	LSI Comp	
	S566A	Siemens	160
	S566B	Siemens	
	S576A	Siemens	
	S576B	Siemens	

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† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR-Consumer Circuits (Cont'd)

Function	Device	Source	Line
Miscellaneous (Cont'd)			
Switches, Touch-Sensitive Light Dimmer (Cont'd)			
	S576C	Siemens	
	TDA1010	Signetics	
Tachometer Circuit			
	CS189	Cherry	
	CS2917	Cherry	
	LM2907	National	
	LM2917	National	
	AN603	Panasonic	
	SN76810	TI	
Thermo Controller (for air conditioners, refrigerators, etc.)			
	TA7165	Toshiba	
Thermometer Circuit, Digital (−40 to 0°C)			
	AY3-1270	GI	10
Timers. See Appliance Timers, Clock, Watch circuits in this section and Linear-Timers			
Tone Synthesizer for Doorchimes, Toys			
	AY3-1350	GI	
Tuning Voltage Stabilizer, for use with Variable Capacitance Diodes			
	TCA720	ITT	
	TAA550	SGS	

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Followers

Bias Current nA 25°C	Offset Voltage mV 25°C	Voltage Drift µV/°C	Unity Gain Bandwidth MHz min	Slew Rate v/us	Output V mA	Supply Range, V	Comments	Device	Source	Line
Followers										
See also Linear-Amplifiers, Special Purpose - Current Amplifiers										
0.1	10	25 *	100 *	1000	9 @ 100	±5 to ±20	Fast Follower	**ADLH0033**	**†AD (3155)**	
								LH0033	**†National (3342)**	
	50	400	200	3000	10 @ 200	±11 to ±18	Very Fast, FET	9963	† OEI	
0.15	20	25 *	100 *	1000	9 @ 100	±5 to ±20	Fast Follower	**ADLH0033C**	**AD (3155)**	
								LH0033C	**National (3342)**	
0.2	25	300 *	200 *	2000	10 @ 200	±5 to ±20	Very Fast Follower	**LH0063**	**†National (3342)**	
	50	300 *	200 *	2000	10 @ 200	±5 to ±20	Very Fast Follower	**LH0063C**	**National (3342)**	
0.2 *	50	300 *	300 *	2000	10 @ 200	±5 to ±20	Gain 0.094 (50 Ohm)	3553	† Burr-Brown	
0.4	6.0	90	55 *	220	10 @ 22	±6 to ±18	Very Fast Follower	BUF-03E	PMI	10
		100	55 *	220	10 @ 21	±6 to ±18	Very Fast Follower	BUF-03A	PMI	
0.7	15.0	150	50 *	180	10 @ 25	±6 to ±18	Very Fast Follower	BUF-03F	PMI	
			170	50 *	180	±6 to ±18	Very Fast Follower	BUF-03B	† PMI	
3	4.0	6 *	12 *	30 *	10 @ 1	±5 to ±18	Follower, Replaces 102	SG210	Silicon G	
			20 *	30 *	10 @ 1	±5 to ±18	Dual 210 Follower	LH2210	National	
							Follower, Replaces 102	LM210	National	
		10 *	20 *	30 *	10 @ 1	±5 to ±18	Follower, Replaces 102	LM110	† Intersil	
		12 *	12 *	30 *	10 @ 1	±5 to ±18	Follower, Replaces 102	SG110	† Silicon G	
			20 *	30 *	10 @ 1	±5 to ±18	Dual 110 Follower	LH2110	Intersil	
								LH2110	**†National (3342)**	20
							Follower, Replaces 102	LM110	† National	
5	20.0	100	200	1000	10 @ 500	±11 to ±18	Fast, High Current	9911	† OEI	
7	7.5	10 *	12 *	30 *	10 @ 1	±5 to ±18	Follower, Replaces 102	SG310	Silicon G	
			20 *	30 *	10 @ 1	±5 to ±18	Dual 310 Follower	LH2310	Intersil	
								LH2310	† National	
							Follower, Replaces 102	LM310	Intersil	
								LM310	Motorola	
								LM310	National	
10	5.0	6 *	—	—	10 @ 1.25	±15	Follower	LM102	† Intersil	
			8 *	10 *	10 @ 1	±15	Follower	SG102	† Silicon G	30
			10 *	10 *	10 @ 1.25	±12 to ±18	Follower	LM102	† National	
15	10.0	15 *	8 *	10 *	10 @ 1	±15	Follower	SG202	Silicon G	
			10 *	10 *	10 @ 1.25	±12 to ±18	Follower	LM202	National	
20	20.0	100	60	2000	10 @ 100	±6 to ±18	Very Fast Follower	9910	† OEI	
30	15.0	20 *	—	—	10 @ 1.25	±15	Follower	LM302	Intersil	
			8 *	10 *	10 @ 1	±15	Follower	SG302	Silicon G	
			10 *	10 *	10 @ 1.25	±12 to ±18	Follower	LM302	National	
			20 *	20 *	10 @ 1.25	±5 to ±18	Follower	LM302	AMD	
	20	100	25	1000	10 @ ±50	±3 to ±15	6 Identical Sections	MZ320	Analog Sys	

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers

General Purpose

Dual Amplifiers. The 1458 (0°C to 70°C) and the 1558 (−55°C to 125°C) offer approximately the same performance as the 741. Compensation is built in.

Device	Source	Line
XR1458	Exar	
µA1458	Fairchild	
MC1458	Motorola	
LM1458	National	
µPC1458	NEC-Electron	
OP-14	PMI	
PM1458	PMI	
RC1458	Raytheon	
CA1458	RCA	
NE5512	Signetics	10
NE5514	Signetics	
SE5512	† Signetics	
SE5514	† Signetics	
MC1458	Silicon G	
SG1458	Silicon G	
MC1458	TI	

The 101A series consists of the 101A (−55°C to 125°C), the 201A (−25°C to 85°C) and the 301 (0°C to 70°C). These units require an external compensation capacitor which permits the bandwidth to be optimized for particular applications.

Device	Source	Line
AD101A	**† AD (3153)**	
µA101A	Fairchild	
LM101A	† Harris	
LM101A	† Motorola	20
LM101A	† National	
LM101A	† Raytheon	
CA101A	† RCA	
SG101A	† Silicon G	
LM101A	† TI	
TA7506	Toshiba	

The performance of the 741 series is similar to the 101. These units include internal compensation to make the device stable and to eliminate the need for an external capacitor.

Device	Source	Line
AD741	**† AD (3153)**	
µA741	Fairchild	
ICL741	† Intersil	
MP5502	**† Micro Pwr (401,3292)**	30
MC1741	† Motorola	
LM741	† National	
µPC741	NEC-Electron	
OP-02	PMI	
PM741	PMI	
RC741	Raytheon	
CA741	RCA	
µA741	† Signetics	
SG741	† Silicon G	
SFC2741	Thomson-CSF	40
TA7504	Toshiba	

FET Input. The "741" of the FET input devices has yet to be established. Such a device requires very low cost, several sources, and many users. Commercial devices in the 155 series above meet some of these criteria, however, devices from the series below are generally lower in cost.

Device	Source	Line
LF13741	National	

FET Input. The "741" of the FET input devices has yet to be established. Such a device requires very low cost, several sources, and many users. Commercial devices in the 155 series above meet some of these criteria, however, devices from the series below are generally lower in cost.

Device	Source	Line
µAF771	Fairchild	
LF351	**National (3309)**	
CA3140	**† RCA (3350)**	
CA3160	**† RCA (3349)**	
CA3260	**RCA (3349)**	

FET Input. Bipolar/JFET available in standard (155), wideband (156) and uncompensated (157) versions, premium performance (A and B suffixes), and various temperature ranges (155, 255, 355, etc are available.) Some versions approach the low cost of the units below.

Device	Source	Line
LF155	† AMD	
LF155	† Intersil	
LF155	† Motorola	50
LF157	Motorola	
PM155	† PMI	

High Output Current

mA @ V	Device	Source	Line
3500 at 18	**MCEL165**	**Micro Eng (4440)**	
	MCEL2165	Micro Eng	
3000 at 18	MCETCA2365	Micro Eng	
	MCETCA365	**Micro Eng (4440)**	
2700 @ 24	ICH8530I	Intersil	
	ICH8530M	† Intersil	
2000 @ 24	ICH8520I	Intersil	
	ICH8520M	† Intersil	60
2000 @ 22	**LH0021**	**† National (3342)**	
	LH0101	**National (3342)**	
	LH0101A	**† National (3342)**	
	LH0101AC	**National (3342)**	
	LH0101C	**National (3342)**	
2000 @ 20	3573	Burr-Brown	
1000 @ 30	3571A	Burr-Brown	
	3572A	Burr-Brown	
1000 @ 24	ICH8510I	Intersil	
	ICH8510M	† Intersil	70
1000 @ 10	**LH0021C**	**National (3342)**	
750 @ 34	1461	Teledyne P	
500 @ 10	**LH0061**	**† National (3342)**	
	LH0061C	**National (3342)**	
200 @ 10	µA759	† Fairchild	
	µA759C	Fairchild	
130 @ 13	**LH0041**	**† National (3342)**	
	LH0041C	**National (3342)**	
100 @ 10	3554A	Burr-Brown	
	3554B	Burr-Brown	80
	3554S	Burr-Brown	
	LH0003	† National	
	TP3554	Teledyne P	
100 @ —	CA3094	† RCA	
75 @ 145	1480	Teledyne P	
60 @ 30	3580J	Burr-Brown	
50 @ 10	3329	Burr-Brown	
	9914	**OEI (3346)**	
	9918	**OEI (3346)**	
	1430	Teledyne P	90
50 @ 5	LH0005	National	
	LH0005A	† National	
47 @ 14	**LH0020**	**† National (3342)**	
	LH0020C	**National (3342)**	
40 @ 4	LH0005C	National	
30 @ 70	3581J	Burr-Brown	
20 @ 12	TAA2761	Siemens	
	TAA2762	† Siemens	
	TAA2765	Siemens	
	TAA4761	Siemens	100
	TAA4765	Siemens	
	TAA761	Siemens	
	TAA762	† Siemens	
	TCA311	Siemens	
	TCA312	† Siemens	
	TCA315	Siemens	
	TCA325	Siemens	
	TCA331	Siemens	
	TCA332	† Siemens	
	TCA335	Siemens	110
20 @ 10	**9912**	**† OEI (3346)**	
20 @ 8	TAA861	Siemens	
	TAA862	† Siemens	
	TAA865	Siemens	
15 @ 30	LH0004C	National	

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers (Cont'd)

High Output Current (Cont'd)

mA @ V	Device	Source	Line
15 @ 145	3582J	Burr-Brown	
	3583	Burr-Brown	
	3584	Burr-Brown	
15 @ 10	**HA-2620**	**† Harris (3228,3287)**	
	HA2620	† Intersil	

High Speed

Unity Gain Slew Rate (V/μs min)	Device	Source	Line
2500 (g=5)	**9909**	**OEI (3346)**	
1000	**AM-500GC**	**Datel (2623)**	
	AM-500MC	Datel	
	9914	OEI	
600	9912	† OEI	10
	9932	**OEI (3346)**	
500	1430	Teledyne P	
	1430-83	† Teledyne P	
400	**LH0024**	**† National (3342)**	
350	**LH0032**	**† National (3342)**	
	LH0032C	**National (3342)**	
300	**HOS-050**	**AD (3155)**	
	HOS-050A	**AD (3155)**	
	9916	**† OEI (3346)**	
280	HA-2530	† Harris	20
	HA2530	† Intersil	
250(g=5)	**9906**	**† OEI (3346)**	
250	HA-2535	Harris	
	LH0024C	**National (3342)**	
	1435	† Teledyne P	
200	**HA-5190**	**Harris (3275,3287,3289)**	
	HA-5195	**Harris (3275,3287,3290)**	
	9908	**† OEI (3346)**	
	9917	OEI	
100(g=3)	**HA-2520**	**† Harris (3220,3287)**	30
	HA2520	† Intersil	
100	**AD509K**	**AD (3155)**	
	AD509S	**† AD (3155)**	
	3550K	Burr-Brown	
	OPA605	Burr-Brown	
80	**AD509J**	**AD (3155)**	
	3507J	Burr-Brown	
	1322	Teledyne P	
	1322-01	† Teledyne P	
65	3550J	Burr-Brown	40
	3550S	† Burr-Brown	
50	LM118	† AMD	
	LM318	AMD	
	AD518	**AD (3155)**	
	AD518S	**† AD (3155)**	
	AD528	AD	
	AD528S	† AD	
	μA118	† Fairchild	
	μA318	Fairchild	
	HA-2510	**† Harris (3218,3287)**	50
	LM118	**† Harris (3286,3288)**	
	LM318	**Harris (3286,3288)**	
	HA2510	Intersil	
	LH0062	**† National (3342)**	
	LH0062C	**National (3342)**	
	LM118	† National	
	LM318	National	
	LM118	† Raytheon	
	LM118	† TI	
	LM318	TI	60
	SFC2118	† Thomson-CSF	
	SFC2318	Thomson-CSF	

High Voltage

Maximum Supply Voltage	Device	Source	Line
±150	3582J	Burr-Brown	
	3583	Burr-Brown	
	3584	Burr-Brown	
±75	3581J	Burr-Brown	
±40	3571A	Burr-Brown	
	3572A	Burr-Brown	
	AM-464-2	**Datel (2622)**	
	AM-464-2M	† Datel	70
	HA-2640	**† Harris (3232,3287)**	
	HA-2645	**Harris (3232,3287)**	
	LM143	**† Harris (3286,3288)**	
	MC1536	† Motorola	
	LH0004	† National	
	LH0004C	National	
	LM143	† National	
	LM144	† National	
	LM1536	† National	
	SG1536	† Silicon G	80
	1332	Teledyne P	
±35	3580J	Burr-Brown	
±34	MC1436	Motorola	
	LM344	National	
	SG1436	Silicon G	
±30	ICH8510I	Intersil	
	ICH8510M	† Intersil	
	ICH8520I	Intersil	
	ICH8520M	† Intersil	
	ICH8530I	Intersil	90
	ICH8530M	† Intersil	
	MC1436C	Motorola	
	LM1436	National	
	LM343	National	
	SG1436C	Silicon G	

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers (Cont'd)

Low Bias Current

Rated values do not usually include thermal rise due to circuit operation.

Current pA 25°C	Device	Source	Line
0.01	ICH8500A	Intersil	
0.075	3528C	Burr-Brown	
	AD515L	**AD (3153)**	
	OPA104CM	Burr-Brown	
0.1	3523L	Burr-Brown	
	ICH8500	Intersil	
	AM-490-2C	Datel	
0.15	**AD515K**	**AD (3153)**	
0.2	ADOP-07	† AD	10
0.25	AD523L	AD	
	3523K	Burr-Brown	
	OPA104BM	Burr-Brown	
0.3	**AD515J**	**AD (3153)**	
	AM-490-2B	Datel	
	HA-2904	Harris	
0.5	AD523K	AD	
	3523J	Burr-Brown	
	OPA104AM	Burr-Brown	
	AD504M	AD	20
	AD510L	AD	
	AD517L	AD	
	3510C	Burr-Brown	
	MP517L	Micro Pwr	
	MP5505A	† Micro Pwr	
	LH0044A	† National	
	LH0044AC	National	
1.0	AD523J	AD	
	3522L	Burr-Brown	
	ICL8007AC	Intersil	30
	ICL8007AM	† Intersil	
	LH0052	**† National (3342)**	
2.0	3527B	Burr-Brown	
	OPA103BM	Burr-Brown	
5.0	**AD506L**	**AD (3153)**	
	OPA103AM	Burr-Brown	
	CA3080	RCA	
	CA3080A	† RCA	
	3522K	Burr-Brown	
	3522S	Burr-Brown	40
	3527A	Burr-Brown	
	3527C	Burr-Brown	
	LH0052C	National	
	1425-01	Teledyne P	
	1425-02	Teledyne P	
10.0	**MP5507A**	**† Micro Pwr (401,3292)**	
	OPA101	Burr-Brown	
	OPA106/MIL	† Burr-Brown	

Low Drift

Function	Device	Source	Line
0.5	LH0044B	National	
	OP-05A	† PMI	50
0.6	MP5507A	† Micro Pwr	
	MP5507E	Micro Pwr	
	SSS725A	† AMD	
	AM-430B	Datel	
	AM-490-2M	† Datel	
	μA714	† Fairchild	
	HA-2900	† Harris	
	HA-5130-5	Harris	
	HA-5135-5	Harris	
	OP-05E	PMI	60
	OP-07A	† PMI	
1.0	**AD510K**	**AD (3153)**	
	AD510S	**† AD (3153)**	
	LM725A	National	
	AD504L	AD	
	AD504S	† AD	
	AD517K	AD	
	AD517S	† AD	
	3271	Burr-Brown	
	3291	Burr-Brown	70
	3354	Burr-Brown	
	3500E	Burr-Brown	
	3510B	Burr-Brown	
	3510S	† Burr-Brown	
	3521L	Burr-Brown	
	AM-490-2A	Datel	
	μA725A	† Fairchild	
	μA725E	Fairchild	
	MP517K	Micro Pwr	
	MP517S	† Micro Pwr	80
	MP5505A	† Micro Pwr	
	LH0044	† National	
	LH0044C	National	
	LM11	† National	
	LM11C	National	
	OP-05	† PMI	
1.0 (dual unit)	**MP5510A**	**† Micro Pwr (401,3292)**	
	MP5510B	**Micro Pwr (401,3292)**	
	MP5510E	**Micro Pwr (401,3292)**	
	OP-10	† PMI	90
	OP-10A	† PMI	
	OP-10E	PMI	
1.3	**MP5507E**	**Micro Pwr (401,3292)**	
	AM-430M	† Datel	
	μA741E	Fairchild	
	MP5507B	† Micro Pwr	
	OP-07	† PMI	
	OP-07E	PMI	
	AM-430A	Datel	
1.5	**MP5505C**	**Micro Pwr (401,3292)**	100
	3510A	Burr-Brown	
	OP-05C	PMI	
	OP-20B	† PMI	
	OP-20F	PMI	
1.5 (Dual Unit)	OP-10C	PMI	
	SSS725C	PMI	
1.6	μA714C	Fairchild	
	MP5507C	Micro Pwr	
	OP-07C	PMI	
2.0	3510VM	Burr-Brown	110
	3527C	Burr-Brown	
	OPA103CM	Burr-Brown	
	CA3193B	† RCA	

Low Power Non-Adjustable

Supply Current μA ± 15V	Device	Source	Line
9	OP-215B	† PMI	
	OP-215C	† PMI	
	OP-215F	PMI	
	OP-215G	PMI	
45	OP-20B	† PMI	
	OP-20C	† PMI	
	OP-20F	PMI	120
	OP-20G	PMI	
	OP-20H	PMI	
150	HA-2700	† Harris	
	HA-2704	Harris	
	HA-2705	Harris	
200	**TL061 Series**	**TI (3425)**	
220	OP-420B	† PMI	
	OP-420C	† PMI	
	OP-420F	PMI	
	OP-420G	PMI	130
350	OP-21B	† PMI	
	OP-21F	PMI	
400	**LF442A**	**National (3309,3314)**	
	OP-21C	† PMI	
	OP-21G	PMI	
475	OP-21H	PMI	
500	**LF442**	**National (3309,3314)**	
600	LM112	† National	
	LM212	National	
	LM316A	National	140
	LM108	† AMD	
	AD108	**† AD (3153)**	
	LM108	**† Harris (3286,3288)**	
	LM108	† Intersil	
	LM108	† Motorola	
	LM108	† National	
	PM108	† PMI	
	SG108	† Silicon G	
	SFC2108	† Thomson-CSF	
	LM112	† AMD	150
	μA108	† Fairchild	
	OP-08	† PMI	
	OP-12	† PMI	

Programmable

The current drain limits of these units are approximately 10-300 μa.	CA3094	† RCA	
	CA3094A	† RCA	
	CA3094B	† RCA	
The current drain limits of these units are approximately 10-300 μA.	μA776C	Fairchild	
	HA-2720	**† Harris (3236)**	
	HA-2725	**Harris (3236)**	
	LM4250C	**Harris (3286,3288)**	160
	ICL4250	† Intersil	
	ICL4250C	† Intersil	
	MC1776	† Motorola	
	LM4250	† National	
	LM4250C	† National	
	SG3250	Silicon G	
	SG4250	† Silicon G	
	SG4250C	† Silicon G	
	CA3078	**† RCA (3354)**	
	UC4250	† Solitron	170
	UC4250C	Solitron	
	μA776	† Fairchild	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers (Cont'd)

Low Power Programmable (Cont'd)

The current drain limits of these units are approximately 10-300 μA. (Cont'd)

Supply Current μA ±15V	Device	Source	Line
	LM4250	**† Harris (3286,3288)**	
	ICL8021C	Intersil	
	ICL8021M	† Intersil	
	MC1776C	Motorola	
	MC3476	Motorola	
	CA3078A	**† RCA (3354)**	
	CA6078A	**† RCA (3354)**	
	SG1250	† Silicon G	
	SG2250	Silicon G	
μA @ ±8V			
20	ICL7611M	† Intersil	10
	ICL7613M	† Intersil	
	ICL7631M	† Intersil	
	ICL7632M	† Intersil	
	ICL7642M	† Intersil	
200	ICL7612C	Intersil	
	ICL7611C	Intersil	
	ICL7612M	† Intersil	
	ICL7613C	Intersil	
	ICL7614C	Intersil	
	ICL7615C	Intersil	20
	ICL7621C	Intersil	
	ICL7622C	Intersil	
	ICL7631C	Intersil	
	ICL7642C	Intersil	

Programmable

Function	Device	Source	Line
Adjustable Current/Performance Single (1 unit per package)			
	ICL7612C	Intersil	
	CA3094	† RCA	
	CA3094A	† RCA	
	CA3094B	† RCA	
	μA776C	Fairchild	
	μA776M	† Fairchild	30
	HA-2720	† Harris	
	HA-2725	Harris	
	LM4250C	Harris	
	ICL4250	† Intersil	
	ICL4250C	† Intersil	
	ICL7611C	Intersil	
	MC1776	† Motorola	
	LM4250	† National	
	LM4250C	† National	
	SG3250	Silicon G	40
	SG4250	† Silicon G	
	SG4250C	† Silicon G	
	CA3078	† RCA	
	CA3080	RCA	
	CA3080A	† RCA	
	LM4250	† Harris	
	ICL7611M	† Intersil	
	ICL7612M	† Intersil	
	ICL7613C	Intersil	
	ICL7613M	† Intersil	50
	ICL8021C	Intersil	
	ICL8021M	† Intersil	
	MC1776C	Motorola	
	MC3476	Motorola	
	CA3078A	† RCA	
	SG1250	† Silicon G	
	SG2250	Silicon G	
Dual (2 units per package)			
	HA-2730	**† Harris (3239,3287)**	
	HA-2735	**Harris (3239,3287)**	
	ICL8022C	Intersil	60
	ICL8022M	† Intersil	
	LH24250	**† National (3342)**	
	LH24250C	**National (3342)**	
Triple (3 units per package)			
	CA3060	† RCA	
	ICL7632C	Intersil	
	ICL7632M	† Intersil	
	ICL8023C	Intersil	
	ICL8023M	† Intersil	
	CA3060A	RCA	
	CA3060B	RCA	70
	SG1253	† Silicon G	
	SG2253	Silicon G	
	SG3253	Silicon G	
	L144A	† Siliconix	
	L144B	Siliconix	
	L144C	Siliconix	
Quad (4 units per package)			
	XR146	**† Exar (3207)**	
	XR246	**Exar (3207)**	
	XR346	**Exar (3207)**	
	XR4202	Exar	80
	XR4202M	† Exar	
	MC3575	† Motorola	
	TCA3002	Motorola	
	TCA3003	Motorola	
	LM146	† National	
	LM246	National	
	LM346	National	

(Continued)

Function	Device	Source	Line
Quad (4 units per package) (Cont'd)			
	LM146	Raytheon	
	LM246	Raytheon	
	LM346	Raytheon	90

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers (Cont'd)

Single Supply

Single Units

Supply Voltage, V	Device	Source	Line
to 24	CA3094	† RCA	
to 36	μA759	† Fairchild	
	μA759C	Fairchild	
	CA3140	† RCA	
	CA3094A	† RCA	
to 44	CA3094B	† RCA	
1 to 16	ICL7612C	Intersil	
	ICL7612M	† Intersil	
5 to 16	**CA3130**	**† RCA (3349)**	
	CA3130A	**† RCA (3349)**	10
	OP-20B	† PMI	
	OP-20C	† PMI	
	OP-20F	PMI	
	OP-20G	PMI	
	OP-20H	PMI	

Dual Units

Supply Voltage, V	Device	Source	Line
to 20	OP-215B	† PMI	
	OP-215C	† PMI	
	OP-215F	PMI	
	OP-215G	PMI	
3 to 26	HA17902	Hitachi	20
	LM2902	Motorola	
	LM2904	Motorola	
	LM2902	National	
	LM2904	National	
	LM2902	Raytheon	
	CA2904	RCA	
	LM2902	TI	
	LM2904	TI	
3 to 30	LM158	† Motorola	
	LM258	Motorola	30
	LM358	Motorola	
	LM158	† National	
	LM258	National	
	LM258A	National	
	LM358A	National	
	CA158	† RCA	
	CA258	RCA	
	LM158	† Signetics	
	LM258	Signetics	
	NE532	Signetics	40
	NE535	† Signetics	
	SE532	† Signetics	
	SE535	† Signetics	
	LM158	† TI	
	TL321C	TI	
	TL321M	† TI	
	LM158A	† National	
	LM358	National	
	CA358	RCA	
	LM358	Signetics	50
	LM358	TI	
3 to 36	μA798	Fairchild	
	MC3458	Motorola	
4 to 36	**CA3240**	**RCA (3350)**	
8 to 36	TBA231	SGS	

Quad Units

Supply Voltage, V	Device	Source	Line
3 to 30	μA124	† Fairchild	
	μA224	Fairchild	
	μA324	Fairchild	
	LM124	† Intersil	
	LM324	Intersil	60
	LM124	† Motorola	
	LM224	Motorola	

(Continued)

Supply Voltage, V	Device	Source	Line
3 to 30		(Cont'd)	
	LM324	Motorola	
	LM124	† National	
	LM224	National	
	LM324	National	
	μPC224	NEC-Electron	
	μPC324	NEC-Electron	
	LM124	† Raytheon	
	LM224	Raytheon	70
	LM324	Raytheon	
	CA124	† RCA	
	CA224	RCA	
	CA324	RCA	
	LM124	† Signetics	
	LM224	Signetics	
	LM324	Signetics	
	SG124	† Silicon G	
	SG224	Silicon G	
	SG324	Silicon G	80
	LM124	† TI	
	LM224	TI	
	LM258	TI	
	LM324	TI	
3 to 36	**XR3403**	**Exar (3207)**	
	XR3503	**† Exar (3207)**	
	μA3303C	Fairchild	
	μA3403C	Fairchild	
	MC3303	Motorola	
	MC3403	Motorola	90
	MC3503	† Motorola	
	RC3403	Raytheon	
	RM3503	† Raytheon	
	RV3403	Raytheon	
4 to 18	MC3401	Motorola	
	LM3401	National	
	RC3401	Raytheon	
	CA3401	† RCA	
4 to 28	MC3301	Motorola	
	LM3301	National	100
	RC3301	Raytheon	
4 to 32	LM2900	National	
	LM3900	National	
	LM2900	Raytheon	
	LM3900	Raytheon	
	LM2900	TI	
	LM3900	TI	
4 to 36	LM1900	TI	
5 to 30	OP-420B	† PMI	
	OP-420C	† PMI	110
	OP-420F	PMI	
	OP-420G	PMI	

Wide Band

Unity Gain Bandwidth MHz	Device	Source	Line
30 *	LH0003	† National	
	LH0003C	National	
	LH0005	National	
	LH0005A	† National	
	LH0005C	National	
	μPC702	NEC-Electron	
	TL702C	TI	
	TL702M	† TI	120
	μPC51A	NEC-Electron	
	SL565	Plessey	
35 *	**AD507J**	**AD (3155)**	
	AD507K	**AD (3155)**	
	AD507S	**† AD (3155)**	
	9917	OEI	
38 *	CA3100	† RCA	
40	9932	OEI	
50 *	CA3015	† RCA	
	CA3015A	† RCA	130
	CA3016	† RCA	
	CA3016A	† RCA	
	CA3030	RCA	
	CA3030A	RCA	
	CA3038	† RCA	
	CA3038A	† RCA	
	3551J	Burr-Brown	
	3551S	† Burr-Brown	
	OPA101	Burr-Brown	
	OPA102	Burr-Brown	140
60 *	1430	Teledyne P	
	1430-83	† Teledyne P	
	9912	† OEI	
65 *	μA715C	Fairchild	
	μA715M	† Fairchild	
70 *	3554A	Burr-Brown	
	3554B	Burr-Brown	
	3554S	Burr-Brown	
	ADLH0032	**† AD (3155)**	
	ADLH0032C	**AD (3155)**	150
	LH0032	† National	
	LH0032C	National	
	LH0024	† National	
	LH0024C	National	
	OPA605	Burr-Brown	
100	AM-500GC	Datel	
	AM-500MC	Datel	
	9912	† OEI	
	9906	† OEI	
	NE5539	Signetics	160
	SE5539	† Signetics	
	9908	† OEI	
	9909	OEI	
200	9916	† OEI	
	9918	OEI	
300	9914	OEI	
500 *	1435	† Teledyne P	
1000	OPA600/MIL	Burr-Brown	

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers-Characteristics

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift µV/°C	Band-width MHz	Slew Rate V/µs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source	Line
Single Units												
In this list the "Comp." column indicates the number of compensation components required at unity gain. Thus 0 indicates a fully compensated amplifier. The bandwidth and slew rate are listed with the amplifier compensated for unity gain.												
0.005	0.01	0.005	0.01	2.0 *	2.5 *	10M	120	0	Chopper Stabilized	ICL7650C	Intersil	
	3	—	0.1	0.3	—	30K	88 *	0	Commutating Auto Zero, Compensated	ICL7600C	Intersil	
										ICL7600M	† Intersil	
									Commutating Auto Zero, Uncompensated	ICL7601C	Intersil	
										ICL7601M	† Intersil	
0.01 *	10	—	0.2 *	8 *	2.8 *	1.5M *	120	0	Ultra-Low Noise	**MP5527**	**Micro Pwr (401,3292)**	
				63 *	17 *	1.5M *	120	0	Ultra-Low Noise	**MP5537**	**Micro Pwr (401,3292)**	
0.020 *	0.15 *	0.05 *	0.1	3 *	2.5 *	1M	120	3	Chopper Stabilized	AM-490-2C	Datel	
			0.3	3 *	2.5 *	1M	120	3	Chopper Stabilized	AM-490-2B	Datel	10
			0.6	3 *	2.5 *	1M	120	3	Chopper Stabilized	AM-490-2M	† Datel	
			1.0	3 *	2.5 *	1M	120	3	Chopper Stabilized	**AM-490-2A**	**Datel (2623)**	
0.025	1	0.25	0.5	0.25 *	0.1 *	1M	110	0	Ultra Low Offset Voltage, Low Drift	**AD517L**	**AD (3153)**	
										MP517L	Micro Pwr	
	2	2	0.6	0.6 *	0.17 *	300K	110	0	Ultra Low Offset Voltage, Low Drift	**ADOP-07A**	**†AD (3153)**	
										OP-07A	† Intersil	
				1.2 *	0.25 *	300K	110	0	Ultra Low Offset Voltage, Low Drift	MP5507A	† Micro Pwr	
										OP-07A	† Micro Pwr	
										OP-07A	† PMI	
				2.5 *	0.8 *	1M	100	0	Ultra Low Offset Voltage, Low Drift	**HA-5130-2**	**Harris (3264,3287)**	20
										HA-5135-2	**Harris (3264,3287)**	
										HA-5130-5	**Harris (3264,3287)**	
										HA-5135-5	**Harris (3264,3287)**	
	10	2.5	2	0.3 *	0.1 *	1M	110	0	Trimmed Offset	**AD510L**	**AD (3153)**	
	15	2.5	0.5	0.4 *	0.06 *	1M	120	1	Precision, Low Noise	**LH0044A**	**†National (3342)**	
										LH0044AC	**National (3342)**	
	20	20	0.75	—	—	5-1000	100	0	Instrumentation (2 amps available as pair)	3629B	† Burr-Brown	
	25	30	0.5	—	—	5-1000	100	0	Instrumentation (2 amps available as pair)	3629C	Burr-Brown	
										3629S	† Burr-Brown	
	35	50	3	—	—	5-1000	100	0	Instrumentation (2 amps available as pair)	3629A	Burr-Brown	30
	40	35	—	8 *	3.2	1200K *	126 *	0	Ultra Low Noise, Low Offset	OP-27A	† PMI	
										OP-27E	PMI	
				63 *	11 *	—	—	0	Low Noise, High Slew Rate	OP-37A	† Raytheon	
			0.2	25 *	18 *	1M	—	0	Ultra Low Noise, Low Offset	OP-37A	† PMI	
										OP-37E	PMI	
			0.6	5	1.7	1M	114	0	Ultra Low Noise	AM-427-B	Datel	
						600K	114	0	Ultra Low Noise	OP-27A	† Raytheon	
										OP-27E	Raytheon	
				8 *	1.7	1000K	114	0	Ultra Low Noise	OPA27A	† Burr-Brown	
										OPA27E	Burr-Brown	40
				40 *	11	1000K	114	0	Ultra Low Noise	OPA37A	† Burr-Brown	
										OPA37E	Burr-Brown	
0.05	0.014	0.014	45	7	13 *	128	86	0	High Speed Instrumentation	AM-543MM	† Datel	
										AM-543MR	Datel	
	0.05	0.05	45	7	13 *	128	86	0	High Speed Instrumentation	AM-543MC	Datel	
	1	0.5	0.4	3 *	2.5 *	10M	130	3	Chopper Stabilized	HA-2904	Harris	
	2	0.75	1	0.25 *	0.1 *	1M	100	0	Ultra Low Offset Voltage, Low Drift	**AD517K**	**AD (3153)**	
										AD517S	**†AD (3153)**	
										MP517K	Micro Pwr	
										MP517S	† Micro Pwr	50
	5	0.5	0.5	0.2	—	2M	126	0	Precision Instrumentation	LM163A	† National	
										LM363A	† National	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift µV/°C	Band-width MHz	Slew Rate V/µs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source	Line
Single Units											**(Cont'd)**	
0.05											(Cont'd)	
	10	10	0.5	—	5	1000	90	0	Precision Insrumentation	**AD524C**	**AD (3158)**	
	13	4.0	1	0.3 *	0.1 *	1M	110	0	Trimmed Offset	AD510K	AD	
										AD510S	† AD	
	14	14	1	0.5 *	—	1024	86	0	Low Drift Instrumentation	AM-542MM	† Datel	
										AM-542MR	Datel	
	30	—	0.2	0.25	5	1K	115	0	Precision Instrumentation	**AD624C**	**AD (3156,3158)**	
		5	0.5	0.4 *	0.06 *	500K	114	1	Precision, Low Noise	**LH0044B**	**National (3342)**	
			1	0.4 *	0.06 *	500K	114	1	Precision, Low Noise	**LH0044**	**† National (3342)**	
	50	50	1	0.5 *	—	1024	86	0	Low Drift Instrumentation	AM-542MC	Datel	
0.06	1	0.5	0.6	3 *	2.5 *	1M	120	3	Chopper Stabilized	HA-2900	† Harris	10
	15	10	0.5	0.4 *	0.5 *	1M	110	1	Low Drift	3510C	Burr-Brown	
	55	50	—	63 *	11 *	—	—	0	Low Noise, High Slew Rate	OP-37B	† Raytheon	
										OP-37F	Raytheon	
			0.3	8 *	3.2 *	1200K *	123 *	0	Ultra Low Noise	OP-27B	PMI	
										OP-27F	PMI	
				25 *	18 *	1M	—	0	Ultra Low Noise, Low Offset	OP-37B	† PMI	
										OP-37F	PMI	
			1.3	5	1.7	500K	106	0	Ultra Low Noise	OP-27B	† Raytheon	
										OP-27F	Raytheon	
0.060	55	50	1.3	8 *	1.7	1000K	106	0	Ultra Low Noise	OPA27B	† Burr-Brown	20
										OPA27F	Burr-Brown	
				40 *	11	1000K	106	0	Ultra Low Noise	OPA37B	† Burr-Brown	
										OPA37F	Burr-Brown	
0.075	3	2.8	1.3	0.6 *	0.17 *	200K	110	0	Ultra Low Offset Voltage, Low Drift	OP-07	† Intersil	
										ADOP-07	**† AD (3153)**	
				1.2 *	0.25 *	200K	110	0	Ultra Low Offset Voltage, Low Drift	OP-07	† Micro Pwr	
										µA714	† Fairchild	
										MP5507B	**† Micro Pwr (401,3292)**	
										OP-07	† PMI	
	4	3.8	0.2	0.4	0.2	150K	106	0	Ultra-Low Offset Voltage	OP-07E	TI	30
			1.3	0.6 *	0.17 *	200K	123 *	0	Ultra Low Offset Voltage, Low Drift	**ADOP-07E**	**AD (3153)**	
										OP-07E	Intersil	
				1.2 *	0.25 *	200K	106	0	Ultra Low Offset Voltage, Low Drift	µA714E	Fairchild	
										MP5507E	Micro Pwr	
										OP-07E	Micro Pwr	
										OP-07E	PMI	
	15	3	2	1.2 *	0.25 *	1M	120	0	Precision Instrumentation	**CA3493B**	**† RCA (3351)**	
										CA3193B	**† RCA (3351)**	
0.08	1	0.5	0.2 *	3 *	2.5 *	1M	120	3	Chopper Stabilized	AM-490	Datel	
										HA-2905	Harris	40
										1340	Teledyne P	
	15	0.5	1.5	0.1 *	—	1M	105	0	Precision, Low Power	OP-20B	† PMI	
										OP-20F	PMI	
0.10	3	2.8	0.4 *	1.2 *	0.25 *	500K	—	0	Ultra Low Offset Voltage	OP-207A	† PMI	
										OP-207B	PMI	
	5	1	3	0.2 *	—	2M	120	0	Precision Instrumentation	LM163	† National	
	20	15	0.5	—	5	1000	90	0	Precision Insrumentation	**AD524B**	**AD (3158)**	
	25	5	3	3 *	0.1 *	250K	94	0	Trimmed Offset	**AD510J**	**AD (3153)**	
	35	5	1	0.4 *	0.06 *	500K	114	1	Precision, Low Noise	**LH0044C**	**National (3342)**	
	40	1	0.8	—	1.7	1800	114	0	Ultra Low Noise	OP-27	Micro Pwr	50
	50	—	0.5	0.25	5	1K	110	0	Precision Instrumentation	**AD624B**	**AD (3156,3158)**	
		35	0.5	—	5	1000	90	0	Precision Insrumentation	**AD524S**	**† AD (3158)**	
	70	1	0.6	—	—	1M	120	4	Instrumentation	SSS725A	† PMI	
			0.8	—	—	1M	120	4	High Performance 725	SSS725A	† AMD	
					0.01	100K	120	4	High Gain Instrumentation	OP-06A	† PMI	
	80	40	0.4 *	8 *	3.2 *	17	1800	114	0	OP-37	Micro Pwr	
		75	—	63 *	11 *	—	—	0	Low Noise, High Slew Rate	OP-37C	† Raytheon	
										OP-37G	Raytheon	
			0.4 *	8 *	3.2 *	1200K	120	0	Ultra Low Noise	OP-27G	PMI	
						1200K *	120	0	Ultra Low Noise	OP-27C	PMI	60
											(Continued)	

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift µV/°C	Band-width MHz	Slew Rate V/µs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source	Line
Single Units											**(Cont'd)**	
											(Cont'd)	
0.10	80	75	0.4 *									
				25 *	18 *	700K	120	0	Ultra Low Noise	OP-37C	† PMI	
										OP-37G	PMI	
			1.8	5	1.7	106K	100	0	Ultra Low Noise	AM-427-A	Datel	
										AM-427-M	† Datel	
						300K	100	0	Ultra Low Noise	OP-27C	† Raytheon	
										OP-27G	Raytheon	
				8 *	1.7	700K	100	0	Ultra Low Noise	OPA27C	† Burr-Brown	
										OPA27G	Burr-Brown	
										OPA37C	† Burr-Brown	
										OPA37G	Burr-Brown	10
	100	—	1	0.25	5	1K	100	0	Precision Instrumentation	**AD624S**	**† AD (3156,3158)**	
	150	15	0.5	0.6 *	0.25	2M	110	0	Precision, Low Power	OP-21B	† PMI	
										OP-21F	PMI	
0.12	25	15	1	0.4 *	0.5	1M	110	1	Low Drift	3510B	Burr-Brown	
										3510S	† Burr-Brown	
			2	0.25	0.5	1M	110	1	Precision, Low Drift	3510V	† Burr-Brown	
0.13	12	6	0.2	0.4	0.2	100K	110	0	Ultra-Low Offset Voltage	OP-07D	TI	
0.15	2	0.2	2.5	0.8 *	0.12 *	80K	104	0	Improved 108 A, Low Bias, Compensated	OP-12A	† PMI	
										OP-12E	PMI	
								1	Improved 108 A, Low Bias	OP-08A	† PMI	20
										OP-08E	PMI	
		2	0.9	0.5 *	0.1	500K	114	0	Ultra Low Noise	OP-05A	† Raytheon	
				0.6	0.17	300K	126	0	Low Bias, Low Drift	OP-05A	† Intersil	
				1.2 *	0.25 *	300K	114	0	Instrumentation	OP-05A	† Micro Pwr	
										MP5505A	**† Micro Pwr (401,3292)**	
										OP-05A	† PMI	
	5	1	3	0.25 *	0.1 *	1M	94	0	Ultra Low Offset Voltage, Low Drift	**AD517J**	**AD (3153)**	
										MP517J	Micro Pwr	
	7	6	0.2	0.4	0.2	100K	100	0	Ultra-Low Offset Voltage	OP-07C	TI	
			1.8	0.5 *	0.1	100K	100	0	Ultra Low Noise	OP-07C	Raytheon	30
				0.6 *	0.17 *	120K	100	0	Ultra Low Offset Voltage, Low Drift	**ADOP-07C**	**AD (3153)**	
										OP-07C	Intersil	
				1.2 *	0.25 *	120K	100	0	Ultra Low Offset Voltage, Low Drift	OP-07C	Micro Pwr	
										µA714C	Fairchild	
										MP5507C	**Micro Pwr (401,3292)**	
										OP-07C	PMI	
	7.0	6.0	0.5 *	0.5 *	0.17 *	120K	100	0	Low Noise	µPC354	NEC-Electron	
	12	6	2.5	0.5 *	0.1	100K	94	0	Ultra Low Noise	OP-07D	Raytheon	
				0.6 *	0.17 *	120K	94	0	Ultra Low Offset Voltage, Low Drift	**ADOP-07D**	**AD (3153)**	
										OP-07D	Intersil	40
				1.2 *	0.25 *	120K	94	0	Ultra Low Offset, Low Drift	**MP5507D**	**Micro Pwr (401,3292)**	
										OP-07D	PMI	
	35	20	2	0.4 *	0.5 *	1M	110	1	Low Drift	3510A	Burr-Brown	
0.17	85	90	2	4.5	11	50K	100	1	Ultra Low Noise	OP-34	PMI	
					17 *	500K	100		Ultra Low Noise	**MP5534**	**Micro Pwr (401,3292)**	
				5	1.7	50K	100	1	Ultra Low Noise	OP-24	PMI	
					2.8 *	500K	100		Ultra Low Noise	**MP5524**	**Micro Pwr (401,3292)**	
0.20	7	6	0.7 *	1.2 *	0.25 *	400K	—	0	Ultra Low Offset Voltage	OP-207E	PMI	
										OP-207F	PMI	
	10	3	3	0.2 *	—	1M	114	0	Precision Instrumentation	LM363	National	50
	15	15	2	0.3 *	0.1 *	1-1000	80	0	Instrumentation	AD522B	AD	
	20	5	3	1.2 *	0.25	300K	110	0	Precision, Instrumentation	**CA3193A**	**RCA (3351)**	
	25	2.5	5	0.1 *	—	400K	100	0	Precision, Low Power	OP-20C	† PMI	
										OP-20G	PMI	
		20	6	0.3 *	0.1 *	1-1000	75	0	Instrumentation	AD522S	† AD	
	100	2	5	0.1 *	1 *	1-1024	74	0	Instrumentation	AD612A	AD	
											(Continued)	

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR—Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift µV/°C	Bandwidth MHz	Slew Rate V/µs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source	Line
Single Units											**(Cont'd)**	
0.20	100	2	5	0.1 *	1 *	1-1024	74	0	Instrumentation		(Cont'd)	
										AD612B	AD	
										AD612C	AD	
										AD614A	AD	
										AD614B	AD	
	200	20	0.5	0.6 *	0.25	1.5M	105 *	0	Precision, Low Power	OP-21C	† PMI	
										OP-21G	PMI	
0.25	0.00015	0.00004	5	0.5 *	0.3	—	80	—	Ultra Low Bias FET	3528B	Burr-Brown	
	0.001	0.0002	2	1 *	0.9	100K	76	1	Low Bias, FET Input	OPA105WM/ MIL	† Burr-Brown	
						200K	76	1	Low Drift, Low Bias FET	OPA103DM	Burr-Brown	
			5	1 *	0.9	100K	76	1	Low Bias, FET Input	OPA105VM	† Burr-Brown	10
						200K	76	1	Low Drift, Low Bias FET	OPA103CM	Burr-Brown	
			25	1 *	0.9	100K	76	1	Low Bias, FET Input	OPA105UM	† Burr-Brown	
		0.0005	3	0.7 *	0.3	40K	76	0	Precision, Low Drift FET	**AD545M**	**AD (3153)**	
	0.002	0.0003 *	5	1 *	0.6	100K	76 *	0	Low Drift FET	3527B	Burr-Brown	
	0.010	0.002 *	1	1.5 *	0.6	100K	90 *	0	Ultra Low Drift FET	3521L	Burr-Brown	
		0.004	5 *	10	6.5 *	50K	105	0	Low Noise, Wideband JFET	OPA101BM	Burr-Brown	
										OPA102BM	Burr-Brown	
	0.015	0.002 *	2	1.5 *	0.6	100K	90 *	0	Ultra Low Drift FET	3521K	Burr-Brown	
	0.020	0.020 *	5	1.5 *	0.6	50K	90 *	0	Ultra Low Drift FET	3521J	Burr-Brown	
										3521R	† Burr-Brown	20
	0.025	0.002	1	1	3	250K	80	2	Ultra Low Drift BIFET	**AD547L**	**AD (3151,3153)**	
	2	2	0.6	0.5 *	0.1	150K	110	0	Ultra Low Noise	OP-07A	† Raytheon	
				2.5 *	0.5	1M	100	0	Ultra Low Drift	AM-430B	Datel	
	40	35	—	63 *	11 *	—	—	0	Low Noise, High Slew Rate	OP-37E	Raytheon	
	50	0.005	5	5 *	30 *	60K	80	—	High Speed, Low Drift FET	**AD381L**	**AD (3155)**	
		35	0.5	—	5	1000	90	0	Precision Instrumentation	**AD524A**	**AD (3158)**	
	100	—	1	0.25	5	1K	100	0	Precision Instrumentation	**AD624A**	**AD (3156,3158)**	
0.30	0.050	0.010	1 *	1 *	0.3	100K	110	0	Improved 108 A, Low Power	LM11	† National	
	0.1	0.03	5	3	10	100K	90	—	Precision JFET	MA337	Analog Sys	
	2	0.00004	10	0.035 *	2.2 *	100K	80	0	Ultra Low Bias FET	OPA104CM	Burr-Brown	30
		0.2	3.5	0.8 *	0.12 *	80K	104	0	Improved 108 A, Low Power, Compensated	OP-12B	† PMI	
										OP-12F	PMI	
								1	Improved 108 A, Low Power	OP-08B	† PMI	
										OP-08F	PMI	
	25	2	5	0.1 *	—	500K	90	0	Precision, Low Power	OP-20H	PMI	
	1000	200	2	20	10	10K	90	1	Precision, Bipolar	MA327	Analog Sys	
0.35	2	2	0.2	3.5	0.12 *	300K	104		Low Bias Current	**MP5512**	**Micro Pwr (401,3292)**	
	3	2	0.2	2.5	0.12 *	300K	104		Low Bias Current	**MP5508**	**Micro Pwr (401,3292)**	
0.4	5	1	1.5	0.25	0.08	900K *	82	0	Programmable Micropower	OP-22A	PMI	
0.40	25	20	6	0.3 *	0.1 *	1-1000	75	0	Instrumentation	AD522A	AD	40
0.5	0.000075	0.00002	10	0.5 *	0.3	—	70	—	Ultra Low Bias FET	3528C	Burr-Brown	
	0.0001	0.00005	25	1 *	0.6	100K	80 *	0	Ultra Low Bias FET	3523L	Burr-Brown	
	0.00015	0.00008	15	0.035 *	2.2 *	100K	66	0	Ultra Low Bias FET	OPA104BM	Burr-Brown	
	0.00025	0.0001	25	1 *	0.6	100K	80 *	0	Ultra Low Bias FET	3523K	Burr-Brown	
	0.0003	0.00008	10	0.5 *	0.3	—	66	—	Ultra Low Bias FET	3528A	Burr-Brown	
	0.001	0.0001	5	1 *	1.5	100K	80	0	Precision FET	LH0052	† National	
		0.0005	5	0.7 *	0.3	40K	76	0	Precision, Low Drift FET	**AD545L**	**AD (3153)**	
		0.002 *	15	1 *	1.3 *	200K	76	0	Low Drift, Low Bias FET	OPA103BM	Burr-Brown	
	0.002	0.003 *	25	1 *	1.3 *	200K	76	0	Low Drift, Low Bias FET	OPA103AM	Burr-Brown	
	0.005	0.0003 *	2	1 *	0.6	100K	76 *	0	Ultra Low Drift FET	3527C	Burr-Brown	50
			10	1 *	0.6	100K	76 *	0	Low Drift FET	3527A	Burr-Brown	
		0.001 *	25	1 *	0.6	50K	90 *	0	Low Offset FET	3522K	Burr-Brown	
										3522S	Burr-Brown	
	0.020	0.002 *	10	1.5 *	0.6	50K	90 *	0	Ultra Low Drift FET	3521H	Burr-Brown	
	0.025	0.002	2	1	3	250K	80	2	Ultra Low Drift BIFET	**AD547K**	**AD (3151,3153)**	
			5	1	3	250K	80	2	Ultra Low Drift BIFET	**AD547S**	**AD (3151,3153)**	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift µV/°C	Band-width MHz	Slew Rate V/µs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source	Line
Single Units											**(Cont'd)**	
											(Cont'd)	
0.5	0.025	0.002	5	2.0	17 *	50K	80	0	High Speed Precision Bipolar JFET	**AD544L**	**AD (3153)**	
				5 *	30 *	40K	80	1	High Speed, Low Drift FET	**AD382T**	**†AD (3155)**	
						60K	80	—	High Speed, Low Drift FET	**AD381T**	**†AD (3155)**	
			10	5 *	30 *	40K	80	1	High Speed, Low Drift FET	**AD382K**	**AD (3155)**	
						60K	80	—	High Speed, Low Drift FET	**AD381K**	**AD (3155)**	
		0.010	5	1.0 *	3	200K	80	0	Precision Bipolar JFET	**AD542L**	**AD (3153)**	
		0.03	0.03	5 *	0.11	5	100K	100	Precision JFET Input	**HA-5170-2**	**†Harris (3270,3287)**	
	0.035	0.002	5	1.5 *	300 *	10K	80	1	Wideband, Fast Settling	OPA605C	Burr-Brown	
										OPA605K	Burr-Brown	
			10	1.5 *	300 *	10K	80	1	Wideband, Fast Settling	OPA605B	Burr-Brown	10
										OPA605J	Burr-Brown	
	0.050	0.01	5	—	45	100K	86	—	Wideband, Decompensated, Settles to 0.01% in 1.5 µs	OP-17A	† Micro Pwr	
										OP-17E	Micro Pwr	
										OP-17A	† PMI	
										OP-17E	PMI	
				14 *	10	100K	86	0	Bipolar-JFET, Bias Comp.	OP-15A	† Micro Pwr	
										OP-15E	Micro Pwr	
										OP-15A	† PMI	
										OP-15E	PMI	
				19 *	18	100K	86	0	Wideband-JFET, Bias Comp.	OP-16A	† Micro Pwr	20
										OP-16E	Micro Pwr	
										OP-16A	† PMI	
										OP-16E	PMI	
			5 *	0.8 *	40	60K	86	1	Wideband-JFET, Comp. for G>10	**HA-5110-2**	**†Harris (3262,3287)**	
				18 *	12 *	75K	86	0	Wideband-JFET	**HA-5100-2**	**†Harris (3260,3287)**	
										HA-5100-5	**Harris (3260,3287)**	
			10 *	0.8 *	40	60K	86	0	Wideband-JFET, Comp. for G>10	**HA-5110-5**	**Harris (3262,3287)**	
		0.025	10	1	1	50K	80	0	Low Power BIFET	**LF441A**	**National (3309,3313)**	
				3	10	50K	80	0	Wideband JFET	**LF411A**	**National (3309,3311)**	
		0.06	0.06	5 *	0.11	7	80K	90	Precision JFET Input	**HA-5170-5**	**Harris (3270,3287)**	30
	0.1	—	50	15 *	150 *	100K	90	1	High Speed, High Power	1461-83	† Teledyne P	
	0.10	0.02	5 *	2.5 *	5 *	50K	85	0	Bipolar—JFET	LF155	† AMD	
										LF155	† Intersil	
										LF155	† Motorola	
										PM155	† PMI	
	0.15	0.006	10 *	10 *	6.5 *	50K	105	0	Low Noise, Wideband JFET	OPA101AM	Burr-Brown	
										OPA102AM	Burr-Brown	
	0.2	0.1	10 *	3 *	13 *	50K	70	0	Low Offset JFET	**TL087M**	**†TI (3424)**	
	0.4	0.05	10 *	3 *	13 *	25K	70	0	Low Offset JFET	**TL087C**	**TI (3424)**	
	1	0.2	5 *	0.11	4	1M	90	1	Low Bias Current, Low Power	**HA-5180A-2**	**Harris (3272,3287)**	40
										HA-5180A-5	**Harris (3272,3287)**	
	2	0.2	5	1 *	0.3 *	80K	96	1	Precision Bipolar, Low Bias	LM108A	† AMD	
										LM208A	AMD	
										AD108A	**†AD (3153)**	
										AD208A	**AD (3153)**	
										µA108AM	† Fairchild	
										µA208AM	Fairchild	
										LM108A	**†Harris (3286,3288)**	
										LM108A	† Intersil	
										LM108A	† Motorola	50
										LM208A	Motorola	
										LM108A	† National	
										LM208A	National	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift µV/°C	Band-width MHz	Slew Rate V/µs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source	Line
Single Units											**(Cont'd)**	
0.5	2	0.2	5	1 *	0.3 *	80K	96	1	Precision Bipolar, Low Bias		(Cont'd)	
										PM108A	† PMI	
										PM208A	PMI	
										SG108A	† Silicon G	
										SG208A	Silicon G	
										SFC2108A	† Thomson-CSF	
										SFC2208A	Thomson-CSF	
	3	2.8	1	0.6	0.1	200K	114	0	Low Bias, Low Drift	OP-05	† Intersil	
			2	0.5 *	0.1	500K	114	0	Ultra Low Noise	OP-05	† Raytheon	
				0.6	0.25 *	200K	110	0	Instrumentation	**MP5505B**	**† Micro Pwr (401,3292)**	
										OP-05	† Micro Pwr	10
										OP-05	† PMI	
	4	3.8	0.9	0.5 *	0.1	500K	110	0	Ultra Low Noise	OP-05E	Raytheon	
			1.5	0.6	0.1	200K	123	0	Low Bias, Low Drift	OP-05E	Intersil	
			2	0.6	0.25 *	200K	107	0	Instrumentation	**MP5505E**	**Micro Pwr (401,3292)**	
										OP-05E	Micro Pwr	
										OP-05E	PMI	
	7	1	5	1 *	0.3 *	80K	96	1	Precision Bipolar	LM308A	AMD	
										AD308A	**AD (3153)**	
										µA308AC	Fairchild	
										LM308A	**Harris (3286,3288)**	20
										LM308A	Intersil	
										LM308A	Motorola	
										LM308A	National	
										PM308A	PMI	
										SG308A	Silicon G	
	30	2	8	0.8	0.25	100K	85	0	General Purpose	**MP5502A**	**† Micro Pwr (401,3292)**	
										MP5502E	**Micro Pwr (401,3292)**	
										OP-02A	† Micro Pwr	
										OP-02E	Micro Pwr	
		5	5	1 *	0.25 *	80K	90	1	High Accuracy 301	**AD301AL**	**AD (3153)**	30
	35	2	8	0.8	0.25	100K	90	0	General Purpose	OP-02A	† PMI	
										OP-02E	PMI	
	40	10	5	1.2 *	0.25 *	100K	100	0	Precision, Instrumentation	**CA3193**	**RCA (3351)**	
										CA3493	**RCA (3351)**	
	50	5	2 *	1.3	1.2 *	100K	—	1	High Performance BIFET	OP19A	† PMI	
										OP19E	PMI	
				5 *	5.5 *	100K	—	1	High Performance BIFET	OP18A	† PMI	
										OP18E	PMI	
			5	1 *	0.5 *	50K	90	0	Higher Accuracy 741	**AD741L**	**AD (3153)**	
		30	1	1.5 *	0.8	100K *	100 *	0	Low Drift	3500E	Burr-Brown	40
	75	5	2	1	0.005 *	1000K	110	4	High Accuracy Instrumentation	µA725AM	† Fairchild	
	80	5	1	—	—	1000K	120	4	Instrumentation	SSS725	PMI	
			2	—	0.01	1000K	120	4	High Gain Instrumentation	OP-06B	† PMI	
										OP-06F	PMI	
		10	0.5	0.3 *	0.12 *	1000K	110	1	Precision Low Noise	**AD504M**	**AD (3153)**	
			1.0	0.3 *	0.12 *	1000K	110	1	Precision Low Noise	**AD504L**	**AD (3153)**	
										AD504S	**†AD (3153)**	
	300	30	0.5	0.6 *	0.25 *	1000K	100	0	Precision Low Power	OP-21H	PMI	
	500	200	15	0.3	—	—	72	0	Instrumentation	HC3020	HyComp	
0.6	0.100	0.01	5	1 *	0.3 *	100K	110	0	Precision, Low Input Current	LM11C	National	50
	7.5	2	2.0	0.25	0.08	500K *	80	0	Programmable Micropower	OP-22B	PMI	
0.7	30	2	5	2.5 *	18 *	50K	90	0	High Speed	**MP5501A**	**Micro Pwr (401,3292)**	
										MP5501H	**†Micro Pwr (401,3292)**	
										OP-01A	† Micro Pwr	
										OP-01H	Micro Pwr	
										OP-01A	† PMI	
										OP-01H	PMI	

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift µV/°C	Band-width MHz	Slew Rate V/µs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source	Line
Single Units											**(Cont'd)**	
0.75	3	2.8	1.3	0.5 *	0.1	150K	110	0	Ultra Low Noise	OP-07	† Raytheon	
	4	3.8	1.3	0.5 *	0.1	150K	106	0	Ultra Low Noise	OP-07E	Raytheon	
		4	1.3	2.5 *	0.5	1M	100	0	Ultra Low Drift	**AM-430A**	**Datel (2622)**	
										AM-430M	† Datel	
	80	5	—	0.44 *	0.3	50K	80	0	High Performance	µA741EC	Fairchild	
				1 *	0.3 *	50K	80	0	High Performance	µA741AM	† Fairchild	
			2.8 *	—	—	1000K	110	4	High Performance 725	SSS725B	AMD	
1.0	0.000075	—	25	0.35	0.3	50K	70	0	FET Electrometer	AD515L	AD	
	0.00015	—	15	0.35	0.3	100K	80	0	FET Electrometer	AD515K	AD	
	0.0003	0.00008	25	0.035 *	2.2 *	100K	66	0	Ultra Low Bias FET	OPA104AM	Burr-Brown	10
	0.0005	0.0002	50	1 *	0.6	100K	80 *	0	Ultra Low Bias FET	3523J	Burr-Brown	
	0.001	0.0005	15	0.7 *	0.3	40K	70	0	Precision Low Drift FET	**AD545K**	**AD (3153)**	
	0.002	0.001	25	0.7 *	0.3	20K	66	0	Precision Low Drift FET	**AD545J**	**AD (3153)**	
	0.005	—	10	1 *	3	75K	80	0	High Accuracy, FET	AD506L	AD	
				2 *	3	50K	72	0	Low Bias Current, FET	1425-02	Teledyne P	
			25	2 *	3	50K	72	0	Low Bias Current, FET	1425-01	Teledyne P	
		0.0002	10	1 *	1	75K	76	0	Precision FET	**LH0052C**	**National (3342)**	
	0.010	—	25	2 *	3	50K	72		Low Drift, FET	1426-01	Teledyne P	
		0.002 *	50	1 *	0.6	50K	90 *	0	Low Offset FET	3522J	Burr-Brown	
		0.005 *	25	10 *	65	25K	70 *	0	Fast Settling, 1 µs to 0.01%	3550J	Burr-Brown	20
										3550S	† Burr-Brown	
				20 *	100	25K	70 *	0	Fast Settling, 0.6 µs to 0.01%	3550K	Burr-Brown	
	0.015	—	25	10 *	50	50K	80	0	Fast Wide Band, High Accuracy, FET Input	AD528K	AD	
									Fast Wideband, High Accuracy, FET Input	AD528S	† AD	
	0.025	—	5	2 *	3	50K	72	0	Low Drift, FET	1426-03	Teledyne P	
			10	2 *	3	50K	72	0	Low Drift, FET	1426-02	Teledyne P	
		0.002	10	2	16	50K	80	0	High Speed Precision Bipolar JFET	**AD544K**	**† AD (3153)**	
				5 *	30 *	40K	80	1	High Speed, Low Drift FET	**AD382S**	**† AD (3155)**	
						60K	80	—	High Speed, Low Drift FET	**AD381S**	**† AD (3155)**	
			15	2	16	50K	80	0	High Speed Precision Bipolar JFET	**AD544S**	**AD (3153)**	30
		0.01	10	1.0 *	3	50K	76	0	Precision Bipolar JFET	**AD542S**	**† AD (3153)**	
						200K	80	0	Precision Bipolar JFET	**AD542K**	**AD (3153)**	
	0.035	0.002	25	1.5 *	300 *	10K	70	1	Wideband, Fast Settling	OPA605A	Burr-Brown	
										OPA605H	Burr-Brown	
		0.005	5	1	3	100K	76	2	Ultra Low Drift BIFET	**AD547J**	**AD (3151,3153)**	
	0.05	0.005	15	5 *	30 *	40K	76	1	High Speed, Low Drift FET	**AD382J**	**AD (3155)**	
						60K	76	—	High Speed, Low Drift FET	**AD381J**	**AD (3155)**	
	0.050	0.01	5 *	18 *	8 *	150K *	86 *	0	Wideband, FET	AM-410-2M	† Datel	
				60 *	50 *	150K *	94 *	0	Wideband, FET	AM-411-2M	† Datel	
			15	70	1000	100K	44	1	150 ns Settling to 0.05%	3554B	Burr-Brown	
						30K	60	1	Wideband, Fast Settling FET	**AD3554B**	**AD (3155)**	40
			25	70	1000	100K	44	1	150 ns Settling to 0.05%	3554S	Burr-Brown	
						30K	60	1	Wideband, Fast Settling FET	**AD3554S**	**† AD (3155)**	
	0.10	0.01	50	50 *	250 *	100K	70 *	1	Wideband, Fast Settling	3551J	Burr-Brown	
										3551S	† Burr-Brown	
		0.02	—	35	75K	86	—	0	Wideband-JFET, Bias Comp.	OP-17B	† Micro Pwr	
										OP-17F	Micro Pwr	
			10	—	35	75K	86	—	Wideband, Decompensated, Settles to 0.01% in 1.5 µs	OP-17B	† PMI	
										OP-17F	PMI	
				13 *	7.5	75K	86	0	Bipolar-JFET, Bias Comp.	OP-15B	† Micro Pwr	50
										OP-15F	Micro Pwr	
										OP-15B	† PMI	
										OP-15F	PMI	
				18 *	12	75K	86	0	Wideband-JFET, Bias Comp.	OP-16B	† Micro Pwr	
										OP-16F	Micro Pwr	
										OP-16B	† PMI	
										OP-16F	PMI	
			20	40	330 *	25K	60	1	Wideband, Fast Settling	**AD380K**	**AD (3155)**	
										AD380L	**† AD (3155)**	
										AD380S	**AD (3155)**	60

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† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift µV/°C	Band-width MHz	Slew Rate V/µs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source	Line
Single Units											**(Cont'd)**	
1.0	0.10										(Cont'd)	
		0.05	5 *	18 *	12 *	60K	80	0	Wideband-JFET	**HA-5105-5**	**Harris (3260,3287)**	
		0.05 *	15 *	0.6 *	35 *	50K	80	1	Wideband-JFET, Comp. for G>10	**HA-5115-5**	**Harris (3262,3287)**	
	0.30	0.02	15	40 *	220 *	25K	60	1	Wideband, Fast Settling	1437	Teledyne P	
										1437-80	† Teledyne P	
	2	100	10	30	300 *	100K	70	2	Low Offset, Fast Settling	**HOS-060**	**† AD (3152,3155)**	
										HOS-060/883	**† AD (3152,3155)**	
	5	0.5	10	0.8 *	0.12 *	40K	84	0	Precision, Low Input Current	OP-12C	† PMI	
										OP-12G	PMI	
								1	Precision, Low Input Current	OP-08C	† PMI	
										OP-08G	PMI	10
	15	7 *	3	1.5 *	1	45K	100 *	0	Low Bias, Low Noise	3500C	Burr-Brown	
			5	1.5 *	1	45K	100 *	0	Low Bias, Low Noise	3500T	† Burr-Brown	
	100	20	4 *	1 *	0.25 *	30K	70	2	High Voltage	LH0004	† National	
			5	—	—	1000K	110	4	Instrumentation	µPC154	NEC-Electron	
										PM725	† PMI	
				0.5 *	0.01 *	1000K	110	4	Instrumentation	RM725	† Raytheon	
				1 *	0.005 *	1000K	110	4	High Accuracy Instrumentation	µA725M	† Fairchild	
										LM725	† National	
	200	50	6	1 *	0.4 *	25K	80	3	General Purpose	RM709A	† Raytheon	
	250	70	20	—	—	20K	70	1	General Purpose	TA7502B	Toshiba	20
1.2	0	3	2.0	0.35	0.08	250K *	80	0	Programmable Micropower	OP-22H	PMI	
1.3	7	6	2	0.5 *	0.1	400K	100	0	Ultra Low Noise	OP-05C	Raytheon	
			2.0	0.6	0.17	120K	100	0	Low Bias, Low Drift	OP-05C	Intersil	
			4.5	1.2 *	0.25 *	120K	100	0	Instrumentation	MP5505C	Micro Pwr	
										OP-05C	Micro Pwr	
										OP-05C	PMI	
							120	0	Instrumentation	µPC254	NEC-Electron	
	110	13	1.4 *	—	0.01	500K	110	4	High Gain Instrumentation	OP-06G	PMI	
			4.5	—	—	500K	100	4	Instrumentation	SSS725C	PMI	
1.5	0.010	—	25	1 *	3	50K	80	0	High Accuracy, FET	**AD506K**	**AD (3153)**	30
			50	1 *	3	50K	80	0	High Accuracy, FET	**AD506S**	**† AD (3153)**	
	0.10	0.05	15 *	18 *	8 *	100K *	86 *	0	Wideband, FET	**AM-410-2C**	**Datel (2622)**	
				50 *	40 *	100K *	94 *	0	Wideband, FET	**AM-411-2C**	**Datel (2622)**	
	80	5	2	0.5 *	0.005 *	1000K	120	4	Instrumentation	LM725A	National	
	100	15	3	0.3 *	0.12 *	500K	100	1	Low Drift, Low Noise	**AD504K**	**AD (3153)**	
	120	45	4 *	1 *	0.25 *	30K	70	2	High Voltage	LH0004C	National	
2.0	0.001	0.0007	4 *	0.5 *	0.5 *	20K	55	0	Low Supply Voltage, BIMOS	**CA3420B**	**† RCA (3352)**	
	0.010	—	50	2 *	3	50K	72	—	Low Bias Current, FET	1425	Teledyne P	
		0.0005 *	15	1 *	3	50K	70	0	Low Offset Voltage, FET	ICL8007	† Intersil	
	0.02	—	50	100	1000	100K	90	1	Fast-Settling, FET Input	1443-83	† Teledyne P	40
	0.025	—	50	2	3	50K	72	0	Low Drift, FET	1426	Teledyne P	
	0.025 *	0.010 *	20	1.0 *	3	50K	76	0	Precision Bipolar JFET	**AD542J**	**AD (3153)**	
	0.030	0.01	4 *	0.063 *	0.03 *	32K	75	0	Manopower, BIMOS	**CA3440B**	**RCA (3353)**	
	0.05	0.01	50	70	1000	100	60	1	Wideband, Fast Settling FET	**AD3554A**	**AD (3155)**	
	0.050	0.005	20	2	15	30K	74	0	High Speed Precision Bipolar JFET	**AD544J**	**AD (3153)**	
		0.01	5	—	40	50K	85	—	Wideband Decompensated	LF357A	AMD	
										LF157A	**† Harris (3286,3288)**	
										LF357A	**Harris (3288)**	
										LF157A	† Intersil	
										LF357A	Intersil	50
										LF157A	† Motorola	
										LF357A	Motorola	
										LF157A	**† National (3309)**	
										LF357A	**National (3309)**	
										PM157A	† PMI	
										PM357A	PMI	
				2.5 *	3	50K	85	0	Bipolar - JFET	LF155A	† AMD	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift µV/°C	Band-width MHz	Slew Rate V/µs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source	Line
Single Units											**(Cont'd)**	
2.0	0.050	0.01	5	2.5 *	3	50K	85	0	Bipolar - JFET		(Cont'd)	
										LF355A	AMD	
										LF155A	† Intersil	
										LF355A	Intersil	
										LF155A	† Motorola	
										LF355A	Motorola	
										LF155A	**† National (3309)**	
										LF355A	**National (3309)**	
										PM155A	† PMI	
										PM355A	PMI	
				4	10	50K	85	0	Wideband - JFET	LF156A	† AMD	10
										LF356A	AMD	
										LF156A	**† Harris (3286,3288)**	
										LF356A	**Harris (3288)**	
										LF156A	† Intersil	
										LF356A	Intersil	
										LF156A	† Motorola	
										LF356A	Motorola	
										LF156A	**† National (3309)**	
										LF356A	**National (3309)**	
										PM156A	† PMI	20
										PM356A	PMI	
			50	70	1000	100K	44	1	150 ns Settling to 0.05%	3554A	Burr-Brown	
		0.03	10 *	1	1.6	80K *	70	0	Low Power	ICL7611AC	Intersil	
										ICL7611AM	† Intersil	
									Low Power, Extended CMVR	ICL7612AC	Intersil	
										ICL7612AM	† Intersil	
									Low Power, Input Protected	ICL7613AC	Intersil	
								1	Low Power	ICL7614AC	Intersil	
										ICL7614AM	† Intersil	
									Low Power, Input Protected	ICL7615	† Intersil	30
										ICL7615AC	Intersil	
	0.075	0.025	10 *	4 *	13 *	50K	80	0	Precision BIFET	**MC35001A**	**† Motorola (3293)**	
	0.10	0.05	10 *	4 *	13 *	50K	80	0	Precision BIFET	**MC34001A**	**Motorola (3293)**	
									Wideband Bipolar JFET	**LF351A**	**National (3309)**	
			20	150	400	10K	60	3	Fast Settling, Wideband	OPA600N	Burr-Brown	
										OPA600V/ 883B	† Burr-Brown	
										OPA600V/ MIL	† Burr-Brown	
		0.05 *	40	0.5 *	3	50K	80	1	High Current, High Power	3571A	Burr-Brown	
										3572A	Burr-Brown	
		0.050	10 *	3 *	13 *	50K	80	0	Bipolar JFET	µAF771A	Fairchild	40
										µAF771AM	† Fairchild	
	0.15	0.05	20	0.06	10	3K	100	—	JFET Input	MA403	Analog Sys	
	0.20	0.10	20	2.7	8	25K	70	0	Wideband JFET	**LF411**	**National (3309,3311)**	
			20 *	3	10	50K	80	0	Wideband Bipolar JFET	LF151A	† National	
	0.50	—	75	60 *	500	200K	—	0	Inverting, Settles to 0.01% in 200 ns	1430	Teledyne P	
										1430-83	† Teledyne P	
	2	0.2	15	0.3 *	0.3 *	50K	85	1	Low Noise 108	ICL108LN	† Intersil	
				1 *	0.2 *	50K	85	0	Micropower, Supply Current 600 µa	LM112	† National	
										LM212	National	
					0.3 *	50K	85	1	Precision Bipolar	LM108	† AMD	50
										LM208	AMD	
										AD108	† AD	
										AD208	**AD (3153)**	
										µA108M	† Fairchild	
										µA208M	Fairchild	
										LM108	† Harris	
										LM108	† Intersil	
										LM108	† Motorola	
										LM208	Motorola	
										LM108	† National	60
										LM208	National	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift µV/°C	Band-width MHz	Slew Rate V/µs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source	Line
Single Units											**(Cont'd)**	
2.0	2	0.2	15	1 *	0.3 *	50K	85	1	Precision Bipolar		(Cont'd)	
										PM108	† PMI	
										PM208	PMI	
										SG108	† Silicon G	
										SG208	Silicon G	
										SFC2108	† Thomson-CSF	
										SFC2208	Thomson-CSF	
	3	2	10	0.5 *	0.1	45K	100 *	0	Low Bias Current	3501C	Burr-Brown	
	5	0.5	10	—	1.7 *	2.5K	80	3	Wideband	µA702M	† TI	
	7	3	10	0.5 *	0.1	45K	100 *	0	Low Bias Current	3501B	Burr-Brown	
										3501S	† Burr-Brown	10
	10	5	10 *	50 *	60 *	50K	86	0	Wideband-JFET	HA-5150	Harris	
	20	0.7	2.0 *	—	—	60K	89	0	Op Amp and Voltage Reference	LM10BL	National	
						120K	93	0	Op Amp and Voltage Reference	**MCELM10**	**Micro Eng (4440)**	
										LM10	† National	
										LM10B	National	
		10 *	5	1.5 *	1	45K	100 *	0	Low Bias, Low Noise	3500B	Burr-Brown	
			10	1.5 *	1	45K	100 *	0	Low Bias, Low Noise	3500S	† Burr-Brown	
	25	3	15	0.5	0.5 *	50K	80	1	Low Offset Current	µA777M	† TI	
	50	5	—	—	—	100K	80	0	High Performance 741	SSS741	† AMD	
			8	2.5 *	18 *	50K	80	0	High Speed	**MP5501E**	**Micro Pwr (401,3292)**	20
										MP5501F	**† Micro Pwr (401,3292)**	
										OP-01E	Micro Pwr	
										OP-01F	† Micro Pwr	
										OP-01E	PMI	
										OP-01F	† PMI	
			10	0.8	0.25	50K	90	0	General Purpose	MP5502	† Micro Pwr	
										OP-02	† Micro Pwr	
										OP-02C	Micro Pwr	
										OP-02	PMI	
										OP-02C	PMI	30
		10	—	—	—	100K	80	0	High Performance 741	222741	† AMD	
			15	4 *	1.5	25K	80	0	High Performance, High Gain	RM4131	† Raytheon	
	60	6	4 *	1.3 *	1.2 *	50K	—	1	High Performance BIFET	OP-19B	PMI	
										OP-19F	PMI	
				5 *	5.5 *	50K	—	—	High Performance BIFET	OP-18B	PMI	
										OP-18F	PMI	
		10	15	—	40	50K	70	1	60 V/µs Comp. for g=5	SE538	† Signetics	
				3 *	25	50K	70	0	High Slew Rate	SE530	† Signetics	
	75	10	15	0.8 *	0.5 *	50K	80	1	Low Noise 101A	ICL101ALN	† Intersil	
				1 *	0.5 *	50K	80	0	General Purpose, Compensated	LM107	† Harris	40
										LM107	† Intersil	
										LM107	† Motorola	
										LM207	Motorola	
										LM107	† National	
										LM207	National	
										LM107	† Raytheon	
										SG107	† Silicon G	
										SG207	Silicon G	
										LM107	† TI	
										LM207	TI	50
										SFC2107	† Thomson-CSF	
										SFC2207	Thomson-CSF	
									Higher Accuracy 741	**AD741S**	**† AD (3153)**	
								1	General Purpose, Improved 101, Uncompensated	AD101A	† AD	
										AD201A	**AD (3153)**	
										µA101AM	† Fairchild	
										µA201AM	Fairchild	
										LM101A	† Harris	
										LM101A	† Motorola	
										LM201A	Motorola	60
										LM101A	† National	
										LM201A	National	
											(Continued)	

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift µV/°C	Band-width MHz	Slew Rate V/µs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source	Line
Single Units											**(Cont'd)**	
2.0	75	10	15	1 *	0.5 *	50K	80	1	General Purpose, Improved 101, Uncompensated		(Cont'd)	
										LM101A	† Raytheon	
										CA101A	† RCA	
										CA201A	RCA	
										SG101A	† Silicon G	
										SG201A	Silicon G	
										LM101A	† TI	
										LM201A	TI	
							90	0	Higher Accuracy 741C	**AD741K**	**AD** **(3153)**	
	200	50	10	5 *	0.3 *	25K	80	3	General Purpose	µA709AM	† Fairchild	
										MC1709A	† Motorola	10
										LM709A	† National	
										SFC2709A	† Thomson-CSF	
			25	—	0.3 *	45K *	80	3	General Purpose	µA709AM	† TI	
	800	200	—	10 *	13 *	50K	80	1	Wideband, Low Noise	**XR5534M**	**† Exar** **(3209)**	
										RM5534	† Raytheon	
										SE5534	† Signetics	
										SE5534A	† Signetics	
										SE5534	† TI	
	4000	1500	1.2 *	15 *	3 *	0.7K	70	1	6 Volt, Wideband	CA3008A	RCA	
										CA3010A	† RCA	20
										CA3029A	RCA	
										CA3037A	† RCA	
	6000	1600	1.2 *	50 *	7 *	2K	80	1	12 Volt, Wideband	CA3015A	† RCA	
										CA3016A	† RCA	
										CA3030A	RCA	
										CA3038A	† RCA	
2.5	125	35	2 *	1 *	0.005 *	250K	94	4	High Accuracy Instrumentation	µA725C	Fairchild	
										LM725C	National	
										µPC725	NEC-Electron	
										PM725C	PMI	30
										RC725	Raytheon	
			3	—	—	250K	96	4	725 Type	µPC154A	NEC-Electron	
	200	40	5	0.3 *	0.12 *	250K	94	1	Low Drift, Low Noise	**AD504J**	**AD** **(3153)**	
		75	2 *	8 *	1	100K	86	0	High Performance	HS3546RH	† Harris	
	250	50	10 *	1 *	0.25 *	100K	90	2	High Gain Instrumentation, 50 mA	LH0020	† National	
3	20	5	—	0.85 *	0.55	80K	80	0	Low Power, Radiation Resistant	HS3530RH	† Harris	
	100	100	—	10	22	10K	80	1	High Slew Rate, Wideband	HS3511RH	† Harris	
3.0	0.0003	—	50	0.35	0.3	40K	66	0	FET Electrometer	AD515J	AD	
	0.020	0.020 *	25	3 *	20 *	100K	110 *	0	High Voltage FET	3582J	Burr-Brown	
				5	20 *	50K	110 *	0	High Voltage FET	3581J	Burr-Brown	40
				5 *	20 *	400K	110 *	0	High Voltage FET	3583	Burr-Brown	
				7 *	—	1000K	110 *	2	High Voltage FET	3584	Burr-Brown	
	0.030	—	50	10 *	50	25K	70	0	Fast Wideband, High Accuracy FET	AD528J	AD	
		0.01	10 *	5 *	13	200K	86 *	0	FET Input, Bipolar/MOS Output	**CA081B**	**RCA** **(3348)**	
								1	FET Input, Bipolar/MOS Output	**CA080B**	**RCA** **(3348)**	
	0.040	0.02	10 *	5 *	13 *	50K	80	0	FET Input, Bipolar/MOS Output	**CA081AT**	**† RCA** **(3348)**	
								1	FET Input, Bipolar/MOS Output	**CA080AT**	**† RCA** **(3348)**	
	0.05	—	75	90	900	56K	80	1	Fast-Settling, FET Input	1443	Teledyne P	
		0.01	10 *	1 *	100	75K	74	1	Wideband, High Slew Rate	**HA-5160-2**	**† Harris** **(3268,3287)**	
			20 *	1 *	100	75K	74	1	Wideband, High Slew Rate	**HA-5160-5**	**Harris** **(3268,3287)**	50
	0.050	0.015	—	1 *	0.3 *	40K	80	0	High Performance, Low Input Current	LM316A	AMD	
										LM316A	National	
	0.15	0.03	10	0.11	10	3K	90	—	Low Wideband Noise	MA344	Analog Sys	
	0.2	0.05	15	—	25	50K	82	—	Wideband, Decompensated, Settles to 0.01% in 1.6 µs	OP-17C	† PMI	
										OP-17G	PMI	
				12 *	5	50K	82	0	Bipolar-JFET, Bias Comp.	OP-15C	† Micro Pwr	
										OP-15G	Micro Pwr	
										OP-15C	† PMI	
										OP-15G	PMI	
				17 *	9	50K	82	0	Wideband-JFET, bias comp.	OP-16C	† Micro Pwr	60

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† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift µV/°C	Band-width MHz	Slew Rate V/µs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source	Line
Single Units											**(Cont'd)**	
3.0	0.2	0.05	15	17 *	9	50K	82	0	Wideband-JFET, bias comp.		(Cont'd)	
										OP-16G	Micro Pwr	
										OP-16C	† PMI	
										OP-16G	PMI	
				20	25	50K	82	—	Wideband, Decompensated, Settles to 0.01% in 1.6 µs	OP-17C	† Micro Pwr	
										OP-17G	Micro Pwr	
		0.1	10 *	1 *	3.5 *	4K	80	0	Low Power, Bipolar-JFET	**TL061BC**	**TI** **(3425)**	
					4 *	20K	80	0	Low Power, JFET Input	**HA-5062B-5**	**Harris** **(3252,3287)**	
				3 *	13 *	50K	80	0	Bipolar-JFET	**TL088C**	**TI** **(3424)**	
										TL088M	**†TI** **(3424)**	
				4	15 *	50K	80	1	JFET Input	**HA-5082B-5**	**Harris** **(3256,3287)**	10
	0.30	75	10 *	0.3	10	200K *	85	0	2.0 A Power	LH0101A	† National	
										LH0101AC	National	
	1	0.2	5 *	0.11	4	1M	90	1	Low Bias Current, Low Power	**HA-5180-2**	**Harris** **(3272,3287)**	
										HA-5180-5	**Harris** **(3272,3287)**	
	4	0.5	5	100	1000	1000K	0		Settles to 0.01% in 200 ns	AM-500GC	Datel	
										AM-500MC	Datel	
			7	100	1000	1000K	0	—	Fast Setting	AM-500MR	Datel	
			10	100	1000	1000K	0	—	Fast Setting	**AM-500MM**	**†Datel** **(2620)**	
	5	3	10 *	—	0.1 *	40K	80	0	Programmable Amplifier	HA-2720	† Harris	
	7.5	3	—	0.25 *	0.16 *	100K	70	0	Programmable	ICL4250	† Intersil	20
										LM4250	† National	
										SG4250	† Silicon G	
										UC4250	† Solitron	
	10	2	15	0.3 *	0.13 *	50K	80	0	Micropower	RM4132	† Raytheon	
				12 *	4	100K	80	0	High Impedance	**HA-2600**	**†Harris** **(3226,3287)**	
										HA2600	† Intersil	
		1000	50	1	500	300	80	2	High Slew Rate	MA207	Analog Sys	
	15	4	15	0.05	0.015	—	70	0	High Output, Low Power	MA112	Analog Sys	
		15	15	35 *	25	100K	80	1	Wideband, General Purpose	AD507K	AD	
	20	10	5 *	1 *	10	400K	86	0	Wide Response, Low Power	HA-2700	† Harris	30
										HA-2704	Harris	
	25	5	10 *	—	—	4K	60	3	Matched Transistors	LH0005A	† National	
	80	30	—	1 *	0.6	50K	80	0	to 500 mA, single supply	µA759	† Fairchild	
			15	0.4	0.3	50K	80	0	Higher Performance	LM741A	† National	
										LM741E	National	
								1	High Slew Rate Inverting	HA-2530	† Harris	
	200	50	20	1 *	0.5 *	50K	80	0	High Current	AD512K	AD	
									Higher Accuracy 741C	**AD741J**	**AD** **(3153)**	
			25	1 *	0.5 *	50K	80	0	High Current	AD512S	† AD	
	300	100	3 *	1 *	1.5 *	100K	70	1	0.2 A Power	LH0041	† National	40
			10	1 *	0.4 *	25K	70	3	High Gain	RM709	† Raytheon	
			25	1 *	1.5	100K	70	1	1.0 A Power	LH0021	† National	
	500	75	3 *	2 *	4.2 *	50K	80	2	General Purpose	MC1539	† Motorola	
	1000	200	10	40	20	100K	70	0	Low Noise, Wideband	MA322	Analog Sys	
		500	10	300	50	100K	90	2	Fast, Wideband	MA326	Analog Sys	
	2000	200	4	10 *	—	20K	70	0	General Purpose Wide Bandwidth	LH0003	† National	
										LH0003C	National	
3.5	0.015	—	75	1*	3	20K	70	0	High Accuracy, FET	**AD506J**	**AD** **(3153)**	
	12	2.5	6 *	—	0.04	150K	115 *	2	Micropower	RC3078A	† Raytheon	
4.0	0.010	0.002	10	1 *	1.5	100K	80	0	Micropower	**LH0022**	**†National** **(3342)**	50
	15	2	—	1 *	2.5 *	100K	80	0	High Performance	MC1556	Signetics	
			10 *	1 *	2.5 *	100K	80	0	High Performance	MC1556	Motorola	
		15	10 *	35 *	25	100K	80	1	Wide Band, High Impedance	HA-2620	† Harris	
										HA2620	† Intersil	
			20	35 *	20	100K	80	1	Wideband, General Purpose	AD507S	† AD	

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† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift µV/°C	Band-width MHz	Slew Rate V/µs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source	Line
Single Units											**(Cont'd)**	
4.0											(Cont'd)	
	25	12	15 *	4 *	5 *	100K	80	0	High Voltage	HA-2640	† Harris	
	30	2.0	5.0	—	—	40K	80	0	Op Amp and Voltage Reference	LM10CL	National	
						80K	90	0	Op Amp and Voltage Reference	LM10C	National	
	80	20	4 *	1 *	10	50K	70	0	High Slew Rate	SE535	† Signetics	
	200	50	15	12 *	10	50K	80	0	High Speed, Fast Setting	**AD518K**	**AD (3155)**	
			20	12 *	10	50K	80	0	High Speed, Fast Settling	AD518S	† AD	
	250	50	—	15 *	50	50K	80	0	Precision High Speed	LM118	† AMD	
										LM218	AMD	
										LM118	† Harris	
										LM118	† National	10
										LM218	National	
										LM118	† Raytheon	
										LM118	† TI	
										LM218	TI	
										SFC2118	† Thomson-CSF	
										SFC2218	Thomson-CSF	
	300	100	5 *	1 *	25	50K	70	1	0.5 A Wideband	LH0061	† National	
	350	100	3	—	0.5 *	50K	80	0	Short Circuit Protected	TBA222	† Siemens	
					5.5 *	50K	90	1	Adjustable Input Offset Voltage	TBC0748	† Siemens	
	700	100	10	—	—	25K	70	1	40mA Output	MA342	Analog Sys	20
			25	—	—	18K	70	1	20 mA Output	TAA762	† Siemens	
										TAA862	† Siemens	
	1500	300	—	10 *	6 *	25K	70	1	Low noise, Comp. for G=3	**XR5534**	**Exar (3209)**	
										XR5534C	**Exar (3209)**	
										RC5534	Raytheon	
										NE5534	Signetics	
										NE5534A	Signetics	
										NE5534	TI	
										NE5534A	TI	
					13 *	100K *	80	1	Low Noise, Comp. for G=3	AM-453-2C	Datel	30
										AM-453-2M	† Datel	
	30000	5000	20 *	70 *	400	4K	60 *	3	High Slew Rate	LH0024	† National	
4.5	170	32	6 *	—	0.04	—	110	2	Micropower	RC3078	Raytheon	
					0.04 *	25K	80	1	Micropower	CA3078	† RCA	
5.0	0.001	0.0005 *	25	1 *	0.6	50K	90 *	0	Low Offset FET	3522L	Burr-Brown	
	0.003	0.002	4 *	0.5 *	0.5 *	20K	70	0	Low Supply Voltage	**CA3420A**	**† RCA (3352)**	
	0.005	0.0006		2 *	50 *	—	80	0	Micropower, Transconductance Amplifier	CA3080	RCA	
										CA3080A	† RCA	
	0.025	0.002	25	15 *	50	50K	80	0	Precision, High Speed FET	LH0062	† National	
	0.030	0.02	6 *	4 *	10 *	50K	80	0	MOS-Bipolar	**CA3160A**	**† RCA (3349)**	40
			10 *	4 *	10 *	50K	80	1	MOS, Single Supply, Strobe	CA3130A	† RCA	
	0.040	0.02	0.063 *	0.03 *	10K	70	0	Manpower BIMOS				
										CA3440A	**RCA (3353)**	
			6 *	4.5 *	9 *	20K	70	0	MOS FET, Single Supply	**CA3140A**	**RCA (3350)**	
	0.050	0.030	15 *	1	1.6	80K *	70	0	Low Power	ICL7611BC	Intersil	
										ICL7611BM	† Intersil	
									Low Power, Extended CMVR	ICL7612BC	Intersil	
										ICL7612BM	† Intersil	
									Low Power, Input Protected	ICL7613BC	Intersil	
										ICL7613BM	† Intersil	
								1	Low Power	ICL7614BC	Intersil	50
										ICL7614BM	† Intersil	
									Low Power, Input Protected	ICL7615BC	Intersil	
										ICL7615BM	† Intersil	
	0.10	0.02	5 *	—	—	50K	85	—	Wideband Decompensated	LF257	AMD	
										LF157	**Harris (3286,3288)**	
										LF157	† Intersil	
										LF357B	Motorola	
										LF157	**† National (3309)**	
										LF257	**National (3309)**	
										LF357B	**National (3309)**	60

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift µV/°C	Band-width MHz	Slew Rate V/µs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source	Line
Single Units											**(Cont'd)**	
5.0	0.10	0.02	5 *	—	—	50K	85	—	Wideband Decompensated		(Cont'd)	
										PM157	† PMI	
										PM257	PMI	
				2.5 *	5 *	50K	85	0	Bipolar-JFET	LF255	AMD	
										LF255	Motorola	
										LF355B	Motorola	
										LF155	**† National (3309)**	
										LF255	**National (3309)**	
										LF355B	**National (3309)**	
										PM255	PMI	
				5 *	7,5 *	50K	85	0	Wideband-JFET	LF156	† AMD	10
										LF256	AMD	
										LF156	**Harris (3286,3288)**	
										LF156	† Intersil	
										LF156	† Motorola	
										LF256	Motorola	
										LF356B	Motorola	
										LF156	**† National (3309)**	
										LF256	**National (3309)**	
										LF356B	**National (3309)**	
										PM156	† PMI	20
										PM256	PMI	
		0.025	10	1	1	25K	70	0	Low Power-BIFET	**LF441**	**National (3309,3313)**	
			25 *	70 *	350	1K	50	2	Ultra Fast FET	TP0032	† Teledyne P	
									Ultra Fast-FET	ADLH0032	† AD	
										LH0032	† National	
		0.05	10 *	3 *	13 *	50K	80	0	Bipolar JFET	µ	Fairchild	
									Bipolar-JFET	µAF771B	Fairchild	
										µAF771BM	† Fairchild	
				4 *	13 *	50K	80	0	Precision-BIFET	**MC35001B**	**† Motorola (3293)**	
			80	150	400	10K	60	3	Fast Settling, Wideband	OPA600U	Burr-Brown	30
			100	150	400	10K	60	3	Fast Settling, Wideband	OPA600U/ 883B	† Burr-Brown	
	0.20	0.025	3 *	1 *	0.3 *	25K	96	0	Precision Bipolar	LM11CL	National	
		0.10	10 *	4 *	13 *	50K	80	0	Precision-BIFET	**MC34001B**	**Motorola (3293)**	
									Wideband Bipolar-JFET	**LF351B**	**National (3309)**	
					15 *	50K	100 *	0	Wideband Bipolar-JFET	LF151	† National	
	4	1	10	1 *	0.5 *	20K	80	0	Low Input Current 741	AD502L	AD	
	7	4	20	1 *	0.5 *	20K	80	0	Low Input Current 741	AD502K	AD	
	10	5	7 *	1 *	0.5 *	20K	70	0	Low Input Current	ICL8008M	† Intersil	
			10 *	—	0.1 *	25K	74	0	Programmable Amplifier	HA-2725	Harris	
			20 *	1 *	0.5 *	20K	80	0	Darlington 741	AD502S	† AD	40
		6	—	0.25 *	0.16 *	50K	70	0	Programmable	LM4250C	Harris	
										ICL4250C	† Intersil	
										LM4250C	† National	
										SG4250C	† Silicon G	
										UC4250C	Solitron	
	15	5	20	0.5 *	0.1	45K	100 *	0	Low Bias Current	3501A	Burr-Brown	
										3501R	† Burr-Brown	
	20	3	—	—	2.5 *	100K	80	1	High Voltage	LM144	† National	
				1 *	2 *	100K	80	0	High Voltage	MC1536	† Motorola	
										LM1536	† National	50
										SG1536	† Silicon G	
	25	5	20	0.3 *	0.13 *	50K	70	0	Micropower	RC4132	Raytheon	
		25	5 *	12 *	4	300K	100	0	Wide Temperature Range	OPA11HT	† Burr-Brown	
			10 *	12 *	4	80K	74	0	High Impedance	**AM-460-2**	**Datel (2622)**	
										AM-460-2M	† Datel	
										HA-2602	**† Harris (3226,3287)**	
										HA-2605	**Harris (3226,3287)**	
										HA2602	† Intersil	
										HA2605	Intersil	
			15 *	35 *	20	80K	74	1	Wide Band, High Impedance	AM-462-1	Datel	60
											(Continued)	

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift µV/°C	Band-width MHz	Slew Rate V/µs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source	Line
Single Units											**(Cont'd)**	
5.0	25	25	15 *	35 *	20	80K	74	1	Wide Band, High Impedance		(Cont'd)	
										AM-462-1M	† Datel	
										AM-462-2	**Datel (2622)**	
										AM-462-2M	† Datel	
										HA-2622	**† Harris (3228,3287)**	
										HA-2625	**Harris (3228,3287)**	
										HA2622	† Intersil	
										HA2625	Intersil	
			30 *	1	—	80K	74	1	Wideband	3508J	Burr-Brown	
				70	20	80K	100 *	1	Wideband, High Gain	1321	Teledyne P	
										1321-01	† Teledyne P	10
	30	15 *	20	1.5 *	0.6	45K	100 *	0	Low Bias, Low Noise	3500A	Burr-Brown	
										3500R	† Burr-Brown	
		30	20	2	0.4	50K	80	0	General Purpose	3500R/MIL	† Burr-Brown	
			60	2	0.4	50K	80	0	General Purpose	3500U/883B	† Burr-Brown	
	40	2.5 *	30 *	1 *	10	200K	80	0	Micropower FET High Current Out	1323	Teledyne P	
		15	5	—	20	300K	106	0	High Speed	**AM-470-2C**	**Datel (2623)**	
										AM-470-2M	† Datel	
			10	1 *	10	200K	80	0	Wide Response, Low Power	HA-2705	Harris	
	50	15	—	0.2	0.35	50K	70	0	Programmable Low Power	MC1776	† Motorola	
	100	20	—	—	—	50K	70	0	High Performance 741C	SSS741C	AMD	20
			10	2.5 *	18 *	25K	80	0	High Speed	**MP5501C**	**Micro Pwr (401,3292)**	
										MP5501G	**† Micro Pwr (401,3292)**	
										OP-01C	Micro Pwr	
										OP-01G	† Micro Pwr	
										OP-01C	PMI	
										OP-01G	† PMI	
			30	0.5	0.5 *	25K	70	1	Precision	µA777C	TI	
				1 *	0.5 *	25K	70	1	Precision	µA777C	Intersil	
		25	20	1.3	0.25	25K	70	0	General Purpose	**MP5502B**	**† Micro Pwr (401,3292)**	
										MP5502D	**Micro Pwr (401,3292)**	30
										OP-02B	† Micro Pwr	
										OP-02D	Micro Pwr	
										OP-02B	† PMI	
										OP-02D	PMI	
		50	3 *	—	—	20-40K	80	1	Micropower	µPC153A	NEC-Electron	
										µPC253A	NEC-Electron	
		100	—	1 *	0.4 *	50K	70	0	Programmable	XR146	† Exar	
	120	40	6 *	3 *	20	50K	70	0	High Slew Rate	NE530	Signetics	
	150	20	20	4 *	2 *	25K	70	0	High Performance, High Gain	RC4131	Raytheon	
		30	—	—	—	50K	70	0	Single Supply	TL3211	TI	40
										TL321I	TI	
										TL321M	† TI	
		40	6 *	—	60 *	50K	70	1	60 V/µs, Comp. for G=5	NE538	Signetics	
	200	—	10 *	10 *	130	25K	—	2	High Speed Inverting	ICL8017M	† Intersil	
		20	5 *		250	100K	80	1	High Slew Rate, Inverting	HA-2535	Harris	
		25	20 *	12 *	25	20K	80	0	High Slew Rate	**HA-2500**	**† Harris (3216,3287)**	
										HA2500	† Intersil	
		50	20 *	8 *	15 *	50K	80	1	Four Addressable Inputs, Single Amplifier	HA-2400	† Harris	
										HA-2404	Harris	
	250	20	20	1 *	0.5 *	25K	96	0	General Purpose	LM307	Raytheon	50
								1	General Purpose	LM301A	Raytheon	
	300	150	10 *	7 *	3.5	25K	80	0	Low Noise	HA-909	† Harris	
	500	150	20	—	—	20K	70	1	General Purpose	TA7502	Toshiba	
										TA7502A	Toshiba	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift µV/°C	Band-width MHz	Slew Rate V/µs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source	Line
Single Units										**(Cont'd)**		
										(Cont'd)		
5.0	500											
		200	—	0.5 *	35	50K	70	1	High Slew Rate	RM4531	† Raytheon	
				1 *	0.7	50K	70	0	High Speed 741	ICL741MHS	† Intersil	
					30 *	50K	70	1	High Slew Rate	SE531	† Signetics	
			3 *	0.5 *	0.3 *	25K	70	3	General Purpose	µA709M	† Fairchild	
										MC1709	† Motorola	
										LM709	† National	
				0.8 *	5 *	50K	70	0	Wideband 741	SG1217	† Silicon G	
				1 *	0.5 *	50K	70	0	General Purpose Compensated	AD741	† AD	
										µA741M	† Fairchild	
										ICL741	† Intersil	10
										MC1741	† Motorola	
										LM741	† National	
										PM741	PMI	
										RM741	† Raytheon	
										µA741	† Signetics	
										SG741	† Silicon G	
										µA741M	† TI	
									Low Noise 741	ICL741LN	† Intersil	
										MC1741N	† Motorola	
										CA6741	† RCA	20
								1	General Purpose, Uncompensated	µA101	† Fairchild	
										LM101	† National	
										SG101	† Silicon G	
									Uncompensated 741	µA748M	† Fairchild	
										MC1748	† Motorola	
										LM748	† National	
										LM748C	National	
										SL748A	Plessey	
										CA748	† RCA	
										µA748	† Signetics	30
										SG748	† Silicon G	
										µA748M	† TI	
					10	50K	70	0	High Slew Rate 741	MC1741S	† Motorola	
										SG741S	† Silicon G	
									Low Noise 741	MC1741NS	Motorola	
			4 *	30 *	0.7 *	20K	70	2	Programmable	CA3094A	† RCA	
										CA3094B	† RCA	
			6 *	—	0.3 *	45K *	70	3	General Purpose	µA709M	† TI	
	700	100	25	—	50 *	10K	65	0	20 mA Output	TCA322	† Siemens	
	750	250	6 *	65 *	15	15K	74	3	High Speed High Gain	µA715M	† Fairchild	40
	850	200	20	—		2K	70	3	709 Type	µPC55A	NEC-Electron	
	1000	300	20	30	15	50K	90	0	Precision, Audio	MA332	Analog Sys	
		300 *	50	150	60	10K	70	1	High Power	1460	Teledyne P	
	2000	400	—	38 *	25 *	0.6K	76	1	Large Signal Wideband	CA3100	† RCA	
	5000 *	1000 *	20	150 *	160	15K	74	1	Wideband, Fast Settling	HA-5190	Harris	
	7000	2000	5 *	—	—	2K	70	1	702 Type	UPC51A	NEC-Electron	
	7500	2000	20	30 *	3.5 *	2K	70	3	Wideband	µPC702	NEC-Electron	
	10000	2000	10 *		1.7 *	1.4K	70	3	General Purpose	TL702M	† TI	
	12000	5000	1.2 *	15 *	3 *	0.7K	70	1	6 Volt, Wideband	CA3008	† RCA	
										CA3010	† RCA	50
										CA3029	RCA	
										CA3037	† RCA	
	15000	4000	10 *	6.5 *	200 *	28K *	—	1	Wideband, Comp. for G>5	HA-5195	Harris	
	20000	—	10	—	800	250	70	1	Fast, Slews 800 V/µs	NE5539	Signetics	
										SE5539	† Signetics	
		300 *	25	500 *	250	10K	80	1	Settles to 0.01% in 70 ns	1435	† Teledyne P	
		6000	20	6	350	15K	60	—	Wideband, Fast Settling	**HA-2540-2**	**† Harris (3224,3287)**	
	24000	5000	3.5 *	50 *	7 *	2K	80	1	12 Volt, Wideband	CA3015	† RCA	
										CA3016	† RCA	
										CA3030	RCA	60
										CA3038	† RCA	

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift µV/°C	Band-width MHz	Slew Rate V/µs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source	Line
Single Units											**(Cont'd)**	
6.0	0.025	0.002	15	1 *	1	75K	70	0	High Performance FET	**LH0022C**	**National (3342)**	
	0.04	0.02	10 *	5 *	13 *	50K	80	1	MOS/FET Input, Bipolar/MOS Output	**CA080A**	**†RCA (3348)**	
										CA080T	**†RCA (3348)**	
										CA081A	**†RCA (3348)**	
										CA081T	**†RCA (3348)**	
	0.2	—	10 *	3 *	13 *	15K	80	0	Low Noise Bipolar-JFET	**TL075M**	**†TI (3427)**	
		0.05	10 *	3 *	13	50K	80	0	Low Noise Bipolar-JFET	**TL070M**	**†TI (3427)**	
										TL071M	**†TI (3427)**	
		0.1	10 *	1 *	3.5 *	40K	80	0	Low Power Bipolar JFET	**TL061AC**	**TI (3425)**	
										TL061M	**†TI (3425)**	10
									Programmable Bipolar JFET	MCE66	Micro Eng	
										TL066M	**†TI (3423)**	
								1	Low Power Bipolar JFET	MCE60	Micro Eng	
										TL060AC	**TI (3425)**	
										TL060M	**†TI (3425)**	
					4 *	20K	80	0	Low Power, JFET Input	**HA-5062-2**	**†Harris (3252,3287)**	
										HA-5062A-5	**Harris (3252,3287)**	
				3 *	13 *	50K	80	0	Bipolar-JFET	MCE80	Micro Eng	
										TL080AC	TI	
								1	Bipolar-JFET	TL080AC	TI	20
				4	15 *	25K	80	1	JFET Input	**HA-5082-2**	**†Harris (3256,3287)**	
						50K	80	1	JFET Input	**HA-5082A-5**	**Harris (3256,3287)**	
	25	10	6 *	—	0.2 *	75K	70	0	Programmable	SG3250	Silicon G	
		12	40	1 *	0.5 *	20K	80	0	Low Input Current 741	AD502J	AD	
		20	15 *	—	0.5 *	20K	70	0	Low Input Current	ICL8008C	Intersil	
		25	15 *	35 *	20	80K	74	1	Wideband, General Purpose	AD507J	AD	
	30	30	—	0.05	4	70K	74	0	Wideband	HA-2607	Harris	
										HA2607	Intersil	
			15 *	0.6	17	70K	74	0	Wideband	HA-2627	Harris	
										HA2627	Intersil	30
				4 *	5 *	100K	74	0	High Voltage	AM-464-2	Datel	
										AM-464-2M	†Datel	
										HA-2645	Harris	
										1332	Teledyne P	
	75	10	—	0.4	1.5	100K	80	—	Ultra-Low Power	HA-514A	Harris	
		20	—	—	—	60K	70	0	Programmable	µPC4250C	NEC-Electron	
	100	30	5 *	—	0.3 *	25K	70	1	Supply to +-10 V	TCA520B	Signetics	
	150	40	6 *	1 *	10	50K	70	0	High Slew Rate	NE535	Signetics	
	250	50	—	1 *	0.5	25K	80	0	to 500 mA, Single Supply	µA759C	Fairchild	
	500	200	—	—	0.5 *	5K	70	0	Short Circuit Protected	TBA221	Siemens	40
					5.5 *	5K	70	1	Adjustable Input Offset Voltage	TBB0748	Siemens	
					10	20K	70	1	1 A Output	TDB0791	Thomson-CSF	
				1 *	0.5	20-50K	70	0	General Purpose Compensated	**AD741C**	**AD (3153)**	
										IC450	Cherry	
										µA741C	Fairchild	
										HA17741	Hitachi	
										MC1741C	Motorola	
										LM741C	National	
										µPC151	NEC-Electron	
										µPC741	NEC-Electron	50
										PM741C	PMI	
										RC741	Raytheon	
										CA741C	RCA	
										µA741C	Signetics	
										SG741C	Silicon G	
										µA741C	TI	
										SFC741C	Thomson-CSF	
					0.5 *	20-50K	70	1	General Purpose	µA748C	Fairchild	
										µA748C	Intersil	
										MC1748C	Motorola	60
										SL748	Plessey	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift µV/°C	Band-width MHz	Slew Rate V/µs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source	Line
Single Units											**(Cont'd)**	
6.0	500	200	—	1 *	0.5 *	20-50K	70	1	General Purpose		(Cont'd)	
										CA748C	RCA	
										µA748C	Signetics	
										SG748C	Silicon G	
										µA748C	TI	
										SFC748C	Thomson-CSF	
					0.7	25K	70	0	High Speed 741	ICL741CHS	Intersil	
				1 *	1	100K	70	1	0.2 amp Power	LH0041C	National	
			3 *	1 *	10	20K	70	0	High Slew Rate 741	MC1741SC	Motorola	
										SG741SC	Silicon G	
									Low Noise 741	MC1741NC	Motorola	10
			5 *	0.8 *	5 *	20K	70	0	Wideband 741C	SG3217	Silicon G	
			10 *	1 *	0.25	100K	90	2	High Gain, Instrumentation, 50 mA Output	LH0020C	National	
					0.5 *	25K	70	0	Low Noise 741	ICL741CLN	Intersil	
			15 *	0.2 *	0.2 *	20K	70	0	High Power	µA791C	Fairchild	
										TBA0791	Thomson-CSF	
			30	1 *	1 *	100K	70	0	1.0 amp Power	LH0021C	National	
		300	10 *	7 *	5 *	20K	74	0	Low Noise	HA-911	Harris	
				12 *	50	25K	70	0	High Speed, Fast Setting	**AD518J**	**AD** **(3155)**	
	1000	300	6 *	—	18 *	12K	65	1	20 mA Output	TAA761	Siemens	
	1200	500	5 *	4 *	100 *	10K	70	2	Gated	ZN424	Ferranti	20
	1500	200	—	0.5 *	35 *	20K	70	1	High Slew Rate	RC4531	Raytheon	
				1 *	20 *	20K	70	1	High Slew Rate, High Performance	NE531	Signetics	
7.0	100	10	—	0.4	1	100K	77	—	Ultra-Low Power	**HA-5141**	**Harris** **(3266)**	
	200	10 *	10 *	10 *	130 *	25K	—	2	High Speed Inverting	ICL8017C	Intersil	
	400	75	5 *	—	—	3K	63	0	250 mA Output, Electronic Shutdown	LM13080	National	
				1 *	0.4 *	3K	63	0	250 mA Output, Electronic Shutdown	MA13080	Analog Sys	
	6000	75	5 *	—	1.6	3K	63	0	450 mA Output, Electronic Shutdown	MA324	Analog Sys	
7.5	7	1	—	0.3 *	0.3 *	25K	80	1	Low Noise 308	LM308LN	Intersil	
			6 *	—	—	25K	80	1	308 Type	µPC156A	NEC-Electron	
			30	1 *	0.3 *	25K	80	0	Micropower, Supply Current 800 µA	LM312	National	30
								1	Precision Bipolar	LM308	AMD	
										AD308	**AD** **(3153)**	
										LM308	**Harris** **(3286,3288)**	
										LM308	Intersil	
										LM308	Motorola	
										LM308	National	
										PM308	PMI	
										SG308	Silicon G	
										SFC2308	Thomson-CSF	
	15	2	30		0.1	25K	80	1	Precision	1660	AMD	40
	250	50	—	0.8 *	0.5 *	25K	70	1	Low Noise 301A	ICL301ALN	Intersil	
			30	1 *	0.5 *	25K	70	0	General Purpose, Compensated	LM307	Harris	
										LM307	Intersil	
										LM307	Motorola	
										LM307	National	
										CA307	RCA	
										SG307	Silicon G	
										LM307	TI	
										SFC2307	Thomson-CSF	
								1	General Purpose Uncompensated	**AD301A**	**AD** **(3153)**	50
										µA301A	Fairchild	
										LM301A	Harris	
										LM301A	Motorola	
										LM301A	National	
										µPC157	NEC-Electron	
										µPC301	NEC-Electron	
										CA301A	RCA	
										LM301A	Signetics	
										SG301A	Silicon G	
										LM301A	TI	60
										SFC2301A	Thomson-CSF	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift µV/°C	Band-width MHz	Slew Rate V/µs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source	Line
Single Units											**(Cont'd)**	
7.5											(Cont'd)	
	1000	150	3 *	2 *	4.2 *	15K	80	2	General Purpose	MC1439	Motorola	
		300	6 *	—	18 *	5K	60	0	20 mA Output	TCA321	Siemens	
										TCA325	Siemens	
	1500	250	6	65 *	10	10K	74	3	High Speed	µA715C	Fairchild	
		500	6 *	—	0.3 *	15K	65	3	General Purpose	µA709C	TI	
				1 *	0.5 *	20K	65	1	General Purpose	µA201	Fairchild	
										LM201	National	
										SG201	Silicon G	
			6-10 *	1 *	0.3 *	15K	65	3	General Purpose	µA709C	Fairchild	
										LM709C	National	10
										RC709	Raytheon	
								4	General Purpose	TAA521	Siemens	
8.0	40	10	—	1 *	2.5 *	70K	70	1	High Voltage	LM344	National	
	200	25	20 *	10 *	50	10K	80	0	High Slew Rate	HA-2510	† Harris	
										HA2510	Intersil	
				20 *	100	10K	80	1	100 v/µs, Gain =3	HA-2520	† Harris	
										HA2520	† Intersil	
			30	20 *	100	10K	80	1	High Speed, Fast Settling	AD509K	AD	
										AD509S	† AD	
	250	50	20 *	12 *	20	15K	74	0	High Slew Rate	**AM-450-2**	**Datel (2622)**	20
										AM-450-2M	† Datel	
										HA-2502	**† Harris (3216.3287)**	
										HA-2505	**Harris (3216.3287)**	
										HA2502	† Intersil	
										HA2505	Intersil	
	40000	15000	25 *	70 *	250	3K	60 *	3	High Slew Rate	LH0024C	National	
9.0	0.40	0.20	10 *	1 *	0.6 *	200K	70	0	JFET Input	TL091M	† TI	
	250	50	30 *	8 *	15 *	50K	74	1	Four Addressable Inputs Single Amplifier	HA-2405	Harris	
10.0	0.003	0.002	4 *	0.5 *	0.5 *	10K	70	0	Low Supply Voltage	**CA3420**	**† RCA (3352)**	
	0.050	0.020 *	30	3 *	15 *	20K	86 *	0	High Voltage FET	3580J	Burr-Brown	30
		0.025	4 *	0.063 *	0.03 *	10K	70	0	Nanopower BiMOS	**CA3440**	**RCA (3353)**	
	0.10	0.03	10	—	10	3K	90	1	FET Input, Low Noise	MA333	Analog Sys	
				12	35	100K	90	0	JFET Input	MA334	Analog Sys	
										MA400	Analog Sys	
	0.15	0.05	20	1 *	0.3 *	20K	80	0	High Performance, Low Input Current	LM316	National	
					10	30K	90	0	Low 1/f Noise	MA339	Analog Sys	
	0.20	0.05	5 *	—	—	25K	80	—	Wideband Decompensated	LF357	AMD	
										LF357	**Harris (3288)**	
										LF357	Intersil	
										LF357	Motorola	40
										LF357	**National (3309)**	
										PM357	PMI	
				2.5	5 *	25K	80	0	Bipolar-JFET	LF355	AMD	
										LF355	Intersil	
										LF355	Motorola	
										LF355	**National (3309)**	
										PM355	PMI	
										LF355	Signetics	
				5	12 *	25K	80	0	Wideband-JFET	LF356	AMD	
										LF356	**Harris (3288)**	50
										LF356	Intersil	
										LF356	Motorola	
										LF356	**National (3309)**	
										PM356	PMI	
										LF356	Signetics	
			10 *	3 *	13 *	15K	80	0	Low Noise Bipolar-JFET	**TL070AC**	**TI (3427)**	
										TL070C	**TI (3427)**	
										TL071AC	**TI (3427)**	
										TL071BC	**TI (3427)**	
										TL071C	**TI (3427)**	60
											(Continued)	

† Military Temperature Range (– 55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR-Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift μV/°C	Band-width MHz	Slew Rate V/μs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source	Line
Single Units											**(Cont'd)**	
											(Cont'd)	
10.0	0.20											
		0.1	10 *	3 *	13 *	50K	70	0	Bipolar JFET	μAF771	Fairchild	
				4 *	13	25K	70	0	Bipolar-JFET	LF351	National	
					13 *	25K	70	0	Precision BIFET	**MC34001**	**Motorola (3293)**	
		2	10 *	3 *	13 *	15K	80	0	Low Noise Bipolar-JFET	TL075C	TI	
	0.60	0.1	20 *	18 *	57 *	200K	80	0	Wideband-JFET	LF400	National	
	1	0.25	10	5	10	50K	85	0	2.0 A Power	LH0101	National	
										LH0101C	National	
	10	3	150	—	250	0.7K	50	1	100 MHz	9906	† OEI	
	30	10	—	1 *	2.5 *	70K	70	0	High Performance	MC1456	Motorola	
	40	10	—	1 *	2 *	70K	70	0	High Voltage	MC1436	Motorola	10
										MC1456	Signetics	
										SG1436	Silicon G	
			65	1 *	1.5	—	70	0	2 A Continuous	3573	Burr-Brown	
	50	20	20 *	—	—	2K	55	3	Matched Input Transistors	LH0005	National	
	100	25	25 *	—	—	2K	50	3	Matched Input Transistors	LH0005C	National	
	250	50	20 *	20 *	80	7.5K	74	1	High Speed, Fast Settling	AD509J	AD	
			25 *	12 *	15	15K	74	0	High Slew Rate	HA-2507	Harris	
										HA2507	Intersil	
					40	7.5K	74	0	High Slew Rate	**HA-2512**	**† Harris (3218,3287)**	
										HA2512	Intersil	20
				20 *	80	7.5K	74	1	80 V/μs Gain=3	**HA-2522**	**† Harris (3220,3287)**	
										HA2522	† Intersil	
			30 *	—	80	7K	74	1	Fast Slewing	3507J	Burr-Brown	
				12 *	30	7.5K	74	0	High Slew Rate	HA-2517	Harris	
										HA2517	Intersil	
					40	7.5K	74	0	High Slew Rate	**HA-2515**	**Harris (3218,3287)**	
										HA2515	Intersil	
					80	7.5K	74	1	80 V/μs Gain = 3	**HA-2525**	**Harris (3220,3287)**	
										HA2525	Intersil	
									80 V/μs Gain=3	**AM-452-2**	**Datel (2622)**	30
										AM-452-2M	† Datel	
				20 *	60	7.5K	74	0	High Slew Rate	HA-2527	Harris	
										HA2527	Intersil	
					80	7.5K	90 *	1	High Slew Rate	1322	Teledyne P	
										1322-01	† Teledyne P	
						70K	90 *	0	High Slew Rate/Temperature	OPA12HT	† Burr-Brown	
	500	200	—	15 *	50	25K	70	0	Precision, High Speed	LM318	AMD	
										μA318	Fairchild	
										LM318	Harris	
										LM318	National	40
										μPC159A	NEC-Electron	
										LM318	TI	
										SFC2318	Thomson-CSF	
			5 *	1 *	25	25K	60	1	0.5 A, Wideband	LH0061C	National	
		300	10	2	10	50K	70	1	Up to ±40 V Output	MA700	Analog Sys	
	750	—	—	—	—	14K	—	1	Telephone Channel Amplifier	LS045	SGS	
	1000	300	6 *	—	18 *	0.56K	60	1	to 90 mA Output	TAA861	Siemens	
										TAA865	Siemens	
	3000	300	16	20	10	100K	60	2	Up to 400 mA Output	MA206	Analog Sys	
	15000	5000	5 *	—	1.7 *	1K	65	3	General Purpose	TL702C	TI	50
12.0	90	25	—	1 *	2 *	50K	50	0	High Voltage	MC1436C	Motorola	
										SG1436C	Silicon G	
		30	—	1 *	2.5	25K	110 *	0	High Performance	MC1456C	Motorola	
										LM1436	National	
14.0	200	15	50 *	—	—	10K	65	1	Darlington Input	TCA312	† Siemens	
										TCA332	† Siemens	

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift µV/°C	Band-width MHz	Slew Rate V/µs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source	Line
Single Units											**(Cont'd)**	
15.0	0.010	—	25	2 *	3	50K	72	0	High Performance, Low Bias	1421-02	Teledyne P	
	0.015	—	50	2 *	3	50K	72	0	High Performance, Low Bias	1421-01	Teledyne P	
	0.050	—	50	2 *	3	50K	72	0	High Performance FET	1421	Teledyne P	
		0.030	8 *	4 *	10 *	50K	70	0	MOS FET, Single Supply	CA3160	† RCA	
				4.5 *	9 *	20K	70	0	MOS FET, Single Supply	CA3140	† RCA	
			10 *	4 *	10 *	50K	70	1	MOS FET Single Supply, Strobe	CA3130	† RCA	
			5 *	13 *	50K	70	0	FET Input, Bipolar/MOS Output	**CA081**	**RCA**	(3348)	
										CA081C	**RCA**	(3348)
								1	FET Input, Bipolar/MOS Output	**CA080**	**RCA**	(3348)
										CA080C	**RCA**	(3348) 10
			25 *	1	1.6	80K	70	0	Low Power	ICL7611C	Intersil	
									Low Power, Extended CMVR	ICL7612C	Intersil	
									Low Power, Input Protected	ICL7613DC	Intersil	
								1	Low Power	ICL7614DC	Intersil	
									Low Power, Input Protected	ICL7615DC	Intersil	
	0.065	0.005	35	15 *	50	25K	70	0	Precision, High Speed, FET	LH0062C	National	
		0.01	20 *	1 *	50	25K	70	1	Wideband, High Slew Rate	**HA-5162-5**	**Harris** (3268,3287)	
	0.20	0.05	10 *	1 *	0.5 *	25K	70	0	JFET-741	**LF13741**	**National** (3309)	
			25 *	50 *	350	1K	50	2	Ultra Fast FET	ADLH0032C	AD	
										LH0032C	National	20
		0.10	10 *	3 *	13 *	50K	70	0	Bipolar-JFET	µAF771L	Fairchild	
	0.4	0.05	—	3 *	13 *	25K	70	1	Low Noise Bipolar-JFET	MCE70	Micro Eng	
		0.2	10 *	1 *	3.5 *	3K	70	0	Low Power Bipolar-JFET	**TL061C**	**TI** (3425)	
								1	Low Power Bipolar-JFET	**TL060C**	**TI** (3425)	
					4 *	10K	70	0	Low Power, JFET Input	**HA-5062-5**	**Harris** (3252,3287)	
				3 *	13 *	25K	70	0	Bipolar-JFET	µPC4081	NEC-Electron	
								1	Bipolar-JFET	TL080C	TI	
				4	15 *	25K	70	—	JFET Input	**HA-5082-5**	**Harris** (3256,3287)	
	0.40	0.20	10 *	1 *	0.6 *	200K	70	0	JFET Input	TL091C	TI	
	750	150	30	300	15	10K	84	1	High Power	MA329	Analog Sys	30
	20000	6000	20	6	350	10K	60	—	Wideband, Fast Settling	**HA-2540-5**	**Harris** (3224,3287)	
			20 *	9.5 *	550	10K	60	—	High Slew Rate, Wideband	**HA-2539-5**	**Harris** (3222,3287)	
						15K	60	—	High Slew Rate, Wideband	**HA-2539-2**	**†Harris** (3222,3287)	
20.0	0.00025	—	60	0.5 *	3	40K	80	0	Electrometer, FET	AD523L	AD	
	0.0005	—	30	0.5 *	3	40K	80	0	Electrometer, FET	AD523K	AD	
	0.010	—	25	0.75 *	0.5 *	50K	70	0	Low Noise FET	AD514L	AD	
		0.002 *	25	1 *	2.5	31K	86 *	0	High Performance, Low Bias FET	3503B	Burr-Brown	
										3503S	† Burr-Brown	
	0.020	—	25	0.75 *	0.5	50K *	70	0	Low Noise FET	AD514K	AD	
			50	0.75 *	0.5 *	50K *	70	0	Low Noise FET	AD514S	† AD	40
		0.0005 *	75	1 *	6 *	50K	70	0	High Performance FET	ICL8007M	† Intersil	
	0.025	—	25	1 *	6 *	50K	70	0	Low Cost FET Input	**AD540K**	**AD** (3153)	
			50	1 *	0.5 *	25K	80	0	FET	AD3542J	AD	
					6 *	50K	70	0	Low Cost FET Input	**AD540S**	**†AD** (3153)	
		0.002 *	50	1 *	0.5 *	25K	80 *	0	Low Noise	3542J	Burr-Brown	
										3542S	† Burr-Brown	
		0.010	20	1 *	1.5	50K	70	0	Low Cost FET Input	LH0042	† Intersil	
										LH0042	**†National** (3342)	
	0.030	0.005 *	20 *	1 *	6 *	50K	70	0	FET	SU536	Signetics	
	0.050	—	25	1 *	6 *	25K	70	0	Low Cost FET	AD0042C	AD	50
		0.005	25	1 *	1	25K	70	0	Low Cost FET	LH0042C	Intersil	
										LH0042C	**National** (3342)	
	0.10	—	25	1 *	3	50K	80	0	Low Cost FET Input	**AD503K**	**AD** (3153)	
										AD503S	**†AD** (3153)	
	0.20	0.15	0.06 *	1 *	6 *	1000K	80 *	0	High Slew Rate FET	µA740C	Signetics	
			20 *	3 *	6 *	25K	64	0	High Slew Rate FET	µA740	† Intersil	

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† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift µV/°C	Band-width MHz	Slew Rate V/µs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source	Line
Single Units											**(Cont'd)**	
											(Cont'd)	
20.0	50	20	12 *	—	9 *	0.5K	60	1	Darlington Input	TBB1331A	Siemens	
	200	25	12 *	—	—	6K	60	0	Darlington Input	TCA311	Siemens	
										TCA315	Siemens	
								1	Darlington Input	TCA331	Siemens	
	50000	10000	30	1	300	70K	90	2	Low Propagation Delay	9818	OEI	
25.0	40000	10000	1000	100	600	1K	50	2	Wide Gain-Bandwidth	9912	† OEI	
30.0	0.001	0.0002 *	50	1 *	2.5	20K	86	0	Low Bias FET	ICL8007AC	Intersil	
										ICL8007AM	† Intersil	
	30000	10000	150	200	300	1K	50	0	Wideband	9916	† OEI	
	50000	20000	100	300	1K	4K	90	1	Wideband	9914	OEI	10
30.0 *	5000 *	6000	50 *	150 *	600	40	—	0	Fast Settling, Wideband	CLC103AM	† Comlinear	
		8000	50 *	150 *	600	40	—	0	Fast Settling, Wideband	CLC103AI	Comlinear	
35.0	2	0.1	150	100	300	100K	70	0	High Slew Rate	HDS-060	AD	
50.0	0.00001	—	—	—	0.5 *	20K	60	0	Ultra low Bias FET	ICH8500A	Intersil	
	0.0001	—	—	—	0.5 *	20K	60	0	Ultra low Bias FET	ICH8500	Intersil	
	0.001	—	50	0.3 *	—	10K	70		MOS FET	µPC250A	NEC-Electron	
		0.0005 *	90	0.5 *	3	20K	70	0	Electrometer, FET	AD523J	AD	
	0.015	—	75	1 *	3	20K	70	0	Los Cost FET Input	**AD503J**	**AD (3153)**	
	0.025	0.005 *	75	1 *	2.5	20K	86 *	0	High Performance, Low Bias FET	3503A	Burr-Brown	
										3503R	† Burr-Brown	20
	0.050	—	75	0.75 *	0.5 *	20K	70	0	Low Noise FET	AD514J	AD	
				1 *	6 *	20K	70	0	Low Cost FET	**AD540J**	**AD (3153)**	
							72	0	High Performance FET	1424	Teledyne P	
		0.0005 *	75	1 *	6 *	20K	70	0	High Performance, FET	ICL8007C	Intersil	
90.0	0.10	0.005 *	30 *	1 *	6 *	50K	64	0	FET, High Input Impedance	NE536	Signetics	
110.0	0.20	0.15	20 *	3 *	6 *	25K	64	0	High Slew Rate FET	µA740C	† Intersil	
200.0	0.01	—	50 *	1 *	0.4 *	10K	70 *		MOS FET	µPC152A	NEC-Electron	
Dual Units												
—	8000 *	—	—	30	60 *	4K	—	0	GB Product = 400 MHz	LM159	† National	
										LM359	National	
0.08	40	35	1	5	1.7	250K	114	0	Ultra Low Noise Instrumentation	OP-227A	† PMI	30
										OP-227E	PMI	
0.12	55	50	1.5	5	1.7	250K	106	0	Ultra Low Noise Instrumentation	OP-227B	† PMI	
										OP-227F	PMI	
0.15	7.0	6.0	0.5 *	0.5 *	0.17 *	120K	100	0	Low Noise	µPC454	NEC-Electron	
	20	2	2	100 *	—	500K	96	0	Low Power, Single/Dual Supply	OP-220A	† PMI	
										OP-220E	PMI	
0.18	80	75	2	5	1.7	200K	106	0	Ultra Low Noise Instrumentation	OP-227C	† PMI	
										OP-227G	PMI	
0.25	0.035	0.002	2.5	1 *	3 *	250K	80	—	Ultra Low Drift BiFET	**AD647L**	**AD (3151,3153)**	
0.3	0.050	0.010	3	1 *	0.3 *	300K	110	0	Dual LM11, High Performance	**LH2011**	**† National (3342)**	40
	25	2.5	5	100 *	—	300K	90	0	Low Power, Single/Dual Supply	OP-220B	† PMI	
										OP-220F	PMI	
0.5	0.035	0.002	5	1 *	3 *	250K	80	—	Ultra Low Drift BiFET	**AD647K**	**AD (3151,3153)**	
										AD647S	**† AD (3151,3153)**	
										AD647S/ 883B	**† AD (3151,3153)**	
		0.005 *	5	2 *	3 *	250K	80	0	Dual 544	**AD644L**	**AD (3153)**	
			5 *	1 *	3 *	300K *	80	0	Dual 542	**AD642L**	**AD (3153)**	
			15	2 *	3 *	250K	80	0	Dual 544	**AD644S**	**† AD (3153)**	
	0.06	0.025	5 *	—	13 *	50K	80	0	Precision BIFET	MC35003A	† Motorola	
										MC35022A	† Motorola	50
	0.075	0.03	5 *	—	13 *	50K	80	0	Precision BIFET	MC34003A	Motorola	
										MC34022A	Motorola	
	2	0.2	15	1 *	0.3 *	80K	96	1	Dual 108A	LH2108A	† Intersil	
										LH2108A	**† National (3342)**	
										LH2208A	**National (3342)**	
										PM2108A	† PMI	
										PM2208A	PMI	
	3	2.8	2	0.6 *	0.17 *	150K	110	0	Dual Matched Instrumentation	OP-10	† Micro Pwr	

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† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift µV/°C	Band-width MHz	Slew Rate V/µs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source	Line
Dual Units											**(Cont'd)**	
0.5	3	2.8	2	0.6 *	0.17 *	150K	110	0	Dual Matched Instrumentation		(Cont'd)	
										OP-10A	† Micro Pwr	
										OP-10E	Micro Pwr	
	7	1	30	1 *	0.3 *	80K	96	1	Dual 308A	LH2308A	Intersil	
										LH2308A	**National (3342)**	
										PM2308A	PMI	
	20	0.1	10	3	13	50K	80	0	Bipolar-JFET	**TL287C**	**TI (3424)**	
										TL287M	**† TI (3424)**	
0.6	0.10	0.01	2	0.8 *	0.3	250K	110	0	Dual LM11, High Performance	**LH2011B**	**† National (3342)**	
	40	4	10	100 *	—	500 *	76	0	Low Power, Single/Dual Supply	OP-220C	† PMI	
										OP-220G	PMI	10
0.75	50	2	8	0.8	0.5	100K	90	0	Dual Matched	OP-04A	† PMI	
										OP-04E	PMI	
										OP-14A	† PMI	
										OP-14E	PMI	
									OP-04 with Internally Connected Vcc Terminals	MC35022	† Motorola	
										OP-03A	† PMI	
										OP-03E	PMI	
1.0	0.035	0.005 *	10	1 *	3 *	300K *	80 *	0	Dual 542	**AD642K**	**AD (3153)**	
										AD642S	**† AD (3153)**	
				2 *	3 *	250K	80	0	Dual 544	**AD644K**	**AD (3153)**	20
	0.05	0.025	10	1	1	50K	80	0	Low Power BIFET	LF422A	National	
										LF442A	National	
	0.075	0.005	10	1 *	3 *	100K	76	—	Ultra Low Drift BiFET	**AD647J**	**AD (3151,3153)**	
		0.050	5 *	4 *	13 *	50K	80	0	BIFET	MC35022B	† Motorola	
	0.18	0.02	3	0.8 *	0.3	90K	—	0	Dual LM11, High Performance	**LH2011C**	**National (3342)**	
	0.2	0.10	10	3	10	50K	80	0	Wideband JFET	**LF412A**	**National (3309,3312)**	
	500	600	—	2 *	50 *	20K	80	0	Transconductance Amplifier	LM11700A	National	
										LM13700A	**National (3326,3328)**	
1.3	7	6	4.5	1.2 *	0.25 *	120K	100	0	Dual Matched Instrumentation	OP-10C	PMI	
						250K	100	0	Dual Matched Instrumentation	**MP5510C**	**Micro Pwr (401,3292)**	30
										OP-10C	Micro Pwr	
2.0	0.02	0.01	5 *	4 *	10 *	50K *	86	0	Dual 3160	**CA3260B**	**RCA (3349)**	
	0.05	0.030	10 *	1	1.6	80K *	70	0	Low Power, Dual 747	ICL7622AC	Intersil	
										ICL7622AM	† Intersil	
									Low Power, Dual 1458	ICL7621AC	Intersil	
										ICL7621AM	† Intersil	
	0.075	0.025	10 *	4 *	13 *	50K	80	0	Precision BIFET	**MC35002A**	**† Motorola (3293)**	
		0.030	5 *	4 *	13 *	50K	80	0	Precision BIFET	MC34022A	Motorola	
		0.075 *	20 *	1 *	3 *	200K *	76 *	0	Dual 542	**AD642J**	**AD (3153)**	
				2.0	3 *	100K	76	0	Dual 544	**AD644J**	**AD (3153)**	40
	0.10	0.05	10 *	3 *	13 *	50K	80	0	Bipolar-JFET	µAF772A	Fairchild	
										µAF772AM	† Fairchild	
				4 *	13 *	50K	80	0	Dual 351A	**LF353A**	**National (3309,3326)**	
									Precision BIFET	**MC34002A**	**Motorola (3293)**	
	0.15	0.05	20	0.06	10	3K	100	—	JFET Input	MA406	Analog Sys	
		0.07	5 *	4 *	13 *	25K	80	0	Precision BIFET	MC34022	Motorola	
										MC35022	† Motorola	
	2	0.2	15	1 *	0.3 *	50K	85	1	Dual 108	**LH2108**	**† National (3342)**	
										LH2208	**National (3342)**	
										PM2108	PMI	50
										PM2208	PMI	
	50	10	15	1 *	—	50K	70	0	Low Power, Single Supply	CA158A	† RCA	
		25	5	1.5 *	0.8	100K *	100 *		Matched Amplifier Pairs	3500MP	Burr-Brown	
	60	10	15	—	—	50K	70	1	40 V/µs, G=5	SE5538	† Signetics	
				3 *	35 *	50K	70	0	High Slew Rate	SE5530	† Signetics	
	75	5	10	0.8	0.5	50K	90	0	Dual Matched	OP-04	PMI	
										OP-04C	PMI	
										OP-14C	PMI	
											(Continued)	

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift µV/°C	Band-width MHz	Slew Rate V/µs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source		Line
Dual Units												**(Cont'd)**	
2.0	75	5	10	0.8	0.5	50K	90	0				(Cont'd)	
									OP-04 with Internally Connected VCC Terminals	OP-03	PMI		
										OP-03C	PMI		
		10	15	1 *	0.5 *	50K	80	1	Dual LM101A High Performance	LH2101A	† AMD		
										LH2201A	AMD		
										LH2101A	Intersil		
										LH2101A	**† National**	**(3342)**	
										LH2201A	**National**	**(3342)**	
										LH2101A	Raytheon		
	100	20	10	5.7 *	16 *	220K	100 *	0	Precision Bipolar-JFET	OP-215B	† PMI		
										OP-215F	PMI		10
	800	200	—	10 *	13	50K	80	1	Dual 5534	SE5532	† Signetics		
										SE5532A	† Signetics		
										SE5533	† Signetics		
										SE5533A	† Signetics		
3.0	0.03	0.01	10 *	5 *	13 *	50K	80	0	MOS/FET Input, Bipolar/MOS Output	**CA082B**	**RCA**	**(3348)**	
										CA083B	**RCA**	**(3348)**	
	0.04	0.02	10 *	5 *	13 *	50K	80	0	MOS/FET Input, Bipolar/MOS Output	**CA082AT**	**† RCA**	**(3348)**	
	0.15	0.03	10	0.11	10	3K	90	—	Low Wideband Noise	MA345	Analog Sys		
	0.2	0.1	10 *	1 *	3.5 *	4K	80	0	Low Noise Bipolar-JFET	**TL062BC**	**TI**	**(3425)**	
				3 *	15 *	50K	80	0	Bipolar-JFET	TL082BC	TI		20
										TL288C	**TI**	**(3424)**	
										TL288M	**† TI**	**(3424)**	
			20	0.7	8	25K	70	0	Wideband JFET	**LF412**	**National**	**(3309,3312)**	
	5	3	10 *	25 *	0.1 *	40K	80	0	Programmable	HA-2730	† Harris		
		5	—	1	1	100K	100	0	Low Noise	SE5512	† Signetics		
	15	5	—	0.25	0.16	100K	—	0	Low Power	**LH2250**	**† National**	**(3342)**	
										LH2250C	**National**	**(3342)**	
				.25 *	0.16 *	100K	70	0	Programmable Dual LM4250	LH24250	† National		
	20	7.5	5 *	0.27 *	0.16 *	50K	70	0	Low Power Adjustable Current	ICL8022M	† Intersil		
	80	15	15	1 *	—	50K	70	0	Low Power, Single Supply	LM258A	National		30
										CA258A	RCA		
		30	15	0.44	0.3	50K	80	0	Dual 741	µA747AM	† Fairchild		
										µA747EC	Fairchild		
										LM747A	† National		
										LM747E	National		
	100	30	8 *	8 *	2	25K	80	0	High Slew Rate	**HA-2650**	**† Harris**	**(3234,3287)**	
			20	1 *	—	25K	65	0	Low Power, Single Supply	LM358A	National		
										CA358A	RCA		
	750	400	3 *	—	2 *	20K	70	3	Audio Preamp	µA749C	Fairchild		
	5000	700	5 *	9 *	125 *	50K	80	1	Transconductance Amp	CA3280	RCA		40
4.0	80	20	4 *	1 *	10	50K	70	0	High Slew Rate	SE5535	† Signetics		
	150	25	—	—	—	50K	70	0	2 Op Amp/Comparators	LM192	† National		
	200	50	20	5.4 *	15 *	200K	96 *	0	Precision Bipolar-JFET	OP-215C	† PMI		
										OP-215G	PMI		
	350	100	3 *	—	0.5 *	50K	80	0	Dual 222	TBC0747	† Siemens		
	500	600	—	2 *	50 *	20K *	80	0	Transconductance Amplifier	**LM13700**	**† National**	**(3326,3328)**	
	700	100	25	—	—	18K	70	0	20 mA Output	TAA2762	† Siemens		
	800	150	—	10 *	9	25K	70	1	Low Noise	NE5532	TI		
										NE5532A	TI		
	1500	300	—	10 *	13 *	25K	70	1	Dual 5534	**XR5532**	**Exar**	**(3208)**	50
										XR5533	**Exar**	**(3208)**	
										NE5532	Signetics		
										NE5532A	Signetics		
										NE5533	† Signetics		
										NE5533A	Signetics		
5.0	0.03	0.02	6 *	4 *	10 *	50K *	70	0	Dual 3160	**CA3260AE**	**RCA**	**(3349)**	
										CA3260AT	**† RCA**	**(3349)**	
												(Continued)	

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift µV/°C	Band-width MHz	Slew Rate V/µs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source	Line
Dual Units											**(Cont'd)**	
5.0											(Cont'd)	
	0.04	0.02	15 *	45 *	9 *	20K	70	0	Dual 3140A, MOS FET	**CA3240A**	**RCA (3350)**	
	0.050	0.030	15 *	1	1.6	80K	70	0	Low Power, Dual 1458	ICL7621BC	Intersil	
										ICL7621BM	† Intersil	
									Low Power, Dual 747	ICL7622BC	Intersil	
										ICL7622BM	† Intersil	
	0.10	0.05	10 *	1 *	1 *	25K	70	0	Low Power JFET	LF442	National	
				4 *	13 *	50K	80	0	Precision BIFET	**MC35002B**	**† Motorola (3293)**	
		0.07	10 *	4 *	13 *	25K *	70	0	Precision BIFET	**MC34002B**	**Motorola (3293)**	
		0.10	10 *	3 *	13 *	50K	80	0	Bipolar JFET	µAF772B	Fairchild	
										µAF772BM	† Fairchild	10
	0.20	0.10	10 *	3	10	50K	80	0	Dual 151	LF153	† National	
				4 *	13 *	50K	80	0	Dual 351B	**LF353B**	**National (3309,3326)**	
	7.5	3	3 *	1 *	15 *	200K	70	0	Multi-Purpose Programmable	µA776M	† Fairchild	
	10	5	10 *	—	0.1 *	25K	74	0	Programmable	HA-2735	Harris	
		10	—	1	1	100K	100	0	Low Noise	NE5512	Signetics	
										NE5517	Signetics	
										NE5517A	Signetics	
	100	25	—	—	—	50K	70	0	Dual High Performance 741C	SSS747C	AMD	
			10	0.8	0.25	50K	70	0	Dual Matched	OP-04B	† PMI	
										OP-04D	PMI	20
									OP-04 with Internally Connected VCC Terminals	OP-03B	† PMI	
										OP-03D	PMI	
		40	—	0.8 *	0.5 *	4K	60	0	Low Power	TL022M	† TI	
	120	40	6 *	3 *	35 *	50K	70	0	High Slew Rate	NE5530	Signetics	
	150	30	7 *	1 *	—	50K	70	0	Half LM124	LM158	† Motorola	
										LM158	† National	
										LM258	National	
										CA158	† RCA	
										CA258	RCA	
										LM158	† Signetics	30
										LM258	Signetics	
										SE532	† Signetics	
										LM158	† TI	
		40	6 *	—	60 *	—	70	1	60 V/µs, G=5, Dual 538	NE5538	Signetics	
	200	60	8 *	8 *	2	20K	74	0	High Slew Rate	**HA-2655**	**Harris (3234,3287)**	
		80	—	0.8 *	0.5 *	1K	60	0	Low Power	TL022C	TI	
	250	50	—	—	—	25K	65	0	2 Op Amp/Comparators	LM292	National	
										LM392	National	
	500	50	10 *	1 *	0.6 *	50K	70	0	Single Supply	MC3558	† Motorola	
		200	—	—	10	50K	70	0	High Slew Rate 1558	MC1558S	† Motorola	40
				2	1.5 *	50K	70	0	Dual Wideband 741	RM4558	† Raytheon	
				2.5	1	20K	70	0	General Purpose	SE4558	† Signetics	
					1.5 *	50K	70	0	Dual Wideband 741	MC4558	† Motorola	
										MC4558A	Motorola	
									Low Noise	MC4558N	† Motorola	
				3	1.5 *	50K	70	0	3 MHz Min. Bandwidth	RM4559	† Raytheon	
			1.5 *	1 *	0.3 *	25K	70	3	Matched Dual 709	RM1537	† Raytheon	
			2-15 *	1 *	0.5 *	50K	70	0	Dual 741	µA1558M	† Fairchild	
										µA747M	† Fairchild	
										MC1558	† Motorola	50
										MC1747	† Motorola	
										LM1558	† National	
										LM747	† National	
										PM1558	† PMI	
										PM747	† PMI	
										RM1558	† Raytheon	
										RM747	† Raytheon	
										CA1558	† RCA	
										CA747	† RCA	
										MC1558	† Signetics	60
										µA747	† Signetics	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift µV/°C	Band-width MHz	Slew Rate V/µs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source		Line
Dual Units												**(Cont'd)**	
5.0	500	200	2-15 *	1 *	0.5 *	50K	70	0	Dual 741			(Cont'd)	
										SG1558	† Silicon G		
										SG747	† Silicon G		
										MC1558	† TI		
										µA747M	† TI		
										TA75458	Toshiba		
										TA75747	Toshiba		
									Low Noise	MC1558N	† Motorola		
				3 *	0.25	25K	70	3	Dual MC1709	MC1537	† Motorola		
	7000	8000	6000	—	2 *	50	80	0	Transconductance Amplifier	**LM13600**	**National**	**(3326)**	
6.0	0.04	0.02	10 *	5 *	13 *	50K	80	0	MOS/FET Input, Bipolar/MOS Output	**CA082A**	**RCA**	**(3348)**	10
										CA082T	**†RCA**	**(3348)**	
										CA083A	**RCA**	**(3348)**	
	0.2	0.05	10 *	3 *	13 *	50K	80	0	Low Noise Bipolar-JFET	**TL072M**	**†TI**	**(3427)**	
		0.1	10 *	1 *	3.5 *	4K	80	0	Low Power Bipolar-JFET	**TL062AC**	**TI**	**(3425)**	
										TL062M	**†TI**	**(3425)**	
				3 *	13 *	50K	80	0	Bipolar JFET	**XR082**	**Exar**	**(3206)**	
										XR082M	**†Exar**	**(3206)**	
										XR083	**Exar**	**(3206)**	
										XR083M	**†Exar**	**(3206)**	
										TL082AC	TI		20
										TL082M	† TI		
										TL083AC	TI		
										TL083M	† TI		
	10	6	3 *	1 *	15 *	50K	70	0	Multi-Purpose Programmable	µA776C	Fairchild		
	30	10	—	0.25 *	0.16 *	75K	70	0	Programmable Dual LM4250	LH24250C	National		
			5 *	0.27 *	0.16 *	50K	70	0	Low Power Adjustable Current	ICL8022C	Intersil		
	75	10	—	0.4	1.5	100K	80	—	Ultra-Low Power	**HA-5142A**	**Harris**	**(3266)**	
	150	40	6 *	1 *	10	50K	70	0	High Slew Rate	NE5535	Signetics		
	250	50	7 *	1 *	0.6 *	25K	65	0	Half LM244/324	LM258	Motorola		
										LM358	Motorola		30
										NE532	Signetics		
		75	10 *	1 *	0.6 *	20K	70	0	Single Supply, I/O Operates to Ground	µA798C	Fairchild		
	500	200	—	—	0.5 *	5K	70	0	Dual 221	TBB0747	Siemens		
										TBB1458	Siemens		
					1 *	20K	70	0	Wideband 741	µPC4557	NEC-Electron		
					2 *	20K	70	0	Wideband 741	µPC4559	NEC-Electron		
					5 *	20K	70	0	Wideband 741	µPC4556	NEC-Electron		
				1 *	0.5 *	20-50K	70	0	Dual 741C	IC900	Cherry		
										XR1458	Exar		
										µA1458C	Fairchild		40
										µA747C	Fairchild		
										MC1458	Motorola		
										MC1747C	Motorola		
										LM1458	National		
										LM747C	National		
										µPC1458	NEC-Electron		
										µPC251	NEC-Electron		
										AN6550	Panasonic		
										AN6551	Panasonic		
										AN6552	Panasonic		50
										PM747C	PMI		
										RC747	Raytheon		
										CA747C	RCA		
										µA747C	Signetics		
										SG747C	Silicon G		
										µA747C	TI		
				2	0.5 *	20K	70	0	Dual Wideband 741C	MC4558C	Motorola		
									Low Noise	MC4558NC	Motorola		
					1	50K	70	0	General Purpose	NE4558	Signetics		
				3	1.5	20K	70	0	3 MHz Min. Bandwidth	RC4559	Raytheon		60
										RV4559	Raytheon		
				3 *	1	20K	70	0	Low Noise	RC4739	Raytheon		
									Wideband 741	XR4558	Exar		

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift µV/°C	Band-width MHz	Slew Rate V/µs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source	Line
Dual Units											**(Cont'd)**	
6.0	500	200	—	3 *	1	20K	70	0	Wideband 741		(Cont'd)	
										µPC4558	NEC-Electron	
										RC4558	Raytheon	
										RC4558	TI	
									Low Noise	XR4739	Exar	
				10 *	2.8 *	20K	70	0	Wideband 741	µPC4560	NEC-Electron	
			10 *	1 *	0.8 *	20K	70	0	Low Noise	MC1458N	Motorola	
					10	20K	70	0	High Slew Rate 1458	MC1458S	Motorola	
	2000	1000	—	—	1 *	6.5K	70	2	Low Noise	µA739	Fairchild	
7.0	100	10	—	0.4	1	100K	77	—	Ultra-Low Power	**HA-5142**	**Harris (3266)**	
	200	50	—	—	—	25K	65	0	Single Supply	TL321C	TI	10
	250	50	7 *	1 *	—	25K	65	0	Half LM224	µPC1251	NEC-Electron	
										µPC358	NEC-Electron	
7.5	7	1	30	1 *	0.3 *	25K	80	1	Dual 308	**LH2308**	**National (3342)**	
										PM2308	PMI	
	250	50	30	1 *	0.5 *	25K	70	1	Dual High Performance	LH2301A	AMD	
										LH2301A	Intersil	
										LH2301A	**National (3342)**	
	1500	500	1.5 *	1 *	0.25 *	15K	65	3	Matched Dual MC1709C	MC1437	Motorola	
					0.3 *	15K	65	3	Matched Dual 709	RC1437	Raytheon	
8.0	500	75	10 *	1 *	0.6 *	20K	70	0	Low Power	TL322M	TI	20
9.0	0.40	0.20	10 *	1 *	0.6 *	200K	70	0	JFET Input	TL092M	† TI	
10.0	0.10	0.03	10	3	10	100K *	100 *	1	JFET Input	MA336	Analog Sys	
		0.10	10 *	4 *	13 *	25K	70	0	BIFET	**MC34002**	**Motorola (3293)**	
									Precision BIFET	**MC35002**	**Motorola (3293)**	
	0.20	0.05	10 *	3 *	13 *	25K	70	0	Low Noise Bipolar-FET	MCE72	Micro Eng	
										TL072C	**TI (3427)**	
							80	0	Low Noise Bipolar-JFET	**TL072AC**	**TI (3427)**	
										TL072BC	**TI (3427)**	
		0.10	10 *	3 *	13 *	50K	70	0	Bipolar JFET	µAF772	Fairchild	
				4 *	13 *	25K	70	0	Dual 351, Wide Band	**LF353**	**National (3309,3326)**	30
										SE571	† Signetics	
	500	75	10 *	1 *	0.6 *	20K	70	0	Low Power	TL322C	TI	
	700	300	15 *	1.1 *	0.5 *	20K	60	0	General Purpose	MC1458C	Motorola	
	1500	600	—	—	—	10K	70	0	Audio Preamp	µA749D	Fairchild	
15.0	0.050	0.030	8 *	4 *	10 *	50K *	70	0	Dual 3160	**CA3260E**	**RCA (3349)**	
										CA3260T	**† RCA (3349)**	
			10 *	5 *	13 *	50K	70	0	MOS/FET Input, Bipolar/MOS Output	**CA082**	**RCA (3348)**	
										CA083	**RCA (3348)**	
						200K	76 *	0	MOS/FET Input, Bipolar/MOS Output	**CA082C**	**RCA (3348)**	
										CA083C	**RCA (3348)**	40
			25 *	1 *	1.6	80K *	70	0	Low Power, Dual 1458	ICL7621DC	Intersil	
									Low Power, Dual 747	ICL7622DC	Intersil	
	0.20	0.10	10 *	3 *	13 *	50K	70	0	Bipolar JFET	µAF772L	Fairchild	
	0.4	0.2	10 *	1 *	3.5 *	3K	70	0	Low Power Bipolar-JFET	**TL062C**	**TI (3425)**	
				3 *	11 *	25K	70	0	Bipolar-JFET	µPC4082	NEC-Electron	
					13 *	25K	70	0	Bipolar-JFET	**XR082C**	**Exar (3206)**	
										XR083C	**Exar (3206)**	
										MCE82	Micro Eng	
										MCE83	Micro Eng	
										TL082C	TI	50
										TL083C	TI	
	0.40	0.20	10 *	1 *	0.6 *	200K	70	0	JFET Input	TL092C	TI	
	50	25	12 *	—	18 *	3K	65	0	Darlington Input	TBB2331	Siemens	
	200	100	30	—	2	10K	40	0	Power Op Amp, Comp. for G>30	MA208	Analog Sys	
20.0	0.02	0.0005 *	75	1 *	6 *	50K	70	0	FET Input Dual	ICL8043M	† Intersil	
50.0	0.05	0.0005 *	75	1 *	6 *	20K	70	0	FET Input Dual	ICL8043C	Intersil	
Triple Units												
3.0	0.03	0.01	5 *	0.27	0.1	5K	70	0	Low Power, Programmable	**HA-8023-2**	**† Harris (3282,3287)**	

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR-Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift µV/°C	Band-width MHz	Slew Rate V/µs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source	Line
Triple Units											**(Cont'd)**	
5.0	0.050	0.030	10 *	1	1.6	80K *	70	0	Low Power	ICL7631BC ICL7631BM	Intersil † Intersil	
								1	Low Power	ICL7632BC ICL7632BM	Intersil † Intersil	
	70	14	—	0.02 *	0.1 *	—	70	0	Micropower, Transconductance Amplifier	CA3060	† RCA	
6.0	0.03	0.01	5 *	0.27	0.1	5K	70	0	Low Power, Programmable	**HA-8023-5**	**Harris (3282,3287)**	
10.0	0.050	0.030	20 *	1	1.6	80K	70	0	Low Power	ICL7631CC ICL7631CM	Intersil † Intersil	
								1	Low Power	ICL7632CC ICL7632CM	Intersil † Intersil	10
	2000	200 *	—	5	0.46	4K *	90 *	2	Supply +-6 V	TCA220	Signetics	
20.0	0.050	0.030	30 *	1	1.6	80K	70	0	Low Power	ICL7631EC	Intersil	
								1	Low Power	ICL7632EC	Intersil	
Quad Units												
0.5	0.075	0.025	10 *	4 *	13 *	50K	80	0	Precision BIFET	**MC35004A**	**† Motorola (3293)**	
	300	20	10	1.5	0.7	100K	100	0	Symmetrical, Matched	**MP5509A**	**† Micro Pwr (401,3292)**	
										MP5509E	**Micro Pwr (401,3292)**	
										MP5511A	**† Micro Pwr (401,3292)**	
										MP5511E	**Micro Pwr (401,3292)**	
										OP-09A OP-09E	† PMI PMI	20
										OP-11A OP-11E	† PMI PMI	
2.0	0.10	0.05	10 *	4 *	13 *	50K	80	0	Precision BIFET	**MC34004A**	**Motorola (3293)**	
	0.2	0.1	8.3 *	0.24	15 *	50K	80	—	JFET Input	**HA-5084B-5**	**Harris (3258,3287)**	
	50	10	20	1 *	—	50K	70	0	Low Power	LM124A	† National	
2.5	50	5	10	750 *	0.25 *	400K *	100K	0	Quad Micropower OP-21	OP-421B OP-421F	† PMI PMI	
	200	75	2 *	0.26	12	100K	86	0	Wideband; High Performance	**HA-4620-2**	**† Harris (3248,3287)**	
										HA-4620-5	**Harris (3248,3287)**	
				8 *	1	100K	86	0	High Performance	**HA-4600-2**	**† Harris (3246,3287)**	30
										HA-4600-5	**Harris (3246,3287)**	
										HS4602RH	† Harris	
					4 *	100K	86	0	Wideband	**HA-4602-2**	**† Harris (3246)**	
	500	50	15	1.5	0.7	100K	100	0	Symmetrical, Matched	OP-09B OP-09F	† PMI PMI	
										OP-11B OP-11F	† PMI PMI	
3.0	0.03	0.02	10 *	5 *	13 *	50K	80	0	MOS/FET Input, Bipolar/MOS Output	**CA084B**	**RCA (3348)**	
	0.2	0.1	10 *	0.63	2	20K	80	—	Low Power, JFET Input	**HA-5064B-5**	**Harris (3254,3287)**	
				1 *	3.5 *	4K	80	0	Low Power Bipolar-JFET	**TL064BC**	**TI (3425)**	40
				3 *	3	50K	80	0	JFET	TL084BC	TI	
	20	10	—	1 *	0.8 *	25K	74	0	Programmable	**HA-2740**	**† Harris (3242,3287)**	
						30K	100 *	0	Programmable	**HA-2740-2**	**† Harris (3242,3287)**	
	80	15	20	1 *	—	50K	70	0	Low Power	LM224A	National	
	100	30	30	1 *	—	25K	65	0	Low Power	LM324A LM324A	National TI	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift µV/°C	Band-width MHz	Slew Rate V/µs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source	Line
Quad Units											**(Cont'd)**	
3.0											(Cont'd)	
	200	30	5 *	0.02	1.3	100K	80	0	General Purpose	**HA-4156-2**	**† Harris (3244,3287)**	
				3	1.2	25K	80	0	Noise 2µV Max	RM4156	† Raytheon	
					1.6 *	50K	80	0	Quad 741	XR4741M	† Exar	
				3.5 *	1.6 *	50K	80	0	Quad 741	**HA-4741-2**	**† Harris (3250,3287)**	
										HA4741-2	† Raytheon	
				19 *	8 *	25K	80	0	Uncompensated 4156	RC4157	Raytheon	
										RM4157	† Raytheon	
	325	125	2 *	70 *	12	100K	86	0	Wideband, Comp. for g>10	**HA-4622-2**	**† Harris (3248,3287)**	
3.5	300	100	2 *	8 *	4 *	75K	80	0	Wideband	**HA-4605-5**	**Harris (3246)**	
4.0	125	12	15	750 *	0.25 *	200K	96 *	0	Quad, Micropower OP-21	OP-421C	† PMI	10
										OP-421G	PMI	
	400	50	5 *	1 *	1.2 *	50K	70	0	LM124 with Improved Output	RM3503A	† Raytheon	
		120	2 *	70 *	11	75K	80	0	Wideband, Comp. for g>10	**HA-4625-5**	**Harris (3248,3287)**	
5.0	0.050	0.030	15 *	1	1.6	80K	70	0	Low Power	ICL7641BC	Intersil	
										ICL7641BM	† Intersil	
										ICL7642BC	Intersil	
										ICL7642BM	† Intersil	
		0.050	10	1	1	50K	80	0	Low Power BIFET	**LF444A**	**National (3309,3315)**	
	0.10	0.05	10 *	4 *	13 *	50K	80	0	Precision BIFET	**MC35004B**	**† Motorola (3293)**	
		0.10	10 *	3 *	13 *	50K	80	0	Bipolar JFET	µAF774B	Fairchild	20
										µAF774BM	† Fairchild	
	0.20	0.10	8.3 *	0.24	15 *	50K	80	—	JFET Input	**HA-5084-2**	**† Harris (3258,3287)**	
										HA-5084A-5	**Harris (3258,3287)**	
			10 *	4 *	13 *	50K	80	0	Precision BIFET	**MC34004B**	**Motorola (3293)**	
									Wideband, Quad 351B	**LF347B**	**National (3309,3326)**	
	30	10	—	1 *	0.8 *	25K	74	0	Programmable	**HA-2740-5**	**Harris (3242,3287)**	
	100	25	—	1 *	0.5 *	50K	70	0	Quad 741 with Standard npn Input Stage	LM148	† AMD	
										µA148	† Fairchild	
										LM148	**† Harris (3286,3288)**	
										LM148	† Motorola	30
										LM148	† Raytheon	
										LM148	† TI	
				4 *	2.0 *	50K	70	0	Wideband Quad 741 for Gains >5	LM149	† National	
										LM149	† Raytheon	
		40	—	0.8 *	0.5 *	4K	60	0	Low Power	TL044M	† TI	
	250	80	—	0.8 *	0.5 *	1K	60	0	Low Power	TL044C	TI	
	300	50	5 *	0.02	1.3	50K	60	0	General Purpose	**HA-4156-5**	**Harris (3244,3287)**	
				3	1.2	25K	80	0	Noise 2 µV Max	RC4156	Raytheon	
										RV4156	Raytheon	
				3 *	1.6 *	25K	80	0	Quad 741	µPC4741	NEC-Electron	40
				3.5 *	1.6 *	25K	80	0	Quad 741	XR4741C	Exar	
										HA-4741-5	**Harris (3250,3287)**	
										HA4741-5	Raytheon	
	500	50	—	2 *	1.5 *	5K	70	0	Programmable Quad 741	MC4202	Motorola	
					1.6 *	20K	70	0	Low Noise, Low Power	XR4212M	† Exar	
			10	1	0.6	200K	90	0	Low Power	MC3503	Signetics	
		200	—	3 *	1.5 *	50K	70	0	Quad 741, High Gain	XR4136M	† Exar	
										µA4136M	† Fairchild	
										MP4136	**Micro Pwr (3292)**	
										PM4136	† PMI	50
										RM4136	† Raytheon	

(Continued)

† Military Temperature Range (−55° to 125°C) * Typical Value

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LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift µV/°C	Band-width MHz	Slew Rate V/µs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source	Line
Quad Units											**(Cont'd)**	
											(Cont'd)	
5.0	500	200	—	3.5	1.5	96	110	0	Programmable	TAB1042	Plessey	
										TAB1043	Plessey	
			15 *	1	0.5 *	50K	70	0	Quad 741	MC4741	† Motorola	
6.0	0.04	0.02	10 *	5 *	13 *	50K	80	0	MOS/FET Input, Bipolar/MOS Output	**CA084A**	**RCA (3348)**	
	0.2	0.05	—	8	20	50K	80	0	FET, Wideband	MC3571	† Motorola	
			10 *	3 *	13 *	50K	80	0	Low Noise Bipolar-JFET	MCE74	Micro Eng	
										TL074M	**† TI (3427)**	
		0.1	10 *	0.63	2	20K	80	—	Low Power, JFET Input	**HA-5064-2**	**† Harris (3254,3287)**	
										HA-5064A-5	**Harris (3254,3287)**	
				1 *	3.5 *	4K	80	0	Low Power Bipolar-JFET	**TL064AC**	**TI (3425)**	10
				3 *	13 *	50K	80	0	Bipolar JFET	**XR084**	**Exar (3206)**	
										XR084M	**† Exar (3206)**	
										MCE84	Micro Eng	
										TL084AC	TI	
										TL084M	† TI	
										TL085AC	TI	
									Indiv. Program	XR096	Exar	
										XR096M	† Exar	
									Programmable, Bipolar - FJET	XR094	Exar	
										XR094M	† Exar	20
										XR095	Exar	
										XR095M	† Exar	
	75	10	—	0.4	1.5	100K	80	—	Ultra-Low Power	**HA-5144A**	**Harris (3266)**	
	200	50	—	1 *	0.5 *	25K	70	0	Quad 741 with Standard npn Input Stage	LM248	AMD	
										LM348	AMD	
										µA248	Fairchild	
										µA348	Fairchild	
										LM348	**Harris (3286,3288)**	
										LM248	National	
										LM348	National	30
										LM248	Raytheon	
										LM348	Raytheon	
										LM248	TI	
										LM348	TI	
				4 *	2 *	25K	70	0	Wideband Quad for Gains >5	LM249	National	
										LM349	National	
										LM249	Raytheon	
										LM349	Raytheon	
	250	20	25	750 *	0.25 *	200K *	90 *	0	Quad OP-21	OP-421H	PMI	
	500	50	—	1 *	1.2 *	25K	70	0	LM324 with Improved Output	RC3403A	† Raytheon	40
				2	1.6	5K	70	0	Quad 741	XR4212C	Exar	
		100	—	1	0.4 *	20K	70	0	346 w/Sep Bias Resister for Each Pair	**XR346-2**	**Exar (3207)**	
		200	—	1 *	0.5 *	20K	70	0	Quad 741	MC4741C	Motorola	
				3 *	1 *	20K	60-70	0	Quad 741	XR4136C	Exar	
										µA4136C	Fairchild	
										MP4136C	**Micro Pwr (3292)**	
										RC4136	Raytheon	
										RV4136	Raytheon	
										SG4136	† Silicon G	
										SG4136C	Silicon G	50
										RC4136	† TI	
					2.4 *	20K	70	0	High Performance	TL136C	TI	
7.0	100	10	—	0.4	1	100K	77	—	Ultra-Low Power	**HA-5144**	**Harris (3266)**	
	150	30	—	—	—	20K	60	0	Single Supply	TA75902	Toshiba	
	250	50	—	—	—	25K	65	0	324 Type	TBB0324	Siemens	
	500	50	—	—	—	100K	50	0	Single Supply	µPC2902	NEC-Electron	
						100K *	85 *	0	324 Type	µPC451	NEC-Electron	
8.0	500	75	10	1	0.6	200K	90	0	Low Power	MC3303	Signetics	
			10 *	1 *	0.6 *	20K	70	0	Single Supply: I/O Operates to Ground	MC3303	TI	

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Operational Amplifiers–Characteristics (Cont'd)

Offset Voltage mV (25°C)	Bias Current nA (25°C)	Offset Current nA (25°C)	Voltage Drift µV/°C	Band-width MHz	Slew Rate V/µs	Voltage Gain V/V	CMRR dB	Comp.	Comments	Device	Source	Line
Quad Units											**(Cont'd)**	
9.0	0.2	0.1	10 *	1 *	3.5 *	4K	80	0	Low Power Bipolar-JFET	**TL064M**	**† TI (3425)**	
	0.40	0.20	10 *	1 *	0.6 *	200K	70	0	JFET Input	TL094M	† TI	
10.0	0.050	0.030	20 *	1 *	1.6 *	80K	70	0	Low Power	ICL7641CC	Intersil	
										ICL7641CM	† Intersil	
										ICL7642CC	Intersil	
										ICL7642CM	† Intersil	
	0.10	0.05	10	1	1	25K	70	0	Low Power BIFET	**LF444**	**National (3309,3315)**	
	0.20	0.05	0.10	5	15 *	25K	70	0	Bipolar-JFET, Quad 351	**LF347**	**National (3309,3326)**	
			10 *	3 *	13 *	25K	70	0	Low Noise Bipolar-JFET	**TL074AC**	**TI (3427)**	
										TL074BC	**TI (3427)**	10
										TL074C	**TI (3427)**	
										TL075C	**TI (3427)**	
		0.10	10 *	3 *	13 *	50K	70	0	Bipolar JFET	µAF774	Fairchild	
	0.20 *	0.05 *	10 *	1 *	0.6 *	20K	70	0	JFET Input	TL094C	TI	
										TL094M	† TI	
	500	50	10	1	0.6	200K	90	0	Low Power	MC3403	Signetics	
			10 *	1 *	0.6 *	20K	70	0	Single Supply: I/O Operates to Ground	µA3403	Fairchild	
										MC3403	TI	
15.0	0.05	0.03	10 *	5 *	13 *	25K	70	0	MOS/FET Input, Bipolar/MOS Output	**CA084**	**RCA (3348)**	
	0.20	0.10	10 *	3 *	13 *	50K	70	0	Bipolar-JFET	µAF774L	Fairchild	20
	0.40	0.2	8.3 *	0.24	15 *	25K	70	—	JFET Input	**HA-5084-5**	**Harris (3258,3287)**	
			10 *	1 *	3.5 *	3K	70	0	Low Power Bipolar-JFET	**TL064C**	**TI (3425)**	
				3 *	11 *	25K	70	0	Bipolar-FET	µPC4084	NEC-Electron	
					13 *	25K	70	0	Bipolar-FET	**XR084C**	**Exar (3206)**	
										TL084C	TI	
										TL085C	TI	
									Indiv. Program.	XR096C	Exar	
									Programmable Bipolar-JFET	XR094C	Exar	
										XR095C	Exar	
			20 *	0.63	2	10K	70	—	Low Power, JFET Input	**HA-5064-5**	**Harris (3254,3287)**	30
		0.20	10 *	1 *	0.6 *	200K	70	0	JFET Input	TL094C	TI	
	50	25	12 *	—	—	3K	65	0	Darlington Input	TBB4331	Siemens	
										TBE4335	Siemens	
20.0	0.050	0.030	30 *	1	1.6	80K	70	0	Low Power	ICL7641EC	Intersil	
										ICL7642EC	Intersil	
30.0	0.050	0.100	15 *	1 *	0.8 *	1K *	70 *	0	Low Power	MC14573	Motorola	
Hex Units												
5	100	25	—	1.0	0.5	25K	70	0	Hex 741 W/NPN Input	TL326M	† TI	

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Phase Locked Loops/Synthesizers

Phase Locked Loops/ Synthesizers

CB device sets and support circuits are also found in Consumer Circuits

Count Extender, ÷4, ÷ 10/11 becomes ÷40/41

Device	Source	
SP8790A	† Plessey	
SP8790B	Plessey	

Count Extender, ÷8 (extends division ratio of a two modulus prescaler while retaining the difference, ie ÷ 10/ 10/11 becomes ÷80/81)

Device	Source	
SP8794A	† Plessey	
SP8794B	Plessey	

Counter Logic Control

Device	Source	
SP8790	Plessey	

Counter Logic Control (use with MC12012 for high frequency programming)

Device	Source	
MC12014	Motorola	

Crystal Oscillator (0.1 to 2.0 MHz)

Device	Source	
MC12060	Motorola	
MC12560	† Motorola	

Crystal Oscillator (2 to 20 MHz)

Device	Source		Line
MC12000	**Motorola**	**(733)**	10
MC12061	Motorola		
MC12561	† Motorola		

Crystal Oscillator (250 kHz to 60 MHz)

Device	Source	
CK1100A	Solarise	
CK1114A	Solarise	
CK1144A	Solarise	
CK1145A	Solarise	

Double Balanced Mixer

Device	Source	
MC12002	Motorola	
MC12502	† Motorola	

FSK Modulator/Demodulator

Device	Source		Line
XR210	**Exar**	**(3195)**	
XR210M	**† Exar**	**(3195)**	20
XR2211	**† Exar**	**(3195)**	
XR2211	Exar		
XR2211C	**Exar**	**(3195)**	
XR2211M	**† Exar**	**(3195)**	
XR2212M	**† Exar**	**(3196)**	
XR2211C	Raytheon		
XR2211M	† Raytheon		

Offset Control System (for synthesizer tuned transceivers)

Device	Source		Line
MC12020	Motorola		
MC12021	Motorola		
MC12520	† Motorola		30
MC12521	Motorola		

Phase Comparator and Programmable Counter

Device	Source	
MC14568BA	† Motorola	
MC14568BC	Motorola	

Phase Locked Loop

Device	Source		Line
XR215	Exar		
XR215M	† Exar		
SL652	Plessey		
SDA2002	Siemens		
SDA2112	Siemens		
NE564	Signetics		
SE564	† Signetics		40
SN54LS297	**† TI**	**(926)**	
SN74LS297	**TI**	**(926)**	

Phase Locked Loop (CMOS)

Device	Source		Line
F4046BC	Fairchild		
F4046BM	† Fairchild		
MC14046BA	† Motorola		
MC14046BC	Motorola		
CD4046BC	National		
CD4046BM	† National		
CD4046A	**† RCA**	**(748)**	
CD4046AE	**RCA**	**(748)**	50
CD4046B	**† RCA**	**(748)**	

(Continued)

Phase Locked Loop (CMOS) (Cont'd)

Device	Source		Line
CD4046BE	**RCA**	**(748)**	
883/4046B	† SSS		
883/4446B	† SSS		
SCL4046B	SSS		
SCL4446B	SSS		

Phase Locked Loop for Motor Control

Phase Locked Loop System (multiplier, VCO and Op Amp)

Device	Source	
XRS200	Exar	

Phase-Frequency Detector

Device	Source		Line
11C44C	Fairchild		
11C44M	† Fairchild		60
MC12040	Motorola		
MC12540	† Motorola		
MC4044	Motorola		
MC4344	† Motorola		

PLL Peripheral (VCO, mixer, amp for CB)

Device	Source	
AN103	Panasonic	
TA7310	Toshiba	

Prescaler

Device	Source	
SDA4040	Siemens	
SDA4041	Siemens	

Prescaler, Divide by 20

Device	Source	
MC3396	Motorola	

Prescaler, Divide by 64

Device	Source		Line
SDA2001	Siemens		70

Prescaler, for AM/FM

Device	Source	
TD6102	Toshiba	

Prescaler, for FM Radio

Device	Source	
DS8626	National	
DS8629	National	
SP8627	Plessey	
SP8628	Plessey	
SP8629	Plessey	

Prescaler for PLL Tuner, Divide by 8

Device	Source	
LB3500	Sanyo	

Prescaler for VHF/UHF, Divide by 64

Device	Source		Line
MC12071	Motorola		
DS8621	National		
CA3179	RCA		80

Prescaler for VHF/UHF, Divide by 4

Device	Source	
CA3199	**RCA**	**(3364)**

Prescaler for VHF/UHF, Dual Modulus

Device	Source	
DS8622	National	

Prescalers—see also Digital-Special, Dividers, Digital-ECL

Programmer, for CB Synthesizer

Device	Source	
MP7156	Micro Pwr	
MM57190	National	

Programmers and Controllers for Citizens Band See Linear-Consumer Circuits

Synthesizer, Marine Band (PLL)

Device	Source	
MN6043	Panasonic	
MN6141	Panasonic	
MN6143	Panasonic	

Synthesizer, Mobile Radio (2 device set)

Device	Source		Line
NJ8811	Plessey		90
NJ8812	Plessey		
SP8901	Plessey		
SP8906	Plessey		

Synthesizer, PLL

Device	Source		Line
HCTR0347	Hughes		
MC145104	Motorola		
MC145106	Motorola		
MC145107	Motorola		
MC145109	Motorola		
MC145112	Motorola		
MC145143	Motorola		100
MC145144	Motorola		
MC145145	Motorola		
MC145146	Motorola		

(Continued)

Synthesizer, PLL (Cont'd)

Device	Source		Line
MC145151	Motorola		
MC145152	Motorola		
MC145155	Motorola		
MC145156	Motorola		
MC145157	Motorola		
MC145158	Motorola		
MC145159	Motorola		110
MC6195	Motorola		
DS8906	National		
DS8907	National		
DS8908	National		
MM55108	National		
MM55110	National		
MM55121	National		
MM55123	National		
MM55124	National		
MM55126	National		120
μPD861	NEC-Electron		
MN6040	Panasonic		
MN6040A	Panasonic		
MN6040Z	Panasonic		
MN6041A	Panasonic		
MN6043A	Panasonic		
MN6043B	Panasonic		
MN6140	Panasonic		
MN6142	Panasonic		
LC7210	Sanyo		130
LC7220	Sanyo		
LC7225	Sanyo		
HEF4750	Signetics		
SAA1056	Signetics		
SAA1057	Signetics		
TC9106B	Toshiba		
TC9109B	Toshiba		
TC9111B	Toshiba		

Synthesizer (programmable divider, to 1021 channels, adder, phase comparator)

Device	Source	
HCTR0320	Hughes	

Synthesizer (programmable dividers, phase comparator)

Device	Source		Line
S187A	Siemens		140

Synthesizer, 150 Channel, Phase Comparator

Device	Source	
MP7149	Micro Pwr	

Synthesizer, 200 Channel, for AM/FM

Device	Source	
8X08	Signetics	

Tone Decoder

Device	Source		Line
XR2211C	Exar		
XR2211M	† Exar		
XR2213C	**Exar**	**(3196)**	
XR2213M	**† Exar**	**(3196)**	
XR567C	**Exar**	**(3194)**	
XR567M	**† Exar**	**(3194)**	
XRL567C	**Exar**	**(3194)**	
XRL567M	**† Exar**	**(3194)**	150
LM567	† National		
LM567C	National		
XR2211C	Raytheon		
XR2211M	† Raytheon		
NE567	Signetics		
SE567	† Signetics		

VCO

Device	Source		Line
11C58C	Fairchild		
MC1648	Motorola		
MC1648M	† Motorola		
MC1658	Motorola		160
SP1648	Plessey		
SP1658	Plessey		
SN54LS324	† TI		
SN54LS624	**† TI**	**(977)**	
SN54LS628	**† TI**	**(978)**	
SN74LS624	**TI**	**(977)**	
SN74LS628	**TI**	**(978)**	

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Phase Locked Loops/Synthesizers (Cont'd)

Phase Locked Loops/Synthesizers (Cont'd)

Function	Device	Source		Line
VCO and Phase Comparator				
	LM565	Motorola		
	NE565	Motorola		
	LM565	National		
	LM565C	† National		
	NE565	Signetics		
	SE565	† Signetics		
	TA7133	Toshiba		
VCO Function Generator, (Includes square and triangular waveforms - but not sine.)				
	XR2207	**Exar**	**(3198)**	
	XR2207C	**Exar**	**(3198)**	
	XR2209C	**Exar**	**(3197)**	10
	XR2209M	**† Exar**	**(3197)**	
	LM566	National		
	LM566C	† National		
	XR2207C	Raytheon		
	XR2207M	† Raytheon		
	NE566	Signetics		
	SE566	† Signetics		
VCO Phase Comparator, Multiplier				
	SL651	Plessey		
VCO Phase Comparator, Multiplier, with Auxiliary Amplifier				
	SL650	† Plessey		
VCO Waveform Generator (includes sinewave output among its functions)				
	XR205	Exar		20
	XR2206	**† Exar**	**(3197)**	
	XR2206	Exar		
	XR2206C	**Exar**	**(3197)**	
	XR2206M	**† Exar**	**(3197)**	
	XR8038	**Exar**	**(3198)**	
	XR8038A	**Exar**	**(3198)**	
	XR8038M	**† Exar**	**(3198)**	
	ICL8038C	Intersil		
	ICL8038M	† Intersil		
VCO, Dual	11C24C	Fairchild		30
	11C24M	† Fairchild		
	MC4024	Motorola		
	MC4324	† Motorola		
	SN54LS325	TI		
	SN54LS326	† TI		
	SN54LS327	† TI		
	SN54LS625	**† TI**	**(977)**	
	SN54LS626	**† TI**	**(977)**	
	SN54LS627	**† TI**	**(978)**	
	SN54LS629	**† TI**	**(978)**	40
	SN54S124	**† TI**	**(874)**	
	SN74LS124	TI		
	SN74LS325	TI		
	SN74LS326	TI		
	SN74LS327	TI		
	SN74LS328	TI		
	SN74LS625	**TI**	**(977)**	
	SN74LS626	**TI**	**(977)**	
	SN74LS627	**TI**	**(978)**	
	SN74LS629	**TI**	**(978)**	50
	SN74S124	**TI**	**(874)**	
Dual Tone Decoder				
	XR2567C	Exar		
	XR2567M	† Exar		
Two Modulus Prescaler (÷3/4)				
	SP8720	Plessey		
	SP8725	Plessey		
Two Modulus Prescaler (÷4/8)				
	11C91C	Fairchild		
	11C91M	† Fairchild		
	95H91C	Fairchild		
	95H91M	† Fairchild		
Two Modulus Prescaler (÷4/8) (Cont'd)				
	MC12009	Motorola		60
	MC12509	† Motorola		
	SP8740	Plessey		
	SP8745	Plessey		
	TD6102	Toshiba		
Two Modulus Prescaler (÷5/6)				
	MC12009	Motorola		
	MC12509	† Motorola		
Two Modulus Prescaler (÷5/6, 10/11, 10/12)				
	MC12012	Motorola		
Two Modulus Prescaler (÷6/7)				
	SP8741	Plessey		
	SP8746	Plessey		
Two Modulus Prescaler (÷8/9)				
	MC12011	Motorola		70
	MC12511	† Motorola		
	SP8743	Plessey		
Two Modulus Prescaler (÷10/11)				
	11C90C	Fairchild		
	11C90M	† Fairchild		
	95H90C	Fairchild		
	95H90M	† Fairchild		
	MC12013	Motorola		
	MC12513	† Motorola		
	SP8643	Plessey		
	SP8647	Plessey		80
	SP8685	Plessey		
	SP8690	Plessey		
Two Modulus Prescaler (÷15/16)				
	MC3393	Motorola		
Two Modulus Prescaler (÷31/32)				
	11C79	Fairchild		
Two Modulus Prescaler (÷40/41)				
	SP8793	Plessey		
	SP8793A	Plessey		
Two Modulus Prescaler (÷64/256)				
	MC12071	Motorola		
	DS8621	National		
	CA3163	RCA		
	CA3179	**RCA**	**(3363)**	90
Two Modulus Prescaler (÷80/81)				
	SP8792	Plessey		
	SP8792A	Plessey		
Two Modulus Prescaler (÷248/256)				
	11C82	Fairchild		
	11C83	Fairchild		
	SAB1077	Signetics		
Four Modulus Prescaler (÷256/512)				
	SP8901	Plessey		
	SP8906	Plessey		

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Telecommunication Circuits

Telecommunication Circuits

Function	Device	Source	
Address Selector (gives output if sequential input is entered in a fixed order within a maximum time)	7511-01	Telaris	
Amplifier, Microphone	SL792	Plessey	
	SL793	Plessey	
Amplifier, Telephone Handset	TEA1045	ITT	
Antiope Character Generator, Europe	SAA5151	Signetics	
Antiope Character Generator, French	SAA5150	Signetics	
Antiope Character Generator, USA	SAA5155	Signetics	
Antiope Timing Circuit, 525 Lines	SAA5125	Signetics	
Antiope Timing Circuit, 625 Lines	SAA5120	Signetics	
Bandpass Filters	R5602	Reticon	
	R5604	Reticon	
	R5605	Reticon	
	R5606	Reticon	
	R5609	Reticon	
	R5610	Reticon	
	R5611	Reticon	
	R5612	Reticon	
	R5613	Reticon	
Bandpass Filters (touchtone)	**S3525A**	**AMI**	**(3146)**
	S3525B	**AMI**	**(3146)**
	S3526A	**AMI**	**(3147)**
	S3526B	**AMI**	**(3147)**
	ITT3040A	Aptek	
	ITT3041A	Aptek	
	ITT3044	Aptek	
	ITT3045	Aptek	
	CH1295	Cermetek	
	CH1296	Cermetek	
	G8865	GTE Micro	
	MT8865	Mitel	
	AF101	National	
	AF102	National	
	AF103	National	
	AF121	National	
	AF122	National	
Bandsplit Filter, DTMF	S3525A	AMI	
	S3525B	AMI	
	G8865X	GTE Micro	
	MV8865	Plessey	
	TT6177	Teltone	
Click Suppressor	ZSY0	ITT	
Codec, A Law	5156	Fairchild	
	HC5156A	**Harris**	**(2737)**
	2911A	Intel	
	MK5156	Mostek	
	TP3021	**National**	**(3332)**
	TP5156	**National**	**(3337)**
	TP5156A	**National**	**(3337)**
	μPD7711	NEC-Electron	
	MJ1480	Plessey	
	SL1480	Plessey	
	CD22404	**RCA**	**(749)**
	M090	SGS	
	M5156	SGS	
	S0291	Siemens	
	DF341A	Siliconix	

(Continued)

Function	Device	Source	
Codec, A Law (Cont'd)	DF342A	Siliconix	
	TCM2911A	TI	
Codec/Filter, A Law	**S3506**	**AMI**	**(3145)**
	MT8961	Mitel	
	MT8963	Mitel	
Codec/Filter, A Law, Asynchronous	S3508	AMI	
Codec/Filter, A Law PCM	S3503	AMI	
	S3504	AMI	
Codec/Filter, Parallel Data Interface	**TP3051**	**National**	**(3334)**
	TP3056	**National**	**(3334)**
Codec/Filter, Pin Selectable μLaw or A Law	2913	Intel	
	2914	Intel	
	MC14403	**Motorola**	**(3298)**
	MC14405	**Motorola**	**(3298)**
	TCM2913	TI	
	TCM2914	TI	
Codec/Filter, Serial Interface	**TP3052**	**National**	**(3335)**
	TP3053	**National**	**(3335)**
	TP3054	**National**	**(3335)**
	TP3057	**National**	**(3335)**
Codec/Filter, μ255 Law	**S3507**	**AMI**	**(3145)**
	S3507A	**AMI**	**(3145)**
	MT8960	Mitel	
	MT8962	Mitel	
	MK5300	Mostek	
Codec/Filter, μ255 Law, Asynchronous	S3509	AMI	
	S3509A	AMI	
Codec/Filter, μ255 Law PCM	S3505	AMI	
	S3505A	AMI	
Codec, μ255/A Law	ZNPCM1	Ferranti	
	AY3-9900	GI	
	HC5117A	**Harris**	**(2737)**
	MC14404	**Motorola**	**(3298)**
	MC14407	**Motorola**	**(3298)**
	TP5117A	**National**	**(3337)**
	S291	Siemens	
	SM61C	Siemens	
Codec, μ255 Law	5116	Fairchild	
	5151	Fairchild	
	HC5116A	**Harris**	**(2737)**
	2910	Intel	
	2910A	Intel	
	MK5116	Mostek	
	MK5151	Mostek	
	MC14406	**Motorola**	**(3298)**
	TP3020	**National**	**(3332)**
	TP5116	**National**	**(3337)**
	TP5116A	**National**	**(3337)**
	μPD7710	NEC-Electron	
	CD22406	**RCA**	**(749)**
	CD22407	**RCA**	**(749)**
	M5116	SGS	
	ST101	Signetics	
	TCM2910A	TI	
	TCM4110	TI	
	TCM4910	TI	
Companding A/D and D/A Converter	MM8100	National	

Function	Device	Source	
Companding Analog to Digital Converter	MN5110	Micro Net	
	MN5111	Micro Net	
	DF331A	Siliconix	
Companding Digital to Analog Converter	DF332A	Siliconix	
Compandor (signal expander/compressor)	XR2216	Exar	
	NE570	**Signetics**	**(3391)**
	NE571	**Signetics**	**(3391)**
	NE572	Signetics	
	SA571	**† Signetics**	**(3391)**
	SE570	† Signetics	
Crosspoint Switch (double 4x4 matrix)	RC4444	Raytheon	
	RM4444	Raytheon	
Crosspoint Switch (2x8 matrix)	M089	SGS	
	M099	SGS	
Crosspoint Switch (4x4 matrix with control memory)	**MC142100**	**Motorola**	**(3298)**
	MC145100	**† Motorola**	**(3298)**
	μPD22100	NEC-Electron	
	CD22100	**RCA**	**(749,753)**
	M22100	SGS	
Crosspoint Switch (4x4x2 with control memory)	**CD22101**	**RCA**	**(749,754)**
	CD22102	**RCA**	**(749,754)**
Crosspoint Switch (8x4 switch matrix)	MT8804A	Mitel	
	MT8804B	† Mitel	
CTCSS (continuous tone-controlled squelch system) Encoder/Decoder	MC1938	NEC-Electron	
	MC4137	NEC-Electron	
	MC4138	NEC-Electron	
Delta Modulation System, Continuously Variable Slope	**XR3417**	**Exar**	**(3187)**
	XR3418	**Exar**	**(3187)**
	XR3517	Exar	
	XR3518	Exar	
	HC55516-2	**† Harris**	**(2739,3287)**
	HC55516-8	**† Harris**	**(2739,3287)**
	HC55516-9	**Harris**	**(2739,3287)**
	HC55532-2	† Harris	
	HC55532-8	† Harris	
	HC55532-9	Harris	
	HC55536	Harris	
	MC3417	Motorola	
	MC3418	Motorola	
	MC3517	† Motorola	
	MC3518	† Motorola	
Delta Sigma Modulator/Demodulator	ZNPCM2	Ferranti	
Dialer, Microcomputer (clock, duration, fee pulse counter, redial, storage)	SAA6002	ITT	
	MK5170	Mostek	
	PCD3340	Signetics	
Dialer, Microcomputer (clock, stopwatch, redial, 16/32 number)	TZ2001	GI	
	TZ2002	GI	
	TZ2003	TI	
Dialer, Loop Disconnect	DF820	ITT	
	DF821	ITT	
	DF822	ITT	
	DF823	ITT	

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† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Telecommunication Circuits (Cont'd)

Telecommunication Circuits (Cont'd)

Function	Device	Source	Line
Dialer, Loop Disconnect (Cont'd)			
	M760	SGS	
	M760A	SGS	
Dialer, Push Buton Telephone Dialer Circuit (converts push button inputs to pulses)			
	S2560A	AMI	
	AY5-9151	GI	
	AY5-9153	GI	
	AY5-9154	GI	
	DF320	ITT	
	MT4320	Mitel	
	MT4322	Mitel	
	MT4323	Mitel	10
	MT4325	Mitel	
	MT4326	Mitel	
	MT4327	Mitel	
	MK50981	Mostek	
	MK50982	Mostek	
	MK50991	Mostek	
	MK50992	Mostek	
	MC14408	**Motorola (3298)**	
	MC14409	**Motorola (3298)**	
	MM53143	National	20
	MM53144	National	
	MM53190	National	
	MM5393	National	
	MM5394	National	
	NC2000	Nitron	
	NC2001	Nitron	
	NC2320	Nitron	
	NC2321	Nitron	
	NC2322	Nitron	
	CRC8000	Rockwell	30
	CRC8001	Rockwell	
	M761	SGS	
	M761A	SGS	
	PCD3320	Signetics	
	PCD3321	Signetics	
	PCD3322	Signetics	
	PCD3323	Signetics	
	TCD3311	Signetics	
	TCD3312	Signetics	
	TDA1077	Signetics	40
	TEA1021	Signetics	
	TEA1043	Signetics	
	TEA1044	Signetics	
	DF320	Siliconix	
	DF320A	Siliconix	
	DF322	Siliconix	
	DF328	Siliconix	
	TCM1101	TI	
Dialer, Repertory			
	S25610	**AMI (3141)**	
	S2562	AMI	50
	S2563	**AMI (3140)**	
	CET200	Fairchild	
	MK5175	Mostek	
	SFF19200	Thomson-CSF	
Digital Filter with Utility Peripheral			
	S28215	AMI	
Digital Line Interface Controllers			
	TP3110	**National (3336)**	
	TP3120	**National (3336)**	
Digital Timer/Space Switch			
	MT8980	Mitel	
Echo Canceller Peripheral			
	S28216	AMI	
Elastic Store (provides buffer store and justification function in a 2nd order PCM multiplexer)			
	TCM2401	TI	60
Encoder 8 of 8 Keyboard to Binary Encoder (4x4 key input to 4 line output)			
	MC14419	**Motorola (3298)**	
Filter, Codec (A law/μlaw)			
	MB6001	Fujitsu	
	MB6002	Fujitsu	
	MC14400	**Motorola (729,3298)**	
	MC14401	**Motorola (3298)**	
	MC14402	**Motorola (3298)**	
	MC14403	Motorola	
	MC14405	Motorola	
Filter, PCM	ITT3064	Aptek	
	ITT3065	Aptek	70
	HC5512	**Harris (2730,3287)**	
	HC5512A	**Harris (2730,3287)**	
	MT8912	Mitel	
	AF132	National	
	AF133	National	
	AF134	National	
	MC4264	NEC-Electron	
	SM153	Siemens	
	TCM2912A	TI	
Filter, PCM Transmit/Receive			
	G8912	GTE Micro	80
	2912A	Intel	
	MT8912	Mitel	
	MK5912	Mostek	
	MK8912	Mostek	
	MC14413-1	**Motorola (3298)**	
	MC14413-2	**Motorola (3298)**	
	MC14414-1	**Motorola (3298)**	
	MC14414-2	**Motorola (3298)**	
	TP3040	National	
	TP3040A	National	90
	CD22413	**RCA (749)**	
	CD22414	**RCA (749)**	
	M5912	SGS	
Filter, Speech (dual, tunable low-pass)			
	MC145414	Motorola	
Filter, Tunable (lowpass/bandpass)			
	MC145431	**Motorola (3298)**	
Filter, Tunable (notch, bandpass)			
	MC145433	**Motorola (3298)**	
	MC145434	**Motorola (3298)**	
Gyrator	**AF120**	**National (3345)**	
HDB3 Transcoder			
	TCM2201	TI	
IR Receiver	SM802	Siemens	100
IR Transmitter	SM801	Siemens	
Limiter (limits voltage on two-wire speech)			
	U225	Telefunken	
Modem Circuit, V23 or Bell 202			
	TCM3101	TI	
Modem Circuits, for CCITT FSK System			
	CH1225	Cermetek	
	CH1253	Cermetek	
	CH1258	Cermetek	
	CH1259	Cermetek	
	CH1263	Cermetek	
	CH1268	Cermetek	
Modem Circuits, for 103/113 and Other FSK Systems			
	CH1222	Cermetek	110
	CH1223	Cermetek	
	CH1224	Cermetek	
	CH1252	Cermetek	
		(Continued)	
Modem Circuits, for 103/113 and Other FSK Systems (Cont'd)			
	CH1257	Cermetek	
	CH1262	Cermetek	
	CH1265	Cermetek	
	CH1266	Cermetek	
	CH1267	Cermetek	
	CH1271	Cermetek	
	CH1272	Cermetek	120
	CH1273	Cermetek	
	CH1280	Cermetek	
Modem, DTMF	7900	Telaris	
Modem Filter, General Purpose (bandpass filter and MUX)			
	R5633	Reticon	
Modem Filter, 212/V.22, 1200 Baud			
	R5632	Reticon	
Modem Filter (300 baud)			
	MC145440	**Motorola (3298)**	
	MC145441	**Motorola (3298)**	
	MC6170	Motorola	
Modem Filter (1200 baud)			
	CH1710	Cermetek	
	CH1720	Cermetek	130
	CH1730	Cermetek	
	CH1740	Cermetek	
Modem Filter (1200/2400 baud)			
	MC6862	**Motorola (1351)**	
Modem (for serial communications at up to 600 b/s)			
	MC6860	**Motorola (1351,3298)**	
Modem (frequency-shift keying modulator/demodulator)			
	MC14412	**Motorola (3298)**	
	ESM501	Thomson-CSF	
Modem, FSK Demodulator			
	XR2211	† Exar	
	XR2211	Exar	
	XR2211M	† Exar	
Modem, FSK Modulator			
	XR2206	† Exar	140
	XR2206	Exar	
	XR2206M	† Exar	
	XR2207	Exar	
	XR2207M	**Exar (3198)**	
Modem Interface and Receiver Filter Circuit (300 baud modem)	CH1230	Cermetek	
Modem System, FSK			
	XR14412F	**Exar (3187)**	
	XR14412V	**Exar (3187)**	
Modem, 2400 bps Demodulator			
	MC6173	**Motorola (3298)**	
Multifrequency Interface Line Circuit			
	LS342	SGS	
PCM Repeater	XR-C240	Exar	150
	XR-C262	Exar	
	XR-C277	Exar	
	RPT-81	PMI	
	TCM2101	TI	
PCM Signal Monitor			
	SP1450B	Plessey	
	SP1455B	Plessey	
Polarity Guard Bridge			
	TCM1703	TI	
Polynomial Generator/Checker (for character-oriented data communication links)			
	SCN2653A	**Signetics (1520)**	
RC Decoder, Two Channel			
	NE5046	Signetics	
RC Encoder, Programmable 7-Channel			
	NE5044	Signetics	160

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Telecommunication Circuits (Cont'd)

Telecommunication Circuits (Cont'd)

Function	Device	Source	
RD Decoder, Seven Channel	NE5045	Signetics	
Receiver, DTMF (hybrid)	MH88315	Mitel	
	MH88305	Mostek	
Receiver, Hex DTMF	7904	Telaris	
Receiver, 1x16 DTMF	7916	Telaris	
Receiver, 2x8 DTMF	7908	Telaris	
Relay Driver (for 48 V telephone relays)	DS1686	† National	
	DS1687	† National	
	DS3686	National	
	DS3687	National	
	UDN-2580A	**Sprague**	**(2843)**
	UDN-2585A	**Sprague**	**(2843)**
	UDN-2588A	**Sprague**	**(2843)**
	UDN-2956A	Sprague	
	UDN-2957A	Sprague	
Ring Detector (operates from 16 to 68 Hz)	TCM1520	TI	
Serial Receiver (changes T1-D2 or T1-D3 input to parallel output)	R8060	Rockwell	
Serial Transmitter (generates 193-Bit data stream in T1-D2 or T1-D3 format)	R8050	Rockwell	
Signal Processing Peripheral (arithmetic processor, RAM, ROM, I/O)	**S28211A**	**AMI**	**(3142)**
	S28211B	**AMI**	**(3142)**
Speech Circuit for Electronic Telephones	PBL3725	RIFA	
	PBL3726	RIFA	
	TCM1705A	TI	
	TCM1706	TI	
Subscriber Line Interface Circuit (performs 2-wire to 4-wire conversion)	ITT2001	Aptek	
	ITT2002	Aptek	
	ITT3081	Aptek	
	ITT3082	Aptek	
	ITT3084	Aptek	
	ITT3085	Aptek	
	HC5501	Harris	
	MH88500	Mitel	
	MH88500	Mostek	
	MC3419	**Motorola**	**(2756)**
	MC3419A	**Motorola**	**(2756)**
	MC3419C	**Motorola**	**(2756)**
	MC3519	Motorola	
	CD22419	**RCA**	**(749)**
	G150	Siemens	
	TCM4204	TI	
	TCM4205	TI	
Telephone Restricter	CRN3300	Thomson-CSF	
Telephone Speech Circuit (programmable)	LS288	SGS	
Teletex Acquisition/Control	SAA5040	Signetics	
Teletex Adaptive Data Slicer (provides data, clock and synchronizing signals)	SN76940	TI	
Teletex Character Generator, American	SAA5055	Signetics	
Teletex Character Generator, British	SAA5050	Signetics	
Teletex Character Generator, German	SAA5051	Signetics	
Teletex Character Generator, Swedish	SAA5052	Signetics	
Teletex Timing Circuit, 525 Lines	SAA5025A	Signetics	
	SAA5025B	Signetics	
	SAA5025C	Signetics	
Teletex Timing Circuit, 625 Lines	SAA5020	Signetics	
Teletex Video Input Processor	SAA5030	Signetics	
Time Slot Access Circuit	MJ1446	Plessey	
Time Slot Asigner Circuit	**MC14416**	**Motorola**	**(3298)**
	MC14417	**Motorola**	**(3298)**
	MC14418	**Motorola**	**(3298)**
	CD22416	**RCA**	**(749)**
	CD22417	**RCA**	**(749)**
	CD22418	**RCA**	**(749)**
Tone Caller	ZN473E	Ferranti	
Tone Decoder (operates from 0.01 Hz to 500 kHz)	XR2211C	Exar	
	XR2211M	† Exar	
	XR567C	Exar	
	XR567M	† Exar	
	LM567C	National	
	XR2211C	Raytheon	
	XR2211M	† Raytheon	
	NE567	Signetics	
	SE567	† Signetics	
Tone Decoder, Dual (operates from 0.01 Hz to 500 kHz)	XR2567	Exar	
	XR2567M	† Exar	
Tone Decoder, Dual	MT8860	Mitel	
	MT8862	Mitel	
	MT8863	Mitel	
	MV8820	Plessey	
	MV8860	Plessey	
	MV8862	Plessey	
	MV8863	Plessey	
	CRC8030	Rockwell	
	7516-01	Telaris	
Tone Receiver Circuit, Dual (combine with filters for touch tone receiver)	G8860	GTE Micro	
	G8860X	GTE Micro	
	MK5102-5	Mostek	
	MK5103-5	Mostek	
	AF104	National	
	AF105	National	
	AF110	National	
	SM301A	Siemens	
	7640-01	Telaris	
	TT6174	Teltone	
Tone Receiver Circuit, Dual (with filters)	ITT3201	Aptek	
	ITT88205-5NC	Aptek	
	MH-88305	Mitel	
	MH88210	Mitel	
	MT8870	Mitel	
	SSI201	Silicon Sys	
	M927	Teltone	
	M937	Teltone	
	M947	Teltone	
	M967	Teltone	
Tone Ringer (operates from ring signal, drives speaker)	**S2561**	**AMI**	**(3139)**
	S2561A	**AMI**	**(3139)**
	S2561C	**AMI**	**(3139)**
Tone Ringer (operates from ring signal, drives speaker) (Cont'd)	CS8204	Cherry	
	CS8205	Cherry	
	ML8204	Mitel	
	ML8205	Mitel	
	MT8251	Mitel	
	M764	SGS	
	M764A	SGS	
	TCM1501	TI	
	TCM1504	TI	
	TCM1505	TI	
	TCM1506	TI	
	TCM1512	TI	
	TCM1512A	TI	
Transcoder, with Error Detection (10 kb/s to 2.048 Mb/s)	**CD22103**	**RCA**	**(749.756)**
Transmission Interface	TEA1042	Signetics	
	TEA1046	Signetics	
	TEA1055	Signetics	
Tri-Port Memory (T1 carrier)	R8040	Rockwell	
Videotex Decoder, Interactive	SAA5070	Signetics	
Dual Tone Generator (DTMF) or Dial Pulses	**HC5541**	**Harris**	**(2740)**
Dual Tone Generator (generates 12-16 tone pairs)	AY3-9400	GI	
	AY3-9410	GI	
Dual Tone Generator (touchtone frequencies)	S25089	AMI	
	S2559A	**AMI**	**(3138)**
	S2559B	**AMI**	**(3138)**
	S2559C	**AMI**	**(3138)**
	S2559D	**AMI**	**(3138)**
	S2559E	**AMI**	**(3138)**
	S2559F	**AMI**	**(3138)**
	S2559G	**AMI**	**(3138)**
	S2559H	**AMI**	**(3138)**
	S2859	AMI	
	S2860	AMI	
	ICM7206A	Intersil	
	ICM7206B	Intersil	
	ICM7206C	Intersil	
	ICM7206D	Intersil	
	SBA5089	ITT	
	SBA5091	ITT	
	MT5087	Mitel	
	MT5089	Mitel	
	MT5091	Mitel	
	MT5092	Mitel	
	MK5087	Mostek	
	MK5089	Mostek	
	MK5091	Mostek	
	MK5092	Mostek	
	MK5094	Mostek	
	MK5380	Mostek	
	MK5382	Mostek	
	MK5389	Mostek	
	MC14410	**Motorola**	**(3298)**
	MM53125	National	
	MM53130	National	
	MM5395	National	
	μPC767	NEC-Electron	
	NC2030	Nitron	
	CD22859	**RCA**	**(749.758)**
	PBD3534	RIFA	
	PBD3535	RIFA	
	M751	SGS	
	S359	Siemens	
	SCT5087	SSS	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Telecommunication Circuits (Cont'd)

Function	Device	Source	Line
Telecommunication Circuits (Cont'd)			
Dual Tone Generator (touchtone frequencies) (Cont'd)			
	SCT5089	SSS	
	7603-02	Telaris	
	TCM5087	TI	
	TCM5089	TI	
	TCM5092	TI	
Two-Wire-to-Four Wire Converter (replaces hybrid transformer)	LS285A	SGS	
	ST120	Signetics	

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Timers

Timers

Function	Device	Source	Line
Adjustable Threshold			
	MC1422	Motorola	
Delayed Switch ON/OFF (for driving relays, lamps, etc.)			
	PBA3008	RIFA	
	PBA3009	RIFA	
Internal Current Source			
	XR320	Exar	
Long Period (1 sec to 1 week)			
	AN6780	Panasonic	
Long Period (10 ms to 10,000 hours)			
	MW122	Analog Sys	
Low Power (supply 3 V)			
	SN76812	TI	
Micropower, Long Range (microseconds to days)			
	XR2243	**Exar (3201)**	
Microwave Oven Controller			
	TMS1117	TI	
	TMS1117NLP	**TI (1559)**	10
Precision	MW107	Analog Sys	
	MW197	Analog Sys	
	LM122	† National	
	LM2905	National	
	LM322	National	
	LM3905	National	
Precision Decade, Direct 7 Segment and Digit Drivers			
	ICM7045A	Intersil	
Programmable (includes a counter for long time delays) Binary Control			
	XR2240C	**Exar (3200)**	
	XR2240M	**† Exar (3200)**	
	μA2240C	Fairchild	20
	μA2240M	† Fairchild	
	ICM7240	Intersil	
	ICM7242	Intersil	
	ICM7250	Intersil	
	ICM7260	Intersil	
	LS7210	**LSI Comp (696)**	
	MC14541BA	† Motorola	
	MC14541BC	Motorola	
	μA2240C	TI	
	μA2240M	† TI	30
Timer	XR555C	Exar	
	XR555M	† Exar	
	XRL555	Exar	
	μA555C	Fairchild	
	NE555	Intersil	
	SE555	† Intersil	
	MC1455	Motorola	
	MC1555	† Motorola	
	LM555C	National	
	μPC1555	NEC-Electron	40
	RC555	Raytheon	
	RM555	† Raytheon	
	CA555	† RCA	
	CA555C	RCA	
	NE555	Signetics	
	SE555	† Signetics	
	SE555C	† Signetics	
	SG555	† Silicon G	
	SG555C	Silicon G	
	ULN-3304M	Sprague	50
	355A/C	Teledyne S	
	355B/M	† Teledyne S	
	NE555	TI	
	SE555	† TI	
	TA7326	Toshiba	
	TA7327	Toshiba	

Function	Device	Source	Line
Timer (CMOS 555), Low Power			
	ICM7555	Intersil	
	ICM7555M	† Intersil	
Timer with ÷ 12 Counter (time constant 7200 RC)			
	ZN1034E	Ferranti	
Timer with Counter, (time constant 128 RC)			
	XR2242C	**Exar (3201)**	60
	XR2242M	**† Exar (3201)**	
Universal (includes two 4-digit counters, comparator, clock oscillator and divider)			
	MM5865	National	
Dual (CMOS 556) Low Power			
	ICM7556	Intersil	
	ICM7556M	† Intersil	
Dual (dual 555), Pinout Variations			
	XR2556C	Exar	
	XR2556M	† Exar	
Dual (dual 555)			
	XR556C	Exar	
	XR556M	† Exar	
	XRL556C	Exar	
	XRL556M	† Exar	70
	μA556C	Fairchild	
	NE556	Intersil	
	SE556	† Intersil	
	MC3456	Motorola	
	MC3556	† Motorola	
	LM556	† National	
	LM556C	National	
	RC556	Raytheon	
	RM556	† Raytheon	
	NE556	Signetics	80
	NE556-1	Signetics	
	SE556	† Signetics	
	SE556-1	† Signetics	
	SE556-1C	† Signetics	
	SG556	† Silicon G	
	SG556C	Silicon G	
	NE556	TI	
	SE556	† TI	
Quad, Current Sink Output			
	XR558C	Exar	
	XR558M	† Exar	90
	NE558	Signetics	
	SE558	† Signetics	
Quad, Current Source Output			
	XR559C	Exar	
	XR559M	† Exar	
4 Digit Up/Down Presettable Counter/Timer, Settable Register with Comparison to Counter, Multiplexed 7-Segment and BCD Output (maximum count 5959)			
	ICM7217B	Intersil	
	ICM7217C	Intersil	
	ICM7227B	Intersil	
	ICM7227C	Intersil	

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Voltage Regulators

Fixed, Positive

For low amounts of current, voltage references can be used as voltage regulators. See Linear—Other Devices, Reference Diodes

Output Voltage, V	Output Current, mA	Device	Source		Line
2.6	100	MC78L02C	Motorola		
		μA78L02AC	TI		
		μA78L02C	TI		
		TA7316	Toshiba		
5	100	μA78L05C	Fairchild		
		MC78L05AC	Motorola		
		MC78L05C	Motorola		
		LM140LA-5	**National**	**(3299)**	
		LM78L05A	National		10
		LM78L05C	National		
		μPC78L05	NEC-Electron		
		μA78L05AC	TI		
		μA78L05C	TI		
		TA78L005	Toshiba		
		TA78L005A	Toshiba		
	150	LM2930-5	TI		
		LM330-5	TI		
	200	**LM109H**	**Motorola**	**(3294)**	
		LM209H	**Motorola**	**(3294)**	20
		LM309H	**Motorola**	**(3294)**	
		LM109H	**† National**	**(3299)**	
		LM209H	**National**	**(3299)**	
		LM2930-5	**National**	**(3299)**	
		LM309H	**National**	**(3299)**	
		LM330-5	**National**	**(3299)**	
		SG109T	† Silicon G		
		SG209T	Silicon G		
		SG309T	Silicon G		
		SFC2109	† Thomson-CSF		30
		SFC2209	Thomson-CSF		
		SFC2309	Thomson-CSF		
	250	**LM342-5**	**National**	**(3299)**	
	500	μA78M05C	Fairchild		
		μA78M05M	† Fairchild		
		TDD1605	ITT		
		MC7705C	Motorola		
		MC78M05C	Motorola		
		LM341-5	**National**	**(3300)**	
		LM78M05	National		40
		μPC78M05	NEC-Electron		
		L194-5	SGS		
		L2605	SGS		
		SG140-05T	† Silicon G		
		SG340-05T	Silicon G		
		SG7805ACT	Silicon G		
		SG7805AT	† Silicon G		
		μA78M05C	TI		
		μA78M05M	† TI		
	850	L129	SGS		50
	1000	μA109M	† Fairchild		
		μA209M	Fairchild		
		μA309C	Fairchild		
		LM109K	**† Motorola**	**(3294)**	
		LM209K	**Motorola**	**(3294)**	
		LM309K	**Motorola**	**(3294)**	
		LM109K	**† National**	**(3299)**	
		LM209K	**National**	**(3299)**	
		LM309K	**National**	**(3299)**	
		μPC7805	NEC-Electron		60
		L7805	† SGS		
		L7805C	SGS		
		SG109K	† Silicon G		
		SG209K	Silicon G		
		SG309K	Silicon G		
		SG7805ACP	Silicon G		
		SG7805AP	† Silicon G		

(Continued)

Output Voltage, V	Output Current, mA	Device	Source		Line
5	1000				(Cont'd)
		SG7805CP	† Silicon G		
		SG7805P	Silicon G		
		SFC2109M	Thomson-CSF		70
		TA78005	Toshiba		
	1200	SI3551M	Sanken		
	1500	μA7805C	Fairchild		
		μA7805M	† Fairchild		
		LAS1505	Lambda		
		LAS15A05	Lambda		
		LM140-5	**† Motorola**	**(3294)**	
		LM340-5	**Motorola**	**(3294)**	
		MC7805	† Motorola		
		MC7805A	† Motorola		80
		MC7805AC	Motorola		
		MC7805C	Motorola		
		LM140-5	**† National**	**(3299)**	
		LM140A-5	**† National**	**(3299)**	
		LM2931-5	**National**	**(3299)**	
		LM340-5	**National**	**(3299)**	
		LM340A-5	**National**	**(3299)**	
		LM7805	National		
		SG140-05K	Silicon G		
		SG140-05R	Silicon G		90
		SG340-05K	Silicon G		
		SG340-05R	Silicon G		
		SG7805ACK	Silicon G		
		SG7805ACR	Silicon G		
		SG7805AK	† Silicon G		
		SG7805CK	Silicon G		
		SG7805CR	Silicon G		
		SG7805K	† Silicon G		
		LM340-5	TI		
		TL780-05C	**TI**	**(3433)**	100
	2000	HA17805P	Hitachi		
		LAS1605	Lambda		
		Si3050G	Sanken		
		SI3552M	Sanken		
		L78S05	† SGS		
		L78S05C	SGS		
	3000	SH123	† Fairchild		
		SH223	Fairchild		
		SH323	Fairchild		
		LAS1405	Lambda		110
		LM123	**Motorola**	**(3294)**	
		LM223	**Motorola**	**(3294)**	
		LM323	**Motorola**	**(3294)**	
		MC78T05	† Motorola		
		MC78T05A	† Motorola		
		MC78T05AC	Motorola		
		MC78T05C	Motorola		
		LM123	**† National**	**(3299)**	
		LM223	**National**	**(3299)**	
		LM323	**National**	**(3299)**	120
		SI3554M	Sanken		
		SG123	† Silicon G		
		SG153-05	† Silicon G		
		SG223	Silicon G		
		SG253-05	Silicon G		
		SG323	Silicon G		
		SG353-05	Silicon G		
	5000	μA78H05	Fairchild		
		μA78H05A	Fairchild		
		LAS1905	Lambda		130
		42050-055	Micropac		
	8000	LAS3905	Lambda		
		LAS3905K	Lambda		
	10000	μA78P05	Fairchild		
		42050-510	Micropac		
	20000	52055-520	Micropac		

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Voltage Regulators (Cont'd)

Output Voltage, V	Output Current, mA	Device	Source	Line
Fixed, Positive			**(Cont'd)**	
6	100	TA78L006	Toshiba	
		TA78L006A	Toshiba	
	500	μA78M06C	Fairchild	
		μA78M06M	† Fairchild	
		TDD1606	ITT	
		MC78M06C	Motorola	
		SG140-06T	† Silicon G	
		SG340-06T	Silicon G	
		SG7806ACT	Silicon G	
		SG7806AT	† Silicon G	10
		SG7806CT	Silicon G	
		SG7806T	† Silicon G	
		μA78M06C	TI	
		μA78M06M	† TI	
	1000	SG7806ACP	Silicon G	
		SG7806AP	† Silicon G	
		SG7806CP	Silicon G	
		SG7806P	† Silicon G	
	1500	μA7806C	Fairchild	
		LAS1506	Lambda	20
		LM140-6	**† Motorola (3294)**	
		LM340-6	**Motorola (3294)**	
		MC7806	† Motorola	
		MC7806A	† Motorola	
		MC7806AC	Motorola	
		MC7806C	Motorola	
		SG140-06K	Silicon G	
		SG140-06R	Silicon G	
		SG340-06K	Silicon G	
		SG340-06R	Silicon G	30
		SG7806ACK	Silicon G	
		SG7806ACR	Silicon G	
		SG7806AK	† Silicon G	
		SG7806CK	Silicon G	
		SG7806CR	Silicon G	
		SG7806K	† Silicon G	
		LM340-6	TI	
		μA7806C	TI	
	2000	HA17806P	Hitachi	
		CJSE017	Solitron	40
		CJSE019	Solitron	
		CJSE021	Solitron	
	3000	LAS1406	Lambda	
		MC78T06	† Motorola	
		MC78T06C	Motorola	
	10000	42050-610	Micropac	
	20000	52055-620	Micropac	
6.2	100	μA78L62C	Fairchild	
		μA78L06AC	TI	
		μA78L06C	TI	50
7	100	TA78L007	Toshiba	
		TA78L007A	Toshiba	
	10000	42050-710	Micropac	
	20000	42055-720	Micropac	
7.5	100	TA78L075	Toshiba	
		TA78L075A	Toshiba	
	1000	L7875	† SGS	
		L7875C	SGS	
		L78C75C	SGS	
		L78S75	† SGS	60
8	100	MC78L08AC	Motorola	
		MC78L08C	Motorola	
		μPC78L08	NEC-Electron	
		μA78L08AC	TI	
		μA78L08C	TI	
		TA78L008	Toshiba	
		TA78L008A	Toshiba	

(Continued)

Output Voltage, V	Output Current, mA	Device	Source	Line
8			(Cont'd)	
	150	LM2930-8	TI	
	200	**LM2930-8**	**National (3299)**	
	500	μA78M08C	Fairchild	70
		μA78M08M	† Fairchild	
		TDD1608	ITT	
		MC78M08C	Motorola	
		μPC78M08	NEC-Electron	
		SG140-08T	† Silicon G	
		SG340-08T	Silicon G	
		SG7808ACT	Silicon G	
		SG7808AT	† Silicon G	
		SG7808CT	Silicon G	
		SG7808T	† Silicon G	80
		μA78M08C	TI	
		μA78M08M	† TI	
	1500	μA7808C	Fairchild	
		μA7808M	† Fairchild	
		HA17808	Hitachi	
		LAS1508	Lambda	
		LM140-8	**† Motorola (3294)**	
		LM340-8	**Motorola (3294)**	
		MC7808	**† Motorola (3294)**	
		MC7808A	**† Motorola (3294)**	90
		MC7808AC	**Motorola (3294)**	
		MC7808C	**Motorola (3294)**	
		SG140-08K	Silicon G	
		SG140-08R	Silicon G	
		SG340-08K	Silicon G	
		SG340-08R	Silicon G	
		SG7808ACK	Silicon G	
		SG7808ACR	Silicon G	
		SG7808AK	† Silicon G	
		SG7808CK	Silicon G	100
		SG7808CR	Silicon G	
		SG7808K	† Silicon G	
		LM340-8	TI	
		μA7808C	TI	
	2000	LAS1608	Lambda	
	3000	MC78T08	Motorola	
		MC78T08C	Motorola	
		SG153-08	† Silicon G	
		SG253-08	Silicon G	
		SG353-08	Silicon G	110
	5000	μA78H08C	Fairchild	
	10000	μPC7808	NEC-Electron	
		SG7808ACP	Silicon G	
		SG7808AP	† Silicon G	
		SG7808CP	Silicon G	
		SG7808P	† Silicon G	
	20000	42055-820	Micropac	
8.2	100	μA78L82C	Fairchild	
8.5	500	L2685	SGS	
	1000	μA7885	Fairchild	120
		μA7885C	TI	
9	100	μA78L09C	Fairchild	
		μA78L09AC	TI	
		μA78L09C	TI	
		TA78L009	Toshiba	
		TA78L009A	Toshiba	
	1500	L7809	SGS	
		L78S09	† SGS	
		SL78S09C	SGS	
	20000	42055-920	Micropac	130
10	100	μA78L10AC	TI	
		μA78L10C	TI	
		TA78L010	Toshiba	
		TA78L010A	Toshiba	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Voltage Regulators (Cont'd)

Output Voltage, V	Output Current, mA	Device	Source	Line
Fixed, Positive			**(Cont'd)**	
10			(Cont'd)	
	200	**LH0075**	**† National (3303,3343)**	
	500	TDD1610	ITT	
		L2610	SGS	
		μA78M10C	TI	
	1500	LAS1510	Lambda	
		LM340-10	TI	
		μA7810C	TI	
	2000	L78S10	† SGS	
		L78S10C	SGS	
	9000	42050-109	Micropac	10
	20000	42055-1020	Micropac	
12	100	μA78L12C	Fairchild	
		MC78L12AC	† Motorola	
		MC78L12C	Motorola	
		LM140LA-12	**† National (3299)**	
		LM340LA-12	**National (3299)**	
		LM78L12A	National	
		LM78L12C	National	
		μPC78L12	NEC-Electron	
		μA78L12AC	TI	20
		μA78L12C	TI	
		TA78L012	Toshiba	
		TA78L012A	Toshiba	
	250	**LM342-12**	**National (3299)**	
	500	μA78M12C	Fairchild	
		μA78M12M	† Fairchild	
		TDD1612	ITT	
		MC78M12C	Motorola	
		LM341-12	**National (3300)**	
		LM78M12	National	30
		μPC78M12	NEC-Electron	
		L194-12	SGS	
		SG140-12T	† Silicon G	
		SG340-12T	Silicon G	
		SG7812ACT	Silicon G	
		SG7812AT	† Silicon G	
		SG7812CT	Silicon G	
		SG7812T	† Silicon G	
		μA78M12C	TI	
		μA78M12M	† TI	40
	720	L130	SGS	
	1000	μPC7812	NEC-Electron	
		SI3120E	Sanken	
		SI3120T	Sanken	
		STK521	Sanyo	
		STK541	Sanyo	
		SG7812ACR	Silicon G	
		SG7812AR	† Silicon G	
		SG7812CR	Silicon G	
		SG7812R	† Silicon G	50
		TA78012	Toshiba	
	1500	μA7812C	Fairchild	
		μA7812M	† Fairchild	
		LAS1512	Lambda	
		LAS15A12	Lambda	
		LM140-12	**† Motorola (3294)**	
		LM340-12	**Motorola (3294)**	
		MC7812	**† Motorola (3294)**	
		MC7812A	**† Motorola (3294)**	
		MC7812AC	**Motorola (3294)**	60
		MC7812C	**Motorola (3294)**	
		LM140-12	**† National (3299)**	
		LM140A-12	**† National (3299)**	
		LM340-12	**National (3299)**	
		LM340A-12	**National (3299)**	
		LM7812	National	
			(Continued)	

Output Voltage, V	Output Current, mA	Device	Source	Line
12	1500		(Cont'd)	
		SI3120G	Sanken	
		SI3120M	Sanken	
		L7812	† SGS	
		L7812C	SGS	70
		SG140-12K	† Silicon G	
		SG140-12R	† Silicon G	
		SG340-12K	Silicon G	
		SG340-12P	Silicon G	
		SG340-12R	Silicon G	
		SG7812ACK	Silicon G	
		SG7812ACP	Silicon G	
		SG7812AK	† Silicon G	
		SG7812CK	Silicon G	
		SG7812CP	Silicon G	80
		SG7812K	† Silicon G	
		LM340-12	TI	
		TL780-12C	**TI (3433)**	
		μA7812C	TI	
	2000	HA17812P	Hitachi	
		LAS1612	Lambda	
		STK531	Sanyo	
		L7812	† SGS	
		L7812C	SGS	
		L78S12C	SGS	90
	3000	LAS1412	Lambda	
		MC78T12	† Motorola	
		MC78T12A	† Motorola	
		MC78T12AC	Motorola	
		MC78T12C	Motorola	
		SG153-12	† Silicon G	
		SG253-12	Silicon G	
		SG353-12	Silicon G	
	5000	μA78H12	Fairchild	
		LAS1912	Lambda	100
	8000	42050-128	Micropac	
	16000	42055-1216	Micropac	
13.2	100	TA78L132	Toshiba	
		TA78L132A	Toshiba	
	1500	LAS15CB	Lambda	
13.8	2000	LAS16CB	Lambda	
14	2000	LAS16CB	Lambda	
	8000	42050-148	Micropac	
	16000	42055-1416	Micropac	
15	100	μA78L15C	Fairchild	110
		MC78L15AC	Motorola	
		MC78L15C	Motorola	
		LM140LA-15	**† National (3299)**	
		LM340LA-15	**National (3299)**	
		LM78L15A	National	
		LM78L15C	National	
		μPC78L15	NEC-Electron	
		μA78L15AC	TI	
		μA78L15C	TI	
		TA78L015	Toshiba	120
		TA78L015A	Toshiba	
	250	**LM342-15**	**National (3299)**	
	500	μA78M15C	Fairchild	
		μA78M15M	† Fairchild	
		TDD1615	ITT	
		MC78M15C	Motorola	
		LM341-15	**National (3300)**	
		LM78M15	National	
		μPC78M15	NEC-Electron	
		L194-15	SGS	130
		SG140-15T	† Silicon G	
		SG7815ACT	Silicon G	
		SG7815AT	† Silicon G	
		SG7815CT	Silicon G	
			(Continued)	

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Voltage Regulators (Cont'd)

Output Voltage, V	Output Current, mA	Device	Source		Line
Fixed, Positive				**(Cont'd)**	
15	500			(Cont'd)	
		SG7815T	† Silicon G		
		μA78M15C	TI		
		μA78M15M	† TI		
	600	L131	SGS		
	1000	SI3150E	Sanken		
		SI3150T	Sanken		
		L7815	† SGS		
		L7815C	SGS		
		SG7815ACR	Silicon G		
		SG7815AR	† Silicon G		10
		SG7815CR	Silicon G		
		SG7815R	† Silicon G		
		TA78015	Toshiba		
	1500	μA7815C	Fairchild		
		μA7815M	† Fairchild		
		LAS1515	Lambda		
		LAS15A15	Lambda		
		LM140-15	**† Motorola**	**(3294)**	
		LM340-15	**Motorola**	**(3294)**	
		MC7815	**† Motorola**	**(3294)**	20
		MC7815A	**† Motorola**	**(3294)**	
		MC7815AC	**Motorola**	**(3294)**	
		MC7815C	**Motorola**	**(3294)**	
		LM140-15	**† National**	**(3299)**	
		LM140A-15	**† National**	**(3299)**	
		LM340-15	**National**	**(3299)**	
		LM340A-15	**National**	**(3299)**	
		LM7815	National		
		SI3150G	Sanken		
		SI3150M	Sanken		30
		SG140-15K	† Silicon G		
		SG140-15R	† Silicon G		
		SG7815ACK	Silicon G		
		SG7815ACP	Silicon G		
		SG7815AK	† Silicon G		
		SG7815CK	Silicon G		
		SG7815CP	Silicon G		
		SG7815K	† Silicon G		
		LM340-15	TI		
		TL780-15C	**TI**	**(3433)**	40
		μA7815C	TI		
	2000	HA17815P	Hitachi		
		LAS1615	Lambda		
		L78S15	† SGS		
		L78S15C	SGS		
		CJSE001	Solitron		
		CJSE003	Solitron		
		CJSE005	Solitron		
	3000	LAS1415	Lambda		
		MC78T15	† Motorola		50
		MC78T15A	† Motorola		
		MC78T15AC	Motorola		
		MC78T15C	Motorola		
		SG153-15	† Silicon G		
		SG253-15	Silicon G		
		SG353-15	Silicon G		
	5000	LAS1915	Lambda		
	8000	42050-158	Micropac		
	16000	42055-1516	Micropac		
16	8000	42050-168	Micropac		60
	12000	42055-1612	Micropac		
18	100	MC78L18AC	Motorola		
		MC78L18C	Motorola		
		TA78L018	Toshiba		
		TA78L018A	Toshiba		
	500	TDD1618	ITT		
				(Continued)	

Output Voltage, V	Output Current, mA	Device	Source		Line
18	500			(Cont'd)	
		MC78M18C	Motorola		
		μPC78M18	NEC-Electron		
		SG140-18T	† Silicon G		
		SG340-18T	Silicon G		70
		SG7818ACT	Silicon G		
		SG7818AT	† Silicon G		
		SG7818CT	Silicon G		
		SG7818T	† Silicon G		
	1000	μPC7818	NEC-Electron		
		STK522	Sanyo		
		STK542	Sanyo		
		L7818	† SGS		
		L7818C	SGS		
		SG7817AP	† Silicon G		80
		SG7818ACP	† Silicon G		
		SG7818AP	Silicon G		
		SG7818P	Silicon G		
	1500	μA7818C	Fairchild		
		μA7818M	† Fairchild		
		HA17818P	Hitachi		
		LAS1518	Lambda		
		LM140-18	**† Motorola**	**(3294)**	
		LM340-18	**Motorola**	**(3294)**	
		MC7818	**† Motorola**	**(3294)**	90
		MC7818A	**† Motorola**	**(3294)**	
		MC7818AC	**Motorola**	**(3294)**	
		MC7818C	**Motorola**	**(3294)**	
		SG140-18K	Silicon G		
		SG140-18R	Silicon G		
		SG340-18K	Silicon G		
		SG340-18R	Silicon G		
		SG7818ACK	Silicon G		
		SG7818ACP	Silicon G		
		SG7818AK	† Silicon G		100
		SG7818CK	Silicon G		
		SG7818CP	Silicon G		
		SG7818K	† Silicon G		
		LM340-18	TI		
		μA7818C	TI		
	2000	MC78T18	† Motorola		
		MC78T18C	Motorola		
		STK532	Sanyo		
		L78S18	† SGS		
		L78S18C	SGS		110
	3000	SG153-18	† Silicon G		
		SG253-18	Silicon G		
		SG353-18	Silicon G		
	8000	42050-188	Micropac		
	12000	42055-1812	Micropac		
		42055-1812	Toshiba		
20	100	TA78L020	Toshiba		
		TA78L020A	Toshiba		
	500	MC78M20C	Motorola		
		SG140-20T	† Silicon G		120
		SG340-20T	Silicon G		
		SG7820ACT	Silicon G		
		SG7820AT	† Silicon G		
		SG7820CT	Silicon G		
		SG7820T	† Silicon G		
		μA78M20C	TI		
		μA78M20M	† TI		
	1000	LAS1520	Lambda		
		SG140-20K	† Silicon G		
		SG140-20R	† Silicon G		130
		SG240-20K	Silicon G		
		SG340-20P	Silicon G		
		SG340-20R	Silicon G		
		SG7820K	† Silicon G		
		SG7820R	† Silicon G		
				(Continued)	

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Voltage Regulators (Cont'd)

Output Voltage, V	Output Current, mA	Device	Source	Line
Fixed, Positive			**(Cont'd)**	
20			(Cont'd)	
	2000	CJSE009	Solitron	
		CJSE011	Solitron	
		CJSE013	Solitron	
	8000	42050-208	Micropac	
		42055-2010	Micropac	
22	500	μA78M22C	TI	
	1500	μA7822C	TI	
	4000	42050-224	Micropac	
	10000	42055-2210	Micropac	
24	100	MC78L24AC	Motorola	10
		MC78L24C	Motorola	
		TA78L024	Toshiba	
		TA78L024A	Toshiba	
	300	STK507	Sanyo	
	500	μA78M24C	Fairchild	
		μA78M24M	† Fairchild	
		TDD1624	ITT	
		MC78M24C	Motorola	
		μPC78M24	NEC-Electron	
		SG140-24T	† Silicon G	20
		SG340-24T	Silicon G	
		SG7824ACT	Silicon G	
		SG7824AT	† Silicon G	
		SG7824CT	Silicon G	
		SG7824T	† Silicon G	
		μA78M24C	TI	
		μA78M24M	† TI	
	1000	μPC7824	NEC-Electron	
		SI3240E	Sanken	
		SI3240T	Sanken	30
		STK523	Sanyo	
		L7824	† SGS	
		L7824C	SGS	
		SG7824ACP	Silicon G	
		SG7824AP	† Silicon G	
		SG7824CP	Silicon G	
		SG7824P	† Silicon G	
	1500	μA7824C	Fairchild	
		μA7824M	† Fairchild	
		LAS1524	Lambda	40
		LM140-24	**† Motorola** **(3294)**	
		LM340-24	**Motorola** **(3294)**	
		MC7824	† Motorola	
		MC7824A	† Motorola	
		MC7824AC	Motorola	
		MC7824C	Motorola	
		SI3240G	Sanken	
		SI3240T	Sanken	
		SG140-24K	Silicon G	
		SG140-24R	Silicon G	50
		SG340-24K	Silicon G	
		SG340-24P	Silicon G	
		SG340-24R	Silicon G	
		SG7824ACK	Silicon G	
		SG7824ACR	Silicon G	
		SG7824AK	† Silicon G	
		SG7824CK	Silicon G	
		SG7824CR	Silicon G	
		SG7824K	† Silicon G	
		LM340-24	TI	60
		μA7824C	TI	
	2000	HA17824P	Hitachi	
		MC78T24	† Motorola	
		MC78T24C	Motorola	
		STK533	Sanyo	
		L78S24	† SGS	
		L78S24C	SGS	
			(Continued)	

Output Voltage, V	Output Current, mA	Device	Source	Line
24			(Cont'd)	
	4000	42050-244	Micropac	
	10000	42055-2410	Micropac	
26	4000	42050-264	Micropac	70
	8000	42055-2608	Micropac	
28	1500	LAS1528	Lambda	
	4000	42050-284	Micropac	
	8000	42055-2808	Micropac	
30	4000	42050-304	Micropac	
31	Shunt	TAA550	National	
32	4000	42050-324	Micropac	
33	Shunt	TAA550	National	
34	4000	42050-344	Micropac	
35	Shunt	TAA550	National	80
190	20	DI900	Dionics	
	50	DI905	Dionics	
Fixed, Negative				
2	1000	MC7902C	Motorola	
	1500	LAS1802	Lambda	
	2000	μA79E02	† Fairchild	
		μA79E02C	Fairchild	
3	100	MC79L03AC	Motorola	
		MC79L03C	Motorola	
5	100	MC79L05AC	Motorola	
		MC79L05C	Motorola	90
		LM320L05	National	
		LM79L05	National	
		LM79L05A	National	
		MC79L05AC	TI	
	250	LM320ML05	National	
	500	μA79M05C	Fairchild	
		μA79M05M	† Fairchild	
		LM120H5	† National	
		LM320H5	National	
		LM320MP5	National	100
		LM79M05	National	
		SG120-05T	† Silicon G	
		SG220-05T	Silicon G	
		SG320-05T	Silicon G	
		μA79M05C	TI	
		μA79M05M	† TI	
	1000	μPC7905	NEC-Electron	
		SG120-05P	† Silicon G	
		SG220-05P	Silicon G	
		SG320-05P	Silicon G	110
	1500	μA7905C	Fairchild	
		μA7905M	† Fairchild	
		LAS1805	Lambda	
		LAS18A05	Lambda	
		MC7905C	**Motorola** **(3294)**	
		LM120K5	† National	
		LM320K5	National	
		LM320T5	National	
		LM7905	National	
		SG120-05K	† Silicon G	120
		SG220-05K	Silicon G	
		SG220-05R	Silicon G	
		SG320-05K	Silicon G	
		SG320-05R	Silicon G	
		SG7905	† Silicon G	
		SG7905A	† Silicon G	
		SG7905C	Silicon G	
		μA7905C	TI	
	3000	MC79052C	Motorola	
		LM145K5	† National	130
		LM345K5	National	
			(Continued)	

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Voltage Regulators (Cont'd)

Output Voltage, V	Output Current, mA	Device	Source	Line
Fixed, Negative			**(Cont'd)**	
5			(Cont'd)	
	5000	42051-055	Micropac	
5.2	500	SG120-5	† Silicon G	
		SG220-5	Silicon G	
		SG320-5	Silicon G	
	1000	SG120-5	† Silicon G	
		SG220-5	Silicon G	
		SG320-5	Silicon G	
	1500	LAS18052	Lambda	
		MC7905	Motorola	
		SG120-5	Silicon G	10
		SG220-5	Silicon G	
		SG220-5	Silicon G	
		SG320-5	Silicon G	
		SG320-5	Silicon G	
		SG7905	† Silicon G	
		SG7905	† Silicon G	
		SG7905	Silicon G	
		SG7905	Silicon G	
		μA7952C	TI	
	3000	LM145K5	† National	20
		LM345K5	National	
6	500	μA79M06C	TI	
		μA79M06M	† TI	
	1500	LAS1806	Lambda	
		MC7906C	**Motorola (3294)**	
		μA7906C	TI	
	2000	CJSE018	Solitron	
		CJSE020	Solitron	
	5000	42051-065	Micropac	
7	5000	42051-075	Micropac	30
8	500	μ79M08C	Fairchild	
		μA7908M	† Fairchild	
		SG120-08T	† Silicon G	
		SG320-08T	Silicon G	
		μA79M08C	TI	
		μA79M08M	† TI	
	1000	μA7908C	Fairchild	
		LAS1808	Lambda	
		MC7908C	**Motorola (3294)**	
		μPC7908	NEC-Electron	40
		SG120-08K	† Silicon G	
		SG120-08R	† Silicon G	
		SG320-08K	Silicon G	
		SG320-08P	Silicon G	
		SG320-08R	Silicon G	
		SG7908	† Silicon G	
		SG7908A	† Silicon G	
		SG7908AC	Silicon G	
		SG7908C	Silicon G	
		μA7908C	TI	50
	5000	42051-085	Micropac	
9	1500	42051-095	Micropac	
10	500	μA79M10C	TI	
		μA79M10M	† TI	
	1500	LAS1810	Lambda	
	5000	42051-105	Micropac	
12	100	MC79L12AC	Motorola	
		MC79L12C	Motorola	
		LM320L12	National	
		LM79L12	National	
		LM79L12A	National	60
		MC79L12AC	TI	
	200	LM120H12	† National	
		LM320H12	National	
		SG120-12T	† Silicon G	
			(Continued)	

Output Voltage, V	Output Current, mA	Device	Source	Line
12	200		(Cont'd)	
		SG220-12T	Silicon G	
		SG320-12T	Silicon G	
	500	μA79M12C	Fairchild	
		μA79M12M	† Fairchild	
		LM320MP12	National	70
		LM79M12	National	
		μA79M12C	TI	
		μA79M12M	† TI	
	1000	LM120K12	† National	
		LM320K12	National	
		LM320T12	National	
		μPC7912	NEC-Electron	
		SG120-12P	† Silicon G	
		SG220-12P	Silicon G	
		SG320-12P	Silicon G	80
	1500	μA7912C	Fairchild	
		μA7912M	† Fairchild	
		LAS1812	Lambda	
		LAS18A12	Lambda	
		MC7912AC	**Motorola (3294)**	
		MC7912C	**Motorola (3294)**	
		LM7912	National	
		SG120-12K	† Silicon G	
		SG220-12K	Silicon G	
		SG220-12R	Silicon G	90
		SG320-12K	Silicon G	
		SG320-12R	Silicon G	
		SG7912	† Silicon G	
		SG7912A	† Silicon G	
		SG7912AC	Silicon G	
		SG7912C	Silicon G	
		μA7912C	TI	
	4000	42051-124	Micropac	
14	4000	42051-144	Micropac	
15	100	MC79L15AC	Motorola	100
		MC79L15C	Motorola	
		LM320L15	National	
		LM79L15	National	
		LM79L15A	National	
		MC79L15AC	TI	
	200	LM120H15	† National	
		LM320H15	National	
		SG120-15T	† Silicon G	
		SG220-15T	Silicon G	
		SG320-15T	Silicon G	110
	250	LM320ML15	National	
	500	μA79M15C	Fairchild	
		μA79M15M	† Fairchild	
		LM320MP15	National	
		LM79M15	National	
		μA79M15C	TI	
		μA79M15M	† TI	
	1000	MC79L15A	Motorola	
		LM120K15	† National	
		LM320K15	National	120
		LM320T15	National	
		μPC7915	NEC-Electron	
		SG120-15R	† Silicon G	
		SG220-15R	Silicon G	
		SG320-15R	Silicon G	
	1500	μA7915C	Fairchild	
		μA7915M	† Fairchild	
		LAS1815	Lambda	
		LAS18A15	Lambda	
		MC7915AC	**Motorola (3294)**	130
		MC7915C	**Motorola (3294)**	
		LM7915	National	
		SG120-15K	† Silicon G	
		SG220-15K	Silicon G	
			(Continued)	

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Voltage Regulators (Cont'd)

Fixed, Negative (Cont'd)

Output Voltage, V	Output Current	Device	Source	Line
15	1500			(Cont'd)
		SG220-15P	Silicon G	
		SG320-15K	Silicon G	
		SG320-15P	Silicon G	
		SG7915	† Silicon G	
		SG7915A	† Silicon G	
		SG7915AC	Silicon G	
		SG7915C	Silicon G	
		μA7915	† TI	
		μA7915C	TI	
	2000	42051-154	Micropac	10
		CJSE002	Solitron	
		CJSE004	Solitron	
		CJSE006	Solitron	
16	4000	42051-164	Micropac	
18	100	MC79L18C	Motorola	
	500	SG120-18T	† Silicon G	
		SG320-18T	Silicon G	
	1000	μPC7918	NEC-Electron	
	1500	LAS1818	Lambda	
		MC7918C	**Motorola (3294)**	20
		MC79L18AC	Motorola	
		SG120-18K	† Silicon G	
		SG120-18R	† Silicon G	
		SG320-18K	Silicon G	
		SG320-18P	Silicon G	
		SG320-18R	Silicon G	
		SG7918	† Silicon G	
		SG7918A	† Silicon G	
		SG7918AC	Silicon G	
		SG7918C	Silicon G	30
		μA7918C	TI	
	4000	42051-184	Micropac	
20	500	SG120-20T	† Silicon G	
		μA79M20C	TI	
		μA79M20M	† TI	
	1500	LAS1820	Lambda	
		SG120-20K	† Silicon G	
		SG120-20R	† Silicon G	
		SG7920	† Silicon G	
		SG7920A	† Silicon G	40
		SG7920AC	Silicon G	
		SG7920C	Silicon G	
	2000	CJSE010	Solitron	
		CJSE012	Solitron	
		CJSE014	Solitron	
	3000	42051-204	Micropac	
22	3000	42051-223	Micropac	
24	100	MC79L24AC	Motorola	
		MC79L24C	Motorola	
	500	μA79M24C	TI	50
		μA79M24M	† TI	
	1000	μPC7924	NEC-Electron	
	1500	LAS1824	Lambda	
		MC7924C	**Motorola (3294)**	
		μA7924C	TI	
	3000	42051-243	Micropac	
26	3000	42051-263	Micropac	
28	1500	LAS1828	Lambda	
	3000	42051-283	Micropac	
30	3000	42051-303	Micropac	60
31	Shunt	TAA550	National	
32	3000	42051-323	Micropac	
33	Shunt	TAA550	National	
35	Shunt	TAA550	National	
36	3000	42051-363	Micropac	

Fixed, Dual

Output Voltage, V	Output Current	Device	Source	Line
±6	5000	42051	Micropac	
±12	100	LM126	† National	
		LM326	National	
±15	100	**MC1468**	**Motorola (3296)**	
		MC1568	**† Motorola (3296)**	70
		SG1468	Silicon G	
		SG1568	† Silicon G	
		SG4501	Silicon G	
		XR1468	Exar	
		XR1568	† Exar	
		XR4195	Exar	
		LM125	† National	
		LM325	National	
		RC4195	Raytheon	
		RM4195	† Raytheon	80
		TA7179	Toshiba	
	200	SG1501A	† Silicon G	
		SG2501A	Silicon G	
		SG3501A	Silicon G	

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Voltage Regulators

Adjustable, Positive

Arranged in sequence by Output Voltage-High, Output Current, and then Output Voltage-Low.

Suffixes designating package style differences are basically dropped in the Adjustable Voltage Regulator Section. Thus identical part numbers may be referenced more than once under different parameters. Consult manufacturers on availability of different grades.

Output Voltage Hi	Low	Output Current, mA	Device	Source	Line
15	5	1500	SI3580M	Sanken	
16	1.3	40	ICL7663	Intersil	
	4	6000	LAS39U	Lambda	
20	1.2	10000	**LM196**	**National (3299)**	
			LM396	**National (3299)**	
	2	20	LM300	Intersil	
			SG300	Silicon G	
			SFC2300	Thomson-CSF	10
	5	5000	μA78H	Fairchild	
24	3	150	**LM2931**	**National (3299)**	
	5	50000	μA78HG	Fairchild	
26	1.8	12	CA3085	† RCA	
27	0	200	LH0075	† National	
			LH0075C	**National (3303,3343)**	
30	2	20	LM100	† Intersil	
			SG100	† Silicon G	
			SG200	Silicon G	
			SFC2100	† Thomson-CSF	20
			SFC2200	Thomson-CSF	
	2.6	3000	LAS14AU	Lambda	
	3	Shunt	TL430C	TI	
		1800	L200	SGS	
	4	1500	LAS15U	Lambda	
		2000	LAS16U	Lambda	
		5000	LAS19U	Lambda	
	4.5	12	μA305C	Fairchild	
			LM305	Intersil	
			LM305	Motorola	30
			LM305	National	
			μPC141	NEC-Electron	
			μPC325	NEC-Electron	
			otPC305	NEC-Micro	
			SG305	Silicon G	
	5	500	μA78MG	Fairchild	
		1000	μA78G	Fairchild	
		5000	μ78HG	Fairchild	
32	1.2	100	TL317	TI	
		3000	**LM150**	**† Motorola (3295)**	40
			LM250	**Motorola (3295)**	
			LM350	**Motorola (3295)**	
			LM150	**† National (3299)**	
			LM250	**National (3299)**	
			LM350	**National (3299)**	
			SG150	† Silicon G	
			SG150A	Silicon G	
			SG250	Silicon G	
			SG250A	Silicon G	
			SG350	Silicon G	50
			SG350A	Silicon G	
		5000	**LM138**	**† National (3299)**	
			LM238	**National (3299)**	
			LM338	**National (3299)**	
	2.5	200	**MC1469**	**Motorola (3295)**	
		500	MC1469	Motorola	
	3.3	200	TA7089	Toshiba	
33	1.2	3000	LLM350	Lambda	
		5000	LLM338	Lambda	
36	1.7	100	CA3085A	† RCA	60
	2.5	100	μA431	Fairchild	
			TL431C	TI	
			TL431M	† TI	
37	1.2	100	**LM117L**	**† Motorola (3295)**	
			LM217L	**Motorola (3295)**	
			LM317L	**Motorola (3295)**	
			LM317L	**National (3299)**	
		500	SG117	† Silicon G	
			SG217	Silicon G	
			SG317	Silicon G	70
			TL117L	† TI	
		1500	μA117	† Fairchild	
			μA217	Fairchild	
			μA317	Fairchild	
			LLM317	Lambda	
			MCELM117	Micro Eng	
			MCELM217	Micro Eng	
			MCELM317	Micro Eng	
			LM117	**† Motorola (3295)**	
			LM217	**Motorola (3295)**	80
			LM317	**Motorola (3295)**	
			LM117	**† National (3299)**	
			LM217	**National (3299)**	
			LM317	**National (3299)**	
			SG117	† Silicon G	
			SG217	Silicon G	
			SG317	Silicon G	
			LM217	TI	
			LM317	TI	
	2	150	μA723C	Fairchild	90
			μA723M	† Fairchild	
			μA723	Intersil	
			MC1723	**† Motorola (3295)**	
			MC1723C	**Motorola (3295)**	
			LM723	† National	
			LM723C	National	
			RC723	Raytheon	
			RM723	† Raytheon	
			CA723	† RCA	
			CA723C	RCA	100
			μA723	† Signetics	
			μA723C	Signetics	
			SG723	† Silicon G	
			SG723C	Silicon G	
			μA723C	TI	
			μA723M	† TI	
			SFC2723C	† Thomson-CSF	
			SFC2723EC	Thomson-CSF	
	2.5	250	**LM117M**	**† Motorola (3295)**	
			LM217M	**Motorola (3295)**	110
			LM317M	**Motorola (3295)**	
			MC1569	**† Motorola (3295)**	
		600	MC1569	† Motorola	
	5	25	μA376C	Fairchild	
			LM376	National	
		50	SE550	† Signetics	
38	2	100	SG3532	Silicon G	
		150	LAS1000	Lambda	
			LAS723	Lambda	
	3	150	L123CB	SGS	120
			L123CT	SGS	
40	0	150	LAS3700	Lambda	
	2	50	NE550	Signetics	
	4.5	12	μA105M	† Fairchild	
			LM205	Motorola	
			LM105	† National	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Voltage Regulators (Cont'd)

Output Voltage Hi	Low	Output Current, mA	Device	Source	Line
Adjustable, Positive				**(Cont'd)**	
40	4.5	12		(Cont'd)	
			LM205	National	
			SG105	† Silicon G	
			SG205	Silicon G	
			SFC2105	† Thomson-CSF	
			SFC2205	Thomson-CSF	
		45	μA305AC	Fairchild	
			LM305A	National	
			SG305A	Silicon G	
			SFC2305	Thomson-CSF	
46	1.7	100	CA3085B	† RCA	10
48	2	100	SG1532	† Silicon G	
			SG2532	Silicon G	
		150	LAS1100	Lambda	
			LAS723B	Lambda	
56	8	1000	CJCA001	Solitron	
			CJCA007	Solitron	
77	2	150	L146	SGS	
125	1.25	700	**TL783C**	**TI (3431)**	
1000	0	100	**MC1466**	**Motorola (3296)**	
			MC15666	† Motorola	20
Adjustable, Negative					
16	1.3	40	ICL7664	Intersil	
24	2.2	5000	μ79HGA	Fairchild	
27	0	200	**LH0076**	**† National (3303,3343)**	
			LH0076C	**National (3303,3343)**	
30	0.035	20	LM304	Motorola	
			LM304	National	
			μPC142	NEC-Electron	
			SG304	Silicon G	
	2.2	500	μA79MG	Fairchild	
		1000	μA79G	Fairchild	30
	2.6	1500	LAS18U	Lambda	
32	3.8	250	**MC1463G**	**Motorola (3295)**	
		500	TA7085A	Toshiba	
33	3.6	250	**MC1563G**	**Motorola (3295)**	
34	3.8	600	**MC1463R**	**Motorola (3295)**	
37	1.2	500	**LM137**	**† Motorola (3295)**	
			LM237	**Motorola (3295)**	
			LM337	**Motorola (3295)**	
		1500	MCELM137	Micro Eng	
			MCELM237	Micro Eng	40
			MCELM337	Micro Eng	
			LM137	**† National (3301)**	
			LM237	**National (3301)**	
			LM337	**National (3301)**	
			SG137	† Silicon G	
			SG237	Silicon G	
			SG337	Silicon G	
			LM137	† TI	
			LM237	TI	
			LM337	TI	50
	3.6	600	MC1536R	† Motorola	
40	0.015	20	LM104	† Motorola	
			LM204	Motorola	
			LM104	† National	
			LM204	National	
			SG204	Silicon G	
			SG304	Silicon G	
			SFC2204	Thomson-CSF	
			SGC2104	† Thomson-CSF	

Output Voltage Hi	Low	Output Current, mA	Device	Source	Line
56	8	1000	CJCA002	Solitron	60
			CJCA008	Solitron	
57	1.2	100	**LM337L**	**National (3301)**	
		1500	LM137	† National	
			LM237	National	
			LM337	National	
Adjustable, Dual					
±15.5	±14.5	100	MC1468	Motorola	
			MC1568	† Motorola	
±20	±8	100	MC1468	Motorola	
			MC1568	† Motorola	
			SG1468	Silicon G	70
			SG1568	† Silicon G	
	±14.5	100	SG1468T	Silicon G	
			SG1568T	† Silicon G	
±28	±10	100	SG1502	† Silicon G	
			SG2502	Silicon G	
			SG3502	Silicon G	
			SG4501	Silicon G	
±42	±0.01	100	XR4194M	† Exar	
		200	**MCE4194**	**Micro Eng (4440)**	
			RC4194	Raytheon	80
			RM4194	† Raytheon	
			SG4194	† Silicon G	
			SG4194C	Silicon G	
Switching Regulators					
Switching Regulator Circuits					
			AM6301	**AMD (3115)**	
			722	Burr-Brown	
			724	Burr-Brown	
			XR1524	**† Exar (3190)**	
			XR1525A	**† Exar (3191)**	
			XR1527A	**† Exar (3191)**	
			XR2230	Exar	90
			XR2235	**Exar (3192)**	
			XR2524	**Exar (3190,3209)**	
			XR2525A	**Exar (3191)**	
			XR2527A	**Exar (3191)**	
			XR3524	**Exar (3190)**	
			XR3525A	**Exar (3191)**	
			XR3527A	**Exar (3191)**	
			XR494	**Exar (3189)**	
			XR495	**Exar (3190)**	
			SH1605	Fairchild	100
			μA494	Fairchild	
			μA494M	† Fairchild	
			μA78S40	Fairchild	
			μA78S40M	† Fairchild	
			ZN1060	† Ferranti	
			ZN1066E	Ferranti	
			ZN1066J	† Ferranti	
			MB3759	Fujitsu	
			MB3760	Fujitsu	
			LAS3800	Lambda	110
			LAS6300	Lambda	
			LAS6301	Lambda	
			MC3380	Motorola	
			MC34060	**Motorola (3297)**	
			MC3420	**Motorola (3297)**	
			MC35060	**Motorola (3297)**	
			MC3520	**† Motorola (3297)**	
			SG1526	**Motorola (3297)**	
			SG2526	**Motorola (3297)**	
			SG3526	**Motorola (3297)**	120
			TL494C	**Motorola (3297)**	
			TL494M	**† Motorola (3297)**	
			TL495C	**Motorola (3297)**	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Voltage Regulators (Cont'd)

Switching Regulators (Cont'd)

Switching Regulator Circuits

Output Voltage Hi	Low	Output Current, mA	Device	Source		Line
					(Cont'd)	
			TL495M	**† Motorola**	**(3297)**	
			μA78540	Motorola		
			LH1605	**† National**	**(3343)**	
			LH1605C	**National**	**(3343)**	
			LM1524	† National		
			LM2524	National		
			LM3524	National		
			SL442	Plessey		
			RC4191	Raytheon		
			RC4192	Raytheon		10
			RC4193	Raytheon		
			RM4191	† Raytheon		
			RM4192	† Raytheon		
			RM4193	Raytheon		
			CA1524	**† RCA**	**(3368)**	
			CA2524	**RCA**	**(3368)**	
			CA3524	**RCA**	**(3368)**	
			TDA4600	Siemens		
			TDA4700A	Siemens		
			NE5560	**Signetics**	**(3402)**	20
			NE5561	Signetics		
			SE5560	**† Signetics**	**(3402)**	
			SE5561	† Signetics		
			SG1524	† Signetics		
			SG3524	Signetics		
			TDA1060	Signetics		
			TDA2581	Signetics		
			TDA2640	Signetics		
			SG1524	† Silicon G		
			SG1525A	† Silicon G		30
			SG1526	† Silicon G		
			SG1527A	† Silicon G		
			SG2524	Silicon G		
			SG2525A	Silicon G		
			SG2526	Silicon G		
			SG2527A	Silicon G		
			SG3524	Silicon G		
			SG3525A	Silicon G		
			SG3526	Silicon G		
			SG3527	Silicon G		40
			SG3527A	Silicon G		
			PWM25	**Siliconix**	**(2820)**	
			PWM27	**Siliconix**	**(2820)**	
			SI1525B	Siliconix		
			SI1527B	Siliconix		
			SI2525B	Siliconix		
			SI2527B	Siliconix		
			SI3525B	Siliconix		
			SI3527B	Siliconix		
			ULN-8126	Sprague		50
			ULN-8160	Sprague		
			ULN-8161	Sprague		
			ULS-8126	† Sprague		
			ULS-8160	† Sprague		
			SG1524	† TI		
			SG2524	TI		
			SG3524	TI		
			SG3525A	TI		
			SG3527A	TI		
			TL493C	TI		60
			TL494C	TI		
			TL494M	† TI		
			TL495C	TI		
			TL497AC	TI		
			TL497AM	† TI		
			TL593C	**TI**	**(3428)**	
			TL594C	**TI**	**(3429)**	
			TL594M	**† TI**	**(3429)**	

(Continued)

Switching Regulator Circuits

Output Voltage Hi	Low	Output Current, mA	Device	Source		Line
					(Cont'd)	
			TL595C	**TI**	**(3430)**	
			PIC600	**Unitrode**	**(3446)**	70
			PIC601	**Unitrode**	**(3446)**	
			PIC602	**Unitrode**	**(3446)**	
			PIC610	**Unitrode**	**(3446)**	
			PIC611	**Unitrode**	**(3446)**	
			PIC612	**Unitrode**	**(3446)**	
			PIC625	**Unitrode**	**(3446)**	
			PIC626	**Unitrode**	**(3446)**	
			PIC627	**Unitrode**	**(3446)**	
			PIC635	**Unitrode**	**(3446)**	
			PIC636	**Unitrode**	**(3446)**	80
			PIC637	**Unitrode**	**(3447)**	
			PIC645	**Unitrode**	**(3446)**	
			PIC646	**Unitrode**	**(3446)**	
			PIC647	**Unitrode**	**(3446)**	
			PIC655	**Unitrode**	**(3446)**	
			PIC656	**Unitrode**	**(3446)**	
			PIC657	**Unitrode**	**(3446)**	
			PIC660	**Unitrode**	**(3446)**	
			PIC661	**Unitrode**	**(3446)**	
			PIC662	**Unitrode**	**(3446)**	90
			PIC670	**Unitrode**	**(3446)**	
			PIC671	**Unitrode**	**(3446)**	
			PIC672	**Unitrode**	**(3446)**	
			PIC730	**Unitrode**	**(3446)**	
			PIC740	**Unitrode**	**(3446)**	
			PIC800	**Unitrode**	**(3446)**	
			PIC801	**Unitrode**	**(3446)**	
			PIC810	**Unitrode**	**(3446)**	
			PIC811	**Unitrode**	**(3446)**	
			UC1524A	**Unitrode**	**(3444)**	100
			UC1527A	**Unitrode**	**(3445)**	
			UC1535	**Unitrode**	**(3445)**	
			UC1840	**Unitrode**	**(3445)**	
			UC2524A	**Unitrode**	**(3444)**	
			UC2525A	**Unitrode**	**(3445)**	
			UC2527A	**Unitrode**	**(3445)**	
			UC2840	**Unitrode**	**(3445)**	
			UC3524	**Unitrode**	**(3444)**	
			UC3524A	**Unitrode**	**(3444)**	
			UC3527A	**Unitrode**	**(3445)**	110
			UC3840	**Unitrode**	**(3445)**	
			UC493	**Unitrode**	**(3444)**	
			UC494	**Unitrode**	**(3444)**	
			UC495	**Unitrode**	**(3444)**	

† Military Temperature Range (−55° to 125°C)

* Typical Value

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LINEAR–Other Devices

Other Linear Devices

Function	Device	Source		Line
Absolute Module Value				
	9014	**OEI**	**(3347)**	
	9934	**OEI**	**(3347)**	
AC Amplifier, Quad, Single Supply				
	CA3048	† RCA		
AC Phase Control				
	TEA1087	Telefunken		
	U111	Telefunken		
Active Filter, Voltage Controlled, 4 stage				
	SSM2040	SSM		
	SSM2044	SSM		
Active Filters (See also Linear - Telecommunications Circuits)	ATF76	Burr-Brown		
	UAF11	Burr-Brown		
	UAF11H	† Burr-Brown		10
	UAF21	Burr-Brown		
	UAF21H	† Burr-Brown		
	UAF31	Burr-Brown		
	UAF41	Burr-Brown		
	CH1290	Cermetek		
	CH1295	Cermetek		
	CH1296	Cermetek		
	FLT-U2	Datel		
	FLT-U2M	Datel		
	ACF7092C	GI		20
	ACF7301C	GI		
	ACF7302C	GI		
	AF100	**† National**	**(3345)**	
	AF150	**National**	**(3345)**	
	AF151	**National**	**(3345)**	
	AF160	**National**	**(3345)**	
	AF161	National		
	MF10	**National**	**(3308)**	
	MF4	**National**	**(3305)**	
	MF5	**National**	**(3306)**	30
	MF6	**National**	**(3307)**	
ADC Subsystem, 5 1/2 Digit, Quad Slope Integrating				
	AD7555	**AD**	**(3174)**	
Alarm Circuit	S2561	AMI		
Alarm Circuit (Single chip detector/alarm system)				
	CA3164E	RCA		
	SCL5284	SSS		
	SCL5285	SSS		
	SCL5331	SSS		
Amplifier-SCR firing Circuit				
	ULN-2300M	Sprague		
Analog Memory, Serial-In, Parallel-Out				
	R5351	Reticon		
Analog Memory, Triple (three analog outputs which can be stepped up or down)				
	S175	Siemens		40
Analog Multiplexer, 16-Bit, Parallel-In, Serial Out				
	CCD16MUX	Micro Tech		
Analog Multiplexer, 16-Bit, Serial-In, Parallel-Out				
	CCD16DMUX	Micro Tech		
Analog Shift Register (Bucket Brigade Device) Dual 512 stage, acts as a variable delay line in the audio frequency range)	MN3001	Panasonic		
	MN3010	Panasonic		
	TDA1096	Signetics		
	TDA2110	Signetics		
Analog Shift Register (Bucket Brigade Device) (Dual 64 stage, acts as a variable delay line in the audio range)				
	MN3003	Panasonic		
Analog Shift Register (Bucket Brigade Device, 1024 stage)				
	MN3007	Panasonic		
	MN3204	Panasonic		
	MN3207	Panasonic		50
	TDA2107	Signetics		

Function	Device	Source		Line
Analog Shift Register (Bucket Brigade Device, 128 Stage)	MN3006	Panasonic		
Analog Shift Register (Bucket Brigade Device, 2048 stage)	MN3008	Panasonic		
	SAD4096	Reticon		
	TDA2108	Signetics		
Analog Shift Register (Bucket Brigade Device, 256 Stage)	MN3009	Panasonic		
Analog Shift Register (Bucket Brigade Device, 3328 stage)	MN3011	Panasonic		
Analog Shift Register (Bucket Brigade Device) (3,5,190 stages)	MN3012	Panasonic		
Analog Shift Register (Bucket Brigade Device, 4096 stage)	MN3005	Panasonic		
	TDA2015	Signetics		60
Analog Shift Register (Bucket Brigade Device, 512 stage)	MN3002	Panasonic		
	MN3004	Panasonic		
	TDA1022	Signetics		
	TDA2104	Signetics		
Analog Shift Register (CCD), 295x2 stage	R5104	Reticon		
Analog Shift Register Clock Generator/Driver	MN3101	Panasonic		
Analog Shift Register (Quad 64 stage)	CCD64	Micro Tech		
Analog Shift Register (185 stage, 190x2 stage)	S10110	AMI		
	S10111	AMI		
Analog Shift Register (256 stage)	CCD256SERP	Micro Tech		70
	CCD256SPS	Micro Tech		
Analog Shift Register (2000 stage, audio delay)	R5101	Reticon		
Analog Shift Register (455x2)	CCD321	Fairchild		
Analog Signal Averager (32 sample)	R5701	Reticon		
Analog Signal Processor - contains two transconductance amplifiers, two current-mode switches, output voltage buffer amplifier, and precision comparator	GAP-01A	PMI		
	GAP-01B	† PMI		
	GAP-01E	PMI		
	GAP-01F	PMI		
Attenuator	AN829	Panasonic		
Attenuator, Dual	AN829S	Panasonic		80
Attenuator, 3 1/2-Digit BCD, digitally controlled	AD7525K	AD		
	AD7525T	† AD		
	MP7525B	Micro Pwr		
	MP7525K	Micro Pwr		
	MP7525T	Micro Pwr		
Balanced Mixer	TL442C	TI		
	TL442M	TI		
Balanced Modulator	SL1025	Plessey		
Balanced Modulator/Demodulator	**AD630**	**AD**	**(3160,3161)**	
	MC12002	Motorola		
	MC12502	† Motorola		90
	MC1496	Motorola		
	MC1596	† Motorola		
	LM1496	National		
	LM1596	† National		
	AN610	Panasonic		
	AN612	Panasonic		
	SL640C	Plessey		

(Continued)

Function	Device	Source		Line
Balanced Modulator/Demodulator				
			(Cont'd)	
	SL641C	Plessey		
	LS025	SGS		100
	S042	Siemens		
	MC1496	Signetics		
	MC1596	† Signetics		
	TCA240	Signetics		
	TDA0820	Signetics		
	SG1496	Silicon G		
	SG1596	Silicon G		
	TA7320	Toshiba		
Blowout Resistant Transistor (simulates 40 V transistor with special protection)	LM195	† National		
	LM295	National		110
	LM395	National		
Bubble Memory Coil Driver	DS3616	National		
Bubble Memory Controller	7220-1	Intel		
Bubble Memory Current Pulse Generator	7230	Intel		
Bubble Memory Function Driver	DS3615	National		
	DS3618	National		
Bubble Memory Predriver	**SI7250**	**Siliconix**	**(2830)**	
Bubble Memory Sense Amplifier	DS3617	National		
Bubble Memory Dual Formatter/Sense Amplifier	7242	Intel		
Bubble Memory Quad VMOS Drive Transistors	7242	Intel		120
Comparator, Cache Address	**TMS2150-4**	**TI**	**(3961)**	
	TMS2150-5	**TI**	**(3961)**	
	TMS2150-7	**TI**	**(3961)**	
	TMS2150-9	**TI**	**(3961)**	
Comparator, Drives Lamps, Relays or Logic Loads	4082/03	Burr-Brown		
Comparator, Window (Internally set limits)	MK104	Analog Sys		
	4115/04	Burr-Brown		
Comparators, Programmable with Memory (High/Low Comparator)	CA3098	† RCA		
	CA3099	† RCA		
Constant Current Source, 1 μA to 10 mA	LM134	† National		130
	LM234	National		
	LM334	National		
Coordinate Converter (polar to cartesian)	**5090A**	**OEI**	**(3347)**	
Correlator, Analog to Analog	R5403	Reticon		
Correlator, Binary to Analog	R5401	Reticon		
	R5406	Reticon		
Correlator, 16 programmable taps	R5404	Reticon		
Correlator, 32 programmable taps	R5405	Reticon		
CRT Geometry/Focus Corrector	C310	Intronics		
	C311	Intronics		140
	C312	Intronics		
	C410	Intronics		
	C411	Intronics		
CRT Vertical Countdown	SN76566	TI		

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Other Devices (Cont'd)

Other Linear Devices (Cont'd)

Function	Device	Source	Line
Crystal Oscillators			
	SL1680	Plessey	
	SL680	Plessey	
Current Mirror, Adjustable Ratio NPN			
	TL010	TI	
Current Sensing Latch			
	SG1549	† Silicon G	
	SG2549	Silicon G	
	SG3549	Silicon G	
Current Source, Programmable			
	MJ335	Analog Sys	
Current Source, 4-Bit			
	9650	Fairchild	
Data Acquisition Controller for A/D Converter (ASCII Output)	CY600	Cybernetic	
Data Acquisition System, front end. Multiplexer, instrumentation amp (digitally programmable) and sample/hold	**HI5900-2**	**† Harris (2713,3288,3291)**	10
	HI5900-5	**Harris (2713,3288,3291)**	
Data Acquisition System front end. 16 pseudo-differential/ single ended input channels.	**HI5901**	**Harris (2715,3288,3291)**	
Data Acquisition System, 6 Channel, Sample/Hold, Pulse Width Output	μA9708	Fairchild	
Data Acquisition System, 8 Channel Differential, Sample/ Hold, 12-Bit Conversion	**HDAS-8MC**	**Datel (2623)**	
	HDAS-8MM	**† Datel (2620)**	
Data Acquisition System, 8 Channel Differential, 16 Channel Single Ended, Sample/Hold, 12-Bit Conversion (2 device set)	AD363K	AD	
	AD363S	† AD	
	AD364J	AD	
	AD364K	AD	
	AD364S	† AD	20
	AD364T	† AD	
Data Acquisition System, 8 Channel (expandable), Sample/ Hold, 8-Bit Conversion	MN7100	Micro Net	
	MN7100H	† Micro Net	
	MN7120	Micro Net	
	MN7120H	† Micro Net	
Data Acquisition System, 8 Channel, Sample/Hold, 12-Bit A/D	MN7140	Micro Net	
	MN7140H	† Micro Net	
Data Acquisition System, 8 Channel, 8-Bit Conversion	**ADC0808**	**National (3319)**	
	ADC0809	**National (3319)**	
Data Acquisition System, 8 Channel, 8-Bit Conversion, Microprocessor Compatible	**AD7581A**	**AD (3174)**	30
	AD7581B	**AD (3174)**	
	AD7581C	**AD (3174)**	
	AD7581J	**AD (3174)**	
	AD7581K	**AD (3174)**	
	AD7581L	**AD (3174)**	
	MP7581	**Micro Pwr (401,2749)**	
Data Acquisition System, 16 Channel or 8 Channel Differential, 12-Bit A/D	AD362K	AD	
	AD362S	† AD	
	DSM856	Burr-Brown	
	SDM854	Burr-Brown	40
	SDM857	Burr-Brown	

Function	Device	Source	Line
Data Acquisition System, 16 Channel, Sample/Hold, 12-Bit Conversion	**HDAS-16MC**	**Datel (2623)**	
	HDAS-16MM	**† Datel (2620)**	
Data Acquisition System, 16 Channel 8-Bit Conversion	**DAS-952R**	**Datel (2623)**	
	ADC0816C	**National (3319)**	
	ADC0817C	**† National (3319)**	
DC to DC Converter: See Regulators, Switching, under Linear - Voltage Regulators.			
Deglitcher (suppresses transients at outputs of D/A)	4902	Teledyne P	
	4902-83	Teledyne P	
Delay Line, Analog Audio Frequency Signals	CCD341A	Fairchild	50
Delay Line, Tapped	R5501	Reticon	
	R5502	Reticon	
Divider (See also Multipliers/Dividers below.)	AD535J	AD	
	AD535K	AD	
	4291	Burr-Brown	
	DIV100	Burr-Brown	
DVM Circuits-See Interface-Analog to Digital Converters, also Digital-Special			
Electronic Switching Circuit (for ignitions)	CA3165	RCA	
Electro-Optic Driver/Modulator	MU115	Analog Sys	
Fiber Optic Data Link	3712T/R	Burr-Brown	60
	3713T/R	Burr-Brown	
	3714T	Burr-Brown	
Fiber Optic Data Link Controller	SN76333	TI	
	SN76334	TI	
Fiber Optic Detector/Preamplifier	TIED461	TI	
	TIED463	TI	
Fiber Optic Emitter	**FOE360B-1**	**National (3345)**	
	FOE360B-2	**National (3345)**	
Fiber Optic Receiver	FOR110	Burr-Brown	
	FOR100B	**National (3345)**	70
	FOR261F-1	**National (3345)**	
	FOR261F-2	**National (3345)**	
Fiber Optic Transmitter	FOT110	Burr-Brown	
	FOT100B	**National (3345)**	
Flasher (LED)	LM3909	National	
Fluid Detector (oscillator, balance detector)	CS166	Cherry	
	LM1830	National	
	ULN-2429A	Sprague	
Frequency Switch, Programmable	MC3344	Motorola	
Frequency to Voltage/Voltage to Frequency Converter	VFC32	Burr-Brown	80
	VFC32M	† Burr-Brown	
	VFC42	Burr-Brown	
	VFC42M	† Burr-Brown	
	VFC52	Burr-Brown	
	VFC52M	† Burr-Brown	
	VFQ-1C	Datel	
	VFQ-3C	Datel	
	XR4151C	**Exar (3193)**	
	XR4151M	**† Exar (3193)**	
	LM131	† National	90
	LM131A	† National	
	LM231	National	

(Continued)

Function	Device	Source	Line
Frequency to Voltage/Voltage to Frequency Converter (Cont'd)			
	LM231A	National	
	LM331	National	
	LM331A	National	
	RC4151	Raytheon	
	RC4152	Raytheon	
	RC4153	Raytheon	
	RM4151	† Raytheon	
	RM4152	† Raytheon	100
	RM4153	† Raytheon	
	RV4151	Raytheon	
	RV4152	Raytheon	
	4780	Teledyne P	
	4781	Teledyne P	
	4782	Teledyne P	
	9400	Teledyne S	
	9401	Teledyne S	
	9402	Teledyne S	
Frequency/Tone Operated Devices-See Linear-Telecommunication Circuits			110
Frequency-to-Voltage Converter (precision)	CS2907	Cherry	
	CS2917	Cherry	
	LM2907	National	
	LM2917	National	
	L290	SGS	
	L291	SGS	
	L292	SGS	
	L293	SGS	
	4736	Teledyne P	
Function Generator, D/A Controller	CY360	Cybernetic	120
Hall Effect Devices (sense magnetic field) See also Digital-Other Digital Devices	DN6835	Panasonic	
	DN6837	Panasonic	
	DN835	Panasonic	
	UGN-3013	Sprague	
	UGN-3030	Sprague	
	UGN-3040	Sprague	
	UGN-3220	Sprague	
	UGN-3501	Sprague	
	UGN-3600	Sprague	
	UGN-3601	Sprague	130
	UGS-3030	† Sprague	
	TL172C	TI	
	TL173C	TI	
Image Area Sensor, Linear Self-Scanning, X-Ray Sensitive	IPI2D1	IPI	
	RA100X100	Reticon	
	RA256X256	Reticon	
	RA32X32	Reticon	
	RA50X50	Reticon	
	RL1024SFX	Reticon	
	RL128SFX	Reticon	140
	RL512SFX	Reticon	
Image Area Sensor, 488x380	CCD221	Fairchild	
Image Rotator	6125A	OEI	
Image Sensor, CC Photodiode	CCPD128x2	Reticon	
	CCPD128x4	Reticon	
	CCPD128x8	Reticon	
	CCPD256	Reticon	
Image Sensor, CC Photodiode, 1024x1	CCPD1024	Reticon	
Image Sensor, Circular, Self Scanning	R064	Reticon	
	R0720A	Reticon	150

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Other Devices (Cont'd)

Other Linear Devices (Cont'd)

Function	Device	Source	Line
Image Sensor, Linear Self Scanning			
	CCD111	Fairchild	
	CCD122	Fairchild	
	CCD133	Fairchild	
	CCD142	Fairchild	
	CCD143	Fairchild	
	IPI3010	IPI	
	IPI3016	IPI	
	IPI3032	IPI	
	IPI4050	IPI	
	IPI4064	IPI	10
	IPI4100	IPI	
	IPI4128	IPI	
	IPI4256	IPI	
	IPI7050	IPI	
	IPI7064	IPI	
	IPI7100	IPI	
	IPI7128	IPI	
	IPI7256	IPI	
	M256	IPI	
	M512	IPI	20
	MI1024	IPI	
	MEL1024K	Panasonic	
	MEL1024KV	Panasonic	
	MEL128	Panasonic	
	MEL512KV	Panasonic	
	MEL64A	Panasonic	
	MEL64x64	Panasonic	
	MEL864A	Panasonic	
	MN512	Panasonic	
	RL1024	Reticon	30
	RL1024S	Reticon	
	RL1024SF	Reticon	
	RL128	Reticon	
	RL128S	Reticon	
	RL128SF	Reticon	
	RL1728	Reticon	
	RL1872	Reticon	
	RL2048	Reticon	
	RL256	Reticon	
	RL512	Reticon	40
	RL512S	Reticon	
	RL512SF	Reticon	
	RL64	Reticon	
	RL936	Reticon	
Image Sensor, Photodiode, Circular and Annular			
	IPL30	IPI	
Image Sensor, 128x1, CCD			
	TC102	TI	
Image Sensor, 256x1, CCD			
	CCD111	Fairchild	
Image Sensor, 488x380 Area Element, CCD			
	CCD222	Fairchild	
Image Sensor, 1024x1, CCD			
	CCD133	Fairchild	
Image Sensor, 1024x1, CCD			
	MN8026	Panasonic	50
Image Sensor, 1728x1, CCD			
	CCD122	Fairchild	
Image Sensor, 1728x1, CCD			
	CCD121	Fairchild	
	TC101	TI	
Image Sensor, 2048x1, CCD			
	CCD142	Fairchild	
	CCD143	Fairchild	
	TC103	TI	
Image Sensor, 2048x1, CCD			
	μPD792	NEC-Electron	
	μPD794	NEC-Electron	
	MN8027	Panasonic	
Image Sensor, 3456x1, CCD			
	TC104	TI	60
Induction Motor Energy Saver			
	HV1000	**Harris (2741,3288)**	
	HV1005	**Harris (2741,3288)**	
	HV1010	**Harris (2741,3288)**	
Level Detector, Analog			
	TL489C	TI	
	TL490C	TI	
	TL491C	TI	
Level Detector, Logarithmic (3 DB increments)			
	TL487C	TI	
Level Detector, Logarithmic, 10 Step Analog			
	NSL4944	National	
Level Detector, Precision, (with internal reference, schmitt trigger action)			
	CS127	Cherry	
	CS401	Cherry	70
	CS402	Cherry	
	CS450	Cherry	
	TL560C	TI	
Level Detector, Precision Dual			
	CS122	Cherry	
	CS129	Cherry	
	CS130	Cherry	
Level Detector, 12-Point (for fluorescent displays)			
	XR2276	**Exar (3204)**	
	LC7555	Sanyo	
	LC7556	Sanyo	
Level Meter, Analog Input Drives a Bar of LED's			
	LB1405	Sanyo	80
	UAA170	Siemens	
	UAA180	Siemens	
Light Activated Switch			
	ZNP100	Ferranti	
	ZNP102	Ferranti	
	ZNP103	Ferranti	
	IPI15	IPI	
	IPI17	IPI	
	IPI1700	IPI	
	IPI18	IPI	
	IPI1800	IPI	90
	PS12	IPI	
	PS24	IPI	
	ULN-3330Y	Sprague	
	PF100	Unitrode	
	PF200	Unitrode	
	PF30	Unitrode	
	PF300	Unitrode	
	PF400	Unitrode	
	PF60	Unitrode	
	PR100	Unitrode	100
	PR200	Unitrode	
	PR30	Unitrode	
	PR300	Unitrode	
	PR400	Unitrode	
	PR60	Unitrode	
Light Detector (with buffer amplifier)			
	IPI16	IPI	
	μPC558	NEC-Electron	
	U123	Telefunken	
Light to Frequency Converter			
	IPI13	IPI	
Linear Filter (for sensor and control systems)			
	MF409	Analog Sys	110
Linear Isolator (for sensor and control systems)			
	MI900	Analog Sys	
Low Battery Indicator, Triggers on 3 V (for use with 3 NiCd cells)	ICM7201	Intersil	
LVDT Signal Conditioner			
	NE5520	Signetics	
	SE5520	**† Signetics (3372)**	
Motor and Solenoid Driver			
	CA3169	**RCA (3362)**	
	CA3169M	**† RCA (3362)**	
Motor Driver, Full Bridge			
	UDN-2952	**Sprague (2843)**	
	PIC900	**Unitrode (3446)**	
Motor Driver, Half Bridge			
	SG1635	Silicon G	
	SG3635	Silicon G	120
Motor Driver, Half H			
	SN75603	**TI (2857)**	
	SN75604	**TI (2857)**	
Motor Speed Controller			
	MC213	Analog Sys	
Motor Speed Regulator (for small dc motors). See also Linear—Consumer Circuits.			
	MC212	Analog Sys	
	CS140	Cherry	
	CS175	Cherry	
	CS2907	Cherry	
	CS2917	Cherry	
	μA7392	Fairchild	
	LM1014	National	130
	SL440	Plessey	
	TCA900	SGS	
	TCA910	SGS	
	TCA955	Siemens	
	NE5520	**Signetics (3372)**	
	TDA1003A	Signetics	
	TDA1006A	Signetics	
	TDA1506	Signetics	
	SG1731	† Silicon G	
	SG2731	Silicon G	140
	SG3731	Silicon G	
Motor, Stepping Motor Driver			
	SAA1027	Signetics	
	UDN-2949Z	**Sprague (2843)**	
	TL376C	TI	
Motor, Stepping Motor Translator/Driver			
	UCN-4202A	**Sprague (2843)**	
Multifunction Converter (generates output=(V1÷V2)			
	LH0094	**National (3343)**	
	LH0094C	**National (3343)**	
Multifunction Convertors (XY/Z)expM			
	4301	Burr-Brown	
	4302	Burr-Brown	
Multipliers	**AD539J**	**AD (3161)**	150
	AD539K	**AD (3161)**	
	AD539S	**† AD (3161)**	
	MM109	Analog Sys	
	XR2208	**Exar (3202)**	
	XR2208M	**† Exar (3202)**	
	XR2228	**Exar (3202)**	
	XR2228M	**† Exar (3202)**	
	ICL8013C	Intersil	
	ICL8013M	† Intersil	
	MC1494	Motorola	160
	MC1495	Motorola	
	MC1594	† Motorola	
	MC1595	† Motorola	
	CA3091	† RCA	
	SG1402	† Silicon G	
	SG1495	Silicon G	
	SG1595	† Silicon G	
	SG2402	Silicon G	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Other Devices (Cont'd)

Other Linear Devices (Cont'd)

Function	Device	Source		Line
Multipliers			(Cont'd)	
	SG3402	Silicon G		
	TA7158	Toshiba		
Multipliers/Dividers				
	AD530J	AD		
	AD530K	AD		
	AD530L	AD		
	AD530S	† AD		
	AD531J	**AD**	**(3161)**	
	AD531K	**AD**	**(3161)**	
	AD531L	**AD**	**(3161)**	
	AD531S	**† AD**	**(3161)**	10
	AD532J	**AD**	**(3161)**	
	AD532K	**AD**	**(3161)**	
	AD532S	**† AD**	**(3161)**	
	AD533J	**AD**	**(3161)**	
	AD533K	**AD**	**(3161)**	
	AD533L	**AD**	**(3161)**	
	AD533S	**† AD**	**(3161)**	
	AD534J	**AD**	**(3161)**	
	AD534K	**AD**	**(3161)**	
	AD534L	**AD**	**(3161)**	20
	AD534S	**† AD**	**(3161)**	
	AD534T	**† AD**	**(3161)**	
	4203	Burr-Brown		
	4203S	† Burr-Brown		
	4204	Burr-Brown		
	4204S	† Burr-Brown		
	4205	Burr-Brown		
	4205S	† Burr-Brown		
	4206	Burr-Brown		
	4213	Burr-Brown		30
	4213S	† Burr-Brown		
	4214	Burr-Brown		
	4214M	† Burr-Brown		
	RC4200	Raytheon		
	RC4200A	Raytheon		
Noise Generator (psuedo-ramdom sequence generator for audio)	S2688	AMI		
	MM5837	National		
Oscillator, Crystal Clock (250 kHz to 60 MHz)				
	CK1100A	Solarise		
	CK1114A	Solarise		
	CK1144A	Solarise		40
	CK1145A	Solarise		
Oscillator, Fixed Frequency (10 Hz to 20 kHz)				
	4023	Burr-Brown		
	4025	Burr-Brown		
Oscillator, Quadrature				
	4423	Burr-Brown		
Overvoltage Protector				
	L20V12	Lambda		
	L20V15	Lambda		
	L20V18	Lambda		
	L20V20	Lambda		
	L20V24	Lambda		
	L20V5	Lambda		50
	L20V6	Lambda		
	L20V9	Lambda		
	L60V12	Lambda		
	L60V15	Lambda		
	L60V24	Lambda		
	L60V28	Lambda		
	L60V5	Lambda		
	L60V6	Lambda		
	MC3423	Motorola		
	MC3523	† Motorola		60
	SG1542	† Silicon G		
	SG2542	Silicon G		
	SG3423	Silicon G		

(Continued)

Function	Device	Source		Line
Overvoltage Protector			(Cont'd)	
	SG3423A	Silicon G		
	SG3523	† Silicon G		
	SG3523A	† Silicon G		
	SG3542	Silicon G		
	MC3423	TI		
Peak Detector (senses and holds peak)				
	4085	Burr-Brown		
	4085M	† Burr-Brown		70
	5030A	**OEI**	**(3347)**	
	5032A	**OEI**	**(3347)**	
	5902	**† OEI**	**(3347)**	
	5905	**OEI**	**(3347)**	
	PKD-01	PMI		
Phase Detector (module)				
	3420	**OEI**	**(3347)**	
	3421	**OEI**	**(3347)**	
PIN Diode Driver				
	DH0035	**† National**	**(3344)**	
	DH0035C	**National**	**(3344)**	
	UDS-5790H	**† Sprague**	**(2843)**	80
	UDS-5791H	**† Sprague**	**(2843)**	
Potentiometer, Dual Double				
	TDA1074	Signetics		
Potentiometer, 3 1/2-Digit BCD				
	AD7525K	**AD**	**(3166)**	
	AD7525L	**AD**	**(3166)**	
	AD7525T	**† AD**	**(3166)**	
	AD7525U	**† AD**	**(3166)**	
Power Control Subsystem				
	AM6300	**AMD**	**(3112)**	
Power Control Zero Voltage Switch				
	SL445A	Plessey		
Power Supply Control (voltage reference, over and under voltage sensing)				
	XR1543	**Exar**	**(3192)**	
	XR2543	**Exar**	**(3192)**	90
	XR3543	**Exar**	**(3192)**	
	SG1543	† Silicon G		
	SG1544	† Silicon G		
	SG2543	Silicon G		
	SG2544	Silicon G		
	SG3543	Silicon G		
	SG3544	Silicon G		
Power Supply Controller (voltage reference, pulse generator and timing circuitry, error amp)				
	LA5700	Sanyo		
	TL496C	TI		
Power Supply Fault Monitor (monitors 3 dc voltages and ac input)	SG1547	† Silicon G		100
	SG2547	Silicon G		
	SG3547	Silicon G		
Power Supply Overvoltage Sensing Circuit, Pin Programmable				
	MC34062	Motorola		
	MC35062	Motorola		
Power Supply Overvoltage Sensing Circuit, Three-Terminal				
	MC34061	Motorola		
	MC34061A	Motorola		
	MC35061	Motorola		
	MC35061A	Motorola		
Power Supply Supervisory Circuit				
	MC3324	Motorola		
	MC3324A	Motorola		110
	MC3424	Motorola		
	MC3424A	Motorola		
	MC3524	Motorola		
	MC3524A	Motorola		

Function	Device	Source		Line
Power Supply Supervisory/Over-Under Voltage Protection Circuit	MC3425	Motorola		
	MC3425A	Motorola		
	MC3525	Motorola		
	MC3525A	Motorola		
Pressure Transducers, Absolute				
	LX04XXA	National		
	LX05XXA	National		120
	LX05XXA0	National		
	LX06XXXA	National		
	LX14XXA	National		
	LX14XXAF	National		
	LX14XXAS	National		
	LX1600A	National		
	LX16XXA	National		
	LX18XXA	National		
Pressure Transducers, Backward Gage				
	LX0603GB	National		
	LX06XXGB	National		130
	LX16XXGB	National		
	LX18XXGB	National		
Pressure Transducers, Differential				
	LX16XXD	National		
	LX18XXD	National		
	LX96XXD	National		
Pressure Transducers, Gage				
	LX06002D	National		
	LX06002G	National		
	LX06XXXD	National		
	LX16XXG	National		
	LX18XXG	National		140
Programmable Quad Comparator, Micropower				
	LP165	**National**	**(3316)**	
	LP365	**National**	**(3316)**	
Proximity Detector, Electromagnetic				
	CS191	Cherry		
	CS209	Cherry		
Pulse-Width Modulated Controller (for motors, heaters, lamps)	MC343	Analog Sys		
Pulse-Width Modulator Control System (for switching regulators, motor-speed controllers)				
	XR2230	**Exar**	**(3191)**	
Quantizer, 4-Bit (Quantizes analog voltage into 15 equally-spaced levels and outputs 4-Bit binary digital word at sampling rates up to 100 MHz.)				
	AM6688	**AMD**	**(3109)**	
	AM6688L-6	**AMD**	**(3109)**	
	AM6688L-7	**AMD**	**(3109)**	
	AM6688L-8	**AMD**	**(3109)**	150
	AM6688M-6	**† AMD**	**(3109)**	
	AM6688M-7	**† AMD**	**(3109)**	
	AM6688M-8	**† AMD**	**(3109)**	
Read Chain Data Comparator				
	TL712	TI		
	TL721	TI		
Read/Write System for Magnetic Cards, Tapes, or Disks				
	CA3196	RCA		
	CA3197	RCA		
	CA3198	RCA		
Reference Diode				
	AN156	Panasonic		
	AN179	Panasonic		160
Reference Voltage				
	AD584J	AD		
	AD584K	AD		
	AD584L	AD		
	AD584S	† AD		
	AD584T	† AD		
	AD584U	† AD		
	MC1400-6	**Motorola**	**(2761)**	
	MC1400A-6	**Motorola**	**(2761)**	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Other Devices (Cont'd)

Other Linear Devices (Cont'd)

Function	Device	Source		Line
Reference Voltage (Cont'd)				
	MC1404-6	Motorola	(2761)	
	MC1500-6	† Motorola	(2761)	
	MC1500A-6	† Motorola	(2761)	
	MC1504-6	† Motorola	(2761)	
Reference Voltage (two terminal active circuit 1.220 V ± 5%)	MP5010	† Micro Pwr	(401,3292)	
	MP5010A	† Micro Pwr	(401,3292)	
	LM113	† National	(3304)	
	LM113-1	† National	(3304)	
	LM113-2	National	(3304)	
	LM313	National	(3304)	10
	9491AM	† Teledyne S		
	9491B	Teledyne S		
	9491BM	Teledyne S		
Reference Voltage (two terminal active circuit) 1.235 V ± 2%	LM185	† National	(3304)	
	LM285	National	(3304)	
	LM385	National		
Reference Voltage (two terminal active circuit) 1.8 to 5.6 V	LM103	† National		
Reference Voltage, 1.23 V	AD589J	AD	(3178)	
	AD589K	AD	(3178)	
	AD589L	AD	(3178)	20
	AD589M	AD	(3178)	
	AD589S	† AD	(3178)	
	AD589T	† AD	(3178)	
	AD589U	† AD	(3178)	
	ICL8069	Intersil		
	ICL8069M	† Intersil		
	LM185-1	† National	(3304)	
	LM285-1	National	(3304)	
	LM385-1	National		
Reference Voltage, 1.26 V (two terminal active circuit)	ZN423	Ferranti		30
Reference Voltage, 2.45 V (two terminal active circuit)	VR-182A	Datel		
	VR-182B	Datel		
	VR-182C	Datel		
	ZN404	Ferranti		
	ZN458	Ferranti		
	ZN458A	Ferranti		
	ZN458B	Ferranti		
Reference Voltage, 2.5 V	AD1403	AD	(3178)	
	AD1403A	AD	(3178)	
	AD580J	AD	(3178)	40
	AD580K	AD	(3178)	
	AD580L	AD	(3178)	
	AD580S	† AD	(3178)	
	AD580T	† AD	(3178)	
	AD580U	† AD	(3178)	
	MP5540	Micro Pwr		
	MC1400-2	Motorola	(2761)	
	MC1400A-2	Motorola	(2761)	
	MC1403	Motorola	(2761)	
	MC1403A	Motorola	(2761)	50
	MC1500-2	† Motorola	(2761)	
	MC1500A-2	† Motorola	(2761)	
	MC1503	† Motorola	(2761)	
	MC1503A	Motorola	(2761)	
	LM136-2	† National	(3304)	
	LM136A-2	† National	(3304)	
	LM185-2	† National	(3304)	
	LM236-2	National	(3304)	
	LM236A-2	National	(3304)	

(Continued)

Function	Device	Source		Line
Reference Voltage, 2.5 V (Cont'd)				
	LM285-2	National	(3304)	60
	LM336-2	National	(3304)	
	LM385-2	National		
	SG1503	Silicon G		
	SG2503	Silicon G		
	SG3503	Silicon G		
Reference Voltage, 2.5 V (trimmable output)	ZNREF025	Ferranti		
Reference Voltage, 4 V (trimmable output)	ZNREF040	Ferranti		
Reference Voltage, 5 V	HA-1620	Harris		
	HA-1625	Harris		
	MP5531	† Micro Pwr	(401,3292)	70
	MP5541	† Micro Pwr		
	MP5543	† Micro Pwr		
	REF-02	† Micro Pwr		
	REF-02A	† Micro Pwr		
	REF-02C	Micro Pwr		
	REF-02D	Micro Pwr		
	REF-02E	Micro Pwr		
	REF-02H	Micro Pwr		
	MC1400-5	Motorola	(2761)	
	MC1400A-5	Motorola	(2761)	80
	MC1404-5	Motorola	(2761)	
	MC1500-5	† Motorola	(2761)	
	MC1500A-5	Motorola	(2761)	
	MC1504-5	† Motorola	(2761)	
	LM136-5	† National	(3304)	
	LM136A-5	† National	(3304)	
	LM236-5	National	(3304)	
	LM236A-5	National	(3304)	
	LM336-5	National	(3304)	
	LM336B-5	National	(3304)	90
	REF-02	† PMI		
	REF-02A	† PMI		
	REF-02C	PMI		
	REF-02D	PMI		
	REF-02E	PMI		
	REF-02H	PMI		
	REF-05A	PMI		
	REF-05B	† PMI		
	9495A	† Teledyne S		
	9495C	Teledyne S		100
	TSC9495	Teledyne S		
Reference Voltage, 5 V (trimmable output)	ZNREF050	Ferranti		
Reference Voltage, 6.1 V (trimmable output)	ZN406	Ferranti		
	ZNREF061	Ferranti		
Reference Voltage, 6.9 V Temperature Stabilized	LM129	† National	(3304)	
	LM199	† National	(3304)	
	LM199A	† National	(3304)	
	LM299	National	(3304)	
	LM299A	National	(3304)	
	LM329	National	(3304)	110
	LM399	National	(3304)	
	LM3999	National	(3304)	
	LM399A	National	(3304)	
	LM329	Raytheon		
Reference Voltage, 7.5 V	MP5544	Micro Pwr		
Reference Voltage, 10 V (trimmable output)	ZNREF100	Ferranti		
Reference Voltage, 10 V(or -10 V)	AD2700J	AD	(3178)	
	AD2700L	AD	(3178)	
	AD2700S	† AD	(3178)	

(Continued)

Function	Device	Source		Line
Reference Voltage, 10 V(or -10 V) (Cont'd)				
	AD2700U	† AD	(3178)	120
	AD2701J	AD	(3178)	
	AD2701L	AD	(3178)	
	AD2701S	† AD	(3178)	
	AD2701U	† AD	(3178)	
	AD2710K	AD	(3178)	
	AD2710L	AD	(3178)	
	AD581J	AD	(3178)	
	AD581K	AD	(3178)	
	AD581L	AD	(3178)	
	AD581S	† AD	(3178)	130
	AD581T	† AD	(3178)	
	AD581U	† AD	(3178)	
	HA-1600-2	† Harris		
	HA-1602-2	† Harris		
	HA-1605-5	Harris		
	HA-1610-2	† Harris		
	HA-1615-2	† Harris		
	HA-1615-5	Harris		
	HSREF01	Hybrid Sys		
	R675B-1	† Hybrid Sys		140
	R675B-4	† Hybrid Sys		
	R675B-5	† Hybrid Sys		
	R675C-1	Hybrid Sys		
	R675C-5	Hybrid Sys		
	MP5532	† Micro Pwr	(401,3292)	
	MP5542	† Micro Pwr		
	MP5545	† Micro Pwr		
	MC1400-10	Motorola	(2761)	
	MC1400A-10	Motorola	(2761)	
	MC1404-10	Motorola	(2761)	150
	MC1404A-10	Motorola	(2761)	
	MC1500-10	† Motorola	(2761)	
	MC1500A-10	† Motorola	(2761)	
	MC1504-10	† Motorola	(2761)	
	MC1504A-10	† Motorola	(2761)	
	LH0070	† National	(3304,3343)	
	REF-01	† PMI		
	REF-01A	† PMI		
	REF-01C	PMI		
	REF-01D	PMI		160
	REF-01E	PMI		
	REF-01H	PMI		
	REF-10A	PMI		
	REF-10B	† PMI		
	REF-01	Raytheon		
	REF-01A	Raytheon		
	REF-01C	Raytheon		
	REF-01D	Raytheon		
	REF-01E	Raytheon		
	REF-01H	Raytheon		170
	TSC9496	Teledyne S		
Reference Voltage, 10.024 V	LH0071-0	National	(3304,3343)	
	LH0071-1	National	(3304,3343)	
	LH0071-2	National	(3304,3343)	
Reference Voltage, 10.24 V	LH0071	National	(3304,3343)	
Reference Voltage, ± 10 V	AD27025	AD		
	AD2702L	AD	(3178)	
	AD2702S	† AD	(3178)	
	AD2702U	AD	(3178)	
	AD2712K	AD	(3178)	180
	AD2712L	AD	(3178)	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Other Devices (Cont'd)

Other Linear Devices (Cont'd)

Function	Device	Source	Line
Reference Voltage, ± 10 V (Cont'd)			
	AD2720	**AD (3177)**	
	HA-1608	**Harris (3210,3287)**	
	R675B-3	† Hybrid Sys	
	R675C-3	Hybrid Sys	
Regulator Diode with Amplifier (6.8 to 11 V)			
	MCA-series	Motorola	
Resolver and Synchro Systems			
	SDC1740	AD	
	SDC1741	AD	
	SDC1742	AD	
	DRC10500	DDC	
	HMSDC-8700	DDC	10
	HRCDX-14	DDC	
	HRCT-14	DDC	
	HRDC-10	DDC	
	HRDC-14	DDC	
	HSCDX-14	DDC	
	HSCT-14	DDC	
	HSDC-10	DDC	
	HSDC-14	DDC	
	HSDC-360	DDC	
	HSDC-8915	DDC	20
	HSDC-8916	DDC	
	HSDC-8917	DDC	
	HSDC-8918	DDC	
	HSDC-8919	DDC	
	HSDC-8920	DDC	
	HSDC-8921	DDC	
	HSDC-8922	DDC	
	HXCDX-14	DDC	
	HXCT-14	DDC	
	HXDC-10	DDC	30
	HXDC-14	DDC	
	SDC-14510	DDC	
	SDC-14520	DDC	
	SDC19100	DDC	
Ring Modulator, four transistor			
	SL355	Plessey	
	TBA673	Plessey	
	TBA673	Signetics	
RMS to DC Converter			
	AD536A	**AD (3161)**	
	AD536AJ	**AD (3161)**	
	AD536AK	**AD (3161)**	40
	AD536AS	**† AD (3161)**	
	AD636J	**AD (3161)**	
	AD636K	**AD (3161)**	
	AD637J	**AD (3159,3161)**	
	AD637K	**AD (3159,3161)**	
	4340	Burr-Brown	
	4341	Burr-Brown	
	LH0091	**† National (3343)**	
	LH0091C	**National (3343)**	
Sample and Hold Circuits			
	LF198	AMD	50
	LF298	AMD	
	LF398	† AMD	
	AD582K	**AD (3181)**	
	AD582S	**† AD (3181)**	
	AD583K	**AD (3181)**	
	AD583S	**† AD (3181)**	
	AD585J	**AD (3179,3181)**	
	AD585S	**† AD (3179,3181)**	
	ADSHC-85	**AD (3181)**	
	ADSHC-85E	† AD	60
	ADX346	AD	
	HTC-0300	**AD (3181)**	
	HTC-0500	**AD (3180)**	

(Continued)

Function	Device	Source	Line
Sample and Hold Circuits (Cont'd)			
	HTS-0025	**AD (3181)**	
	MH410	Analog Sys	
	MN245	Analogic	
	SHC23	Burr-Brown	
	SHC298AM	Burr-Brown	
	SHC80	Burr-Brown	
	SHC85	Burr-Brown	70
	SHC85ET	Burr-Brown	
	SHM-6MM	**† Datel (2620)**	
	SHM-7MC	**Datel (2622)**	
	SHM-7MR	† Datel	
	SHM-8MC	Datel	
	SHM-HUMC	**Datel (2622)**	
	SHM-HUMM	**† Datel (2620)**	
	SHM-IC-1	**Datel (2622)**	
	SHM-IC-1M	**† Datel (2622)**	
	SHM-LM-2	**Datel (2622)**	80
	SHM-LM-2M	**† Datel (2622)**	
	μA398	Fairchild	
	μAF198	† Fairchild	
	μAF298	Fairchild	
	HA-2420	**Harris (3214,3287)**	
	HA-2425	**† Harris (3214,3287)**	
	HA-5310	Harris	
	HA-5315	Harris	
	HA-5320-2	**† Harris (3277,3287)**	
	HA-5320-5	**Harris (3277,3287)**	90
	SH-8518	DDC	
	IH5110	† Intersil	
	IH5111	† Intersil	
	IH5112	Intersil	
	IH5113	Intersil	
	IH5114	Intersil	
	IH5115	Intersil	
	MN343	Micro Net	
	MN343H	† Micro Net	
	MN344	Micro Net	100
	MN344H	† Micro Net	
	MN346	Micro Net	
	MN346H	† Micro Net	
	MN347	Micro Net	
	MN347H	† Micro Net	
	MN375	Micro Net	
	MN7130	Micro Net	
	MN7130H	† Micro Net	
	LF198	† National	
	LF198A	† National	110
	LF298	National	
	LF298A	National	
	LF398	National	
	LF398A	National	
	LH0023	**† National (3343)**	
	LH0023C	**National (3343)**	
	LH0043	**† National (3343)**	
	LH0043C	**National (3343)**	
	LH0053	**† National (3343)**	
	LH0053C	**National (3343)**	120
	SHM6401	National	
	μPC649	NEC-Electron	
	5021	**OEI (3347)**	
	5025	**OEI (3347)**	
	SMP10A	† PMI	
	SMP10B	† PMI	
	SMP10E	PMI	
	SMP10F	PMI	
	SMP11A	† PMI	
	SMP11B	† PMI	130
	SMP11E	PMI	

(Continued)

Function	Device	Source	Line
Sample and Hold Circuits (Cont'd)			
	SMP11F	PMI	
	SMP11G	PMI	
	SMP81E	PMI	
	SMP81F	PMI	
	LF298	Signetics	
	LF398	Signetics	
	NE5537	Signetics	
	SE5537	† Signetics	
	CSH101A	† Teledyne C	140
	4856	Teledyne P	
	4857	Teledyne P	
	4860	Teledyne P	
	4860-83	† Teledyne P	
	TL195C	**TI (3436)**	
SCR/TRIAC Control (burst control)			
	L121	SGS	
SCR/TRIAC Control (phase control)			
	L120	SGS	
	UAA145	Telefunken	
	UAA146	Telefunken	
Sensor/Controller, Air Temperature			
	MS120	Analog Sys	150
Sensor/Controller, Ground Moisture and Liquid Level			
	MS211	Analog Sys	
Sensor/Controller, Relative Humidity			
	MS214	Analog Sys	
Sensor, Ultrasonic Object Detector (position and distance)			
	MS118	Analog Sys	
Sequencer, 10 Outputs, 100 μs to 100 Seconds			
	MC116	Analog Sys	
Serial Analog Delay (analog storage units with read in/read out shift register) (See also Analog Shift Registers above)			
	DAS1024A	Reticon	
	SAD1024A	Reticon	
	SAD512	Reticon	
	SAD512D	Reticon	
Serial Analog Delay, Tapped (bucket brigade with 32 taps)			
	TAD32A	Reticon	
Serial Analog Memory (analog storage with independent read-in and read-out shift registers)			
	SAM128LR	Reticon	160
	SAM128V	Reticon	
Servo Amplifier, for Motor Control			
	ZN409CE	Ferranti	
	ZN419CE	Ferranti	
Servo Controller, for VTR or dc Servos			
	AN6880	Panasonic	
	LB1601	Sanyo	
Servo Controller, Proportional Control			
	XR2264	Exar	
	XR2265	Exar	
Servo Controller, Radio Controlled Cars, 2 Channel			
	XR2266	Exar	
Signal Processor, Real Time Digital Processing of Analog Signals (programmable)			
	2920-10	Intel	
	2920-16	Intel	170
	2920-18	Intel	
Smoke Detectors: See Linear-Consumer Circuit, Miscellaneous			
Solar Transceiver			
	M1812	National	
Solenoid Driver	MC3484V2	TI	
	MC3484V4	TI	
Switch Driver, for Power Transistors			
	SG1629	† Silicon G	
	SG3629	Silicon G	

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

LINEAR–Other Devices (Cont'd)

Other Linear Devices (Cont'd)

Function	Device	Source	Line
Switches	ICL8018AC	Intersil	
	ICL8018AM	† Intersil	
	ICL8019AC	Intersil	
	ICL8019AM	† Intersil	
	ICL8020AC	Intersil	
	ICL8020AM	† Intersil	
Switching Regulators. See Linear-Voltage Regulators, Switching			
Tachometer: See Frequency to Voltage and Frequency Switch above			
Temperature Controlled Differential Pair			
	μA726C	Fairchild	
	μA726M	† Fairchild	10
Temperature Transducers			
	AD590I	† AD	
	AD590J	† AD	
	AD590K	† AD	
	AD590L	† AD	
	AD590M	AD	
	AD590I	† Intersil	
	AD590J	† Intersil	
	AD590K	† Intersil	
	AD590L	† Intersil	
	AD590M	† Intersil	20
	ICL8073	Intersil	
	ICL8074	Intersil	
	MMBTS102	Motorola	
	MMBTS103	Motorola	
	MMBTS105	Motorola	
	LM134	† National	
	LM135	† National	
	LM234	National	
	LM334	National	
	LM335	National	30
	LM3911	National	
	μPC3911	NEC-Electron	
	REF-02	† PMI	
	REF-02A	† PMI	
	REF-02C	PMI	
	REF-02D	PMI	
	REF-02E	PMI	
	REF-02H	PMI	
	LA7011	Sanyo	
Thermal Converter (matched transistors, diffused resistors)	4131	Burr-Brown	40
Threshold Switch (oscillator, switch with hysteresis)	TCA105	Siemens	
Threshold Switch (2/3 supply voltage)			
	CS560	Cherry	
	TCA345	Siemens	
Tone Decoder (traffic signal control and detector)	LA2200	Sanyo	
Track and Hold			
	ADH-050	DDC	
	ADH-051	DDC	
	TH-8530	DDC	
Traffic Information Control System (ARI-DK type)	LA2211	Sanyo	
Transversal Filter, Quad Chirped (for discrete fourier transform and power spectral density applications)			
	R5601-1	Reticon	
	R5601-2	Reticon	50
Undervoltage Protector/Low Voltage Monitor	CS188	Cherry	
Video Delay, CCD			
	CCD321A	Fairchild	
Voltage Converter, +5 V to ±5 V			
	VI-7660C	Datel	
	VI-7660M	Datel	
	ICL7660	Intersil	
Voltage Detector, Indicator, Regulator, (programmable zener)	ICL8211C	Intersil	
	ICL8211M	† Intersil	
	ICL8212C	Intersil	
	ICL8212M	† Intersil	
Voltage Overvoltage Protector. (Crowbar) See Overvoltage Protector above			60
Voltage to Frequency Converter			
	AD537J	**AD** **(3176)**	
	AD537K	**AD** **(3176)**	
	AD537S	**† AD** **(3176)**	
	AD650	**AD** **(3176)**	
	ADVFG32	AD	
	VFQ-1	Datel	
	VFQ-2	Datel	
	VFQ-3	Datel	
	3930	**OEI** **(3347)**	
	SSM2031	SSM	70
	4731	† Teledyne P	
	4731-83	† Teledyne P	
	4732	Teledyne P	
	4732-83	† Teledyne P	
	4733	† Teledyne P	
	4733-83	† Teledyne P	
	4734	Teledyne P	
	4734-83	† Teledyne P	
	4735	† Teledyne P	
	4735-83	† Teledyne P	80
	4736-83	† Teledyne P	
	4739	Teledyne P	
	4739-80	† Teledyne P	
	4743	Teledyne P	
	4743-80	† Teledyne P	
Voltage to Frequency/Frequency to Voltage Converter			
	VFC32	Burr-Brown	
	VFC32M	† Burr-Brown	
	VFC32UM	† Burr-Brown	
	VFC32VM	† Burr-Brown	
	VFC32WM	† Burr-Brown	90
	VFC42	Burr-Brown	
	VFC42M	† Burr-Brown	
	VFC52	Burr-Brown	
	VFC52M	† Burr-Brown	
	VFV-100K	Datel	
	VFV-10K	Datel	
	XR4151	**Exar** **(3193)**	
	XR4151M	† Exar	
	MCEVFC32	**Micro Eng** **(4440)**	
	LM131	† National	100
	LM131A	† National	
	LM231	National	
	LM231A	National	
	LM331	National	
	LM331A	National	
	RC4151	Raytheon	
	RC4152	Raytheon	
	RC4153	Raytheon	
	RM4151	† Raytheon	
	RM4152	† Raytheon	110
	RM4153	† Raytheon	
	RV4151	Raytheon	
	RV4152	Raytheon	
	4780	Teledyne P	
	4781	Teledyne P	
	4782	Teledyne P	
	9400	Teledyne S	
	9401	Teledyne S	
	9402	Teledyne S	
Voltage Variable Gain Block	MQ328	Analog Sys	120
Window Discriminator (indicates voltage above, below, inside, or outside two adjustable limits)	TCA965	Siemens	
Window Discriminator (indicates when input is above or below two limits)	CS180	Cherry	
Zero Voltage and Zero Crossing Triggers (triac and SCR control)	CA3059	Motorola	
	CA3079	Motorola	
	MC3370	Motorola	
	SL441	Plessey	
	SL443	Plessey	
	SL446	Plessey	
	CA3058	† RCA	
	CA3059	† RCA	130
	CA3079	† RCA	
	TCA780	Siemens	
	TCA280A	Signetics	
	TDA1023	Signetics	
	TDA1024	Signetics	
	SG3059	Silicon G	
	SG3079	Silicon G	
	U106	Telefunken	
	U217	Telefunken	
	TL440C	TI	140
	TA7606	Toshiba	
Dual Over/Under-Voltage Detector	ICL7665	Intersil	
Dual Transistors, Monolithic, Matched, See Linear-Arrays			
Dual Voltage Level indicator: See Window Discriminator below			
Quad Voltage Level Monitor/Alarm (activated if any of 4 inputs differs by more than ±5, ±10 or ±20% of selected value)	ULN-2401A	Sprague	
Two-Wire Bidirectional Communication System	**LM1893**	**National** **(3331)**	

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

Advanced Micro Devices

LINEAR
Am6012

Distinctive Characteristics

- All grades 12-bit monotonic over temperature
- Differential nonlinearity to ±.012% (13 bits) max. over temperature
- Trimless design is inherently monotonic
- Fast settling output current: 250nsec
- Full scale current 4mA
- High output impedance and compliance: −5 to +10V
- 100% MIL-STD-883 reliability assurance testing
- Differential current outputs
- Low cost
- High-speed multiplying capability
- Direct interface to TTL, CMOS, ECL, HTL, NMOS
- Performance unchanged over supply range
- Low power consumption: 230mW
- R_{OUT}, C_{OUT} independent of logic code

GENERAL DESCRIPTION

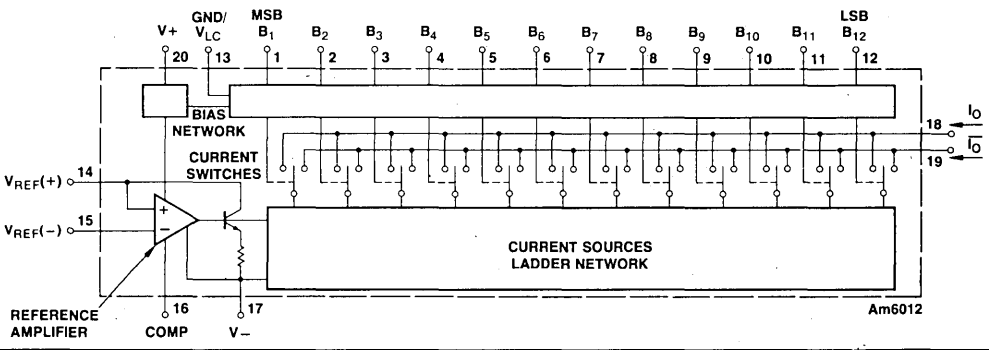
The Am6012 series of 12-bit monolithic multiplying Digital to Analog Converters represent a new level of high speed and accuracy coupled with low cost. The Am6012 is the first 12-bit D/A Converter ever built using standard processing without the requirements of thin film resistors and/or active trimming of individual devices. The Am6012 uses sophisticated new circuit design concepts that give inherent monotonicity without requiring ultra precision internal components.

The Am6012 design guarantees a more uniform step size than is possible with standard binarily weighted DAC's. This ±1/2 LSB differential nonlinearity is desirable in many applications where local linearity is critical. The uniform step size allows finer resolution of levels and in most applications is more useful than conformance to an ideal straight line from zero to full scale.

The Am6012 has high voltage compliance, high impedance dual complementary outputs which increase its versatility and enable differential operation to effectively double the peak to peak output swing. These outputs can be used directly without op amps in many applications. The dual complementary outputs can also be connected in A/D converter applications to present a constant load current and significantly reduce switching transients and increase system throughput. Output full scale current is specified at 4mA, allowing use of smaller load resistors to minimize the output RC delay which usually dominates settling time at the 12-bit level.

The Am6012 series guarantees full 12-bit monotonicity for all grades and differential nonlinearity as tight as ±.012% (13 bits) over the entire temperature range. Device performance is essentially independent of power supply voltage. The devices work over a wide operating range of +5, −12 volts to ±18 volts.

FUNCTIONAL DIAGRAM

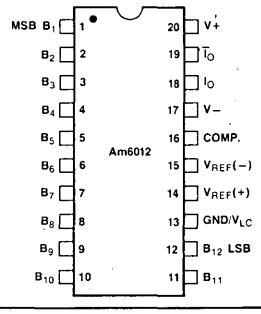


LIC-846

ORDERING INFORMATION

Order Number	Package	Temperature Range	Differential Nonlinearity
AM6012ADM	Ceramic	−55 to +125°C	±.012%
AM6012DM	Ceramic	−55 to +125°C	±.025%
AM6012ADC	Ceramic	0 to +70°C	±.012%
AM6012APC	Plastic	0 to +70°C	±.012%
AM6012DC	Ceramic	0 to +70°C	±.025%
AM6012PC	Plastic	0 to +70°C	±.025%

CONNECTION DIAGRAM – Top View



Note:
Pin 1 is marked for orientation.

LIC-847

LINEAR
Am6012

MAXIMUM RATINGS above which useful life may be impaired

Operating Temperature		Power Supply Voltage	±18V
Am6012ADM, Am6012DM	−55 to + 125°C	Logic Inputs	−5 to +18V
Am6012ADC, Am6012DC	0 to +70°C	Analog Current Outputs	−8 to +12V
Am6012APC, Am6012PC	0 to +70°C	Reference Inputs V_{14}, V_{15}	V− to V+
Storage Temperature	−65 to +125°C	Reference Input Differential Voltage (V_{14} to V_{15})	±18V
Lead Temperature (Soldering, 60 sec)	300°C	Reference Input Current (I_{14})	1.25mA

ELECTRICAL CHARACTERISTICS

These specifications apply for $V_+ = +15V$, $V_- = -15V$, $I_{REF} = 1.0mA$, over the operating temperature range unless otherwise specified.

				Am6012A			Am6012			
Parameter	Description		Test Conditions	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
	Resolution			12	12	12	12	12	12	Bits
	Monotonicity			12	12	12	12	12	12	Bits
D.N.L.	Differential Nonlinearity		Deviation from ideal step size	–	–	±.012	–	–	±.025	%FS
				13	–	–	12	–	–	Bits
N.L.	Nonlinearity		Deviation from ideal straight line	–	–	±.05	–	–	±.05	%FS
I_{FS}	Full Scale Current		V_{REF} = 10.000V $R_{14} = R_{15}$ = 10.000kΩ T_A = 25°C	3.967	3.999	4.031	3.935	3.999	4.063	mA
TCI_{FS}	Full Scale Tempco			–	±5	±20	–	±10	±40	ppm/°C
				–	±.0005	±.002		±.001	±.004	%FS/°C
V_{OC}	Output Voltage Compliance		D.N.L. Specification guaranteed over compliance range R_{OUT} > 10 megohms typ.	−5	–	+10	−5	–	+10	Volts
I_{FSS}	Full Scale Symmetry		$I_{FS} - \overline{I_{FS}}$	–	±0.2	±1.0	–	±0.4	±2.0	μA
I_{ZS}	Zero Scale Current			–	–	0.10	–	–	0.10	μA
t_S	Settling Time		To ±1/2 LSB, all bits ON or OFF, T_A = 25°C	–	250	500	–	250	500	nsec
t_{PLH} t_{PHL}	Propagation Delay – all bits		50% to 50%	–	25	50	–	25	50	nsec
C_{OUT}	Output Capacitance			–	20	–	–	20	–	pF
V_{IL}	Logic Input Levels	Logic "0"		–	–	0.8	–	–	0.8	Volts
V_{IH}		Logic "1"		2.0	–	–	2.0	–	–	
I_{IN}	Logic Input Current		V_{IN} = −5 to +18V	–	–	40	–	–	40	μA
V_{IS}	Logic Input Swing		V− = −15V	−5	–	+18	−5	–	+18	Volts
I_{REF}	Reference Current Range			0.2	1.0	1.1	0.2	1.0	1.1	mA
I_{15}	Reference Bias Current			0	−0.5	−2.0	0	−0.5	−2.0	μA
dI/dt	Reference Input Slew Rate		$R_{14(eq)}$ = 800Ω CC = 0pF	4.0	8.0	–	4.0	8.0	–	mA/μs
$PSSI_{FS+}$	Power Supply Sensitivity		V+ = +13.5V to +16.5V, V− = −15V	–	±.00005	±.001	–	±0.0005	±.001	%FS/%
$PSSI_{FS-}$			V− = −13.5V to −16.5V, V+ = +15V	–	±.00025	±.001	–	±.00025	±.001	
V+	Power Supply Range		V_{OUT} = 0V	4.5	–	18	4.5	–	18	Volts
V−				−18	–	−10.8	−18	–	−10.8	
I+	Power Supply Current		V+ = +5V, V− = −15V	–	5.7	8.5	–	5.7	8.5	mA
I−				–	−13.7	−18.0	–	−13.7	−18.0	
I+			V+ = +15V, V− = −15V		5.7	8.5	–	5.7	8.5	
I−				–	−13.7	−18.0	–	−13.7	−18.0	
P_D	Power Dissipation		V+ = +5V, V− = −15V	–	234	312	–	234	312	mW
			V+ = +15V, V− = −15V	–	291	397	–	291	397	

Advanced Micro Devices

LINEAR
Am6108

DISTINCTIVE CHARACTERISTICS

- 1μs conversion time
- Trimmed internal voltage reference
- 0,1% nonlinearity
- Ratiometric operation
- Low operating voltages
- Internal matched gain reference and offset resistors
- Microprocessor compatible
- 3-state outputs
- Pin-programmable unipolar or bipolar twos complement conversion
- Conversion complete available as interrupt or as multiplexed output on data bus

The International Standard of Quality guarantees these electrical AQLs on all parameters over the operating temperature range: 0.1% on MOS RAMs & ROMs; 0.2% on Bipolar Logic & Interface; 0.3% on Linear, LSI, Logic & other memories.

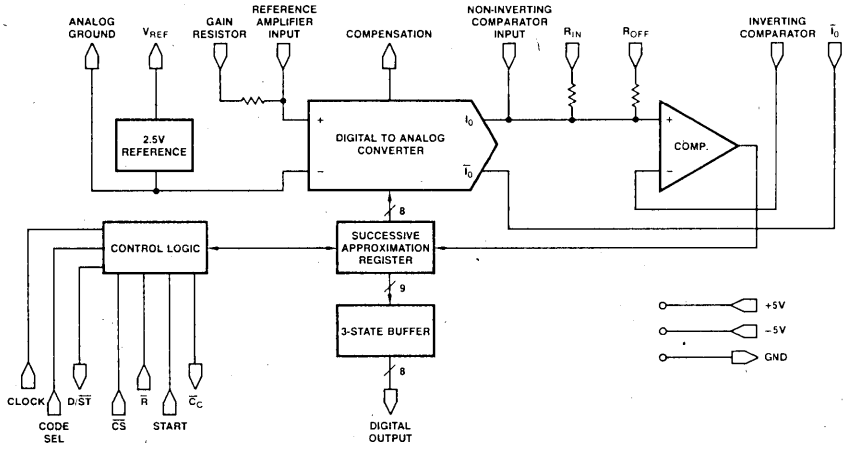
~~DESCRIPTION~~ Effective April 1, 1981

GENERAL DESCRIPTION

The Am6108 is a microprocessor compatible 8-bit high-speed analog-to-digital converter. The Am6108 is the first fully monolithic high-speed A/D to include a precision reference, DAC, comparator, SAR, scale resistors, output 3-state buffers and control logic. The Am6108 is capable of completing an 8-bit conversion in under one microsecond and can handle input voltage ranges of 0 to 10V, 0 to 5V, and ±5V without external components. With appropriate external resistors, the user can program the device to operate on other input signal ranges (2 or 3 precision resistors are required). Full 8-bit performance is guaranteed over temperature. The device has 3-state outputs for bus compatibility and two status outputs – one a standard TTL signal and the other available as a status output on the data bus.

The Am6108 is useful in microprocessor-based systems, or can be used in a stand-alone mode. The conversion time is short enough to allow most microprocessors to accept data immediately after requesting a conversion. Applications include Analog I/O subsystems and servomechanism control.

EQUIVALENT CIRCUIT

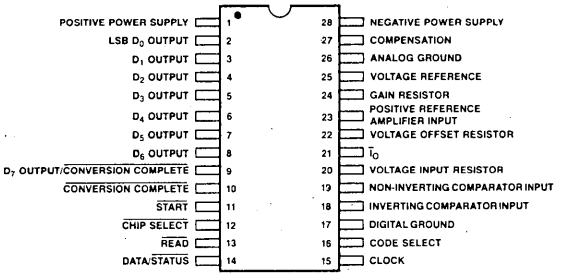


LIC-860

ORDERING INFORMATION

Order Number	Temperature Range
AM6108DM	−55 to +125°C
AM6108DC	0 to 70°C
AM6108PC	0 to 70°C
AM6108XM	Dice
AM6108XC	Dice

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LIC-861

LINEAR
Am6108

MAXIMUM RATINGS above which useful life may be impaired

V+ to D GND	−0.5 to +7.0V	Voltage at GAIN R, REF_{IN}	V− to V+
V− to D GND	+0.5 to −7.0V	Voltage at R_{IN}, R_{OFF}	−5 to +10V
Max Differential V+ to V−	±12V	DAC Compliance Voltage	−2 to +10V
Digital Inputs to D GND	−0.5 to +7.0V	Operating Temperature	−55 to +125°C
A GND to D GND	±1V	Storage Temperature	−65 to +150°C
V_{REF} Max Output Current	15mA	Lead Temperature (Soldering 60 sec)	300°C
Max Input Current at REF_{IN}	2mA		

ELECTRICAL CHARACTERISTICS ($V^+ = 5V, V^- = -5V$)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
Transfer Characteristic						
	Resolution		8	8	8	Bits
	Monotonicity		8	8	8	Bits
	Differential Non-Linearity	T_A = 25°C			±1/2	LSB
	Linearity	T_A = 25°C			±1/2	LSB
	Inherent Quantization Error				±1/2	LSB
	Unipolar Gain Error	T_A = 25°C		±3/4		LSB
	Unipolar Offset Error	T_A = 25°C		±1/2		LSB
	Bipolar Gain Error	T_A = 25°C		±1		LSB
	Bipolar Offset Error	T_A = 25°C		±3/4		LSB
	Positive Power Supply Sensitivity	V+ = 4.5 to 5.5V		.002		%FS/%
	Negative Power Supply Sensitivity	V− = 4.5 to −5.5V		.002		%FS/%
Drift						
	Monotonicity		8	8	8	Bits
	Differential Non-Linearity			±10		ppm/°C
	Linearity			±10		ppm/°C
	Unipolar Gain Error			±30		ppm/°C
	Unipolar Offset Error			±30		ppm/°C
	Bipolar Gain Error			±30		ppm/°C
	Bipolar Offset Error			±30		ppm/°C
Internal Reference						
V_{REF}	Reference Voltage		2.495	2.5	2.505	Volts
V_{REF}/T_A	Reference Voltage Tempco			25		ppm/°C
V_{REF}/I_{REF}	Load Regulation	I_{REF} = 1mA to 5mA		.05		%V_{REF}/mA
$V_{REF}/V+$	Line Regulation	V+ = 4.5 to 5.5V		.05		%V_{REF}/V
	Noise			20		μV
Analog Inputs						
	Input Impedance					
	±5V			2.5		KΩ
	0 to 10V			2.5		KΩ
	0 to 5V			1.25		KΩ
	Input Capacitance					
	R_{IN}, R_{OFF}			20		pF
	$\overline{I_O}$			20		pF
	COMP+			20		pF
	COMP−			2		pF
	GAIN R			2		pF
	REF_{IN}			2		pF

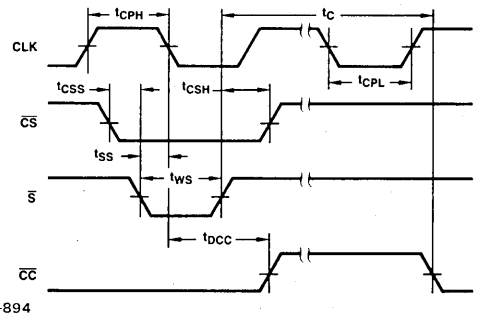
ELECTRICAL CHARACTERISTICS (Cont.)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
Digital Inputs						
	Logic Level Input Voltage					
V_{IH}	Logic 1		2.0			Volts
V_{IL}	Logic 0				08	Volts
	Logic Level Input Current					
I_{IH}	Logic 1			40		μA
I_{IL}	Logic 0			0.1		μA
Digital Outputs						
	Logic Level Output Voltages					
V_{OH}	Logic 1	I_{OH} = −400μA	2.4			Volts
V_{OL}	Logic 0	I_{OL} = 8mA			.5	Volts
I_{SC}	Output Short Circuit Current	V+ = 5.5V			−20	mA
I_{OZ}	Off-State Output Current	V+ = 5.5V				
		V_O = 2.4V		20		μA
		V_O = 0.4V		−20		μA
Power Requirements						
V+	Positive Supply			44	82	mA
V−	Negative Supply			−65	−100	mA
	Power Dissipation			600	1000	mW

SYSTEM TIMING

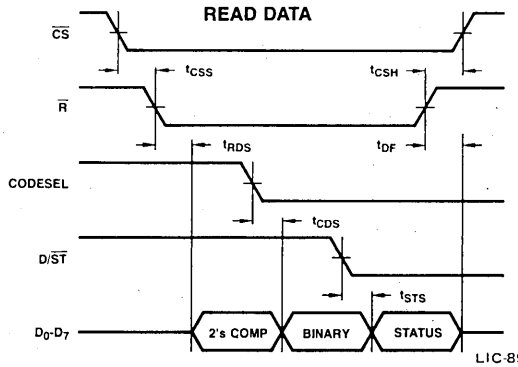
Parameters	Description	Min	Typ	Max	Units
t_C	Conversion Time		1		μs
t_{CSS}	$\overline{CS}$ Low Set-up Time	0			ns
t_{SS}	$\overline{S}$ Low to CLK Low Set-up Time	0			ns
t_{WS}	$\overline{S}$ Pulse Width	20			ns
t_{CSH}	$\overline{CS}$ Low Hold Time	0			ns
t_{DCC}	CLK Low to $\overline{CC}$ High Delay		10		ns
t_{DRS}	$\overline{R}$ Low to Data Stable		30		ns
t_{CDS}	CODESEL to Data Stable		20		ns
t_{STS}	D/$\overline{ST}$ to Data Stable		20		ns
t_{DF}	Data Float After Read		50		ns
t_{CPL}	CLK Low Period	50			ns
t_{CPH}	CLK High Period	50			ns
f_C	Clock Frequency			10	MHz

START CONVERSION



LIC-894

READ DATA



LIC-895

Advanced Micro Devices

LINEAR
Am6112
PRELIMINARY DATA

Am6112
3μs Microprocessor Compatible
12-Bit A/D Converter

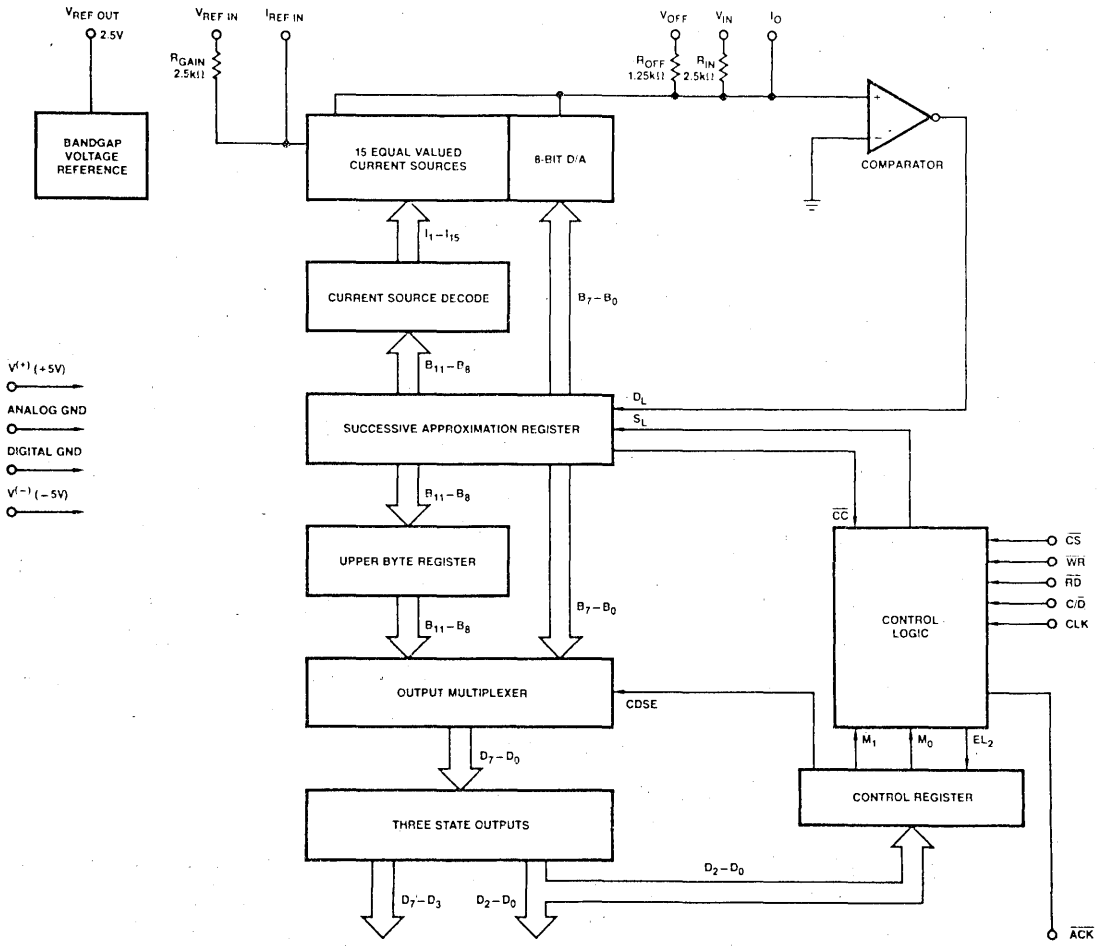
- First totally monolithic, high-speed 12-bit ADC
- 3μs typical conversion time
- Internal precision voltage reference
- Guaranteed monotonicity with no missing codes over full operating temperature range
- Easy interfacing with 8- and 16-bit μP's
- Internal command register for programmable modes of operation
- Offset binary or 2's complement output code
- 0 to 10V, 0 to 5V or ±5V input range
- 24-pin package

FUNCTIONAL DESCRIPTION

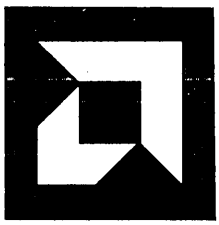
The Am6112 is the first fully monolithic microprocessor compatible 12-bit high-speed analog-to-digital converter. The Am6112 high-speed A/D contains a precision reference, DAC, comparator, SAR, scale resistors, output three-state buffers and comprehensive control logic, enabling the device to be interfaced with a variety of microprocessors. The Am6112 is capable of completing a 12-bit conversion in under three microseconds and can handle input voltage ranges of 0 to 10V, 0 to 5V, and ±5V without external components.

The Am6112 has four modes of operation, two microprocessor, one DMA, and a stand-alone mode. These modes are software programmable, except for the stand-alone mode which is pin selectable. Applications include analog I/O subsystems, servo-control and high-speed digital signal processing of analog events.

BLOCK DIAGRAM



ABI-008



LINEAR
Am6112

ELECTRICAL CHARACTERISTICS ($V+ = 5V, V- = -5V$)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
Transfer Characteristic						
	Resolution		12	12	12	Bits
	Monotonicity	(Guaranteed Over Full Operating Temperature Range)				
	Differential Non-Linearity	$T_A = 25°C$		±1/2	1	LSB
	Linearity	$T_A = 25°C$		±1/2		LSB
	Inherent Quantitization Error	$T_A = 25°C$			±1/2	LSB
	Unipolar Gain Error	$T_A = 25°C$		±1/2		LSB
	Unipolar Offset Error	$T_A = 25°C$		±1/2		LSB
	Bipolar Gain Error	$T_A = 25°C$		±3		LSB
	Bipolar Offset Error	$T_A = 25°C$		±2		LSB
	Positive Power Supply Sensitivity	$V+ = 4.5$ to $5.5V$		0.001		%/V
	Negative Power Supply Sensitivity	$V- = -4.5$ to $-5.5V$		0.001		%/V
Drift (−55 to +125°C)						
	Differential Non-Linearity			±0.5		ppm/°C
	Linearity			±0.5		ppm/°C
	Unipolar Gain Error			±2		ppm/°C
	Unipolar Offset Error			±1		ppm/°C
	Bipolar Gain Error			±4		ppm/°C
	Bipolar Offset Error			±1		ppm/°C
Internal Reference						
V_{REF}	Reference Voltage		2.4975	2.5	2.5025	Volts
V_{REF}/T_A	Reference Voltage Tempco	$T_A = -55$ to $+125°C$		+8		ppm/°C
V_{REF}/I_{REF}	Load Regulation	$I_{REF} = 1mA$ to $5mA$		0.005		$\%V_{REF}/mA$
$V_{REF}/V+$	Line Regulation	$V+ = 4.5$ to $5.5V$ $V- = -4.5$ to $-5.5V$		0.005		$\%V_{REF}/mA$
	Noise			20		μV
Digital Inputs						
	Logic Level Input Voltage					
V_{IH}	Logic 1		2.0			Volts
V_{IL}	Logic 0				.8	Volts
	Logic Level Input Current					
I_{IH}	Logic 1			40		μA
I_{IL}	Logic 0			0.1		μA
Digital Outputs						
	Logic Level Output Voltages					
V_{OH}	Logic 1	$I_{OH} = -400\mu A$	2.4			Volts
V_{OL}	Logic 0	$I_{OL} = 8mA$			.5	Volts
I_{SC}	Output Short Circuit Current	$V+ = 5.5V$			−20	mA
I_{OZ}	Off-State Output Current	$V+ = 5.5V$				
		$V_O = 2.4V$		20		μA
		$V_O = 0.4V$		−20		μA
Clock Frequency						
f_C				4		MHz
Conversion Time						
t_C				3.3		μs
Power Requirements						
V+	Positive Supply	$T_A = 25°C$		50		mA
V−	Negative Supply			−70		mA
	Device Power Dissipation			600		mW

LINEAR
Am6112

STATUS TRUTH TABLE

Control Logic Inputs				Am6112 Status
$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	C/$\overline{D}$	
1	X	X	X	Output Data Lines (D_7-D_0) in High Impedance State
0	0	0	X	Forced to Mode 3 Operation
0	1	0	1	Write into Command Register to Select Mode of Operation
0	0	1	0	Read 8 LSB's (Low Byte)
0	0	1	1	Read 4 MSB's and Sign Bit (High Byte)

COMMAND REGISTER BITS

D_2 D_1 — Mode Select

D_0: 1 = 2's complement output code. 0 = offset binary output code.

Mode Select

- 0 0 = Mode 0 – Am6112 under μP control. Conversion cycle started by active $\overline{WR}$.
- 0 1 = Mode 1 – Am6112 under μP control. Conversion cycle started by active $\overline{RD}$.
- 1 0 = Mode 2 – Am6112 under DMA control (such as Am9517A). Conversion cycle started by active $\overline{RD}$. Data outputted as 8 LSB's and 4 MSB's. Output data control is done internally and not accessible by the user.
- 1 1 = Mode 3 – Stand-alone operation.

Am6112 FUNCTIONAL PIN DESCRIPTION

$V_{REF}OUT$ 2.5V internal voltage reference output.

$V_{REF}IN$ Connected to an external voltage reference ($V_{REF}OUT$) to establish a reference current for the DAC bit currents.

$I_{REF}IN$ External reference current input for ratiometric operation.

I_0 DAC current output.

V_{IN} Analog voltage input.

R_{OFF} When connected to $V_{REF}OUT$, 1/2 scale offset is generated to accommodate bipolar analog input signals.

D_0-D_7 Three-state data lines. D_0-D_2 are bidirectional data lines, while D_3-D_7 are strictly output data lines. Data is loaded into the internal COMMAND register via D_0-D_2 to select one of four modes of operation. D_0-D_3 are also used to output the 4 MSBs (B_8-B_{11}) of the 12-bit data. D_4-D_7 also output the sign bit (B_{11}).

$\overline{WR}$ Active low input used to reset the SAR and start a conversion cycle (MODE 0 operation). This input line is also used to load data into the command register along with C/$\overline{D}$ line held high.

$\overline{RD}$ Active low input used to read the SAR data. SAR data is read in two bytes. The reading of the high byte (B_8-B_{11}) or low byte is user selectable except during Mode 2 via the C/$\overline{D}$ line (see Status Truth Table).

C/$\overline{D}$ Used in loading the COMMAND register with an active $\overline{WR}$ or outputting the HIGH and LOW data bytes with an active $\overline{RD}$ (see Status Truth Table).

$\overline{CS}$ Active low input allows the Am6112 to be involved in I/O operations (see Status Truth Table).

$\overline{ACK}$ Open collector, active low output indicating the status of the Am6112.

CLK Clock input synchronizing and controlling the operation of the Am6112.

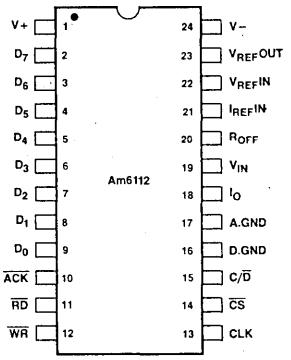
V+ +5V power supply input.

V– –5V power supply input.

AGND Analog ground.

DGND Digital ground.

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

ABI-009

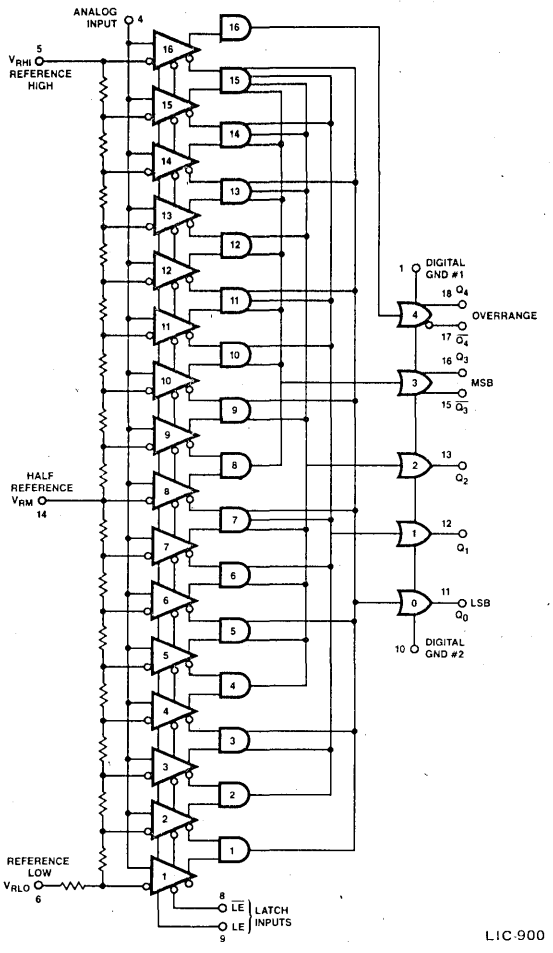
Advanced Micro Devices

LINEAR
Am6688

Distinctive Characteristics:

- 100MHz sampling rate
- 5ns maximum encode delay
- 4-bit resolution, expansible to 8 bits
- 8-bit accuracy
- Large bipolar input voltage range
- Low input current
- Q and $\overline{Q}$ Outputs on MSB for 2's complement conversion
- 100% MIL-STD-883 reliability assurance testing

FUNCTIONAL DIAGRAM



LIC-900

The International Standard of Quality guarantees these electrical AQLs on all parameters over the operating temperature range: 0.1% on MOS RAMs & ROMs; 0.2% on Bipolar Logic & Interface; 0.3% on Linear, LSI, CMOS Logic & other memories.

FUNCTIONAL DESCRIPTION

The Am6688 4-bit quantizer consists of an array of 16 high-speed ECL sampling comparators, a resistor voltage divider, and an ECL-compatible binary encoder. It will accurately quantize an analog voltage into 15 equally-spaced levels and output a 4-bit binary digital word at sampling rates up to 100 MHz.

Resolution above 4-bits, up to a maximum of 8, may be obtained by stacking quantizers (n bits of resolution requires 2^{n-4} quantizers). An overrange output signal is provided to indicate that the input signal has exceeded the full-scale limit. This overrange output is also the enable gating signal used to encode the higher-order bits of the output in a stacked configuration.

The high speed latch enable inputs are intended to be driven from the complementary outputs of a standard ECL gate or a high-speed comparator such as the Am685. If LE is driven high and $\overline{LE}$ is driven low, the quantizer is in the sample mode and operates like a low-gain, high-bandwidth amplifier. When LE is driven low and LE is driven high, the quantizer will hold its existing digital binary output word.

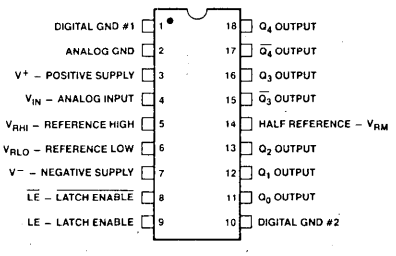
The outputs are open emitters, requiring external pull-down resistors of at least 200Ω to −2V or 500Ω to −5.2V.

These devices can be used in video data conversion and time-base correction, radar signal processing, nuclear pulse-height analysis, and other systems requiring very high-speed analog-to-digital conversion.

ORDERING INFORMATION

Order Number	Temperature Range	Maximum Error
Am6688DL-8	−30 to +85°C	±5mV
Am6688DL-7	−30 to +85°C	±10mV
Am6688DL-6	−30 to +85°C	±20mV
Am6688DM-8	−55 to +125°C	±5mV
Am6688DM-7	−55 to +125°C	±10mV
Am6688DM-6	−55 to +125°C	±20mV

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LIC-901

LINEAR
Am6688

MAXIMUM RATINGS (Above which the useful life may be impaired)

Supply Voltage:	Positive	+7V
	Negative	−6V
Input Voltage:	Analog	−5V to +3V
	References	−5V to +3V
	Digital	−5V to 0V
Differential Voltage:	Analog Input to References	±6V
	Analog Gnd to Digital Gnds	±0.1V

Output Current (each output)		15mA
Temperature:	Operating, Am6688DL	−30 to +85°C
	Am6688DM	−55 to +125°C
	Storage	−65 to +150°C
	Junction	+175°C
	Lead (soldering, 60sec)	+300°C
Minimum Operating Voltage (V^+ to V^-)		10V

ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE RANGES
(Unless otherwise specified)

DC Characteristics

Symbol	Parameter (see definitions)	Conditions (Note 1)	Am6688DL Min	Am6688DL Max	Am6688DM Min	Am6688DM Max	Units
	Resolution		4		4		Bits
V_{OS}	Error Voltage (each transition)	Am6688 − 8	−5	+5	−5	+5	mV
		− 7	−10	+10	−10	+10	mV
		− 6	−20	+20	−20	+20	mV
DNL	Differential Nonlinearity	$\Delta V_{REF} = \Delta V_{REF(min)}$	−0.5	0.5	−0.5	0.5	LSB
V_{IN}	Input Voltage		−3.3	+2.7	−3.3	+2.7	V
ΔV_{REF}	Reference Resistor Voltage ($V_{RHI} - V_{RLO}$)	Am6688 − 8	0.16	6.0	0.16	6.0	V
		− 7	0.32	6.0	0.32	6.0	V
		− 6	0.64	6.0	0.64	6.0	V
I_{REF}	Reference Current	$\Delta V_{REF} = 2.56V$	6.0	17	5.0	18	mA
I_B	Analog Input Current	$V_{IN} \geq V_{RHI}$		230		250	μA
I_L	Latch Input Current	$V_L \geq V_{OH}$		200		220	μA
V_{OH}	Output HIGH Voltage	$T_A = 25°C$	−0.93	−0.72	−0.93	−0.72	V
		$T_A = T_{A(min)}$	−1.03	−0.80	−1.08	−0.83	V
		$T_A = T_{A(max)}$	−0.86	−0.64	−0.83	−0.58	V
V_{OL}	Output LOW Voltage	$T_A = 25°C$	−1.90	−1.62	−1.90	−1.62	V
		$T_A = T_{A(min)}$	−1.93	−1.65	−1.95	−1.66	V
		$T_A = T_{A(max)}$	−1.86	−1.58	−1.84	−1.54	V
I^+	Positive Supply Current			100		100	mA
I^-	Negative Supply Current			100		100	mA
P_{DISS}	Power Dissipation	$\Delta V_{REF} = 2.56V$		1.2		1.2	W

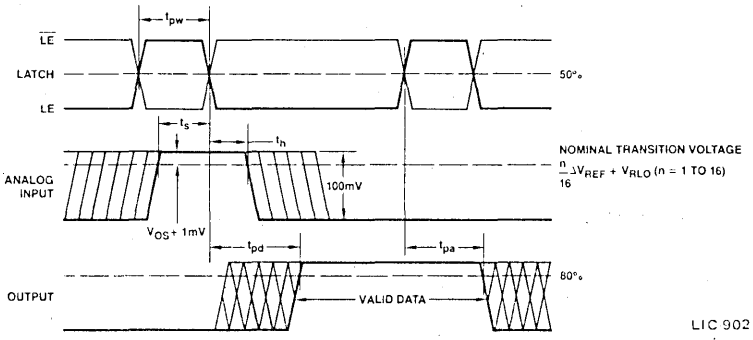
Switching Characteristics (Note 2)

F_{MAX}	Maximum Sampling Frequency		100		100		MHz
t_{pw}	Minimum Sample Time			3		3	ns
t_{pd}	Encode Delay (each transition)	$T_{A(min)} \leq T_A \leq 25°C$		5		5	ns
		$T_A = T_{A(max)}$		6		8	ns
t_s	Minimum Set-up Time	$T_A = 25°C$		3		3	ns
t_h	Minimum Hold Time	$T_A = 25°C$		1		1	ns
t_{pa}	Analog Delay (each transition)	$T_{A(min)} \leq T_A \leq 25°C$	3		3		ns
		$T_A = T_{A(max)}$	4		4		ns

Notes: 1. Unless otherwise specified, $V^+ = +6.0V$, $V^- = -5.2V$, $V_{RHI} = +2.56V$, $V_{RM} = +1.28V$, $V_{RLO} = 0V$, $t_{pw} = 5ns$, and $R_L = 100\Omega$ to $-2V$ at all outputs. The specifications given for V_{OS}, DNL, and t_{pd} apply over the full V_{IN} range and for ±5% supply voltages. The Am6688 is designed to meet the specifications given in the table after thermal equilibrium has been established with a transverse air flow of 500 LFPM or greater.

2. Switching characteristics are for a 100mV analog input pulse level-shifted at each transition point to provide an overdrive of 1mV past the maximum specified error voltage.

TIMING DIAGRAM



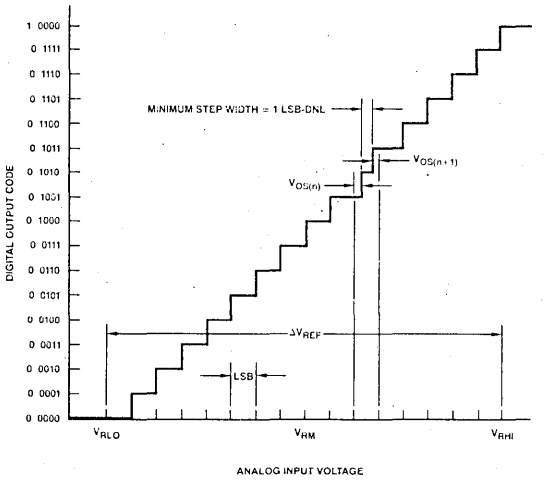
LIC 902

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN

During the sampling time, the quantizer acts like a low-gain, very wide-bandwidth linear amplifier. The gain is not high enough to hold the outputs in a stable logic state under all conditions; consequently, the outputs may be undefined during this period. The time that the outputs are unstable begins t_{pa} after the Latch Enable goes HIGH, and terminates t_{pd} after it goes LOW. It is best to minimize this time by using as narrow a sampling pulse as possible, since the possibility of oscillation due to external parasitic feedback is greater the longer the device is in the analog mode.

TYPICAL TRANSFER FUNCTION



LIC 903

TRUTH TABLE

Analog Input (relative to V_{RLO})	Q_4	Q_3	Q_2	Q_1	Q_0
$V_{IN} < \frac{1}{16}\Delta V_{REF}$	L	L	L	L	L
$\frac{1}{16}\Delta V_{REF} < V_{IN} < \frac{1}{8}\Delta V_{REF}$	L	L	L	L	H
$\frac{1}{8}\Delta V_{REF} < V_{IN} < \frac{3}{16}\Delta V_{REF}$	L	L	L	H	L
$\frac{3}{16}\Delta V_{REF} < V_{IN} < \frac{1}{4}\Delta V_{REF}$	L	L	L	H	H
$\frac{1}{4}\Delta V_{REF} < V_{IN} < \frac{5}{16}\Delta V_{REF}$	L	L	H	L	L
$\frac{5}{16}\Delta V_{REF} < V_{IN} < \frac{3}{8}\Delta V_{REF}$	L	L	H	L	H
$\frac{3}{8}\Delta V_{REF} < V_{IN} < \frac{7}{16}\Delta V_{REF}$	L	L	H	H	L
$\frac{7}{16}\Delta V_{REF} < V_{IN} \frac{1}{2}\Delta V_{REF}$	L	L	H	H	H
$\frac{1}{2}\Delta V_{REF} < V_{IN} < \frac{9}{16}\Delta V_{REF}$	L	H	L	L	L
$\frac{9}{16}\Delta V_{REF} < V_{IN} < \frac{5}{8}\Delta V_{REF}$	L	H	L	L	H
$\frac{5}{8}\Delta V_{REF} < V_{IN} < \frac{11}{16}\Delta V_{REF}$	L	H	L	H	L
$\frac{11}{16}\Delta V_{REF} < V_{IN} < \frac{3}{4}\Delta V_{REF}$	L	H	L	H	H
$\frac{3}{4}\Delta V_{REF} < V_{IN} < \frac{13}{16}\Delta V_{REF}$	L	H	H	L	L
$\frac{13}{16}\Delta V_{REF} < V_{IN} < \frac{7}{8}\Delta V_{REF}$	L	H	H	L	H
$\frac{7}{8}\Delta V_{REF} < V_{IN} < \frac{15}{16}\Delta V_{REF}$	L	H	H	H	L
$\frac{15}{16}\Delta V_{REF} < V_{IN} < \Delta V_{REF}$	L	H	H	H	H
$V_{IN} > \Delta V_{REF}$	H	L	L	L	L

LINEAR
Am6300

DISTINCTIVE CHARACTERISTICS

- 2.5V ±0.25% temperature compensated reference
- Versatile 100mA output for driving external NPN or PNP power transistors
- Thermal shutdown
- Logic control power up enable
- Programmable delay and rise time for power supply
- ±5% or ±10% over/under voltage detection/protection
- Programmable current limit detection/protection
- Programmable delays for the over/under voltage and current shutdown circuits
- Status outputs for fault conditions and output state

GENERAL DESCRIPTION

The Am6300 Power Control Subsystem consists of a regulator section, an over/under voltage detection section, a current limit section and a reset and control section.

The regulator section contains a complete series pass voltage regulator with thermal shutdown, which uses external resistors to set the output voltage. Both the collector and emitter of the regulator output transistor are available to the user for flexibility in driving external power devices. The regulator also contains a precision, trimmed 2.5 volt reference which is capable of supplying 5mA of current for external purposes in addition to controlling the regulator and generating over and under voltage references.

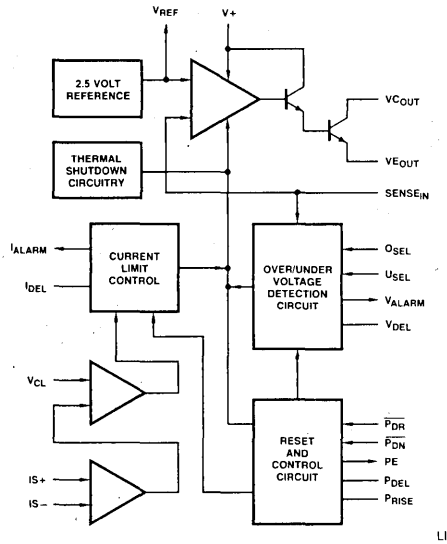
The over/under voltage section compares the voltage at the sense input of the regulator to the internal reference and determines if the difference exceeds the user programmed limits, ±5% or ±10%. If one of the limits is exceeded for a period longer than the user programmed delay, the regulator shuts down and the voltage alarm output is activated. The regulator is reset by activating the power down inputs or removing power from the device.

The current limit section detects overload current by means of an external sense resistor in series with V_{IN}, GND, or the output of the regulator. The user programs the threshold of this detection circuit with external resistors. The regulator shuts down if a current overload is detected for a period longer than a user programmed delay and the current alarm is activated. The regulator is reset by activating the power down inputs or removing power from the device.

The reset and control section provides to the user, the ability to turn the regulator on and off by logic control. The start up of the regulator is delayed by a user programmed interval after the power up signal is received. After this delay the regulator output ramps up at a rate which is also determined by the user. When the output voltage levels off at the preset value, the over/under voltage and current limit circuits are activated and a power up output is activated which can be used to signal to the user that the supply is operating or enable other circuits.

The Am6300 allows the user a great deal of flexibility in power supply configuration and control. It can be operated locally or remotely in a stand alone configuration or with external power transistors to increase the output current. The Am6300 can be cascaded with other Am6300s for a sequenced supply application.

BLOCK DIAGRAM

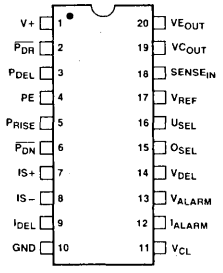


LIC-885

ORDERING INFORMATION

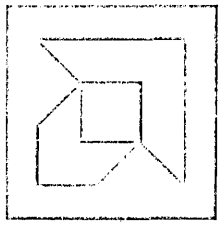
Package Type	Temperature Range	Order Number
Hermetic DIP	−55 to +125°C	AM6300DM
Hermetic DIP	0 to 70°C	AM6300DC
Plastic DIP	0 to 70°C	AM6300PC

CONNECTION DIAGRAM
Top View



Pin 1 is marked for orientation.

LIC-886



LINEAR
Am6300

MAXIMUM RATINGS

Pulse Voltage at V+ (50ms)	50V	Input Voltage (all pins)	Gnd to V+
Continuous Voltage at V+	40V	Maximum Output Current	100mA
Input-Output Voltage Differential	37.5V	Internal Power Dissipation	1000mW (Note 1)

ELECTRICAL CHARACTERISTICS (Note 2)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
Voltage Regulator						
	Output Error (Note 3)		−1.0		+1.0	$\%V_{OUT}$
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation, T_A = 25°C	V_{IN} = 12 to 40V	.02	.2		$\%V_{OUT}$
$\Delta V_{OUT}/\Delta I_L$	Load Regulation, T_A = 25°C	I_L = 1mA to 50mA	.03	.15		$\%V_{OUT}$
	Ripple Rejection	f = 1kHz T_A = 25°C	74	86		dB
I_{BIAS}	Sense Input Bias Current			2	4	μA
V_{IN}	Input Operating Range		5		40	Volts
V_{OUT}	Output Operating Range		2.5		37.5	Volts
V_{IN}-V_{OUT}	Input-Output Differential		2.5		37.5	Volts
I_S	Supply Current			5	10	mA
Voltage Reference						
V_{REF}	Reference Voltage	T_A = 25°C	2.494	2.5	2.506	Volts
$\Delta V_{REF}/\Delta V_{IN}$	Line Regulation	V_{IN} = 12 to 40V				$\%V_{REF}$
$\Delta V_{REF}/\Delta I_{REF}$	Load Regulation	I_{REF} = 1mA to 5mA		.15	.30	$\%V_{REF}$
$\Delta V_{REF}/\Delta T_A$	Temperature Stability	0 to 70°C −55 to 125°C				ppm/°C
I_{SC}	Short Circuit Current	V_{REF} = 0V	10	30	60	mA
Current Overload Circuit						
V_{IS} (diff)/V_{CL}	Trip Point Ratio		.45	.5	.55	V/V
V_{CL}	Trip Point Input Range		0		.4	Volts
V_{IS} (diff)	Sense Voltage Input Range		0		.2	Volts
CMVR	Sense Input Common Mode Range		0		V_{IN}	Volts
I_{BIAS}	Input Bias Current (IS+, IS−)	V_{IS} = 0V to +2V V_{IS} = +2V to V_{IN}		−8 +8	−20 +20	μA
I_{OS}	Input Offset Current (IS+, IS−)			±1	±5	μA
I_{BIAS}	Input Bias Current (V_{CL})			−.25	−1.0	μA
Voltage Protection Circuit						
	+5% Error Trip Point	O_{SEL} = 5V	4.5	5	5.5	$\%V_{OUT}$
	−5% Error Trip Point	U_{SEL} = 5V	−4.5	−5	−5.5	$\%V_{OUT}$
	+10% Error Trip Point	O_{SEL} = 0V	9	10	11	$\%V_{OUT}$
	−10% Error Trip Point	U_{SEL} = 0V	−9	−10	−11	$\%V_{OUT}$
Digital Characteristics (Note 4)						
V_{IH}	Input High Level		2.0		V_{IN}	Volts
V_{IL}	Input Low Level		0		.8	Volts
V_{OL}	Open Collector Output Voltage	I_{OL} = 8mA I_{OL} = 15mA			.4 1.5	Volts

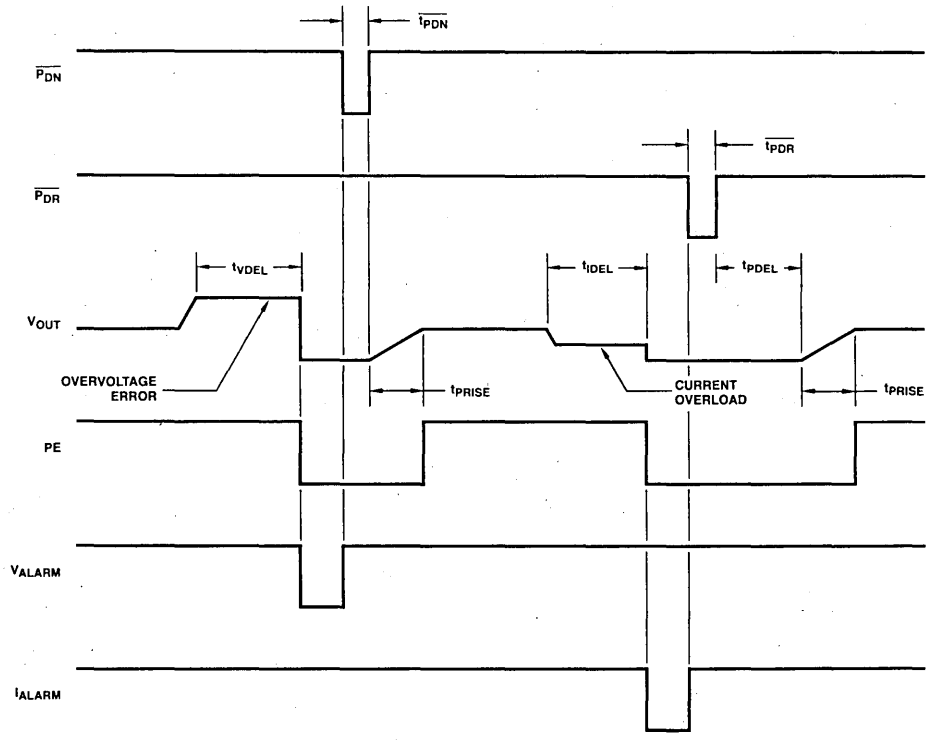
Notes: 1. Power dissipation ratings apply for T_A = 25°C. Derate linearly at 8mW/°C above 25°C for commercial parts and above 50°C for military parts.
2. All specifications are for V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 1mA, I_{REF} = 1mA and over the operating temperature range unless otherwise specified.
3. Includes all errors associated with on chip reference source and temperature effects.
4. Digital Inputs are $\overline{PDN}$, $\overline{PDR}$, OSEL, USEL
Digital Outputs are V_{ALARM}, I_{ALARM}, PE

TIMING CHARACTERISTICS

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{IDEL}, t_{VDEL}	Current Overload and Voltage Error Power Down Delays	Without external cap		1.2		μs
		With external cap, additional delay		.22		μs/pF
t_{PDEL}	Power Up Delay (Note 5)	Without external cap		1.2		μs
		With external cap, additional delay		.22		μs/pF
t_{PRISE}	Power Up Rise Time (Note 5)	Without external cap		1.5		μs
		With external cap		.22		μs/pF
t_{PDN}, t_{PDR}	Power Down Reset Pulse Width		10			μs

Note 5: It is necessary to make the total time t_{PDEL} + t_{PRISE} greater than the rise time of the supply to the Am6300 to insure proper power up.

TIMING WAVEFORMS



LIC-887

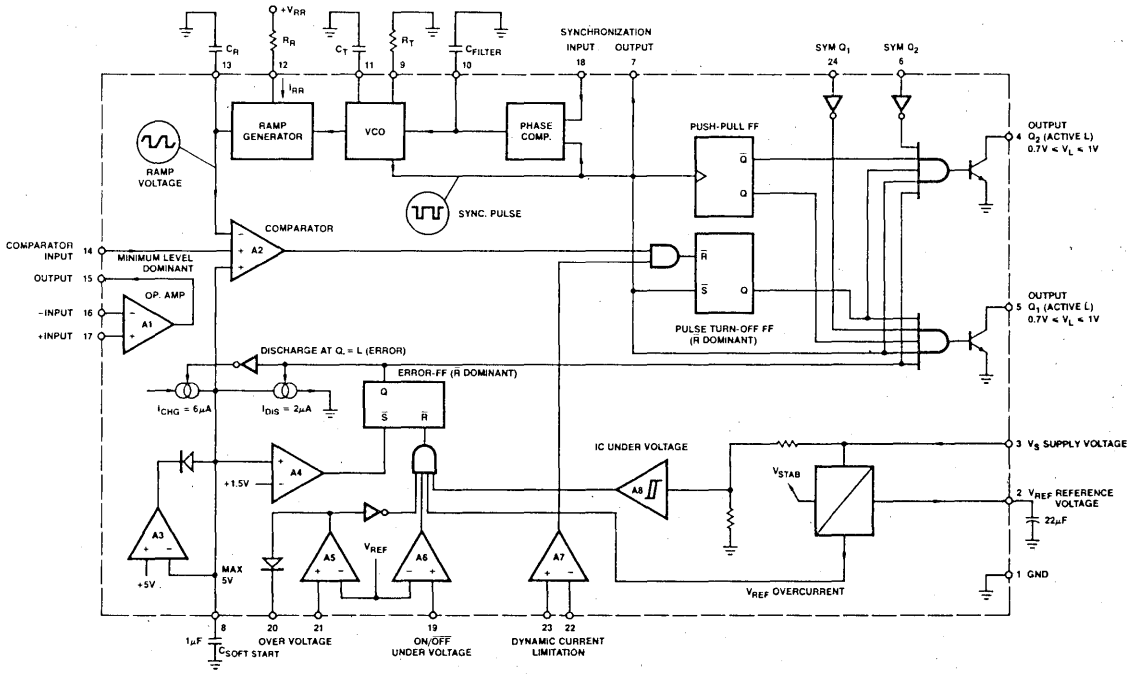
Am6301
Switching Power Supply Controller

- Feed-forward (line hum suppression)
- Output over/under voltage protection
- Input under voltage protection
- Cycle-by-cycle current limiting
- Soft start
- 250kHz max. oscillator frequency
- Phase lock capability
- 96% max. duty cycle
- Double pulse suppression
- Symmetry inputs for push-pull converter
- Remote shutdown
- Pin equivalent to the Siemens' TDA 4700

GENERAL DESCRIPTION

The Am6301 Switching Power Supply Controller contains all the digital and analog functions necessary to control blocking, single-ended, or push-pull switching power supplies. It contains the voltage controlled oscillator, ramp generator, comparator, and reference for basic switched mode power supplies, as well as, a full complement of interface circuits and circuitry to protect both the power supply and its load.

BLOCK DIAGRAM



ABI-020

LINEAR
Am6301

MAXIMUM RATINGS (Above which useful life may be impaired)

Supply Voltage V_S	33V	Voltage at Q_1, Q_2	33V
Input Voltage (all inputs)	Gnd to V_S	Current at Q_1, Q_2	70mA
Output Voltage A5	33V	Input Current R_{ramp}	1mA
Output Voltage A1	6.5V		

ELECTRICAL CHARACTERISTICS
(V_S = 12V, T_A = 25°C, f_{VCO} = 15kHz)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
Regulator						
V_S	Supply Voltage		11		30	Volts
I_S	Supply Current			12		mA
f_{VCO}	Operating Frequency Range		40		250k	Hz
Reference						
V_{REF}	Reference Voltage		2.35	2.5	2.65	Volts
$\Delta V_{REF}/\Delta V_S$	Line Regulation	V_S = 25V ± 20%		15		mV
$\Delta V_{REF}/\Delta I_{REF}$	Load Regulation	I_{REF} = 0 to 5mA		3		mV
$\Delta V_{REF}/\Delta T_A$	Temperature Stability				100	ppm/°C
Oscillator						
f_{VCO}	Operating Frequency Range		40		250k	Hz
$\Delta f/f$	Initial Tolerance	ΔC_T = 0%, ΔR_T = 0%			±7	%
$\Delta f/\Delta T_A$	Temperature Stability	T_A = 0 to 70°C			300	ppm/°C
$\Delta f/\Delta V_S$	Frequency Stability	V_S = 25V ± 20%			1	%
t_{VCO}	Fall Time	C_T = 1nF		1		μs
Ramp Generator						
f_{ramp}	Frequency Range		40		250k	Hz
V_{ramp} Hi	Voltage at C_{ramp} High			5.5		Volts
V_{ramp} Low	Voltage at C_{ramp} Low			1.8		Volts
I_{ramp}	Input Current at R_{ramp}		10		400	μA
Synchronization						
V_{IH}	Synchronization Input		2			Volts
V_{IL}					0.8	Volts
V_{OH}	Synchronization Output	I_{OH} = 200μA	4			Volts
V_{OL}		I_{OL} = 1.6mA			0.4	Volts
Comparator A2						
I_B	Input Bias Current			−1		μA
t_{A2}	Turn-Off Delay				500	ns
V_{IN}	Input Voltage for Duty Cycle	T_{On}/T_{Off} = 0%			1.8	Volts
		T_{On}/T_{Off} = 48%	5			
Soft Start						
I_{CHG}	Charging Current			6		μA
I_{DIS}	Discharging Current			2		μA
V_{LIM}	Upper Limiting Voltage			5		Volts
V_{TH}	Reset Voltage			1.5		Volts

ELECTRICAL CHARACTERISTICS (Cont.)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
Operational Amplifier						
A_{OL}	Open Loop Gain		60	80		dB
V_{OS}	Input Offset Voltage				20	mV
$\Delta V_{OS}/\Delta T_A$	V_{OS} Tempco				100	$\mu V/^\circ C$
I_B	Input Bias Current			−0.5		μA
V_{CM}	Common Mode Range		0		5	Volts
I_O	Output Current			±2		mA
$\Delta V/\Delta t$	Output Slew Rate			1		$V/\mu s$
BW	3dB Bandwidth			3		MHz
ϕ_t	Phase Shift at 3MHz			120		degrees
Symmetry						
V_{IH}	Input Voltage		2			Volts
V_{IL}					0.8	Volts
I_{IL}	Input Low Current			−1		μA
Output States Q_1, Q_2						
V_{OL}	Output Voltage	I_O = 25mA			1	Volts
I_{OH}	Output Current	V_{OH} = 30V			2	μA
ON/$\overline{\text{OFF}}$, Under Voltage						
V_{TH}	Threshold Voltage			V_{REF}		Volts
I_B	Input Bias Current			−1		μA
t_{OFF}	Turn-Off Delay			250		ns
t_{ERR}	Error Recognition Time			50		ns
Dynamic Current Limiting						
V_{CM}	Common Mode Range		0		4	Volts
V_{OS}	Input Offset Voltage				20	mV
I_B	Input Bias Current			−1		μA
t_{OFF}	Turn-Off Delay			250		ns
t_{ERR}	Error Recognition Time			50		ns
Over Voltage						
V_{TH}	Threshold Voltage			V_{REF}		Volts
I_B	Input Bias Current			−1		μA
I_{OH}	Output Current	V_{OH} = 5V			−200	μA
t_{OFF}	Turn-Off Delay			250		ns
t_{ERR}	Error Recognition Time			50		ns
Supply Under Voltage						
V_{ON}	Turn-On Threshold, V_S Rising			9.6		Volts
V_{OFF}	Turn-Off Threshold, V_S Falling			9		Volts

Am6301 FUNCTIONAL DESCRIPTION

VOLTAGE-CONTROLLED OSCILLATOR (VCO)

The VCO (voltage-controlled oscillator) generates a sawtooth voltage at C_T. The duration of the falling edge is determined by the selection of C_T. The duration of the rising edge and thus the oscillator frequency is determined by R_T and C_T. Maximum oscillator frequency is 250kHz. The oscillator frequency can be varied for frequency synchronization purposes by varying the voltage at C_{filter}. The falling edge of the VCO generates the synchronization pulse and triggers the ramp generator and other parts of the Am6301.

RAMP GENERATOR – FEED-FORWARD CONTROL

The ramp generator is triggered by the synchronization pulse of the VCO and oscillates at the same frequency. The duration of the falling edge of the ramp generator must be shorter than the fall time of the VCO. The voltage of the rising edge of the ramp generator and a DC voltage at comparator A2 are compared for pulse width control of the output. The slope of the rising edge is adjusted via the current through R_R. This enables an additional superimposed control of the duty cycle dependent on the input voltage of the Switched Mode Power Supplies (SMPS). This capability (feed-forward) allows for compensation of a known interference (e.g. line hum).

PHASE COMPARATOR – SYNCHRONIZATION

If the Am6301 is operated without external synchronization, the synchronization input must be connected to the synchronization output, so that the phase comparator sets the voltage at C_{filter}. The VCO then oscillates at the frequency set by R_T and C_T. Other circuits can be synchronized with the synchronization output. The Am6301 can be synchronized to an external signal of any duty cycle. The synchronization input and output are TTL compatible.

PUSH-PULL FLIP-FLOP

The push-pull flip-flop is toggled by the falling edge of the VCO. This guarantees that only one of the two push-pull outputs can be enabled at any one time.

COMPARATOR A2 – PULSE WIDTH MODULATION

The two noninverting inputs of the comparator are switched in such a manner that the lowest level is always compared with the inverting input. As soon as the voltage of the rising sawtooth at C_R exceeds the lower of the two levels, both outputs are disabled via the pulse turn-off flip-flop.

REGULATING AMPLIFIER A1

A1 is a high-quality regulating amplifier. It can be used in the control loop to transmit the amplified error voltage onto the free noninverting input of the comparator A2. A voltage change is thus transformed into a duty cycle change. The common mode range of A1 covers 0 to +5V. A1's low output impedance allows the use of feedback for the adjustment of the regulator loop-characteristics.

PULSE TURN-OFF FLIP-FLOP

This flip-flop enables the outputs at the beginning of each half period, and upon an error signal from A7 or a turn-off signal from A2 switches the outputs off for the remainder of the half period. Double pulses at the output cannot occur.

COMPARATOR A3

A3 limits the voltage at the $C_{soft\ start}$ pin (and also one input of A2) to a maximum of 5V. For a specified slope of the rising ramp generator edge, the duty cycle can be limited to a maximum value.

COMPARATOR A4

Comparator A4 has its switching threshold set to 1.5V and its output connected to the error flip-flop, so that when the voltage at capacitor $C_{soft\ start}$ is less than 1.5V the flip-flop is set. The error flip-flop only accepts the set pulse if no reset signal is present. Thus, an output turn-on is prevented as long as an error signal is present.

SOFT START

The output duty cycle is a function of the lower of the two voltages at the noninverting inputs of A2. At the time the Am6301 is turned on, the voltage at capacitor $C_{soft\ start}$ is equal to 0V. As long as no error exists, this capacitor is charged with a current of 6μA to the maximum value of 5V. In the case of an error, $C_{soft\ start}$ is discharged with a current of 2μA. The error flip-flop is set when the $C_{soft\ start}$ voltage is below 1.5V and the outputs are enabled if a reset signal is not present at the same time. The minimum ramp generator voltage is 1.8V, therefore, the soft start circuit only controls the duty cycle after the voltage at $C_{soft\ start}$ exceeds 1.8V.

ERROR FLIP-FLOP

Error signals to input $\overline{R}$ of the error flip-flop cause the outputs to be disabled immediately. The system turns on again using the soft start, after the error has been eliminated.

COMPARATOR A5 – OVER VOLTAGE

The input or output voltages of an SMPS can be monitored using A5. In the case of an over voltage, the error flip-flop immediately disables the IC outputs. After the over voltage is reduced, the SMPS turns back on using the soft start. The output of A5 can be fed back to the input. This causes the IC output stage to remain disabled even after elimination of the over voltage, until the supply voltage is briefly turned off, or the over voltage input is briefly connected to ground. To use this SCR-type action, the voltage to be monitored must be coupled resistively ($\geq$5KΩ) to the over voltage comparator.

COMPARATOR A6 – ON/$\overline{\text{OFF}}$ UNDER VOLTAGE

The comparator A6 reacts to an under voltage relative to V_{REF} and switches the IC outputs off. The input voltage of the SMPS can for example, be monitored, turning the outputs off if the input voltage is below a desired level. When the input voltage returns to the desired level, the Am6301 turns back on using the soft start. This input can also be used as a TTL compatible ON/$\overline{\text{OFF}}$ control.

COMPARATOR A7 – DYNAMIC CURRENT LIMITING CIRCUIT

A7 provides for the recognition of over current in the switching transistors. The system is turned on again at the beginning of the half period after the error is eliminated, the soft start is not used however. The A7 common mode range extends from 0 to +4V so that the smallest voltage drops can be recognized. The delay time from the occurrence of an error to the disabling of the outputs is only 250ns.

COMPARATOR A8 – IC UNDER VOLTAGE

Comparator A8 prevents undefined operating conditions of the IC outputs if the IC supply voltage becomes too low. If $V_S \leq$9V, the output stage is disabled. This condition is maintained until V_S = 0V. Built-in hysteresis prevents permanent switching at the comparator's switching threshold. At a supply voltage of $V_S \geq$9.6V, the Am6301 turns on using the soft start.

SYMMETRY

Saturation of the transformer core must be prevented in push-pull converters. The degree of saturation of the transformer can be determined with an external circuit; and, in relation to this, the on times of the outputs can be asymmetrically shortened. If the symmetry correction circuit is not required, the symmetry inputs must be connected to ground. The input levels are TTL compatible.

OUTPUTS, DEADTIME

The two outputs Q_1 and Q_2 are transistors with open collectors. Their saturation voltage is 1V at 25mA. They operate in a push-pull mode and can be connected in parallel to drive single-ended converters with a maximum duty cycle of 96%. The time, during which only one of the two outputs is on, can be varied. The duration of the falling edge at the VCO is the same as the minimum time (dead time) during which both outputs are disabled simultaneously. The dead time, in push-pull SMPS, prevents the power transistors from being on at the same time.

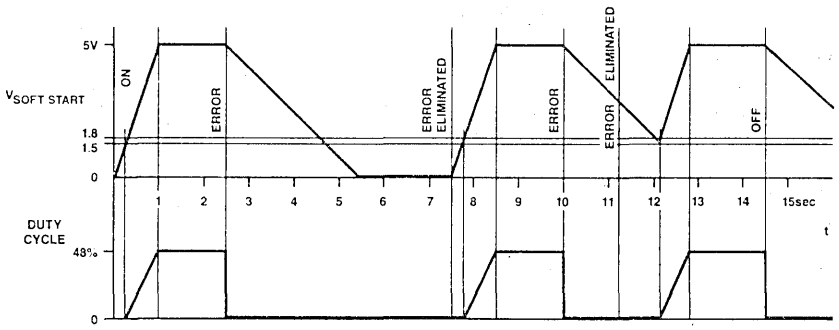


Figure 1. Am6301 System Timing Showing Soft Start, Error Timing, and Remote Shutdown. ($C_{soft\ start}$ = 1μF.)

ABI-021

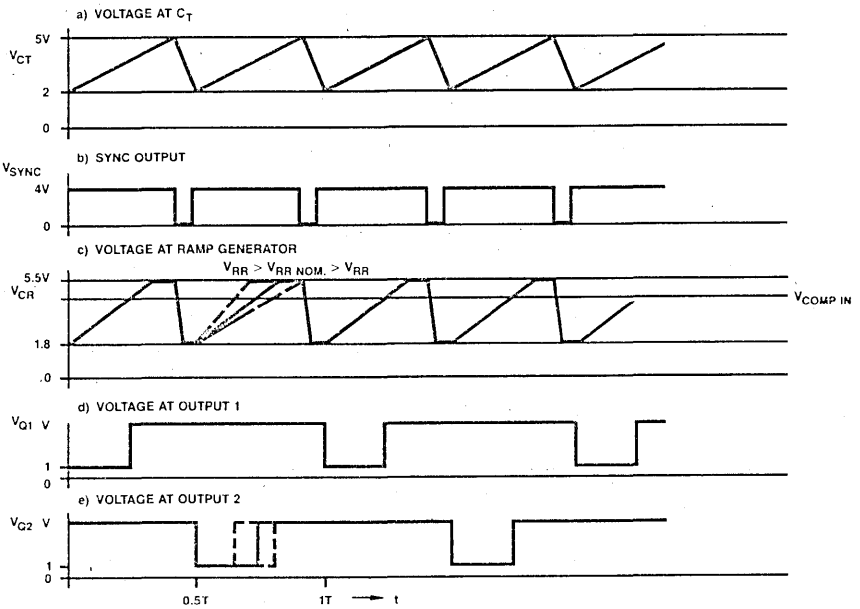


Figure 2. Am6301 Pulse Timing Diagram, Dotted Lines Show the Effect of Feed-Forward Control.

ABI-022

LINEAR
Am6301

FUNCTIONAL PIN DESCRIPTION

V_{REF} The output of the internal 2.5V reference.

Output Q_1, Q_2 The open collector output transistors capable of sinking 70mA each.

SYMQ_1, Q_2 Transformer unbalance control inputs. With a small amount of external circuitry these inputs can be used to cause assymetrical output duty cycles. This allows correction for imbalances in the push-pull circuitry.

SYNC OUT The VCO output, used for synchronizing other circuits to the Am6301.

$C_{soft\ start}$ An external capacitor at this pin causes the output duty cycle to increase linearly during power up.

R_T, C_T An external resistor and a capacitor at these pins control the VCO center frequency of the phase locked loop oscillator.

C_{filter} An external filter capacitor for the control voltage of the phase locked loop is connected to this pin.

SYNC IN This pin is connected to one input of the phase comparator in the phase locked loop, the other input is internally connected to the VCO output.

R_R, C_R An external resistor and a capacitor at these pins control the slope of the ramp generator. The feed-forward control works by changing the voltage across R_{ramp} which affects the ramp slope and causes a modulation of the duty cycle.

Comp In The noninverting input of the pulse width modulating comparator.

Amp Out The output of the uncommitted operational amplifier. This amplifier is used as the error amplifier in most systems.

(+) Amp In, (−) Amp In These are the inputs of the uncommitted operational amplifier.

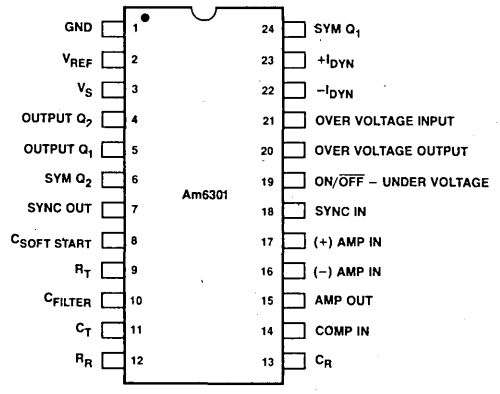
ON/$\overline{OFF}$ Under Voltage This input disables the outputs when it is connected to a voltage lower than V_{REF}. It can be connected as a remote shutdown or as an under voltage protection.

Over Voltage Input This input disables the outputs whenever it is higher than V_{REF}.

Over Voltage Output The output of the over voltage comparator. This pin can be connected back to the over voltage input for SCR-type protection.

$+I_{DYN}$, $-I_{DYN}$ Sense inputs for the dynamic current limiting circuit.

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

ABI-029

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM6301DL	D-24-1	L	C-1
AM6301DC	D-24-1	C	C-1
AM6301PC	P-24-1	C	C-1

Notes: 1. D = Hermetic DIP, P = Plastic DIP. Number following letter is number of leads.
2. C = 0 to 70°C; L = −25 to 85°C.
3. Level C-1 conforms to MIL-STD-883, Class C.

COMMUNICATIONS
Am7910
PRELIMINARY DATA (Revised)

Am7910
FSK Modem
WORLD-CHIP™

- Complete FSK MODEM in a 28-pin package (except line interface)
- Meets basic Bell 103/113/108, Bell 202, CCITT V.21, CCITT V.23 specifications (pin-programmable selection)
- No external filtering required
- All digital processing, including digital filters
- ADC/DAC on chip
- Includes essential RS-232/CCITT V.24 handshake signals
- Auto-answer capability
- Local copy/test modes
- 1200 bps full duplex on 4-wire line

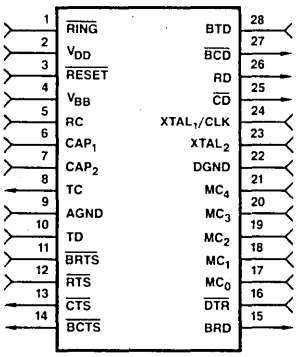


Figure 1. Am7910 Pinout

MMC-036

GENERAL DESCRIPTION

The Am7910 is a single-chip asynchronous Frequency Shift Keying (FSK) voiceband modem. Operating at rates up to 300, 600 or 1200 bits per second, it is compatible with the applicable Bell and CCITT recommended standards for 103/113/108, 202, V.21 and V.23 type modems. Five mode control lines select a desired modem configuration.

Digital signal processsing techniques are employed in the Am7910 to perform all major functions such as modulation, demodulation and filtering. The Am7910 contains on-chip analog-to-digital and digital-to-analog converter circuits to minimize the external components in a system. This device includes the essential RS-232/CCITT V.24 terminal control signals with TTL levels.

Clocking can be generated by attaching a crystal to drive the internal crystal oscillator or by applying an external clock signal.

A data access arrangement (DAA) or acoustic coupler must provide the phone line interface externally.

The Am7910 is fabricated using N-channel MOS technology in a 28-pin package. All the digital input and output signals (except the external clock signal) are TTL compatible. Power supply requirements are ±5 volts.

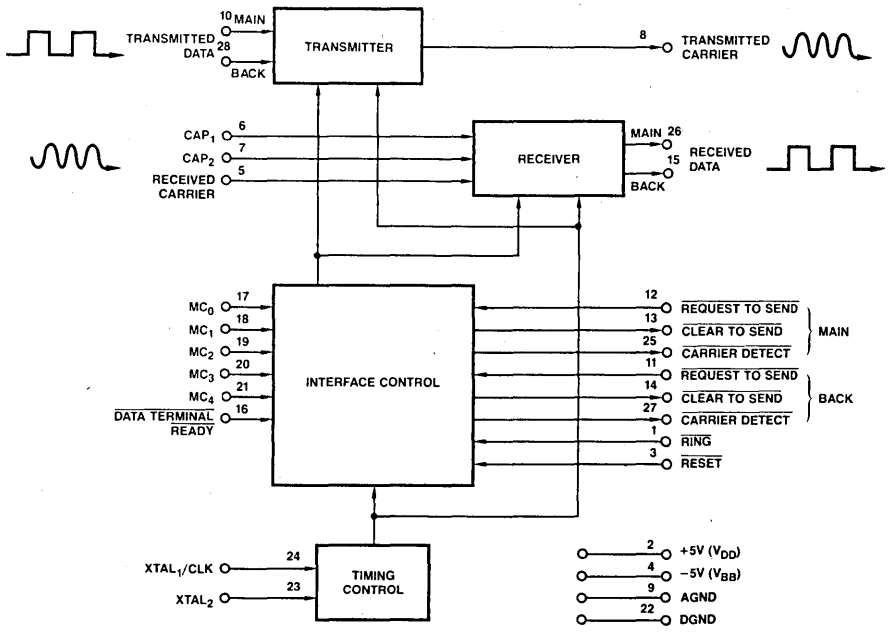


Figure 2. Am7910 Block Diagram

MMC-179

WORLD-CHIP is a trademark of Advanced Micro Devices.

A COMPLETE FSK MODEM ON ONE WORLD-CHIP™

It's the World's First

The new Am7910 is the first complete, asynchronous Frequency Shift Keying modem ever offered on a single LSI chip. Our Am7910, a crystal, and a few inexpensive, non-critical components are all you need. No external filters, no hybrids, no tuned circuits are needed. Never before has the modem function been so easy to build into your products. See Figure 1.

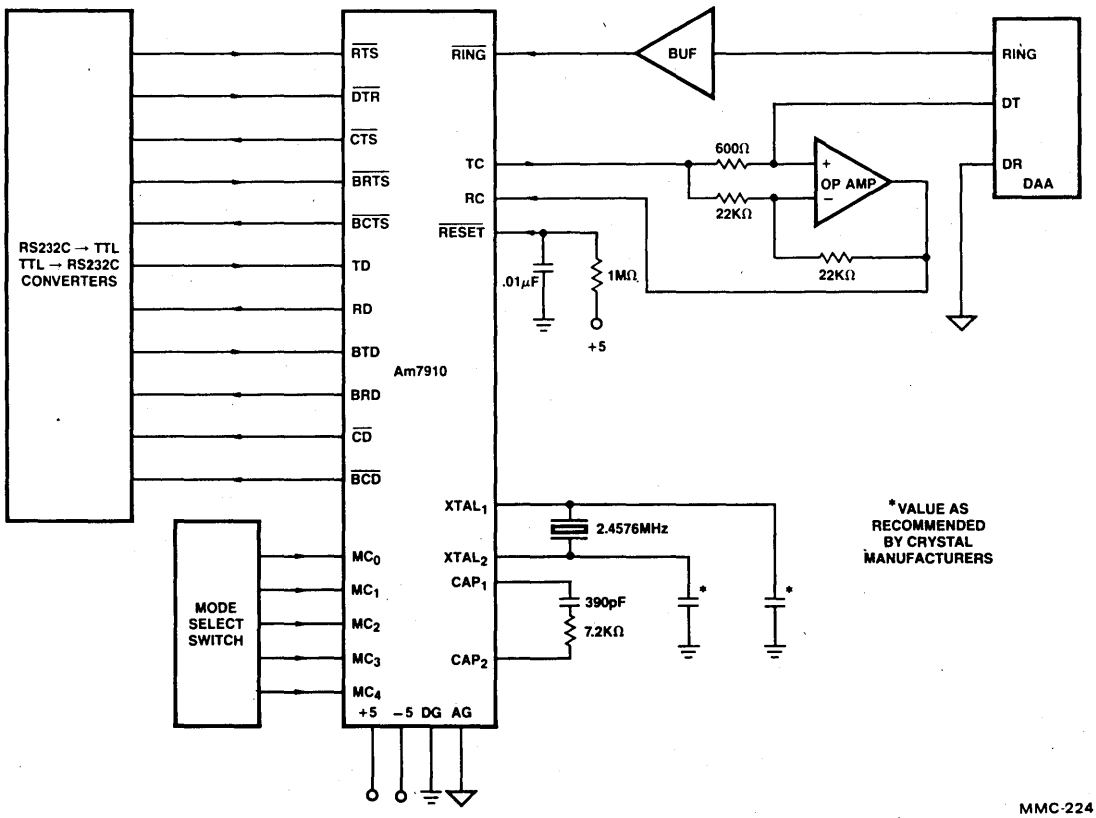
It's the World's Most Complete

All the features a modem should have are built right in. Filters are already there. Handshake signals already there. Auto-answer is already there. Local loopback is already there. Back channels are already there. No extra components are required to implement these functions. Even line equalization is available if you want it. No modem chip or chip set has ever offered you so many features.

It's a WORLD-CHIP™

No matter where you market your product, the Am7910 is the perfect modem solution. It's designed to meet communications performance standards around the world. Without any additional circuitry, it can be switched to any of 9 Bell or CCITT standards. The flexibility of Digital Signal Processing allows systems built with the Am7910 to be used all over the world without modification to the modem circuit.

Figure 1. Stand-Alone Am7910 Application



DIGITAL SIGNAL PROCESSING FOR HIGH STABILITY, WITHOUT CRITICAL COMPONENTS

The Am7910 Doesn't Drift With Time or Temperature

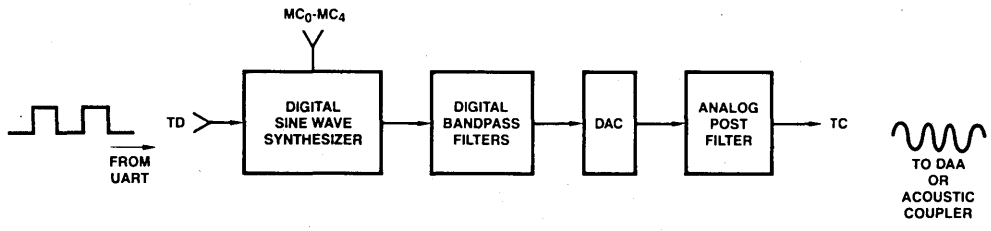
The Am7910 uses digital signal processing techniques (DSP) to perform all major functions, including modulation, demodulation and filtering. Because of the use of DSP, the performance of each section of the Am7910 is perfectly predictable and inherently stable over time and temperature. The modem performance specifications are designed into the digital signal processing algorithms, and that's where they stay, inside the chip, never changing, guaranteed. There's nothing to adjust, nothing to age or drift. See Figure 2.

No External Filters

Digital Signal Processing completely eliminates the need for external critical-tolerance filters that analog designs require. Since no critical tuned components are required, printed circuit board design with the Am7910 is easier than ever. And DSP does not produce the noise and supply voltage sensitivity that is commonly found in switched capacitor designs. The bottom line is, fewer components, therefore a lower cost system solution.

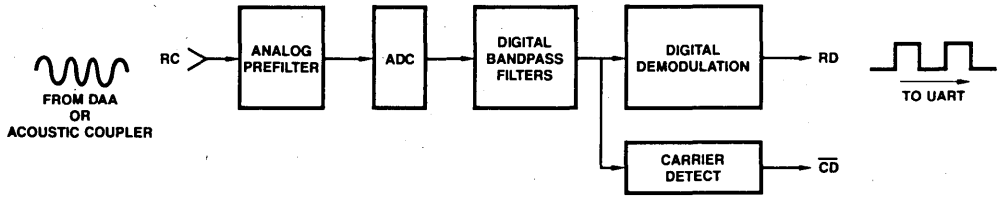
Figure 2.

a) Transmitter Block Diagram



MMC-033

b) Receiver Block Diagram



MMC-034

SELECTABLE TO ANY OF 9 DIFFERENT WORLD STANDARDS

The Am7910 is designed to be used in equipment all over the world. The device operates in Bell 103 and 202, and CCITT V.21 and V.23 modem configurations at baud rates from 300 to 1200bps (with back channel). Mode selection is controlled by five simple programming inputs. No crystals need to be changed. No extra resistors, capacitors, or interface circuits. Just switch a few control lines.

MODEM CONFIGURATIONS

STD	BPS	DUPLEX	FEATURES
Bell 103	300	Full	Originate
Bell 103	300	Full	Answer
Bell 202	1200	Half	
Bell 202	1200	Half	Line Equalizer
CCITT V.21	300	Full	Originate
CCITT V.21	300	Full	Answer
CCITT V.23 mode 2	1200	Half	
CCITT V.23 mode 2	1200	Half	Line Equalizer
CCITT V.23 mode 1	600	Half	

MORE BUILT-IN FEATURES MAKE THE Am7910 THE EASIEST MODEM TO USE

Loopback for Simplified Testing

Ten loopback modes exist which permit both analog and digital loopback for each modem configuration. When a loopback mode is selected, the signal processing circuits for both the transmitter and receiver are set to operate on the same channel or frequency band. The analog output (Transmitted Carrier) and the analog input, (Received Carrier) can be externally connected together for local analog loopback. Alternatively, the digital data signals (TD and RD, or BTD and BRD,) can be connected externally, allowing a remote modem to test the local modem with its digital data signals looped back. Thus, the Am7910 reduces maintenance, service time, and cost. The 202 and V.23 loopback modes can also be used for 1200bps full duplex operation over 4-wire lines.

Back Channel Option Included

Low bit-rate back channels are provided by the Am7910 when the Bell 202 or CCITT V.23 modem configurations are selected. The back channel uses the remaining bandwidth of the line to return acknowledgement and control signals to the sender on another channel, while the sender continues to transmit at 1200 baud. Overall transmission speed is improved by not having to turn the line around to send an acknowledgement, nor is it necessary to complete transmission of a data block before receiving an error signal. The 202 back channel allows up to 5 bits per second and the V.23 back channel allows up to 75 bits per second.

Auto-Answer for Remote Installations

Auto-answer capability, important for equipment in remote places, is also built in. Upon receipt of a signal at its Ring Input, the Am7910 generates a silence interval followed by an answer tone of the proper duration at the Transmitted Carrier output. The auto-answer sequence meets Bell and V.25 specifications.

RS-232 and CCITT V.24 Terminal Control Signals Provided On-Chip

Essential terminal control signals such as Data Terminal Ready (DTR), Request to Send (RTS), Clear to Send (CTS) and Carrier Detect (CD), are included in the Am7910. All the specified delays, such as Request-to-Send ON to Clear-to-Send ON are automatically inserted. The control signals are TTL compatible.

SETS THE INTERNATIONAL STANDARD OF PERFORMANCE

The measure of a modem's performance is its ability to extract correct data from a signal received over a line with severe distortion, attenuation, and noise. The graphs below show the Bit Error Rate (BER) of the Am7910 under two sets of conditions. At the left is the data for a Bell 103 configuration over an undistorted line and a line with amplitude and group delay distortion. On the right is the data for a V.23 configuration for an undistorted and a severely distorted line. Compare this performance data with any other modem chip or chip set and you'll see why the Am7910 sets the standard.

Performance Curves

Figure 3. 103 ORIG, 300bps BER versus SNR, Different Lines

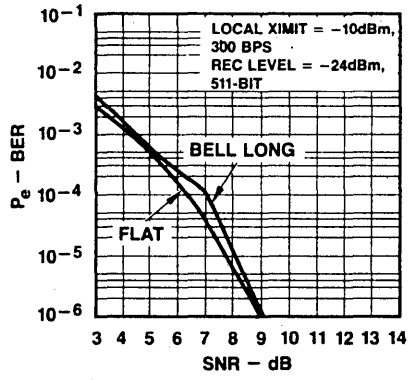
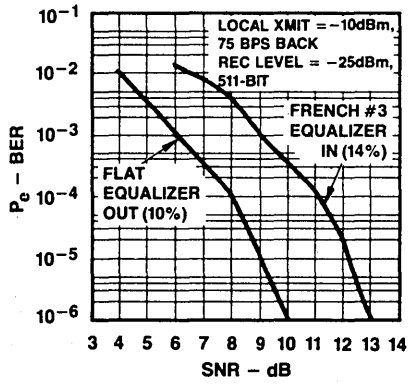


Figure 4. CCITT V.23, 1200bps Different Lines



MMC-054

MEETS THE INTERNATIONAL STANDARD OF QUALITY

Fabricated using N-channel MOS technology in a 28-pin package, every lot of Am7910 FSK modems that Advanced Micro Devices ships meets or exceeds the International Standard of Quality, INT-STD-123. We promise you a 0.3% AQL-the best guarantee available. When you choose the Am7910, you have opted for state-of-the-art design along with quality that's second to none.

THE WORLD-CHIP™ SERIES

Telephone systems around the world are evolving rapidly into something new: a huge digital data communications network. The crossbar switches of yesterday are being replaced by compact electronic switches that route digital bit streams from one subscriber to another. The wires that used to carry human speech alone now also carry streams of digital data via modems. Soon the telephone set itself will be changed from a simple device for talking and listening into a specialized data terminal, capable of doing much more.

As the information carried by our telephone networks has changed, new standards have been added to the old. Standards to digitize voice. Standards for sending digital data over voice-grade lines. Standards for multiplexing many data packets onto a single line. Around the world, two groups of standards are used – one developed by Bell in the U.S., another developed by the CCITT. Until now, the electronic components designed to make this revolution possible have been specialized for one group of standards or the other, and usually for only one standard or variation within that group.

Advanced Micro Devices' World-Chip™ Series is different. We're using a variety of technologies to create circuits that support the telecom revolution all over the world. We're using advanced architectural concepts, especially digital signal processing, to move critical filtering and signal conditioning directly onto the integrated circuit. Digital techniques provide guaranteed high stability and repeatability, and also allow changes to filtering characteristics under user program control. We're using our skills in both linear and digital circuit design to put the conversions between analog signals and digital data on the same IC as the digital processing circuits. And we're using our MOS and Bipolar process technologies to solve each part of the system problem in an optimum way with parts that are designed to work together. By the end of the decade AMD will have led the way to more efficient, effective and inexpensive methods for making the world an even smaller (and faster) place in which to communicate.

AMD has developed a set of components that work in any of the world's telecommunications systems. Each integrated circuit can be programmed to perform its function in conformance with any of the applicable standards. The state-of-the-art features built into our devices are available simultaneously to customers designing equipment for any of the world's telecom markets. And customers who themselves design equipment for more than one market can use a single set of circuits – Advanced Micro Devices' World-Chips™ – to meet all their needs.

RELATED WORLD-CHIP™ SERIES PRODUCTS:

- Am7901/7902 Subscriber Line Audio-Processing Circuit
- Am7950 SLIC

Advanced Micro Devices

COMMUNICATIONS
Am7990 Family Ethernet Node

Advanced Micro Devices has developed a set of MOS and Bipolar high performance integrated circuits designed to minimize the cost of connecting multivendor devices to an Ethernet bus. This family is designed to provide in the minimum package count, all the logic, protocol and control functions required to interface all the popular 16-bit processors to an Ethernet local area network.

Am7990 Local Area Network Controller for Ethernet (LANCE)

- Buffer management
- On board DMA
- Limit Error Detection
- Address Detection
- Line Access Protocol (CSMA/CD)
- Collision handling

Am7991 Serial Interface Adaptor (SIA)

- Manchester encoding/decoding
- Differential to TTL signal conversion
- Transceiver cable interface

Am79XX Ethernet Transceiver

- Collision detection
- Line protection

Key System Level Features

16-Bit Bus Interface

Compatible with

- **Z8000**
- **8086**
- **68000**
- **LSI-II**

Broad Range of Diagnostics

Alternate Sourced

Meets the Ethernet Specification

Ethernet Data Link Layer Support

- Buffer management
- Data encapsulation
- Framing and packet control
- CRC generation/check
- Serial/deserialization

Ethernet Physical Link Layer Support

- Data rate: 10 Mb/s
- Carrier-sense multiple-access with collision detection
- Transceiver interface compatibility

COMMUNICATIONS
Am7990 Family Ethernet Node System Overview

Advanced Micro Devices is introducing a set of LSI devices that provides the Ethernet system designer, and designers of Ethernet compatible products, a low cost physical and link level interface to the Ethernet Bus.

The Am7990 Ethernet interface family is being designed using a combination of MOS and IMOX™ bipolar technologies. This family consists of the Am7990 Local Area Network Controller for Ethernet (LANCE), and the Am7991 Serial Interface Adapter (SIA). As shown in Figure 1, the Am7990 family provides the complete interface between the device System Bus and the Ethernet Transceiver Cable.

The Am7990 LANCE is a 10M-bit/sec MOS device in a 48-pin package, optimized to perform the link level Ethernet protocol. The CSMA/CD network access, memory management (onboard DMA), error reporting, packet handling, and microprocessor interface functions also reside in the LANCE.

The Am7991 Serial Interface Adaptor provides Manchester encoding and decoding of the serial bit stream and interfaces the TTL output of the LANCE to the differential inputs of the transceiver. It has an on board phase locked loop to recover clock from an incoming signal and can use an external crystal oscillator or TTL inputs to provide clock for transmission.

Coupling the Ethernet Node to the Ethernet Cable requires a transceiver. Commercially available board or module transceivers can be used with the LANCE and SIA. Advanced Micro Devices has a monolithic transceiver in an early phase of development which should lower the cost significantly in this area as well.

BASIC SYSTEM OPERATION

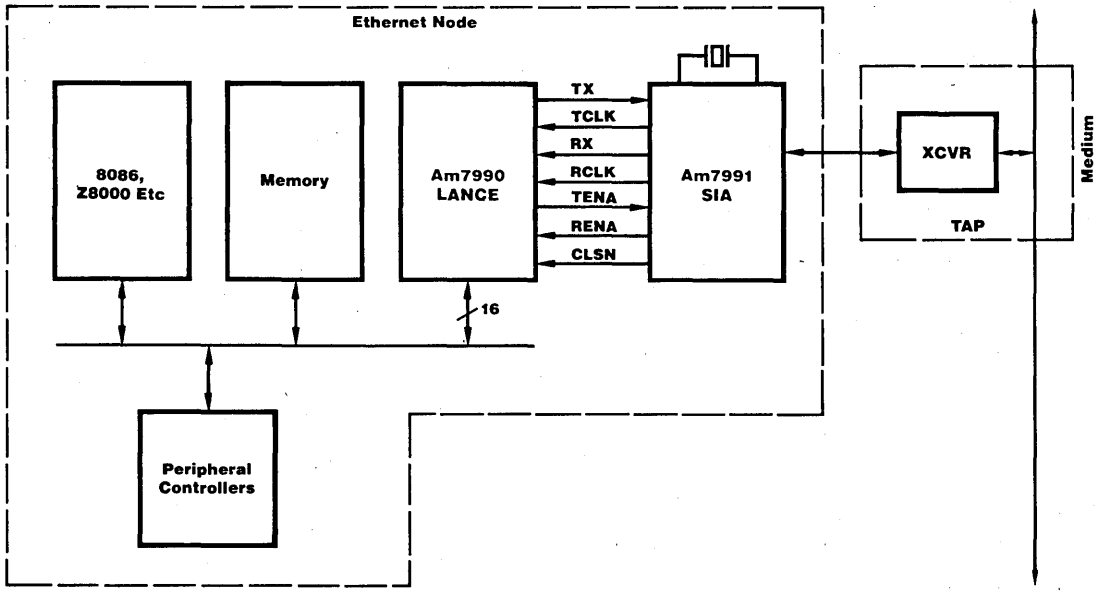
Ethernet is a send and receive half duplex system. The node must function in either transmit or receive mode at any instant in time. Before transmission the node must be sure there is no contention for the bus. The Ethernet CSMA/CD network access algorithm is implemented completely within the LANCE. In addition to listening for a clear coax before transmitting, Ethernet handles collisions in a predetermined way. Should two nodes attempt to transmit at the same time, the signals will collide and the data on the coax will be garbled. The transmitting nodes listen while they transmit and detect the collision. Both continue to transmit for a predetermined length of time to "jam" the network, insuring all nodes have recognized the collision. The transmitting nodes then delay a random amount of time according to the "truncated binary backoff" algorithm implemented in the LANCE, before attempting to transmit again. This minimizes the possibility of collision on retransmission.

TRANSMIT MODE

In the transmit mode, the LANCE initiates a DMA cycle to access data from a transmit buffer. It prefaces the data with a preamble, and sync pattern then calculates and appends a 32-bit CRC.

This packet is transmitted serially to the SIA. The Manchester encoder in the SIA takes the transmitted data from the LANCE and creates the Manchester encoded differential signals TRANSMIT+ and TRANSMIT− to drive the Transceiver cable. These differential signals are coupled through the transceiver cable, transceiver and on to the Ethernet coaxial cable.

Figure 1. Ethernet Node Architecture



RECEIVE MODE

When carrier is present on the Ethernet coax, the Transceiver will create the differential signals RECEIVE+ and RECEIVE−. These inputs to the SIA are decoded by the Manchester decoder. A phase locked loop synchronizes to the Ethernet Preamble, allowing the decoder to recover clock and data from the encoded signals. These two signals are supplied to the LANCE as the TTL signals RECEIVE DATA and RECEIVE CLOCK. In addition, the SIA creates the signal CARRIER PRESENT while it is receiving data from the cable, indicating to the LANCE that receive data and clock are available. When these signals reach the LANCE, the CRC is calculated and compared to the CRC checksum at the end of the packet. If the calculated CRC doesn't agree with the packet CRC an error bit is set and an interrupt generated to the microprocessor.

ADDRESSING

There are three addressing modes. The first is physical addressing which requires a comparison of the 48-bit destination address in the packet with the node address programmed into the LANCE during initialization. The second mode is multi-cast addressing. This mode can be useful when sending packets to all of one type of a device simultaneously on the network, or for a broadcast situation where all nodes on the network receive the packet. In the final "promiscuous" mode of operation, a node will accept all packets on the coax regardless of their destination address.

ERROR REPORTING

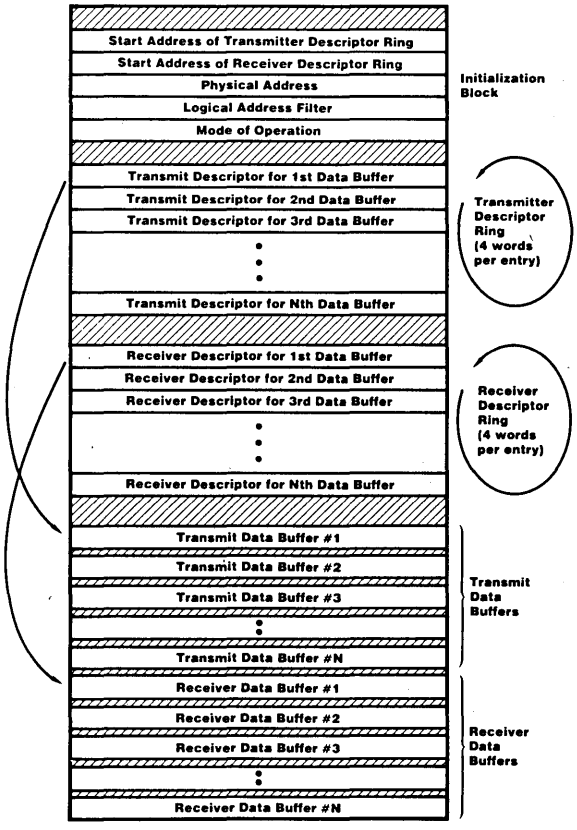
Extensive error reporting is provided by the LANCE through microprocessor interrupt and error bits in a status register. The following are the significant error conditions:

- CRC error on receive
- Babbling error
- Missed packet
- Memory error

BUFFER MANAGEMENT

A key feature of the LANCE and it's on board DMA channel is the flexibility and speed of communication between the LANCE and the host microprocessor through common memory locations. The basic organization of the buffer management consists of circular task queues called descriptor rings for transmit and receive operations. Up to 128 tasks may be queued on a descriptor ring awaiting execution by the LANCE. (Figure 2)

Figure 2. LANCE/Processor Memory Interface



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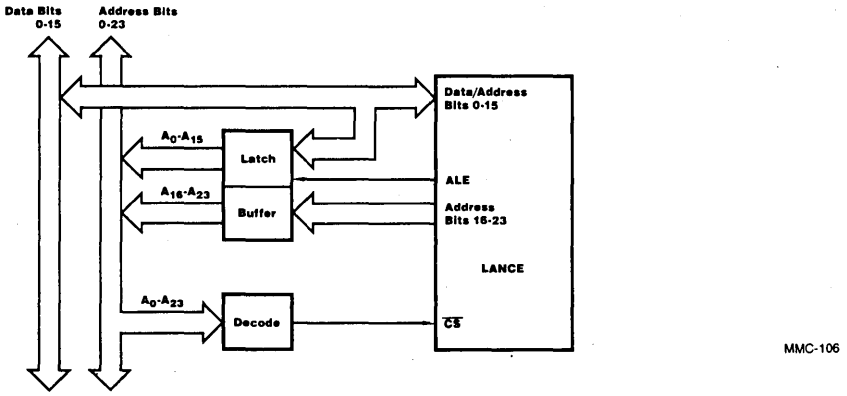
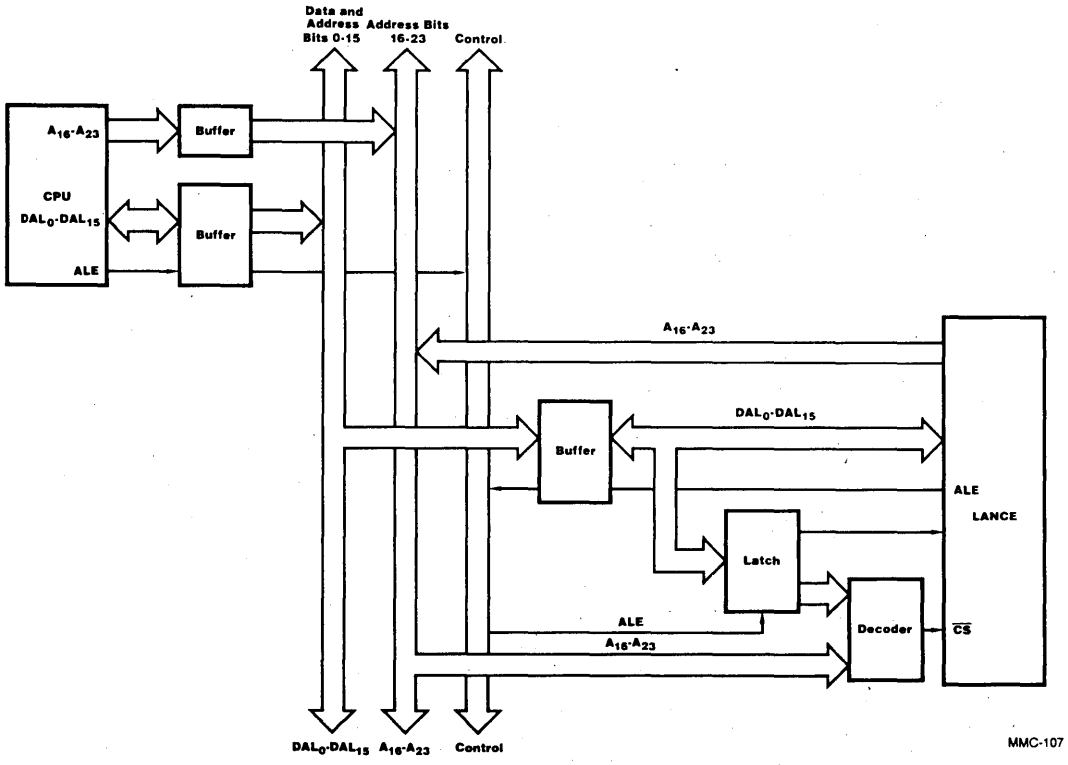
MICROPROCESSOR INTERFACE

The parallel interface of the LANCE has been designed to be "friendly" or easy to interface to a variety of popular 16-bit microprocessors. These microprocessors include the 68000, Z8000, 8086, and LSI-II devices.

The LANCE has a 24-bit wide linear address space when it is in the Bus Master Mode allowing it to DMA directly into the entire address space of the above microprocessors. The LANCE interfaces with both multiplexed and demultiplexed data busses (Figure 3) and features control signals for address/data bus transceivers.



a) Demultiplexed Bus



b) Multiplexed Bus System Overview

Figure 3.

COMMUNICATIONS
Am7990 Family Ethernet Node
IN DEVELOPMENT

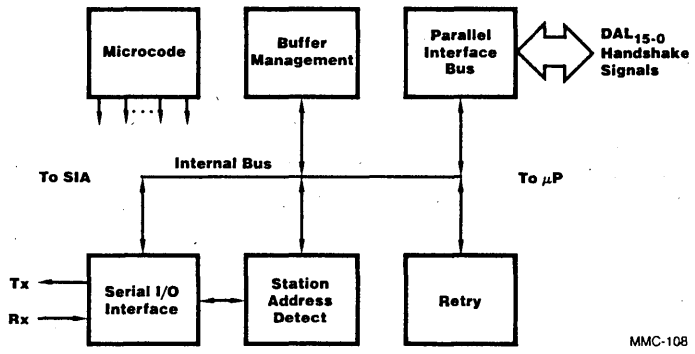
Am7990
Local Area Network Controller for Ethernet™ (LANCE)

- Compatible with Ethernet specifications
- Single +5 volt power supply
- Single phase 10MHz TTL level clock
- TTL compatible inputs and outputs
- Direct interface to variety of microprocessors
- CSMA/CD access protocol
- Collision handling and retry
- On board DMA control
- Error detection and interrupt capability
- Packet formatting including:
  preamble and CRC insertion
  preamble stripping and CRC checking

GENERAL DESCRIPTION

The Am7990 Local Area Network Controller for Ethernet (LANCE) is a 48 pin VLSI device designed to greatly simplify interfacing a microcomputer or minicomputer to an Ethernet Local Area Network. This chip, in conjunction with the Am7991 Serial Interface Adapter (SIA), and closely coupled local memory and microprocessor is intended to provide the user with a complete interface module for an Ethernet network. The Am7990 is designed using a scaled N Channel MOS technology and is compatible with a variety of microprocessors.

LANCE BLOCK DIAGRAM



PIN DEFINITIONS

DAL_{00}-DAL_{15} **Data/Address Lines (Input/Output 3-State).** The time multiplexed Address/Data bus.

A_{16}-A_{23} **High Order Address Bus (Output 3-State).** The additional address bits necessary to extend the DAL lines to output a 24 bit address. These lines are driven as a Bus Master only.

READ **(Input/Output 3-State).** Indicates the type of operation to be performed in the current bus cycle. This signal is an output when the LANCE is a Bus Master.

High – Data is placed on the DAL by the chip

Low – Data is taken off the DAL by the chip

The signal is an input when the LANCE is a Bus Slave

High – Data is placed on the DAL by the chip

Low – Data is taken off the DAL by the chip

$\overline{BM_0}$, $\overline{BM_1}$ Byte Mask (Input/Output). Pins 15 and 16 are programmable through bit (00) of CSR3. Asserting $\overline{RESET}$ clears CSR3.

If CSR3 (00) BCON = 0
I/O pin 16 = $\overline{BM_1}$ (Input/Output 3-State)
I/O pin 15 = $\overline{BM_0}$ (Input/Output 3-State)

If CSR3 (00) BCON = 1
I/O pin 16 = $\overline{BUSAKO}$ (Output)
I/O pin 15 = Byte (Input/Output 3-State)

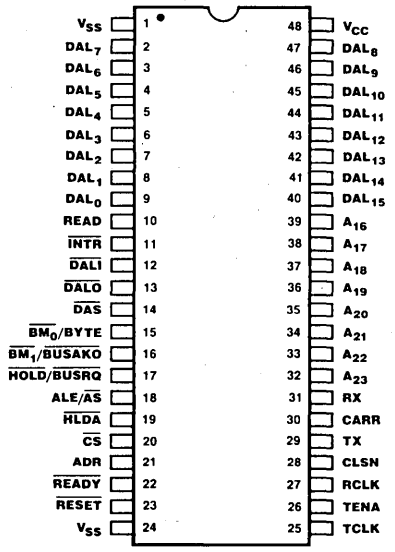
$\overline{BM_0}$, $\overline{BM_1}$ Byte Mask. Indicates the byte(s) of a bus transaction to be read or written. The $\overline{BM}$ lines are ignored by LANCE as a Bus Slave, which assumes word transfers only. The LANCE drives the $\overline{BM}$ lines only as a Bus Master. Byte selection is done as outlined in the following table.

CSR3 (00) BCON = 0

$\overline{BM_1}$	$\overline{BM_0}$	
LOW	LOW	Whole word
LOW	HIGH	Upper byte
HIGH	LOW	Lower byte
HIGH	HIGH	None

BYTE An alternate byte selection line. Byte selection is done using the BYTE line and DAL_{00} line, latched during the address portion of the bus transaction. The BYTE line is ignored by a Bus Slave (similar to $\overline{BM_0}$, $\overline{BM_1}$). There are two modes of ordering bytes dependent on bit 02 of CSR_3 (BSWP). This programmable ordering of upper and lower bytes is necessary for compatibility with the various 16 bit microprocessors.

Signal Line \ Mode Bits	BSWP = 0 and BCON = 1	BSWP = 1 and BCON = 1
BYTE = L and DAL_{00} = L	Word	Word
BYTE = L and DAL_{00} = H	Illegal	Illegal
BYTE = H and DAL_{00} = H	Upper Byte	Lower Byte
BYTE = H and DAL_{00} = L	Lower Byte	Upper Byte



Note: Pin 1 is marked for orientation.

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$\overline{CS}$ **Chip Select (Input).** Indicates, when asserted, that the LANCE is the slave device of the data transfer. $\overline{CS}$ must be valid throughout the data portion of the bus cycle.

ADR **Register Address Port Select (Input).** When LANCE is slave, ADR indicates which of the two register ports is selected. ADR LOW selects register data port, ADR HIGH selects register address port. ADR must be valid throughout the data portion of the bus cycle.

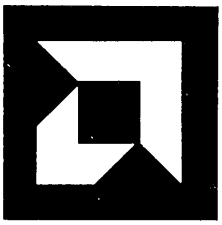
ALE/$\overline{AS}$ **Address Latch Enable (Output 3-State).** Used to demultiplex the DAL lines and define the address portion of the bus cycle. This I/O pin is programmable through bit (01) of CSR3. As ALE, (CSR3 (01), ACON = 0) the signal transitions from a HIGH to a LOW during the entire data portion of the transaction. As AS (CSR3 (01), ACON = 1), the signal pulses LOW during the address portion of the bus transaction. The LANCE drives the ALE/$\overline{AS}$ line only as a Bus Master.

$\overline{DAS}$ **Data Strobe (Input/Output 3-State).** Defines the data portion of the bus transaction. $\overline{DAS}$ is driven only as a Bus Master.

$\overline{DALO}$ **Data/Address Line Out (Output 3-State).** An external bus transceiver control line. $\overline{DALO}$ is asserted when the LANCE drives the DAL lines.

$\overline{DALI}$ **Data/Address Line Out (Output 3-State).** An external bus transceiver control line. $\overline{DALI}$ is asserted when the LANCE reads from the DAL lines.

$\overline{HOLD}$/$\overline{BUSRQ}$ **Bus Hold Request (Output Open Drain).** Asserted by the LANCE when it requires access to memory.



COMMUNICATIONS
Am7990 Family Ethernet Node

$\overline{\text{HOLD}}$ is held LOW for the entire ensuing bus transaction. The function of this pin is programmed through bit (00) of CSR3. Bit (00) of CSR3 is cleared when $\overline{\text{RESET}}$ is asserted.

When CSR3 (00) BCON = 0

I/O pin 17 = $\overline{\text{HOLD}}$ (Output Open Drain)

When CSR3 (00) BCON = 1

I/O pin 17 = $\overline{\text{BUSRQ}}$ (Output Open Drain)

BUSRQ will be asserted only if I/O pin 17 is high prior to assertion.

$\overline{\text{HLDA}}$ **Bus Hold Acknowledge (Input).** A response to $\overline{\text{HOLD}}$ indicating that the LANCE is the Bus Master. $\overline{\text{HLDA}}$ goes back high after $\overline{\text{HOLD}}$ has gone high.

$\overline{\text{INTR}}$ **Interrupt (Ouput Open Drain).** An attention signal that indicates, when active, that one or more of the following events have occurred: a message reception or transmission has completed, an error has occurred during the transaction, the initialization procedure has completed, or a memory error has been encountered. $\overline{\text{INTR}}$ is enabled by programming register CSR0.

RX **Receive (Input).** Receive Input Bit Stream.

TX **Transmit (Output).** Transmit Output Bit Stream.

TENA **Transmit Enable (Output).** Transmit Output Bit Stream enable. A level asserted with the Transmit Output Bit Stream, TX, to enable the external transmit logic.

RCLK **Receive Clock (Input).** Normally a 10MHz square wave synchronized to the Receive data and only active while receiving an Input Bit Stream.

CLSN **Collision (Input).** A logical input that indicates that a collision is occurring on the channel.

CARR **Carrier (Input).** A logical input that indicates the presence of Carrier on the channel.

TCLK **Transmit Clock (Input).** Normally a freerunning 10MHz clock.

$\overline{\text{READY}}$ **(Input/Output Open Drain).** When the LANCE is a Bus Master, $\overline{\text{READY}}$ is an asynchronous input from external memory acknowledging that it will complete the data transfer. As a Bus Slave, the LANCE asserts $\overline{\text{READY}}$ when it has put data on the Bus, or is about to take data off the Bus. $\overline{\text{READY}}$ is a response to $\overline{\text{DAS}}$. $\overline{\text{READY}}$ returns HIGH after $\overline{\text{DAS}}$ has gone HIGH.

$\overline{\text{RESET}}$ **(Input).** Bus Reset signal. Causes the LANCE to cease operation and enter an idle state.

V_{CC} Power supply pin +5 volts ± 5%

V_{SS} Ground

FUNCTIONAL DESCRIPTION

The parallel interface of the Local Area Network Controller for Ethernet (LANCE) has been designed to be "friendly" or easy to interface to a variety of popular 16-bit microprocessors. These microprocessors include the following: Z8000, 8086, 68000, and LSI-11. The LANCE has a 24-bit wide linear address space when it is in the Bus Master Mode allowing it to DMA directly into the entire address space of the above microprocessors. When the LANCE is a Bus Master a programmable mode of operation allows byte addressing in one of two ways: A Byte/Word control signal compatible with the 8086 and Z8000, or an Upper Data Strobe and Lower Data Strobe signal compatible with microprocessors such as the 68000. A programmable polarity on the Address Strobe signal eliminates the need for external logic. The LANCE interfaces with both multiplexed and demultiplexed data busses and features control signals for address/data bus transceivers.

During initialization, the CPU loads the starting address of the initialization block into two internal control registers. The LANCE has four internal control and status registers (CSR0, 1, 2, 3) which are used for various functions such as the loading of the initialization block address, different programming modes, and status conditions. The host processor communicates with the LANCE during the initialization phase, for demand transmission, and periodically to read the status bits following interrupts. All other transfers to and from the memory are handled as DMA under microword control.

Interrupts to the microprocessor are generated by the LANCE upon completion of its initialization routine, the reception of a packet, the transmission of a packet, transmitter timeout error, a missed packet, and memory error.

The cause of the interrupt is ascertained by reading CSR0. Bit (06) of CSR0, (INEA) enables or disables interrupts to the microprocessor. In systems where polling is used in place of interrupts, Bit (07) of CSR0 (INTR) indicates an interrupt condition.

The basic operation of the LANCE consists of two distinct modes: transmit and receive. In the transmit mode the LANCE chip directly accesses data in a transmit buffer in memory. It prefaces the data with a preamble, sync pattern, and calculates and appends a 32 bit CRC. This packet is then ready for transmission to the Am7991 SIA.

In the receive mode, packets are sent via the SIA to the LANCE. The packet is loaded into buffer memory, a CRC is calculated and compared with the CRC appended to the data packet. If the calculated CRC checksum doesn't agree with the packet CRC an error bit is set.

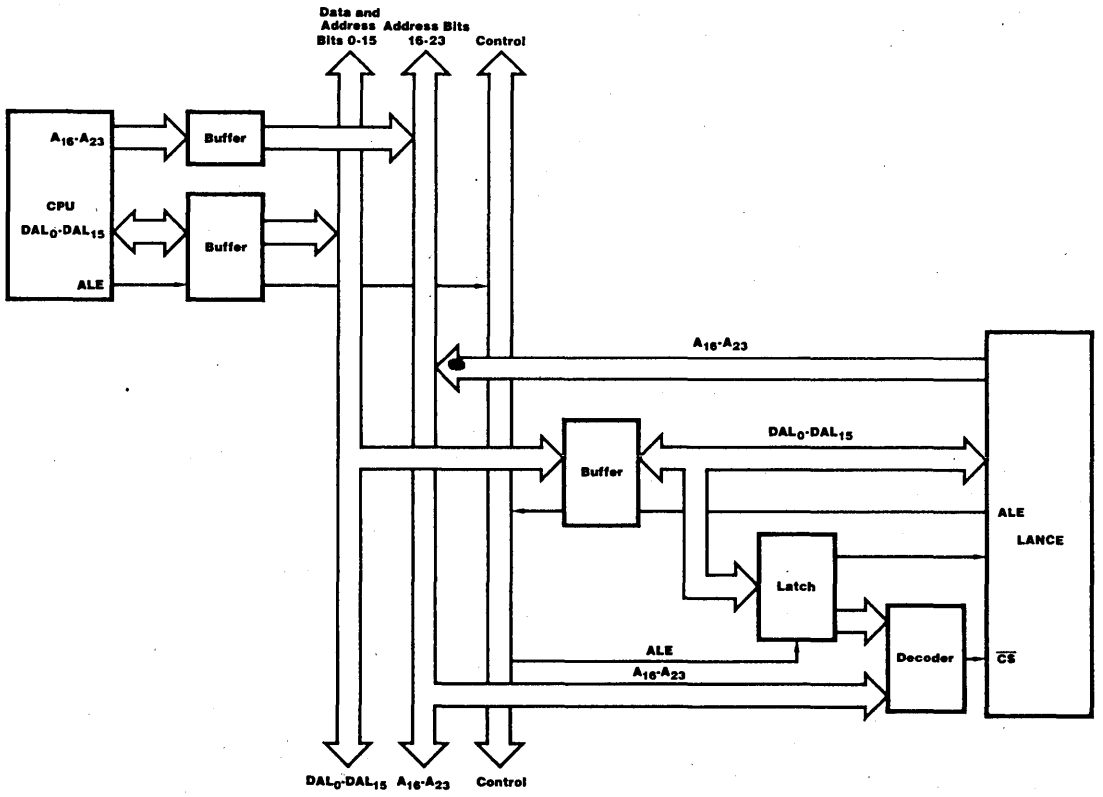
Addressing

Packets can be received using 3 different destination addressing schemes; physical, logical, and promiscuous.

The first type is a full comparison of the 48 bit destination address in the packet with the node address that was programmed into the LANCE during an initialization cycle. There are two types of logical address, one is group type mask where the 48 bit address in the packet is put through a hash filter in order to map the 48 bit physical addresses into 1 of 63 logical groups. This mode can be useful if sending packets to all of a particular type of device simultaneously (i.e., send a packet to all file servers or all printer servers). The second logical address is a multicast address where all nodes on the network receive the packet. The last receive mode of operation is the so-called "promiscuous mode" in which a node will accept all packets on the coax regardless of their destination address.

Collision Detection and Implementation

The Ethernet CSMA/CD network access algorithm is implemented completely within the LANCE. In addition to listening for a clear coax before transmitting, Ethernet handles collisions in a predetermined way. Should two transmitters attempt to seize the coax at the same time they will collide and the data on the coax will be garbled. The transmitting nodes listen while they transmit and detect the fact that the data on the coax is garbled, continue to transmit for a predetermined length of time to "jam" the network and ensure that all nodes have recognized the collision. The transmitting nodes then delay a random amount of time



a) Multiplexed Bus

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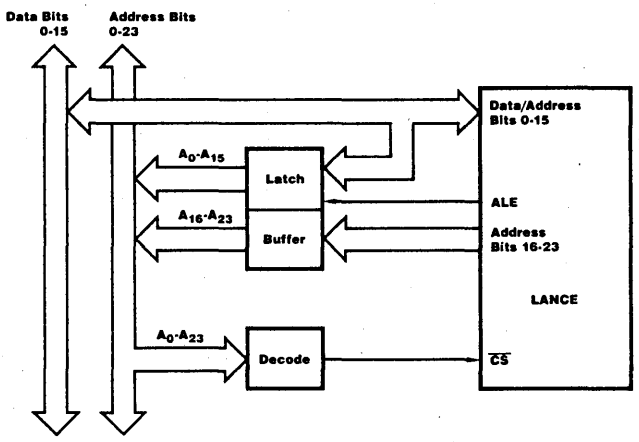


b) Demultiplexed Bus

Figure 1. LANCE/CPU Interfacing

MMC-106

according to the "truncated binary backoff" algorithm specified in the Ethernet specification in order that the colliding nodes don't try to repeatedly access the network at the same time. Up to 16 attempts to access the network are made by the LANCE before reporting back an error due to excessive collisions.

Error Reporting

Extensive error reporting is provided by the LANCE through a microprocessor interrupt and error bits in a status register. The following are the significant error conditions – CRC error on received data, transmitter on longer than was needed to send the data, missed packet error (i.e., a packet on the coax was missed because there were no empty buffers in memory), and memory error in which the memory did not respond (handshake) to a memory cycle request.

Buffer Management

A key feature of the LANCE and its on board DMA channel is the flexibility and speed of communication between the LANCE and the host microprocessor through common memory locations. The basic organization of the buffer management is a circular queue of tasks in memory called descriptor rings as shown in Figure 2. There are separate descriptor rings to describe transmit and receive operations. Up to 128 tasks may be queued up on a descriptor ring awaiting execution by the LANCE. Each entry in a descriptor ring holds a pointer to a data memory buffer and an entry for the length of the data buffer. Data buffers can be chained or cascaded in order to handle a long packet in multiple data buffer areas. The LANCE searches the descriptor rings in a "look ahead manner" to determine the next empty buffer in order to chain buffers together or to handle back to back packets. As each buffer is filled, an "own" bit is reset allowing the host processor to empty this buffer.

LANCE Interface

CSR bits such as ACON, BCON, and BSWP are used for programming the pin functions used for different interfacing schemes. For example, ACON is used to program the polarity of the Address Strobe signal (ALE/$\overline{AS}$).

BCON is used for programming the pins for handling either the BYTE/$\overline{WORD}$ method for addressing word organized, byte addressable memories where the BYTE signal is decoded along with the least significant address bit to determine upper or lower byte, or an explicit scheme in which two signals labeled as BYTE MASK (BM0 and BM1) indicate which byte is addressed. When the BYTE scheme is chosen the BM1 pin can be used for performing the function $\overline{BUSACKO}$.

BCON is also used to program pins for different DMA modes. In a daisy chain DMA scheme, 3 signals ($\overline{BUSRQ}$, $\overline{HLDA}$, $\overline{BUSACKO}$), are used. In systems using a DMA controller for arbitration, only $\overline{HOLD}$ and $\overline{HLDA}$ are programmed by BCON.

All data transfers from the LANCE in the Bus Master mode are timed by ALE, $\overline{DAS}$ and $\overline{READY}$. The automatic adjustment of the LANCE cycle by the $\overline{READY}$ signal allows synchronization with variable cycle time memory due either to memory refresh or to dual port access. Bus cycles are a minimum of 600 nsec in length and can be increased in 200 nsec increments.

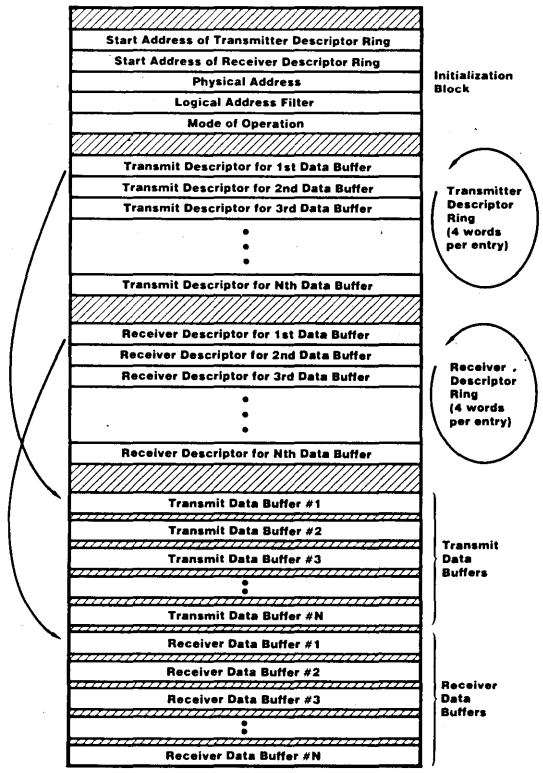


Figure 2. LANCE/Processor Memory Interface

MMC-105

Read Sequence

The read cycle is begun by valid addresses being placed on DAL_{00}-DAL_{15} and A_{16}-A_{23}. The BYTE MASK signals are placed valid to indicate a word, upper byte or lower byte memory reference and READ indicates the type of cycle. ALE or AS are pulsed and the trailing edge of either can be used to latch addresses. DAL_{00}-DAL_{15} go into a 3-state mode and DAS falls low to signal the beginning of the memory access. The memory responds by placing $\overline{READY}$ low to indicate that the DAL lines have valid data. The LANCE then latches memory data on the rising edge of $\overline{DAS}$ which in turn ends the memory cycle and $\overline{READY}$ returns high.

The bus transceiver controls, $\overline{DALI}$ and $\overline{DALO}$, are used to control the bus transceivers. $\overline{DALI}$ signals to strobe data toward the LANCE and $\overline{DALO}$ signals to strobe data or addresses away from the LANCE. During a read cycle $\overline{DALO}$ goes inactive to avoid "spiking" of the bus transceivers.

Write Sequence

The write cycle is very similar except that the DAL_{00}-DAL_{15} lines change from containing addresses to data after ALE or $\overline{AS}$ go inactive $\overline{DAS}$ goes active after data is valid on the bus. Data to memory is held valid after $\overline{DAS}$ goes inactive.

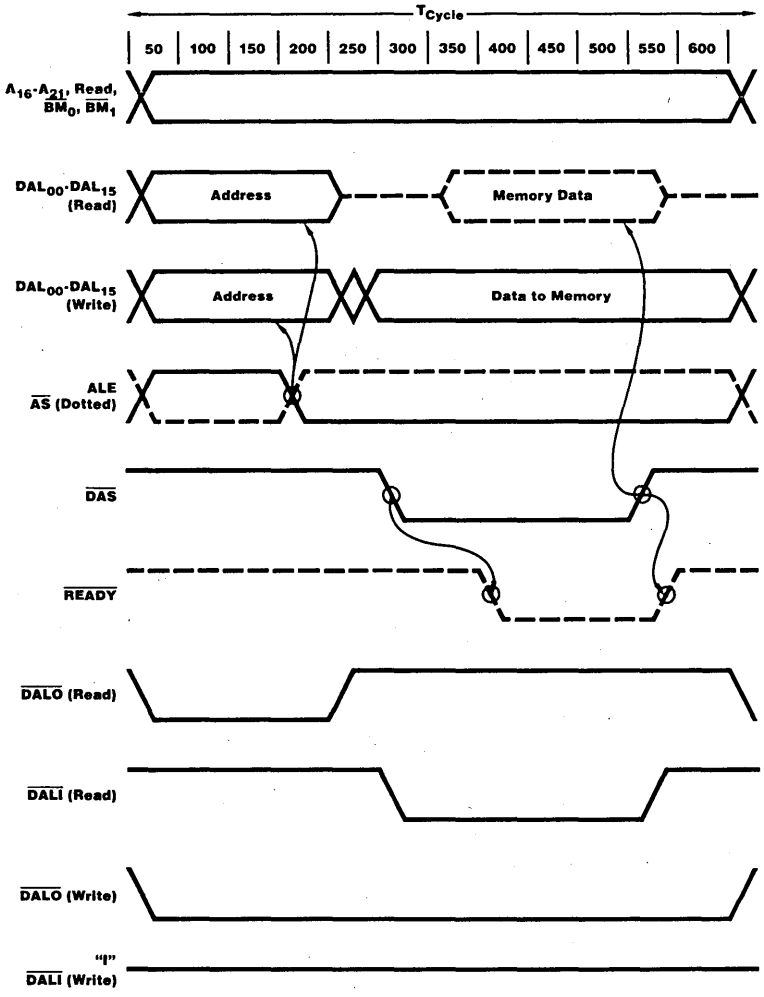


Figure 3. Bus Master Timing

MMC-110

COMMUNICATIONS
Am7990 Family Ethernet Node
IN DEVELOPMENT

Am7991
Serial Interface Adapter (SIA) IMOX

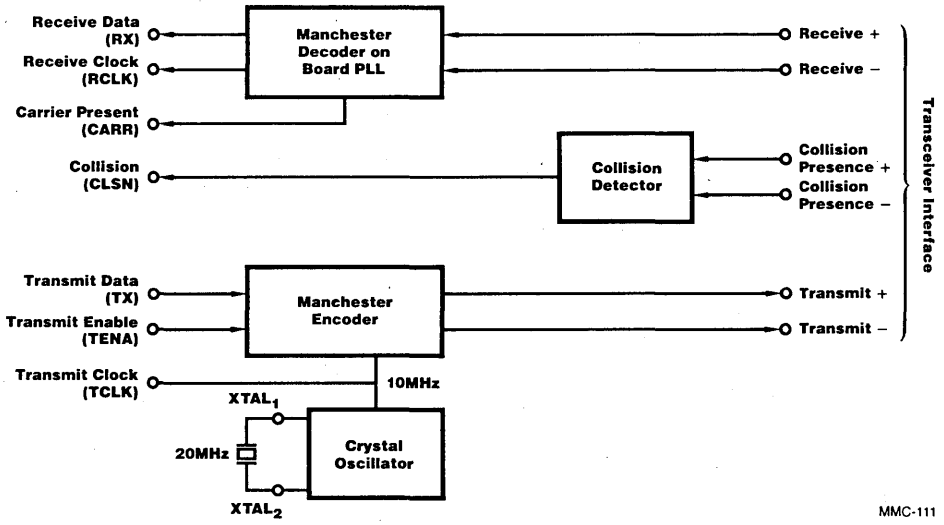
- Complete compatibility with Ethernet specifications
- Manchester encoding/decoding with phase locked loop
- Single 5V power supply
- TTL compatible inputs
- Differential transmit transceiver cable drive
- Transmit clock may be derived from external 20MHz oscillator or TTL level signal

FUNCTIONAL DESCRIPTION

The Am7991 Serial Interface Adapter (SIA) interfaces the Local Area Network Controller for Ethernet (LANCE) with a standard Ethernet transceiver cable. The SIA provides node data and clock encoding/decoding functions using standard Manchester code. The SIA is compatible with transceiver signalling detailed in the Ethernet specification. (Version 1)

BLOCK DIAGRAM

Serial Interface Adaptor (SIA)



Transmit Mode

The Manchester Encoder takes the TTL TRANSMIT DATA (TX) and TRANSMIT ENABLE (TENA) signals from the LANCE and creates the Manchester encoded differential signals TRANSMIT+ and TRANSMIT– to drive the transceiver interface. An external 20MHz crystal oscillator or TTL signal may be used to drive the encoder and to provide transmit clock (TCLK) to the LANCE.

Receive Mode

When data is on the Ethernet coax, the transceiver creates the differential signals RECEIVE+ and RECEIVE–. The Manchester decoder is synchronized to the incoming signals by the Phase Locked Loop. Clock and data are recovered and passed on to the LANCE as the TTL signals RECEIVE DATA (RX) and RECEIVE CLOCK (RCLK). In addition, the SIA creates the signal CARRIER PRESENT (CARR) while it is receiving data from the cable to indicate to the LANCE that receive data and clock are valid and available.

Collision Signalling

When a collision on the Ethernet cable is sensed by the Transceiver, it will create the differential signals COLLISION PRESENCE+ and COLLISION PRESENCE–. These inputs are conditioned to produce the TTL Collision Signal (CLSN) for the LANCE.

IMOX™ High Performance IMplanted OXide
Isolated Bipolar Process

AMERICAN MICROSYSTEMS, INC.

S2559E/F/G/H

DTMF TONE GENERATOR

Features

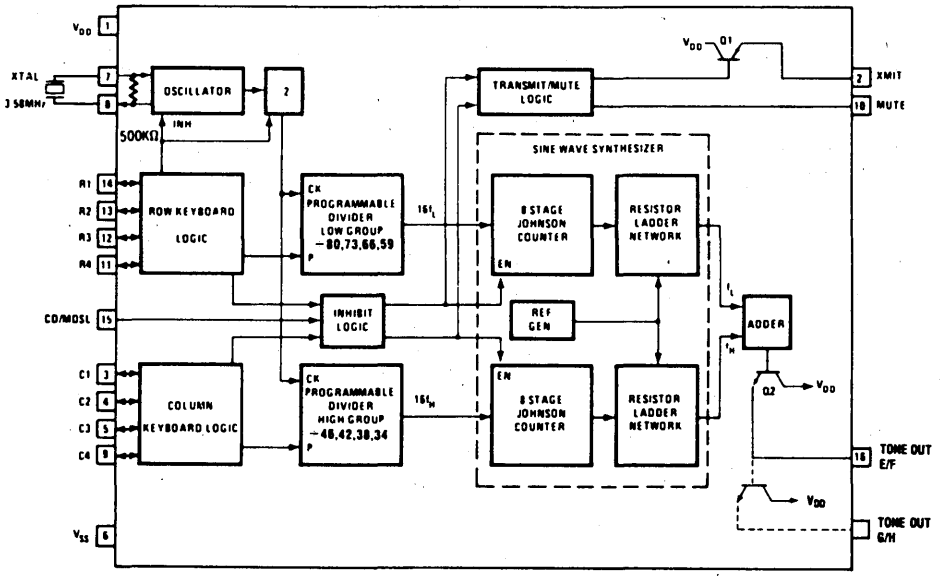
- ☐ Low Output Tone Distortion: 7%
- ☐ Wide Operating Supply Voltage Range: 2.5 to 10 Volts
- ☐ Oscillator Bias Resistor On-Chip
- ☐ Can be Powered Directly from Telephone Line or from Small Batteries
- ☐ Interfaces Directly to a Standard Telephone Push-Button or Calculator Type X-Y Keyboard
- ☐ Four Options Available on Pin 15:
  - Bipolar Output
    - E: Mode Select
    - F: Chip Disable
  - Darlington Output
    - G: Mode Select
    - H: Chip Disable

General Description

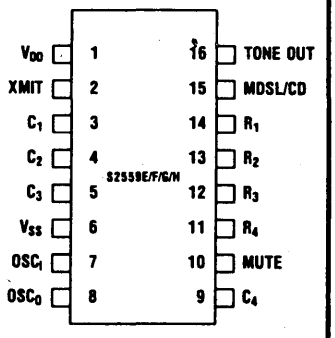
The S2559E, F, G and H are improved members of the S2559 Tone Generator Family. The new devices feature extended operating voltage range, lower tone distortion, and an on-chip oscillator bias resistor. The S2559E and F are pin and functionally compatible with the S2559C and D, respectively.

The S2559 G and H are identical to the E and F, except that there is a Darlington amplifier configuration on the tone out pin, rather than a single bipolar transistor as shown in the block diagram. In many applications this eliminates the need for a transistor in the telephone circuit. Tone distortion in the telephone is also likely to be lower.

Block Diagram



Pin Configuration



LINEAR

American Microsystems, Inc.

AMERICAN MICROSYSTEMS, INC.

S2561A/S2561C

TONE RINGER

Features

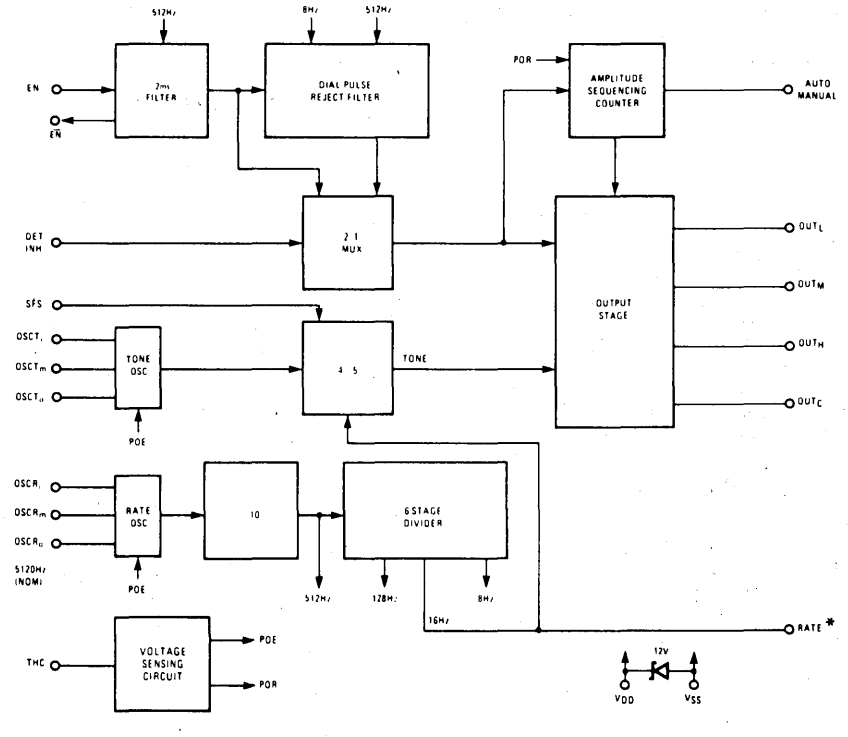
- ☐ CMOS Process for Low Power Operation
- ☐ Operates Directly from Telephone Lines with Simple Interface
- ☐ Also Capable of Logic Interface for Non-Telephone Applications
- ☐ Provides a Tone Signal that Shifts Between Two Predetermined Frequencies at Approximately 16Hz to Closely Simulate the Effects of the Telephone Bell
- ☐ Push-Pull Output Stage Allows Direct Drive, Eliminating Capacitive Coupling and Provides Increased Power Output
- ☐ 50mW Output Drive Capability at 10V Operating Voltage
- ☐ Auto Mode Allows Amplitude Sequencing such that the Tone Amplitude Increases in Each of the First Three Rings and Thereafter Continues at the Maximum Level
- ☐ Single Frequency Tone Capability

General Description

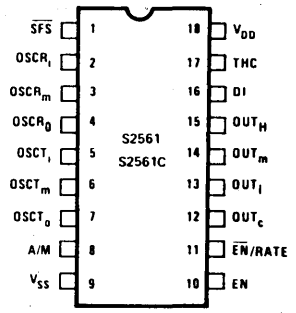
The S2561 Tone Ringer is a CMOS integrated circuit that is intended as a replacement for the mechanical telephone bell. It can be powered directly from the telephone lines with minimum interface and can drive a speaker to produce sound effects closely simulating the telephone bell.

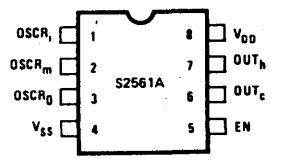
Data subject to change at any time without notice. These sheets transmitted for information only.

Block Diagram



Pin Configuration





LINEAR

American Microsystems, Inc.

AMERICAN MICROSYSTEMS, INC.

S2563

REPERTORY DIALER

Features

- ☐ Specifically Designed for Telephone Line Powered Applications
- ☐ CMOS Process Achieves Low Power Operation
- ☐ 8 or 16 Digit Number Capability (Pin Programmable)
- ☐ Dial Pulse and Mute Output
- ☐ Tone Outputs Obtained by Interfacing With Standard AMI S2559 Tone Generator
- ☐ Two Selections of Dial Pulse Rate
- ☐ Two Selections of Inter-Digit Pause
- ☐ Two Selections of Mark/Space Ratio
- ☐ Memory Storage of 29 8-Digit Numbers or 16-Digit Numbers with Standard AMI S5101 RAM
- ☐ 16-Digit Memory for Input Buffering and for Redial with Access Pause Capability
- ☐ Accepts the Standard Telephone DPCT Keypad or SPST Switch X-Y Matrix Keyboards; Also Capable of Logic Interface
- ☐ Can Use Standard 3×4 or 4×4 Keyboards
- ☐ Inexpensive, but Accurate R-C Oscillator Design
- ☐ BCD Output with Update for Single Digit Display

General Description

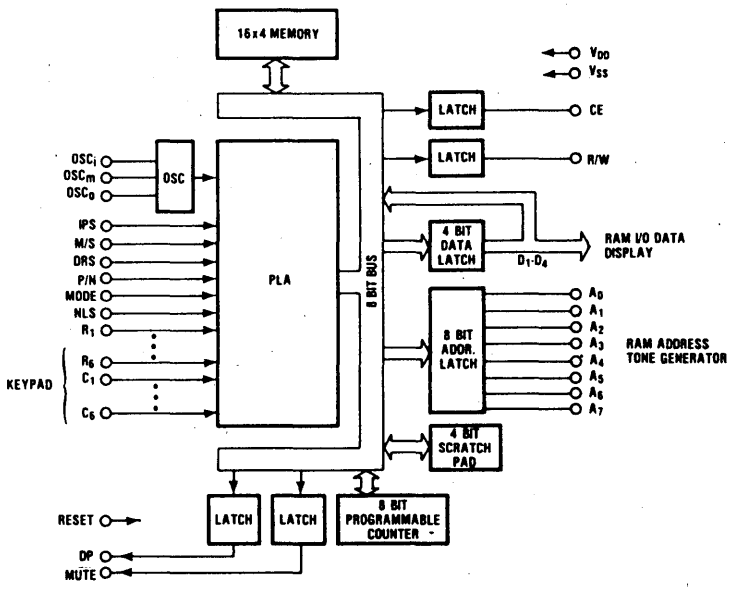
The S2563 is an improved version of the S2562 repertory dialer and can replace the S2562 in existing applications using local power. It is however specifically designed for applications that will only use telephone line power. To achieve this following changes were made to the S2562 design.

a. $\overline{PF}$ output was replaced by a level reset input which allows the device to be totally powered down in the on-hook state of the telephone.

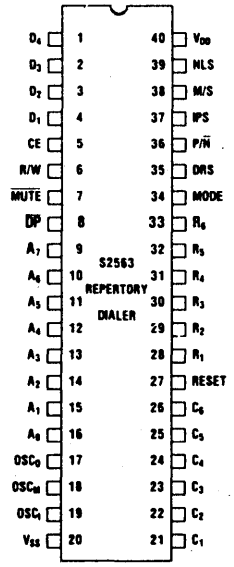
b. To reduce power consumption in the associated S5101 memory in the standby mode, the interface was changed so that its CE_2 input rather than the the $\overline{CE_1}$ input is controlled by the device.

c. Process was changed to a lower voltage CMOS process. Additionally a mark/space selection input (M/S) was added to allow selection of either 40/60 or 33/67 ratio. Provision was also made to allow the device to work with a standard 3×4 or 4×4 keyboard.

Block Diagram



Pin Configuration



AMERICAN MICROSYSTEMS, INC.

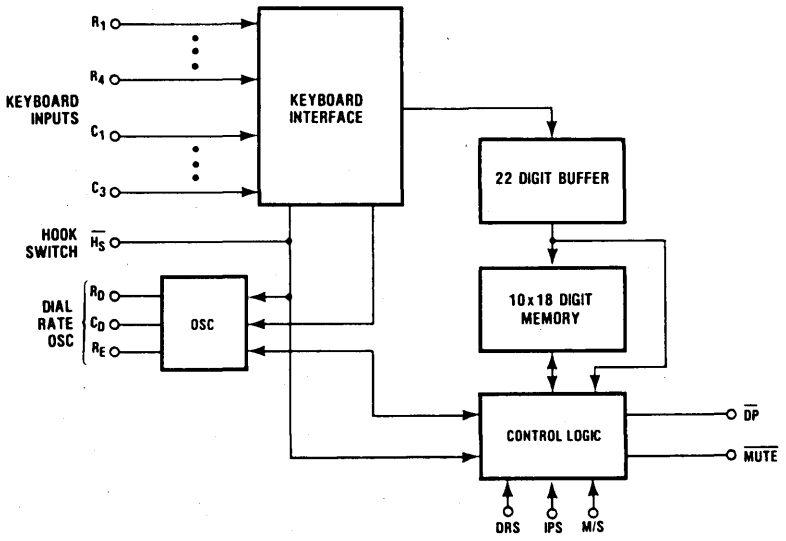
S25610

S25610 SINGLE CHIP REPERTORY DIALER

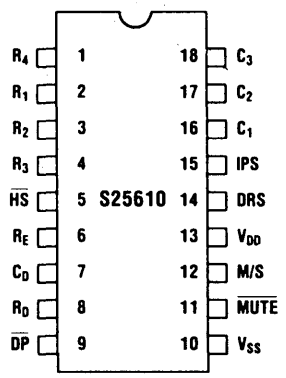
Features:

- ☐ Complete Pin Compatibility With S2560A Pulse Dialer Allowing Easy Upgrading of Existing Designs.
- ☐ Ten 18-Digit Number Memories Plus Last Number Redial (22 Digit) Memory On Chip.
- ☐ Low Voltage CMOS Process for Direct Operation From Telephone Lines.
- ☐ Inexpensive R-C Oscillator Design With Accuracy Better Than ±5% Over Temperature and Unit-Unit Variations.
- ☐ Independent Select Inputs for Variation of Dialing Rates (10pps/20pps), Mark/Space Ratio (33⅓ - 66⅔/40-60), Interdigit Pause (400ms/800ms).
- ☐ Can Interface With Inexpensive XY Matrix or Standard 2 of 7 Keyboard With Common. Also Capable of Logic Interface (Active High).
- ☐ Mute and Pulse Drivers On Chip.
- ☐ Call Disconnect by Pushing * and # Keys Simultaneously.

Block Diagram



Pin Configuration



LINEAR

American Microsystems, Inc.

AMERICAN MICROSYSTEMS, INC.

S28211A/B

SIGNAL PROCESSING PERIPHERAL

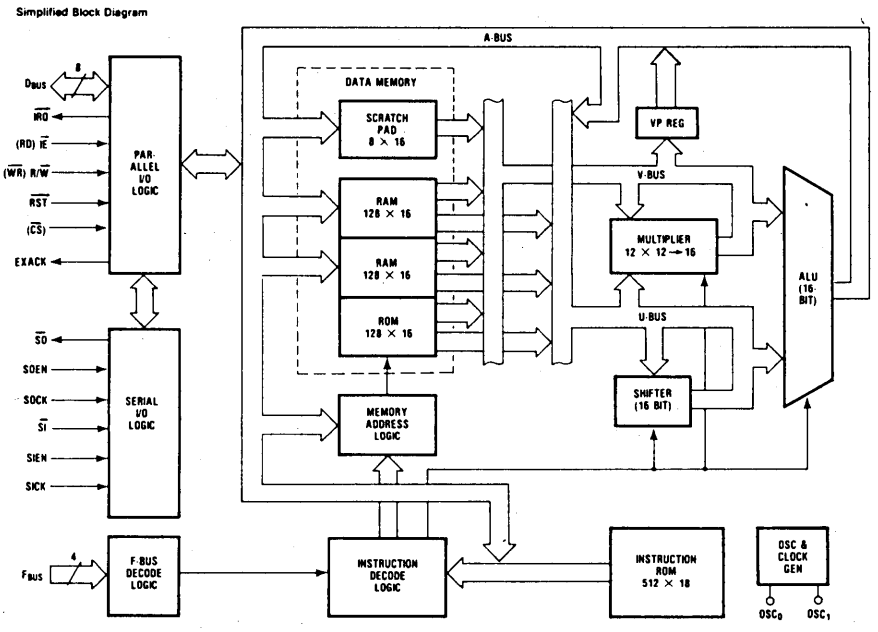
Features

- ☐ Single-Chip Programmable Digital Signal Processor
- ☐ May Be Customized (ROM Programmed) With Customer Generated Routines
- ☐ Self-Emulation Capability
- ☐ Standard Preprogrammed Processors Available
- ☐ Fetch/Multiply/Add/Store Cycle
- ☐ 512 Word × 18 Bit Instruction Memory
- ☐ Unique Three Port Data Memory 256 × 16 RAM/128 × 16 ROM
- ☐ 12 × 12 Pipelined Multiplier With 16 Bit Product
- ☐ 16 Bit Accumulator With Overflow Detect/Protect
- ☐ Double Buffered Asynchronous Serial I/O Port
- ☐ μP-Compatible I/O Port i.e. 6800 (A Version), 8080 (B Version), etc.

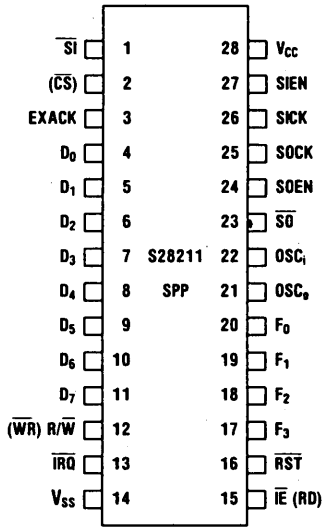
General Description

The S28211 is a single-chip microcomputer which has been optimized to execute digital signal processing algorithms commonly used in applications such as telecommunications speech processing, industrial process control instrumentation, etc. It may be used as a stand alone unit, or may be operated as a peripheral in a microprocessor based system. The latter configuration allows arrays of S28211s to be used together for increased processing throughput. The S28211's multi-bus, pipelined architecture and powerful multi-operation instructions make it possible to write very compact algorithms. This allows the available memory to be used efficiently and increases the execution speed of a given algorithm. The S28211 may be customized with user generated algorithms (Factory ROM Programmed).

Simplified Block Diagram



Pin Configuration



NOTE:
PIN FUNCTIONS IN PARENTHESIS APPLY ONLY FOR B VERSION

LINEAR

American Microsystems, Inc.

AMERICAN MICROSYSTEMS, INC.

S2814A

FAST FOURIER TRANSFORMER

Features

- ☐ Based on AMI's Signal Processing Peripheral Chip (S2811)
- ☐ Performs 32 Complex Point Forward or Inverse FFT in 1.3msec, Using Decimation in Frequency (DIF)
- ☐ Transform Expandable either by Using Multiple S2814As (for Minimum Processing Time) or by a Single S2814A (for Minimum Hardware)
- ☐ Operates with any 8 or 16 Bit Microprocessor, including S6800 and S9900. Optional DMA Controller Increases Speed
- ☐ All Data I/O Carried Out on Microprocessor Data Bus
- ☐ Basic Resolution of 57dB. Optional Conditional Array Scaling (CAS) Routine Increases Dynamic Range to 70dB
- ☐ Optional Windowing Routine Incorporated to Permit Use of Arbitrary Weighting Function
- ☐ Coefficient Generation On Chip, with Rotation Algorithm for Transform Expansion up to 512 Points
- ☐ Optional Power Spectrum Computation

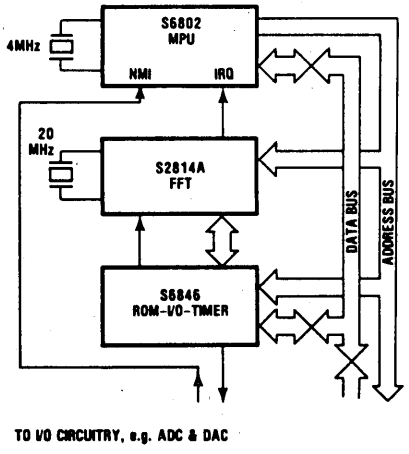
General Description

The AMI S2814A Fast Fourier Transformer is a preprogrammed version of the S2811 Signal Processing Peripheral. For further information on the internal operation of the S2811, please refer to the S2811 Advanced Product Description. It calculates FFTs and IFFTs using a decimation in frequency (DIF) technique for minimum distortion. The S2814A calculates a 32 complex point FFT using internally generated coefficients in a single pass. A coefficient rotation algorithm allows larger FFTs to be implemented (in blocks of 32 points). This implementation may be carried out by successive passes of the data through the two main routines in the S2814A, allowing larger transforms to be carried out with a single S2814A. Alternatively, an array of S2814As may be used to increase the transformation speed by parallel processing.

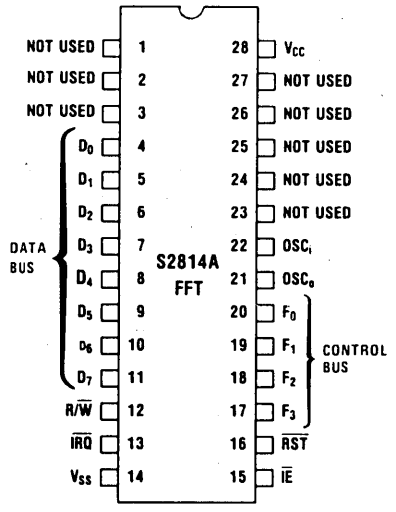
The word length used in the S2814A gives the transformed data a resolution of up to 57dB, but the total dynamic range can be increased up to 70dB by using the Conditional Array Scaling (CAS) routine incorporated.

The S2814A is intended to be used in a microprocessor system (see Block Diagram), using an 8 or 16 bit microprocessor, ROM, RAM and an optional DMA Controller or Address Generator.

Block Diagram: Minimum System Configuration



Pin Configuration



LINEAR

American Microsystems, Inc.

AMERICAN MICROSYSTEMS, INC.

S2815

DIGITAL FILTER/UTILITY PERIPHERAL

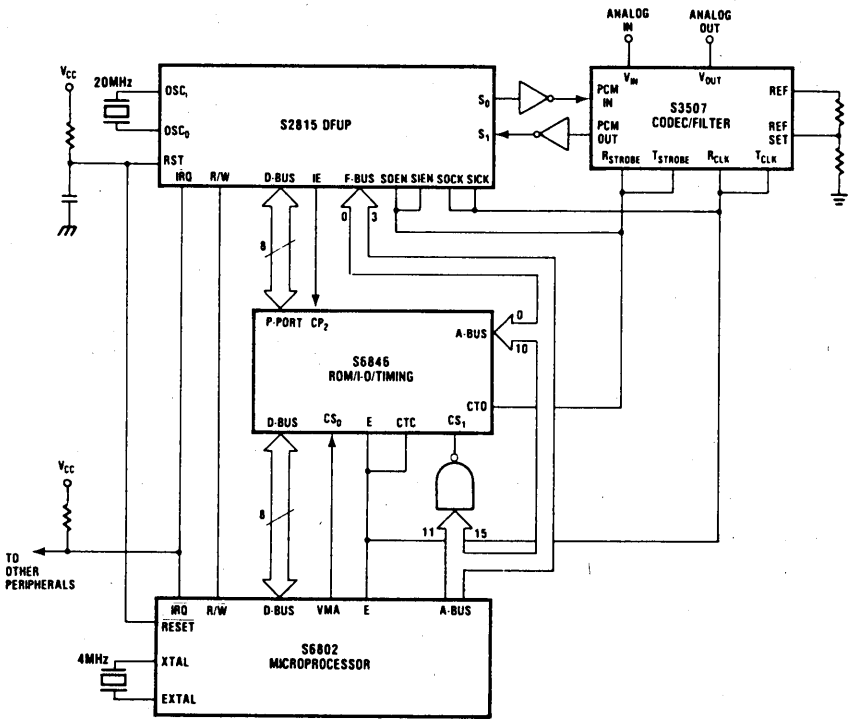
Features

- ☐ S2811 Signal Processing Peripheral Programmed With Filter and Utility Routines
- ☐ Microprocessor Compatible Interface Plus Asynchronous Serial Interface
- ☐ Two Independent 32 Tap Transversal Filter Routines, Cascadable into a Single 64 Tap Filter
- ☐ Two Recursive (biquadratic) Filters Providing a Total of 16 Filter Sections
- ☐ Computation Functions: Two Integrating, Two Rectifying, Squaring, and Block Multiply Routines
- ☐ Conversion Functions: μ255 Law-to-Linear, Linear-to-μ255 Law, and Linear-to-dB Transformations
- ☐ Generator Functions: Sine and Pseudo-Random Noise Patterns

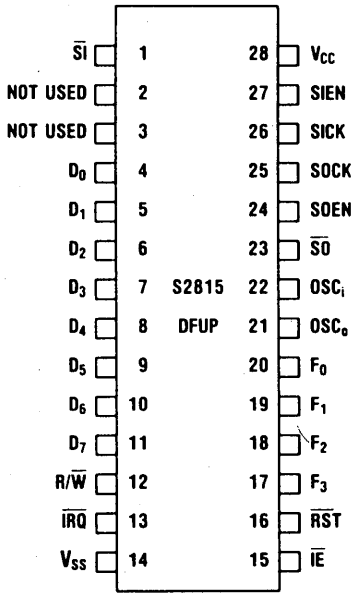
General Description

The AMI S2815 Digital Filter/Utility (DFUP) is a pre-programmed version of the S2811. Architectural and internal operating details of the S2811 may be found in the S2811 Advanced Product Description. The S2815 has been programmed with a collection of filter, computational, conversion, and generator routines which may be selected individually, or cascaded under control of the host processor.

Typical System Configuration



Pin Configuration



AMERICAN MICROSYSTEMS, INC.

S3506/S3507/S3507A

CMOS SINGLE CHIP μ-LAW/A-LAW COMBO CODECS WITH FILTERS

Features

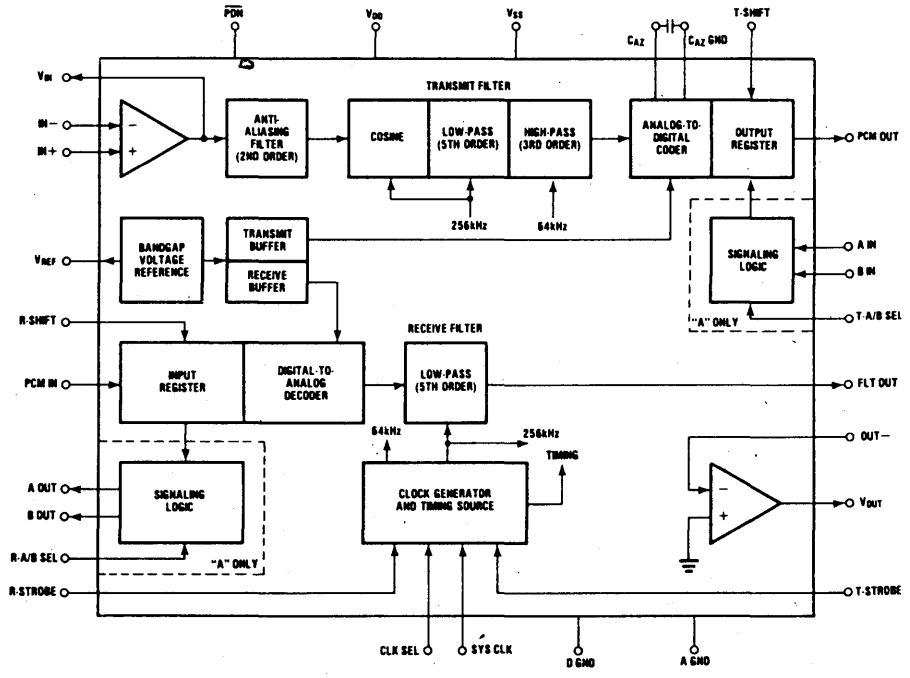
- ☐ Independent Transmit and Receive Sections With 75dB Isolation
- ☐ Low Power CMOS 80mW (Operating) 8mW (Standby)
- ☐ Stable Voltage Reference On-Chip
- ☐ Meets or Exceeds AT&T D3, and CCITT G.711, G.712 and G.733 Specifications
- ☐ Input Analog Filter Eliminates Need for External Anti-Aliasing Prefilter
- ☐ Input/Output Op Amps for Programming Gain
- ☐ Output Op Amp Provides ±3.1V into a 1200Ω Load or Can Be Switched Off for Reduced Power (70mW)
- ☐ Special Idle Channel Noise Reduction Circuitry for Crosstalk Suppression
- ☐ Encoder has Dual-Speed Auto-Zero Loop for Fast Acquisition on Power-Up
- ☐ Low Absolute Group Delay = 450μsec. @ 1kHz

General Description

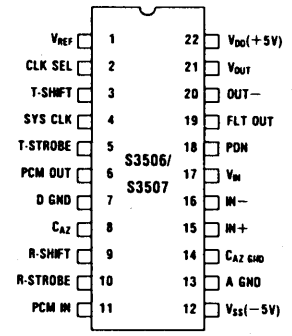
The S3506 and S3507 are monolithic silicon gate CMOS Companding Encoder/Decoder chips designed to implement the per channel voice frequency Codecs used in PCM systems. The chips contain the band-limiting filters and the analog↔digital conversion circuits that conform to the desired transfer characteristic. The S3506 provides the European A-Law companding and the S3507 provides the North American μ-Law companding characteristic.

These circuits provide the interface between the analog signals of the subscriber loop and the digital signals of the PCM highway in a digital telephone switching system.

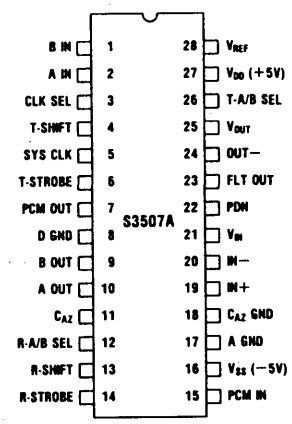
Block Diagram



Pin Configuration (22 Pin)



Pin Configuration (28 Pin)



LINEAR

American Microsystems, Inc.

DTMF BANDSPLIT FILTER

Introduction

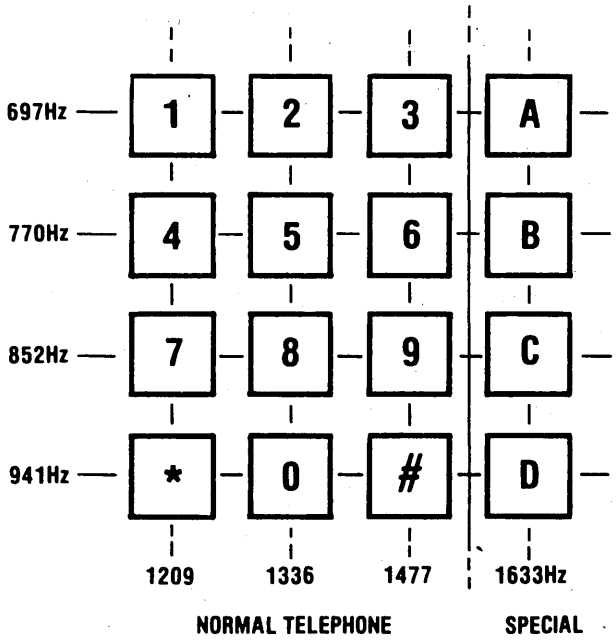
DTMF (Dual-Tone, Multi-Frequency) or Touch-Tone®, is widely used for controlling and signaling. Bell System originally designed this signaling method to provide customers with a more rapid, convenient means of transmitting digits of the called party phone to the central office. Now, it is used in many other applications.

Pushing a button produces 2 tones simultaneously. It is this particular set of tones that the DTMF Receiver at the telephone central office (or exchange) uses to determine which button was pushed (see Figure 1). By analyzing the series of tones sent, the receiver determines what number was dialed and the switching equipment then acts accordingly.

The requirements for accuracy and reliability in the telephone network have been well defined. As a result a DTMF Receiver for a central office must have high quality and reliability.

The performance of DTMF in the telephone network is well appreciated by designers of other systems evidenced by the familiar Touch-Tone® pad present on radios, remote credit card terminals, electronic bank tellers, etc. These applications take advantage of the end-to-end capability inherent in the DTMF method. The tones, like voice, go from the originating end to the receiving end without significant degradation.

Figure 1. DTMF Keyboard



AMERICAN MICROSYSTEMS, INC.

S3526A/S3526B

TUNEABLE BANDPASS/NOTCH FILTER

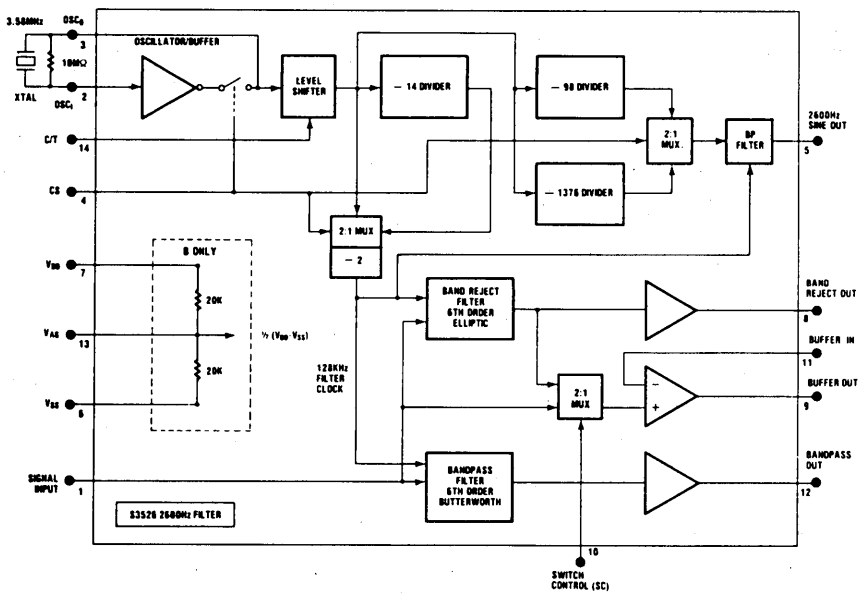
Features

- ☐ **Provides Band Pass and Band Reject Outputs**
- ☐ **Uses 3.58MHz TV Crystal or 256KHz Clock as Timebase for 2600Hz Center Frequency**
- ☐ **Generates 2600Hz Sinewave**
- ☐ **Single or Dual Supply Operation**
- ☐ **Buffer Drives 600Ω Loads**
- ☐ **The bandpass/notch frequency can be shifted from 2600Hz by using other clock frequencies.**

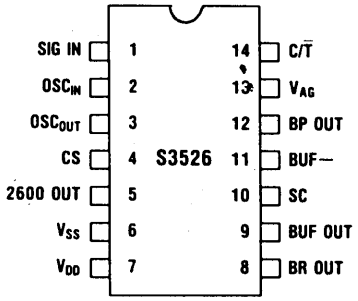
General Description

The S3526 Single Frequency (SF) Filter is a 14-pin monolithic CMOS circuit designed to implement a precision SF tone receiver. When used with an inexpensive 3.58 MHz TV crystal or a 256kHz clock input it provides sharp 2600 Hz bandpass and notch filters as well as a 2600Hz sine wave output. The 256kHz clock can be at CMOS or TTL levels. A change in the crystal (or clock) frequency from 3.58MHz (256kHz) will proportionately change the bandpass, notch and sine wave output frequencies. The S3526A is intended for dual +5V and −5V power supply operation, whereas the S3526B is intended for a single +10V supply.

Block Diagram



Pin Configuration



LINEAR

American Microsystems, Inc.

AMERICAN MICROSYSTEMS, INC.

S3610

LPC-10 SPEECH SYNTHESIZER WITH ON-CHIP 20K SPEECH DATA ROM

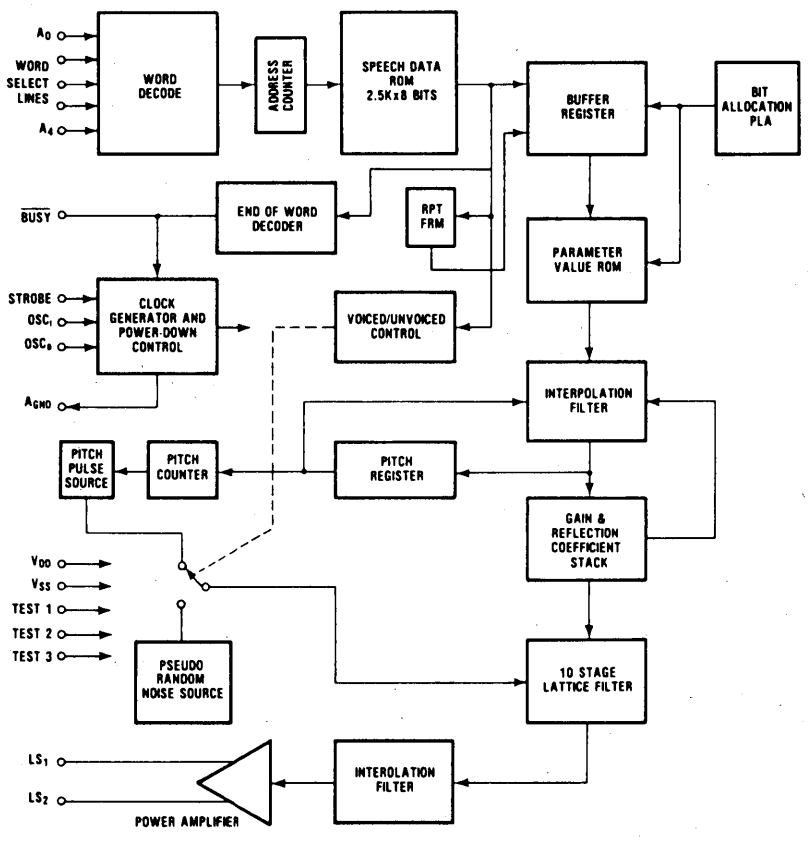
Features

- ☐ Simple Digital Interface
- ☐ CMOS Switched-Capacitor Filter Technology
- ☐ Automatic Powerdown
- ☐ Single Power Supply Operation
- ☐ Direct Loudspeaker Drive
- ☐ 30mW Audio Output
- ☐ 20K Bits Speech ROM
- ☐ Low Data Rate
- ☐ Up to 32 Word Vocabulary

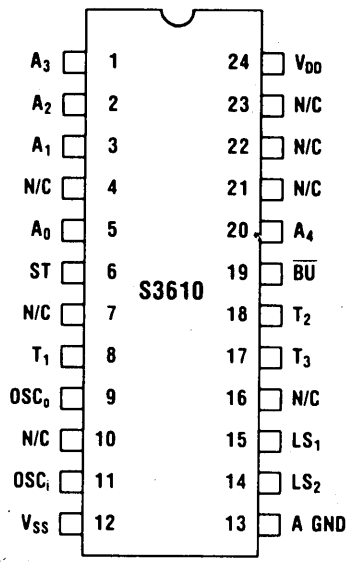
General Description

The S3610 LPC-10 Speech Synthesizer generates speech of high quality and intelligibility from LPC (Linear Predictive Coding) data stored in an internal 20K bit ROM. The simple digital interface consists of 5 word-select lines, a strobe input to load the address data and initiate operation, and a busy output signal. At the end of enunciation the chip automatically goes into the power-down mode until a new word select address is strobed in. The data rate from the speech ROM into the synthesizer is 2.0K bits/sec max. Typically the average data rate will be reduced to about 1.2K bits/sec. by means of the data rate reduction techniques used internally, giving about 17 seconds of speech from the ROM data. The 5 word-select lines allow a maximum vocabulary of 32 words.

Block Diagram



Pin Configuration



N/C = NO CONNECTION

LINEAR

American Microsystems, Inc.

AMERICAN MICROSYSTEMS, INC.

S3620

LPC-10 SPEECH SYNTHESIZER

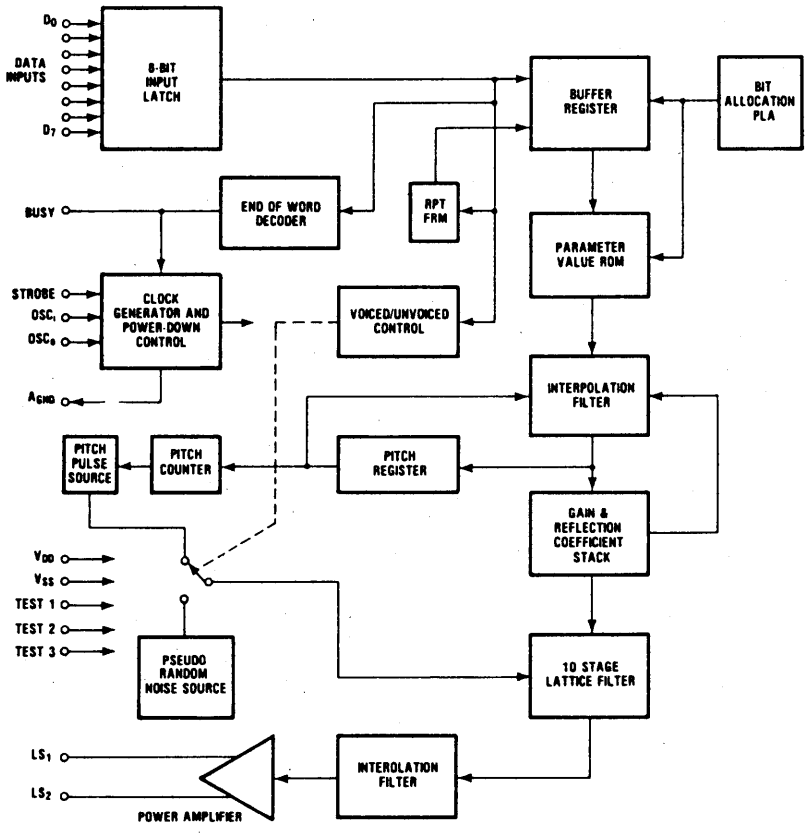
Features

- ☐ Simple Microprocessor Interface
- ☐ CMOS Switched-Capacitor Filter Technology
- ☐ Automatic Powerdown
- ☐ Single Supply Operation
- ☐ Direct Loudspeaker Drive
- ☐ 30mW Audio Output
- ☐ Low Data Rate

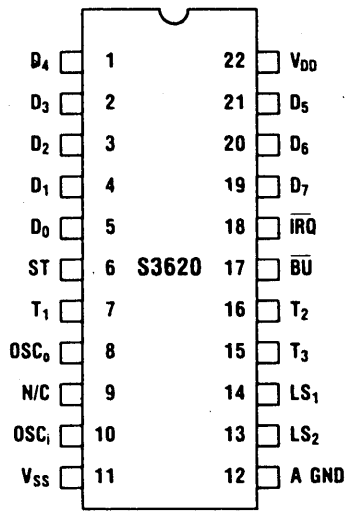
General Description

The S3620 LPC-10 Speech Synthesizer generates speech of high quality and intelligibility from LPC (Linear Predictive Coding) data stored in an external memory. The digital interface circuitry is fully microprocessor compatible and allows the processor to load the data with or without a DMA controller. The loading takes place on a handshake basis, and in the absence of a response from the processor the synthesizer automatically shuts down and goes into the powerdown mode. A busy signal allows the processor to sense the status of the synthesizer. The input data rate is 2.0K bits/sec. max., but typically the average data rate will be reduced to about 1.4K bits/sec. by means of the data rate reduction techniques used internally.

Block Diagram



Pin Configuration



N/C = NO CONNECTION

LINEAR

American Microsystems, Inc.

AMERICAN MICROSYSTEMS, INC.

S3630A/B

128K (16K×8) BIT NMOS ROM

Features

- ☐ Single +5V Power Supply
- ☐ Directly TTL Compatible Inputs
- ☐ Directly TTL Compatible Outputs, Three State on S3630A
- ☐ Low Power: Supply Current-20mA Max.
- ☐ Power Down Capability (S3630A)

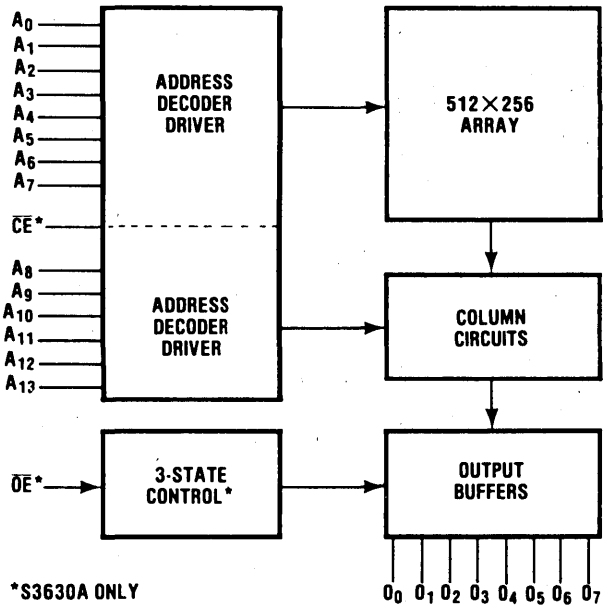
General Description

The S3630A/B is a high density 131072 bit NMOS mask programmable Read Only Memory. The device is fully TTL compatible and the organization as 16K×8 bits makes it very suitable for use in microprocessor systems. It is available in both 6μsec and 10μsec versions.

The S3630 is available in two pin configurations. The S3630A has the industry standard pinout (28-pin package). The S3630B has a minimum pin configuration, allowing it to be packaged in a 24-pin DIL pack, saving valuable board space where this configuration is usable, as well as reducing costs.

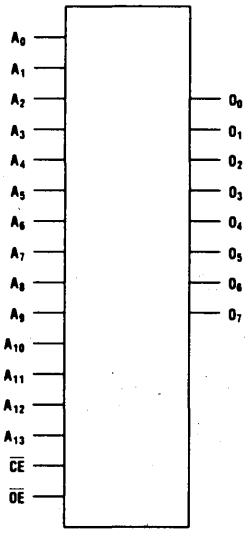
The S3630 is manufactured in a high density silicon gate, depletion load, N-channel process. Its high data capacity makes it extremely suitable for use in speech synthesis systems.

Block Diagram



*S3630A ONLY

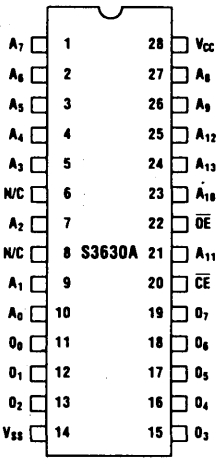
Logic Symbol



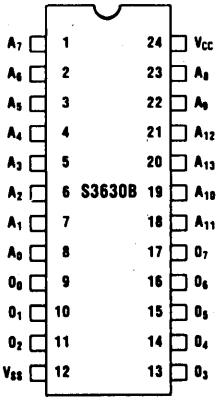
Pin Names

A_0-A_{13}	Address Inputs
O_0-O_7	Data Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable

Pin Configuration



N.C. = NO CONNECTION



LINEAR

American Microsystems, Inc.

ANALOG DEVICES

Ultra Low Drift BIFET Operational Amplifiers

AD547/AD647

FEATURES

- Ultra Low Drift (1μV/°C)
- Low Offset Voltage (0.25mV)
- Low Input Bias Currents (25pA)
- Low Quiescent Current
- Low Noise (2μV p-p)
- High Open Loop Gain (110dB)
- Matched Offset Voltage – AD647
- Matched Offset Voltage Over Temperature – AD647
- Matched Bias Current – AD647
- Crosstalk 124dB at 1kHz
- Low Total Harmonic Distortion

PRODUCT DESCRIPTION

The AD547 and AD647 are monolithic, FET input operational amplifiers combining the very low input bias current advantages of a BIFET op amp with offset and drift performance previously available only in high quality bipolar amplifiers.

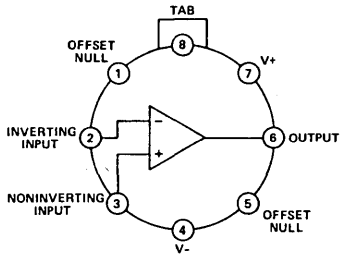
The exclusive Analog Devices laser wafer trim process trims both the input offset voltage and offset voltage drift to levels far lower than any competing BIFET amplifier (1mV, 5μV/°C-J versions, 0.25mV, 1μV/°C–L versions).

In addition, the offset voltage is laser trimmed to less than 0.25mV and matched to 0.25mV for the AD647L, 0.5mV and matched to 0.25mV for the AD647K.

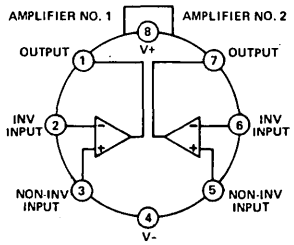
The AD547 offers the lowest guaranteed input bias currents of any BIFET amplifier with 50pA max for the J grade and 25pA max for the L grade. The AD647 offers matched bias currents that are significantly lower than currently available monolithic dual FET input operational amplifiers: 35pA max, matched to 15pA for the AD647K and L; 75pA max, matched to 25pA for the AD647J and S.

PRODUCT HIGHLIGHTS

1. Advanced laser wafer trimming techniques reduce offset voltage drift to 1μV/°C max and reduce offset voltage to only 0.25mV max on the AD547L.



AD547 SINGLE VERSION

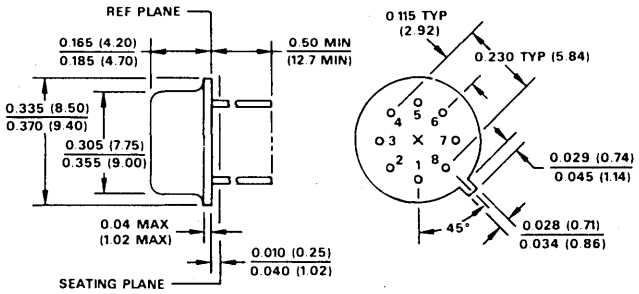


AD647 DUAL VERSION

2. Analog Devices BIFET processing provides 25pA max (10pA typical) bias currents specified after 5 minutes of warm-up.
3. Low voltage noise, high open loop gain and outstanding offset performance make the series true precision BIFET amplifiers.
4. The AD647 dual has tight matching specifications to ensure high performance, eliminating the need to match individual devices.
5. Laser-wafer-trimming reduces offset voltage to as low as 0.25mV max and matched side to side to 0.25mV (AD647L), thus eliminating the need for external nulling.
6. The standard dual amplifier pin out allows the AD647 to replace lower performance duals without redesign.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



TO-99

ORDERING GUIDE

Model	Initial Offset Voltage	Offset Voltage Drift	Temperature Range
AD547JH	1.0mV	5μV/°C	0 to +70°C
AD547KH	0.5mV	2μV/°C	0 to +70°C
AD547LH	0.25mV	1μV/°C	0 to +70°C
AD547SH	0.5mV	5μV/°C	-55°C to +125°C
AD647JH	1.0mV	10μV/°C	0 to +70°C
AD647KH	0.5mV	5μV/°C	0 to +70°C
AD647LH	0.25mV	2μV/°C	0 to +70°C
AD647SH	0.5mV	10μV/°C	-55°C to +125°C

LINEAR

Analog Devices

ANALOG DEVICES

Low Offset, Fast Settling Video Operational Amplifier

HOS-060

FEATURES
<1mV V_{OS}
Low Drift
80ns Settling to 0.1%; 200ns to 0.01%
100mA Output @ ±10V

APPLICATIONS
D/A Current Converter
Video Pulse Amplifier
CRT Deflection Amplifier
Wideband Current Booster

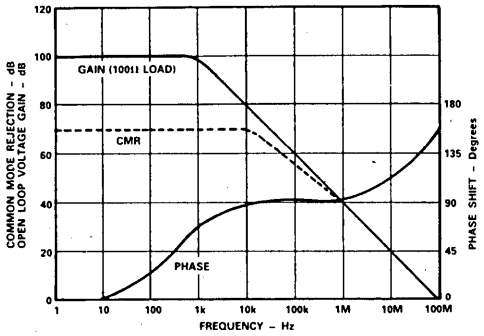


Figure 1. HOS-060 Frequency Response

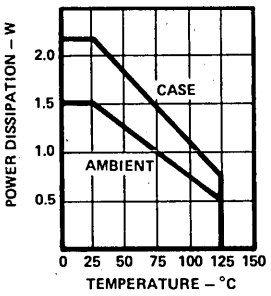


Figure 2. Power Derating

GENERAL DESCRIPTION

The HOS-060 Operational Amplifier is an extension of the proven hybrid technology used in the HOS-050 series of op amps.

The FET input and high-performance characteristics, including wide bandwidth and fast settling, make it useful for a variety of applications in the processing of video signals.

Recent innovations in circuit design have been incorporated into the HOS-060 to make it extremely useful to the designer who needs outstanding performance in current boosting, voltage amplification, impedance matching, or a multiplicity of other high-frequency requirements.

Voltage offset and its temperature coefficient have been dramatically improved in the HOS-060; offset is as low as on most monolithic op amps, despite being a thick-film hybrid.

These improvements, moreover, have been accomplished without any sacrifice in the other parameters which characterize its outstanding performance in video applications.

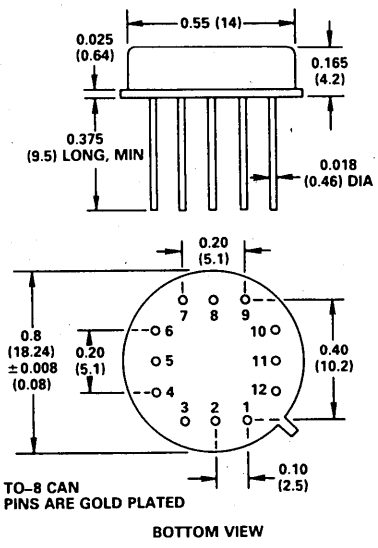
The HOS-060 op amp is pin-for-pin compatible with its forerunner HOS-050 and is useable in the same diversity of video requirements. The reader is strongly urged to refer to the six-page data sheet for the HOS-050 op amp to obtain additional insight and details on potential uses for the HOS-060.

The HOS-060 Operational Amplifier is housed in an industry standard TO-8 metal can and operates over a case temperature range of −55°C to +125°C; the model number for the standard unit is HOS-060SH.

For units processed to MIL-STD-883, Method 5008, specify model number HOS-060SH/883.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



LINEAR

Analog Devices

FEATURE SELECTION CHART

		GENERAL PURPOSE									HIGH ACCURACY							
											LOW V_{OS} DRIFT							
		FET INPUT						WIDEBAND							FET INPUT			
		AD503	AD506	AD540	AD542	AD642	AD644	AD544	AD101 Series	AD741	AD504	AD510	AD OP-07	AD517	AD545	AD547	AD647	AD515
Monolithic Technology	Bipolar Input								•	•	•	•	•	•		•		
	J-FET			•	•			•									•	
	Dual J-FET					•	•											
Multi-Device Technology	Hybrid	•	•												•			•
	Module																	
High Open Loop Gain	≥100dB				•	•					•	•	•	•		•	•	
	≥140dB																	
High CMR	>100dB										•	•	•	•				
Low Offset Voltage	≤5mV		•		•	•	•	•	•	•	•	•	•	•	•	•	•	•
	≤1mV				•	•	•	•								•	•	
	≤50μV												•	•				
Low Offset V, vs. Temp	≤5μV/°C				•	•	•	•			•	•	•	•	•	•	•	
	≤1μV/°C															•	•	
	≤0.6μV/°C										•	•	•					
Low Bias Current	≤50pA	•	•	•	•	•	•	•							•	•	•	•
	≤5pA														•			•
	≤0.5pA																	•
Fast Settling	≤1μs to 0.1%						•	•										
	≤5μs to 0.01%						•	•										
Wideband (Unity Gain)	≥2MHz						•	•	•									
	≥10MHz																	
High Slew Rate	≥10V/μs						•	•	•									
	≥30V/μs																	
	≥100V/μs																	
	≥1000V/μs															•	•	
Low Noise (0.1 to 10Hz) 2μV p-p					•	•	•	•	•		•	•	•	•				
High Voltage Out	≥100V																	
High Current Out	≥20mA																	
Low Power	≤75mW				•	•	•	•	•	•					•	•	•	•
Second Source									•	•			•					
Temperature Range 0 to +70°C		•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
-25°C to +85°C									•									
-55°C to +125°C		•	•	•	•	•	•	•	•	•	•	•	•	•		•	•	
Dice Availability				•	•	•	•	•					•	•		•		

GENERAL PURPOSE BIPOLAR INPUT SPECIFICATIONS (typical @ V_S = ±15V, T_A = +25°C unless otherwise noted)

Model	Gain min	Output V/mA min	Unity Gain MHz	Slew Rate V/μs	V_{OS} mV max	$\Delta V_{OS}/\Delta T$ μV/°C max	I_b nA max	CMR dB min	Temp Range[1]	Package[2]
AD101A	50k	10/5	1.0 to 8.0	0.5 to 10	2.0	15	75	80	M	H
AD201A	50k	10/5	1.0 to 8.0	0.5 to 10	2.0	15	75	80	I	H,N
AD301A	25k	10/5	1.0 to 8.0	0.5 to 10	7.5	30	250	70	C	H,N
AD301AL	80k	10/5	1.0 to 10.0	0.25 to 9.0	1.0	5.0	30	90	C	H,N
AD108	50k	13/1.3	0.3 to 3.0	0.3 to 1.3	2.0	15	2.0	85	M	H
AD208	50k	13/1.3	0.3 to 3.0	0.3 to 1.3	2.0	15	2.0	85	I	H
AD308	25k	13/1.3	0.3 to 3.0	0.3 to 1.3	7.5	30	7.0	80	C	H
AD108A	80k	13/1.3	0.3 to 3.0	0.3 to 1.3	0.5	5.0	2.0	96	M	H
AD208A	80k	13/1.3	0.3 to 3.0	0.3 to 1.3	0.5	5.0	2.0	96	I	H
AD308A	80k	13/1.3	0.3 to 3.0	0.3 to 1.3	0.5	5.0	7.0	96	C	H
AD741	50k	10/5	1.0	0.5	5.0	–	500	70	M	H,N
AD741C	20k	10/5	1.0	0.5	6.0	–	500	70	C	H,N
AD741J	50k	10/10	1.0	0.5	3.0	20	200	80	C	H,N
AD741K	50k	10/5	1.0	0.5	2.0	15	75	90	C	H,N
AD741L	50k	10/5	1.0	0.5	0.5	5.0	50	90	C	H,N
AD741S	50k	10/10	1.0	0.5	2.0	15	75	80	M	H

NOTES
[1] C = 0 to +70°C, I = -25°C to +85°C, M = -55°C to +125°C
[2] H = TO-99 can, N = 8-pin mini DIP

GENERAL PURPOSE FET INPUT
SPECIFICATIONS (typical @ V_S = ±15V, T_A = +25°C unless otherwise noted)

Model	Gain min	Output V/mA min	Unity Gain MHz	Slew Rate V/µs	V_{OS} mV max	$\Delta V_{OS}/\Delta T$ µV/°C max	I_b pA max	CMR dB min	Temp Range[1]	Package[2]
AD503J	20k	10/5	1.0	3.0	50	75	15	70	C	H
AD503K	50k	10/5	1.0	3.0	20	25	10	80	C	H
AD503S	50k	10/5	1.0	3.0	20	50	10	80	M	H
AD506J	20k	10/5	1.0	3.0	3.5	75	15	70	C	H
AD506K	50k	10/5	1.0	3.0	1.5	25	10	80	C	H
AD506L	75k	10/5	1.0	3.0	1.0	10	5	80	C	H
AD506S	50k	10/5	1.0	3.0	1.5	50	10	80	M	H
AD540J	20k	10/5	1.0	6.0	50	75	50	70	C	H
AD540K	50k	10/5	1.0	6.0	20	25	25	70	C	H
AD540S	50k	10/5	1.0	6.0	20	50	25	70	M	H
AD542J	100k	10/5	1.0	3.0	2.0	20	50	76	C	H
AD542K	300k	10/5	1.0	3.0	1.0	10	25	80	C	H
AD542L	300k	10/5	1.0	3.0	0.5	5	25	80	C	H
AD542S	300k	10/5	1.0	3.0	1.0	15	25	80	M	H
AD544J	30k	10/5	2.0	13	2.0	20	50	74	C	H
AD544K	50k	10/5	2.0	13	1.0	10	25	80	C	H
AD544L	50k	10/5	2.0	13	0.5	5	25	80	C	H
AD544S	50k	10/5	2.0	13	1.0	15	25	80	M	H
AD547J	100k	10/5	1.0	3.0	1.0	5	50	76	C	H
AD547K	250k	10/5	1.0	3.0	0.5	2	25	80	C	H
AD547L	250k	10/5	1.0	3.0	0.25	1	25	80	C	H
AD547S	250k	10/5	1.0	3.0	0.5	5	25	80	M	H
AD642J	100k	10/5	1.0	3.0	2.0[3]	3.5mV[4]	75	76	C	H
AD642K	300k	10/5	1.0	3.0	1.0[3]	2.0mV[4]	35	80	C	H
AD642L	300k	10/5	1.0	3.0	0.5[3]	1.0mV[4]	35	80	C	H
AD642S (S/883B)	300k	10/5	1.0	3.0	1.0[3]	3.5mV[4]	75	80	M	H
AD644J	30k	10/5	2.0	13	2.0[3]	3.5mV[4]	75	76	C	H
AD644K	50k	10/5	2.0	13	1.0[3]	2.0mV[4]	35	80	C	H
AD644L	50k	10/5	2.0	13	0.5[3]	1.0mV[4]	35	80	C	H
AD644S (S/883B)	50k	10/5	2.0	13	1.0[3]	3.5mV[4]	75	80	M	H
AD647JH	100k	10/5	1.0	3.0	1.0[3]	10	75	76	C	H
AD647KH	250k	10/5	1.0	3.0	0.5[3]	5	35	80	C	H
AD647LH	250k	10/5	1.0	3.0	0.25[3]	2.5	35	80	C	H
AD647SH/883B	250k	10/5	1.0	3.0	0.5[3]	10	35	80	M	H

NOTES
[1] C = 0 to +70°C; M = -55°C to +125°C
[2] H = TO-99 can; Z = Module
[3] Dual amplifiers with matched side to side offset voltage
[4] Guaranteed max offset error from T_{min} to T_{max}

HIGH ACCURACY LOW V_{OS} DRIFT
SPECIFICATIONS (typical @ V_S = ±15V, T_A = +25°C unless otherwise noted)

Model	Gain min	Output V/mA min	Unity Gain MHz	Slew Rate V/µs	V_{OS} mV max	$\Delta V_{OS}/\Delta T$ µV/°C max	I_b nA max	CMR dB min	Temp Range[1]	Package[2]
AD504J	250k	10/5	0.3 to 1.0[3]	0.12 to 2.5[3]	2.5	5.0	200	94	C	H
AD504K	500k	10/5	0.3 to 1.0[3]	0.12 to 2.5[3]	1.5	3.0	100	100	C	H
AD504L	1000k	10/5	0.3 to 1.0[3]	0.12 to 2.5[3]	0.5	1.0	80	110	C	H
AD504M	1000k	10/5	0.3 to 1.0[3]	0.12 to 2.5[3]	0.5	0.5	80	110	C	H
AD504S	1000k	10/5	0.3 to 1.0[3]	0.12 to 2.5[3]	0.5	1.0	80	110	M	H
AD510J	250k	10/5	0.3	0.1	0.1	3.0	25	94	C	H
AD510K	1000k	10/5	0.3	0.1	0.05	1.0	13	110	C	H
AD510L	1000k	10/5	0.3	0.1	0.025	0.5	10	110	C	H
AD510S	1000k	10/5	0.3	0.1	0.05	1.0	13	110	M	H
AD517J	1000k	10/10	0.25	0.1	0.150	3.0	5	94	C	H
AD517K	1000k	10/10	0.25	0.1	0.075	1.8	2	110	C	H
AD517L	1000k	10/10	0.25	0.1	0.05	1.3	1	110	C	H
AD517S	1000k	10/10	0.25	0.1	0.075	1.8	2	110	M	H
AD547J	100k	10/5	1.0	3.0	1.0	5	50	76	C	H
AD547K	250k	10/5	1.0	3.0	0.5	2	25	80	C	H
AD547L	250k	10/5	1.0	3.0	0.25	1	25	80	C	H
AD547S	250k	10/5	1.0	3.0	0.5	5	25	80	M	H
AD647JH	100k	10/5	1.0	3.0	1.0[3]	10	75	76	C	H
AD647KH	250k	10/5	1.0	3.0	0.5[3]	5	35	80	C	H
AD647LH	250k	10/5	1.0	3.0	0.25[3]	2.5	35	80	C	H
AD647SH	250k	10/5	1.0	3.0	0.5[3]	10	35	80	M	H
AD OP-07EH	2000k	10/10	0.6	0.17	0.075	1.3	±4	106	C	H
AD OP-07CH	1200k	10/10	0.6	0.17	0.150	1.6	±7	100	C	H
AD OP-07DH	1200k	10/10	0.6	0.17	0.150	2.5	±12	94	C	H
AD OP-07AH	3000k	10/10	0.6	0.17	0.025	0.6	±2	110	M	H
AD OP-07H	2000k	10/10	0.6	0.17	0.075	1.3	±3	110	M	H

NOTES
[1] C = 0 to +70°C; M = -55°C to +125°C
[2] H = TO-99 can; N = 8-pin mini DIP
[3] Dependent on compensation capacitor selection

HIGH ACCURACY LOW BIAS CURRENT
SPECIFICATIONS (typical @ V_S = ±15V, T_A = +25°C unless otherwise noted)

Model	Gain min	Output V/mA min	Unity Gain MHz	Slew Rate V/µs	V_{OS} mV max	$\Delta V_{OS}/\Delta T$ µV/°C max	I_b pA max	CMR dB min	Temp Range[1]	Package[2]
AD515J	20k	10/5	0.35	0.3	3.0	50	0.300	66	C	H
AD515K	40k	10/5	0.35	0.3	1.0	15	0.150	80	C	H
AD515L	25k	10/5	0.35	0.3	1.0	25	0.075	70	C	H
AD545J	20k	10/5	0.7	1.0	1.0	25	2	66	C	H
AD545K	40k	10/5	0.7	1.0	1.0	15	1	70	C	H
AD545L	40k	10/5	0.7	1.0	0.5	5	1	76	C	H
AD545M	40k	10/5	0.7	1.0	0.25	3	1	76	C	H

NOTES
[1] C = 0 to +70°C
[2] H = TO-99 can, Z = Module
[3] Adjustable to zero

FEATURE SELECTION CHART

		AD507	AD509	AD518	AD380	AD381	AD382	AD3554	HOS-050	HOS-060	ADLH0032	ADLH0033	HOS-100
		FAST/WIDEBAND											
					FET INPUT								UNITY GAIN BUFFER
Monolithic Technology	Bipolar Input	•	•	•									
	J-FET												
	Dual J-FET												
Multi-Device Technology	Hybrid				•	•	•	•	•	•	•	•	•
	Module												
High Open Loop Gain	≥100dB	•				•	•	•	•	•			
	≥140dB												
High CMR	>100dB												
Low Offset Voltage	≤5mV	•	•		•		•	•			•	•	
	≤1mV					•				•			
	≤50μV						•	•					
Low Offset V, vs. Temp	≤5μV/°C					•	•						
	≤1μV/°C												
	≤0.6μV/°C												
Low Bias Current	≤50pA					•	•	•			•	•	
	≤5pA												
	≤0.5pA												
Fast Settling	≤1μs to 0.1%	•	•	•		•	•		•	•	•	•	•
	≤5μs to 0.01%				•			•	•	•	•		
Wideband (Unity Gain)	≥2MHz					•	•						
	≥10MHz	•	•	•	•			•	•	•	•	•	•
	≥50MHz												
High Slew Rate	≥10V/μs	•		•									
	≥30V/μs					•	•		•	•	•	•	•
	≥100V/μs		•		•								
	≥1000V/μs							•					
Low Noise (0.1 to 10Hz) ≤2μV p-p						•	•						
High Voltage Out	≥100V												
High Current Out	≥20mA	•			•		•	•	•	•		•	•
Low Power	≤75mW												
Second Source		•	•					•			•	•	
Temperature Range 0 to +70°C		•	•	•	•	•	•				•	•	
-25°C to +85°C								•					
-55°C to +125°C		•	•	•	•	•	•	•	•	•	•	•	•
Dice Availability				•									

FAST/WIDEBAND
SPECIFICATIONS (typical @ V_S = ±15V, T_A = +25°C unless otherwise noted)

Model	Gain min	Output V/mA min	Unity Gain MHz	Slew Rate V/μs min	Settling Time μs to 0.1%	V_{OS} mV max	$\Delta V_{OS}/\Delta T$ μV/°C max	I_b nA max	CMR dB min	Temp Range[1]	Package[2]
AD380JH	25k	10/50	40	200	0.13	2.0	50	100	60	C	X
AD380KH	25k	10/50	40	200	0.13	1.0	20	100	60	C	X
AD380LH	25k	10/50	40	200	0.13	1.0	10	100	60	C	X
AD380SH/883B	25k	10/50	40	200	0.13	1.0	50	100	60	M	X
AD381JH	60k	10/5	5	20	0.7	1.0	15	100	76	C	H
AD381KH	100k	10/5	5	20	0.7	0.5	10	100	80	C	H
AD381LH	100k	10/5	5	20	0.7	0.25	5	100	80	C	H
AD381SH/883B	100k	10/5	5	20	0.7	1.0	10	100	80	M	H
AD382JH	25k	10/50	5	20	1.3[3]	1.0	15	100	76	C	X
AD382KH	35k	10/50	5	20	1.3[4]	0.5	10	50	80	C	X
AD382LH	35k	10/50	5	20	1.3[4]	0.25	5	50	80	C	X
AD382SH/883B	35k	10/50	5	20	1.3[4]	1.0	10	50	80	M	X
AD507J	80k	10/10	35	20	0.9	5	15	25	74	C	H
AD507K	100k	10/10	35	25	0.9	3	15	15	80	C	H
AD507S	100k	10/10	35	20	0.9	4	20	15	80	M	H
AD509J	7.5k	10/5	20	80	0.2	10	20	250	74	C	H
AD509K	10k	10/5	20	80	0.2	8	30	200	80	C	H
AD509S	10k	10/5	20	100	0.5	8	30	200	80	M	H
AD518J	25k	10/10	12	50	0.8	10	10	500	70	C	H
AD518K	50k	10/10	12	50	0.8	4	15	250	80	C	H
AD518S	50k	10/10	12	50	0.8	4	20	250	80	M	H
AD3554AM	31.6k	10/100	90	1000	0.12	2.0	50	50	60	I	Y
AD3554BM	31.6k	10/100	90	1000	0.12	1.0	15	50	60	I	Y
AD3554SM	31.6k	10/100	90	1000	0.12	1.0	25	50	60	M	Y
ADLH0032CG	1k	12/10	70	500	0.3	5	25	0.025	60	I	X
ADLH0032G	1k	12/10	70	500	0.3	2	25	0.01	60	M	X
ADLH0033CG	0.98[5]	12/100	100[6]	1400	3.2ns[7]	12	50	0.05	–	I	X
ADLH0033G	0.98[5]	12/100	100[6]	1500	2.9ns[7]	5	50	0.05	–	M	X
HOS-050	100k	10/100	100	300	0.1	35	150	2	70	M	X
HOS-050A	100k	10/100	100	300	0.1	15	35	2	70	M	X
HOS-050C	100k	10/100	100	300	0.1	65	200	2*	70	I	X
HOS-060SH	100k	10/100	100	300	0.1	1.0	10	2*	70	M	X
HOS-100AH	0.96[5]	12/100	125[6]	1400	2.0ns[7]	10	25	5μA	–	I	X
HOS-100SH	0.97[5]	12/100	125[6]	1500	2.0ns[7]	5	25	5μA	–	M	X

NOTES
[1] C = 0 to +70°C, I = -25°C to +85°C, M = -25°C to +125°C
[2] H = TO-99 can, X = 12-lead TO-8 can, Y = TO-3 can, Z = Module
[3] Settling time to 0.01%
[4] Settling time to 0.01%; max
[5] Unity Gain Buffers
[6] Large Signal 3dB BW
[7] Rise Time

ANALOG DEVICES

Precision Instrumentation Amplifier

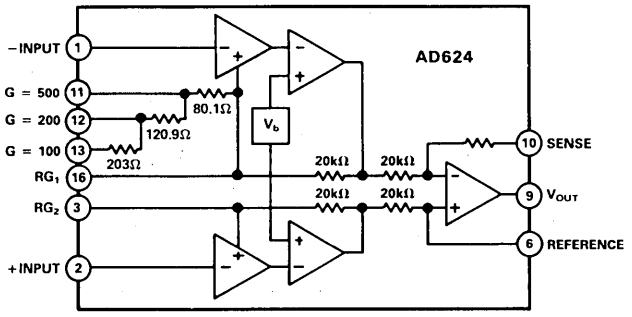
AD624

PRELIMINARY TECHNICAL DATA

FEATURES

- Low Noise: 0.2μV p-p 0.1Hz to 10Hz
- Low Nonlinearity: 0.003% (G = 1)
- High CMRR: 115dB (G = 500)
- Low Offset Voltage: 50μV
- Low Offset Voltage Drift: 0.25μV/°C
- Gain Bandwidth Product: 25MHz
- Pin Programmable Gains of 1, 100, 200, 500
- No External Components Required
- Internally Compensated

AD624 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

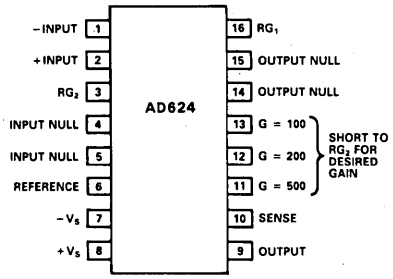
The AD624 is a precision monolithic instrumentation amplifier designed for data acquisition applications requiring high accuracy under worst-case operating conditions. An outstanding combination of high linearity, high common mode rejection, low offset voltage drift, and low noise makes the AD624 suitable for use in many data acquisition systems.

The AD624 has an output offset voltage drift of less than 25μV/°C, input offset voltage drift of less than 0.25μV/°C, CMR above 90dB at unity gain (120dB at G = 500) and maximum nonlinearity of 0.003% at G = 1. In addition to the outstanding dc specifications the AD624 also has a 25MHz gain bandwidth product (G = 100). To make it suitable for high speed data acquisition systems the AD624 has an output slew rate of 5V/μs and settles in 15μs to 0.01% for gains of 1 to 100.

As a complete amplifier the AD624 does not require any external components for fixed gains of 1, 100, 200 and 500. For other gain settings between 1 and 1000 only a single resistor is required.

The AD624 IC instrumentation amplifier is available in four different versions of accuracy and operating temperature range. The economical "A" grade, the low drift "B" grade and lower drift, higher linearity "C" grade are specified from −25°C to +85°C. The "S" grade guarantees performance to specification over the full MIL-temperature range −55°C to +125°C, and is available with MIL-STD-883B screening.

PIN CONFIGURATION

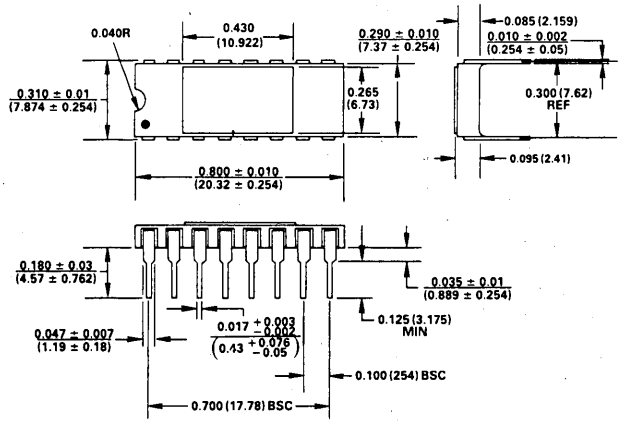


PRODUCT HIGHLIGHTS

1. The AD624 has guaranteed low offset voltage, offset voltage drift and low noise for precision high gain applications.
2. The AD624 is functionally complete with pin programmable gains of 1, 100, 200 and 500, and single resistor programmable for any gain.
3. Input and output offset nulling terminals are provided for very high precision applications and to minimize offset voltage changes in gain ranging applications.
4. The AD624 offers superior dynamic performance with a gain bandwidth product of 25MHz, full power response of 75kHz and a settling time of 15μs to 0.01% of a 10V step (G = 100).

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



16-PIN CERAMIC DIP

LINEAR

Analog Devices

AD9685/AD9687

FEATURES
2.2ns Propagation Delay – AD9685BD/BH
2.7ns Propagation Delay – AD9687BD
0.5ns Latch Set-Up Time
Pin-Compatible to Am685/687 but FASTER
+5V, −5.2V Supply Voltages

APPLICATIONS
Ultra-High-Speed A/D Converters
Ultra-High-Speed Line Receivers
Peak Detectors
Threshold Detectors

GENERAL DESCRIPTION

The AD9685BD/BH and AD9687BD are ultra-fast comparators manufactured with a high performance bipolar process which makes it possible to obtain incredibly short propagation delays and latch set-up times.

The AD9685BD/BH is a single comparator which is pin-compatible with the Am685, but has speed capabilities that far outstrip the earlier unit. The AD9687BD is pin-for-pin compatible with the Am687 and, like its predecessor, is a dual comparator; its speed capabilities are far superior to the Am687.

Both Analog Devices units have differential inputs and complementary outputs fully compatible with ECL logic levels. Their output current levels are capable of driving 50Ω terminated transmission lines, and their high resolution make them ideally suited for a variety of analog-to-digital signal processing applications.

AD9685BD/BH Single Comparator

A latch function allows the AD9685BD/BH to be operated in a sample-hold mode. When the Latch Enable (LE) is ECL HIGH, the comparator functions normally. When the Latch Enable is driven LOW, its outputs are locked in the logic state dictated by the input conditions at the time of the latch input transition. If the latch function is not used, the Latch Enable input should be connected to ground.

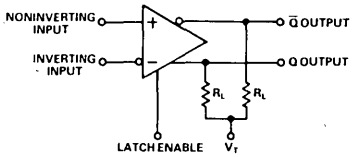
In addition to its speed advantages over the earlier Am685, the AD9685BD/BH also dissipates less power because it operates on a positive 5 volt supply instead of the 6 volts required by the AMD device.

AD9687BD Dual Comparator

The latch function of the AD9687BD provides an ability to operate the unit in either a track-hold or sample-hold mode. The latch function inputs are separated on the two comparators and are designed to be driven from the complementary outputs of a standard ECL logic gate. When LE is High and $\overline{LE}$ is LOW, the normal comparator function is in operation. When LE is forced LOW and $\overline{LE}$ is driven HIGH, the outputs of the comparator being exercised are locked in their existing logical states, as determined by the input conditions present at the time of arrival of the latch signal. If the latch function is not used on either one of the two comparators in the AD9687BD, the appropriate Latch Enable input should be connected to ground; the companion Latch $\overline{\text{Enable}}$ input can be left open.

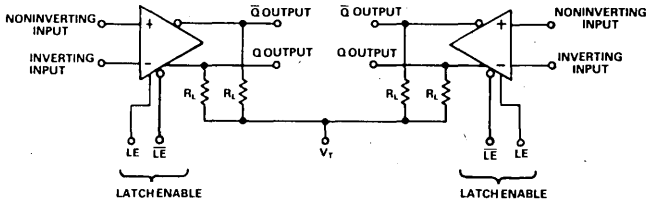
The AD9687BD is basically two AD9685BD/BH units in a single package and operates in a similar fashion to a pair of the single comparators.

AD9685BD/BH FUNCTIONAL BLOCK DIAGRAM



THE OUTPUTS ARE OPEN EMITTERS, REQUIRING EXTERNAL PULL-DOWN RESISTORS. THESE RESISTORS MAY BE IN THE RANGE OF 50Ω–200Ω CONNECTED TO −2.0V; OR 200Ω–2000Ω CONNECTED TO −5.2V.

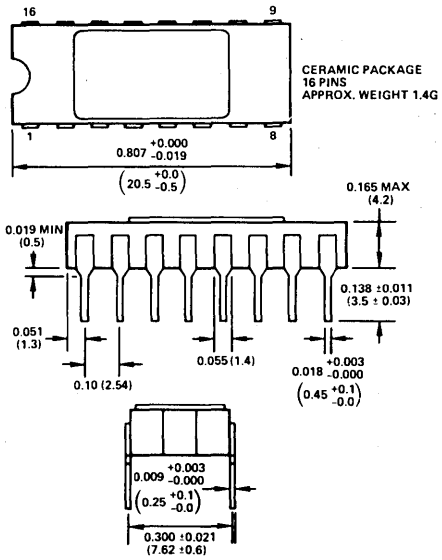
AD9687BD FUNCTIONAL BLOCK DIAGRAM



THE OUTPUTS ARE OPEN EMITTERS, REQUIRING EXTERNAL PULL-DOWN RESISTORS. THESE RESISTORS MAY BE IN THE RANGE OF 50Ω–200ΩCONNECTED TO −2.0V; OR 200Ω–2000Ω CONNECTED TO −5.2V.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



AD9687BD

INSTRUMENTATION AMPLIFIERS

SPECIFICATIONS (typical @ V_S = ±15V, R_L = 2kΩ and T_A = 25°C unless otherwise noted)

Model	Monolithic IC AD521J(K)(L)(S)[1]	Hybrid IC AD522A(B)(S)[1]	Monolithic AD524A(B)(C)(S)	Hybrid IC AD612A(B)(C)	Hybrid IC AD614A(B)	Monolithic AD624A(B)(C)(S)
GAIN						
Range V/V	0.1 to 1000	1 to 1000	1 to 1000	1 to 1024	1 to 1024	1 to 1000
Nonlinearity (G = 100) – % max	0.2(0.2)(0.1)(0.2)	0.01(0.005)(0.005)	0.01(0.005)(0.003)(0.005)	0.001	0.001	0.01(0.005)(0.003)(0.005)
RATED OUTPUT – V dc/mA	±10/±10	±10/±5	±10/±5	±10/±5	±10/±5	±10/±5
DYNAMIC RESPONSE						
Small Signal (–3dB)						
G = 1000	40kHz	300Hz	25kHz	10kHz	20kHz	25kHz
Full Power Frequency	100kHz	1.5kHz	–	–	–	–
Slew Rate – V/μs	10	0.1	5	1	1	5
OFFSET VOLTAGE						
Input Offset Voltage	3(1.5)(1)(1.5)μV max	±400(200)(200)μV max	250(100)(50)(100)μV	±200μV	±200μV	250(100)(50)(100)μV
vs. Temperature	15(15)(2)(5)μV/°C	±6(2)(6)μV/°C	2(0.75)(0.5)(2)μV/°C	±5(2)(1)μV/°C max	±5(2)μV/°C max	1(0.5)(0.2)(1)μV/°C
Output Offset Voltage	400(1200)(100)(200)μV max		5(3)(2)(3)mV	2mV	2mV	5(3)(2)(3)mV
vs. Temperature	400(150)(75)(150)μV/°C		100(50)(25)(50)μV/°C	±200(150)(75)μV/°C	±200(150)μV/°C max	100(50)(25)(50)μV/°C
INPUT BIAS CURRENT – nA max	±80(40)(40)(40)	±25(15)(25)	50(25)(15)(25)	+100	+100	100(50)(30)(100)
INPUT IMPEDANCE						
Common Mode – Ω	6×10^{10}	10^9	10^9/10pF	10^9/3pF	10^9/3pF	10^9/10pF
COMMON MODE REJECTION RATIO min @ 1kΩ Source Unbalance, CMV = ±10V						
G = 1 – dB	70(74)(74)(74)[2]	75(80)(85) dc to 30Hz	70(75)(80)(70)	74[2]	74[2]	
G = 10 – dB	90(94)(94)(94)[2]	90(95)(90) dc to 10Hz	90(95)(100)(90)	80[2]	80[2]	
G = 1000 – dB	100(110)(110)(110)[2]	100(110)(100) dc to 1Hz	100(115)(120)(110)	94[2]	94[2]	100(110)(115)(100)

NOTES
[1] Processing to MIL-STD-883B available.
[2] DC to 60Hz.

COMPARATORS

The AD9685BD/BH and AD9687BD are ultra-fast comparators which make it possible to obtain incredibly short propagation delays and latch setup times. The AD9685BD/BH is a single comparator, with the BD and BH suffixes indicating a DIP or TO-100 configuration; the AD9687BD is a dual comparator in a DIP.

The Analog Devices units are pin-for-pin compatible with the Am685 and Am687 comparators, but are far superior in speed to their forerunners. The ADI devices are an alternate source, not a second source, for the earlier units because of their greater speed capabilities but can be used as a higher-performance replacement for most applications.

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

Model Number	Input Offset Voltage	Max. Input Offset Current	Input Bias Current	Input Voltage Range	Output Levels (Volts) High	Output Levels (Volts) Low	Propagation Delays (ns) Input to Output High	Propagation Delays (ns) Input to Output Low	Latch Enable Times (nanoseconds) Setup	Latch Enable Times (nanoseconds) Hold
AD9685	5mV	5μA	10μA	±5V	-0.88	-1.75	2.2	2.2	0.5	1.0
AD9687	5mV	5μA	10μA	±5V	-0.88	-1.75	2.7	2.7	0.5	1.0

ANALOG DEVICES

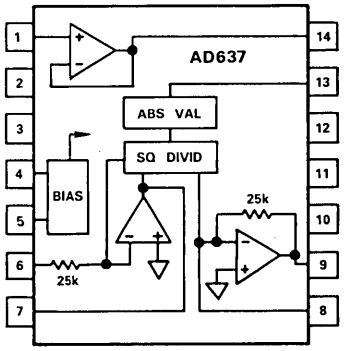
Integrated Circuit True rms-to-dc Converter

AD637

FEATURES

- True rms-to-dc Conversion
- Laser-Trimmed to High Accuracy
  - ±0.1% max Error AD637K
- Wide Response Capability:
  - Computes rms of ac and dc Signals
  - 500kHz Bandwidth: V rms >100mV
  - 5MHz Bandwidth: V rms >1V
  - Signal Crest Factor of 7 for 1% Error
- dB Output with 60dB Range
- Low Power: 2.5mA Operating Current
  - 350μA Power Down
- Monolithic Integrated Circuit

AD637 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

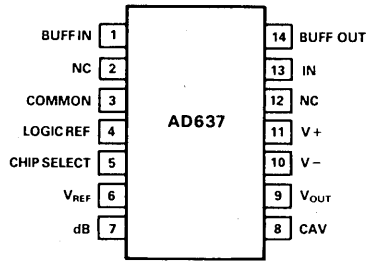
The AD637 is a complete monolithic integrated circuit which performs true rms-to-dc conversion. It offers performance which is comparable or superior to that of hybrid or modular units costing much more. The AD637 directly computes the true rms value of any complex input waveform containing ac and dc components. It has a crest factor compensation scheme which allows measurements with 1% error at crest factors up to 7. The wide bandwidth of the device extends the measurement capability to 500kHz with 3dB error for signal levels above 100mV.

An important feature of the AD637 is an auxiliary dB output. The logarithm of the rms output signal is brought out to a separate pin to allow the dB conversion, with a useful dynamic range of 60dB. Using an externally supplied reference current, the 0dB level can be conveniently set by the user to correspond to any input level from 0.1 to 2 volts rms.

The AD637 is laser trimmed at the wafer level for input and output offset, positive and negative waveform symmetry (dc reversal), and full scale accuracy. As a result, no external trims are required to achieve the rated accuracy of the unit.

There is full protection for both inputs and outputs. The input circuitry can take overload voltages well beyond the supply levels. Loss of supply voltage with inputs connected will not cause unit failure. The output is short-circuit protected.

PIN CONFIGURATION

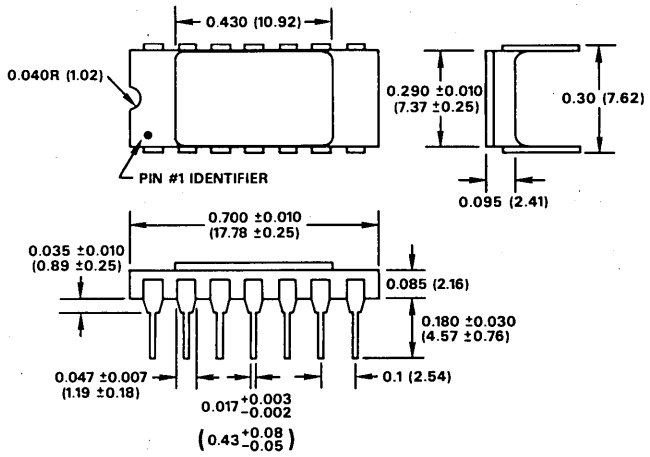


PRODUCT HIGHLIGHTS

1. The AD637 computes the true root-mean-square level of a complex ac (or ac plus dc) input signal and gives an equivalent dc output level. The true rms value of a waveform is a more useful quantity than the average rectified value since it relates directly to the power of the signal. The rms value of a statistical signal also relates to its standard deviation.
2. The crest factor of a waveform is the ratio of the peak signal swing to the rms value. The crest factor compensation scheme of the AD637 allows measurement of highly complex signals with wide dynamic range.
3. The only external component required to perform measurements to the fully specified accuracy is the capacitor which sets the averaging period. The value of this capacitor determines the low frequency ac accuracy, ripple level and settling time.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



14-PIN CERAMIC DIP

LINEAR

Analog Devices

ANALOG DEVICES

Balanced Modulator-Demodulator

AD630

PRELIMINARY TECHNICAL DATA

FEATURES

- Pin Programmable Gains of ±1 and ±2
- Wide Bandwidth: 2MHz
- Low Channel Selection Delay: 200ns
- Crosstalk −80dB at 10kHz
- Low Offset Voltage: 250μV
- High Gain Accuracy: 0.05%

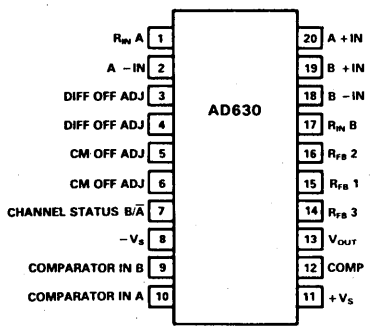
PRODUCT DESCRIPTION

The AD630 is a precision balanced modulator-demodulator consisting of two selectable input amplifiers, an output amplifier, and a fast comparator-controlled channel select switch. Its signal processing applications include modulation, demodulation, quadrature detection, synchronous detection, lock-in amplification, phase detection, and square wave multiplication. It can also be used as a precision two-channel analog multiplexer with pin programmable channel gains of +1, +2, +3 or +4. Other channel gains can be configured using external resistors.

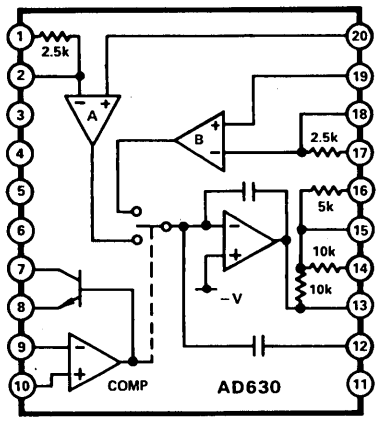
The two signal channels are comprised of two input transconductance stage amplifiers, a current mode switch and a transimpedance output stage. This type of circuit design yields a very high open loop gain, typically 100dB. The open loop channel gain is divided between the input and the output stages so as to minimize switching distortion and maximize the amplifying channel bandwidth which is typically 2MHz.

The AD630 is intended for wide band, low level, and wide dynamic range instrumentation applications. Particular attention was paid to the implementation of the circuit which yielded a good channel separation of 80dB at 10kHz. The use of laser trimmed thin-film resistors provided low offset voltage for both input amplifiers and comparator; 250μV typical. The pin programmable channel gains of ±1 and ±2 are also pretrimmed to 0.05% accuracy and a match of 0.03%.

PIN CONFIGURATION



AD630 FUNCTIONAL BLOCK DIAGRAM

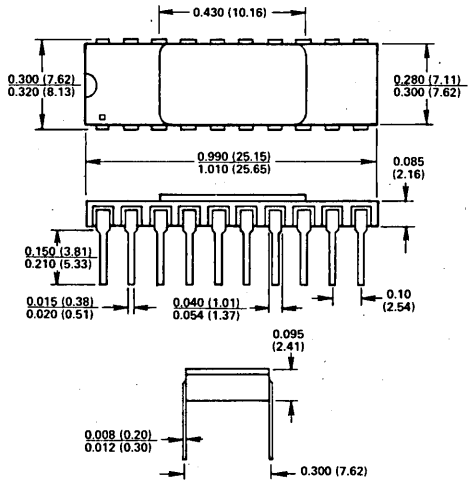


PRODUCT HIGHLIGHTS

1. The applications versatility designed into the AD630 can be utilized for a number of signal processing functions such as:
   - Balanced Modulator
   - Balanced Demodulator
   - Absolute Value Amplifier
   - Phase Detector
   - Square Wave Multiplier
   - Two-Channel Precision Multiplexer
2. Laser wafer trimmed thin-film resistors provide closed loop gain accuracies to within 0.05% and matched to 0.03%.
3. Laser trimming reduces offset voltages on both the input amplifiers and comparator to as low as 250μV, thus eliminating the need for external nulling in many situations.
4. The AD630 has good channel separation of 80dB at 10kHz and a wide bandwidth of 2MHz for use in wide band instrumentation.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



COMPUTATIONAL CIRCUITS
SPECIFICATIONS (typical @ +25°C and rated supply voltage unless noted otherwise)

Model	Transfer Function	Full Scale Accuracy - % Max	Accuracy vs. Temperature %/°C	X Nonlinearity % of Full Scale	Y Nonlinearity % of Full Scale	Bandwidth Small Signal MHz	Operating Power Supply Volts	Operating Temperature Range[1]
AD531J	XY/kI_z	2	0.04	0.8	0.3	1	±15 to ±18	C
AD531K	XY/kI_z	1	0.03	0.5	0.2	1	±15 to ±18	C
AD531L	XY/kI_z	0.5	0.01	0.3	0.2	1	±15 to ±18	C
AD531S	XY/kI_z	1	0.03 max	0.5	0.2	1		M
AD532J	$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10}$	2	0.04	0.8	0.3	1	±15 to ±18	C
AD532K	$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10}$	1	0.03	0.5	0.2	1	±15 to ±18	C
AD532S	$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10}$	1	0.04 max	0.5	0.2	1		M
AD533J	XY/10	2	0.04	0.8	0.3	1	±15 to ±18	C
AD533K	XY/10	1	0.03	0.5	0.2	1	±15 to ±18	C
AD533L	XY/10	0.5	0.01	0.5	0.2	1	±15 to ±18	C
AD533S	XY/10	1	0.01	0.5	0.2	1		M
AD534J	$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10 + Z_2}$	1	0.022	0.4	0.01	1	±8 to ±18	C
AD534K	$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10 + Z_2}$	0.5	0.015	0.3 max	0.01 max	1	±8 to ±18	C
AD534L	$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10 + Z_2}$	0.25	0.008	0.12 max	0.01 max	1	±8 to ±18	C
AD534S	$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10 + Z_2}$	1	0.02 max	0.4	0.01	1	±8 to ±18	M
AD534T	$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10 + Z_2}$	0.5	0.01 max	0.3 max	0.01 max	1	±8 to ±18	M
AD539J	$V_X V_{y1}, V_X V_{y2}$ (Note 2)	2.5	5% Total[3]	0.5dB[4]	–	30 min	±4.5 to ±16.5	C
AD539K	$V_X V_{y1}, V_X V_{y2}$ (Note 2)	1.5	2% Total[3]	0.2dB[4]	–	30 min	±4.5 to ±16.5	C
AD539S	$V_X V_{y1}, V_X V_{y2}$ (Note 2)	2.5	5% Total[3]	0.5dB[4]	–	30 min	±4.5 to ±16.5	M

NOTES
[1]C: 0 to +70°C, M: -55°C to +125°C [2]Channels 1 & 2 [3]Multiplier scaling voltage [4]Absolute gain error

RMS-TO-DC CONVERTERS
SPECIFICATIONS (typical @ +25°C and rated supply voltage unless otherwise noted)

Model	Transfer Function	Conversion Accuracy	Conversion Accuracy vs. Temperature	Input Signal Range	I_{OUT} Scale Factor	Bandwidth Full Scale	Operating Power Supply Volts	Operating Temperature Range[1]
AD536AJ	$V_{OUT} = \sqrt{avg.\ (V_{IN})^2}$	±5mV ±0.5% of RDG max	±(0.1mV ±0.01% of RDG)/°C	±10V	40μA/V rms	2MHz	+5 to ±18	C
AD536AK	$V_{OUT} = \sqrt{avg.\ (V_{IN})^2}$	±2mV ±0.2% of RDG max	±(0.05mV ±0.005% of RDG)/°C	±10V	40μA/V rms	2MHz	+5 to ±18	C
AD536AS	$V_{OUT} = \sqrt{avg.\ (V_{IN})^2}$	±5mV ±0.5% of RDG max	±(0.1mV ±0.01% of RDG)/°C	±10V	40μA/V rms	2MHz	+5 to ±18	M
AD636J	$V_{OUT} = \sqrt{avg.\ (V_{IN})^2}$	±0.5mV ±1.0% of RDG max	±(0.1mV ±0.001% of RDG)/°C	±200mV	100μA/V rms	1.3MHz	+2/-2.5 to ±12	C
AD636K	$V_{OUT} = \sqrt{avg.\ (V_{IN})^2}$	±0.2mV ±0.5% of RDG max	±(0.1mV ±0.0005% of RDG)/°C	±200mV	100μA/V rms	1.3MHz	+2/-2.5 to ±12	C
AD637J	$V_{OUT} = \sqrt{avg.\ (V_{IN})^2}$	±1mV ±0.2% of RDG max	±0.4%	±10V	–	5MHz	±3.0 to ±18	C
AD637K	$V_{OUT} = \sqrt{avg.\ (V_{IN})^2}$	±0.5mV ±0.1% of RDG max	±0.2%	±10V	–	5MHz	±3.0 to ±18	C

NOTE
[1]C: 0 to +70°C, M: -55°C to +125°C

BALANCED MODULATOR-DEMODULATOR
SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

Model	AD630	Model	AD630
Gain		AC Characteristics	
Gain Accuracy ±1, ±2	0.05%	Comparator Hysteresis	1mV (0 min)
Gain Match	0.03%	Comparator Response Time	200ns
		Small Signal -3dB Bandwidth	2MHz
		Slew Rate	40V/μs
Input Characteristics, Amplifiers & Comparator		System Characteristics	
Input Offset Voltage	250μV	CMRR	90dB
Input Bias Current	250nA	PSRR	80dB
Input Offset Current	50nA	Channel Separation @ 10kHz	-80dB
Input Impedance	15MΩ‖1.5pF		

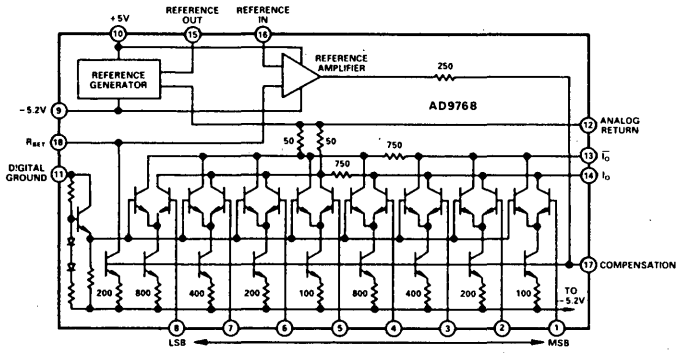
Ultra High-Speed IC D/A Converter

AD9768

FEATURES
- 5ns Settling Time
- 100MHz Update Rate
- 20mA Output Current
- ECL-Compatible
- 40MHz Multiplying Mode

APPLICATIONS
- Raster Scan & Vector Graphic Displays
- High-Speed Waveform Generation
- Digital VCOs
- Ultra-Fast Digital Attenuators

AD9768SD D/A SCHEMATIC



GENERAL DESCRIPTION

The Analog Devices AD9768SD D/A converter is a monolithic current-output converter which can accept ECL-level digital input voltages and convert them into analog voltages at update rates as high as 100MHz. In addition to its use as a standard D/A converter, it can also be utilized as a two-quadrant multiplying D/A at rates up to 40MHz.

An inherently low glitch design is used, and the complementary current outputs are suitable for driving transmission lines directly. Nominal full-scale output is 20mA, which corresponds to a 1-volt drop across a 50Ω load, or ±1 volt across 100Ω returned to +1 volt. The actual output current is determined by the on-chip reference voltage (V_{REF} = −1.28V) and an external current setting resistor, R_{SET}.

Full-scale output current I_{OUT} is calculated with the equation:

$$I_{OUT} = 4 \times \frac{V_{REF}}{R_{SET}}$$

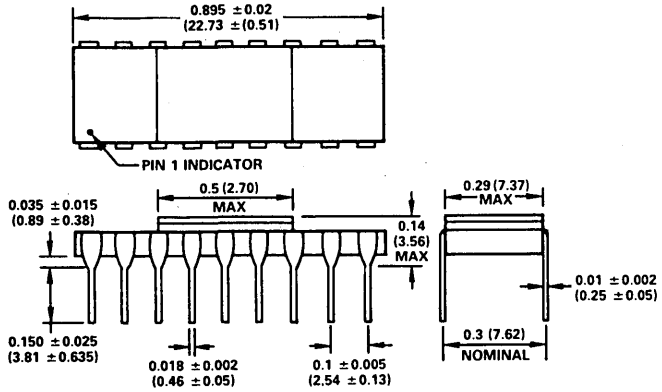
The setting resistor R_{SET} is typically 220Ω and should have a temperature coefficient similar to the output load resistor. A complementary $\overline{I_{OUT}}$ is also provided.

The reference voltage source is a modified bandgap type and is nominally −1.28 volts. This reference supply is on-chip stable; to reduce the possibility of noise generation and/or instability, pin 15 (REFERENCE OUT) can be decoupled using a high-quality ceramic chip capacitor. Stabilization of the internal loop amplifier is by a single capacitor connected from pin 17 (COMPENSATION) to ground. The minimum value for this capacitor is 3900pF, although a 0.01μF chip ceramic capacitor is recommended.

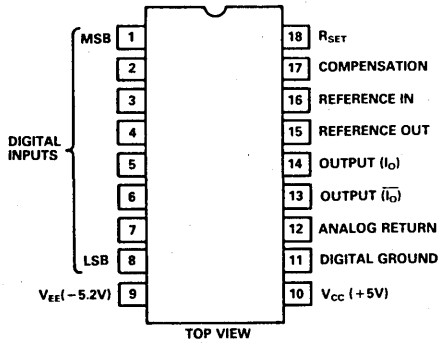
The incredible speed characteristics of the AD9768SD D/A converter make it attractive for a wide range of high-speed applications. The ability of the unit to operate as a two-quadrant multiplying D/A converter adds another dimension to its usefulness and makes the AD9768SD a truly versatile device.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



AD9768SD PIN CONNECTIONS (TOP VIEW)



ANALOG DEVICES

LOGDAC™ CMOS 0.1dB Step Attenuator

AD7115

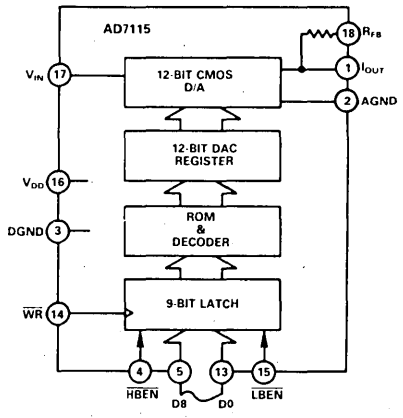
FEATURES

Dynamic Range: 0 to 19.9dB Plus Full Muting
Resolution: 0.1dB
2 1/2 Digit BCD Input Coding
On-Chip Data Latches
Full ±25V Input Range
Low Distortion and Noise
Latch-Up Free (No Protection Schottky Required)
TTL Compatible
Monotonic

APPLICATIONS

Audio Attenuators
Function Generators
Test Equipment
Digitally Controlled AGC Systems

AD7115 FUNCTIONAL BLOCK DIAGRAM



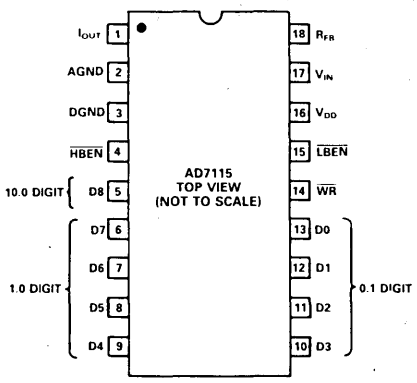
GENERAL DESCRIPTION

The AD7115 is a digitally programmable attenuator which attenuates an analog input signal over the range 0 to −19.9dB in 0.1dB steps.

The degree of attenuation is controlled by a 2 1/2 digit BCD coded input word which is latched into on-chip data latches using microprocessor compatible control signals $\overline{WR}$, $\overline{LBEN}$ and $\overline{HBEN}$. Operating frequency range of the device is from dc to several hundred kHz.

The device is packaged in an 18-pin dual-in-line plastic, cerdip or ceramic package.

PIN CONFIGURATION



PRODUCT HIGHLIGHTS

1. High resolution 0.1dB steps from 0 to 19.9dB with step accuracies better than ±0.04dB allow precision attenuators and other special purpose function generators to be built at low cost.
2. A resolution of 0.1dB is equivalent to step sizes of 1% of reading.
3. The 2 1/2 digit BCD input code can be loaded into the on-chip latches in one $\overline{WRITE}$ operation. Alternatively, for use with an 8-bit data bus, data can be loaded in two $\overline{WRITE}$ operations by using byte enable signals $\overline{HBEN}$ and $\overline{LBEN}$.
4. The AD7115 can be used in series with standard attenuator blocks to position its attenuation range as required, e.g., −40dB to −60dB in 0.1dB steps.
5. Analog input signal can be up to ±25V with V_{DD} = +5V.

ONE TECHNOLOGY WAY • P.O. BOX 280 • NORWOOD, MA 02062 • (617) 329-4700

FEATURE SELECTION CHART

		GENERAL PURPOSE					FAST				μP BUS COMPATIBLE		SPECIAL PURPOSE			MULTIPLYING						
		AD1408	AD DAC80-I	AD DAC80-V	AD DAC85-I	AD DAC85-V	AD DAC-08	AD561	AD DAC100	AD558	AD7524	AD7522	AD7527 SYSTEMS DAC	AD7528 DUAL DAC	AD7523	AD7520	AD7530	AD7533	AD7521	AD7531	AD7541	AD7541A
Resolution	8 Bits	•					•			•	•			•	•							
	10 Bits							•	•			•	•			•	•	•				
	12 Bits		•	•	•	•													•	•	•	•
Accuracy	8 Bits	•					•			•	•	•		•	•	•	•	•	•	•		
	10 Bits							•	•		•	•	•		•	•	•	•	•	•		
	12 Bits		•	•	•	•															•	•
Output Format	Current	•	•		•		•	•	•		•	•	•	•	•	•	•	•	•	•	•	•
	Voltage			•		•				•												
Internal Reference			•	•	•	•		•	•	•												
Multiplication Capability	2 Quadrant	•					•	•	•		•	•	•	•	•	•	•	•	•	•	•	•
	4 Quadrant										•	•	•	•	•	•	•	•	•	•	•	•
Logic Compatible with	TTL	•	•	•	•	•	•	•	•	•	•	•		•		•	•	•	•	•	•	•
	CMOS	•					•	•		•	•	•	•	•	•	•	•	•	•	•	•	•
Input Coding	Binary	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	BCD		•	•	•	•																
Second Source		•	•	•	•	•	•		•		•	•			•	•	•	•	•	•	•	•
Single Power Supply										•												
Input Data Latch Structure	Serial											•										
	Parallel									•	•	•	•	•								
Operating Temperature Ranges[1]	C = 0 to +70°C	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	I = -25°C to +85°C				•	•					•	•	•	•	•	•	•	•	•	•	•	•
	M = -55°C to +125°C	•			•	•	•	•	•	•	•	•	•	•	•	•		•	•		•	•
Low Power										•	•	•	•	•	•	•	•	•	•	•	•	•
Dice Availability							•	•		•	•	•		•	•	•		•	•	•	•	

NOTE
[1] C = Commercial I = Industrial M = Military

GENERAL PURPOSE SPECIFICATIONS (maximum @ +25°C unless otherwise noted as typical)

Model	Resolution	Relative Accuracy	Differential Nonlinearity	Gain T.C. ppm/°C	Settling Time	Temp Range[1]	I/V Out	Input Logic	Package
AD DAC-08(/883B)	8 Bits	±0.19%	Monotonicity	50	135ns	M	I	TTL &	DIP
AD DAC-08A(/883B)	8 Bits	±0.1%	Guaranteed	50	135ns	M	I	CMOS	DIP
AD DAC-08C	8 Bits	±0.39%		80	135ns	C	I		DIP
AD DAC-08E	8 Bits	±0.19%		50	135ns	C	I		DIP
AD DAC-08H	8 Bits	±0.1%		50	135ns	C	I		DIP
AD1408-7	8 Bits	±0.39%	±2LSB	20 typ	250ns typ	C	I	TTL &	DIP
AD1408-8	8 Bits	±0.19%	±1LSB	20 typ	250ns typ	C	I	CMOS	DIP
AD1408-9	8 Bits	±0.1%	±1/2LSB	20 typ	250ns typ	C	I		DIP
AD1508-8(/883B)	8 Bits	±0.19%	±1LSB	20 typ	250ns typ	M	I		DIP
AD1508-9(/883B)	8 Bits	±0.1%	±1/2LSB	20 typ	250ns typ	M	I		DIP
AD DAC80(Z)-CBI-V[2]	12 Bits	±0.012%	±3/4LSB	30	3μs typ	C	V	TTL	DIP
AD DAC80(Z)-CBI-I[2]	12 Bits	±0.012%	±3/4LSB	30	300ns typ	C	I		DIP
AD DAC80(Z)-CCD-V[2]	3 Digits	±0.024%	±1/2LSB	30	3μs typ	C	V		DIP
AD DAC80(Z)-CCD-I[2]	3 Digits	±0.024%	±1/2LSB	30	300ns typ	C	I		DIP
AD DAC85C-CBI-V	12 Bits	±0.012%	±1/2LSB	20	3μs typ	C	V	TTL	DIP
AD DAC85C-CBI-I	12 Bits	±0.012%	±1/2LSB	20	300ns typ	C	I		DIP
AD DAC85C-CCD-V	3 Digits	±0.024%	±1/2LSB	20	3μs typ	C	V		DIP
AD DAC85C-CCD-I	3 Digits	±0.024%	±1/2LSB	20	300ns typ	C	I		DIP
AD DAC85(LD)-CBI-V	12 Bits	±0.012%	±1/2LSB	20 (10)	3μs typ	I	V		DIP
AD DAC85(LD)-CBI-I	12 Bits	±0.012%	±1/2LSB	20 (10)	300ns typ	I	I		DIP
AD DAC85-CCD-V	3 Digits	±0.024%	±1/2LSB	20	3μs typ	I	V		DIP
AD DAC85-CCD-I	3 Digits	±0.025%	±1/2LSB	20	300ns typ	I	I		DIP
AD DAC85MIL-CBI-V	12 Bits	±0.012%	±1/2LSB	20	3μs typ	M	V		DIP
AD DAC85MIL-CBI-I	12 Bits	±0.012%	±1/2LSB	20	300ns typ	M	I		DIP
AD DAC100JD(/883B)	10 Bits	±0.1%	GMOT[3]	±60	375ns	I	I	TTL &	DIP
AD DAC100KD(/883B)	10 Bits	±0.05%	GMOT[3]	±30	375ns	I	I	DTL	DIP
AD DAC100LD(/883B)	10 Bits	±0.05%	GMOT[3]	±15	375ns	I	I		DIP
AD DAC100SD(/883B)	10 Bits	±0.1%	GMOT[3]	±60	375ns	M	I		DIP
AD DAC100TD(/883B)	10 Bits	±0.05%	GMOT[3]	±30	375ns	M	I		DIP
AD561JD	10 Bits	±0.05%	±1/2LSB	80	250ns typ	C	I	TTL &	DIP
AD561KD	10 Bits	±0.025%	±1/2LSB	30	250ns typ	C	I	CMOS	DIP
AD561SD(/883B)	10 Bits	±0.05%	±1/2LSB	60	250ns typ	M	I		DIP
AD561TD(/883B)	10 Bits	±0.025%	±1/2LSB	30	250ns typ	M	I		DIP

NOTES
[1] C = 0 to +70°C, I = -25°C to +85°C, M = -55°C to +125°C
[2] "Z" models specified for operation on ±12V supplies
[3] Guaranteed Monotonic Over Temperature

MULTIPLYING SPECIFICATIONS (maximum @ +25°C unless otherwise noted as typical)

Model	Resolution	Relative Accuracy	Differential Nonlinearity	Gain T.C. ppm/°C	Settling Time	Temp Range[1]	I/V Out	Input Logic	Package
AD7523JN(AD)(SD)	8 Bits	±0.2%	Monotonicity	66/50/30	150ns typ	C/I/M	I	CMOS	DIP
AD7523KN(BD)	8 Bits	±0.1%	Guaranteed	66/50	150ns typ	C/I	I		DIP
AD7523LN(CD)	8 Bits	±0.05%		66/50	150ns typ	C/I	I		DIP
AD7520JN(JD)(SD)	10 Bits	±0.2%	±0.4%	10	500ns typ	C/I/M	I	CMOS &	DIP
AD7520KN(KD)(TD)	10 Bits	±0.1%	±0.2%	10	500ns typ	C/I/M	I	TTL	DIP
AD7520LN(LD)(UD)	10 Bits	±0.05%	±0.1%	10	500ns typ	C/I/M	I		DIP
AD7530JN(JD)	10 Bits	±0.2%	±0.4%	10	500ns typ	C/I	I	CMOS &	DIP
AD7530KN(KD)	10 Bits	±0.1%	±0.2%	10	500ns typ	C/I	I	TTL	DIP
AD7530LN(LD)	10 Bits	±0.05%	±0.1%	10	500ns typ	C/I	I		DIP
AD7533JN(AD)(SD) (SD/883B)	10 Bits	±0.2%	±0.4%	22/16/10	600ns	C/I/M/M	I	CMOS & TTL	DIP
AD7533KN(BD)(TD) (TD/883B)	10 Bits	±0.1%	±0.2%	22/16/10	600ns	C/I/M/M	I	CMOS & TTL	DIP
AD7533LN(LD)(UD) (UD/883B)	10 Bits	±0.05%	±0.1%	22/16/10	600ns	C/I/M/M	I	CMOS & TTL	DIP
AD7521JN(JD)(SD)	12 Bits	±0.2%	±0.4%	10	500ns typ	C/I/M	I	CMOS &	DIP
AD7521KN(KD)(TD)	12 Bits	±0.1%	±0.2%	10	500ns typ	C/I/M	I	TTL	DIP
AD7521LN(LD)(UD)	12 Bits	±0.05%	±0.1%	10	500ns typ	C/I/M	I		DIP
AD7531JN(JD)	12 Bits	±0.2%	±0.4%	10	500ns typ	C/I	I	CMOS &	DIP
AD7531KN(KD)	12 Bits	±0.1%	±0.2%	10	500ns typ	C/I	I	TTL	DIP
AD7531LN(LD)	12 Bits	±0.05%	±0.1%	10	500ns typ	C/I	I		DIP

NOTE
[1] C = 0 to +70°C, I = -25°C to +85°C, M = -55°C to +125°C

μP COMPATIBLE SPECIFICATIONS (maximum @ +25°C unless otherwise noted as typical)

Model	Resolution	Relative Accuracy	Differential Nonlinearity	Gain T.C. ppm/°C	Settling Time	Temp Range[1]	I/V Out	Input Logic	Package
AD558JD(SD)(SD/883B)	8 Bits	±1/2LSB	Monotonicity	±2LSB	800ns typ	C/M	V	TTL &	DIP
AD558KD(TD)(TD/883B)	8 Bits	±1/4LSB	Guaranteed	±2LSB	800ns typ	C/M	V	CMOS	DIP
AD7524JN(AD)(SD)	8 Bits	±0.2%	Monotonicity	10	100ns	C/I/M	I	TTL &	DIP
AD7524KN(BD)(TD)	8 Bits	±0.1%	Guaranteed	10	100ns	C/I/M	I	CMOS	DIP
AD7524LN(CD)(UD)	8 Bits	±0.05%		10	100ns	C/I/M	I		DIP
AD7522JN(JD)(SD)	10 Bits	±0.2%	±0.4%	10	500ns typ	C/I/M	I	TTL &	DIP
AD7522KN(KD)(TD)	10 Bits	±0.1%	±0.2%	10	500ns typ	C/I/M	I	CMOS	DIP
AD7522LN(LD)(UD)	10 Bits	±0.05%	±0.1%	10	500ns typ	C/I/M	I		DIP
DUAL MULTIPLYING									
AD7528JN(AQ)(SD)	8 Bits	±1LSB	±1LSB	±35[2]	200ns[2]	C/I/M	I	TTL &	DIP
AD7528KN(LN)	8 Bits	±1/2LSB	±1LSB	±35[2]	200ns[2]	C	I	CMOS	DIP
AD7528BQ(CQ)	8 Bits	±1/2LSB	±1LSB	±35[2]	200ns[2]	I	I	TTL &	DIP
AD7528TD(UD)	8 Bits	±1/2LSB	±1LSB	±35[2]	200ns[2]	M	I	CMOS	DIP
SYSTEMS DAC[3]									
AD7527KN(BD)(TD)	10 Bits	±1LSB	±2LSB	5	–	C/I/M	I	CMOS	DIP
AD7527LN(CD)(UD)	10 Bits	±0.5LSB	±1LSB	5	–	C/I/M	I	CMOS	DIP
AD7527GLN(GCD)(GUD)	10 Bits	±0.5LSB	±1LSB	5	–	C/I/M	I	CMOS	DIP

NOTES
[1] C = 0 to +70°C, I = -25°C to +85°C, M = -55°C to +125°C
[2] +15V supply
[3] Has double-buffered latches, data readback, data override, L/R - justified data, increment/decrement

HIGH PERFORMANCE SPECIFICATIONS (maximum @ +25°C unless otherwise noted as typical)

Model	Resolution	Relative Accuracy	Differential Nonlinearity	Gain T.C. ppm/°C	Settling Time	Temp Range[1]	I/V Out	Input Logic	Package
AD563JD-BIN/BCD	12 Bits/3 Digits	±1/2LSB	±1/2LSB	50	1.5μs typ	C	I	TTL &	DIP
AD563KD(SD)(TD)-BIN/BCD	12 Bits/3 Digits	±1/4LSB	±1/2LSB	20/30/10	1.5μs typ	C/M	I	CMOS	DIP
AD565JD(SD)(SD/883B)	12 Bits	±1/2LSB	±3/4LSB	30	400ns	C/M/M	I	TTL	DIP
AD565KD(TD)(TD/883B)	12 Bits	±1/4LSB	±1/2LSB	20/15/15	400ns	C/M/M	I		DIP
AD565AJD(SD)(SD/883B)	12 Bits	±1/2LSB	±3/4LSB	50/30/30	250ns	C/M/M	I	TTL	DIP
AD565AKD(TD)(TD/883B)	12 Bits	±1/4LSB	±1/2LSB	20/15/15	250ns	C/M/M	I	TTL	DIP
AD DAC87-CBI-I(/883B)	12 Bits	±1/2LSB	±3/4LSB	25	3μs	M/M	I	TTL &	DIP
AD DAC87-CBI-V(/883B)	12 Bits	±1/2LSB	±3/4LSB	25	300ns	M/M	V	CMOS	DIP
AD370JN(JD)	12 Bits	±1LSB			35μs	C/C	V	TTL &	DIP
AD370KN(KD)(SD)(SD/883B)	12 Bits	±1/2LSB	Monotonic		35μs	C/C/M/M	V	CMOS	DIP
AD371JN(JD)	12 Bits	±1LSB			35μs	C/C	V	TTL &	DIP
AD371KN(KD)(SD)(SD/883B)	12 Bits	±1/2LSB	Monotonic		35μs	C/C/M/M	V	CMOS	DIP

NOTES
[1] C = 0 to +70°C, M = -55°C to +125°C

HIGH PERFORMANCE DACS FEATURE SELECTION CHART

		HIGH PERFORMANCE								FAST			MULTIPLYING
									µP COMPATIBLE				
		AD563	AD DAC87	AD370	AD371	AD DAC71/ DAC72	AD7546	AD3860	AD567	AD565	AD565A	AD566	AD566A
Resolution	0.375dB Steps to 88.5dB												
	1.5dB Steps to 88.5dB												
	8 Bits												
	10 Bits												
	12 Bits	•	•	•	•		•	•	•	•	•	•	•
	16 Bits					•							
	18 Bits												
Output Format	Current	•	•			•			•	•	•	•	•
	Voltage		•	•	•	•	•	•					
Internal Reference		•	•	•	•	•		•	•	•	•		
Multiplication Capability	2 Quadrant						•					•	•
	4 Quadrant												
Logic Compatible with	TTL,	•	•	•	•	•	•	•	•	•	•	•	•
	CMOS	•	•	•	•	•	•						
Input Code	Binary	•	•	•	•	•	•	•	•	•	•	•	•
	BCD	•	•										
Second Source		•	•	•	•	•		•		•	•	•	•
Single Power Supply													
Input Data Latch Structure	Serial												
	Parallel						•	•	•				
Operating Temperature Ranges[1]	C = 0 to +70°C	•	•	•	•	•	•	•	•	•	•	•	•
	I = -25°C to +85°C					•	•						
	M = -55°C to +125°C	•	•	•	•			•	•	•	•	•	•
Low Power				•	•		•	•					
Input/Output Isolation													
Dice Availability									•		•		•

NOTE
[1] C = Commercial I = Industrial M = Military

HIGH PERFORMANCE DACS FEATURE SELECTION CHART (Continued)

		HIGH PERFORMANCE								SPECIAL PURPOSE				
		MULTIPLYING				µP BUS COMPATIBLE				LOG DAC™ ATTENUATORS				QUAD DAC
		AD562	AD7541	AD7541A	AD7525	AD7542	AD7543	AD7541[1]	AD7545	AD7115	AD7111	AD7110	AD7118	AD390
Resolution	0.1dB Steps to 19.9dB									•	•			
	0.375dB Steps to 88.5dB											•	•	
	1.5dB Steps to 88.5dB													
	8 Bits													
	10 Bits				•									
	12 Bits	•	•	•		•	•	•	•					•
	16 Bits													
	18 Bits													
Output Format	Current	•	•	•	•	•	•	•	•	•	•	•	•	
	Voltage													•
Internal Reference														•
Multiplication Capability	2 Quadrant	•	•	•	•	•	•	•	•	•	•	•	•	•
	4 Quadrant		•	•	•	•	•	•	•					•
Logic Compatible with	TTL	•	•	•		•	•	•	•	•	•		•	•
	CMOS	•	•	•	•	•	•	•	•	•	•	•	•	
Input Code	Binary	•	•	•		•	•	•	•		•	•	•	•
	BCD	•			•					•				
Second Source		•	•	•										
Single Power Supply										•	•		•	
Input Data Latch Structure	Serial						•							
	Parallel					•		•	•	•	•			•
Operating Temperature Ranges[2]	C = 0 to +70°C	•	•	•	•	•	•	•	•	•		•	•	•
	I = -25°C to +85°C		•	•	•	•	•	•	•	•			•	
	M = -55°C to +125°C	•	•	•	•	•	•	•	•	•			•	•
Low Power			•	•	•	•	•	•	•	•	•	•	•	
Input/Output Isolation														
Dice Availablity			•			•	•							

NOTE
[1] Six-Stage FIFO Input Register [2] C = Commercial I = Industrial M = Military

μP BUS COMPATIBLE
SPECIFICATIONS (maximum @ +25°C unless otherwise noted as typical)

Model	Resolution	Relative Accuracy	Differential Nonlinearity	Gain T.C. ppm/°C	Settling Time	Temp Range[1]	I/V Out	Input Logic	Package
AD567J(S)(S/883B)	12 Bits	±1/2LSB	±3/4LSB	50/30/30	500ns	C/M/M	I	TTL &	DIP
AD567K(T)(T/883B)	12 Bits	±1/4LSB	±1/2LSB	20	500ns	C/M/M	I	CMOS	DIP
AD3860K	12 Bits	±1/2LSB	±1LSB	±10	5μs[2]	C	V	TTL	DIP
AD3860S	12 Bits	±1/2LSB	GMOT[3]	±10	5μs[2]	M	V	TTL	DIP
AD7542JN(AD)(AD/883B)(SD)(SD/883B)	12 Bits	±1LSB	±0.048%	5	2μs	C/I/I/M/M	I	TTL CMOS	DIP
AD7542KN(BD)(BD/883B)(TD)(TD/883B)	12 Bits	±1/2LSB	±0.024%	5	2μs	C/I/I/M/M	I	CMOS	DIP
AD7543JN(AD)(AD/883B)(SD)(SD/883B)	12 Bits	±1LSB	±0.048%	5	2μs	C/I/I/M/M	I	CMOS	DIP
AD7543KN(BD)(BD/883B)(TD)(TD/883B)	12 Bits	±1/2LSB	±0.024%	5	2μs	C/I/I/M/M	I	CMOS	DIP
AD7544JN(AD)(SD)[4]	12 Bits	±1LSB	±0.048%	5	2μs	C/I/M	I	CMOS	DIP
AD7544KN(BD)(TD)[4]	12 Bits	±1/2LSB	±0.024%	5	2μs	C/I/M	I	CMOS	DIP
AD7544GKN(GBD)(GTD)[4]	12 Bits	±1/2LSB	±0.024%	5	2μs	C/I/M	I	CMOS	DIP
AD7545J(A)(S)	12 Bits	±2LSB	±4LSB	±5[5]		C/I/M	I	TTL &	DIP
AD7545K(B)(T)	12 Bits	±1LSB	±1LSB	±5[5]		C/I/M	I	CMOS	DIP
AD7545L(C)(U)	12 Bits	±1/2LSB	±1LSB	±5[5]		C/I/M	I		DIP
AD7545GL(GC)(GU)[6]	12 Bits	±1/2LSB	±1LSB	±5[5]		C/I/M	I		DIP
AD7546JN(AD)	16 Bits	±0.05% FSR	±0.006% FSR	±2	10μs typ[7]	C/I	V	TTL &	DIP
AD7546KN(BD)	16 Bits	±0.012% FSR	GMOT[3]	±2	10μs typ[7]	C/I	V	CMOS	DIP
LOG DAC™ STEP ATTENUATORS									
AD7111K(B)(T)	0.375dB	30dB ± 0.17dB	GMOT[8]			C/I/M	I	CMOS	DIP
AD7111L(C)(U)	0.375dB	36dB ± 0.17dB	GMOT[9]			C/I/M	I	CMOS	DIP
AD7115K(B)(T)	0.1dB	±0.05dB	Monotonic			C/I/M	I	TTL & CMOS	DIP
QUAD DAC (FOUR DACS IN ONE PACKAGE)									
AD390JD(SD)	12 Bits	±3/4LSB	GMOT[3]	±40/±10[10]	8μs	C/M	V	TTL &	DIP
AD390KD(TD)	12 Bits	±1/2LSB	GMOT[3]	±10/±5[10]	8μs	C/M	V	CMOS	DIP

NOTES
[1] C = 0 to +70°C, I = −25°C to +85°C, M = −55°C to +125°C
[2] To 0.01% for 10-V Step
[3] Guaranteed Monotonic Over Temperature
[4] Six-Stage FIFO Input Register
[5] 5 Volt Supply
[6] 2LSB max gain error (multiplying DAC)[5]
[7] To 0.00076% of final value
[8] 0 to −48dB at 0.375dB, 0 to −60dB at 0.75dB, 0 to −72dB at 1.5dB
[9] 0 to −54dB at 0.375dB, 0 to −72dB at 0.75dB, 0 to −88.5dB at 1.5dB
[10] Internal/External reference

HIGH RESOLUTION
SPECIFICATIONS (maximum @ +25°C unless otherwise noted as typical)

Model	Resolution	Relative Accuracy	Differential Nonlinearity	Gain T.C. ppm/°C	Settling Time	Temp Range[1]	I/V Out	Input Logic	Package
AD7546JN(AD)	16 Bits	±0.05%	±0.006%	±2	10μs typ[2]	C/I	V	CMOS or	DIP
AD7546KN(BD)	16 Bits	±0.012%	±0.0015%	±2	10μs typ[2]	C/I	V	TTL	DIP
AD DAC71	16 Bits	±0.003%	Note 3	±15	10/1μs[4]	C	V/I	TTL	DIP[5]
AD DAC71H	16 Bits	±0.003%	Note 3	±15	10/1μs[4]	C	V/I	TTL	DIP[5]
AD DAC72C	16 Bits	±0.003%	Note 3	±15	10/1μs[4]	C	V/I	TTL	DIP[5]
AD DAC72	16 Bits	±0.003%	Note 6	±15[6]	10/1μs[4]	I	V/I	TTL	DIP[5]

NOTES
[1] C = 0 to +70°C, I = -25°C to +85°C
[2] to 0.00076% of final value
[3] Guaranteed 14-bit monotonic 0 to +50°C
[4] Voltage/current, to ±0.003% FSR
[5] AD DAC71 polymer sealed, AD DAC71H and AD DAC72 hermetic
[6] Guaranteed 14-bit monotonic 0 to +70°C, Gain tempco ±15ppm/°C, T_{min} to +25°C, ±7ppm/°C, +25°C to T_{max}

SPECIAL PURPOSE
SPECIFICATIONS (maximum @ +25°C unless otherwise noted as typical)

Model	Resolution	Relative Accuracy	Differential Nonlinearity	Gain T.C. ppm/°C	Settling Time	Temp Range[1]	I/V Out	Input Logic	Package
LOG DAC™ STEP ATTENUATORS									
AD7110KN	1.5dB	±0.7dB, 0 to -48dB	Monotonic	NA	NA	0 to +50°C	I	CMOS	DIP
AD7118KN(BD)(TD)	1.5dB	±0.75dB, 0 to -42dB	Monotonic	NA	NA	C/I/M	I	CMOS & TTL	DIP
AD7118LN(CD)(UD)	1.5dB	±0.7dB, 0 to -48dB	Monotonic	NA	NA	C/I/M	I	CMOS & TTL	DIP

These devices are digitally controlled attenuators for use in high performance audio systems and wide dynamic range applications.

NOTE
[1] C = 0 to +70°C, I = -25°C to +85°C, M = -55°C to +125°C

MULTIPLYING

Model	Resolution	Relative Accuracy	Differential Nonlinearity	Gain T.C. ppm/°C	Settling Time	Temp Range[1]	I/V Out	Input Logic	Package
AD562KD(AD)-BIN	12 Bits	±1/2LSB	±1/2LSB	3	1.5μs typ	C/I	I	TTL &	DIP
AD562SD-BIN	12 Bits	±1/4LSB	±1/2LSB	3	1.5μs typ	M	I	CMOS	DIP
AD562KD(AD)-BCD	3 Digits	±1/2LSB	±1/2LSB	3	1.5μs typ	C/I	I		DIP
AD562SD-BCD	3 Digits	±1/10LSB	±1/2LSB	3	1.5μs typ	M	I		DIP
AD566JD(SD)(SD/883B)	12 Bits	±1/2LSB	±3/4LSB	10	400ns	C/M/M	I	TTL	DIP
AD566KD(TD)(TD/883B)	12 Bits	±1/4LSB	±1/2LSB	3	400ns	C/M/M	I		DIP
AD566AJD(SD)(SD/883B)	12 Bits	±1/2LSB	±3/4LSB	10	350ns	C/M/M	I	TTL	DIP
AD566AKD(TD)(TD/883B)	12 Bits	±1/4LSB	±1/2LSB	3	350ns	C/M/M	I	TTL	DIP
AD7541JN(AD)(SD)(SD/883B)	12 Bits	±1LSB	±2LSB	10	1μs	C/I/M/M	I	TTL &	DIP
AD7541KN(BD)(TD)(TD/883B)	12 Bits	±1/2LSB	±1LSB	10	1μs	C/I/M/M	I	CMOS	DIP
AD7541AJN(AQ)	12 Bits	±1LSB	±1LSB	5	0.6μs typ[2]	C/I	I	TTL &	DIP
AD7541AKN(BQ)	12 Bits	±1/2LSB	±1/2LSB	5	0.6μs typ[2]	C/I	I	CMOS	DIP
AD7541ASD(SD/883B)	12 Bits	±1LSB	±1LSB	5	0.6μs typ[2]	M/M	I		DIP
AD7541ATD(TD/883B)	12 Bits	±1/2LSB	±1/2LSB	5	0.6μs typ[2]	M/M	I		DIP
AD7525KN(BD)(TD)(TD/883B)	3 1/2 Digits	±1LSB	±1LSB	25	1μs	C/I/M/M	I	CMOS	DIP
AD7525LN(CD)(UD)(UD/883B)	3 1/2 Digits	±1/2LSB	±1/2LSB	25	1μs	C/I/M/M	I		DIP

NOTES
[1] C = 0 to +70°C, I = -25°C to +85°C, M = -55°C to +125°C
[3] Guaranteed Monotonic Over Temperature, -30°C to +85°C

ULTRA FAST/VIDEO DACS FEATURE SELECTION CHART

		CURRENT OUT										
		HDG-0405	HDG-0605	HDG-0805	HDS-0820	HDS-0810E	HDD-0810	HDD-0810C	HDS-1025	HDS-1015E	HDD-1015	AD9768
Settling Time to Resolution in Bits	<550ns											
	<210ns								•			
	<75ns											
	<21ns				•	•	•	•		•	•	
	<8ns	•	•	•								•
Resolution	4 Bits	•										
	6 Bits		•									
	8 Bits			•	•	•	•	•				•
	10 Bits								•	•	•	
	11 Bits											
	12 Bits											
Application	General Purpose				•	•	•		•	•	•	•
	Lowest Glitch	•	•	•				•				
	Multiplying											•
	Composite Video	•	•	•				•				
Output Format	Current	•	•	•	•	•	•	•	•	•	•	•
	Voltage											
Binary Logic	TTL				•				•			
	ECL	•	•	•		•	•	•		•	•	•
	Latched	•	•	•			•	•			•	
Single Power Supply		•	•	•		•	•	•		•	•	
Operating Temperature Ranges	0 to +70°C	•	•	•	•	•	•	•	•	•	•	
	-25°C to +85°C						•	•			•	
	-55°C to +125°C				•	•			•	•		•

ULTRA FAST/VIDEO DACS FEATURE SELECTION CHART (Continued)

		CURRENT OUT			VOLTAGE OUT			
		HDD-1015C	HDS-1250	HDS-1240E	HDH-0802	HDH-1003	HDH-1205	HDD-1206
Settling Time to Resolution in Bits	<2μs						•	•
	<210ns		•	•	•	•		
	<75ns							
	<21ns	•						
	<8ns							
Resolution	4 Bits							
	6 Bits							
	8 Bits				•			
	10 Bits	•				•		
	11 Bits							
	12 Bits		•	•			•	•
Application	General Purpose		•	•	•	•	•	
	Lowest Glitch							•
	Multiplying							
	Composite Video	•						
Output Format	Current	•	•	•				
	Voltage				•	•	•	•
Binary Logic	TTL		•		•	•	•	•
	ECL	•		•				
	Latched	•						•
Single Power Supply		•						
Operating Temperature Ranges	0 to +70°C	•	•	•	•	•	•	•
	-25°C to +85°C	•						
	-55°C to +125°C		•	•[1]	•	•	•	•

NOTE
[1] -55°C to +100°C

ULTRA FAST/VIDEO
SPECIFICATIONS (maximum @ +25°C unless otherwise noted as typical)

Model	Resolution	Relative Accuracy	Differential Nonlinearity	Gain T.C. ppm/°C Typical	Settling Time ns Typical	Temp Range[1]	I/V Out	Input Logic	Package
AD9768	8 Bits	±1/2LSB	GMOT[2]	80	5	M	I	ECL	DIP
HDG-0405[3,4]	4 Bits	±1/2LSB	GMOT[2]	25	4	C	I	ECL	DIP
HDG-0605[3,4]	6 Bits	±1/2LSB	GMOT[2]	25	6	C	I	ECL	DIP
HDG-0805[3,4]	8 Bits	±1/2LSB	GMOT[2]	25	8	C	I	ECL	DIP
HDS-0820(0820M)	8 Bits	±1/4LSB	GMOT[2]	30	20	C/M	I	TTL	DIP
HDS-0810E(0810EM)	8 Bits	±1/4LSB	GMOT[2]	80	10	C/M	I	ECL	DIP
HDD-0810(0810M)[4]	8 Bits	±1/4LSB	GMOT[2]	80	10	C/M	I	ECL	DIP
HDD-0810C(0810CM)[3,4]	8 Bits	±1/4LSB	GMOT[2]	80	10	C/M	I	ECL	DIP
HDS-1025(1025M)	10 Bits	±1/2LSB	GMOT[2]	30	25	C/M	I	TTL	DIP
HDS-1015E(1015EM)	10 Bits	±1/2LSB	GMOT[2]	80	15	C/M	I	ECL	DIP
HDD-1015(1015M)[4]	10 Bits	±1/2LSB	GMOT[2]	80	15	C/M	I	ECL	DIP
HDD-1015C(1015CM)[3,4]	10 Bits	±1/2LSB	GMOT[2]	80	15	C/M	I	ECL	DIP
HDS-1250(1250M)	12 Bits	±1/2LSB	GMOT[2]	30	35	C/M	I	TTL	DIP
HDS-1240E(1240EM)	12 Bits	±1/2LSB	GMOT[2]	25	35	C/MR	I	ECL	DIP
HDD-1206JW	12 Bits	±1/2LSB	GMOT[2]	40	60[5]	C	V	TTL	DIP
HDD-1206SM	12 Bits	±1/2LSB	GMOT[2]	40	60[5]	M	V	TTL	DIP
HDH-0802(0802M)	8 Bits	±1/4LSB	GMOT[2]	30	200	C/M	V	TTL	DIP
HDH-1003(1003M)	10 Bits	±1/2LSB	GMOT[2]	30	300	C/M	V	TTL	DIP
HDH-1205(1205M)	12 Bits	±1/2LSB	GMOT[2]	30	500	C/M	V	TTL	DIP

NOTES
[1] C = 0 to +70°C, I = -25°C to +85°C, M = -55°C to +125°C, MR = -55°C to +100°C
[2] Guaranteed Montonic Over Temperature
[3] Composite video
[4] Latched input
[5] 1LSB settling

ANALOG DEVICES

CMOS uP Compatible 10-Bit+ Sign ADC

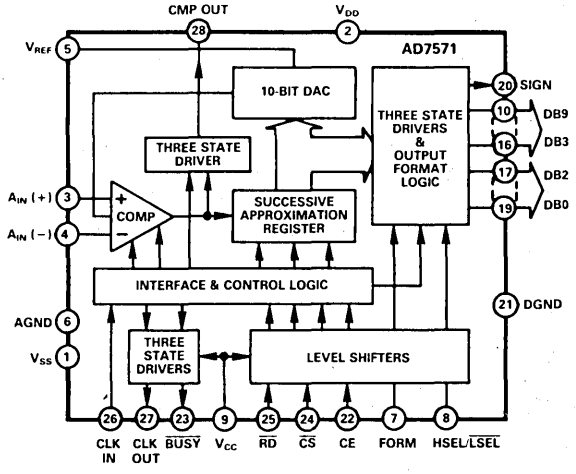
AD7571

PRELIMINARY TECHNICAL DATA

FEATURES

- 10-Bit Plus Sign Resolution
- No Missed Codes Over Full Temperature Range
- Conversion Time 80μs Typ
- Differential Analog Voltage Inputs, ±10V Range
- Serial and Parallel Data Outputs
- Easy Interface to All Microprocessors
- Internal Clock Oscillator

AD7571 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7571 is a low cost 10-bit plus sign CMOS A/D converter which uses the successive approximations technique to provide a typical A/D conversion time of 80μs. The device is designed for easy microprocessor interface allowing single or double byte reading over three-state outputs. Conversion results are also available in serial form allowing opto-isolated operation using as few as two wires for the interconnect.

A new differential analog input configuration is used in the AD7571 increasing the common-mode rejection performance and allowing the analog zero input voltage to be offset from true zero. Analog input voltage range is ±10V using a single positive reference.

PRODUCT HIGHLIGHTS

1. Pin Programmable Data Output Formats
   The output format for the 10 bits + sign data is pin programmable allowing full parallel, two byte (left justified) format. Serial output data is also available.
2. Improved Control Logic
   The AD7571 control logic is an improved version of that used in the highly successful AD7574. This allows the AD7571 to be operated as a memory mapped input device interfacing to the μP via the control lines $\overline{CS}$ (chip select) and $\overline{RD}$ (READ/$\overline{WRITE}$) control.
3. All Active Components on Chip
   The addition of a few passive support components makes the AD7571 a complete 10-bit plus sign converter requiring only a reference voltage and power supplies. An on chip clock is also provided but the device can run from an external clock if required.
4. Differential Analog Inputs
   The analog input voltage can be unipolar or bipolar with an input range of ±10V. The differential input allows asymmetric input voltage ranges to be easily accommodated.

ORDERING INFORMATION

Relative Accuracy (T_{min} to T_{max})	Temperature Range and Package		
	Plastic 0 to +70°C	Cerdip −25°C to +85°C	Side-Brazed Ceramic −55°C to +125°C
±1LSB	AD7571JN	AD7571AQ	AD7571SD
±1/2LSB	AD7571KN	AD7571BQ	AD7571TD

ANALOG DEVICES

Very Fast, Complete, MIL-Temp 12-Bit A/D Converter

AD578S,T

PRELIMINARY TECHNICAL DATA

FEATURES

Performance

- Complete 12-Bit A/D Converter with Reference and Clock
- Fast Successive Approximation Conversion: 4.5μs
- Buried Zener Reference for Long Term Stability and Low Gain T.C.: ±30ppm/°C max
- Max Nonlinearity: <±0.012%
- No Missing Codes Over Temperature
- Low Power: 775mW
- Military Temperature Range
- Hermetic Package

Versatility

- Positive-True Parallel or Serial Logic Outputs
- Short Cycle Capability
- "Z" Models for ±12 Volt Supplies

PRODUCT DESCRIPTION

The AD578 is a high speed low cost 12-bit successive approximation analog-to-digital converter that includes an internal clock, reference and comparator. Its hybrid IC design utilizes MSI digital and linear monolithic chips in conjunction with a 12-bit monolithic DAC to provide superior performance and versatility with IC size, price and reliability.

Important performance characteristics of the AD578 include a maximum linearity error at +25°C of ±0.012%, no missing codes, maximum gain temperature coefficient of ±30ppm/°C, and typical power dissipation of 775mW. The maximum conversion times of 4.5μs (T grade) and 6μs (S grade) make the AD578 an excellent choice in a variety of applications where system throughput rates from 166kHz to 222kHz are required. In addition, it may be short cycled to obtain faster conversion speeds at lower resolutions.

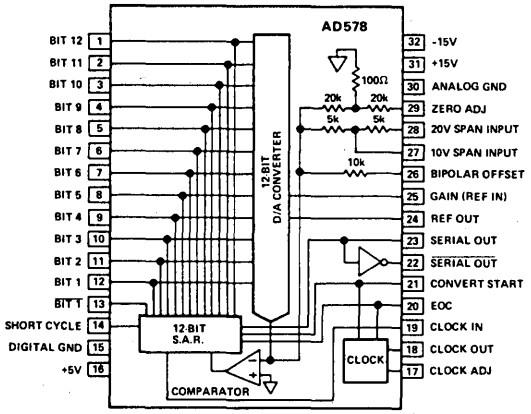
The design of the AD578 includes scaling resistors that provide analog input signal ranges of ±5V, ±10V, 0 to +10V or 0 to +20V. Adding flexibility and value is the +10V precision reference which can be used for external applications.

The AD578S and AD578T are available processed to MIL-STD-883B, Method 5008. Both are packaged in a hermetic 32-pin ceramic DIP. For 883B versions order AD578XX/883B.

AD578S, T ORDERING GUIDE

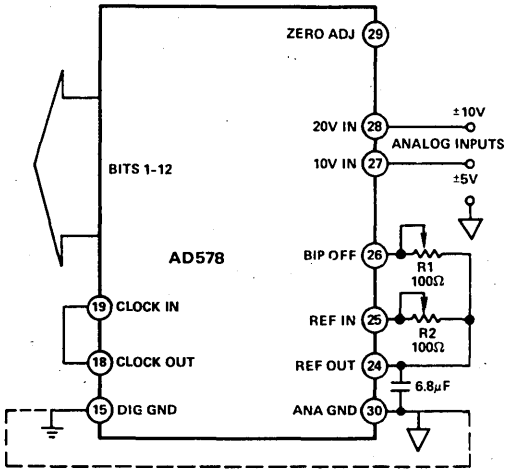
Model	Conversion Speed	Temperature Range	Supply Voltage
AD578SD	6μs	−55°C to +125°C	±15V, +5V
AD578TD	4.5μs	−55°C to +125°C	±15V, +5V
AD578ZSD	6μs	−55°C to +125°C	±12V, +5V
AD578ZTD	4.5μs	−55°C to +125°C	±12V, +5V

AD578 FUNCTIONAL BLOCK DIAGRAM AND PINOUT



PRODUCT HIGHLIGHTS

1. The AD578 is a complete 12-bit A/D converter. No external components are required to perform a conversion.
2. The fast conversion rate of the AD578 makes it an excellent choice for high speed data acquisition and digital signal processing applications.
3. The internal buried zener reference is laser trimmed to 10.00V ±0.1% and ±15ppm/°C typical T.C. The reference is available externally and can provide up to 1mA.
4. The scaling resistors are included on the monolithic DAC for exceptional thermal tracking.
5. Short cycle and external clock capabilities are provided for applications requiring faster conversion speeds and/or lower resolutions.
6. The integrated package construction provides high quality and reliability with small size and weight.



NOTES:
1. TO MINIMIZE NOISE THE REFERENCE OUTPUT (PIN 24) SHOULD BE DECOUPLED BY A 6.8μF CAPACITOR TO PIN 30.
2. EACH OF THE AD578'S SUPPLY TERMINALS (±15V AND +5V) SHOULD BE DECOUPLED BY A 10μF CAPACITOR IN PARALLEL WITH A 0.1μF CAPACITOR AS CLOSE TO THE AD578 AS POSSIBLE.
3. FOR AD578T GRADE 4.5μs CONVERSION SPEED, ADD A 3.32kΩ ±1% RESISTOR BETWEEN PINS 17 & 18.

Figure 1. Bipolar Input Connections

High Resolution 16-Bit A/D Converter

AD ADC71/AD ADC72

PRELIMINARY TECHNICAL DATA

FEATURES

- **Complete 16-Bit Converter With Reference and Clock**
- **±0.003% Maximum Nonlinearity**
- **No Missing Codes to 14 Bits Over Full Temp Range**
- **Fast Conversion – 35μs**
- **Short Cycle Capability**
- **Parallel or Serial Logic Outputs**
- **Low Cost**

PRODUCT DESCRIPTION

The AD ADC71 and AD ADC72 are high resolution 16-bit hybrid IC analog to digital converters including reference, clock, and laser-trimmed thin-film components. The package is a compact 32-pin bottom-brazed ceramic or hermetic ceramic (AD ADC72) DIP. The thin-film scaling resistors allow analog input ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V, and 0 to +20V.

Important performance characteristics of the devices are maximum linearity error of ±0.003% of FSR (AD ADC71K, AD ADC72K and B), and maximum conversion time of 50μs. This performance is due to innovative design and the use of proprietary monolithic D/A converter chips. Laser-trimmed thin-film resistors provide the linearity and wide temperature range for no missing codes.

The AD ADC71 and AD ADC72 provide data in both parallel and serial form with corresponding clock and status output. All digital inputs and outputs are DTL/TTL compatible.

PRODUCT HIGHLIGHTS

1. The AD ADC71 and AD ADC72 provide 16-bit resolution with maximum linearity error less than ±0.003% (±0.006% for J and A grades) at 25°C.
2. Conversion time is 35μs (50μs max) with short cycle capability.
3. The AD ADC72 (KD, BD) have no missing codes (to 14 bits) over the full specification temperature range.
4. Two binary codes are available on the AD ADC71 and AD ADC72 output. They are complementary straight binary (CSB) for unipolar input voltage ranges and complementary offset binary (COB) for bipolar input ranges. Complementary two's complement (CTC) coding may be obtained by inverting pin 1 (MSB).
5. The proprietary chips used in this hybrid design provide excellent stability over temperature and lower chip count for improved reliability.

ORDERING GUIDE

Model	Linearity Error (Max)	Specification Temp Range	Package
AD ADC71JW	±0.006% of FSR	0 to +70°C	Ceramic
AD ADC71KW	±0.003% of FSR	0 to +70°C	Ceramic
AD ADC72JD	±0.006% of FSR	0 to +70°C	Hermetic
AD ADC72KD	±0.003% of FSR	0 to +70°C	Hermetic
AD ADC72AD	±0.006% of FSR	−25°C to +85°C	Hermetic
AD ADC72BD	±0.003% of FSR	−25°C to +85°C	Hermetic

AD ADC71/AD ADC72 FUNCTIONAL BLOCK DIAGRAM

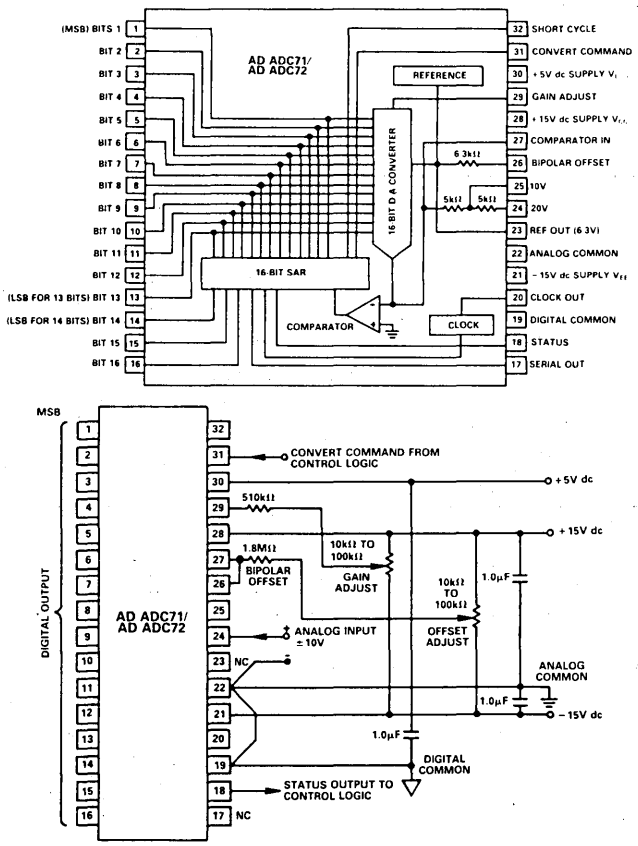
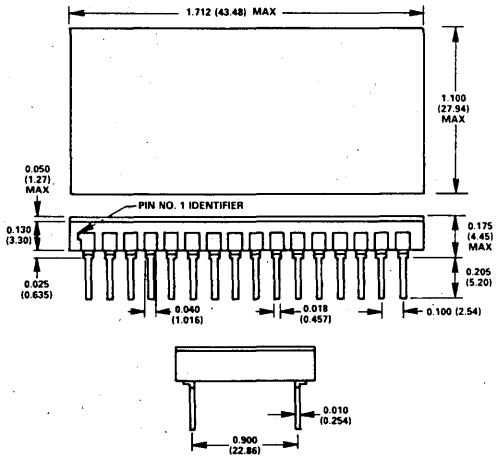


Figure 1. AD ADC71/AD ADC72 Connections for: ±10V Analog Input Parallel Data Output

MECHANICAL OUTLINE

Dimensions shown in inches and (mm).



LINEAR

Analog Devices

HIGH PERFORMANCE/HIGH RESOLUTION FEATURE SELECTION CHART

		GENERAL PURPOSE					μP BUS COMPATIBLE			MULTI-CHAN	HIGH PERFORMANCE				μP BUS COMPATIBLE				HIGH RESOLUTION	
		AD570	AD571	AD ADC80	AD673	AD573	AD7571	AD7574	AD7581	AD5200	AD5210	AD572	AD574/ AD574A	AD7550	AD7552	AD7555	AD ADC71	AD ADC72
Resolution	8 Bits	•			•			•	•									
	10 Bits		•			•												
	10 Bits & Sign						•											
	12 Bits			•						•	•	•	•					
	13 Bits													•	•			
	14 Bits																•	•
	16 Bits																	
	4 1/2 Digits															•		
	5 1/2 Digits															•		
Conversion Time	1800ms															•		
	50ms						•[1]		•[2]					•	•			
	100μs															•		
	50μs									•							•	•
	25μs	•	•	•	•	•					•	•	•					
	15μs							•			•							
Internal Reference		•	•	•	•	•				•	•	•	•				•	•
Ratiometric Capability							•	•	•	•	•			•	•	•		
Low Power							•	•	•					•	•	•		
Second Source				•						•	•		•				•	•
Logic	TTL	•	•	•	•	•	•		•	•	•	•	•	•	•		•	•
Compatibility	CMOS		•				•	•	•					•	•	•		
Operating	C = 0 to +70°C	•	•		•	•	•	•	•				•			•	•	•
Temperature	I = −25°C to +85°C			•			•	•	•	•	•	•		•	•	•		
Ranges	M = −55°C to +125°C	•	•		•	•	•	•		•	•	•	•				•	•
Dice Availability		•	•			•		•						•				

NOTES
[1] 80μs conversion time
[2] 66.6μs/channel

GENERAL PURPOSE SPECIFICATIONS (maximum @ +25°C unless otherwise noted)

Model	Resolution	Relative Accuracy	Differential Nonlinearity	Gain T.C. ppm/°C	Conversion Time	Logic	Temp Range[1]	Package
AD570JD	8 Bits	±1/2LSB	Note 2	176	40μs	TTL	C	DIP
AD570SD(SD/883B)	8 Bits	±1/2LSB	Note 2	80	40μs	TTL	M	DIP
AD571JD(SD)(SD/883B)	10 Bits	±1/2LSB	Note 3	88/50/50	40μs	TTL &	C/M/M	DIP
AD571KD	10 Bits	±1/2LSB	Note 2	44	40μs	CMOS	C	DIP
AD ADC80-10(Z)	10 Bits	±1/2LSB	±1/2LSB	30	21μs	TTL	I	DIP
AD ADC80-12(Z)	12 Bits	±1/2LSB	±1/2LSB	30	25μs	TTL	I	DIP
μP COMPATIBLE								
AD673J	8 Bits	±1/2LSB	Note 2	2[4]	30μs	TTL	C	DIP
AD673S	8 Bits	±1/2LSB	Note 2	2[4]	30μs	TTL	M	DIP
AD7574JN(AD)(SD)(SD/883B)	8 Bits	±3/4LSB	±7/8LSB	Note 5	15μs	CMOS	C/I/M/M	DIP
AD7574KN(BD)(TD)(TD/883B)	8 Bits	±1/2LSB	±3/4LSB	Note 5	15μs	CMOS	C/I/M/M	DIP
AD573J	10 Bits	±1LSB	Note 6	4[4]	20μs	TTL	C	DIP
AD573K	10 Bits	±1/2LSB	Note 2	2[4]	20μs	TTL	C	DIP
AD573S	10 Bits	±1LSB	Note 2	5[4]	20μs	TTL	M	DIP
AD7571JN	10 Bits & Sign	±1LSB	Note 2	5[4]	80μs	TTL &	C	DIP
AD7571KN	10 Bits & Sign	±1/2LSB	Note 2	4[4]	80μs	CMOS	C	DIP
AD7571AQ	10 Bits & Sign	±1LSB	Note 2	5[4]	80μs	TTL &	I	DIP
AD7571BQ	10 Bits & Sign	±1/2LSB	Note 2	4[4]	80μs	CMOS	I	DIP
AD7571SD	10 Bits & Sign	±1LSB	Note 2	5[4]	80μs	TTL &	M	DIP
AD7571TD	10 Bits & Sign	±1/2LSB	Note 2	4[4]	80μs	CMOS	M	DIP
AD574AJD	12 Bits	±1LSB	Note 7	9[4]	35μs	TTL	C	DIP
AD574AKD	12 Bits	±1/2LSB	Note 2	5[4]	35μs	TTL	C	DIP
AD574ALD	12 Bits	±1/2LSB	Note 2	2[4]	35μs	TTL	C	DIP
AD574ASD	12 Bits	±1LSB	Note 7	20[4]	35μs	TTL	M	DIP
AD574ATD	12 Bits	±1/2LSB	Note 2	10[4]	35μs	TTL	M	DIP
AD574AUD	12 Bits	±1/2LSB	Note 2	5[4]	35μs	TTL	M	DIP
AD7552	12 Bits & Sign	1 Count	Note 2	1[4]	160[8]	TTL & CMOS	C	DIP
MULTI-CHANNEL								
AD7581JN(AD)[9]	8 Bits	±1 7/8LSB	±1 7/8LSB	Note 5	66.6μs[10]	TTL &	C/I	DIP
AD7581KN(BD)[9]	8 Bits	±3/4LSB	±7/8LSB	Note 5	66.6μs[10]	CMOS	C/I	DIP
AD7581LN(CD)[9]	8 Bits	±1/2LSB	±3/4LSB	Note 5	66.6μs[10]		C/I	DIP
HIGH PERFORMANCE								
AD5200BD(BD/883B) Series	12 Bits	±1/2LSB	Note 2	Note 11	50μs	TTL	I	DIP
AD5200TD(TD/883B) Series	12 Bits	±1/2LSB	Note 2	Note 11	50μs	TTL	M	DIP
AD574JD(SD)(SD/883B)	12 Bits	±1/2LSB	±1LSB	50	35μs	TTL	C/M/M	DIP
AD574KD(LD)	12 Bits	±1/2LSB	Note 2	27/10	35μs	TTL	C	DIP
AD574TD(TD/883B)(UD)(UD/883B)	12 Bits	±1/2LSB	Note 2	25/12.5	35μs	TTL	M	DIP
AD572AD(BD)	12 Bit	±1/2LSB	±1/2LSB	30/15	25μs	TTL	I	DIP
AD572SD(SD/883B)	12 Bits	±1/2LSB	±1/2LSB	15	25μs	TTL	M	DIP
AD5211B, AD5212B	12 Bits	±1/2LSB	Note 2	0.4%[12]	13μs	TTL	I	DIP
AD5211T, AD5212T	12 Bits	±1/2LSB	Note 2	0.4%[12]	13μs	TTL	M	DIP
AD5214B, AD5215B	12 Bits	±1/2LSB	Note 2	0.1%[12]	13μs	TTL	I	DIP
AD5214T, AD5215T	12 Bits	±1/2LSB	Note 2	0.1%[12]	13μs	TTL	M	DIP

NOTES
[1] C = 0 to +70°C, I = −25°C to +85°C, M = −55°C to +125°C
[2] No missing codes over temperature
[3] No missing codes
[4] Gain error in LSB, T_{min} to T_{max}, max
[5] ±2LSB max gain change from +25°C to T_{min} or T_{max}
[6] No missing codes over temperature, 9-bit resolution
[7] No missing codes over temperature, 11-bit resolution
[8] Milliseconds, typical
[9] 8 channels
[10] Per channel
[11] Absolute Accuracy = ±0.2%/0.1% of full scale input voltage over temperature range
[12] Absolute accuracy error, T_{min} to T_{max}, max

HIGH RESOLUTION SPECIFICATIONS (maximum @ +25°C unless otherwise noted)

Model	Resolution	Relative Accuracy	Differential Nonlinearity	Gain T.C. ppm/°C	Conversion Time	Logic	Temp Range[1]	Package
AD7550BD	13 Bits	±1LSB		1	40ms typ	TTL & CMOS	I	DIP
AD7555KN(BD)	5 1/2 Digits	±10 Counts	Note 2	0.2	1760ms	CMOS	C/I	DIP
	4 1/2 Digits	±1 Count	Note 3	0.2	610ms	CMOS		
AD ADC71JW	16 Bits	±0.006[5]	Note 6	15	50μs	DTL & TTL	C	DIP
AD ADC71KW	16 Bits	±0.003[5]	Note 7	15	50μs	DTL & TTL	C	DIP
AD ADC72JD(AD)	16 Bits	±0.006[5]	Note 6	20(15)	50μs	DTL & TTL	C(I)	DIP
AD ADC72KD(BD)	16 Bits	±0.003[5]	Note 7	20(15)	50μs	DTL & TTL	C(I)	DIP

NOTES
[1] C = 0 to +70°C; I = -25°C to +85°C
[2] Count uncertainty due to noise: ±2 counts
[3] Count uncertainty due to noise: ±1/2 count
[4] No missing codes
[5] % of FSR
[6] No missing codes (to 13 bits) over temperature (0 to +50°C - JW; 0 to +70°C - JD; -25°C to +85°C - AD)
[7] No missing codes (to 14 bits) over temperature (+10°C to +40°C - KW; 0 to +70°C - KD; -25°C to +85°C - BD)

HIGH SPEED/VIDEO FEATURE SELECTION CHART

		HIGH SPEED											
		AD579	AD578	AD ADC84/85[1]	AD5240[1]	HAS-0802	HAS-1002	HAS-1202	MAH-0801	MAH-1001	MAS-1202	AD6020	AD5010
Resolution	6 Bits					•			•			•	•
	8 Bits									•			
	9 Bits												
	10 Bits	•		•			•				•		
	12 Bits		•	•	•			•	•	•	•		
Conversion Time	≤8μs		•	•	•								
	≤3μs	•	•			•	•	•					
	≤1.1μs								•	•	•		
Word Rate	≥5MHz												
	≥16MHz											•	
	≥50MHz												•
	≥100MHz												
Internal Reference		•	•	•	•	•	•	•	•	•	•		
Logic Compatibility	TTL	•	•	•	•	•	•	•	•	•	•		
	ECL											•	•
Operating Temperature Ranges	C = 0 to +70°C	•	•	•	•	•	•	•	•	•	•	•	•
	I = -25°C to +85°C			•		•	•	•					
	M = -55°C to +125°C	•	•	•	•								

NOTES
[1] Second Source
[2] Complete with Track and Hold.

HIGH SPEED SPECIFICATIONS (maximum @ +25°C unless otherwise noted)

Model	Resolution	Relative Accuracy	Differential Nonlinearity	Gain T.C. ppm/°C	Conversion Time, min	Logic	Temp Range[1]	Package
AD578JN(JD)	12 Bits	±1/2LSB	Note 2	30	6μs	TTL	C	DIP
AD578KN(KD)	12 Bits	±1/2LSB	Note 2	30	4.5μs	TTL	C	DIP
AD578LN(LD)	12 Bits	±1/2LSB	Note 2	30	3μs	TTL	C	DIP
AD578SD(SD/883B)	12 Bits	±1/2LSB	Note 2	50	6μs	TTL	M	DIP
AD578TD(TD/883B)	12 Bits	±1/2LSB	Note 2	30	4.5μs	TTL	M	DIP
AD5240KD	12 Bits	±1/2LSB	Note 2	30	5	TTL	C	DIP
AD5240SD	12 Bits	±1/2LSB	Note 2	25	5	TTL	M	DIP
AD ADC84-10(84-12)	10/12 Bits	±1/2LSB	Note 2	30/30	6/10	TTL	C	DIP
AD ADC85C-10(85C-12)	10/12 Bits	±1/2LSB	Notes 2 & 3	40/25	6/10	TTL	C	DIP
AD ADC85-10(85-12)	10/12 Bits	±1/2LSB	Notes 2 & 3	20/15	6/10	TTL	I	DIP
AD ADC85S-10(85S-12)	10/12 Bits	±1/2LSB	Note 2	25	8/10	TTL	M	DIP
AD579JN	10 Bits	±1/2LSB	Note 2	30	2.2	TTL	C	DIP
AD579KN	10 Bits	±1/2LSB	Note 2	30	1.8	TTL	C	DIP
AD579BD	10 Bits	±1/2LSB	Note 2	30	1.8	TTL	I	DIP
AD579TD	10 Bits	±1/2LSB	Note 2	30	1.8	TTL	M	DIP
HAS-0802	8 Bits	±1/4LSB	Note 2	30 typ	1.2μs typ	TTL	C[4]	DIP
HAS-1002	10 Bits	±1/2LSB	Note 2	30 typ	1.4μs typ	TTL	C[4]	DIP
HAS-1202	12 Bits	±1/2LSB	Note 2	30 typ	2.2μs typ	TTL	C[4]	DIP

NOTES
[1] C = 0 to +70°C, I = -25°C to +85°C, M = -55°C to +125°C
[2] No missing codes over temperature
[3] No missing codes
[4] Extended temperature ranges available

IC ADC FLASH ENCODERS SPECIFICATIONS (typical @ +25°C unless otherwise noted)

Model	Resolution	Relative Accuracy %	Aperture Uncertainty ps max	Word Rate	Output Code	Temperature Range °C	Size & Package Inches	Input Voltage Volts	Input Impedance
AD6020KD	6 Bits	±1/8LSB	20	dc to 50MHz	BIN	0 to +70	16-Pin DIP	±2.5 max	25pF[1]
AD5010KD	6 Bits	±1/8LSB	20	dc to 100MHz	BIN	0 to +70	16-Pin DIP	±2.5 max	25pF[1]

NOTE
[1] Input Capacitance

V/F CONVERTERS
SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise noted)

	High Performance 500kHz	Wide Band 1MHz	Economy/Versatile 0 to 150kHz
Model	ADVFC32K(B)(S)	AD650J(K)(S)	AD537JH(KH)(SH[1])(JD)(KD)(SD[1])
Analog Input			
Voltage Signal Range - V min	0 to -10V	0 to -10V	$-V_S$ to ($+V_S$ -4V) min
Current Signal Range - mA min	0 to +0.25	0 to +0.25	0.1μA to 1000μA
Overrange - % min	–	–	100
Accuracy			
Nonlinearity, max - at rate F.S. range			@ F = 10kHz
Voltage Input - %	±0.2	±0.5(±0.1)(±0.2)	
Current Input - %	±0.2	±0.5(±0.1)(±0.2)	0.15(0.07)(0.07)(0.15)(0.07)(0.07)
Gain vs. temperature, ppm/°C, max	150(100)(150)	150(100)(150)	±150(±50)(±150)(±150)(±50)(±150)
Input Offset Voltage - mV	±4 max	±4 max	±5(±2)(±2)(±5)(±2)(±2) max
vs. Temperature (0 to +70°C) - μV/°C	±30 max	±30 max	±5(±1)(±10 max)[3] (±5)(±1)(±10 max)[3]
Response			
Settling Time - μs	1	1	–
Overload Recovery - ms	1μs	1μs	–
Output			
Waveform	← TRAIN OF TTL/DTL COMPATIBLE PULSES →		Symmetrical
Pulse Width - μs	0.1 to 0.15/f max	0.1 to 0.15/f max	Square Wave, TTL, DTL, CMOS,
Pulse Polarity	← POSITIVE →		ECL, HNIL Compatible by Selection
Logic "1" (HIGH) Level - V min	Compatible by	Compatible by	of External Resistor
Logic "0" (LOW) Level) Level - V max	Resistor Selection	Resistor Selection	
Power Supply			
Voltage, Rated Performance - V dc	±9 to ±18	±9 to ±18	+5 to +36 or ±5 to ±18
Current, Quiescent - mA	6	6	1.2
Temperature Range[3]			
Rated Performance - °C	C(I)(M)	C(C)(M)	C(C)(M)(C)(C)(M)
Case Size - Inches	D–14-Pin DIP H–TO-100 Can	D–14-Pin DIP	D–14-Pin DIP: H–TO-100 Can

NOTES
[1] Processing to MIL-STD-883 Level B is available. Consult factory for pricing.
[3] Guaranteed over -55°C to +125°C temperature range
[2] C = 0 to +70°C, M = -55°C to +125°C

MULTIPLEXERS AND SWITCHES

SPECIFICATIONS
(T_A = +25°C, V_{SUPPLY} = ±15V unless otherwise noted)

Type[1]	Function	R_{ON} Ω, max	Off Leakage nA, max	Temp Range[2,3]	Logic Compatibility
AD7501JN(JD)			10	C/I	CMOS
AD7501KN(KD)	8-Channel	300	10	C/I	TTL/CMOS
AD7501SD			5	M	TTL/CMOS
AD7502JN(JD)	Dual		5	C/I	CMOS
AD7502KN(KD)	4-Channel	300	5	C/I	TTL/CMOS
AD7502SD	(differential)		3	M	TTL/CMOS
AD7503JN(JD)			10	C/I	CMOS
AD7503KN(KD)	8-Channel	300	10	C/I	TTL/CMOS
AD7503SD			5	M	TTL/CMOS
AD7506JN(JD)		450	20	C/I	CMOS
AD7506KN(KD)	16-Channel	450	20	C/I	TTL/CMOS
AD7506SD		400	10	M	CMOS
AD7506TD		400	10	M	TTL/CMOS
AD7507JN(JD)	Dual	450	10	C/I	CMOS
AD7507KN(KD)	8-Channel	450	10	C/I	TTL/CMOS
AD7507SD	(differential)	400	5	M	CMOS
AD7507TD		400	5	M	TTL/CMOS

NOTES
[1] Suffix "N": plastic DIP; Suffix "D": ceramic DIP
[2] C: Commerical (0 to +70°C)
I: Industrial (-25°C to +85°C)
M: Military (-55°C to +125°C)
[3] MIL-STD-883 Level B processing available on all I/M versions. Consult factory for pricing.

SPECIFICATIONS
(T_A = +25°C, V_{SUPPLY} = ±15V unless otherwise noted)

Type[1]	Function	R_{ON} Ω, max	OFF Leakage	Temp Range[2,3]	Logic Compatibility
ADG200CJ		80	5nA, max	C	TTL/CMOS
ADG200BP		80	5nA, max	I	TTL/CMOS
ADG200BA	Dual SPST	80	5nA, max	I	TTL/CMOS
ADG200AP		70	2nA, max	M	TTL/CMOS
ADG200AA		70	2nA, max	M	TTL/CMOS
ADG201CJ		100	5nA, max	C	TTL/CMOS
ADG201BP	Quad SPST	100	5nA, max	I	TTL/CMOS
ADG201AP		80	1nA, max	M	TTL/CMOS
AD7510DIJN(JD)			5nA, max	C/I	CMOS
AD7510DIKN(KD)	Quad SPST Note 4	100	5nA, max	C/I	TTL/CMOS
AD7510DISD			3nA, max	M	TTL/CMOS
AD7511DIJN(JD)			5nA, max	C/I	CMOS
AD7511DIKN(KD)	Quad SPST Note 4	100	5nA, max	C/I	TTL/CMOS
AD7511DISD			3nA, max	M	CMOS
AD7511DITD			3nA, max	M	TTL/CMOS
AD7512DIJN(JD)			15nA, max	C/I	CMOS
AD7512DIKN(KD)	Dual SPDT Note 4	100	15nA, max	C/I	TTL/CMOS
AD7512DISD			9nA, max	M	CMOS
AD7512DITD			9nA, max	M	TTL/CMOS
AD7590DIKN	Quad SPST	90	5nA, max	C	TTL/CMOS
AD7590DIBD	with Data	90	5nA, max	I	TTL/CMOS
AD7591DIKN	Latches	90	5nA, max	C	TTL/CMOS
AD7591DIBD		90	5nA, max	I	TTL/CMOS
AD7592DIKN	Dual SPDT	90	5nA, max	C	TTL/CMOS
AD7592DIBD	with Data Latches	90	5nA, max	I	TTL/CMOS

NOTES
[1] Suffixes: N - Plastic DIP
P, D - Ceramic DIP
A, H - TO-100
[2] C: Commercial (0 to +70°C)
I: Industrial (-25°C to +85°C)
M: Military (-55°C to +125°C)
[3] MIL-STD-883 Level B processing available on selected devices. Consult factory for pricing and availability.
[4] Dielectrically isolated features latchup-free overvoltage proof operation.
[5] V_{DD} - V_{SS} (supply voltages) = +15V
[6] V_{DD} (supply voltage) = 8V

ANALOG DEVICES

Ultra High Precision +10.000 Volt Reference

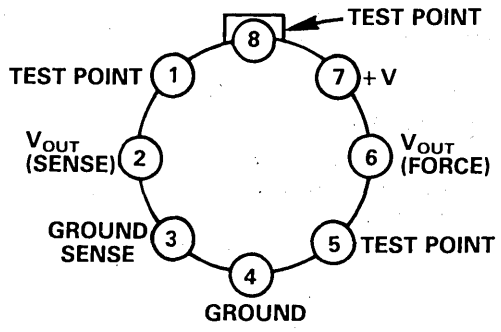
AD2720

PRELIMINARY TECHNICAL DATA

FEATURES

- **Laser Trimmed to High Accuracy: +10.000V ±1mV**
- **Low Temperature Coefficient: 1ppm/°C**
- **Excellent Long Term Stability: 25ppm/1000 Hrs.**
- **MIL Temperature Range Available (−55°C to +125°C)**
- **MIL-STD-883B Screening Available**
- **Low Noise (30μV p-p)**
- **Short Circuit Protected**
- **Low Power (90mW)**
- **Single Supply Operation**
- **Small Size (Standard TO-99 Package)**
- **Output and Ground Sense Provision**

AD2720 PINOUT DIAGRAM



TO-99 STYLE
TOP VIEW

PRODUCT DESCRIPTION

The AD2720 is a temperature compensated voltage reference which provides a precise +10.000V output from an unregulated input level from +14.25 to +15.75 volts. Active laser trimming is used to achieve this high precision, which eliminates the need for any external adjustments. The proprietary design results in ultra high precision performance previously available only in oven-regulated modules. The 1.0mV maximum initial error and 1ppm/°C guaranteed maximum temperature coefficient of the AD2720CH represents the best performance available without using power hungry ovens or heated substrates for temperature regulation.

The AD2720 precision 10.000 volt reference offers the user unequalled accuracy and stability with performance guaranteed over the −25°C to +85°C (AD2720AH, BH, CH) and −55°C to +125°C (AD2720SH and AD2720TH) temperature ranges. These devices combine the recognized advantages of thin film technology and active laser trimming with a unique patent pending circuit design, to provide an excellent reference for use in applications requiring high accuracy and stability.

The AD2720 is recommended for use as a reference for 12-, 14- and 16-bit D/A converters which can use an external reference. The device is also suitable for many types of high resolution A/D converters, either successive approximation or integrating designs. The 5mA output drive capability of the device also makes the AD2720 ideal for use as a master system reference.

PRODUCT HIGHLIGHTS

1. Active laser trimming results in very high accuracy over the full temperature range without the use of external components. The AD2720CH has a maximum deviation from 10.000 volts of ±1.0mV at 25°C with no external adjustments.

   The AD2720TH has a maximum deviation from 10.000 volts of ±1.0mV at 25°C, and a temperature coefficient of ±2ppm/°C (max) over −55°C to +125°C.
2. The AD2720 is well suited for a broad range of applications requiring an accurate, stable reference source such as data converters, test and measurement systems, and calibration standards.
3. The performance of the AD2720 is achieved by a proprietary design and close control over the manufacturing process, and eliminates the need for temperature-controlled ovens or heated substrates to provide stability.
4. The AD2720 is packaged in a small size (standard TO-99) package.
5. Output and ground sense provisions eliminate the problems of ground loops and load regulation errors.
6. Low power consumption insures high reliability and extended temperature range performance.

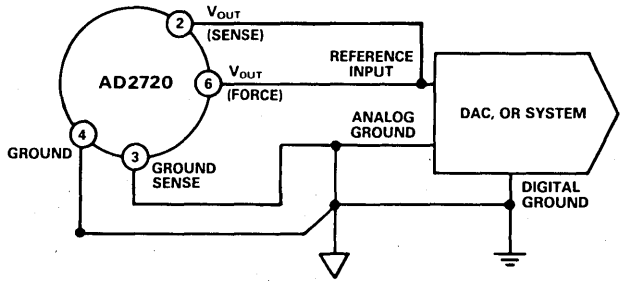


Figure 1. Basic Connections for V_{OUT} (Force and Sense) and Grounding

LINEAR

Analog Devices

INTEGRATED CIRCUIT REFERENCES

The accuracy of all measurements is determined by the reference employed. Analog Devices' references use buffered low TC precision zener diodes or patented laser wafer trimmed monolithic bandgap circuitry. Both include output operational amplifiers for optimum load regulation.

The AD2720 precision hybrid reference provides the highest initial accuracy and lowest temperature coefficient. The proprietary temperature compensated design and active laser trimming result in ultra high precision performance previously available only in oven-regulated modules.

AD584 V_{OUT} = 10.000V or 7.500V or 5.000V or 2.500V

The AD584 is a unique bandgap reference. Depending on user requirements it may be connected to provide any one of four standard voltages without additional external parts.

SPECIFICATIONS

(typical @ V_{IN} = +15V and +25°C unless otherwise noted)

Model	Maximum Error in mV for Nominal Output of: 2.5V	5V	7.5V	10V	Temp Stability ppm/°C max	Temp Range[1]
AD584JH	±7.5	±15	±22	±30	30	C
AD584KH	±3.5	±6	±8	±10	15	C
AD584LH	±2.5	±3	±4	±5	5	C
AD584SH(SH/883B)	±7.5	±15	±22	±30	30	M
AD584TH(TH/883B)	±3.5	±6	±8	±10	15	M

NOTE
[1] C = 0 to +70°C, M = -55°C to +125°C

SPECIFICATIONS

(min–max @ E_{IN} = +15V or -15V and +25°C unless otherwise noted)

Model	Output Voltage Volts	Output Voltage Tolerance % Error	Output Current mA	Temp Stability ppm/°C	Time Stability (typ)	Temp Range[1]
AD580JH(KH)(LH)(MH)	2.5	3.0(1.0)(0.4)(0.4)	10	85(40)(25)(10)	25µV/Month 250µV Long Term	C
AD580SH(TH)(UH)	2.5	1.0(0.4)(0.4)	10	55(25)(10)	25µV/Month 250µV Long Term	M
AD580SH/883B[2]	2.5	±1.0	10	55		M
AD580TH/883B[2]	2.5	±0.4	10	25		M
AD580UH/883B[2]	2.5	±0.4	10	10		M
AD581JH(KH)(LH)	10.000	±0.3(0.1)(0.05)	10	30(15)(5)	25ppm per 1000 Hours Noncumulative	C
AD581SH(TH)(UH)	10.000	±0.3(0.1)(0.05)	10	30(15)(5)	25ppm per 1000 Hours Noncumulative	M
AD581SH/883B[2]	10.000	±0.3	10	30		M
AD581TH/883B[2]	10.000	±0.1	10	15		M
AD581UH/883B[2]	10.000	±0.05	10	5		M
AD589JH(KH)(LH)(MH)	1.235	-2.8, +1.2	5	100(50)(25)(10)		C
AD589SH(TH)(UH)	1.235 typ	-2.8, +1.2	5	100(50)(25)		M
AD589SH/883B[2]	1.235 typ	-2.8, +1.2	5	100		M
AD589TH/883B[2]				50		M
AD589UH/883B[2]				25		M

Model	Output Voltage Volts	Output Voltage Tolerance % Error	Output Current mA	Temp Stability ppm/°C	Time Stability (typ)	Temp Range[1]
AD2700J(S)	10.000	±0.05	10	10(3)	100ppm per 1000 Hours @ +55°C	I/M
AD2700L(U)	10.000	±0.025	10	3		I/M
AD2700SD/883B[2]	10.000	±0.05	10	3		M
AD2700UD/883B[2]	10.000	±0.025	10	3		M
AD2701J(S)	-10.000	±0.05	10	10(3)	100ppm per 1000 Hours @ +55°C	I/M
AD2701L(U)	-10.000	±0.025	10	3		I/M
AD2701SD/883B[2]	-10.000	±0.05	10	3		M
AD2701UD/883B[2]	-10.000	±0.025	10	3		M
AD2702J(S)	±10.000	±0.05	10	10(5)	100ppm per 1000 Hours @ +55°C	I/M
AD2702L(U)	±10.000	±0.025	10	5(3)		I/M
AD2702SD/883B[2]	±10.000	±0.05	10	5		M
AD2702UD/883B[2]	±10.000	±0.025	10	3		M
AD2710KN(LN)	+10.000	±0.01	10	2(1)		C
AD2712KN(LN)	±10.000	±0.01	10	2(1)		C
AD2720AH	+10.000	±0.02	5	4	25ppm per 1000 Hours @ +25°C	I
AD2720BH	+10.000	±0.01	5	2		I
AD2720CH	+10.000	±0.01	5	1		I
AD2720SH(SH/883B)[2]	+10.000	±0.02	5	4		M
AD2720TH(TH/883B)[2]	+10.000	±0.01	5	2		M

NOTES
[1] C = 0 to +70°C, I = -25°C to +85°C, M = -55°C to +125°C
[2] Fully processed to MIL-STD-883, Class B

FEATURE SELECTION CHART

		AD589	AD580	AD1403	AD581	AD584	AD2700	AD2710	AD2720
Output Voltage Range	1.235V	•				•			
	2.5V		•	•		•			
	5.0V					•			
	7.5V					•			
	+10.00V				•	•	•	•	•
	-10.00V						•		
	±10.00V						•	•	
Output Voltage Tolerance	≤±0.4%		•	•	•	•	•	•	•
	≤±0.05%				•	•	•	•	•
	≤±0.025%						•	•	•
	≤±0.012%							•	•
Temperature Stability	≤25ppm/°C	•	•	•	•	•	•	•	•
	≤10ppm/°C		•		•	•	•	•	•
	≤5ppm/°C				•	•	•	•	•
	≤1ppm/°C							•	•
Temperature Range	0 to +70°C	•	•	•	•	•	•		•
	-25°C to +85°C						•	•	•
	-55°C to +125°C	•	•		•	•			
Package Style	Hermetic Package	•	•		•	•	•	•	•
	Plastic Package			•					
Dice Available		•	•		•	•			

ANALOG DEVICES

High Speed Sample and Hold Amplifier

AD585

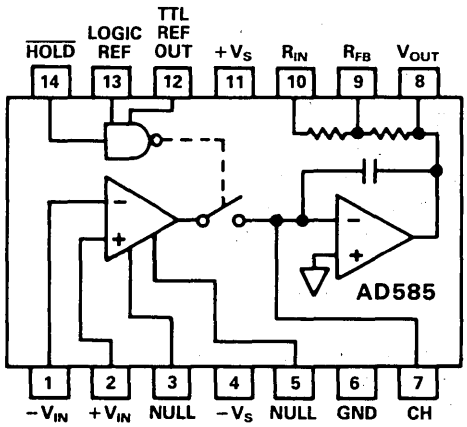
FEATURES

- Fast 2.5μs Acquisition Time to ±0.01%
- Low Droop Rate: 0.5mV/ms
- Low Offset: 1mV
- Sample/Hold Offset Step: 1mV
- Aperture Jitter: 0.5ns
- Military Temperature Range: −55°C to +125°C
- Internal Hold Capacitor

APPLICATIONS

- Data Acquisition Systems
- Data Distribution Systems
- Analog Delay & Storage
- Peak Amplitude Measurements

AD585 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

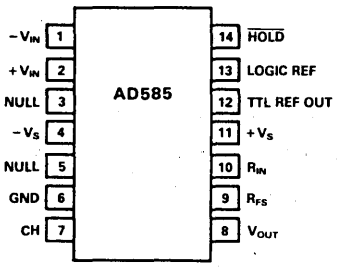
The AD585 is a monolithic sample-and-hold circuit consisting of a high performance operational amplifier in series with an ultra-low leakage analog switch and a FET input integrating amplifier. An internal holding capacitor and connections to the internal feedback resistors, completes the sample and hold.

With the analog switch closed, the AD585 functions like a standard op amp; any feedback network may be connected around the device to control gain and frequency response. With the switch open, the capacitor holds the output at its previous level.

The AD585 offers performance previously unavailable in monolithic sample-and-hold amplifiers. The combination of a fast acquisition time (2.5μs to 0.01%) and low offset step (1mV) are suitable for high speed 12-bit data acquisition systems.

The device is available in two versions: the "J" specified for operation over the 0 to +70°C commercial temperature range and the "S" specified over the full military temperature range −55°C to +125°C.

PIN CONFIGURATION

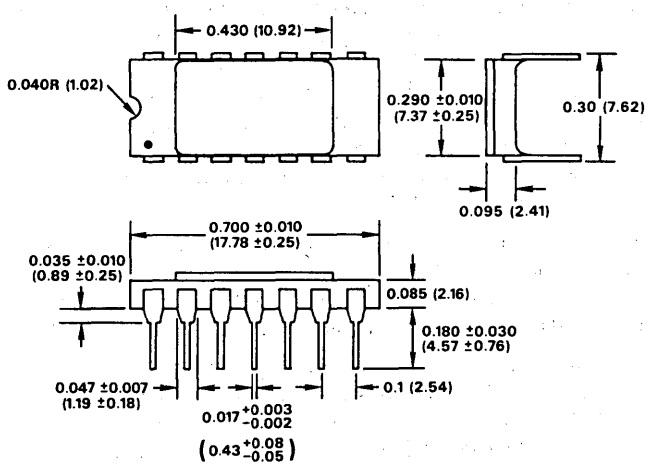


PRODUCT HIGHLIGHTS

1. The droop rate is only 0.5mV/ms so that it may be used in slower high accuracy systems without the loss of accuracy.
2. The fast acquisition time and low aperture make it suitable for very high speed data acquisition systems.
3. The AD585 has internal pretrimmed application resistors for applications versatility.
4. The AD585 is complete with an internal hold capacitor for ease of use and capacitance can be added externally to achieve higher accuracy.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



LINEAR

Analog Devices

ANALOG DEVICES

High Speed Hybrid Track-and-Hold Amplifiers

HTC-0500

FEATURES
700ns Acquisition Time
<750mW Power Dissipation
14-Pin DIP
0.01% Linearity

APPLICATIONS
Data Acquisition Systems
Data Distribution Systems
Analog Delay and Storage
Peak Amplitude Measurements

GENERAL DESCRIPTION

The Analog Devices HTC-0500 Track/Sample Hold is a remarkable combination of speed and low power dissipation in a 14-pin DIP. Its low cost makes it extremely attractive for a wide range of applications which were often uneconomical until now.

Exceptional speed and minimum power in a small, cost-effective package are not the only characteristics which make this unit worth serious consideration for a variety of uses. The innovative design ideas which have been included make it possible for the user to vary the gain of this inverting amplifier.

In many instances, Track/Sample-Hold devices may allow the user to decrease the gain, but increasing the gain is impossible. This is because the majority of these units close the feedback loop internally.

The HTC-0500, however, gives the designer flexibility when it is incorporated into its system application because it can be varied around its normal unity gain. In fact, as shown in Figure 1, the user must close the feedback loop externally with a strap to get proper operation.

Figure 2 shows a suggested method for changing gain over a range which is approximately 8 percent below to approximately 17 percent above nominal. This kind of potential gain variation can be an important element when the HTC-0500 is combined with other components in a system design. The gain of the HTC-0500 can be changed as necessary to compensate for variations in other portions of the system. External adjustments also allow the offset to be nulled.

The HTC-0500 is a perfect choice for use with Analog Devices' converters such as the HAS-1202, AD578, and AD579 in applications which do not require the speed of the model HTC-0300 Track-and-Hold, but require higher speed than the ADSHC-85.

The standard unit is housed in a metal dual in-line package; its model number is HTC-0500AM. A temperature range of −55°C to +125°C is available with model HTC-0500SM. For units processed per MIL-STD-883, Method 5008, specify model number HTC-0500SM/883.

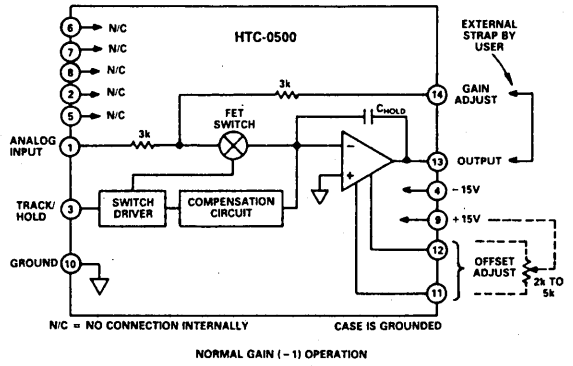


Figure 1.

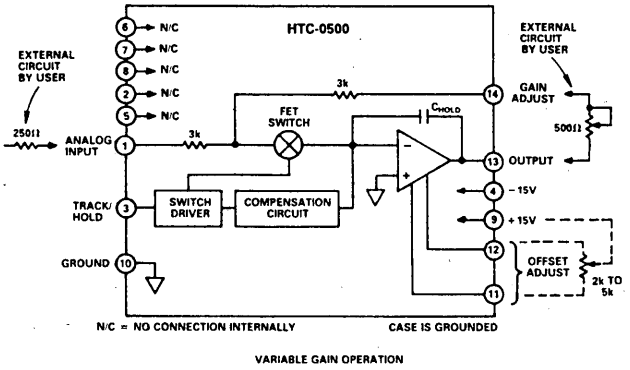
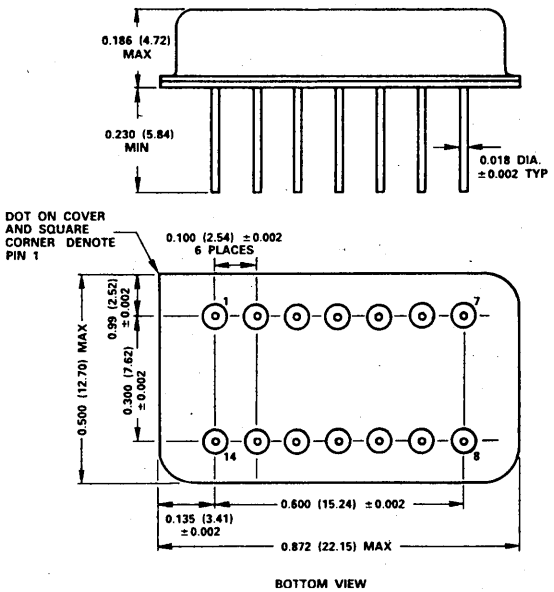


Figure 2.

MECHANICAL DIMENSIONS

Dimensions shown in inches and (mm).



Sample/Track-Hold Amplifiers

IC SAMPLE-HOLD AMPLIFIERS

The AD582, AD583 and AD585 are monolithic sample-and-hold amplifiers with high performance internal amplifiers and a low leakage analog switch. An external hold capacitor is used with the AD582 and AD583, while the AD585 includes an on-chip hold capacitor.

The AD582 is the lowest cost SHA; yet it can replace many modular and hybrid units. For faster acquisition time or greater precision, the AD583 and AD585 are recommended.

Greater speed is provided by the HTC-0500, with an acquisition time of 700ns. The highest speed IC track-and-holds are the HTC-0300, HTC-0300A and HTS-0025. These units have acquisition times, respectively, of 170ns, 150ns and 30ns.

The HTC-0500, HTC-0300 and HTC-0300A are used with fast ADC's such as the HAS Series, the AD578, or AD579. The HTS-0025 is optimized for use with "video" ADC's and is also an excellent choice for use as a deglitcher at the output of high-speed current output DAC's. The ADSHC-85 is a second source for a generic industry-standard device.

SPECIFICATIONS (typical @ +25°C unless otherwise noted)

Model	Open Loop Gain RL=2kΩ k min	Output V_{min}/mA min	Gain Bandwidth MHz	Acquisition Time (0.1%)[1]	Aperture Time ns	Aperture Uncertainty	Droop Rate mV/ms	Oper Temp[2]	Package
AD582K	25[3]	±10/±10	1.5	6μs	150	15ns	100pA[4]	C	14-Pin DIP TO-100
AD582S	25[3]	±10/±10	1.5	6μs	150	15ns	100pA[4]	M	14-Pin DIP TO-100
AD583K	25[3]	±10/±10	2	4μs	50	5ns	50pA[4]	C	14-Pin DIP
AD585J	30[3]	±10/±10	2.5	2.5μs[5]	10	1ns	0.5	C	14-Pin DIP
AD585S	30[3]	±10/±10	2.5	2.5μs[5]	10	1ns	0.5	M	14-Pin DIP
ADSHC-85	+1	±10/±10[6]	0.2	4.5μs[5]	25	0.5ns	0.2	C	14-Pin DIP
ADSHC-85ET	+1	±10/±10[6]	0.2	4.5μs[5]	25	0.5ns	0.2	M	14-Pin DIP
HTS-0025	0.92	±2/±50	30	30ns	10	20ps	200	C	24-Pin DIP
HTS-0025M	0.92	±2/±50	20	30ns	10	20ps	200	MR	24-Pin DIP
HTC-0300	-1	±10/±50	8	170ns	10	100ps	5	C	24-Pin DIP
HTC-0300A	-1	±10/±50	10	150ns	6	100ps	1	C	24-Pin DIP
HTC-0300AM	-1	±10/±50	10	150ns	6	100ps	1	M	24-Pin DIP
HTC-0300M	-1	±10/±50	8	170ns	6	100ps	5	MR	24-Pin DIP
HTC-0500AM	-1	±12/±15	2	700ns	30	60ps	0.5	I	14-Pin DIP
HTC-0500SM	-1	±12/±15	2	700ns	30	60ps	0.5	M	14-Pin DIP

NOTES
[1] A_V=1, R_L=2k, C_L=50pF
[2] C = 0 to +70°C, I = -25°C to +85°C, M = -55°C to +125°C, MR = -55°C to +100°C
[3] Open-loop gain — k min, R_L = 2kΩ
[4] Droop current; rate depends on external capacitance.
[5] Acquisition Time to 0.01%.
[6] Typical outputs

ANALOG DEVICES

16×16-Bit CMOS Multiplier/Accumulator

ADSP-1010

PRELIMINARY TECHNICAL DATA

FEATURES

- 16-by-16 Parallel Multiplication/Accumulation
- 150 Nanosecond Multiply/Accumulate Time
- 250mW Power Dissipation with CMOS Technology
- Improved TDC1010J Second Source
- Double Precision Multiplication/Addition or Subtraction With Three Guard Bits
- Two's Complement or Unsigned Magnitude Input Data Formats
- Round Control
- Available in Hermetically Sealed 64 Pin Flat Pack or 0.7 Square Inch Ceramic DIP
- Operates Off of a Single +5V Power Supply

APPLICATIONS

- Digital Signal Processing
  - Digital Filtering
  - Fourier Transformations
  - Correlations
  - Power Series Expansions
- Matrix Manipulations
- Microprocessor Acceleration

GENERAL INFORMATION

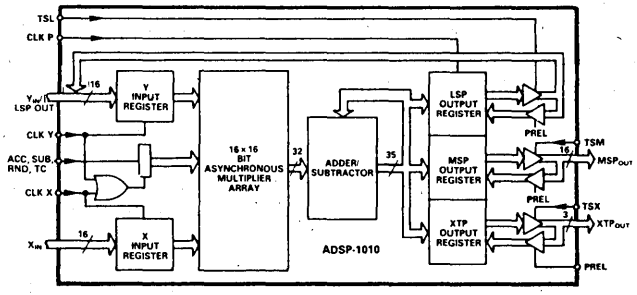
The ADSP-1010 is a TTL compatible high speed low power 16-by-16 multiplier/accumulator that is pin for pin compatible with TRW's TDC1010J. The ADSP-1010 has essentially the same speed as the TDC1010J but consumes only about 1/10 the power.

The low power is obtained by using CMOS technology. The high speed is obtained by the use of three time saving techniques. A modified booth algorithm is used. Feed-forward carry organization is used throughout the array. A conditional sum adder is used in the final adder stage of the multiplier.

The ADSP-1010 has two 16-bit input buses, a 16-bit MSP product bus, a 16-bit LSP product bus, the output port of which is shared with the Y input port, and a 3-bit extended product bus. All inputs are diode protected. The independently controlled input registers are D-type positive edge triggered flip-flops as are the product registers. Each product register has its own three state output control which, when combined with the independent input clocks, allows the ADSP-1010 to operate on a 16-bit microprocessor bus.

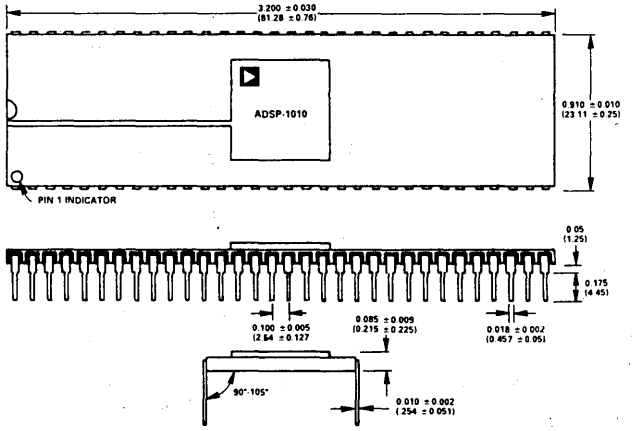
The ADSP-1010 has a RND control which rounds the product to the 16 most significant bits by adding a 1 to the MSB of the 16 LSBs of the multiplier array. The preload control is used in conjunction with the three state control to initialize the contents of the output registers. The ADSP-1010 will perform either a multiplication then addition or multiplication then subtraction or a straight multiplication depending upon the status of the ACC and SUB controls. The TC control provides the capability for either two's complement or unsigned magnitude data formats.

ADSP-1010 FUNCTIONAL BLOCK DIAGRAM



64-PIN HERMETICALLY SEALED DUAL-IN-LINE PACKAGE

Dimensions shown in inches and (mm).



PIN CONFIGURATION

PIN	FUNCTION	PIN	FUNCTION
1	X6	33	P24
2	X5	34	P25
3	X4	35	P26
4	X3	36	P27
5	X2	37	P28
6	X1	38	P29
7	X0	39	P30
8	Y0, P0	40	P31
9	Y1, P1	41	P32
10	Y2, P2	42	P33
11	Y3, P3	43	P34
12	Y4, P4	44	CLK P
13	Y5, P5	45	TSM
14	Y6, P6	46	PREL
15	Y7, P7	47	TSX
16	GND	48	TC
17	Y8, P8	49	V_{CC}
18	Y9, P9	50	CLK Y
19	Y10, P10	51	CLK X
20	Y11, P11	52	ACC
21	Y12, P12	53	SUB
22	Y13, P13	54	RND
23	Y14, P14	55	TSL
24	Y15, P15	56	X15
25	P16	57	X14
26	P17	58	X13
27	P18	59	X12
28	P19	60	X11
29	P20	61	X10
30	P21	62	X9
31	P22	63	X8
32	P23	64	X7

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ANALOG DEVICES

8×8-Bit CMOS Multiplier/Accumulator

ADSP-1008

PRELIMINARY TECHNICAL DATA

FEATURES

- 8×8 Bit Parallel Multiplication/Accumulation
- 150mW Maximum Power Dissipation Through CMOS Technology
- 95 Nanosecond Multiply/Accumulate Time
- Available in 48-Pin DIP or 0.46 Square Inch Flat Pack
- Improved TDC1008J Second Source
- Double Precision Adder With Three Guard Bits
- Round Control
- Accumulator can be Preloaded
- Three State Outputs
- Operates Off of a Single +5V Power Supply

APPLICATIONS

- Extends Capabilities of Microcomputers by Permitting Hardware Multiplication/Accumulation for Increased Computational Speed
- Matrix Manipulations
- Fourier Transformations
- Digital Filtering

GENERAL INFORMATION

The ADSP-1008 is a TTL compatible high speed low power 8-by-8 bit multiplier accumulator that is pin for pin compatible with TRW's TDC1008J. The ADSP-1008 has essentially the same speed as the TDC1008J but consumes only about 1/10 the power.

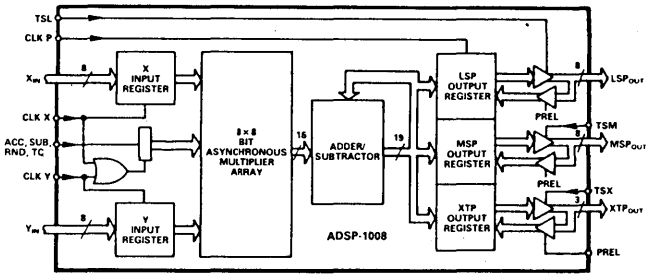
The low power is obtained by using CMOS technology. The high speed is obtained by the use of three time saving techniques. A modified booth algorithm is used. Feed-forward carry organization is used throughout the array. A conditional sum adder is used in the final adder stage of the multiplier.

The ADSP-1008 has two 8-bit input buses, two 8-bit product buses and a 3 bit extra product bus. All inputs are diode protected. The independent input registers are D-type positive edge triggered flip-flops as are the product registers. Each product register has its own three state output control which, when combined with the independent input clocks, allows the ADSP-1008 to operate on an 8-bit microprocessor bus.

The ADSP-1008 has a RND control which rounds the product to the 11 most significant bits by adding a 1 to the MSB of the LSP. The preload control is used in conjunction with the three state control to initialize the contents of the output registers. The ACC and SUB controls are used to determine whether a multiply/add or a multiply/subtract or a straight multiply is performed. The TC control is used to distinguish between two's complement or unsigned magnitude inputs.

The ADSP-1008 is available in either a 48-pin ceramic DIP or a 0.46 square inch flat pack. Each package is available in military or commercial grades.

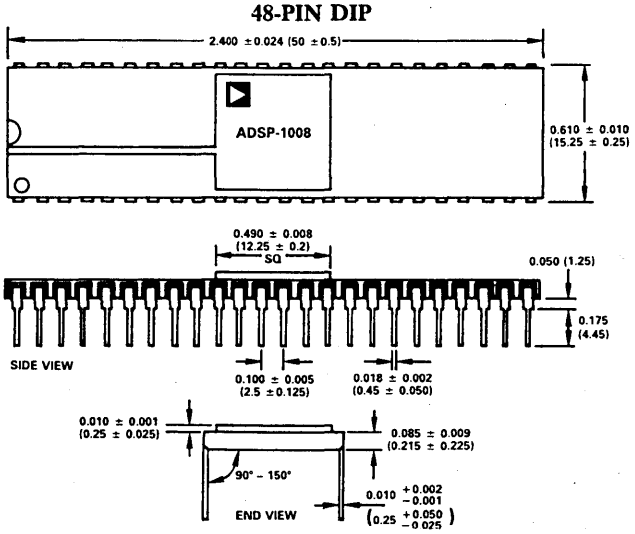
ADSP-1008 FUNCTIONAL BLOCK DIAGRAM



OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

48-PIN DIP



PIN CONFIGURATION

PIN	FUNCTION	PIN	FUNCTION
1	P12	25	X3
2	P11	26	X4
3	P10	27	X5
4	P9	28	X6
5	P8	29	X7
6	TSM	30	CLK X
7	CLK P	31	CLK Y
8	PREL	32	Y0
9	P7	33	Y1
10	P6	34	Y2
11	P5	35	Y3
12	GND	36	Y4
13	P4	37	V_{CC}
14	P3	38	Y5
15	P2	39	Y6
16	P1	40	Y7
17	P0	41	TC
18	TSL	42	TSX
19	SUB	43	P18
20	ACC	44	P17
21	RND	45	P16
22	X0	46	P15
23	X1	47	P14
24	X2	48	P13

ANALOG DEVICES

16×16-Bit CMOS Multiplier

ADSP-1016

PRELIMINARY TECHNICAL DATA

FEATURES

- 16 × 16 Parallel Array Multiplier
- 150mW Power Dissipation with CMOS Technology
- 130 Nanosecond Multiply Time
- Improved MPY-016HJ Second Source
- Two's Complement, Unsigned Magnitude or Mixed Mode Multiplication
- Zero Register Hold Time
- Three State Outputs
- Single +5 Volt Power Supply Operation
- Available in Hermetically Sealed 64-Pin Flat Pack or Ceramic DIP
- Versions Available with Full MIL-STD-883B Processing

APPLICATIONS

- Fourier Transformations
- FIR & IIR Digital Filters
- Microprocessor Accelerators
- Matrix Multiplications

GENERAL DESCRIPTION

The ADSP-1016 is a TTL compatible high speed low power 16 × 16-bit multiplier, that is pin for pin compatible with TRW's MPY-016HJ. The ADSP-1016 has essentially the same speed as the MPY-16HJ but consumes only about 1/10 the power.

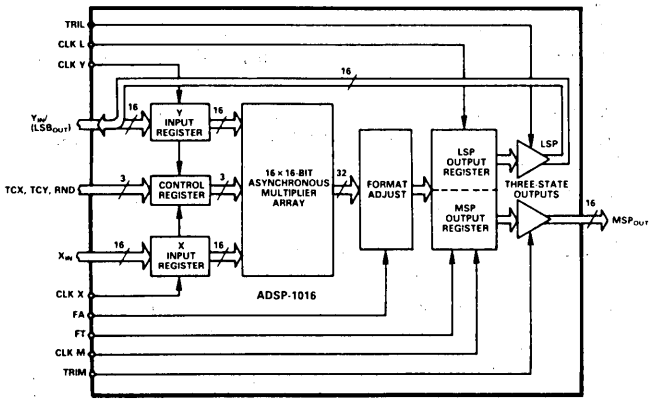
The low power is obtained by using complementary MOS technology. The high speed is achieved by use of three speed saving techniques. A modified booth algorithm is used. Feed-forward carry organization is used throughout the array. A conditional sum adder is used in the final adder stage.

The ADSP-1016 has two 16-bit input buses and two 16-bit product buses. The LSP output port is shared with the Y input port. The inputs can be in either 2's complement unsigned magnitude or mixed mode formats. All inputs are diode protected. The independent input registers are D-type positive edge triggered flip-flops as are the LSP and MSP product registers. The product registers have three-state outputs which, when combined with the independent control of the input registers, allows the ADSP-1016 to operate on a 16-bit microprocessor bus.

The ADSP-1016 has a RND control which rounds the product to the 16 most significant bits by adding a 1 to the MSB of the LSP. The FA control formats the output for 2's complement by shifting the MSP up one bit and then repeating the sign bit in the MSB of the LSP. It should be only used for 2's complement arithmetic. The FT control makes the output latches transparent.

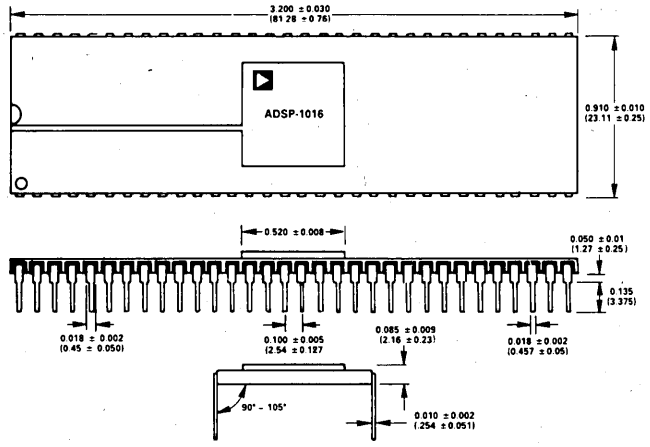
The ADSP-1016 is available in both commercial and MIL temp ranges. Full 883B processing is performed on the MIL grades. Additionally, all versions are available in either a 64-pin hermetically sealed ceramic DIP or a 64-pin hermetically sealed flat pack.

ADSP-1016 FUNCTIONAL BLOCK DIAGRAM



64-PIN HERMETICALLY SEALED DUAL-IN LINE PACKAGE

Dimensions shown in inches and (mm).



PIN CONFIGURATION

PIN	FUNCTION	PIN	FUNCTION
1	X4	33	P24
2	X3	34	P25
3	X2	35	P26
4	X1	36	P27
5	X0	37	P28
6	TRIL	38	P29
7	CLK L	39	P30
8	CLK Y	40	P31
9	P0, Y0	41	CLK M
10	P1, Y1	42	TRIM
11	P2, Y2	43	FA
12	P3, Y3	44	FT
13	P4, Y4	45	GND
14	P5, Y5	46	GND
15	P6, Y6	47	GND
16	P7, Y7	48	$+V_{CC}$
17	P8, Y8	49	$+V_{CC}$
18	P9, Y9	50	TCY
19	P10, Y10	51	TCX
20	P11, Y11	52	RND
21	P12, Y12	53	CLK X
22	P13, Y13	54	X15
23	P14, Y14	55	X14
24	P15, Y15	56	X13
25	P16	57	X12
26	P17	58	X11
27	P18	59	X10
28	P19	60	X9
29	P20	61	X8
30	P21	62	X7
31	P22	63	X6
32	P23	64	X5

LINEAR

Analog Devices

ANALOG DEVICES

8×8-Bit CMOS Multiplier

ADSP-1080

PRELIMINARY TECHNICAL DATA

FEATURES

- 8×8 Bit Parallel Multiplication with Double Precision Product
- 100mW Power Dissipation with CMOS Technology
- 85ns Multiply Time
- Available in 40-Pin DIP or 0.46 Square Inch Flat Pack
- Improved MPY-8HJ Second Source
- Three State Outputs
- Zero Register Hold Time, Positive Setup Time
- Single +5 Volt Power Supply Operation

APPLICATIONS

- High Speed Multiplication for Digital Filters
- Matrix Multiplications
- Fourier Transformations

PRODUCT DESCRIPTION

The ADSP-1080 is a TTL compatible high speed low power 8-by 8-bit multiplier that is pin for pin compatible with TRW's MPY-8HJ. The ADSP-1080 is essentially the same speed as the MPY-8HJ but consumes only about 1/10 the power.

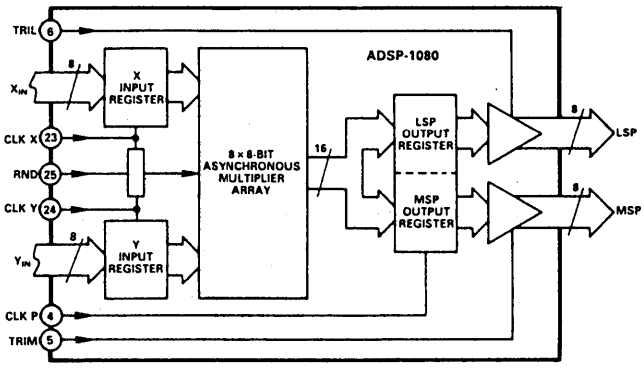
The low power is obtained by using complementary MOS technology. The high speed is achieved by the use of three speed saving techniques. A modified booth algorithm is used. Feed–forward carry organization is used throughout the array. A conditional sum adder is used in the final adder stage.

The ADSP-1080 has two 8-bit input buses and two 8-bit product buses. All inputs are diode protected. The independent input registers are D-type positive edge triggered flip-flops as are the LSP and MSP product registers. The product registers have three state outputs, which when combined with the independent control of the input registers allows the ADSP-1080 to operate on an 8-bit microprocessor bus.

The registered RND control can be used to round the product to the 8 most significant bits by adding a 1 to the MSB of the LSP.

The ADSP-1080 is available in either a 40–pin ceramic DIP or a 0.46 square inch ceramic flat pack. Each package is available in either military or commercial grades.

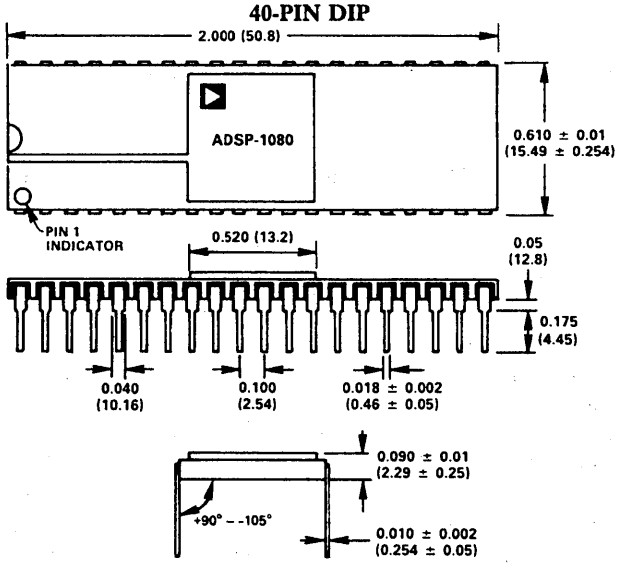
ADSP-1080 FUNCTIONAL BLOCK DIAGRAM



OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

40-PIN DIP



PIN CONFIGURATION

PIN	FUNCTION	PIN	FUNCTION
1	P5	21	X1
2	P6	22	X_{SGN}
3	P7	23	CLKX
4	CLKP	24	CLKY
5	TRIM	25	RND
6	TRIL	26	Y7
7	P_{SGN} (LSP)	27	Y6
8	P8	28	Y5
9	P9	29	Y4
10	P10	30	V_{CC}
11	P11	31	Y3
12	P12	32	GND
13	P13	33	Y2
14	P14	34	Y1
15	X7	35	Y_{SGN}
16	X6	36	P_{SGN} (MSP)
17	X5	37	P1
18	X4	38	P2
19	X3	39	P3
20	X2	40	P4

ANALOG DEVICES

Digital Signal Processing Components

Analog Devices Monolithic Digital Signal-Processing Components are cool, reliable, and compatible in form, function, and pinout with the equivalent industry-standard devices. Employing CMOS for power dissipation as low as 55mW for 8X8-bit and 175mW for 16X16-bit multiplier-accumulators, their speed is compatible with systems having clock rates up to 5MHz and beyond.

Products available include 16X16- and 8X8-bit multipliers and multiplier-accumulators in DIP and Flat Pack configurations for commercial and military temperature ranges at competitive prices.

SPECIFICATIONS (typical @ V_S = +5V, T_A = +25°C unless otherwise noted)

Model	Functional Description	Typical Multiply Time	Maximum Power Dissipation	Package	Temperature
ADSP-1016KD	16X16-Bit Multiplier	130ns	250mW	64-Pin DIP	0 to +70°C
ADSP-1016TD/883B	16X16-Bit Multiplier	130ns	250mW	64-Pin DIP	-55°C to +125°C
ADSP-1016KF	16X16-Bit Multiplier	130ns	250mW	64-Pin Flat Pack	0 to +70°C
ADSP-1016TF/883B	16X16-Bit Multiplier	130ns	250mW	64-Pin Flat Pack	-55°C to +125°C
ADSP-1010KD	16X16-Bit Mult./Accum.	150ns	250mW	64-Pin DIP	0 to +70°C
ADSP-1010TD/883B	16X16-Bit Mult./Accum.	150ns	250mW	64-Pin DIP	-55°C to +125°C
ADSP-1010KF	16X16-Bit Mult./Accum.	150ns	250mW	64-Pin Flat Pack	0 to +70°C
ADSP-1010TF/883B	16X16-Bit Mult./Accum.	150ns	250mW	64-Pin Flat Pack	-55°C to +125°C
ADSP-1080KD	8X8-Bit Multiplier	90ns	150mW	40-Pin DIP	0 to +70°C
ADSP-1080TD/883B	8X8-Bit Multiplier	90ns	150mW	40-Pin DIP	-55°C to +125°C
ADSP-1080KF	8X8-Bit Multiplier	90ns	150mW	40-Pin Flat Pack	0 to +70°C
ADSP-1080TF/883B	8X8-Bit Multiplier	90ns	150mW	40-Pin Flat Pack	-55°C to +125°C
ADSP-1008KD	8X8-Bit Mult./Accum.	95ns	150mW	40-Pin DIP	0 to +70°C
ADSP-1008TD/883B	8X8-Bit Mult./Accum.	95ns	150mW	40-Pin DIP	-55°C to +125°C
ADSP-1008KF	8X8-Bit Mult./Accum.	95ns	150mW	40-Pin Flat Pack	0 to +70°C
ADSP-1008TF/883B	8X8-Bit Mult./Accum.	95ns	150mW	40-Pin Flat Pack	-55°C to +125°C

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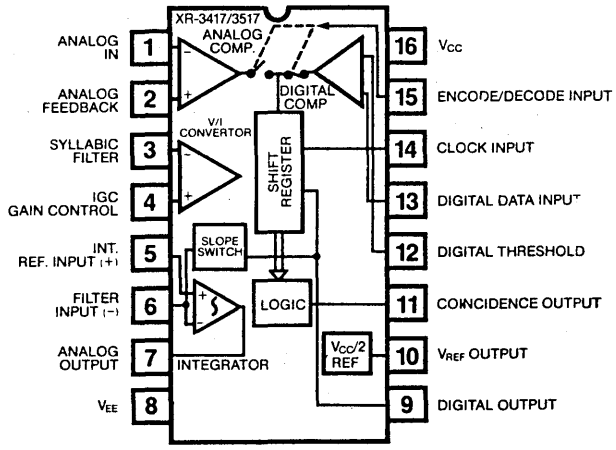
XR-3417/3517 CONTINUOUSLY VARIABLE SLOPE DELTA MODULATOR (CVSD)

The XR3417 is a continuously variable slope delta modulator (CVSD). The circuit's primary function is the digital encoding and analog decoding of voice signals. The circuit consists of a dual comparator, shift register, V/I converter, integrator, and a voltage reference source.

The XR-3417 offers a simplified and economical solution to commercial quality telephone communications, secure military communications, and video game sound production applications.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

ISL (Integrated Schottky Logic) for Increased Gate Speed
TTL/CMOS Compatible
Encode/Decode Selectable
3-Bit Processor Algorithm

APPLICATIONS

Voice Quality CODEC
Video Game Sound Production
Audio Delay Lines

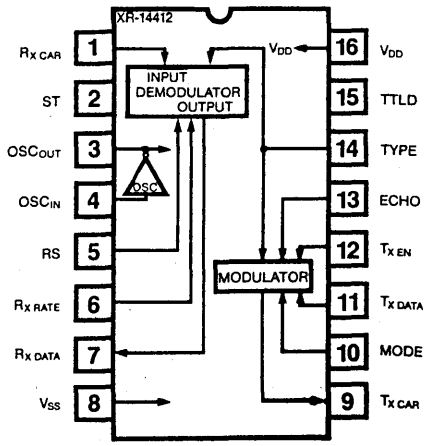
ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-3417CN	Ceramic	0°C to +70°C
XR-3417CP	Plastic	0°C to +70°C
XR-3517M	Ceramic	-55°C to +125°C
XR-3517CN	Ceramic	-55°C to +125°C

XR-14412 FSK MODEM SYSTEM

The XR-14412 contains all the necessary circuitry to construct a complete FSK modulator/demodulator (MODEM) system. Included is circuitry for pin-programmable frequency bands, either U.S. or foreign (CCITT) standards for low-speed MODEMS. The XR-14412 provides T2L-compatible inputs and outputs. Included in the XR-14412 are features for self-testing and an echo suppression tone generator. The XR-14412 utilizes complementary MOS technology for low-power operation.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Simplex, Half-duplex, and Full Duplex Operation
Crystal Controlled
Answer or Originate Modes
Single Supply Operation
Self-test Mode
Selectable Data Rates 200, 300, or 600 bps
T2L- or CMOS-Compatible Inputs and Outputs
Echo Suppressor Disable Tone Generator
U.S. or Foreign (CCITT) Compatible

APPLICATIONS

Stand-Alone MODEMS
Remote Terminals
Acoustical Couplers
Built-in MODEMS

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-14412FN	Ceramic	-40°C to +85°C
XR-14412VN	Ceramic	-40°C to +85°C
XR-14412FP	Plastic	-40°C to +85°C
XR-14412VP	Plastic	-40°C to +85°C

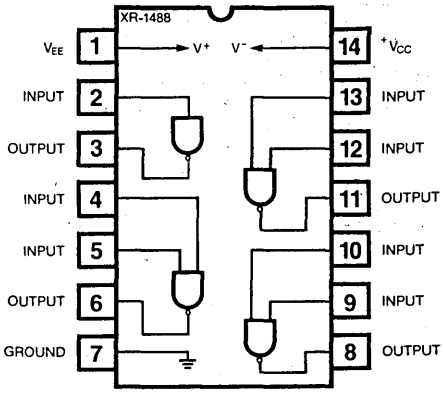
Line Drivers/Receivers

XR-1488 QUAD LINE DRIVER

The XR-1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment, in conformance with the specifications of EIA Standard No. RS232C. This extremely versatile integrated circuit can be used to perform a wide range of applications. The circuit features output current limiting circuitry, and independent positive and negative power supply driving elements. Compatibility with all DTL and TTL logic families enhances the versatility of the circuit.

The XR-1488 quad line driver along with its companion circuit, the XR-1489A quad line receiver, provides a complete interface system between DTL and TTL logic levels, and the RS232C defined voltage and impedance levels.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Current Limited Output
Independent Positive Power Supply Driving Elements
Independent Negative Power Supply Driving Elements
Compatible with DTL and TTL Logic Families
Data Terminal/Data Communication Interface
Conforms to EIA Standard No. RS232C

APPLICATIONS

RS232 C Interface

ORDERING INFORMATION

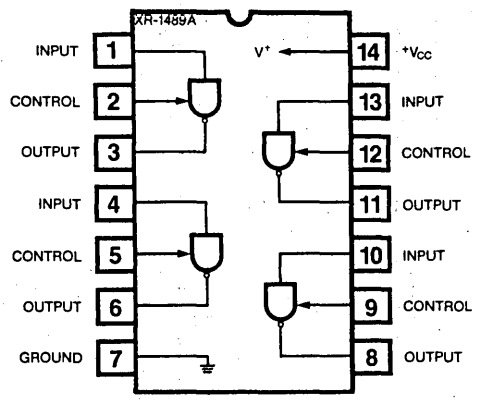
Part Number	Package	Operating Temperature
XR-1488N	Ceramic	0°C to +70°C
XR-1488P	Plastic	0°C to +70°C

XR-1489A QUAD LINE RECEIVER

The XR-1489A is a monolithic quad line receiver especially designed for data bus interface. Each of the line receiver sections has adjustable hysteresis characteristics for improved noise rejection. The input and output levels of the circuit are designed to provide direct interface between RS232C data bus standards and the DTL or TTL type logic levels.

The XR-1489A quad line receiver along with its companion circuit, the XR-1488 quad line driver, provides a complete interface between DTL and TTL logic levels, and the RS232C defined voltage and impedance levels.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Direct Replacement for MC1489A
Current Limited Output
Compatible with DTL and TTL Logic
Meets EIA Standard RS232C

APPLICATIONS

Data Bus Interface
Microprocessor Interface
Remote Terminal Interface
RS232 Interface

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-1489AN	Ceramic	0°C to +70°C
XR-1489AP	Plastic	0°C to +70°C

EXAR

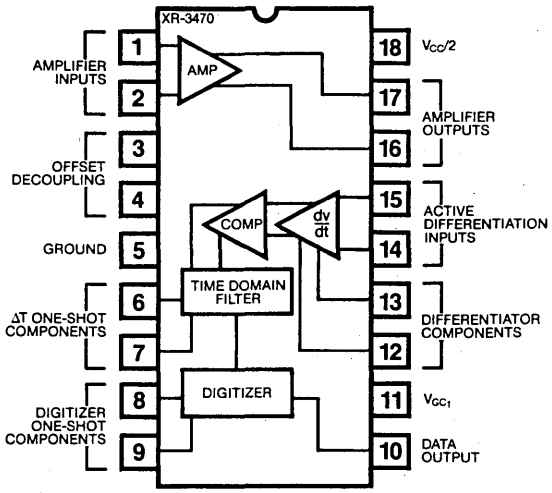
Disc Drives

XR-3470 FLOPPY DISC READ AMPLIFIER

The XR-3470 is a read amplifier system designed primarily for use in a floppy disc system. The circuit is designed to accept the readback signal from a magnetic head and convert the peaks of this signal to digital pulses. The circuit consists of a high-frequency amplifier, an active differentiator, a zero-crossing detector, and a time domain filter.

The XR-3470 can be used to transfer data up to 3 megabaud. This device can also detect voltage levels as low as 1.4 mV pp, which gives it the flexibility to be used for single- or double-density floppy disc systems. The chip contains all the circuitry essential for a floppy disc read amplifier system.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Less Than 5% Peak Shift
Low Input Voltage Detection
Complete Floppy Disc Read System
Increased Preamp Gain 110 V/V, Typical
Up to 3 MBaud Operation

APPLICATIONS

Single/Double Density Floppy Disc Read Amplifier
Magnetic Tape Read Amplifier

ORDERING INFORMATION

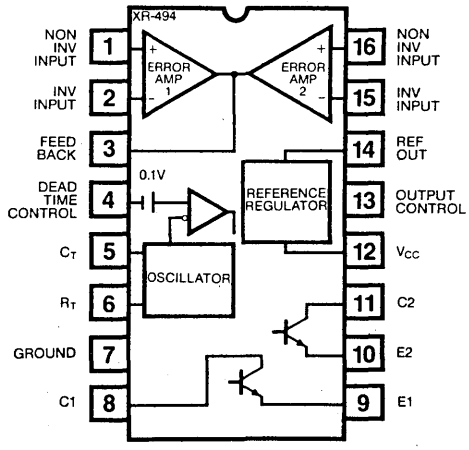
Part Number	Package	Operating Temperature
XR-3470CN	Ceramic	0°C to +70°C
XR-3470CP	Plastic	0°C to +70°C

Switching Regulators

XR-494 PULSE-WIDTH MODULATING REGULATOR

All functions required to construct a pulse-width modulating regulator are incorporated on a single monolithic chip in the XR-494. The device is primarily designed for power supply control and contains an on-chip 5-volt regulator, two error amplifiers, an adjustable oscillator, a dead-time control comparator, a pulse-steering flip-flop, and output control circuits. Either common emitter or emitter follower output capability is provided by the uncommitted output transistors.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Complete PWM Power Control Circuitry
Uncommitted Outputs for 200 mA Sink or Source
Output Control Selects Single-ended or Push-pull Operation
Internal Circuitry Prohibits Double Pulse at Either Output
Variable Dead-time Provides Control Over Total Range
Internal Regulator Provides a Stable 5V Reference Supply
Circuit Architecture Provides Easy Snychronization

APPLICATIONS

Pulse-Width Modulated Power Control Systems
Switching Regulators
Motor Speed Control
Power Inverters

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-494M	Ceramic	-55°C to +125°C
XR-494CN	Ceramic	0°C to +70°C
XR-494CP	Plastic	0°C to +70°C

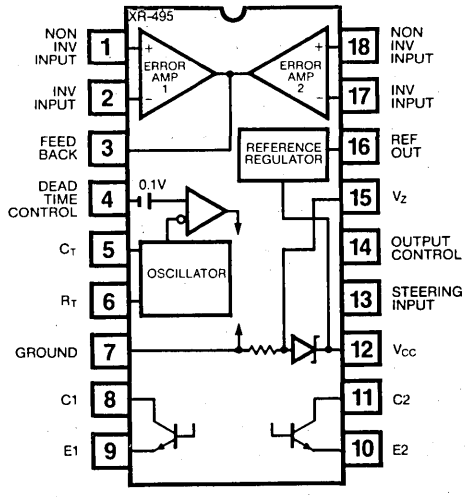
Switching Regulators

XR-495 PULSE-WIDTH MODULATING REGULATOR

All functions required to construct a pulse-width modulating regulator are incorporated on a single monolithic chip. The device is primarily designed for power supply control and contains an on-chip 5-volt regulator, two error amplifiers, an adjustable oscillator, a dead-time control comparator, a pulse-steering flip-flop, and output control circuits. Either common emitter or emitter follower output capability is provided by the uncommitted output transistors.

The XR-495 also contains an on-chip 39-volt Zener diode for high-voltage applications, where V_{CC} is greater than 40 volts, and an output steering control that overrides the internal control of the pulse-steering flip-flop.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Complete PWM Power Control Circuitry
Uncommitted Outputs for 200 mA Sink or Source
Output Control Selects Single-ended
or Push-pull Operation
Internal Circuitry Prohibits Double-Pulse at Either Output
Variable Dead-time Provides Control Over Total Range

APPLICATIONS

Pulse-Width Modulated Power Control Systems
Switching Regulators

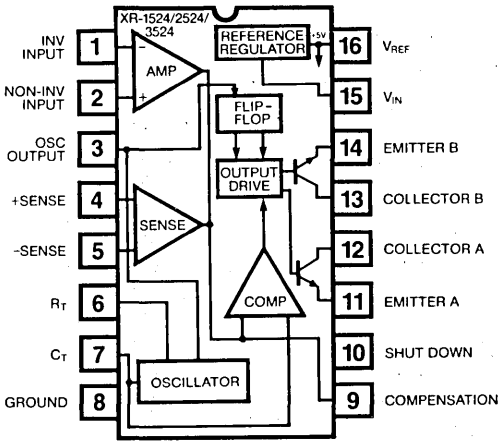
ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-495M	Ceramic	-55°C to +125°C
XR-495CN	Ceramic	0°C to +70°C
XR-495CP	Plastic	0°C to +70°C

XR-1524/2524/3524 PULSE-WIDTH MODULATING REGULATOR

This monolithic integrated circuit contains all the control circuitry for a regulating power supply inverter or switching regulator. Included in the 16-Pin dual-in-line package is the voltage reference, error amplifiers, oscillator, pulse-width modulator, pulse-steering flip-flop, dual alternating output switches, current-limiting, and shut-down circuitry. This device can be used for switching regulators of either polarity, transformer coupled dc-to-dc converters, transformerless voltage doublers, and polarity converters. The XR-1524 is specified for operation over the full military temperature range of -55°C to +125°C, while the XR-2524 and XR-3524 are designed for commercial applications of 0°C to +70°C.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Direct Replacement for SG1524/2524/3524
Complete PWM Power Control Circuitry
Single-ended or Push-pull Outputs
Line and Load Regulation of 0.2%
1% Maximum Temperature Variation
Total Supply Current Less Than 10 mA
Operation Beyond 100 kHz

APPLICATIONS

Switching Power Supply
Motor Speed Control

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-1524M	Ceramic	-55°C to +125°C
XR-2524N	Ceramic	0°C to +70°C
XR-2524P	Plastic	0°C to +70°C
XR-3524N	Ceramic	0°C to +70°C
XR-3524P	Plastic	0°C to +70°C

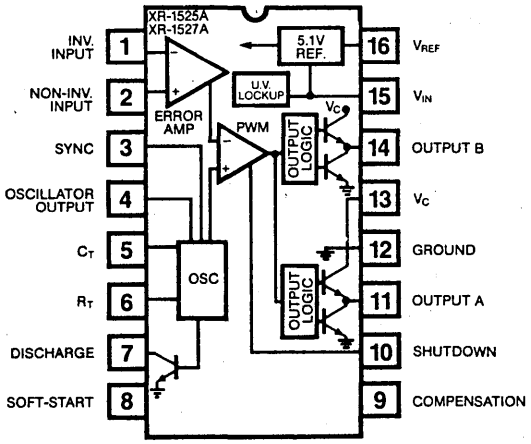
Switching Regulators

XR-1525A/2525A/3525A XR-1527A/2527A/3527A PULSE-WIDTH MODULATING REGULATORS

The XR-1525A/1527A are a series of monolithic integrated circuits that contain all of the control circuitry necessary for a pulse-width modulating regulator. Included are the voltage reference, error amplifier, oscillator, pulse-width modulator, under-voltage lockout, soft-start circuitry, and output drivers.

The on-chip + 5.1-volt reference is trimmed to ± 1% initial accuracy. Dead-time is adjustable with a single external resistor. The XR-1525A series gives a LOW output for an OFF state, while the XR-1527A series gives a HIGH output for an OFF state.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

8- to 35-Volt Operation
Adjustable Dead-Time Control
Internal Soft-Start
Latching PWM to Prevent Double Pulsing
Dual Source/Sink Output Driver Capable of +200 mA

APPLICATIONS

Pulse-Width Modulation
Switching Regulators
Power Control Systems
Industrial Controls

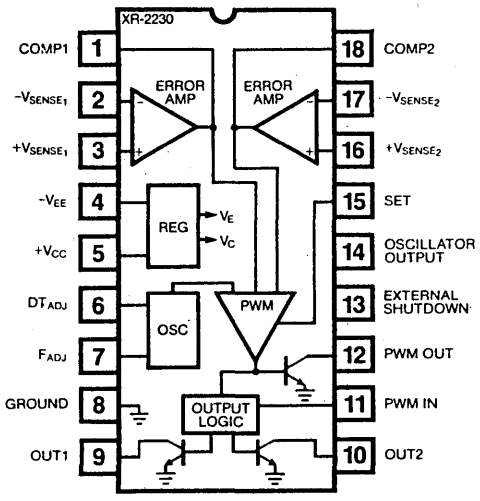
ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-1525/27AN	Ceramic	-55°C to +125°C
XR-2525/27AN	Ceramic	-25°C to +85°C
XR-2525/27AC	Plastic	-25°C to +85°C
XR-3525/27AN	Ceramic	0°C to +70°C
XR-3525/27AC	Plastic	0°C to +70°C

XR-2230 PULSE-WIDTH MODULATOR CONTROL SYSTEM

The XR-2230 is a high-performance monolithic pulse-width modulator control system. It contains all the necessary control blocks for designing switch mode power supplies, and other power control systems. Included in the 18-Pin dual-in-line package are two error amplifiers, a sawtooth generator, and the necessary control logic to drive two open-collector power transistors. Also included are protective features, such as adjustable dead-time control, thermal shutdown, soft-start control, and double-pulse protection circuitry.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Thermal Shutdown
Adjustable Dead-time
Dual Open-Collector 30 mA Output Transistors
Double-Pulse Protection Circuit
Soft-Start Control
High-Speed Remote Shut-Down Input
Two High-Performance Error Amplifiers with ± 5V Input Common-Mode Range

APPLICATIONS

Switching Regulators
Motor-Speed Controllers
Pulse-Width Modulated Control Systems

ORDERING INFORMATION

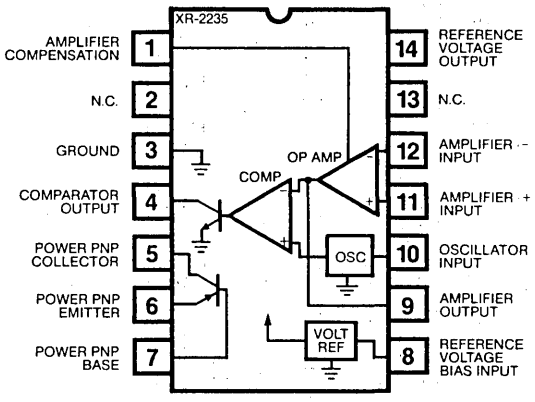
Part Number	Package	Operating Temperature
XR-2230CP	Plastic	0°C to +70°C

Switching Regulators

XR-2235 HIGH-VOLTAGE PULSE-WIDTH MODULATING REGULATOR

The XR-2235 is a monolithic integrated circuit that contains all of the control circuitry for a high-voltage switching regulator. Included in the 14-Pin dual-in-line package is the voltage reference, error amplifier, oscillator, pulse-width modulator, and high-voltage npn and pnp transistors. The XR-2235 is capable of regulating voltages as high as 60 volts down to 5 volts. This device can be used for step-up, step-down, and inverter switching regulator designs. The design of the XR-2235 allows positive or negative input voltages.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Complete Pulse-Width Modulating Control Circuitry
Operation Beyond 100 kHz
Line and Load Regulation of 0.3%
Total Standby Current of 6 mA
Continuous Load Current of 50 mA, Maximum
Input Voltages of 10V to 60V
Single-ended Output

APPLICATIONS

High-Voltage Switching Regulators
Pulse-Width Modulating Power Control Systems
Telephone System Switching Regulators
Power Inversion Circuits

ORDERING INFORMATION

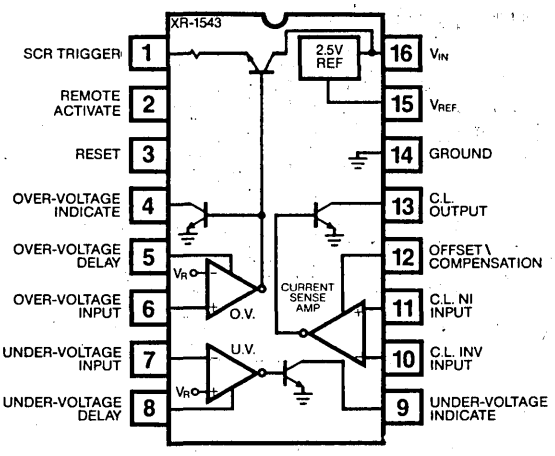
Part Number	Package	Operating Temperature
XR-2235CN	Ceramic	0°C to +70°C
XR-2235CP	Plastic	0°C to +70°C

XR-1543/2543/3543 POWER SUPPLY OUTPUT SUPERVISORY CIRCUIT

The XR-1543/2543/3543 are monolithic integrated circuits that contain all the functions necessary to monitor and control the output of a power supply system. Included in the 16-Pin dual-in-line package are a voltage reference, an operational amplifier, voltage comparators, and a high-current SCR trigger circuit. The functions performed by this device include over-voltage and under-voltage sensing, and current limiting with provisions for triggering an external crowbar.

The internal voltage reference on the XR-1543 is trimmed for an accuracy of ± 1% to eliminate the need for external potentiometers. The entire circuit may be powered from either the output that is being monitored or from a separate bias voltage.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Over-voltage Sensing Capability
Under-voltage Sensing Capability
Current Limited Output
Reference Voltage Trimmed to ± 1% Accuracy
SCR Crowbar Drive to 300 mA
Programmable Time Delays
Open Collector Outputs
Remote Activation Capability
Total Standby Current Less than 10 mA

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-1543N	Ceramic	-55°C to +125°C
XR-2543N	Ceramic	-25°C to +85°C
XR-3543N	Ceramic	0°C to +70°C

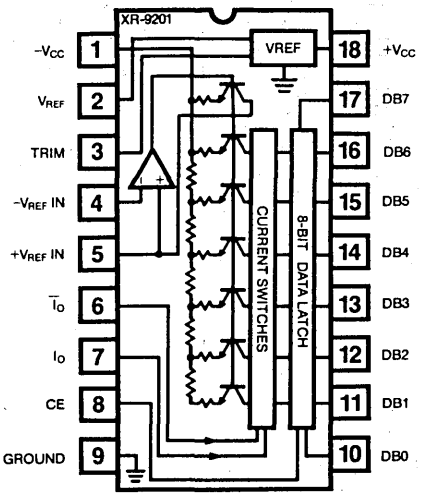
Converters

XR-9201 8-BIT MICROPROCESSOR COMPATIBLE D/A CONVERTER

The XR-9201 is a monolithic 8-bit μP compatible, digital-to-analog converter with differential current outputs. It contains an internal data latch, making it suitable for interfacing with microprocessors. The chip contains a stable voltage reference (2.0V nominal) which is externally adjustable, and can be used as a reference for other D/A and A/D converters.

The XR-9201 features nonlinearity of ± 1/2 LSB maximum (± .19% of full scale current). The internal voltage reference maintains a temperature coefficient of 50 ppm/°C.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

8-Bit Resolution	
Input Data Latches	
Internal Voltage Reference	
Microprocessor Compatible	
Nonlinearity	± 1/2 LSB, Maximum
Reference Voltage Stability	± 50 ppm/°C
TTL Compatible	

APPLICATIONS

A/D Conversion	Programmable Current Source
Test Equipment	Programmable Voltage Source
Bipolar and Unipolar D/A Conversion	Measuring Instruments

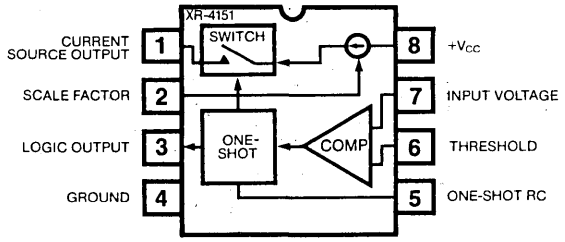
ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-9201CP	Plastic	0°C to +70°C

XR-4151 VOLTAGE-TO-FREQUENCY CONVERTER

The XR-4151 is a device designed to provide a simple, low cost, method for converting a dc voltage into a proportional pulse repetition frequency. It is also capable of converting an input frequency into a proportional output voltage. The XR-4151 is useful in a wide range of applications, including A/D and D/A conversion and data transmission.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Single Supply Operation	+ 8V to + 22V
Pulse Output Compatible with all Logic Forms	
Programmable Scale Factor	
Linearity (Precision Mode)	± 0.05%, Typical
Temperature Stability	± 100 ppm/°C, Typical
High-Noise Rejection	
Inherent Monotonicity	
Easily Transmittable Output	
Simple Full Scale Trim	
Single-ended Input	
Frequency-to-Voltage Conversion	
Direct Replacement for RC/RV/RM4151	

APPLICATIONS

Voltage-to-Frequency Conversion
A/D and D/A Conversion
Data Transmission
Frequency-to-Voltage Conversion
Transducer Interface
System Isolation

ORDERING INFORMATION

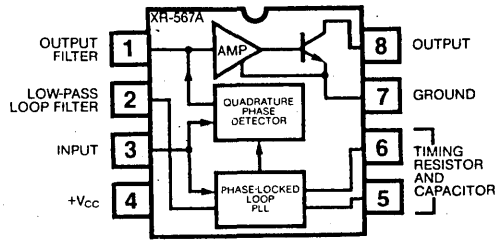
Part Number	Package	Operating Temperature
XR-4151P	Plastic	-40°C to +85°C
XR-4151CP	Plastic	0°C to +70°C

PLL's and Tone Decoders

XR-567A MONOLITHIC TONE DECODER

The XR-567A is a monolithic phase-locked loop system designed for general purpose tone and frequency decoding. It offers a wide frequency band of 0.01 Hz to 500 kHz, and has a logic compatible output capable of sinking up to 100 mA of load current. Four independent external components determine the bandwidth, center frequency, and output delay.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Direct Replacement for SE/NE567	
Adjustable Bandwidth	0% to 14%
Logic Compatible Output with Current Sinking Capability	100 mA
Adjustable Center Frequency	0.01 Hz to 500 kHz
Inherent Immunity to False Signals	
High Rejection of Out-of-Band Signals and Noise	
Adjustable Range Frequency by External Resistor	over 20:1 range

APPLICATIONS

Touch-Tone® Decoding
Sequential Tone Decoding
Communications Paging
Ultrasonic Remote Control and Monitoring
Carrier-Tone Transceiver
Wireless Intercom
Precision Oscillator

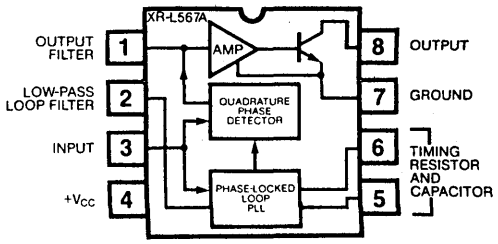
ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-567AM	Ceramic	-55°C to +125°C
XR-567ACN	Ceramic	0°C to +70°C
XR-567ACP	Plastic	0°C to +70°C

XR-L567A MONOLITHIC TONE DECODER

The XR-L567A is a micropower phase-locked loop (PLL) circuit designed for general purpose tone and frequency decoding. It is a direct replacement for the popular 567-type tone decoder IC's, designed for applications requiring very low power dissipation. The XR-L567A offers approximately 1/10th the power dissipation of the conventional 567-type tone decoder, without sacrificing its key features, such as oscillator stability, frequency selectivity and detection threshold. At 5-volt operation, typical quiescent power dissipation is less than 4 mW.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Very Low Power Dissipation	< 4 mW at 5V
Adjustable Bandwidth	0% to 14%
Logic Compatible Output with 10 mA Current Sinking Capability	
Highly Stable Center Frequency	
Adjustable Center Frequency	0.01 Hz to 50 kHz
Inherent Immunity to False Signals	
High Rejection of Out-of-Band Signals and Noise	
Adjustable Frequency Range by External Resistor	over 20:1 range

APPLICATIONS

Battery Operated Tone Detection
Touch-Tone® Decoding
Communications Paging
Ultrasonic Remote Control
Telemetry Decoding

ORDERING INFORMATION

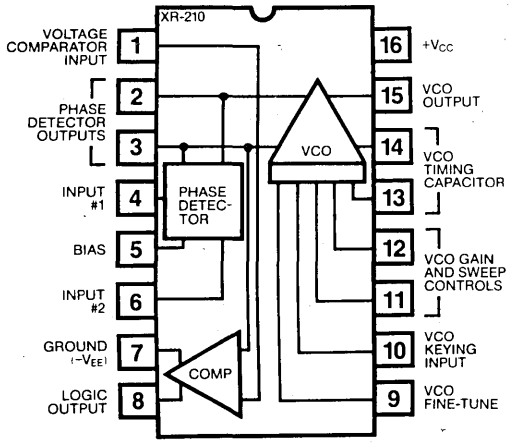
Part Number	Package	Operating Temperature
XR-L567ACN	Ceramic	0°C to +70°C
XR-L567ACP	Plastic	0°C to +70°C

PLL's and Tone Decoders

XR-210 FSK MODULATOR/ DEMODULATOR

The XR-210 is a highly versatile monolithic phase-locked loop system especially designed for data communications. It is particularly well suited for FSK modulation/demodulation (MODEM) applications, frequency synthesis, tracking filters and tone decoding. The XR-210 operates over a power supply range of 5V to 26V, and over a frequency band of 0.5 Hz to 20 MHz. The circuit can accomodate analog signals between 300 μV and 3V, and can interface with conventional DTL, TTL, and ECL logic families.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Digital Programming Capability	
RS-232C Compatible Demodulator Output	
ON-OFF Keying & Sweep Capability	
Wide Tracking Range	± 1% to ± 50%
Good Temperature Stability	200 ppm/°C
High Current Logic Output	50 mA
Independent "Mark" and "Space" Frequency Adjustment	
VCO Duty Cycle Control	

APPLICATIONS

Data Synchronization	Signal Conditioning
FSK Generation	Tone Decoding
Frequency Synthesis	FSK Demodulation
Tracking Filter	FM Detection
FM and Sweep Generation	Wideband Discrimination

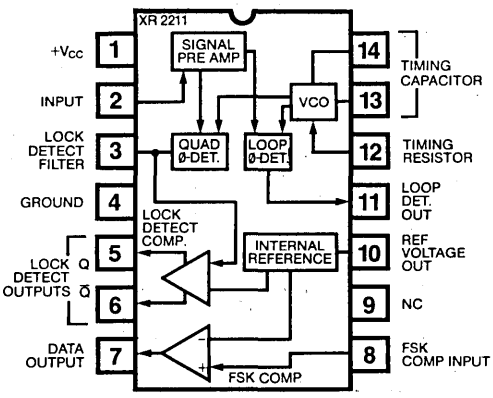
ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-210M	Ceramic	-55°C to +125°C
XR-210CN	Ceramic	0°C to +70°C

XR-2211 FSK DEMODULATOR/ TONE DECODER

The XR-2211 is a monolithic phase-locked loop system especially designed for data communications, and particularly well-suited for FSK modem applications. It has a supply voltage range of 4.5V to 20V and a wide frequency range of 0.01 Hz to 300 kHz. The circuit accomodates analog signals between 2 mV and 3V, and interfaces with conventional DTL, TTL, and ECL logic families. The XR-2211 consists of a basic PLL for tracking an input signal within the passband, a quadrature phase detector for carrier detection, and an FSK voltage comparator for FSK demodulation. Independent external components set the center frequency, bandwidth, and output delay.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Wide Frequency Range	0.01 Hz to 300 kHz
Wide Supply Voltage Range	4.5V to 20V
DTL/TTL/ECL Logic Compatibility	
Wide Dynamic Range	2 mV to 3V rms
Adjustable Tracking Range	± 1% to ± 80%
Excellent Temperature Stability	20 ppm/°C, Typical
FSK Demodulation with Carrier-Detection	

APPLICATIONS

FSK Demodulation	FM Detection
Data Synchronization	Carrier Detection
Tone Decoding	

ORDERING INFORMATION

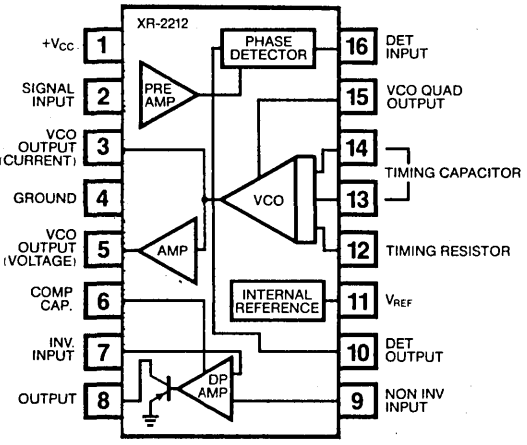
Part Number	Package	Operating Temperature
XR-2211M	Ceramic	-55°C to +125°C
XR-2211N	Ceramic	-40°C to +85°C
XR-2211P	Plastic	-40°C to +85°C
XR-2211CN	Ceramic	0°C to +70°C
XR-2211CP	Plastic	0°C to +70°C

PLL's and Tone Decoders

XR-2212 PRECISION PHASE-LOCKED LOOP

The XR-2212 is an ultra-stable monolithic phase-locked loop (PLL) system especially designed for data communication and control system applications. It is ideally suited for frequency synthesis, FM detection, and tracking filter applications. The circuit consists of a PLL system made up of an input preamplifier, a phase detector, a stable voltage-controlled oscillator (VCO), and a high-gain differential amplifier. The center frequency, bandwidth, and tracking range of the PLL are controlled independently by the choice of external components.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Quadrature VCO Outputs	
Wide Frequency Range	0.01 Hz to 300 kHz
Wide Supply Voltage Range	4.5V to 20V
Adjustable Tracking Range	± 1% to ± 80%
Excellent Temperature Stability	20 ppm/°C, Typical

APPLICATIONS

Frequency Synthesis	FSK Demodulation
Data Synchronization	Tracking Filters
FM Detection	Clock Extraction
Signal Conditioning	

ORDERING INFORMATION

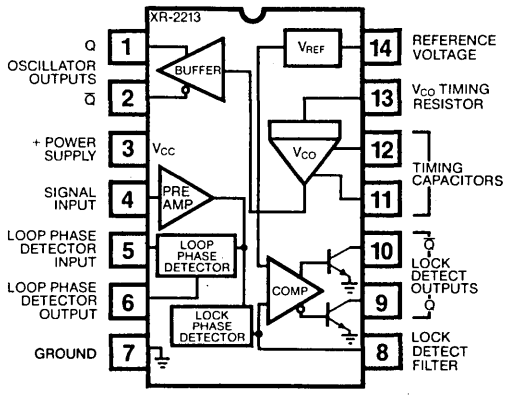
Part Number	Package	Operating Temperature
XR-2212M	Ceramic	-55°C to +125°C
XR-2212N	Ceramic	-40°C to +85°C
XR-2212P	Plastic	-40°C to +85°C
XR-2212CN	Ceramic	0°C to +70°C
XR-2212CP	Plastic	0°C to +70°C

XR-2213 PRECISION PHASE-LOCKED LOOP/TONE DECODER

The XR-2213 is a high-stability phase-locked loop system designed for control systems and tone detection applications. The circuit features a high-stability V_{CO}, an input preamplifier and a high-gain voltage comparator, in addition to loop and quadrature-phase detectors.

The XR-2213 has an operating frequency range of 0.01 Hz to 300 kHz. The input preamplifier allows an input signal range of 2 mV to 3 volts rms, while the V_{CO} and comparator supply TTL-compatible output signals. The V_{CO} and voltage comparator provide both Q and $\overline{Q}$ outputs for greater flexibility and reduced external parts count. All of the loop parameters are independently adjustable by the choice of external components.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Wide Frequency Range	0.01 Hz to 300 kHz
Wide Supply Voltage Range	4.5V to 15V
Uncommitted V_{CO} Q and $\overline{Q}$ Outputs	
Wide Dynamic Input Voltage Range	2 mV to 3V rms
Excellent V_{CO} Stability	20 ppm/°C, Typical

APPLICATIONS

Tone Detection	FM Detection
Frequency Synthesis	Tracking Filters

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2213M	Ceramic	-55°C to +125°C
XR-2213N	Ceramic	-40°C to +85°C
XR-2213P	Plastic	-40°C to +85°C
XR-2213CN	Ceramic	0°C to +70°C
XR-2213CP	Plastic	0°C to +70°C

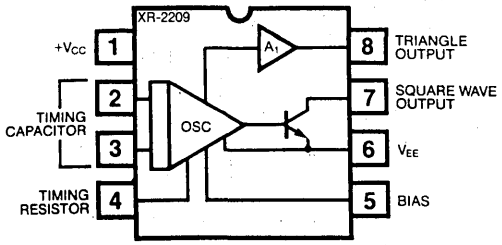
Function Generators

XR-2209 PRECISION OSCILLATOR

The XR-2209 is a monolithic variable frequency oscillator circuit featuring excellent temperature stability and a wide linear sweep range. The circuit provides simultaneous triangle and square wave outputs over a frequency range of 0.01 Hz to 1 MHz. The frequency is set by an external RC product. The device is ideally suited for frequency modulation, voltage-to-frequency or current-to-frequency conversion, sweep or tone generation, as well as for phase-locked loop applications when used in conjunction with a phase comparator such as the XR-2208.

The circuit is comprised of three functional blocks: A variable frequency oscillator and two buffer amplifiers. The XR-2209 has a typical drift specification of 20 ppm/°C. The frequency can be linearly swept over a 1000:1 range, by an external control signal.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Excellent Temperature Stability	20 ppm/°C
Linear Frequency Sweep	
Wide Sweep Range	1000:1, Minimum
Wide Supply Voltage Range	± 4V to ± 13V
Low Supply Sensitivity	0.15%/V
Wide Frequency Range	0.01 Hz to 1 MHz
Simultaneous Triangle and Square Wave Outputs	

APPLICATIONS

V/F Conversion	Waveform Generation
C/F Conversion	Stable Phase-Locked Loop
FM and Sweep Generation	

ORDERING INFORMATION

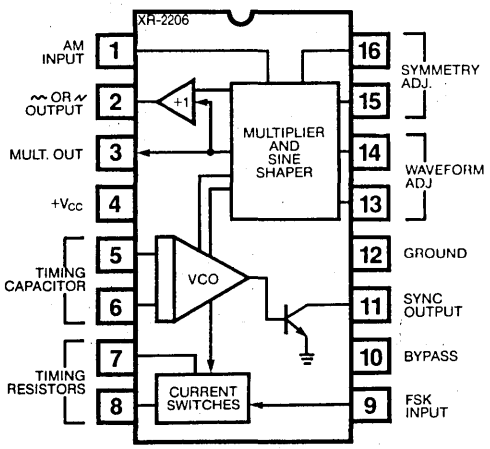
Part Number	Package	Operating Temperature
XR-2209M	Ceramic	-55°C to +125°C
XR-2209CN	Ceramic	0°C to +70°C
XR-2209CP	Plastic	0°C to +70°C

XR-2206 MONOLITHIC FUNCTION GENERATOR

The XR-2206 is a monolithic function generator integrated circuit capable of producing high quality sine, square, triangle, ramp, and pulse waveforms of high stability and accuracy. The output waveforms can be both amplitude and frequency modulated by an external voltage. Frequency of operation can be selected externally over a range of 0.01 Hz to more than 1 MHz.

The circuit is ideally suited for communications, instrumentation, and function generator applications requiring sinusoidal tone, AM, FM, or FSK generation.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Low Sinewave distortion	.5%, Typical
Excellent Stability	20 ppm/°C, Typical
Wide Sweep Range	2000:1, Typical
Linear Amplitude Modulation	
Adjustable Duty Cycle	1% to 99%

APPLICATIONS

Waveform Generation	V/F Conversion
Sweep Generation	FSK Generation
AM/FM Generation	Phase-Locked Loops

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2206M	Ceramic	-55°C to +125°C
XR-2206N	Ceramic	0°C to +70°C
XR-2206P	Plastic	0°C to +70°C
XR-2206CN	Ceramic	0°C to +70°C
XR-2206CP	Plastic	0°C to +70°C

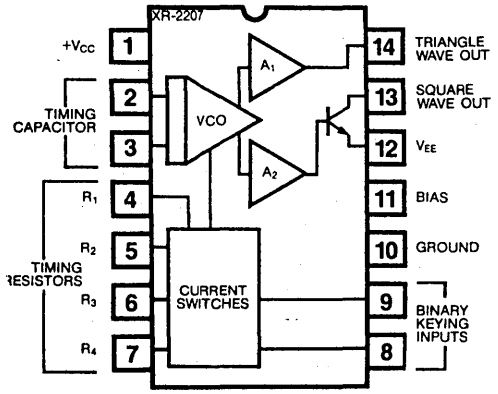
Function Generators

XR-2207 VOLTAGE-CONTROLLED OSCILLATOR

The XR-2207 is a monolithic voltage-controlled oscillator (VCO) integrated circuit featuring excellent frequency stability and a wide tuning range. The circuit provides simultaneous triangle and square wave outputs over a frequency range of 0.01 Hz to 1 MHz. It is ideally suited for FM, FSK, sweep or tone generation, and phase-locked loop applications.

The XR-2207 has a typical drift specification of 20 ppm/°C. The oscillator frequency can be linearly swept over a 1000:1 range with an external control voltage.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Excellent Temperature Stability	20 ppm/°C
Linear Frequency Sweep	
Adjustable Duty Cycle	0.1% to 99.9%
Two or Four Level FSK Capability	
Wide Sweep Range	1000:1, Minimum
Wide Supply Voltage Range	± 4V to ± 13V
Low Power Sensitivity	0.15%/V
Wide Frequency Range	0.01 Hz to 1 MHz
Simultaneous Triangle and Square Wave Outputs	

APPLICATIONS

FSK Generation	FM and Sweep Generation
V/F Conversion	Waveform Generation
C/F Conversion	Stable Phase-Locked Loop

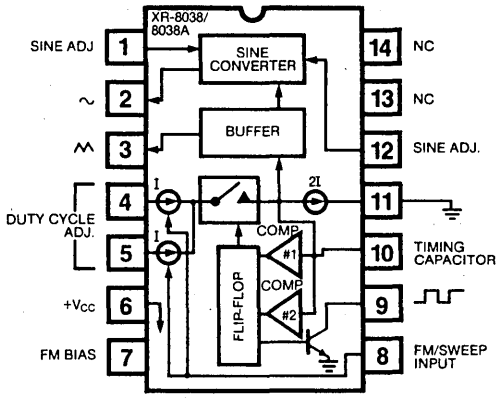
ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2207M	Ceramic	-55°C to +125°C
XR-2207N	Ceramic	0°C to +70°C
XR-2207P	Plastic	0°C to +70°C
XR-2207CN	Ceramic	0°C to +70°C
XR-2207CP	Plastic	0°C to +70°C

XR-8038/8038A PRECISION WAVEFORM GENERATOR

The XR-8038/8038A is a precision waveform generator IC capable of producing sine, square, triangular, sawtooth, and pulse waveforms with a minimum of external components and adjustments. Its operating frequency can be selected over nine decades of frequency, from 0.001 Hz to 1 MHz, by the choice of external RC components. The frequency of oscillation is highly stable over a wide temperature and supply voltage range. The frequency modulation and sweeping can be accomplished with an external control voltage, without affecting the quality of the output waveforms, The frequency can be programmed digitally through the use of either resistors or capacitors.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Direct Replacement for Intersil 8038	
Low Frequency Drift	50 ppm/°C
Simultaneous Sine, Triangle and Square Wave Outputs	
Low Distortion	THD 1%
High FM and Triangle Linearity	
Wide Frequency Range	0.001 Hz to 1 MHz
Minimum External Component Count	
Variable Duty Cycle	2% to 98%

APPLICATIONS

Precision Waveform Generation	Sweep Generation
Test Instrumentation Design	Precision PLL Design
Phase-Locked Clock Generation	Tone Generation

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-8038M	Ceramic	-55°C to +125°C
XR-8038N	Ceramic	0°C to +70°C
XR-8038P	Plastic	0°C to +70°C
XR-8038CN	Ceramic	0°C to +70°C
XR-8038CP	Plastic	0°C to +70°C

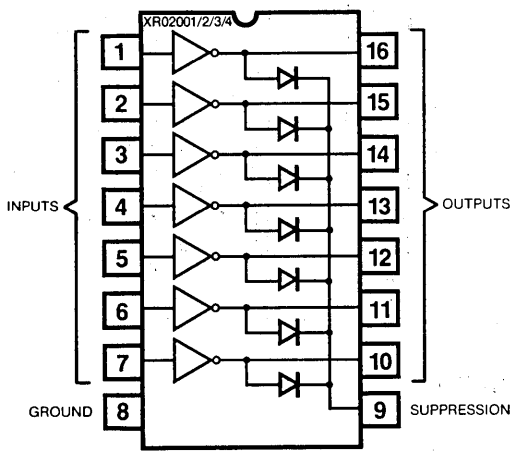
EXAR Integrated Systems, Inc., 750 Palomar Ave., Sunnyvale, CA 94086 * (408) 732-7970

Darlington Arrays

XR-2001/2002/2003/2004
HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

The XR-2001/2002/2003/2004 are high-voltage, high-current Darlington transistor arrays consisting of seven silicon npn Darlington pairs on a common monolithic substrate. All units feature open-collector outputs and integral protection diodes for driving inductive loads. Peak inrush currents of up to 600 mA are allowed, which makes the arrays ideal for driving tungsten filament lamps. The outputs may be paralleled to achieve higher load current capability, although each driver has a maximum continuous collector current rating of 500 mA. The arrays are price competitive with discrete transistor alternatives.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Peak Inrush Current Capability of 600 mA
Internal Protection Diodes for Driving Inductive Loads
Excellent Noise Immunity
Direct Compatibility with Most Logic Families
Opposing Pin Configuration Eases Circuit Board Layout

APPLICATIONS

Relay Drive
High Current Logic Driver

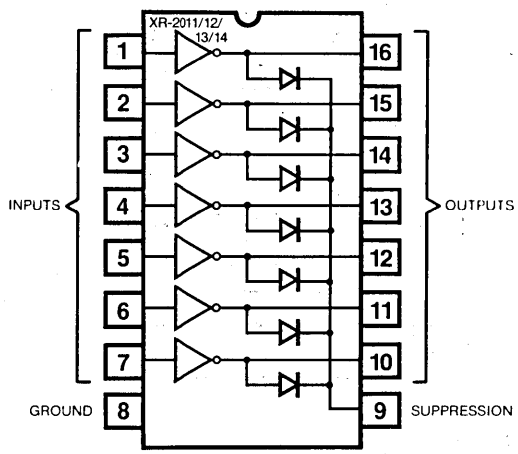
ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2001CN	Ceramic	0°C to +70°C
XR-2002CN	Ceramic	0°C to +70°C
XR-2003CN	Ceramic	0°C to +70°C
XR-2004CN	Ceramic	0°C to +70°C

XR-2011/2012/2013/2014
HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

The XR-2011/2012/2013/2014 are high-voltage, high-current Darlington transistor arrays consisting of seven silicon npn Darlington pairs on a common monolithic substrate. All units feature open collector outputs and integral protection diodes for driving inductive loads. Peak inrush currents of up to 750 mA are allowed, which makes the arrays ideal for driving tungsten filament lamps. The outputs may be paralleled to achieve higher load current capability, although each driver has a maximum continuous collector current rating of 600 mA. The arrays are price competitive with discrete transistor alternatives.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Peak Inrush Current Capability of 750 mA
Internal Protection Diodes for Driving Inductive Loads
Excellent Noise Immunity
Direct Compatibility with Most Logic Families
Opposing Pin Configuration Eases Circuit Board Layout

APPLICATIONS

Relay Drive
High Current Logic Driver

ORDERING INFORMATION

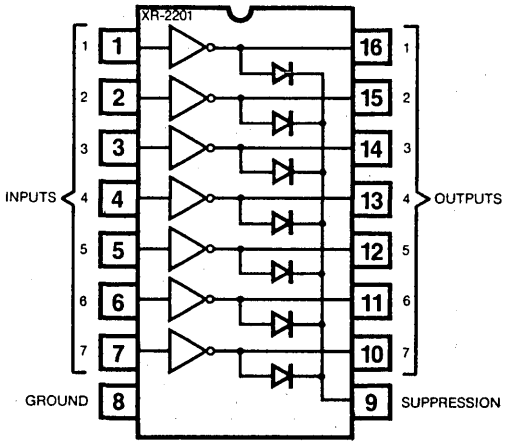
Part Number	Package	Operating Temperature
XR-2011CN	Ceramic	0°C to +70°C
XR-2012CN	Ceramic	0°C to +70°C
XR-2013CN	Ceramic	0°C to +70°C
XR-2014CN	Ceramic	0°C to +70°C

Darlington Arrays

XR-2201/2202/2203/2204 HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

The XR-2201/2202/2203/2204 are Darlington transistor arrays comprised of seven silicon npn Darlington pairs on a single monolithic substrate. All feature open-collector outputs and internal protection diodes for driving inductive loads. Peak inrush currents of up to 600 mA are allowable, making them ideal for driving tungsten filament lamps. Although the maximum continuous collector current rating is 500 mA for each driver, the outputs may be paralleled to achieve higher load current capability.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

High Peak Current Capability	600 mA
Internal Protection Diodes for Driving Inductive Loads	
Directly Compatible with: TTL, CMOS, PMOS, and DTL Logic Families	
Direct Replacement for Sprague: ULN2001A/2002A/2003A/2004A	

APPLICATIONS

Solenoid and Relay Driver	High-Current Switch
High-Current LED Driver	Tungsten Lamp Driver
Printing Calculator Hammer Driver	

ORDERING INFORMATION

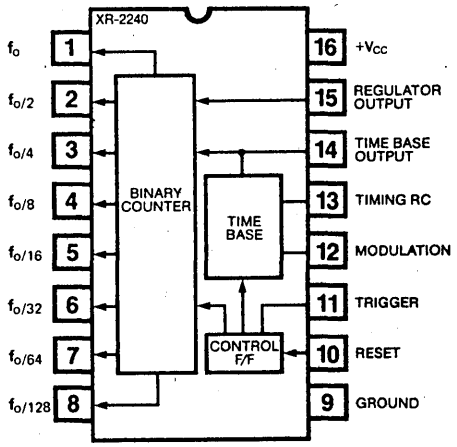
Part Number	Package	Operating Temperature
XR-2201CP	Plastic	0°C to +85°C
XR-2202CP	Plastic	0°C to +85°C
XR-2203CP	Plastic	0°C to +85°C
XR-2204CP	Plastic	0°C to +85°C

Timers

XR-2240 PROGRAMMABLE TIMER/COUNTER

The XR-2240 Programmable Timer/Counter is a monolithic controller capable of producing ultralong time delays (from microseconds to days), without sacrificing accuracy. The circuit is comprised of an internal time-base oscillator, a programmable 8-bit counter, and a control flip-flop. The time delay is set by an external RC network and can be programmed to any value from 1 RC to 225 RC.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Timing from Microseconds to Days	
Programmable Delays	1 RC to 225 RC
Wide Supply Range	4V to 15V
TTL and DTL Compatible Outputs	
High Accuracy	0.5%
External Sync and Modulation Capability	
Excellent Supply Rejection	0.2%/V

APPLICATIONS

Precision Timing	Frequency Synthesis
Long Delay Generation	Pulse Counting/Summing
Sequential Timing	A/D Conversion
Binary Pattern Generation	Digital Sample and Hold

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2240M	Ceramic	-55°C to +125°C
XR-2240N	Ceramic	0°C to +70°C
XR-2240P	Plastic	0°C to +70°C
XR-2240CN	Ceramic	0°C to +70°C
XR-2240CP	Plastic	0°C to +70°C

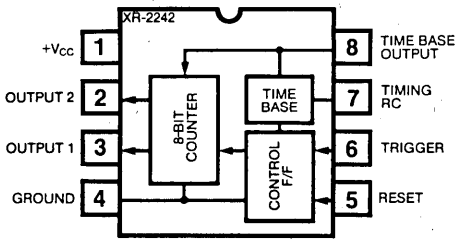
Timers

XR-2242 LONG-RANGE TIMER

The XR-2242 is a monolithic Timer/Controller capable of producing ultralong time delays from microseconds to days. Two timing circuits can be cascaded to generate time delays or timing intervals of up to one year. The circuit is comprised of an internal time-base oscillator, an 8-bit binary counter, and a control flip-flop. For a given external RC network connected to the timing terminal, the circuit produces an output timing pulse of 128 RC. If two circuits are cascaded, a total time delay of $(128)^2$ or 16,384 RC is obtained.

In monostable timer applications, the output terminal (Pin 3) is connected back to the reset terminal, and the circuit continues to operate in an astable mode, subsequent to a trigger input.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Timing from Microseconds to Days	
Wide Supply Range	4.5V to 15V
TTL and DTL Compatible Outputs	
High Accuracy	0.5%
Excellent Supply Rejection	0.2%/V
Monostable and Astable Operation	

APPLICATIONS

Long Delay Generation
Sequential Timing
Ultralow Frequency Oscillator
Precision Timing
Interval Timing

ORDERING INFORMATION

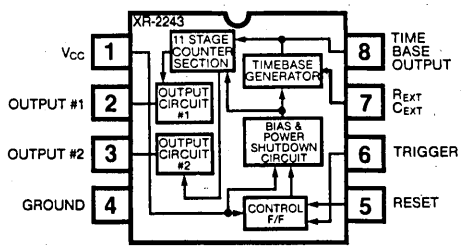
Part Number	Package	Operating Temperature
XR-2242M	Ceramic	-55°C to +125°C
XR-2242CN	Ceramic	0°C to +70°C
XR-2242CP	Plastic	0°C to +70°C

XR-2243 MICROPOWER LONG-RANGE TIMER

The XR-2243 is a monolithic Timer/Controller capable of producing ultralong time delays, from microseconds to days. Two timing circuits can be cascaded to generate time delays or timing intervals of up to one year. The circuit is comprised of an internal time-base oscillator, an 11-bit binary counter, and a control flip-flop. For a given external RC network connected to the timing terminal, the circuit produces an output timing pulse of 1024 RC. If the two circuits are cascaded, a total time delay of $(1024)^2$ or 1,048,576 RC is obtained.

The XR-2243 long-range timer was designed for low power operation. Its supply current requires less than 100 μA in standby or reset mode. Normal operation requires less than 1 mA.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

High-Output Current Sink Capability	
Timing from Microseconds to Days	
Wide Supply Range	2.2V to 15V
TTL and DTL Compatible Outputs	
High Accuracy	0.5%
Excellent Supply Rejection	
Monostable and Astable Operation	
Micropower Consumption/Standby Operation	
Low-power Consumption/Normal Operation	

APPLICATIONS

Long Delay Generation	Sequential Timing
Battery Powered Applications	Precision Timing
Ultralow Frequency Oscillator	

ORDERING INFORMATION

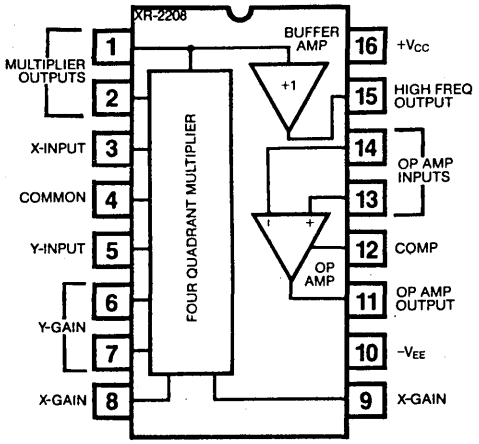
Part Number	Package	Operating Temperature
XR-2243CN	Ceramic	0°C to +70°C
XR-2243CP	Plastic	0°C to +70°C

Multipliers

XR-2208 OPERATIONAL MULTIPLIER

The XR-2208 operational multiplier combines a four-quadrant analog multiplier (or modulator), a high frequency buffer amplifier, and an operational amplifier in a monolithic circuit that is ideally suited for both analog computation and communications signal processing applications. The multiplier/buffer amplifier combination extends the small signal 3 dB bandwidth to 8 MHz, and the transconductance bandwidth to 100 MHz.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Internally Separated Multiplier, Op Amp, and Buffer	
Excellent Linearity	0.3%, Typical
Wide Bandwidth:	
3 dB Bandwidth	8 MHz, Typical
3° Phase Shift Bandwidth	1.2 MHz, Typical
Simplified Offset Adjustments	
Wide Supply Voltage Range	± 4.5V to ± 16V

APPLICATIONS

Analog Computation (Multiplication/Division)
Triangle-to-Sine Wave Converter
AGC Amplifier
Phase Detector

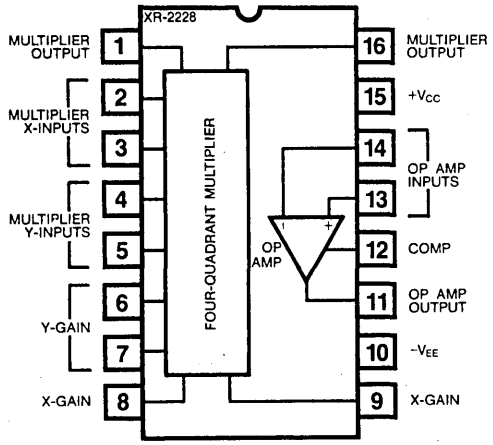
ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2208M	Ceramic	-55°C to +125°C
XR-2208N	Ceramic	0°C to +70°C
XR-2208P	Plastic	0°C to +70°C
XR-2208CN	Ceramic	0°C to +70°C
XR-2208CP	Plastic	0°C to +70°C

XR-2228 MULTIPLIER/DETECTOR

The XR-2228 multiplier/detector circuit is designed as a basic building block for analog signal processing, and communication systems. It contains a four-quadrant analog multiplier/modulator, and a high-gain op amp on the same chip. Because of its wide common-mode range and differential inputs, the XR-2228 can interface with any of the existing PLL circuits in designing synchronous AM detection or frequency translation systems. It can be used as a phase detector for frequencies up to 100 MHz.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Internally Separated Multiplier and Op Amp	
Differential X and Y Inputs	
Interfaces with all PLL and VCO Circuits	
Wide Common-Mode Range	
Wide Transconductance Bandwidth	100 MHz, Typical

APPLICATIONS

Phase-Locked Loop Design
Phase Detection
Synchronous AM Detection
AM Generation
Triangle-to-Sine Wave Conversion
Frequency Translation

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2228M	Ceramic	-55°C to +125°C
XR-2228N	Ceramic	-40°C to +85°C
XR-2228P	Plastic	-40°C to +85°C
XR-2228CN	Ceramic	-40°C to +85°C
XR-2228CP	Plastic	0°C to +70°C

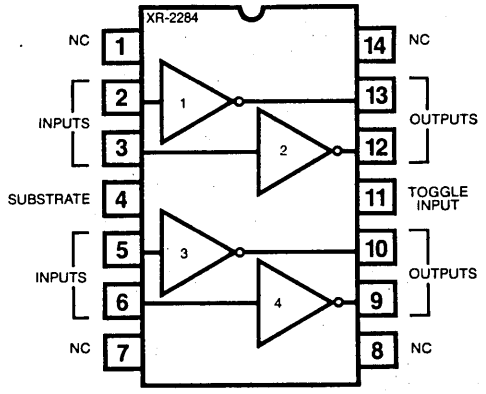
Display Drivers

XR-2284 HIGH-VOLTAGE PLASMA DISPLAY DRIVER

The XR-2284 is a four-channel display driver circuit especially designed for interfacing with high-voltage ac plasma display systems. Each driver array can be used for either the segment or the column (or digit) drive, and several driver arrays can be "stacked" together to drive a large number of display segments or columns.

All four channels of the driver IC are driven by a common ac toggle voltage. Each output can sink or source up to 100 mA of load current and can operate with toggle frequencies of up to 200 kHz. The input threshold levels of each of the driver channels is compatible with TTL or CMOS logic levels. The XR-2284 is designed to operate with 360-volt ac plasma systems, and has a minimum standoff voltage of 90 volts. The commercial version, XR-2284C, is designed for 240-volt plasma systems and has a maximum voltage rating of 60 volts.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

High Standoff Voltage	> 90V (2284) > 60V (2284C)
Very Low ac Standby Power at 100 kHz	< 25 MW/Channel
Zero dc Standby Power	
100 mA Output Drive Capability	

APPLICATIONS

High-Voltage Pulsed Displays & ac Plasma Panels
Pulsed ac Switching

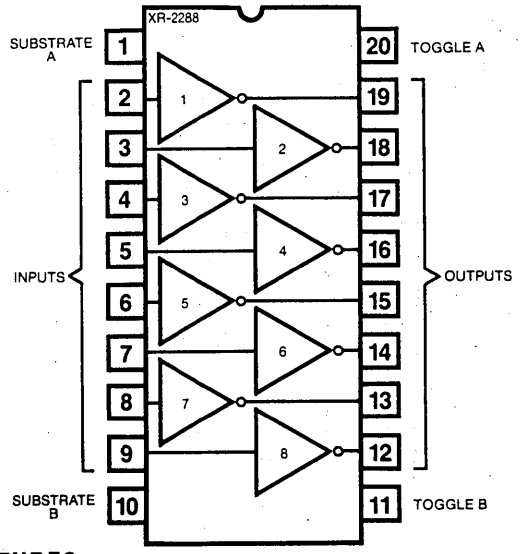
ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2284P	Plastic	0°C to +70°C
XR-2284CP	Plastic	0°C to +70°C

XR-2288 HIGH-VOLTAGE AC PLASMA DISPLAY DRIVER

The XR-2288 is an eight-channel high-voltage display driver circuit especially designed for ac plasma displays. It contains the equivalent of two XR-2284 type driver circuits in a single IC package. Each driver channel can sink or source up to 100 mA of capacitive load current and can operate with toggle frequencies up to 200 kHz. The XR-2288 is designed to operate with 360-volt ac plasma systems, and a minimum standoff voltage of 90 volts. The commercial version, XR-2288C, is designed for 240-volt ac plasma systems, and has a maximum voltage rating of 60 volts.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

High Standoff Voltage	90 volts, Typical
Eight Independent Driver Channels	
Very Low ac Standby Power at 100 kHz	< 25 mW/Channel
Zero dc Standby Power	
100 mA Output Drive Capability	
TTL and CMOS Compatible Inputs	

APPLICATIONS

High-Voltage ac Plasma Panels
High-Voltage Pulsed Displays
Pulsed ac Switching

ORDERING INFORMATION

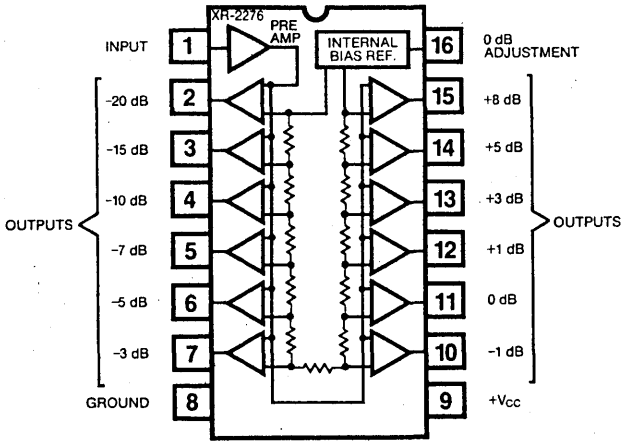
Part Number	Package	Operating Temperature
XR-2288P	Plastic	0°C to +70°C
XR-2288CP	Plastic	0°C to +70°C

Display Drivers

XR-2276 BAR-GRAPH DISPLAY GENERATOR

The XR-2276 is a 12-point level detector circuit particularly designed for interfacing with fluorescent displays. The circuit is comprised of an input buffer amplifier, 12 high-gain comparators, an internal voltage reference, and a bias-setting resistor string. All of the 12 comparator stages have independent buffered outputs. Each of the comparators has a threshold level higher than the preceding comparator. With no input signal, all of the comparators are OFF, and all the outputs are at a LOW state. As the input level is increased, the outputs successively switch to their HIGH state, at 12 discrete input levels. These threshold levels are set to be within the range of -20 dB to +8 dB; with reference to a zero dB level setting.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Direct Fluorescent or LED Display Drive Capability
High Input Impedance
Internal Pulldown Resistors
Logarithmic Display Characteristics
External Reference Level Adjustment

APPLICATIONS

Bar-Graph & Sequential Display Generator
12-Point Display Driver & Digital Controller
Audio Level Indicator
Channel Separation Indicator

ORDERING INFORMATION

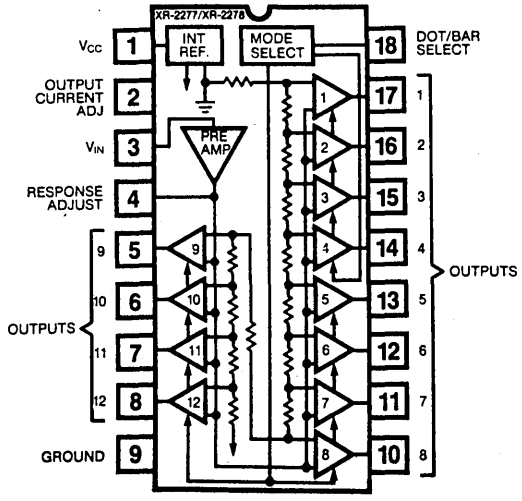
Part Number	Package	Operating Temperature
XR-2276CP	Plastic	0°C to +70°C

XR-2277/XR-2278 DOT OR BAR-GRAPH DISPLAY GENERATORS

The XR-2277 and XR-2278 are 12-point level detector circuits designed for interfacing directly with LED moving dot or bar-graph displays. Each circuit is comprised of an input buffer amplifier, a set of 12 comparators which are biased from an internal voltage reference, and a resistor string. Each comparator provides a high-impedance current source output; each of the output currents is very closely matched and can be adjusted, simultaneously, with a single external setting resistor.

The XR-2277 has 12 discrete output levels, over a range of -30 dB to +6 dB, referenced to an externally set zero dB reference level. The XR-2278 has similar electrical characteristics, except for a dynamic range of -20 dB to +8 dB.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Direct LED Interface
Constant-Current Outputs
External Mode-Select for Dot/Bar-Graph Format
Adjustable Zero dB Reference
Adjustable Output Currents
High Input Impedance

APPLICATIONS

Bar-Graph Display Generator and Driver
Dot Display Generator

ORDERING INFORMATION

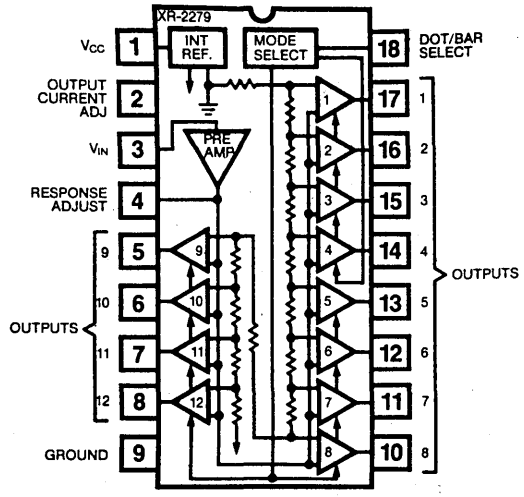
Part Number	Package	Operating Temperature
XR-2277CP	Plastic	0°C to +70°C
XR-2278CP	Plastic	0°C to +70°C

Display Drivers

XR-2279 DOT AND BAR-GRAPH DISPLAY GENERATOR

The XR-2279 is a 12-point logarithmic level-detector circuit comprised of an input buffer amplifier and a set of 12 voltage comparators. The circuit produces 12 discrete output levels, spaced in three dB intervals, over a dynamic range of -27 dB to +6 dB, referenced to an externally adjusted zero dB level. It is designed for interfacing directly with LED moving dot or bar-graph displays. Each of the comparator outputs provides a high-impedance constant-current drive which is well-matched and can be adjusted by an external resistor setting. The circuit output is either a moving dot or a continuous bar-graph format, based on control voltage applied to the mode-select pin.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Direct LED Interface
Constant 3 dB
per Step Logarithmic Scale
External Mode-Select
for Dot/Bar-Graph Formats
Adjustable Output Current Levels
Adjustable Zero dB Reference

APPLICATIONS

Bar-Graph Generator — Logarithmic Level Indicator
Moving Dot Display Generator — Sequential Level Indicator

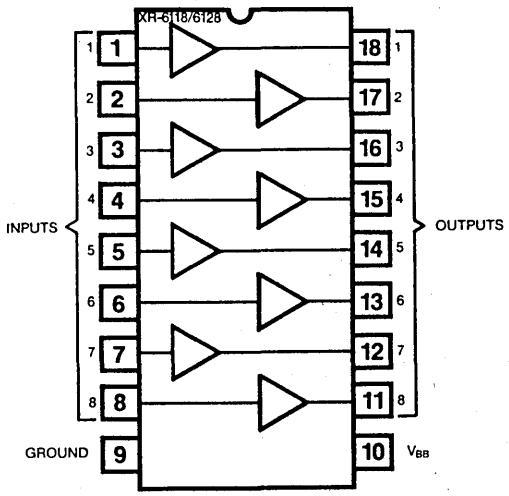
ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2279CP	Plastic	0°C to +70°C

XR-6118/6128 FLUORESCENT DISPLAY DRIVER

The XR-6118 and XR-6128 are high-voltage display driver arrays which are designed to interface between low-level digital logic and vacuum fluorescent displays. Each circuit consists of eight independent signal channels comprised of Darlington output stages and common-emitter type inputs. All channels on the chip share common power supply and ground connections. Both device types are capable of driving digits and/or segments of fluorescent displays, and all of the eight outputs can be activated simultaneously. The XR-6118 is compatible with TTL, DTL, Schottky TLL, and 5-volt CMOS logic families. The XR-6128 is intended for use with PMOS or CMOS logic families, operating with supply voltages of 6V to 15V.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Direct Replacement for Sprague 6118A/6128A
Digit or Segment Drivers
Low Power and Input Current
Internal Output Pulldown Resistors
High Output Breakdown Voltage — 75V, Minimum

APPLICATIONS

Fluorescent Driver — High-Voltage Switching
Gas Discharge Display Driver

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-6118P	Plastic	0°C to +85°C
XR-6128P	Plastic	0°C to +85°C

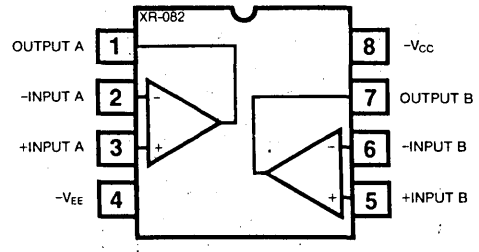
Operational Amplifiers

XR-082/083 DUAL BIFET OPERATIONAL AMPLIFIERS

The XR-082/083 family of junction FET input dual operational amplifiers are designed to offer higher performance than conventional bipolar op amps. Each amplifier features high slew rate, low input bias and offset currents, and low offset voltage drift with temperature. These operational amplifier circuits are fabricated using ion implantation technology to combine well-matched junction FET's and high-performance bipolar transistors on the same monolithic chip.

The XR-082 family of dual BIFET op amps are packaged in an 8-Pin dual-in-line package. The XR-083 family of op amps offers an independent offset adjustment for each of the individual op amps on the same chip, and are available in a 14-Pin dual-in-line package.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Direct Replacement for TL082/083
Low Power Consumption
Wide Common-Mode and Differential Voltage Ranges
Low Input Bias and Offset Currents
Output Short Circuit Protection
High-Input Impedance . . . . FET Input Stage
Internal Frequency Compensation
Latch-Up-Free Operation
High Slew Rate 13V/μs, Typical

APPLICATIONS

Transducer Amplifier High-Impedance Buffer

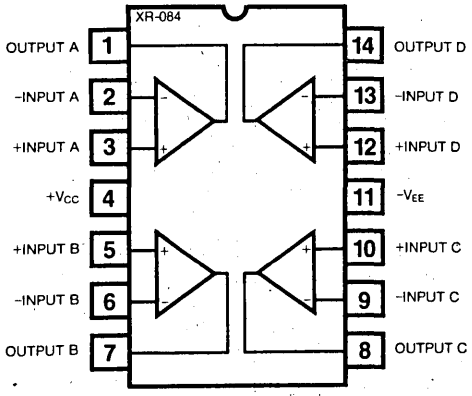
ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-082M	Ceramic	-55°C to +125°C
XR-082N	Ceramic	-25°C to +85°C
XR-082P	Plastic	-25°C to +85°C
XR-082CN	Ceramic	0°C to +70°C
XR-082CP	Plastic	0°C to +70°C
XR-083	Available in 14-Pin	

XR-084 QUAD BIFET OPERATIONAL AMPLIFIER

The XR-084 junction FET input quad operational amplifier is designed to offer higher performance than conventional bipolar quad op amps. Each of the four op amps on the chip is closely matched in performance characteristics, and each amplifier features high slew rate, low input bias and offset currents, and low offset voltage drift with temperature. The XR-084 FET input quad op amp is fabricated using ion implantation bipolar/FET or BIFET technology to combine well-matched junction FET's and high-performance bipolar transistors on the same monolithic chip.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Direct Replacement for TL084
Same Pin Configuration as XR-3403 and LM324
High-Impedance Junction FET Input Stage
Low Power Consumption
Wide Common-Mode and Differential Voltage Ranges
Low Input Bias and Offset Currents
Output Short Circuit Protection
Internal Frequency Compensation
Latch-Up Free Operation
High Slew Rate 13V/μs, Typical

APPLICATIONS

Transducer Amplifier High-Impedance Buffer

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-084M	Ceramic	-55°C to +125°C
XR-084N	Ceramic	-25°C to +85°C
XR-084P	Plastic	-25°C to +85°C
XR-084CN	Ceramic	0°C to +70°C
XR-084CP	Plastic	0°C to +70°C

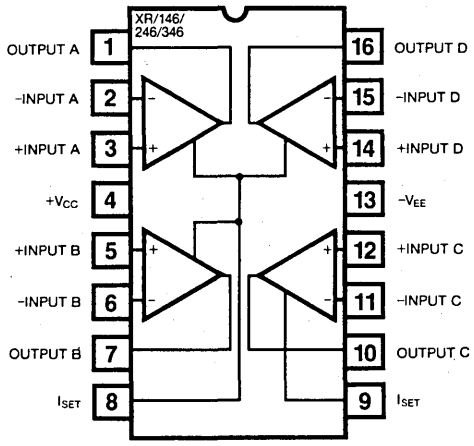
Operational Amplifiers

XR-146/246/346 PROGRAMMABLE QUAD OPERATIONAL AMPLIFIER

The XR-146 family of quad operational amplifiers contain four independent high-gain, low-power, programmable op amps on a monolithic chip. The use of external bias setting resistors permit the user to program the gain bandwidth product, supply current, input bias current, input offset current, input noise, and slew rate.

The basic XR-146 family of circuits offers partitioned programming of the internal op amps. One setting resistor is used to set the bias levels in the three op amps, and a second bias setting is used for the remaining op amp. Its modified version, XR-346-2, provides a separate bias setting resistor for each of the two op amp pairs.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Direct Replacement for LM146/246/346	
Direct Replacement for LM346-2	
Programmable Electrical Characteristics	
Low Supply Current	350 μA per Amplifier
Large dc Voltage Gain	120 dB
Low Noise Voltage	25 nV/$\sqrt{Hz}$
Wide Power Supply Range	± 1.5V to ± 22V
Class AB Output Stage	No Crossover Distortion

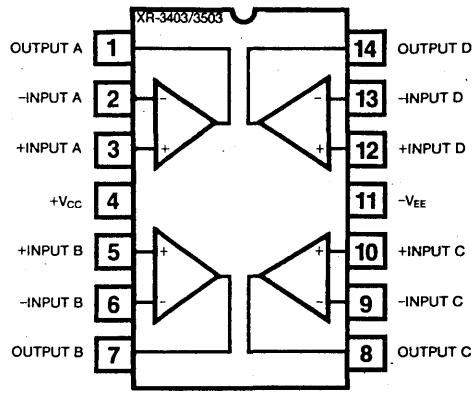
ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-146M	Ceramic	-55°C to +125°C
XR-246N	Ceramic	-25°C to +85°C
XR-246P	Plastic	-25°C to +75°C
XR-346CN	Ceramic	0°C to +70°C
XR-346CP	Plastic	0°C to +70°C
XR-346-2CN	Ceramic	0°C to +70°C
XR-346-2CP	Plastic	0°C to +70°C

XR-3403/3503 QUAD OPERATIONAL AMPLIFIER

The XR-3403 is an array of four independent operational amplifiers, each with true differential inputs. The device has electrical characteristics similar to the popular 741. However, the XR-3403 has several distinct advantages over standard operational amplifier types in single supply applications. The XR-3403 can operate at supply voltages as low as 3.0 volts, or as high as 36 volts. Quiescent currents remain about one-fifth of those associated with the 741 (on a per amplifier basis). The common-mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage swing extends to the negative supply.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Direct Pin for Pin Replacement for MC3403/3503, LM324 & RC4137	
Suitable for Single Supply Operation	
Short Circuit Protected Outputs	
Class AB Output Stage	No Crossover Distortion
Single Supply Operation	3.0V to 36V
Split Supply Operation	± 1.5V to ± 18V
Low Input Bias Currents	500 nA Maximum
Internally Compensated	

APPLICATIONS

Circuits Requiring Ground Sensing at Inputs
Low Supply Voltage Systems

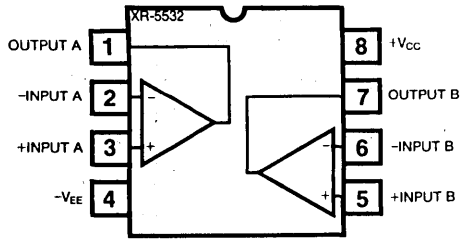
ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-3503M	Ceramic	-55°C to +125°C
XR-3403CN	Ceramic	0°C to +70°C
XR-3403CP	Plastic	0°C to +70°C

XR-5532/5532A DUAL LOW-NOISE OPERATIONAL AMPLIFIER

The XR-5532 ultralow noise dual operational amplifier is especially designed for high quality audio and instrumentation applications. Compared to standard 741- or 301A-type op amps, these operational amplifiers offer an order of magnitude improvement in both noise performance and small signal bandwidth. Higher output drive capability and internal compensation are added features. The XR-5532A is specially screened for a guaranteed ultralow noise specification. This ultralow noise specification makes the XR-5532A ideally suited for audio preamplifier and other low level applications.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Pin for Pin Replacement MC1458, RC4558, TL072 TL082 & LF 353
Direct Replacement for NE5532/NE5532A

Ultralow Input Noise	4 nV/$\sqrt{Hz}$, Typical
Wide Small Signal Bandwidth	10 MHz, Typical
High Output Drive Capability	10V rms into 600Ω
Wide Supply Range	± 3V to ± 20V
Wide Power Bandwidth	200 kHz
High Slew Rate	6V/μsec

APPLICATIONS

Professional Audio Equipment
Instrumentation and Servo Control
Telephone Channel Amplifier
Low-Level Signal Processing
Audio Preamplification
Transducer Amplifiers

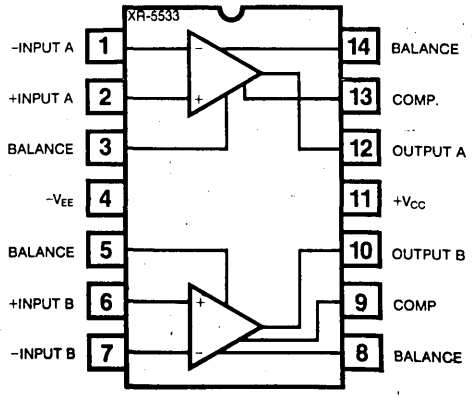
ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-5532ACN	Ceramic	0°C to +70°C
XR-5532CN	Ceramic	0°C to +70°C

XR-5533/5533A DUAL LOW-NOISE OPERATIONAL AMPLIFIER

The XR-5533 ultralow noise dual operational amplifier is especially designed for high quality audio and instrumentation applications. Compared to the standard 741- or 301A-type op amps, these operational amplifiers offer an order of magnitude improvement in noise performance, and small signal bandwidth, in addition to higher output drive capability. The XR-5533 is internally compensated for a voltage gain of three or more, and offers independent offset adjustments for each of the two op amps. The XR-5533A is specially screened for a guaranteed ultralow noise specification.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Direct Replacement for NE5533/NE5533A

Ultralow Input Noise	4 nV/$\sqrt{Hz}$, Typical
Wide Small Signal Bandwidth	10 MHz, Typical
High Output Drive Capability	10V rms into 600Ω
Wide Supply Range	± 3V to ± 20V
Wide Power Bandwidth	200 kHz
High Slew Rate	13V/μsec

APPLICATIONS

Professional Audio Equipment
Instrumentation and Servo Control
Telephone Channel Amplifier
Low-Level Signal Processing
Audio Preamplification

ORDERING INFORMATION

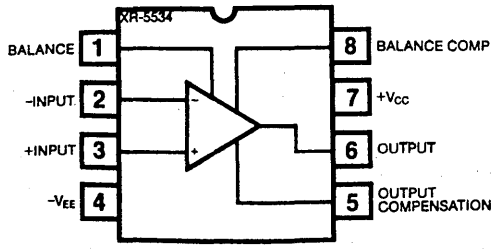
Part Number	Package	Operating Temperature
XR-5533ACN	Ceramic	0°C to +70°C
XR-5533CN	Ceramic	0°C to +70°C
XR-5533ACP	Plastic	0°C to +70°C
XR-5533CP	Plastic	0°C to +70°C

Operational Amplifiers

XR-5534/5534A LOW-NOISE OPERATIONAL AMPLIFIER

The XR-5534 is a high performance, ultralow noise operational amplifier. Compared to the standard 741- or 301A-type op amps, it offers an order of magnitude improvement in noise performance, and small signal bandwidth, as well as significantly better output drive capability. The XR-5534 is ideally suited for applications in high quality and professional audio equipment, instrumentation, control circuits, and telephone channel amplifiers. The op amp is internally compensated for a gain of three or greater. The frequency response can be optimized with an external compensation capacitor for applications requiring unity-gain, low-overshoot response, or capacitive load driving. The XR-5534A is specially screened for a guaranteed ultralow noise specification.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Direct Replacement for NE5534/NE5534A	
Ultralow Input Noise	4 nV/√Hz, Typical
Wide Small Signal Bandwidth	10 MHz, Typical
High Output Drive Capability	10V rms into 600Ω
Wide Supply Range	± 3V to ± 20V
High-Voltage Gain	Av = 100,000 at dc
High Slew Rate	13V/μsec

APPLICATIONS

Professional Audio Equipment
Audio Preamplification

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-5534AM	Ceramic	-55°C to +125°C
XR-5534M	Ceramic	-55°C to +125°C
XR-5534ACN	Ceramic	0°C to +70°C
XR-5534CN	Ceramic	0°C to +70°C
XR-5534ACP	Plastic	0°C to +70°C
XR-5534CP	Plastic	0°C to +70°C

Technical Literature

SWITCHING REGULATOR DATA BOOK:

Exar's entire line of switching regulator IC products are specified in this technical data book. In addition, several design and application articles are included, along with a review of the fundamentals of pulse-width modulated regulator circuits.

TIMER DATA BOOK:

Provided in this publication is a collection of technical articles and application information on monolithic timer IC products. Also included are the data sheets and detailed electrical specifications for all of Exar's timer circuits, including the programmable timer/counter, micropower, and long-delay timers.

PHASE-LOCKED LOOP DATA BOOK:

The fundamentals of design and application of monolithic phase-locked loop (PLL) circuits are included in this data book. A long list of PLL applications are illustrated covering FM demodulation, frequency synthesis, FSK, and tone detection. Particular emphasis is given to the application of PLL circuits in data interface and communication systems such as FSK MODEMS. This book also contains the data sheets and electrical specifications for all of Exar's PLL products.

FUNCTION GENERATOR DATA BOOK:

This comprehensive data book contains a number of technical articles and application notes on monolithic voltage-controlled oscillators (VCO), and function generator IC products. In addition, the data sheets and technical specifications for Exar's monolithic VCO's and function generators are included.

OPERATIONAL AMPLIFIER DATA BOOK:

A collection of technical articles on the fundamentals of monolithic IC op amps is contained in this technical publication. Some of the basic op amp circuits are given, and the application of IC op amps in active filter design is discussed. A complete set of electrical specifications on Exar's bipolar and BIFET op amp products is included.

APPLICATIONS DATA BOOK:

This practical applications guide contains a complete and up-to-date set of application notes prepared by Exar's technical staff. These application notes cover a wide range of subjects, such as FSK MODEMS, active filters, telecommunication circuits, electronic music synthesis and many more. In each case, specific design examples are given to demonstrate the applications discussed.

HARRIS

HA-1608

+10V Adjustable Voltage Reference

FEATURES

- MONOLITHIC CONSTRUCTION
- INITIAL ACCURACY +10V ± 0.010V
- OUTPUT VOLTAGE ERROR, TOTAL ±1/4 LSB
- LOW NOISE 20μV_{p-p}
- WIDE INPUT RANGE 12V TO 30V
- LOW POWER DISSIPATION 30mW
- OUTPUT SHORT CIRCUIT PROTECTION
- ADJUSTABLE OUTPUT

APPLICATIONS

- AN ECONOMICAL EXTERNAL REFERENCE FOR: HI-5608; DAC 08; AD1408; AD559
- VOLTAGE REGULATOR REFERENCE
- PORTABLE BATTERY OPERATED EQUIPMENT
- NEGATIVE 10V REFERENCE

DESCRIPTION

HA-1608 is a monolithic +10V adjustable voltage reference featuring accuracy and temperature stability specifications detailed exclusively for 8 bit data conversion systems. A stable +10V output is provided by a reference zener and buffer amplifier coupled with laser trimmed feedback and zener bias resistors. Long term stability is ensured through integration of all reference components into a monolithic design. Flexibility of HA-1608 is provided through an external trim control which allows the user to adjust the output voltage for binary or BCD applications without affecting overall performance.

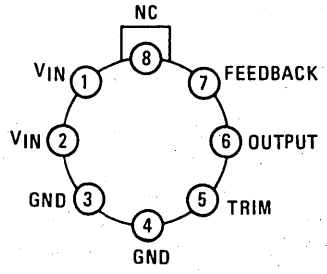
These devices provide a total output voltage error of ± 1/4 LSB for 8 bit D/A or A/D converters. Low standby power (0.3mW) makes HA-1608 a natural selection for portable battery operated equipment, comparator references, and reference stacking circuits. These devices can also be used on -10V references.

HA-1608 is packaged in 8 pin metal cans (TO-99) and the pinout is arranged for convenient replacement of other less accurate regulators in applications demanding minimal change with temperature and time. HA-1608-2 is specified for -55°C to +125°C operation while the HA-1608-5 operates from 0°C to +75°C.

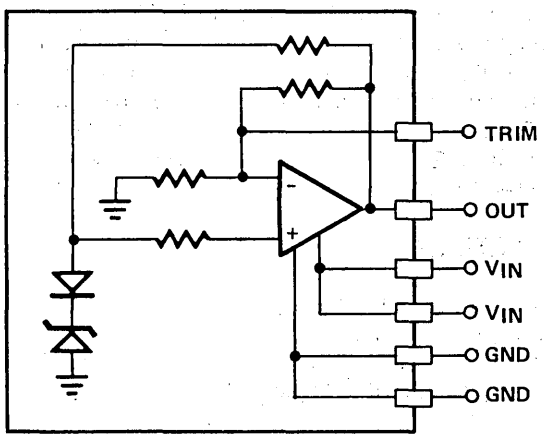
PINOUT

Section 11 for Packaging

TOP VIEW



FUNCTIONAL SCHEMATIC



See Pages 3287-3291 for Package Information.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Voltage	40V	Operating Temperature Range	
Output Short Circuit Duration	Indefinitely	HA-1608-2	-55°C to +125°C
Power Dissipation	500mW	HA-1608-5	0°C to +75°C
Storage Temperature Range	-65°C to +150°C		

ELECTRICAL CHARACTERISTICS (Note 2) (V_{IN} = +15V, I_L = 0mA, unless otherwise specified)

PARAMETER	TEMP	HA-1608-2 -55°C to +125°C MIN	HA-1608-2 -55°C to +125°C TYP	HA-1608-2 -55°C to +125°C MAX	HA-1608-5 0°C to +75°C MIN	HA-1608-5 0°C to +75°C TYP	HA-1608-5 0°C to +75°C MAX	UNITS
POWER INPUT CHARACTERISTICS								
Input Voltage Range, V_{IN}	Full	12	15	30	12	15	30	V
Quiescent Current, I_Q	25°C		1.9			1.9		mA
	Full			3.0			3.0	
REGULATED OUTPUT CHARA.'S								
Output Voltage, V_O	25°C	9.990	10.00	10.010	9.990	10.00	10.010	V
Output Load Current, I_L	Full	10	20		10	20		mA
Line Regulation (V_{IN} = 12V to 30V)	25°C		0.006			0.006		%/V
	Full			0.015			0.015	
Load Regulation (I_L = Open to 10mA)	25°C		0.006			0.006		%/mA
	Full			0.015			0.015	
Output Voltage Error Total I_L = 0mA (Relative to 8-bit accuracy, see Definition #3)	Full			±1/4 LSB			±1/4 LSB	
Output Noise Voltage, EN 0.1Hz to 10Hz	Full		35			35		μV_{p-p}
Dynamic Load Settling Time to ±0.1%	25°C		2.5			2.5		µs
to ±0.01%	25°C		5			5		
Warm-up Time (to ±0.01%)	25°C		1			1		sec
	Full		3			3		

NOTES:

1. Absolute maximum ratings are limiting values beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.

2. The specified electrical characteristics apply to suggested hook-up only.

HARRIS HA-2400/2404/2405

PRAM Four Channel Programmable Amplifier

FEATURES

- PROGRAMMABILITY
- HIGH SLEW RATE 30V/μs
- WIDE GAIN BANDWIDTH 40MHz
- HIGH GAIN 150,000
- LOW OFFSET CURRENT 5nA
- HIGH INPUT IMPEDANCE 30MΩ
- SINGLE CAPACITOR COMPENSATION
- DTL/TTL COMPATIBLE INPUTS

APPLICATIONS

- THOUSANDS OF NEW APPLICATIONS; PROGRAM
  - SIGNAL SELECTION/MULTIPLEXING
  - OP AMP GAIN
  - OSCILLATOR FREQUENCY
  - FILTER CHARACTERISTICS
  - ADD-SUBTRACT FUNCTIONS
  - INTEGRATOR CHARACTERISTICS
  - COMPARATOR LEVELS

DESCRIPTION

HA-2400/2404/2405 comprise a series of four-channel programmable amplifiers providing a level of versatility unsurpassed by any other monolithic operational amplifier. Versatility is achieved by employing four input amplifier channels, any one (or none) of which may be electronically selected and connected to a single output stage through DTL/TTL compatible address inputs. The device formed by the output and the selected pair of inputs is an op amp which delivers excellent slew rate, gain bandwidth and power bandwidth performance. Other advantageous features for these dielectrically isolated amplifiers include high voltage gain and input impedance coupled with low input offset voltage and offset current. External compensation is not required on this device at closed loop gains greater than 10.

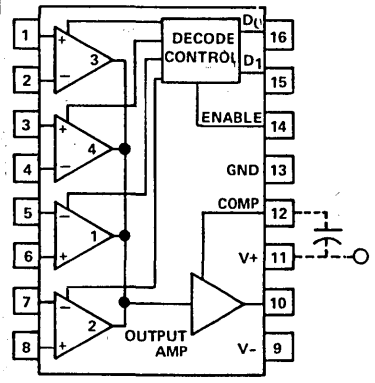
Each channel of the HA-2400/2404/2405 can be controlled and operated with suitable feedback networks in any of the standard op amp configurations. This specialization makes these amplifiers excellent components for multiplexing, signal selection, and mathematical function designs. With 30V/μs slew rate, 40MHz gain bandwidth, and 30M ohms input impedance these devices are ideal building blocks for signal generators, active filters, and data acquisition designs. Programmability coupled with 2mV typical offset voltage and 5nA offset current makes these amplifiers outstanding components for signal conditioning circuits.

HA-2400/2404/2405 are available in a 16 pin dual-in-line package. HA-2400 is specified from -55°C to +125°C. HA-2404 is specified over the -25°C to +85°C range, while HA-2405 operates from 0°C to +75°C.

PINOUT

TOP VIEW

Section 11 for Packaging



TRUTH TABLE

D_1	D_0	EN	SELECTED CHANNEL
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4
X	X	L	NONE

SCHEMATIC

Condensed circuit diagram for a programmable amplifier (PRAM HA-2400)

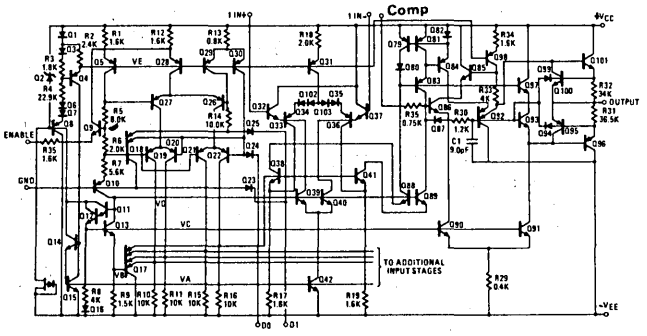


Diagram includes: ONE INPUT STAGE, DECODE CONTROL, BIAS NETWORK AND OUTPUT STAGE

See Pages 3287-3291 for Package Information.

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V− Terminals	45.0V	Internal Power Dissipation (Note 13)	300mW
Differential Input Voltage	$\pm V_{Supply}$	Operating Temperature Range	$-55^oC \leq T_A \leq +125^oC$ (HA-2400)
Digital Input Voltage	−0.76V to +10.0V		$-25^oC \leq T_A \leq +85^oC$ (HA-2404)
Output Current	Short Circuit Protected ($I_{SC} \leq \pm 33mA$)		$0^oC \leq T_A \leq +75^oC$ (HA-2405)
		Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS

Test Conditions: $V_{Supply} = \pm 15.0V$ unless otherwise specified.

Digital inputs: $V_{IL} = +0.5V$, $V_{IH} = +2.4V$
Limits apply to each of the four channels, when addressed.

PARAMETER	TEMP.	HA-2400/HA-2404 LIMITS MIN.	TYP.	MAX.	HA-2405 LIMITS MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		4	9		4	9	mV
	Full			11			11	mV
Bias Current (Note 12)	+25°C		50	200		50	250	nA
	Full			400			500	nA
Offset Current (Note 12)	+25°C		5	50		5	50	nA
	Full			100			100	nA
Input Resistance (Note 12)	+25°C		30			30		MΩ
Common Mode Range	Full	±9.0			±9.0			V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 1,5)	+25°C	50K	150K		50K	150K		V/V
	Full	25K			25K			V/V
Common Mode Rejection Ratio (Note 2)	Full	80	100		74	100		dB
Gain Bandwidth (Note 3)	+25°C	20	40		20	40		MHz
(Note 4)	+25°C	4	8		4	8		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		V
Output Current	+25°C	10	20		10	20		mA
Full Power Bandwidth (Notes 3, 5)	+25°C	200	500		200	500		kHz
(Notes 4,5)	+25°C	100	200		100	200		kHz
TRANSIENT RESPONSE								
Rise Time (Notes 4,6)	+25°C		20	45		20	50	ns
Overshoot (Notes 4,6)	+25°C		25	40		25	40	%
Slew Rate (Notes 3,7)	+25°C	20	30		20	30		V/μs
(Notes 4,7)	+25°C	6	8		6	8		V/μs
Settling Time (Notes 4, 7, 8)	+25°C		1.5	2.5		1.5	2.5	μs
CHANNEL SELECT CHARACTERISTICS								
Digital Input Current ($V_{IN} = 0V$)	Full		1	1.5		1	1.5	mA
Digital Input Current ($V_{IN} = +5.0V$)	Full		5			5		nA
Output Delay (Note 9)	+25°C		100	250		100	250	ns
Crosstalk (Note 10)	+25°C	-80	-110		-74	-110		dB
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		4.8	6.0		4.8	6.0	mA
Power Supply Rejection Ratio (Note 11)	Full	74	90		74	90		dB

NOTES:
1. $R_L = 2K\Omega$
2. $V_{CM} = \pm 5V$.D.C.
3. $A_V = +10$, $C_{COMP} = 0$, $R_L = 2K\Omega$, $C_L = 50pF$
4. $A_V = +1$, $C_{COMP} = 15pF$, $R_L = 2K\Omega$, $C_L = 50pF$
5. $V_{OUT} = 20V$ peak-to-peak
6. $V_{OUT} = 200mV$ peak-to-peak
7. $V_{OUT} = 10.0V$ peak-to-peak
8. To 0.1% of final value
9. To 10% of final value; output then slews at normal rate to final value.
10. Unselected input to output; $V_{IN} = \pm 10$ V.D.C.
11. $V_{SUPP} = \pm 10V$.D.C. to $\pm 20V$.D.C.
12. Unselected channels have approximately the same input parameters.
13. Derate by 4.3mW/°C above 105°C

HARRIS

HA-2420/2425

Fast Sample and Hold

FEATURES

- LOW DROOP RATE (C_H = 1000pF) 5μV/ms
- LOW CHARGE TRANSFER 5pC
- FAST ACQUISITION TIME (10V STEP TO .01%) 5μs
- HIGH SLEW RATE 7V/μs
- BANDWIDTH 2.5MHz
- LOW APERTURE TIME 30ns
- TTL COMPATIBLE CONTROL INPUT

APPLICATIONS

- A TO D CONVERSION SYSTEMS
- D TO A DEGLITCHER
- AUTO ZERO SYSTEMS
- PEAK DETECTOR
- GATED OP AMP

DESCRIPTION

The HA-2420/2425 is a monolithic circuit consisting of a high performance operational amplifier with its output in series with an ultra-low leakage analog switch and a MOSFET input unity gain amplifier.

With an external holding capacitor connected to the switch output, a versatile, high performance sample-and-hold or track-and-hold circuit is formed. When the switch is closed, the device behaves as an operational amplifier, and any of the standard op amp feedback networks may be connected around the device to control gain, frequency response, etc. When the switch is opened the output will remain at its last level.

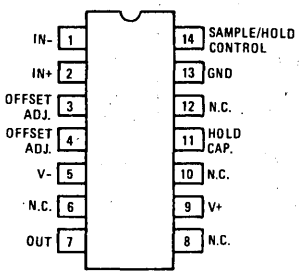
Performance as a sample-and-hold compares very favorably with other monolithic, hybrid, modular, and discrete circuits. Accuracy to better than 0.01% is achievable over the temperature range. Fast acquisition is coupled with superior droop characteristics, even at high temperatures. High slew rate, wide bandwidth, and low acquisition time produce excellent dynamic characteristics. The ability to operate at gains greater than 1 frequently eliminates the need for external scaling amplifiers.

The device may also be used as a versatile operational amplifier with a gated output for applications such as analog switches, peak holding circuits, etc.

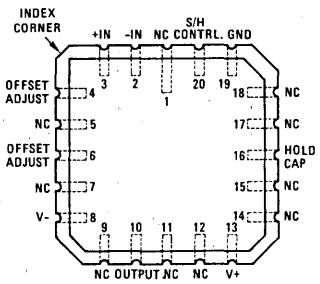
PINOUT

Section 11 for Packaging

TOP VIEW

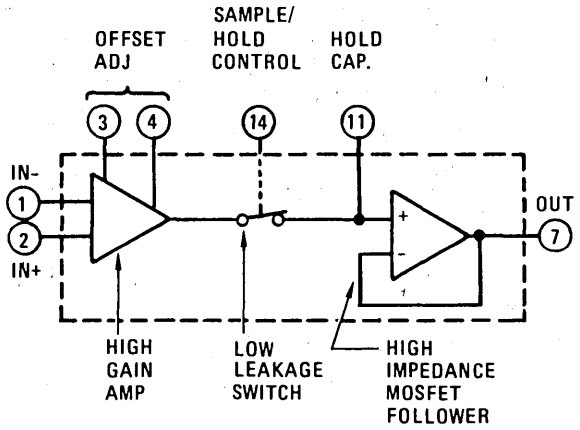


14 PIN DIP



LEADLESS CHIP CARRIER (LCC) PACKAGE

FUNCTIONAL DIAGRAM



See Pages 3287-3291 for Package Information.

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	40V	Operating Temperature Range	
Differential Input Voltage	±24V	HA-2420-2/8	$-55^{o}C \leq T_A \leq +125^{o}C$
Digital Input Voltage (Pin 14)	+8V, -15V	HA-2425-5	$0^{o}C \leq T_A \leq +75^{o}C$
Output Current	Short Circuit Protected	Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$
Internal Power Dissipation	300mW (Note 7)		

ELECTRICAL CHARACTERISTICS

Test Conditions (Unless otherwise specified) $V_{SUPPLY} = \pm 15.0V$; $C_H = 1000pF$; Digital Input (Pin 14), $V_{IL} = +0.8V$ (Sample), $V_{IH} = +2.0V$ (Hold)

PARAMETER	TEMP	HA-2420-2 MIN	HA-2420-2 TYP	HA-2420-2 MAX	HA-2425-5 MIN	HA-2425-5 TYP	HA-2425-5 MAX	UNITS
INPUT CHARACTERISTICS								
*Offset Voltage	+25°C		2	4		3	6	mV
	Full		3	6		4	8	mV
*Bias Current	+25°C		40	200		40	200	nA
	Full			400			400	nA
*Offset Current	+25°C		10	50		10	50	nA
	Full			100			100	nA
Input Resistance	+25°C	5	10		5	10		MΩ
Common Mode Range	Full	±10			±10			V
TRANSFER CHARACTERISTICS								
*Large Signal Voltage Gain (Note 1, 4)	Full	25K	50K		25K	50K		V/V
*Common Mode Rejection (Note 2)	Full	80	90		74	90		dB
Hold Mode Feedthrough Attenuation (Note 9)	Full		-76			-76		dB
Gain Bandwidth Product (Note 3)	+25°C		2.5			2.5		MHz
OUTPUT CHARACTERISTICS								
*Output Voltage Swing (Note 1)	Full	±10			±10			V
Output Current	+25°C	±15			±15			mA
Full Power Bandwidth (Note 3, 4)	+25°C		100			100		kHz
Output Resistance (D.C.)	+25°C		.15			.15		Ω
TRANSIENT RESPONSE								
Rise Time (Note 3, 5)	+25°C		50			50		ns
Overshoot (Note 3, 5)	+25°C		25			25		%
Slew Rate (Note 3, 6)	+25°C		7			7		V/μs
DIGITAL INPUT CHARACTERISTICS								
Digital Input Current ($V_{IN} = 0V$)	Full			0.8			0.8	mA
Digital Input Current ($V_{IN} = +5.0V$)	Full			20			20	μA
Digital Input Voltage (Low)	Full			0.8			0.8	V
Digital Input Voltage (High)	Full	2.0			2.0			V
SAMPLE/HOLD CHARACTERISTICS								
Acquisition Time to .1% 10V Step (Note 3)	+25°C		4			4		μs
Acquisition Time to .01% 10V Step (Note 3)	+25°C		5			5		μs
Aperture Time	+25°C		30			30		ns
Aperture Delay Time	+25°C		50			50		ns
Aperture Uncertainty Time	+25°C		5			5		ns
*Drift Current (Note 3, 8)	+25°C		5	50		5	50	pA
	Full		0.5	4.0		0.5	1.0	nA
*Charge Transfer (Note 8)	+25°C		5	10		5	10	pC
POWER SUPPLY CHARACTERISTICS								
*Supply Current (+)	+25°C		3.5	5.5		3.5	5.5	mA
*Supply Current (-)	+25°C		2.5	3.5		2.5	3.5	mA
*Power Supply Rejection	Full	80	90		74	90		dB

NOTES:
1. $R_L = 2k\Omega$
2. $V_{CM} = \pm 10VDC$
3. $A_V = +1$, $R_L = 2k\Omega$, $C_L = 50pF$
4. $V_{OUT} = 20V$ peak-to-peak
5. $V_{OUT} = 400mV$ peak-to-peak
6. $V_{OUT} = 10.0V$ peak-to-peak
7. Derate Power Dissipation by 4.3mW/°C above +105°C Ambient Temperature
8. $V_{IN} = 0V$
9. $f_{IN} \leq 100kHz$

*100% Tested for DASH 8

HARRIS

HA-2500/02/05

Precision High Slew Rate Operational Amplifiers

FEATURES

- HIGH SLEW RATE 30V/μS
- FAST SETTLING 330ns
- WIDE POWER BANDWIDTH 500kHz
- HIGH GAIN BANDWIDTH 12MHz
- HIGH INPUT IMPEDANCE 50 MΩ
- LOW OFFSET CURRENT 10nA
- INTERNALLY COMPENSATED

APPLICATIONS

- DATA ACQUISTION SYSTEMS
- R.F. AMPLIFIERS
- VIDEO AMPLIFIERS
- SIGNAL GENERATORS
- PULSE AMPLIFICATION

DESCRIPTION

HA-2500/2502/2505 comprise a series of monolithic operational amplifiers whose designs are optimized to deliver excellent slew rate, bandwidth, and settling time specifications. The outstanding dynamic features of this internally compensated device are complemented with low offset voltage and offset current.

These dielectrically isolated amplifiers are ideally suited for applications such as data acquisition, R.F., video, and pulse conditioning circuits. Slew rate of ±25V/μs and 330ns (0.1%) settling time make these devices excellent components in fast, accurate data acquisition and pulse amplification designs. 12 MHz bandwidth and 500kHz power bandwidth make these devices well suited to R.F. and video applications. With 2mV typical offset voltage plus offset trim capability and 10nA offset current, HA-2500/2502/2505 are particularly useful components in signal conditioning designs.

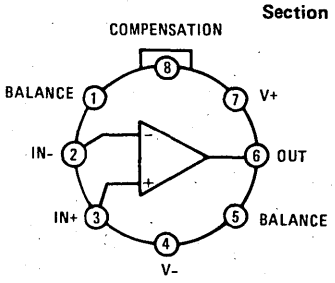
The gain and offset voltage figures of the HA-2500 series are optimized by internal component value changes while the similar design of the HA-2510 series is maximized for slew rate.

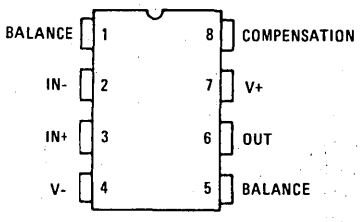
HA-2500/2502/2505 are available in metal can (TO-99) packages. HA-2500 and HA-2502 are specified over the -55°C to +125°C range. HA-2505 is specified from 0°C to +75°C.

PINOUT

Section 11 for Packaging

TOP VIEWS





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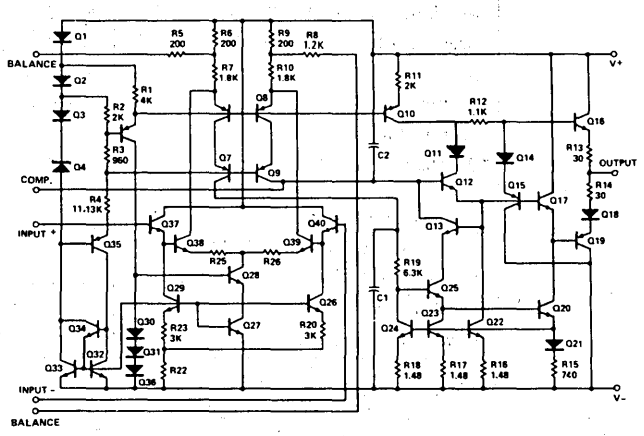


See Pages 3287-3291 for Package Information.

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	40.0V	Operating Temperature Range –	HA-2500/HA-2502	$-55^oC \leq T_A \leq +125^oC$
Differential Input Voltage	±15.0V		HA-2505	$0^oC \leq T_A \leq +75^oC$
Peak Output Current	50mA	Storage Temperature Range		$-65^oC \leq T_A \leq +150^oC$
Internal Power Dissipation	300mW			

ELECTRICAL CHARACTERISTICS

V+ = +15V D.C., V- = -15V D.C.

		HA-2500 -55°C to +125°C			HA-2502 -55°C to +125°C			HA-2505 0°C to +75°C			
		LIMITS			LIMITS			LIMITS			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS											
Offset Voltage	+25°C Full		2	5 8		4	8 10		4	8 10	mV mV
Offset Voltage Average Drift	Full		20			20			20		µV/°C
Bias Current	+25°C Full		100	200 400		125	250 500		125	250 500	nA nA
Offset Current	+25°C Full		10	25 50		20	50 100		20	50 100	nA nA
Input Resistance (Note 10)	+25°C	25	50		20	50		20	50		MΩ
Common Mode Range	Full	±10.0			±10.0			±10.0			V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 1,4)	+25°C Full	20K 15K	30K		15K 10K	25K		15K 10K	25K		V/V V/V
Common Mode Rejection Ratio (Note 2)	Full	80	90		74	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C		12			12			12		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
Output Current (Note 4)	+25°C	±10	±20		±10	±20		±10	±20		mA
Full Power Bandwidth (Note 4)	+25°C	350	500		300	500		300	500		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		25	50		25	50		25	50	ns
Overshoot (Notes 1, 5, 7 & 8)	+25°C		25	40		25	50		25	50	%
Slew Rate (Notes 1,5,8 & 12)	+25°C	±25	±30		±20	±30		±20	±30		V/µs
Settling Time to 0.1% (Notes 1,5,8 & 12)	+25°C		0.33			0.33			0.33		µs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C		4	6		4	6		4	6	mA
Power Supply Rejection Ratio (Note 9)	Full	80	90		74	90		74	90		dB

NOTES:
1. R_L = 2K
2. $V_{CM} = \pm 10V$
3. $A_V > 10$
4. $V_O = \pm 10.0V$
5. C_L = 50pF
6. $V_O = \pm 200mV$
7. $V_O \pm 200mV$
8. See transient response test circuits and waveforms page four.
9. $\Delta V = \pm 5.0V$
10. This parameter value is based on design calculations.
11. Full power bandwidth guaranteed based on slew rate measurement using FPBW = S.R./2π V_{peak}.
12. $V_{OUT} = \pm 5V$

HARRIS

HA-2510/2512/2515

High Slew Rate Operational Amplifiers

FEATURES

- HIGH SLEW RATE 60V/μs
- FAST SETTLING 250ns
- WIDE POWER BANDWIDTH 1,000kHz
- HIGH GAIN BANDWIDTH 12MHz
- HIGH INPUT IMPEDANCE 100MΩ
- LOW OFFSET CURRENT 10nA
- INTERNALLY COMPENSATED

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- R.F. AMPLIFIERS
- VIDEO AMPLIFIERS
- SIGNAL GENERATORS
- PULSE AMPLIFICATION

DESCRIPTION

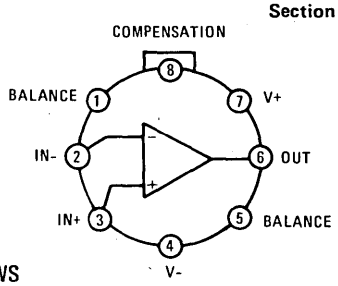
The HA-2510/2512/2515 are a series of high performance operational amplifiers which set the standards for maximum slew rate, highest accuracy and widest bandwidth for internally compensated monolithic devices. In addition to excellent dynamic characteristics, these dielectrically isolated amplifiers also offer low offset current and high input impedance.

The ±60V/ μs slew rate and 250ns (0.1%) settling time of these amplifiers is ideally suited for high speed D/A, A/D, and pulse amplification designs. HA-2510/2512/2515's superior 12MHz gain bandwidth and 1000kHz power bandwidth is extremely useful in R.F. and video applications. For accurate signal conditioning these amplifiers also provide 10nA offset current, coupled with 100MΩ input impedance, and offset trim capability.

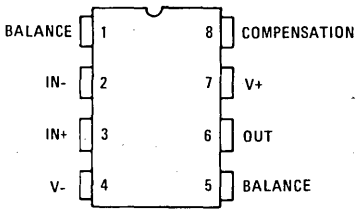
The HA-2510/2512 are available in metal can (TO-99) and 14-pin flat packages. HA-2510 and HA-2512 are specified from -55°C to +125°C. HA-2515 is specified over the 0°C to +75°C range, and is available in the TO-99 package.

PINOUT

Section 11 for Packaging



TOP VIEWS



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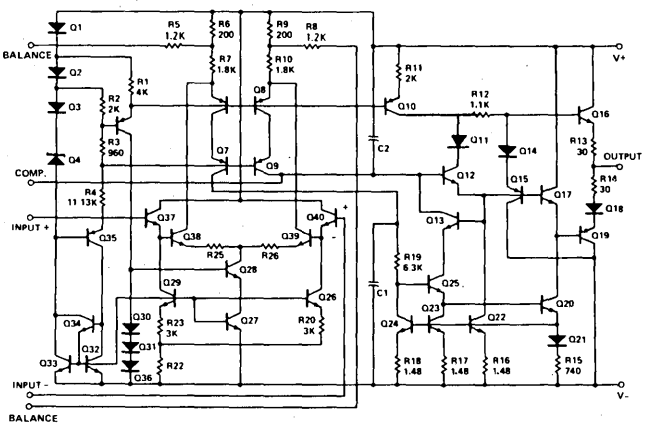


See Pages 3287-3291 for Package Information.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	40.0V	Peak Output Current	50mA
Differential Input Voltage	±15.0V	Internal Power Dissipation	300mW
Operating Temperature Range		Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$
HA-2510/HA-2512	$-55^oC \leq T_A \leq +125^oC$		
HA-2515	$0^oC \leq T_A \leq +75^oC$		

ELECTRICAL CHARACTERISTICS

V+ = +15V D.C., V– = 15V D.C.

PARAMETER	TEMP.	HA-2510 -55°C to +125°C LIMITS MIN.	HA-2510 TYP.	HA-2510 MAX.	HA-2512 -55°C to +125°C LIMITS MIN.	HA-2512 TYP.	HA-2512 MAX.	HA-2515 0°C to +75°C LIMITS MIN.	HA-2515 TYP.	HA-2515 MAX.	UNITS
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		4	8		5	10		5	10	mV
	Full			11			14			14	mV
Offset Voltage Average Drift	Full		20			25			30		µV/°C
Bias Current	+25°C		100	200		125	250		125	250	nA
	Full			400			500			500	nA
Offset Current	+25°C		10	25		20	50		20	50	nA
	Full			50			100			100	nA
Input Resistance (Note10)	+25°C	50	100		40	100		40	100		MΩ
Common Mode Range	Full	±10.0			±10.0			±10.0			V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 1,4)	+25°C	10K	15K		7.5K	15K		7.5K	15K		V/V
	Full	7.5K			5K			5K			V/V
Common Mode Rejection Ratio (Note 2)	Full	80	90		74	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C		12			12			12		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
Output Current (Note 4)	+25°C	±10	±20		±10	±20		±10	±20		mA
Full Power Bandwidth (Note 4, 11)	+25°C	750	1000		600	1000		600	1000		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		25	50		25	50		25	50	ns
Overshoot (Notes 1, 5, 7 & 8)	+25°C		25	40		25	50		25	50	%
Slew Rate (Notes 1, 5, 8 & 12)	+25°C	±50	±65		±40	±60		±40	±60		V/µs
Settling Time (Notes 1, 5, 8 & 12)	+25°C		0.25			0.25			0.25		µs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C		4	6		4	6		4	6	mA
Power Supply Rejection Ratio (Note 9)	Full	80	90		74	90		74	90		dB

NOTES:
1. R_L = 2K
2. $V_{CM} = \pm 10V$
3. $A_V > 10$
4. $V_O = \pm 10.0V$
5. C_L = 50pF
6. $V_O = \pm 200mV$
7. $V_O = \pm 200mV$
8. See transient response test circuits and waveforms
9. $\Delta V = \pm 5.0V$
10. This parameter value is based upon design calculations.
11. Full power bandwidth guaranteed based upon slew rate measurement FPBW = S.R./$2\pi V_{peak}$.
12. $V_{OUT} = \pm 5V$

HARRIS

HA-2520/22/25

Uncompensated High Slew Rate Operational Amplifiers

FEATURES

- HIGH SLEW RATE 120V/μs
- FAST SETTLING 200ns
- WIDE POWER BANDWIDTH 2,000kHz
- HIGH GAIN BANDWIDTH 20MHz
- HIGH INPUT IMPEDANCE 100MΩ
- LOW OFFSET CURRENT 10nA

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- R.F. AMPLIFIERS
- VIDEO AMPLIFIERS
- SIGNAL GENERATORS
- PULSE AMPLIFICATION

DESCRIPTION

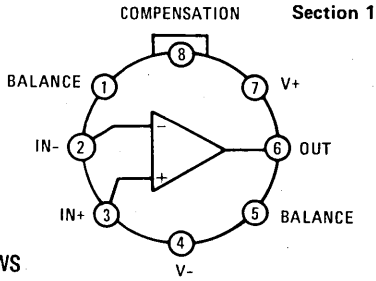
HA-2520/2522/2525 comprise a series of monolithic operational amplifiers delivering an unsurpassed combination of specifications for slew rate, bandwidth and settling time. These dielectrically isolated amplifiers are controlled at closed loop gains greater than 3 without external compensation. In additon, these high performance components also provide low offset current and high input impedance.

120V/μs slew rate and 200ns (0.1%) settling time of these amplifiers make them ideal components for pulse amplification and data acquisition designs. These devices are valuable components for R.F. and video circuitry requiring up to 20MHz gain bandwidth and 2MHz power bandwidth. For accurate signal conditioning designs the HA-2520/2522/2525's superior dynamic specifications are complimented by 10nA offset current, 100MΩ input impedance and offset trim capability.

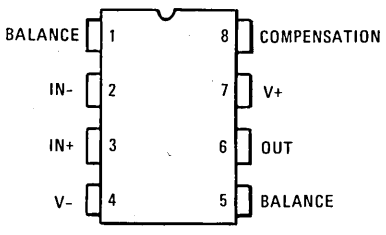
The HA-2520/2522 are available in metal can (TO-99) and 14-pin flat packages. HA-2520 and HA-2522 are specified over -55°C to +125°C range. HA-2525 is specified from 0°C to +75°C, and is available in the TO-99 package.

PINOUT

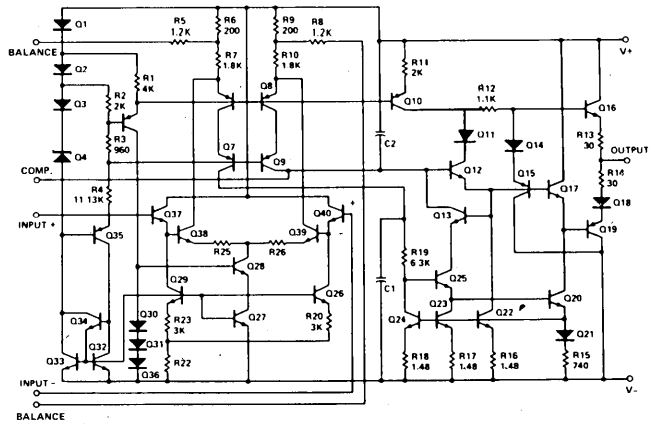
Section 11 for Packaging



TOP VIEWS



SCHEMATIC



See Pages 3287-3291 for Package Information.

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	40.0V	Peak Output Current	50mA
Differential Input Voltage	±15.0V	Internal Power Dissipation	300mW
Operating Temperature Range			
HA-2520/2522	$-55^oC \leq T_A \leq +125^oC$	Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$
HA-2525	$0^oC \leq T_A \leq +75^oC$		

ELECTRICAL CHARACTERISTICS

V+ = +15V D.C., V- = -15V D.C.

PARAMETER	TEMP.	HA-2520 -55°C to +125°C LIMITS MIN.	HA-2520 TYP.	HA-2520 MAX.	HA-2522 -55°C to +125°C LIMITS MIN.	HA-2522 TYP.	HA-2522 MAX.	HA-2525 0°C to +75°C LIMITS MIN.	HA-2525 TYP.	HA-2525 MAX.	UNITS
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		4	8		5	10		5	10	mV
	Full			11			14			14	mV
Offset Voltage Average Drift	Full		20			25			30		µV/°C
Bias Current	+25°C		100	200		125	250		125	250	nA
	Full			400			500			500	nA
Offset Current	+25°C		10	25		20	50		20	50	nA
	Full			50			100			100	nA
Input Resistance (Note 9)	+25°C	50	100		40	100		40	100		MΩ
Common Mode Range	Full	±10.0			±10.0			±10.0			V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 1,4)	+25°C	10K	15K		7.5K	15K		7.5K	15K		V/V
	Full	7.5K			5K			5K			V/V
Common Mode Rejection Ratio (Note 2)	Full	80	90		74	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C	10	20		10	20		10	20		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
Output Current (Note 4)	+25°C	±10	±20		±10	±20		±10	±20		mA
Full Power Bandwidth (Note 4, 10)	+25°C	1500	2000		1200	1600		1200	1600		kHz
TRANSIENT RESPONSE (A_V = +3)											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		25	50		25	50		25	50	ns
Overshoot (Notes 1, 5, 6 & 8)	+25°C		25	40		25	50		25	50	%
Slew Rate (Notes 1, 5, 8 & 11)	+25°C	±100	±120		±80	±120		±80	±120		V/µs
Settling Time (Notes 1, 5, 8 & 11)	+25°C		0.20			0.20			0.20		µs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C		4	6		4	6		4	6	mA
Power Supply Rejection Ratio (Note 7)	Full	80	90		74	90		74	90		dB

NOTES:
1. R_L = 2K
2. $V_{CM} = \pm 10V$
3. $A_V > 10$
4. $V_O = \pm 10.0V$
5. C_L = 50pF
6. $V_O = \pm 200mV$
7. $\Delta V = \pm 5.0V$
8. See transient response test circuits and waveforms
9. This parameter value is based upon design calculations.
10. Full power bandwidth guaranteed based upon slew rate measurement FPBW = S.R./$2\pi V_{peak}$.
11. $V_{OUT} = \pm 5V$

HARRIS

HA-2539

Very High Slew Rate Wideband Operational Amplifiers

FEATURES

- VERY HIGH SLEW RATE — 600V/μs
- OPEN LOOP GAIN — 30kV/V
- WIDE GAIN-BANDWIDTH — 600MHz
- POWER BANDWIDTH — 9.5MHz
- LOW OFFSET VOLTAGE — 3mV
- INPUT VOLTAGE NOISE — 15nV/$\sqrt{\text{Hz}}$
- OUTPUT VOLTAGE SWING — $\pm$10V

APPLICATIONS

- PULSE AND VIDEO AMPLIFIERS
- WIDEBAND AMPLIFIERS
- HIGH SPEED SAMPLE-HOLD CIRCUITS
- RF OSCILLATORS

GENERAL DESCRIPTION

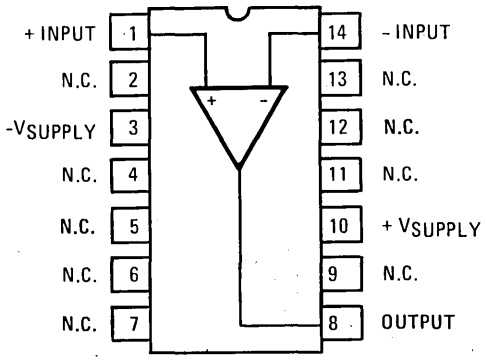
The Harris HA-2539 represents the ultimate in high slew rate wideband, monolithic, operational amplifiers. It has been designed and constructed with the Harris high frequency BIPDIP (Bipolar dielectric isolation process), and features dynamic parameters never before available from a truly differential device.

With a 600V/ μs slew rate and a 600MHz gain-bandwidth-product, the HA-2539 is ideally suited for use in video and RF amplifier designs. Full $\pm$ 10V output swing coupled with outstanding A.C. parameters and complemented by high open loop gain makes these devices useful in high speed data acquisition systems.

The HA-2539 is available in the 14 pin CERDIP. The HA-2539-2 denotes -55°C to +125°C operation while the HA-2539-5 operates over the 0°C to +75°C range.

PINOUT

TOP VIEW



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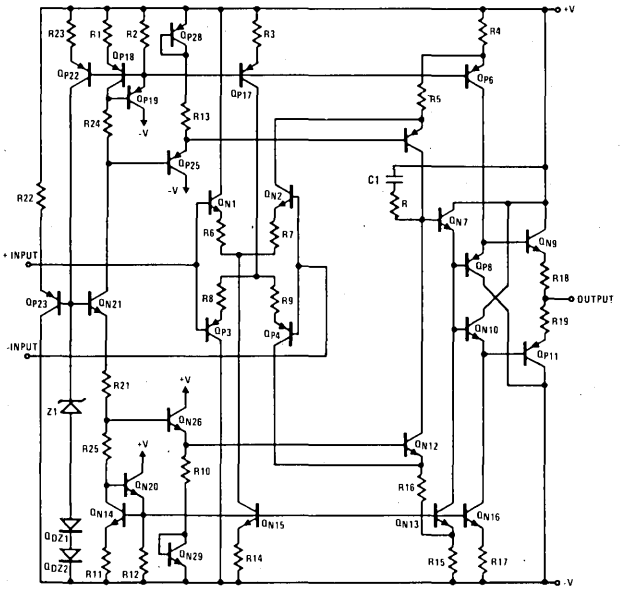


See Pages 3287-3291 for Package Information.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage between V+ and V- Terminals	35V
Differential Input Voltage	6V
Output Current	50mA (Peak)
Internal Power Dissipation (Note 2)	870mW (Cerdip)
Operating Temperature Range: (HA-2539-2)	$-55^oC \leq T_A \leq +125^oC$
(HA-2539-5)	$0^oC \leq T_A \leq +75^oC$
Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS $V_{SUPPLY} = \pm 15$ Volts; R_L = 1K ohms, unless otherwise specified.

		HA-2539-2 -55°C to +125°C			HA-2539-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		3	5		3	15	mV
	FULL			10			20	mV
Average Offset Voltage Drift	FULL		20			20		µV/°C
Bias Current	+25°C		5	20		5	20	µA
	FULL			25			25	µA
Offset Current	+25°C		1	6		1	6	µA
	FULL			8			8	µA
Input Resistance	+25°C		10			10		Kohms
Input Capacitance	+25°C		1.0			1.0		pF
Common Mode Range	FULL	±10			±10			V
Input Voltage Noise (f = 1kHz, $R_g = 0\Omega$)	+25°C		15			15		$nV/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 3)	+25°C	15K	30K		10K	30K		V/V
	FULL	5K			5K			V/V
Common-Mode Rejection Ratio (Note 4)	FULL	60			60			dB
Gain-Bandwidth-Product (Notes 5 & 6)	+25°C		600			600		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 3)	FULL	±10			±10			V
Output Current (Note 3)	+25°C	10			10			mA
Output Resistance	+25°C		30			30		Ohms
Full Power Bandwidth (Note 3 & 7)	+25°C	8.7	9.5		8.7	9.5		MHz
TRANSIENT RESPONSE (Note 8)								
Rise Time	+25°C		7			7		ns
Overshoot	+25°C		15			8		%
Slew Rate	+25°C	550	600		550	600		V/µs
Settling Time: 10V Step to 0.1%	+25°C		350			350		ns
POWER REQUIREMENTS								
Supply Current	FULL		20	25		20	25	mA
Power Supply Rejection Ratio (Note 9)	FULL	60			60			dB

HARRIS

HA-2540

Wideband, Fast Settling Operational Amplifiers

Preliminary

FEATURES

- VERY HIGH SLEW RATE — 400V/μs
- FAST SETTLING TIME — 250ns
- WIDE GAIN-BANDWIDTH — 400MHz
- POWER BANDWIDTH — 6MHz
- LOW OFFSET VOLTAGE — 5mV
- INPUT VOLTAGE NOISE — 15nV/$\sqrt{Hz}$
- OUTPUT VOLTAGE SWING — $\pm$10V
- MONOLITHIC BIPOLAR CONSTRUCTION

APPLICATIONS

- PULSE AND VIDEO AMPLIFIERS
- WIDEBAND AMPLIFIERS
- HIGH SPEED SAMPLE-HOLD CIRCUITS
- FAST, PRECISE D/A CONVERTERS

GENERAL DESCRIPTION

The Harris HA-2540 is a wideband, very high slew rate, monolithic operational amplifier featuring superior speed and bandwidth characteristics. Bipolar construction coupled with dielectric isolation allows this truly differential device to deliver outstanding performance. Additionally, the HA-2540 has a drive capability of $\pm$10V into a 1K ohm load. Other desirable characteristics include low input voltage noise, low offset voltage, and fast settling time.

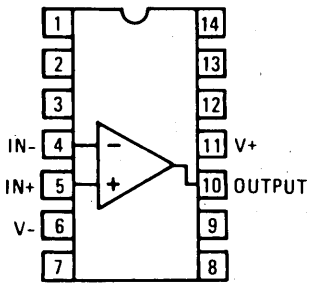
A 400V/μs slew rate ensures high performance in video and pulse amplification circuits, while the 400MHz gain-bandwidth-product is ideally suited for wideband signal amplification. A settling time of 250ns also makes the HA-2540 an excellent selection for high speed Data Acquisition Systems.

The HA-2540-2 is specified over the -55°C to +125°C range while the HA-2540-5 is specified from 0°C to +75°C.

PINOUT

Section 11 for Packaging

TOP VIEW



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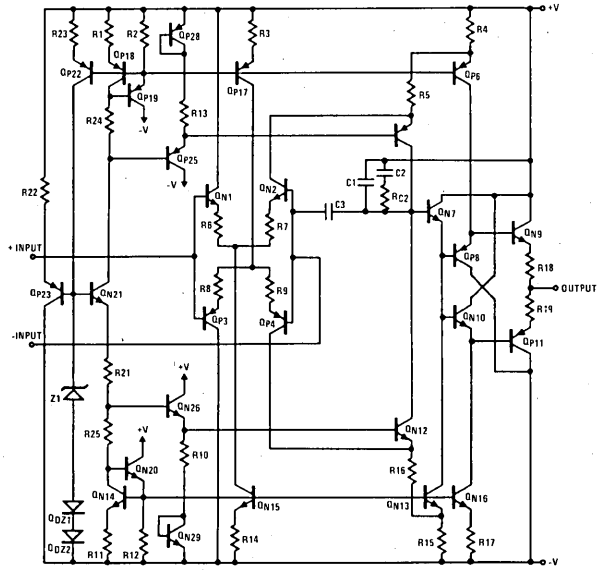


See Pages 3287-3291 for Package Information.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage between V+ and V- Terminals	35V
Differential Input Voltage	6V
Output Current	50mA (Peak)
Internal Power Dissipation (Note 2)	870mW (Cerdip)
Operating Temperature Range: (HA-2540-2)	$-55^{o}C \leq T_A \leq +125^{o}C$
(HA-2540-5)	$0^{o}C \leq T_A \leq +75^{o}C$
Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS $V_{SUPPLY} = \pm 15$ Volts; $R_L = 1K$ ohms, unless otherwise specified.

		HA-2540-2 -55°C to +125°C			HA-2540-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		3	5		3	15	mV
	FULL			10			20	mV
Average Offset Voltage Drift	FULL		20			20		µV/°C
Bias Current	+25°C		5	20		5	20	µA
	FULL			25			25	µA
Offset Current	+25°C		1	6		1	6	µA
	FULL			8			8	µA
Input Resistance	+25°C		10			10		Kohms
Input Capacitance	+25°C		1.0			1.0		pF
Common Mode Range	FULL	±10			±10			V
Input Noise Voltage (f = 1kHz, $R_g = 0\Omega$)	+25°C		15			15		$nV/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 3)	+25°C	15K	30K		10K	30K		V/V
	FULL	5K			5K			V/V
Common-Mode Rejection Ratio (Note 4)	FULL	60			60			dB
Gain-Bandwidth-Product (Notes 5 & 6)	+25°C		400			400		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 3)	FULL	±10			±10			V
Output Current (Note 3)	+25°C	10			10			mA
Output Resistance	+25°C		30			30		Ohms
Full Power Bandwidth (Note 3 & 7)	+25°C	5.5	6		5.5	6		MHz
TRANSIENT RESPONSE (Note 8)								
Rise Time	+25°C		14			14		ns
Overshoot	+25°C		5			5		%
Slew Rate	+25°C	350	400		350	400		V/µs
Settling Time: 10V Step to 0.1%	+25°C		250			250		ns
POWER REQUIREMENTS								
Supply Current	FULL		20	25		20	25	mA
Power Supply Rejection Ratio (Note 9)	FULL	60			60			dB

HARRIS HA-2600/2602/2605

WideBand, High Impedance Operational Amplifiers

FEATURES

- WIDE BANDWIDTH 12MHz
- HIGH INPUT IMPEDANCE 500MΩ
- LOW INPUT BIAS CURRENT 1nA
- LOW INPUT OFFSET CURRENT 1nA
- LOW INPUT OFFSET VOLTAGE 0.5mV
- HIGH GAIN 150K V/V
- HIGH SLEW RATE 7V/μs
- OUTPUT SHORT CIRCUIT PROTECTION

APPLICATIONS

- VIDEO AMPLIFIER
- PULSE AMPLIFIER
- AUDIO AMPLIFIERS AND FILTERS
- HIGH-Q ACTIVE FILTERS
- HIGH-SPEED COMPARATORS
- LOW DISTORTION OSCILLATORS

DESCRIPTION

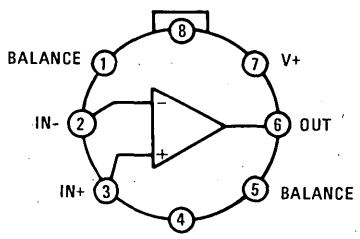
HA-2600/2602/2605 are internally compensated bipolar operational amplifiers that feature very high input impedance (500 MΩ, HA-2600) coupled with wideband AC performance. The high resistance of the input stage is complemented by low offset voltage (0.5mV, HA-2600) and low bias and offset current (1nA, HA-2600) to facilitate accurate signal processing. Input offset can be reduced further by means of an external nulling potentiometer. 12MHz unity gain-bandwidth product, 7V/μs slew rate and 150,000V/V open-loop gain enables HA-2600/2602/2605 to perform high-gain amplification of fast, wideband signals. These dynamic characterisitics, coupled with fast settling times, make these amplifiers ideally suited to pulse amplification designs as well as high frequency (e.g. video) applications. The frequency response of the amplifier can be tailored to exact design requirements by means of an external bandwidth control capacitor.

In addition to its application in pulse and video amplifier designs, HA-2600/2602/2605 is particularly suited to other high performance designs such as high-gain low distortion audio amplifiers, high-Q and wideband active filters and high-speed comparators.

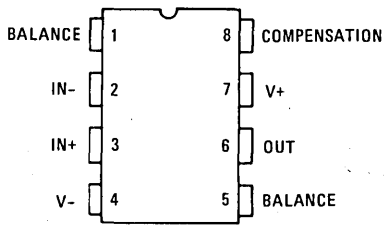
HA-2600 and HA-2602 are guaranteed over -55°C to +125°C. HA-2605 is specified from 0°C to +75°C. All devices are available in TO-99 cans, and HA-2600/2602 are available in 10 lead flat packages.

PINOUT

Section 11 for Packaging



Case Connected to V- TOP VIEWS



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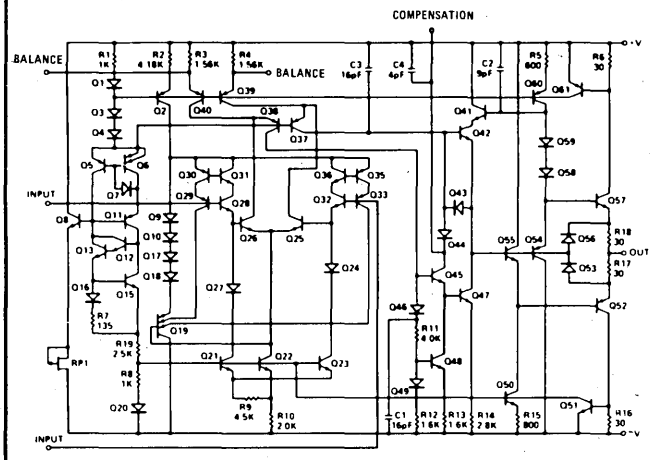


See Pages 3287-3291 for Package Information.

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	45.0V
Differential Input Voltage	±12.0V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation	300mW
Operating Temperature Range – HA-2600/HA-2602	$-55^oC \leq T_A \leq +125^oC$
HA-2605	$0^o \leq T_A \leq +75^oC$
Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS V+ = +15VDC, V- = -15VDC

		HA-2600 −55°C to +125°C			HA-2602 −55°C to +125°C			HA-2605 0°C to +75°C			
		LIMITS			LIMITS			LIMITS			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		0.5	4		3	5		3	5	mV
	Full		2	6			7			7	mV
Offset Voltage Average Drift	Full		5								µV/°C
Bias Current	+25°C		1	10		15	25		5	25	nA
	Full		10	30			60			40	nA
Offset Current	+25°C		1	10		5	25		5	25	nA
	Full		5	30			60			40	nA
Input Resistance (Note 10)	+25°C	100	500		40	300		40	300		MΩ
Common Mode Range	Full	±11.0			±11.0			±11.0			V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Notes 1, 4)	+25°C	100K	150K		80K	150K		80K	150K		V/V
	Full	70K			60K			70K			V/V
Common Mode Rejection Ratio (Note 2)	Full	80	100		74	100		74	100		dB
Unity Gain Bandwidth (Note 3)	+25°C		12			12			12		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
Output Current (Note 4)	+25°C	±15	±22		±10	±18		±10	±18		mA
Full Power Bandwidth (Note 4 &11)	+25°C	50	75		50	75		50	75		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		30	60		30	60		30	60	ns
Overshoot (Notes 1, 5, 7 & 8)	+25°C		25	40		25	40		25	40	%
Slew Rate (Notes 1, 5, 8 & 12)	+25°C	±4	±7		±4	±7		±4	±7		V/µs
Settling Time (Notes 1, 5, 8 & 12)	+25°C		1.5			1.5			1.5		µs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C		3.0	3.7		3.0	4.0		3.0	4.0	mA
Power Supply Rejection Ratio (Note 9)	Full	80	90		74	90		74	90		dB

TEST CONDITIONS

NOTES:
1. R_L = 2K
2. V_{CM} = ± 10V
3. V_O < 90mV
4. V_O = ± 10V
5. C_L = 100pF
6. V_O = ± 200mV
7. V_O = ± 200mV
8. See Transient response test circuits and waveforms
9. ΔVS = ±5V
10. This parameter value guaranteed by design calculations.
11. Full power bandwidth guaranteed by slew rate measurement. FPBW = S.R./2π V_{peak}.
12. V_{OUT} = ± 5V

HARRIS HA-2620/2622/2625

Very Wide Band, Uncompensated Operational Amplifiers

FEATURES

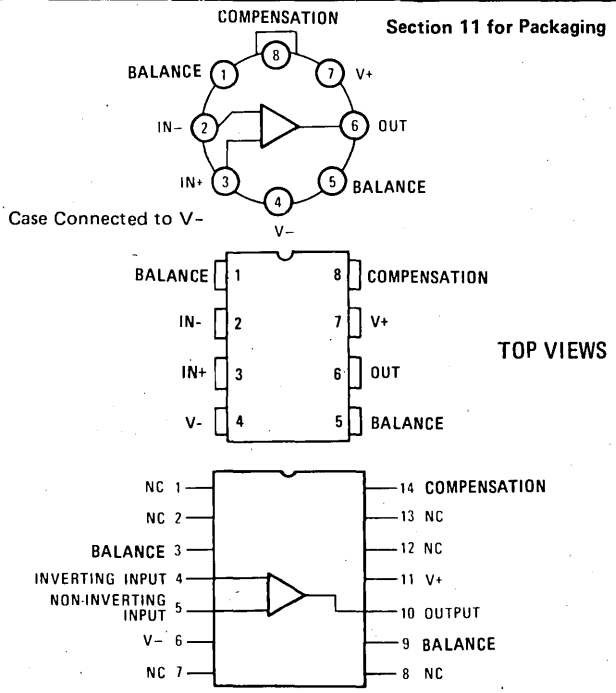
- GAIN BANDWIDTH PRODUCT(A_V = 5) 100MHz
- HIGH INPUT IMPEDANCE 500MΩ
- LOW INPUT BIAS CURRENT 1nA
- LOW INPUT OFFSET CURRENT 1nA
- LOW INPUT OFFSET VOLTAGE 0.5mV
- HIGH GAIN 150K V/V
- HIGH SLEW RATE 35V/μs
- OUTPUT SHORT CIRCUIT PROTECTION

APPLICATIONS

- VIDEO AND R.F. AMPLIFIERS
- PULSE AMPLIFIER
- AUDIO AMPLIFIERS AND FILTERS
- HIGH-Q ACTIVE FILTERS
- HIGH-SPEED COMPARATORS
- LOW DISTORTION OSCILLATORS

PINOUT

Section 11 for Packaging



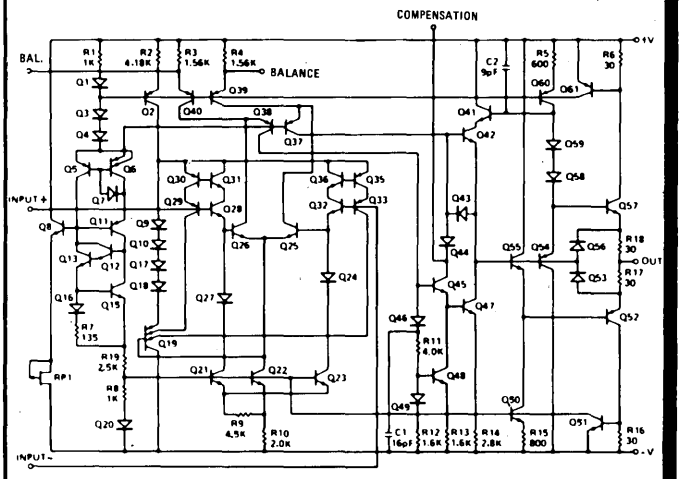
DESCRIPTION

HA-2620/2622/2625 are bipolar operational amplifiers that feature very high input impedance (500MΩ, HA-2620) coupled with wideband AC performance. The high resistance of the input stage is complemented by low offset voltage (0.5mV, HA-2620) and low bias and offset current (1nA, HA-2620) to facilitate accurate signal processing. Input offset can be reduced further by means of an external nulling potentiometer. 100MHz gain-bandwidth product (HA-2620/2622/2625 are stable for closed loop gains greater than 5), 35V/ μs slew rate and 150,000V/V open-loop gain enables HA-2620/2622/2625 to perform high-gain amplification of very fast, wideband signals. These dynamic characterisitcs, coupled with fast settling times, make these amplifiers ideally suited to pulse amplification designs as well as high frequency (e.g. video) applications. The frequency response of the amplifier can be tailored to exact design requirements by means of an external bandwidth control capacitor.

In addition to its application in pulse and video amplifier designs HA-2620/2622/2625 is particularly suited to other high performance designs such as high-gain low distortion audio amplifiers, high-Q and wideband active filters and high-speed comparators.

HA-2620 and HA-2622 are guaranteed over -55°C to +125°C. HA-2625 is specified from 0°C to +75°C. All devices are available in TO-99 cans, and 14 lead D.I.P. packages.

SCHEMATIC



See Pages 3287-3291 for Package Information.

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	45.0V
Differential Input Voltage	±12.0V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation	300mW
Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS

$V^+ = +15$ VDC, $V^- = -15$ VDC

PARAMETER	TEMPERATURE	HA-2620 −55°C to +125°C MIN.	HA-2620 TYP.	HA-2620 MAX.	HA-2622 −55°C to +125°C MIN.	HA-2622 TYP.	HA-2622 MAX.	HA-2625 0°C to +75°C MIN.	HA-2625 TYP.	HA-2625 MAX.	UNITS
INPUT CHARACTERISTICS											
Offset Voltage (Note 1)	+25°C		0.5	4		3	5		3	5	mV
	Full			6			7			7	mV
Bias Current	+25°C		1	15		5	25		5	25	nA
	Full		10	35			60			40	nA
Offset Current	+25°C		1	15		5	25		5	25	nA
	Full		5	35			60			40	nA
Input Resistance (Note 11)	+25°C	65	500		40	300		40	300		MΩ
Common Mode Range	Full	±11.0			±11.0			±11.0			V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Notes 2 & 3)	+25°C	100K	150K		80K	150K		80K	150K		V/V
	Full	70K			60K			70K			V/V
Common Mode Rejection Ratio (Note 4)	Full	80	100		74	100		74	100		dB
Gain Bandwidth Product (Notes 2, 5, &6)	+25°C		100			100			100		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 2)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
Output Current (Note 3)	+25°C	±15	±22		±10	±18		±10	±18		mA
Full Power Bandwidth (Notes 2, 3, 7 &12)	+25°C	400	600		320	600		320	600		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 2, 7 & 8)	+25°C		17	45		17	45		17	45	ns
Slew Rate (Notes 2, 7, 8 & 10)	+25°C	±25	±35		± 20	±35		± 20	±35		V/μs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C		3.0	3.7		3.0	4.0		3.0	4.0	mA
Power Supply Rejection Ratio (Note 9)	Full	80	90		74	90		74	90		dB

NOTES:
1. Offset may be externally adjusted to zero.
2. $R_L = 2K\Omega$, $C_L = 50pF$
3. $V_O = \pm 10.0V$
4. $V_{CM} = \pm 10V$
5. $V_O < 90mV$
6. 40dB Gain
7. See transient response test circuits and waveforms
8. $A_V = 5$ (The HA-2620 family is not stable at unity gain without external compensation.)
9. $\Delta V_{Sup} = \pm 5V$
10. $V_{OUT} = \pm 5V$.
11. This parameter value based upon design calculations.
12. Full power bandwidth guaranteed based upon slew rate measurement $FPBW = S.R./2\pi V_{peak}$.

HA-2630/2635

High Performance Current Booster

FEATURES

- OUTPUT CURRENT ±400mA
- SLEW RATE 500V/μs
- BANDWIDTH 8MHz
- FULL POWER BANDWIDTH 8MHz
- INPUT RESISTANCE $2.0 \times 10^6 \Omega$
- OUTPUT RESISTANCE 2.0Ω
- POWER SUPPLY RANGE ±5V to ±20V
- PACKAGE IS ELECTRICALLY ISOLATED

APPLICATIONS

- COAXIAL CABLE DRIVERS
- AUDIO OUTPUT AMPLIFIERS
- SERVO MOTOR DRIVERS
- POWER SUPPLIES (BIPOLAR)
- PRECISION DATA RECORDING

DESCRIPTION

HA-2630 and HA-2635 are monolithic, unity voltage gain current amplifiers delivering extremely high slew rate, wide bandwidth, and full power bandwidth even under heavy output loading conditions. This dielectrically isolated current booster also offers high input impedance and low output resistance. These devices are intended to be used in series with an operational amplifier and inside the feedback loop whenever additional output current is required. Output current levels are programmable by selecting two optional external resistors.

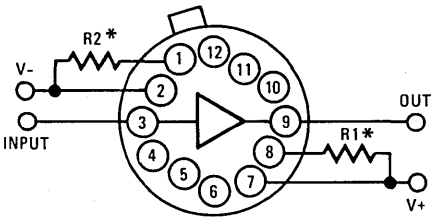
These current amplifiers offer an exceptional 500V/μs slew rate and 8MHz bandwidth which allows them to be used with many high performance op amps in precision data recording and high speed coaxial cable driver designs. 2.0M ohm input resistance and 2 ohm output resistance coupled with ±400mA output current make HA-2630 and HA-2635 ideal components in high fidelity audio output amplifier designs.

HA-2630 and HA-2635 are available in an electrically isolated TO-8 type can for ease of mounting with or without a heat sink. HA-2630 is specified over the -55°C to +125°C range. HA-2635 is specified from 0°C to +75°C.

PINOUT

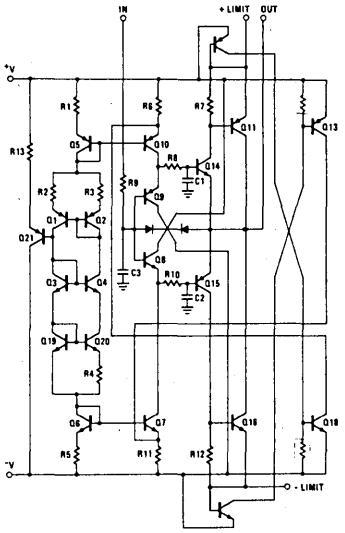
Section 11 for Packaging

TOP VIEW



* Optional Current Limiting Resistor

SCHEMATIC



See Pages 3287-3291 for Package Information.

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	40V
Input Voltage Range	± V Supply
Output Current (Note 2)	±700mA
Internal Power Dissipation (Note 6) Free Air:	1W
In Heat Sink:	4W

Operating Temperature Range:
$-55^{o}C \leq T_A \leq +125^{o}C$ (HA-2630)
$0^{o}C \leq T_A \leq +75^{o}C$ (HA-2635)
Storage Temperature Range:
$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS

$V_{Supply} = \pm 15$ Volts $R_L = 50$ Ohms $R_1 = R_2 = 0$ Ohms Unless otherwise specified.

PARAMETER	TEMP.	HA-2630 -55°C to +125°C MIN.	HA-2630 TYP.	HA-2630 MAX.	HA-2635 0°C to +75°C MIN.	HA-2635 TYP.	HA-2635 MAX.	UNITS
INPUT CHARACTERISTICS								
Bias Current	+25°C		30	150		30	150	µA
	Full			200			200	µA
Input Resistance	+25°C		2.0			2.0		MΩ
Input Capacitance	+25°C		5.0			5.0		pF
TRANSFER CHARACTERISTICS								
Voltage Gain (Note 1)	Full	.85	.95		.85	.95		V/V
Offset Voltage ($V_{OUT} - V_{IN}$)	+25°C		70	±200		70	±200	mV
	Full			±300			±300	mV
Bandwidth (-3dB)	+25°C		8.0			8.0		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing	Full	±10	±12		±10	±12		V
Output Current (Note 1)	Full	±300	±400		±300	±400		mA
Output Resistance	+25°C		2.0			2.0		Ω
Full Power Bandwidth (Note 1)	+25°C		8.0			8.0		MHz
TRANSIENT RESPONSE								
Rise Time (Note 3)	+25°C		30			30		ns
Slew Rate (Note 4)	+25°C	200	500		200	500		V/µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full		15	20		15	23	mA
Supply Voltage Range	Full	±5		±20	±5		±20	V
Power Supply Rejection Ratio (Note 5)	Full		66			66		dB

NOTES:
1. $V_O = \pm 10V$
2. Heat sink is required for continuous short circuit protection, regardless of current limit setting.
3. $V_O = 0.4V$ p-p.
4. $V_O = 10V$ p-p.
5. $\Delta V_{SUPPLY} = \pm 5V$.
6. Without heat sink, derate by 14mW/°C ambient temperature above 100°C ambient, with heat sink, derate by 67mW/°C case temperature above 115°C case.

HARRIS

HA-2640/2645

High Voltage Operational Amplifier

FEATURES

- OUTPUT VOLTAGE SWING ±35V
- SUPPLY VOLTAGE ±10V TO ±40V
- OFFSET CURRENT 5nA
- BANDWIDTH 4MHz
- SLEW RATE 5V/μs
- COMMON MODE INPUT VOLTAGE SWING ±35V
- OUTPUT OVERLOAD PROTECTION

APPLICATIONS

- INDUSTRIAL CONTROL SYSTEMS
- POWER SUPPLIES
- HIGH VOLTAGE REGULATORS
- RESOLVER EXCITATION
- SIGNAL CONDITIONING

DESCRIPTION

HA-2640 and HA-2645 are monolithic operational amplifiers which are designed to deliver unprecedented dynamic specifications for a high voltage internally compensated device. These dielectrically isolated devices offer very low values for offset voltage and offset current coupled with large output voltage swing and common mode input voltage.

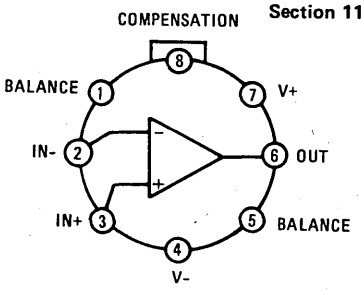
For maximum reliability, these amplifiers offer unconditional output overload protection through current limiting and a chip temperature sensing circuit. This sensing device turns the amplifier "off", when the chip reaches a certain temperature level.

These amplifers deliver ±35V common mode input voltage swing, ±35V output voltage swing, and up to ±40V supply range for use in such designs as regulators, power supplies, and industrial control systems. 4MHz gain bandwidth and 5V/μs slew rate make these devices excellent components for high performance signal conditioning applications. Outstanding input and output voltage swings coupled with a low 5nA offset current make these amplifiers excellent components for resolver excitation designs.

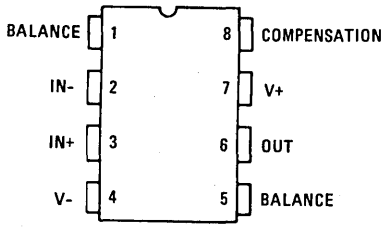
HA-2640 and HA-2645 are available in metal can (TO-99) packages and can be used as high performance pin-to-pin replacements for many general purpose op amps. HA-2640 is specified from -55°C to +125°C and HA-2645 is specified over the 0°C to +75°C range.

PINOUT

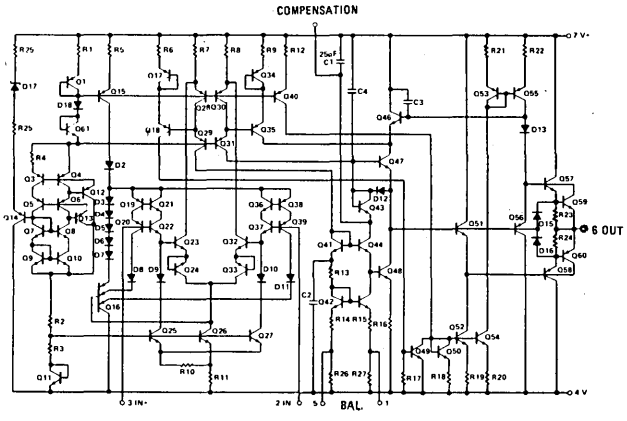
Section 11 for Packaging



TOP VIEWS



SCHEMATIC



See Pages 3287-3291 for Package Information.

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals 100V
Input Voltage Range ±37V
Output Current/Full Short Circuit Protection
Internal Power Dissipation 680mW*

*Derate by 4.6mW/°C above +25°C

Operating Temperature Range
$-55^{\circ}C \leq T_A \leq +125^{\circ}C$ (HA-2640)
$0^{\circ}C \leq T_A \leq +75^{\circ}C$ (HA-2645)
Storage Temperature Range
$-65^{\circ}C \leq T_A \leq +150^{\circ}C$

ELECTRICAL CHARACTERISTICS

$V_{Supply} = \pm 40V$, $R_L = 5K$, Unless Otherwise Specified.

PARAMETER	TEMP.	HA-2640 -55°C to +125°C MIN.	HA-2640 -55°C to +125°C TYP.	HA-2640 -55°C to +125°C MAX.	HA-2645 0°C to +75°C MIN.	HA-2645 0°C to +75°C TYP.	HA-2645 0°C to +75°C MAX.	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		2	4		2	6	mV
	Full			6			7	mV
Offset Voltage Average Drift	Full		15			15		µV/°C
Bias Current	+25°C		10	25		12	30	nA
	Full			50			50	nA
Offset Current	+25°C		5	12		15	30	nA
	Full			35			50	nA
Input Resistance (Note 10)	+25°C	50	250		40	200		MΩ
Common Mode Range	Full	±35			±35			V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 8)	+25°C	100K	200K		100K	200K		V/V
	Full	75K			75K			V/V
Common Mode Rejection Ratio (Note 1)	Full	80	100		74	100		dB
Unity Gain Bandwidth (Note 2)	+25°C		4			4		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing	Full	±35			±35			V
Output Current (Note 9)	+25°C	±12	±15		±10	±12		mA
Output Resistance	+25°C		500			500		Ω
Full Power Bandwidth (Notes 3 &11)	+25°C		23			23		kHz
TRANSIENT RESPONSE (Note 7)								
Rise Time (Notes 4, 6)	+25°C		60	100		60	100	ns
Overshoot (Notes 4, 6)	+25°C		15	30		15	40	%
Slew Rate (Note 6)	+25°C	±3	±5		±2.5	±5		V/µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		3.2	3.8		3.2	4.5	mA
Supply Voltage Range	Full	±10		±40	±10		±40	V
Power Supply Rejection Ratio (Note 5)	Full	80	90		74	90		dB

NOTES:
1. $V_{CM} = \pm 20V$
2. $V_O = 90mV$
3. $V_O = \pm 35V$
4. $V_O = \pm 200mV$
5. $V_S = \pm 10V$ to $\pm 40V$
6. $A_V = 1$
7. $C_L = 50pF$
8. $V_O = \pm 30V$
9. $R_L = 1K$
10. This parameter based upon design calculations.
11. Full power bandwidth guaranteed based upon slew rate measurement. $FPBW = S.R./2\pi V_{peak}$.

HA-2650/2655

Dual High Performance Operational Amplifier

FEATURES

- SLEW RATE — 5V/μs
- BANDWIDTH — 8MHz
- BIAS CURRENT — 35nA
- AV. OFFSET VOLTAGE DRIFT — 8μV/°C
- POWER CONSUMPTION — 75mW
- SUPPLY VOLTAGE RANGE — ±2V TO ±20V

APPLICATIONS

- VIDEO AMPLIFIERS
- HIGH IMPEDANCE, WIDEBAND BUFFERS
- INTEGRATORS
- AUDIO AMPLIFIERS
- ACTIVE FILTERS

DESCRIPTION

HA-2650/2655 contains two internally compensated operational amplifiers offering high slew rate and high frequency performance combined with exceptional DC characteristics. 5V/μ sec slew rate and 8MHz bandwidth make these amplifiers suitable for processing fast, wideband signals extending into the video frequency spectrum. Signal processing accuracy is enhanced by front-end performance that includes 1.5mV offset voltage, 8 μ V/°C offset voltage drift and low offset and bias current (1nA and 35nA respectively). Offset voltage can be trimmed to zero on the devices offered in dual-in-line packages. Signal conditioning is further enhanced by 500MΩ input impedance.

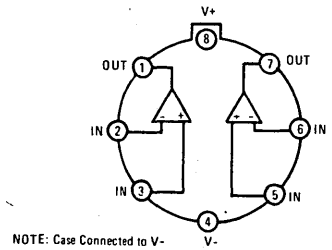
Applications for HA-2650/2655 include video circuit designs such as high impedance buffers, integrators, tone generators and filters. These amplifiers are also ideal components for active filtering of audio and voice signals.

HA-2650/2655 are offered in 14 pin D.I.P. and metal TO-99 packages and are also available in dice form. HA-2650 is specified from -55°C to +125°C. HA-2655 operates from 0°C to +75°C.

PINOUT

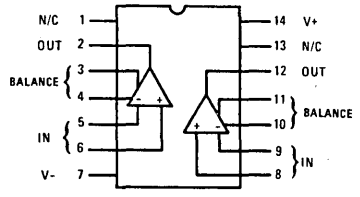
TOP VIEW

Section 11 for Packaging



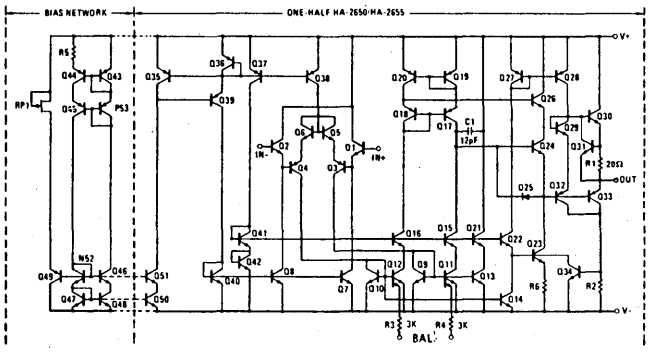
NOTE: Case Connected to V-

TOP VIEW



NOTE: Bottom of package is connected to V-.

SCHEMATIC



See Pages 3287-3291 for Package Information.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

T_A = +25°C Unless Otherwise Stated

Voltage Between V+ and V- Terminals	40.0V
Differential Input Voltage	±30.0V
Input Voltage (Note 1)	±15.0V
Output Short Circuit Duration	Indefinite

Power Dissipation (Note 2)	TO-99	300 mW
	TO-116	300 mW
Operating Temperature Range:		
HA-2650	-55°C ≤ T_A ≤ +125°C	
HA-2655	0°C ≤ T_A ≤ +75°C	
Storage Temperature Range	-65°C ≤ T_A ≤ +150°C	

ELECTRICAL CHARACTERISTICS

V+ = 15V V- = -15V

PARAMETER	TEMP.	HA-2650 -55°C to +125°C MIN.	HA-2650 TYP.	HA-2650 MAX.	HA-2655 0°C to +75°C MIN.	HA-2655 TYP.	HA-2655 MAX.	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		1.5	3		2	5	mV
	Full			5			7	mV
Av. Offset Voltage Drift	Full		8			8		µV/°C
Bias Current	+25°C		35	100		50	200	nA
	Full			200			300	nA
Offset Current	+25°C		1	30		2	60	nA
	Full			60			100	nA
Common Mode Range	Full	±13			±13			V
Differential Input Resistance (Note 9)	+25°C	5	20		5	20		MΩ
Common Mode Input Resistance	+25°C		500			500		MΩ
Input Capacitance	+25°C		5			5		pF
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 3ab)	+25°C	20K	40K		15K	40K		V/V
	Full	15K			10K			V/V
Common Mode Rejection Ratio (Note 4)	+25°C	80	100		74	100		dB
	Full	80			74			dB
OUTPUT CHARACTERISTICS								
*Output Voltage Swing (Note 3c)	+25°C	±13	±14		±13	±14		V
	Full	±13			±13			V
Full Power Bandwidth (Notes 5 & 10)	+25°C	30	80		30	80		KHz
Output Current (Note 3a)	+25°C		±20			±18		mA
Output Resistance	+25°C		100			100		Ω
TRANSIENT RESPONSE (Note 6)								
Rise Time (Note 7)	+25°C		40	80		40	90	ns
Overshoot (Note 7)	+25°C		15	30		15	40	%
Slew Rate	+25°C	±2	±5		±2	±5		V/µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		2.5	4		3	5	mA
Power Supply Rejection Ratio (Note 8)	+25°C	80	100		74	100		dB
	Full	80			74			dB

NOTES:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Derate at 4.7mW/°C at ambient temperatures above +110°C.
3. (a) V_O = ±10V (b) R_L = 2K (c) R_L = 10K
4. V_{CM} = ±5.0V
5. A_V = 1, R_L = 2K, V_O = 20V_{pp}
6. See transient response/slew rate circuit.
7. V_{in} = 200mV
8. Δ V = ±5.0V
9. This parameter value based upon design calculations.
10. Full power bandwidth guaranteed based upon slew rate measurement FPBW = S.R./2πV_{peak}.

HARRIS

HA-2720/25

Wide Range Programmable Operational Amplifier

FEATURES

- WIDE PROGRAMMING RANGE

SLEW RATE	0.06 TO 6V/μs
BANDWIDTH	5kHz TO 10MHz
BIAS CURRENT	0.4 TO 50nA
SUPPLY CURRENT	1μA TO 1.5mA

- WIDE POWER SUPPLY RANGE ±1.2 TO ±18V
- CONSTANT AC PERFORMANCE OVER SUPPLY RANGE

APPLICATIONS

- ACTIVE FILTERS
- CURRENT CONTROLLED OSCILLATORS
- VARIABLE ACTIVE FILTERS
- MODULATORS
- BATTERY-POWERED EQUIPMENT

DESCRIPTION

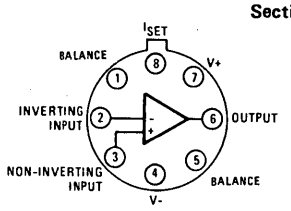
HA-2720/2725 programmable amplifiers are internally compensated monolithic devices offering a wide range of performance, that can be controlled by adjusting the circuits' "set" current (I_{SET}). By means of adjusting an external resistor or current source, power dissipation, slew rate, bandwidth, output current and input noise can be programmed to desired levels. This versatile adjustment capability enables HA-2720/2725 to provide optimum design solutions by delivering the required level of performance with minimum possible power dissipation. HA-2720 and HA-2725 can, therefore, be utilized as the standard amplifier for a variety of designs simply by adjusting their programming current.

A major advantage of HA-2720/2725 is that operating characteristics remain virtually constant over a wide supply range (±1.2V to ±15V), allowing the amplifiers to offer maximum performance in almost any system including battery-operated equipment. A primary application for HA-2720/2725 is in active filters for a wide variety of signals that differ in frequency and amplitude. Also, by modulating the "set" current, HA-2720/2725 can be used for designs such as current controlled oscillators modulators, sample and hold circuits and variable active filters.

HA-2720 is guaranteed over -55°C to +125°C. HA-2725 is specified from 0°C to +75°C. Both parts are available in TO-99 cans or dice form.

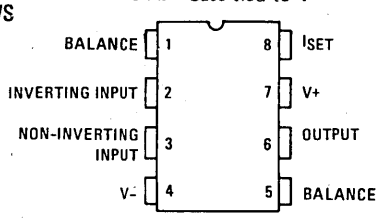
PINOUT

Section 11 for Packaging

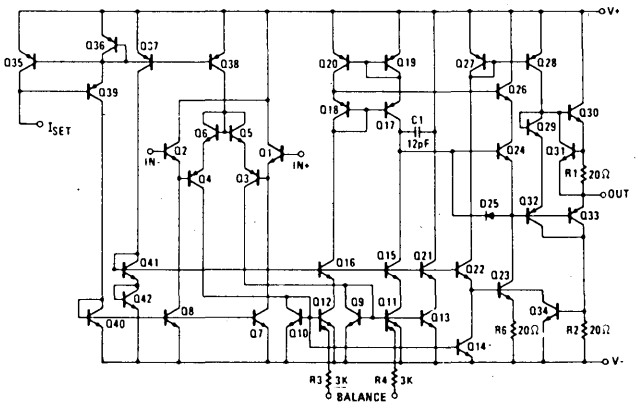


NOTE: Case tied to V⁻

TOP VIEWS



SCHEMATIC



See Pages 3287-3291 for Package Information.

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	45.0V	Power Dissipation (Note 2)	300mW
Differential Input Voltage	±30.0V	Operating Temperature Range:	
Input Voltage (Note 1)	±15.0V	HA-2720	$-55^oC \leq T_A \leq +125^oC$
I_{SET} (Current at I_{SET})	500μA	HA-2725	$0^oC \leq T_A \leq +75^oC$
V_{SET} (Voltage to Gnd. at I_{SET})	$V+ - 2.0V \leq V_{SET} \leq V+$	Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS

V+ = +3.0V, V- = -3.0V

		HA-2720 -55°C to +125°C						HA-2725 0°C to +75°C						
		I_{SET} = 1.5μA			I_{SET} = 15μA			I_{SET} = 1.5μA			I_{SET} = 15μA			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS														
Offset Voltage	25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
Offset Current	25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			20	nA
Bias Current	25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance (Note 10)	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Note 9)	25°C	15K	40K		15K	40K		15K	40K		15K	40K		V/V
	Full	10K			10K			10K			10K			V/V
Common Mode Rejection Ratio (Note 4)	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note 3)	25°C	±2.0	±2.2		±2.0	±2.2		±2.0	±2.2		±2.0	±2.2		V
	Full	±2.0			±1.9			±2.0			±2.0			V
Output Current (Note 5)	25°C		±0.2			±2.0			±0.2			±2.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	25°C		2.8			14			2.8			14		mA
TRANSIENT RESPONSE														
Rise Time (Note 6)	25°C		2.5			0.25			2.5			0.25		μs
Overshoot (Note 6)	25°C		5			10			5			10		%
Slew Rate (Note 7)	25°C		0.07			0.70			0.07			0.70		V/μs
POWER SUPPLY CHARACTERISTICS														
Supply Current	25°C		15			170			15			170		μA
	Full			25			250			25			250	μA
Power Supply Rejection Ratio (Note 8)	Full	100			100			150			150			μV/V

ELECTRICAL CHARACTERISTICS

V+ = +15.0V, V- = -15.0V

PARAMETER	TEMP.	HA-2720 -55°C to +125°C						HA-2725 0°C to +75°C						UNITS
		I_{SET} = 1.5μA			I_{SET} = 15μA			I_{SET} = 1.5μA			I_{SET} = 15μA			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS														
Offset Voltage	25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
Offset Current	25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			20	nA
Bias Current	25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance (Note 10)	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Notes 3 & 9)	25°C	30K	100K		30K	120K		25K	100K		25K	120K		V/V
	Full	20K			20K			20K			20K			V/V
Common Mode Rejection Ratio (Note 4)	25°C		90			90			90			90		dB
	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note 3)	25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
	Full	±10			±10			±10			±10			V
Output Current (Note 5)	25°C		±0.5			±5.0			±0.5			±5.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	25°C		3.7			19			3.7			19		mA
TRANSIENT RESPONSE														
Rise Time (Note 6)	25°C		2.0			0.2			2.0			0.2		μs
Overshoot (Note 6)	25°C		5			15			5			15		%
Slew Rate (Note 7)	25°C		0.1			0.8			0.1			0.8		V/μs
POWER SUPPLY CHARACTERISTICS														
Supply Current	25°C		20			210			20			210		μA
	Full			50			450			50			450	μA
Power Supply Rejection Ratio (Note 8)	Full	100			100			150			150			μV/V

NOTES:
1. For supply voltages less than ±15.0V, the absolute maximum input voltage is equal to supply voltage.
2. Derate at 6.8mW/°C for operation ambient temperatures above 75°C.

	V_{SUPPLY} = ±3.0V	V_{SUPPLY} = ±15.0V	I_{SET} = 1.5μA	I_{SET} = 15μA
3.	T = +25°C and Full	T = +25°C	R_L = 75KΩ	R_L = 5KΩ
	—	T = Full	R_L = 75KΩ	R_L = 75KΩ
4.	V_{CM} = ±1.5V	V_{CM} = ±5.0V		
5.	V_O = ±2.0V	V_O = ±10.0V		
6.	← A_V = +1, V_{IN} = 400mV, R_L = 5K, C_L = 100pF →			
7.	V_O = ±2.0V	V_O = ±10.0V	R_L = 20K	R_L = 5K
8.	ΔV = ±1.5V	ΔV = ±5.0V		
9.	V_O = ±1.0V	V_O = ±10.0V		

10. This parameter based upon design calculations.

HARRIS HA-2730/35

Wide Range Dual Programmable Operational Amplifier

FEATURES

- WIDE PROGRAMMING RANGE

SET CURRENT	0.1 TO 100μA
SLEW RATE	0.06 TO 6V/μs
BANDWIDTH	5kHz TO 10MHz
BIAS CURRENT	0.4 TO 50nA
SUPPLY CURRENT	1μA TO 1.5mA

- WIDE POWER SUPPLY RANGE ±1.2 TO ±18V
- CONSTANT AC PERFORMANCE OVER SUPPLY RANGE

APPLICATIONS

- ACTIVE FILTERS
- CURRENT CONTROLLED OSCILLATORS
- VARIABLE ACTIVE FILTERS
- MODULATORS
- BATTERY-POWERED EQUIPMENT

DESCRIPTION

HA-2730/2735 Dual Programmable Amplifiers are internally compensated monolithic devices offering a wide range of performance, that can be controlled by adjusting the circuits' "set" current (I_{SET}). By means of adjusting an external resistor or current source, power dissipation, slew rate, bandwidth, output current and input noise can be programmed to desired levels. Each amplifier on the chip can be adjusted independently. This versatile adjustment capability enables HA-2730/2735 to provide optimum design solutions by delivering the required level of performance with minimum possible power dissipation. HA-2730/2735 can, therefore, be utilized as the standard amplifier for a variety of designs simply by adjusting their programming current.

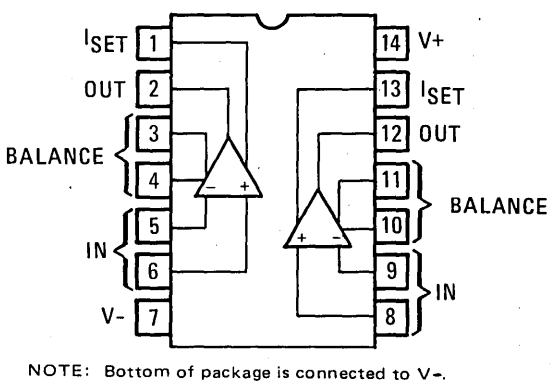
A major advantage of HA-2730/2735 is that operating characteristics remain virtually constant over a wide supply range (±1.2V to ±15V), allowing the amplifiers to offer maximum performance in almost any system including battery-operated equipement. A primary application for HA-2730/2735 is in active filters for a wide variety of signals that differ in frequency and amplitude. Also, by modulating the "set" current, HA-2730/2735 can be used for designs such as current controlled oscillators, modulators, sample and hold circuits and variable active filters.

HA-2730 is guaranteed over -55°C to +125°C. HA-2735 is specified from 0°C to +75°C. Both parts are available in 14 lead D.I.P. package or dice form.

PINOUT

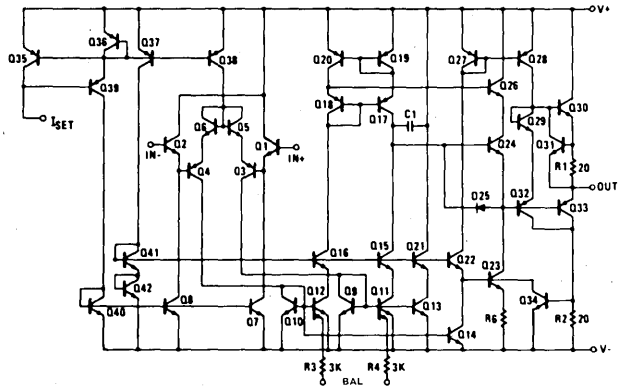
Section 11 for Packaging

TOP VIEW



NOTE: Bottom of package is connected to V-.

SCHEMATIC



(ONE HALF ONLY)
HA-2730/35

See Pages 3287-3291 for Package Information.

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	45.0V	Power Dissipation (Note 2)	500mW
Differential Input Voltage	±30.0V	Operating Temperature Range:	
Input Voltage (Note 1)	±15.0V	HA-2730	$-55^{o}C \leq T_A \leq +125^{o}C$
I_{SET} (Current at I_{SET})	500μA	HA-2735	$0^{o}C \leq T_A \leq +75^{o}C$
V_{SET} (Voltage to Gnd. at I_{SET})	$V+ - 2.0V \leq V_{SET} \leq V+$	Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS (Each Side)

V+ = +3.0V, V- = -3.0V

		HA-2730 -55°C to +125°C						HA-2735 0°C to +75°C						
		I_{SET} = 1.5μA			I_{SET} = 15μA			I_{SET} = 1.5μA			I_{SET} = 15μA			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS														
Offset Voltage	25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
Offset Current	25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			20	nA
Bias Current	25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance (Note 10)	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Notes 3 & 9)	25°C	15K	40K		15K	40K		15K	40K		15K	40K		V/V
	Full	10K			10K			10K			10K			V/V
Common Mode Rejection Ratio (Note 4)	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note 3)	25°C	±2.0	±2.2		±2.0	±2.2		±2.0	±2.2		±2.0	±2.2		V
	Full	±2.0			±1.9			±2.0			±2.0			V
Output Current (Note 5)	25°C		±0.2			±2.0			±0.2			±2.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	25°C		2.8			14			2.8			14		mA
TRANSIENT RESPONSE														
Rise Time (Note 6)	25°C		2.5			0.25			2.5			0.25		μs
Overshoot (Note 6)	25°C		5			10			5			10		%
Slew Rate (Note 7)	25°C		0.07			0.70			0.07			0.70		V/μs
POWER SUPPLY CHARACTERISTICS														
Supply Current (Each Amp)	25°C		15			170			15			170		μA
	Full			25			250			25			250	μA
Power Supply Rejection Ratio (Note 8)	Full	100			100			150			150			μV/V

ELECTRICAL CHARACTERISTICS (Each Side)

V+ = +15.0V, V- = -15.0V

PARAMETER	TEMP.	HA-2730 -55°C to +125°C						HA-2735 0°C to +75°C						UNITS
		I_{SET} = 1.5μA			I_{SET} = 15μA			I_{SET} = 1.5μA			I_{SET} = 15μA			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS														
Offset Voltage	25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
Offset Current	25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			20	nA
Bias Current	25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance (Note 10)	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Notes 3 & 9)	25°C	30K	100K		30K	120K		25K	100K		25K	120K		V/V
	Full	20K			20K			20K			20K			V/V
Common Mode Rejection Ratio (Note 4)	25°C		90			90			90			90		dB
	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note 3)	25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
	Full	±10			±10			±10			±10			V
Output Current (Note 5)	25°C		±0.5			±5.0			±0.5			±5.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	25°C		3.7			19			3.7			19		mA
TRANSIENT RESPONSE														
Rise Time (Note 6)	25°C		2.0			0.2			2.0			0.2		μs
Overshoot (Note 6)	25°C		5			15			5			15		%
Slew Rate (Note 7)	25°C		0.1			0.8			0.1			0.8		V/μs
POWER SUPPLY CHARACTERISTICS														
Supply Current (Each Amp)	25°C		20			210			20			210		μA
	Full			50			450			50			450	μA
Power Supply Rejection Ratio (Note 8)	Full	100			100			150			150			μV/V

NOTES:
1. For supply voltages less than ±15.0V, the absolute maximum input voltage is equal to supply voltage.
2. Derate at 4.7mW/°C at ambient temperat s above 68°C.

	V_{SUPPLY} = ±3.0V	V_{SUPPLY} = ±15.0V	I_{SET} = 1.5μA	I_{SET} = 15μA
3.	T = +25°C and Full	T = +25°C	R_L = 75KΩ	R_L = 5KΩ
	—	T = Full	R_L = 75KΩ	R_L = 75KΩ
4.	V_{CM} = ±1.5V	V_{CM} = ±5.0V		
5.	V_O = ±2.0V	V_O = ±10.0V		
6.	← A_V = +1, V_{IN} = 400mV, R_L = 5K, C_L = 100pF →			
7.	V_O = ±2.0V	V_O = ±10.0V	R_L = 20K	R_L = 5K
8.	ΔV = ±1.5V	ΔV = ±5.0V		
9.	V_O = ±1.0V	V_O = ±10.0V		

10. This parameter value based upon design calculations.

HARRIS

HA-2740

Quad Programmable Operational Amplifier

FEATURES

- WIDE PROGRAMMING RANGE
  - ► SLEW RATE 0.8V/μs
  - ► BANDWIDTH 1MHz
  - ► BIAS CURRENT 8nA
  - ► SUPPLY CURRENT 250μA
- WIDE POWER SUPPLY RANGE
- CONSTANT AC PERFORMANCE OVER SUPPLY RANGE

APPLICATIONS

- ACTIVE FILTERS
- CURRENT CONTROLLED OSCILLATORS
- VARIABLE ACTIVE FILTERS
- MODULATORS
- BATTERY-POWERED EQUIPMENT

DESCRIPTION

The Harris HA-2740 programmable amplifier is an internally compensated monolithic device offering a wide range of performance, that can be controlled by adjusting the circuit "set" current (I_{SET}). By means of adjusting an external resistor or current source, power dissipation, slew rate, bandwidth, output current and input noise can be programmed to desired levels. This versatile adjustment capability enables the HA-2740 to provide optimum design solutions by delivering the required level of performance with minimum possible power dissipation. The HA-2740 can, therefore, be utilized as the standard amplifier for a variety of designs simply by adjusting programming current.

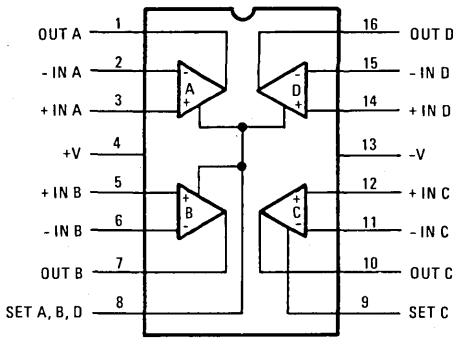
A major advantage of the HA-2740 is that operating characteristics remain virtually constant over a wide supply range ($\pm$1.2V to $\pm$18V), allowing the amplifier to offer maximum performance in almost any system including battery-operated equipment. A primary application for the HA-2740 is in active filters for a wide variety of signals that differ in frequency and amplitude. Also, by modulating the "set" current, the HA-2740 can be used for designs such as current controlled oscillators, modulators, sample and hold circuits and variable active filters.

The HA-2740-2 is guaranteed over -55°C to +125°C. The HA-2740-5 is specified from 0°C to +75°C. Both parts are available in a 16 pin dual-in-line package.

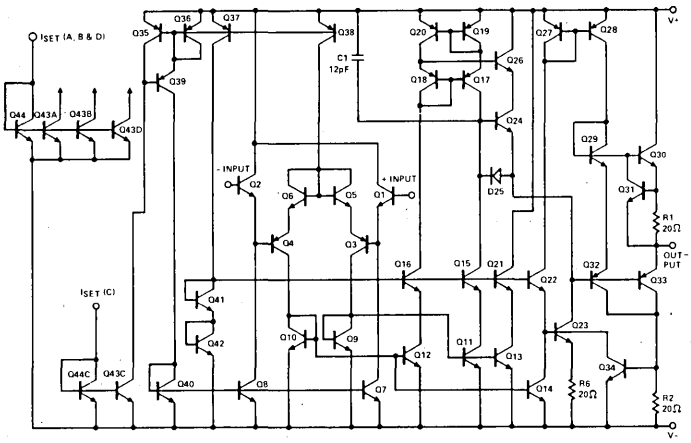
PINOUT

Section 11 for Packaging

TOP VIEW



SCHEMATIC



See Pages 3287-3291 for Package Information.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V- Terminals	45.0V
Differential Input Voltage	±30.0V
Input Voltage (Note 2)	±15.0V
I_{SET} (Current at I_{SET})	500μA
V_{SET} (Voltage to Gnd. at I_{SET})	$V+ - 2.0 \leq V_{SET} \leq V+$
Power Dissipation	300mW
Operating Temperature Range:	
HA-2740-2	$-55^oC \leq T_A \leq +125^oC$
HA-2740-5	$0^oC \leq T_A \leq +75^oC$
Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS V+ = +15.0V, V⁻ = -15.0V

PARAMETER	TEMP	HA-2740-2 -55°C to +125°C						HA-2740-5 0°C to +75°C						UNITS
		I_{SET} = 1.5μA			I_{SET} = 15μA			I_{SET} = 1.5μA			I_{SET} = 15μA			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS														
Offset Voltage	25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
Offset Current	25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			30	nA
Bias Current	25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance (Note 3)	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Note 4)	25°C	30K	100K		30K	120K		25K	100K		25K	120K		V/V
	Full	20K			20K			20K			20K			V/V
Common Mode Rejection Ratio (Note 5)	25°C		100			100			100			100		dB
	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note 6)	25°C	±12	±14		±12	±14		±12	±14		±12	±14		V
	Full	±10			±10			±10			±10			V
Channel Separation (Note 7)	25°C		110			110			110			110		dB
Output Current (Note 8)	25°C		±0.5			±5.0			±0.5			±5.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short Circuit Current	25°C		3.6			16			3.6			16		mA
TRANSIENT RESPONSE														
Rise Time (Note 9)	25°C		2.0			0.2			2.0			0.2		μs
Overshoot (Note 9)	25°C		2			10			2			10		%
Slew Rate (Note 10)	25°C		0.1			0.8			0.1			0.8		V/μs
POWER SUPPLY CHARACTERISTICS														
Supply Current (each amp)	25°C		25			250			25			250		μA
	Full			50			450			50			450	μA
Power Supply Rejection Ratio (Note 11)	Full	100				100		150			150			μV/V

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. This parameter based upon design calculations.
4. $V_O = \pm 10V$, $R_L = 5K$ @ $I_{SET} = 15\mu A$
   $R_L = 75K$ @ $I_{SET} = 1.5\mu A$
5. VCM = ±5V
6. $R_L = 5k\Omega$ @ $I_{SET} = 15\mu A$, $R_L = 75K$ @ $I_{SET} = 1.5\mu A$
7. RS = 1kΩ, f = 100Hz.
8. $V_O = \pm 10V$
9. AV = 1, VIN = 200mV, RL = 5k, CL = 100pF.
10. $V_O = \pm 10V$, $R_L = 5K$ @ $I_{SET} = 15\mu A$,
    $R_L = 20K$ @ $I_{SET} = 1.5\mu A$
11. AV = ±5V.

HARRIS

HA-4156

High Performance Quad Operational Amplifier

FEATURES

- SLEW RATE — 1.6 V/μS (TYP.)
- BANDWIDTH — 3.5 MHz (TYP.)
- INPUT VOLTAGE NOISE (f = 1KHz) — 9 NV/$\sqrt{Hz}$ (TYP.)
- INPUT OFFSET VOLTAGE — 0.5 mV (TYP.)
- INPUT BIAS CURRENT — 60 nA (TYP.)
- SUPPLY RANGE — $\pm$2V to $\pm$20V
- NO CROSSOVER DISTORTION
- STANDARD QUAD PIN-OUT

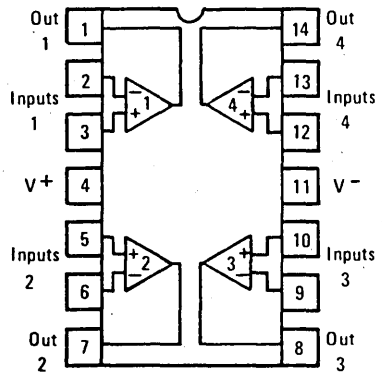
DESCRIPTION

The HA-4156 contains four general purpose operational amplifiers on a monolithic chip. The performance of each amplifier is equal to or better than the 741 type amplifier in all respects. Its superior bandwidth, slew rate and noise characteristics make it an excellent choice for active filter or audio amplifier applications.

The HA-4156-5 is guaranteed over 0°C to +75°C.

PINOUT

PIN OUT Section 11 for Packaging



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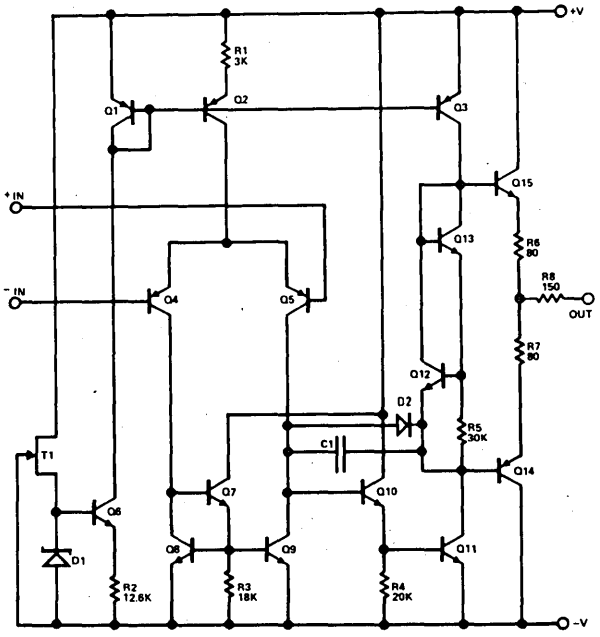


(¼) HA-4156

See Pages 3287-3291 for Package Information.

ABSOLUTE MAXIMUM RATINGS

T_A = +25°C Unless Otherwise Stated

Voltage Between V+ and V- Terminals	40.0V
Differential Input Voltage	±30.0V
Input Voltage (Note 1)	±15.0V
Output Short Circuit Duration (Note 2)	Indefinite
Power Dissipation (Note 3)	880mW
Operating Temperature Range	
HA-4156-5	0°C≤T_A≤+75°C
Storage Temperature Range	-65°C≤T_A≤+150°C

ELECTRICAL CHARACTERISTICS

V+ = 15V, V- = -15V

PARAMETER	TEMP.	HA-4156-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS					
Offset Voltage	+25°C		1.0	5.0	mV
	Full		5.0	6.5	mV
Av. Offset Voltage Drift	Full		5		µV/°C
Bias Current	+25°C		60	300	nA
	Full			400	nA
Offset Current	+25°C		30	50	nA
	Full			100	nA
Common Mode Range	Full	±12			V
Differential Input Resistance	+25°C		5		MΩ
Input Noise Voltage (f = 1KHz)	+25°C		9		nV/√Hz
(f = 20Hz to 20kHz)	+25°C		1.4	2.0	µVRMS
TRANSFER CHARACTERISTICS					
Large Signal Voltage Gain (Note 4)	+25°C	25K	50K		V/V
	Full	15K			V/V
Common Mode Rejection Ratio (Note 8)	+25°C	80			dB
	Full	74			dB
Channel Separation (Note 5)	+25°C		-108		dB
Small Signal Bandwidth	+25°C	2.8	3.5		MHz
OUTPUT CHARACTERISTICS					
Output Voltage Swing (R_L = 10K)	Full	±12	±13.7		V
(R_L = 2K)	Full	±10	±12.5		V
Full Power Bandwidth (Note 4)	+25°C	20	25		KHz
Output Current (Note 6)	Full	±5	±15		mA
Output Resistance	+25°C		300		Ω
TRANSIENT RESPONSE (Note 7)					
Rise Time	+25°C		75		ns
Overshoot	+25°C		25		%
Slew Rate	+25°C	1.3	±1.6		V/µs
POWER SUPPLY CHARACTERISTICS					
Supply Current (I^+ or I^-)	+25°C			7.0	mA
Power Supply Rejection Ratio (Note 8)	Full	80			dB

NOTES:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. One amplifier may be shorted to ground indefinitely.
3. Derate 5.8mW/°C above T_A = +25°C.
4. V_{OUT} = ±10, R_L = 2K
5. Referred to input; f = 10KHz, R_S = 1K
6. V_{OUT} = ±10
7. See pulse response characteristics
8. ΔV = ±5.0V

HARRIS

HA-4600/02/05

High Performance Quad Operational Amplifier

FEATURES

- LOW OFFSET VOLTAGE 0.3mV
- HIGH SLEW RATE ±4V/μs
- WIDE BANDWIDTH 8MHz
- LOW DRIFT 2μV/°C
- FAST SETTLING (0.01%, 10V STEP) 4.2μs
- LOW POWER CONSUMPTION 35mW/AMP
- SUPPLY RANGE ±5V TO ±20V

APPLICATIONS

- HIGH Q, WIDE BAND FILTERS
- INSTRUMENTATION AMPLIFIERS
- AUDIO AMPLIFIERS
- DATA ACQUISITION SYSTEMS
- INTEGRATORS
- ABSOLUTE VALUE CIRCUITS
- TONE DETECTORS

DESCRIPTION

The HA-4600 series are high performance dielectrically isolated monolithic quad operational amplifiers with superior specifications not previously available in a quad amplifier. These amplifiers offer excellent dynamic performance coupled with low values for offset voltage and drift, input noise voltage and power consumption.

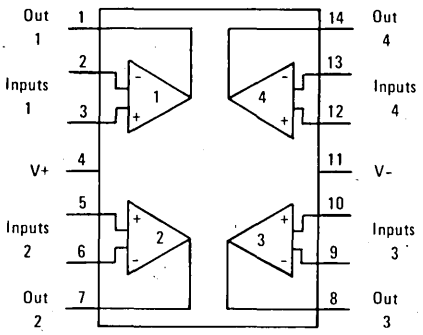
A wide range of applications can be achieved by using the features made available by the HA-4600 series. With wide bandwidth (8MHz), low power (35mW/amp), and internal compensation, these devices are ideally suited for precision active filter designs. For audio applications these amplifiers offer low noise ($8nV/\sqrt{Hz}$) and excellent full power bandwidth (60kHz). The HA-4602/4605 is particularly useful in designs requiring low offset voltage (0.3mV) and drift (2μV/°C), such as instrumentation and signal conditioning circuits. The high slew rate (4V/μs) and fast settling time (4.2μs to 0.01%, 10V step) makes these amplifiers useful compoinents in fast, accurate data acquisition systems.

The HA-4600 series are available in 14 pin CERDIP packages which are interchangeable with most other quad op amps. HA-4600/4602-2 is specified from -55°C to +125°C and HA-4600/4605-5 is specified over 0°C to +75°C range.

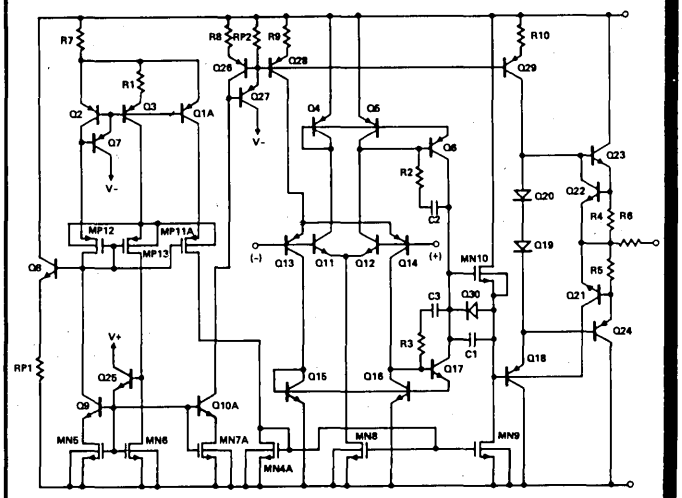
PINOUT

Section 11 for Packaging

TOP VIEW



SCHEMATIC



ONE FOURTH ONLY (HA-4600)

See Pages 3287-3291 for Package Information.

ABSOLUTE MAXIMUM RATINGS (Note 1)

T_A = +25°C Unless Otherwise Stated

Voltage Between V+ and V- Terminals	40.0V	Power Dissipation (Note 4)	880mW
Differential Input Voltage	±7V	Operating Temperature Range	
Input Voltage (Note 2)	±15.0V	HA-4600/4602-2	$-55^oC \leq T_A \leq +125^oC$
Output Short Circuit Duration (Note 3)	Indefinite	HA-4600/4605-5	$0^oC \leq T_A \leq +75^oC$
		Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS V+ = +15V, V- = -15V

		HA-4600-2 HA-4600-5			HA-4602-2 HA-4605-5			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		0.3	2.5		3.0	9	mV
	Full			3.0			10	mV
Av. Offset Voltage Drift	Full		2			5		µV/°C
Bias Current	+25°C		130	200		200	400	nA
	Full			325			500	nA
Offset Current	+25°C		30	75		70	150	nA
	Full			125			175	nA
Common Mode Range	Full	±12			±12			V
Input Noise Voltage (f = 1kHz)	+25°C		8			8		$nV/\sqrt{Hz}$
Input Resistance			500			500		kΩ
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 5)	Full	100K	250K		75K	250K		V/V
Common Mode Rejection Ratio (Note 9)	Full	86			80			dB
Channel Separation (Note 6)	+25°C		-108			-108		dB
Small Signal Bandwidth	+25°C		8			8		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (R_L = 10K)	Full	±12	±13		±12	±13		V
(R_L = 2K)	Full	±10	±12		±10	±12		V
Full Power Bandwidth (Note 5)	+25°C		60			60		kHz
Output Current (Note 7)	Full	±10	±15		±8	±15		mA
Output Resistance	+25°C		200			200		Ω
TRANSIENT RESPONSE (Note 8)								
Rise Time	+25°C		50			50		ns
Overshoot	+25°C		30			30		%
Slew Rate	+25°C	1	±4			±4		V/µs
Settling Time (Note 10)			4.2			4.2		µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		4.6	5.5		5.0	7.5	mA
Power Supply Rejection Ratio (Note 9)	Full	86			74			dB

HARRIS

HA-4620/22/25

Wideband, High Performance Quad Operational Amplifier

FEATURES

- Wide Gain Bandwidth Product — 70MHz
- High Slew Rate — ±20V/μs
- Low Offset Voltage — 0.3mV
- Fast Settling (0.01%, 10V Step) — 2.5μs
- Total Harmonic Distortion — <.01% to 30kHz
- Low Drift — 2μV/°C
- Low Power Consumption — 35mW/Amp
- Supply Range — ±5V to ±20V

APPLICATIONS

- High Q Wide Band Filters
- Pulse Amplifiers
- Audio Amplifiers
- Data Acquisition Systems
- Absolute Value Circuits
- Video and R.F. Amplifiers

DESCRIPTION

The HA-4620 series are wide band quad operational amplifiers featuring high slew rate, wide bandwidth and fast settling time specifications complemented by low input offset voltage, low drift and input noise voltage.

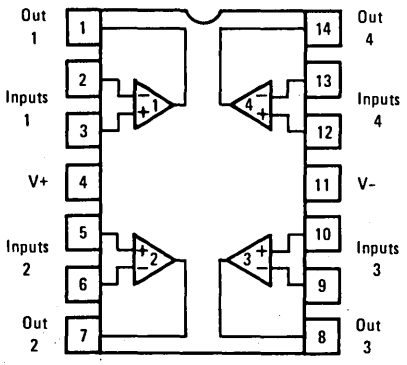
These dielectrically isolated devices are optimized to offer excellent features suitable for applications where a gain of 10 or greater is to be used. The 35mW/amp and a 70MHz gain-bandwidth-product make these monolithic amplifiers valuable components for many active filter circuits. HA-4620 series offers 0.3mW offset voltages and 2μV/°C offset voltage drift for very accurate signal conditioning designs. In high performance audio applications, these amplifiers deliver 260kHz full power bandwidth and $8nV\sqrt{Hz}$ noise voltage. For fast accurate data acquisition systems HA-4620 series offer 20V/μs slew rate and settling time of 2.5μsecs to 0.1% 10V step.

HA-4620 series are available in 14 pin CERDIP packages and are interchangeable with most other quad op amps. HA-4625 is also available in chip form. HA-4620/4622-2 is specified from -55°C to +125°C and HA-4620/4625-5 is specified over 0°C to +75°C range.

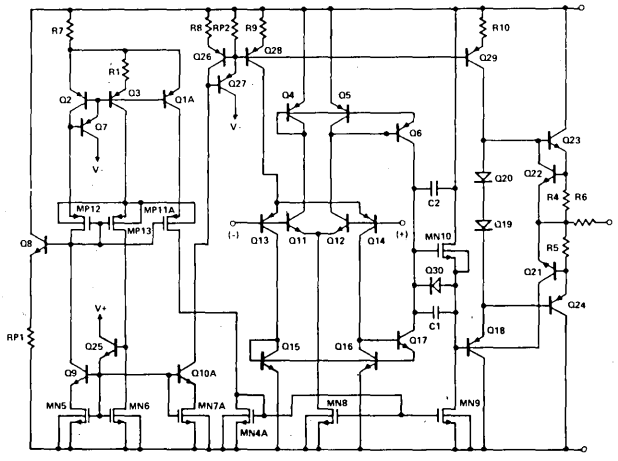
PINOUT

Section 11 for Packaging

TOP VIEW



SCHEMATIC



ONE FOURTH ONLY (HA-4620)

See Pages 3287-3291 for Package Information.

ABSOLUTE MAXIMUM RATINGS (Note 1)

T_A = +25°C Unless otherwise stated.

Voltage between V+ and V- Terminals	40.0V	Power Dissipation (Note 4)	880mW
Differential Input Voltage	±7V	Operating Temperature Range	
Input Voltage (Note 2)	±15.0V	HA-4620/4622-2	$-55°C \leq T_A \leq +125°C$
Output Short Circuit Duration (Note 3)	Indefinite	HA-4620/4625-5	$0°C \leq T_A \leq +75°C$
		Storage Temperature Range	$-65°C \leq T_A \leq +150°C$

ELECTRICAL CHARACTERISTICS

		HA-4620-2 HA-4620-5			HA-4622-2 HA-4625-5			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		0.3	2.5		3.0	9	mV
	Full			3.0			10	mV
Av. Offset Voltage Drift	Full		2			5		µV/°C
Bias Current	+25°C		130	200		200	400	nA
	Full			325			500	nA
Offset Current	+25°C		30	75		70	150	nA
	Full			125			175	nA
Common Mode Range	Full	±12			±12			V
Input Noise Voltage (f = 1kHz)	+25°C		8			8		$nV/\sqrt{Hz}$
Input Resistance	+25°C		500			500		kΩ
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 5)	Full	100K	250K		75K	250K		V/V
Common Mode Rejection Ratio (Note 6)	Full	86			80			dB
Channel Separation (Note 7)	+25°C		-108			-108		dB
Gain Bandwidth Products (Note 8)	+25°C		70			70		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (R_L = 10K)	Full	±12	±13		±12	±13		V
(R_L = 2K)	Full	±10	±12		±10	±12		V
Full Power Bandwidth (Note 9)	+25°C		260			260		kHz
Output Current (Note 7)	Full	±10	±15		±8	±15		mA
Output Resistance	+25°C		200			200		Ω
TRANSIENT RESPONSE (Note 11)								
Rise Time	+25°C		38	60		38		ns
Overshoot	+25°C		45	60		45		%
Slew Rate	+25°C	±12	±20		±12	±20		V/µs
Settling Time (Note 10)			2.5			2.5		µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		4.6	5.5		5.0	7.5	mA
Power Supply Rejection Ratio (Note 9)	Full	86			74			dB

HARRIS

HA-4741

Quad Operational Amplifier

FEATURES

- SLEW RATE — 1.6V/μs (TYP.)
- BANDWIDTH — 3.5MHz (TYP.)
- INPUT VOLTAGE NOISE — 9nV/$\sqrt{Hz}$ (TYP.)
- INPUT OFFSET VOLTAGE — 0.5mV (TYP.)
- INPUT BIAS CURRENT — 60nA (TYP.)
- SUPPLY RANGE — ±2V TO ±20V
- NO CROSSOVER DISTORTION
- STANDARD QUAD PIN-OUT

APPLICATIONS

- UNIVERSAL ACTIVE FILTERS
- D3 COMMUNICATIONS FILTERS
- AUDIO AMPLIFIERS
- BATTERY-POWERED EQUIPMENT

DESCRIPTION

The HA-4741, which contains four amplifiers on a monolithic chip, provides a new measure of performance for general purpose operational amplifiers. Each amplifier in the HA-4741 has operating specifications that equal or exceed those of the 741-type amplifier in all categories of performance.

HA-4741 is well suited to applications requiring accurate signal processing by virtue of its low values of input offset voltage (0.5mV), input bias current (60nA) and input voltage noise (9nV/ $\sqrt{Hz}$ at 1kHz). 3.5MHz bandwidth, coupled with high open-loop gain, allow the HA-4741 to be used in designs requiring amplification of wide band signals, such as audio amplifiers. Audio application is further enhanced by the HA-4741's negligible output crossover distortion. These excellent dynamic characteristics also make the HA-4741 ideal for a wide range of active filter designs. Performance integrity of multi-channel designs is assured by a high level of amplifier-to-amplifier isolation (108dB at 1kHz).

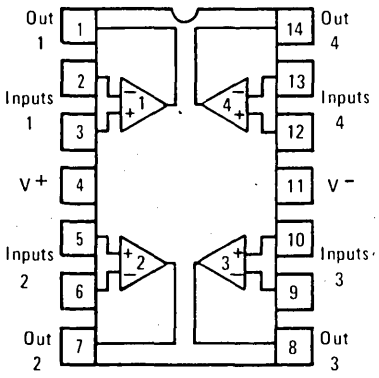
A wide range of supply voltages (±2V to ±20V) can be used to power the HA-4741, making it compatible with almost any system including battery-powered equipment.

The HA-4741 has guaranteed operation over -55°C to +125°C and can be furnished to meet MIL-STD-883 (HA-4741-8). The HA-4741-5 is guaranteed over 0°C to +75°C and is available in ceramic and plastic dual-in-line packages and in dice form.

PINOUT

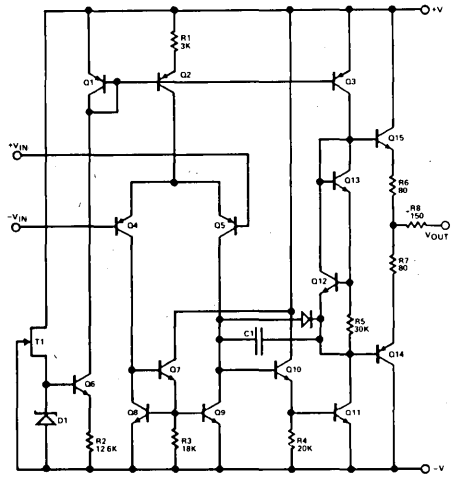
Section 11 for Packaging

TOP VIEW



QUAD OP AMP

SCHEMATIC



(¼) HA-4741

See Pages 3287-3291 for Package Information.

ABSOLUTE MAXIMUM RATINGS

T_A = +25°C Unless Otherwise Stated

Voltage Between V+ and V− Terminals	40.0V
Differential Input Voltage	±30.0V
Input Voltage (Note 1)	±15.0V
Output Short Circuit Duration (Note 2)	Indefinite
Power Dissipation For Epoxy Package. (Note 3)	880mW
Operating Temperature Range	
HA-4741-2	−55°C≤T_A≤+125°C
HA-4741-5	0°C≤T_A≤+75°C
Storage Temperature Range	−65°C≤T_A≤+150°C

ELECTRICAL CHARACTERISTICS

V+ = 15V, V− = −15V

PARAMETER	TEMP.	HA-4741-2 −55°C to +125°C MIN.	TYP.	MAX.	HA-4741-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		0.5	3.0		1.0	5.0	mV
	Full		4.0	5.0		5.0	6.5	mV
Av. Offset Voltage Drift	Full		5			5		µV/°C
Bias Current	+25°C		60	200		60	300	nA
	Full			325			400	nA
Offset Current	+25°C		15	30		30	50	nA
	Full			75			100	nA
Common Mode Range	Full	±12			±12			V
Differential Input Resistance	+25°C		5			5		MΩ
Input Noise Voltage (f = 1KHz)	+25°C		9			9		$nV/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 4)	+25°C	50K	100K		25K	50K		V/V
	Full	25K			15K			V/V
Common Mode Rejection Ratio (Note 8)	+25°C	80			80			dB
	Full	74			74			dB
Channel Separation (Note 5)	+25°C	90	−108		90	−108		dB
Small Signal Bandwidth	+25°C	2.5	3.5		2.5	3.5		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (R_L = 10K)	Full	±12	±13.7		±12	±13.7		V
(R_L = 2K)	Full	±10	±12.5		±10	±12.5		V
Full Power Bandwidth (Notes 4 & 9)	+25°C	14	25		14	25		kHz
Output Current (Note 6)	Full	±5	±15		±5	±15		mA
Output Resistance	+25°C		300			300		Ω
TRANSIENT RESPONSE (Notes 7 & 10)								
Rise Time (Note 11)	+25°C		75	140		75	140	ns
Overshoot (Note 11)	+25°C		25	40		25	40	%
Slew Rate (Note 12)	+25°C		±1.6			±1.6		V/µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C			5.0			7.0	mA
Power Supply Rejection Ratio (Note 8)	Full	80			80			dB

NOTES:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. One amplifier may be shorted to ground indefinitely.
3. Derate 5.8mW/°C above T_A = +25°C.
4. V_{OUT} = ±10, R_L = 2K
5. Referred to input; f = 10KHz, R_S = 1K
6. V_{OUT} = ±10
7. See pulse response characteristics
8. ΔV = ±5.0V
9. Full power bandwidth guaranteed based upon slew rate measurement FPBW = S.R./2πVpeak
10. R_L = 2K, C_L = 50pf.
11. V_{OUT} = ±200mV
12. V_{OUT} = ±5V

HARRIS

HA-5062 Series

Low Power JFET Input Dual Operational Amplifiers

Preliminary

FEATURES

- HIGH INPUT IMPEDANCE $10^{12}\Omega$
- LOW INPUT BIAS CURRENT 200pA
- LOW INPUT OFFSET CURRENT 100pA
- VERY LOW POWER CONSUMPTION
  TYPICAL SUPPLY CURRENT 200μA
- INTERNAL FREQUENCY COMPENSATION
- HIGH SLEW RATE 4V/μs
- PIN COMPATIBLE WITH LM1458
- DIRECT REPLACEMENT FOR TL062

APPLICATIONS

- ACTIVE FILTERS
- INSTRUMENTATION AMPLIFIERS
- AUDIO AMPLIFIERS
- BATTERY OPERATED EQUIPMENT
- SIGNAL CONDITIONING

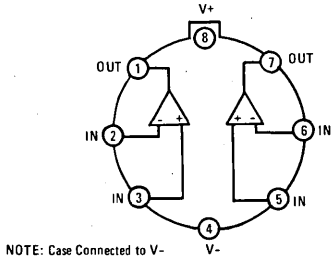
DESCRIPTION

The HARRIS HA-5062 operational amplifiers are a series of dual monolithic JFET-input amplifiers featuring low input bias and offset currents, high input impedence and very low power operation. In addition to being a direct replacement for the TL062 series, the HA-5062 series offers improved performance with a minimum open loop gain 20K V/V and a slew rate of 4v/μs.

This improved performance is a result of the HARRIS FET/Bipolar technology and makes the HA-5062 series of amplifiers ideally suited for applications in industrial control, communication, and battery powered instrumentation equipment.

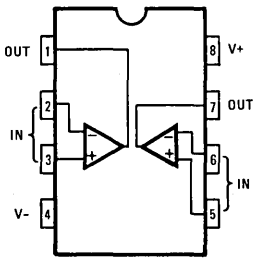
The HA-5062-2 is characterized for operation over the full military temperature range of -55°C to +125°C. The HA-5062A-5, HA-5062B-5 and HA-5062-5 are all characterized over the commercial temperature range of 0°C to +75°C.

PINOUT

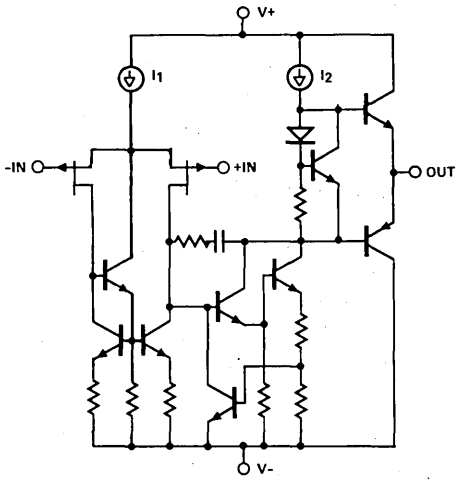


NOTE: Case Connected to V-

TOP VIEWS



SIMPLIFIED SCHEMATIC



(ONE HALF ONLY)

See Pages 3287-3291 for Package Information.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V- Terminals	± 20V
Differential Input Voltage	± 40V
Input Voltage (Note 2)	±15.0V
Output Short Circuit Duration	Indefinite

Power Dissipation	600mW*
Operating Temperature Range:	
HA-5062-2	$-55^oC \leq T_A \leq +125^oC$
HA-5062-5	$0^oC \leq T_A \leq +75^oC$
Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

* To-99 Derate by 6.75mW/°C above +85°C
Dip Derate by 5.57mW/°C above +65°C

ELECTRICAL CHARACTERISTICS

V+ = 15V V- = 15V

Parameters are guaranteed at indicated ambient temperature after warm-up.

		HA-5062-2 -55°C to +125°C			HA-5062A-5 0°C to 75°C			HA-5062B-5 0°C to 75°C			HA-5062-5 0°C to +75°C			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS														
Offset Voltage (Note 3)	+25°C		3	6		3	6		2	3		3	15	mV
	Full			9			7.5			5			20	mV
Av. Offset Voltage Drift	Full		10			10			10			10		µV/°C
Bias Current	+25°C		30	200		30	200		30	200		30	400	pA
	Full			50			7			7			10	nA
Offset Current	+25°C		5	100		5	100		5	100		5	200	pA
	Full			20			3			3			5	nA
Common Mode Range	Full	±10	±12		±10	±12		±10	±12		±10	±12		V
Input Resistance	+25°C		10^{12}			10^{12}			10^{12}			10^{12}		MΩ
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Note 4)	+25°C	20K	25K		20K	25K		20K	25K		10K	25K		V/V
	Full	10K			15K			15K			5K			V/V
Common Mode Rejection Ratio (Note 5)	Full	80	86		80	86		80	86		70	76		dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note 6)	+25°C	±10	±12		±10	±12		±10	±12		±10	±12		V
	Full	±10			±10			±10			±10			V
Unity Gain Bandwidth (Note 6)	+25°C		1			1			1			1		MHz
Full Power Bandwidth (Note 7)	+25°C		63			63			63			63		KHz
TRANSIENT RESPONSE														
Rise Time (Note 8)	+25°C		80			80			80			80		nsec
Overshoot (Note 8)	+25°C		10			10			10			10		%
Slew Rate (Note 9)	+25°C		4			4			4			4		V/µs
Settling Time (Note 10)	+25°C		3.5			3.5			3.5			3.5		µsec
POWER SUPPLY CHARACTERISTICS														
Supply Current (Note 11)	+25°C			0.4			0.4			0.4			0.5	mA
Power Supply Rejection Ratio (Note 12)	Full	80	95		80	95		80	95		70	95		dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. $R_S = 50\Omega$.
4. $R_L \geq 10K\Omega$, $V0 = \pm 10V$.
5. $\Delta V_{IN} = \pm 10V$.
6. $R_L = 10K\Omega$.
7. $R_L = 10K$; Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{SLEW\ RATE}{2\pi V_{PEAK}}$.
8. $V_{IN} = 50mV$, $C_L = 50pF$, $R_L = 10K\Omega$.
9. $V_{IN} = 10V$, $C_L = 50pF$, $R_L = 10K\Omega$.
10. Settling time is measured to 0.1% of final value for a 10 volt output step and $A_V = -1$.
11. No load, No signal.
12. $V_{SUPP} = \pm 5V$.D.C. to ±15 V.D.C.

HA-5064 Series

Low Power, JFET Input Quad Operational Amplifiers

JULY 1982

Preliminary

FEATURES

- LOW INPUT BIAS CURRENT — 100pA
- LOW POWER DISSIPATION — 24mW/Pkg.
- FAST SLEWING — 4V/μs
- LOW VIO DRIFT — 10μV/°C
- HIGH INPUT IMPEDANCE — $10^{12}\Omega$
- GOOD CHANNEL SEPARATION — 120dB
- POWER SUPPLY RANGE — ±5V TO ±20V

APPLICATIONS

WHERE DENSITY AND POWER REQUIREMENTS ARE DEMANDING:

- ACTIVE FILTERS
- SIGNAL CONDITIONING
- SIGNAL GENERATION
- INSTRUMENTATION AMPLIFIERS

DESCRIPTION

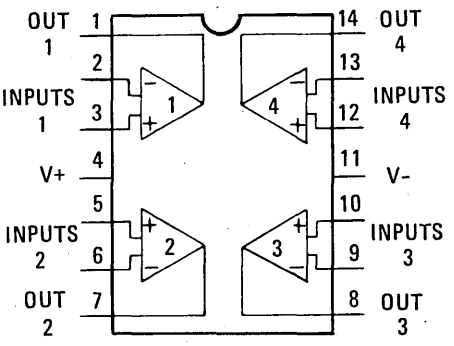
The HARRIS HA-5064 series JFET input monolithic, quad operational amplifiers feature very low power requirements coupled with excellent AC and DC characteristics. Maximum power dissipation of 24 mW/package is achieved by using complementary design, process, and layout techniques.

A 4V/μs slew rate coupled with 1MHz gain-bandwidth makes these devices most suitable for active filter and signal conditioning designs. The HA-5064 series is ideally suited for those applications demanding low power and high density without compromising other performance characteristics. High input impedance and low drift also makes the HA-5064 series useful as instrumentation amplifiers.

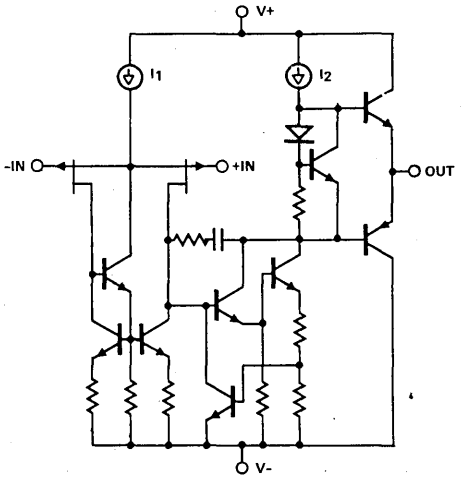
The HA-5064 is packaged in a 14-pin DIP and is pin compatible with most other quad operational amplifiers. The HA-5064-2 is specified for -55°C to +125°C operation while the HA-5064 A-5/HA-5064B-5/HA-5064-5 are specified over the 0°C to +75°C range.

PINOUT

TOP VIEW



SIMPLIFIED SCHEMATIC



ONE-FOURTH ONLY

See Pages 3287-3291 for Package Information.

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V-	40V
Differential Input Voltage (Note 2)	±30V
Output Current (Note 3)	Continuous
Internal Power Dissipation (Note 4)	500mW
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS

V+ = 15VDC; V- = -15VDC

		HA-5064-2 -55°C to +125°C			HA-5064A-5 0°C to +75°C			HA-5064B-5 0°C to +75°C			HA-5064-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS														
Offset Voltage	+25°C		2	6		2	6		2	3			15	mV
	Full			9			7.5			5			20	mV
Offset Voltage Average Drift	Full		10			10			10			20		µV/°C
Bias Current	+25°C			200			200			200			400	pA
	Full			50			7			7			10	nA
Offset Current	+25°C			100			100			100			200	pA
	Full			20			3			3			5	nA
Input Resistance	+25°C		10^{12}			10^{12}			10^{12}			10^{12}		Ω
Common Mode Range	Full	±10			±10			±10			±10			V
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Note 5)	+25°C	20K	25K		20K	25K		20K	25K		10K	25K		V/V
	Full	10K			15K			15K			5K			V/V
Common Mode Rejection Ratio (Note 6)	Full	80			80			80			70			dB
Gain Bandwidth	+25°C		1			1			1			1		MHz
Channel Separation (Note 7)	+25°C		120			120			120			120		dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note 8)	+25°C	±10	±12		±10	±12		±10	±12		±10	±12		V
	Full	±10			±10			±10			±10			V
Output Current (Note 9)	Full	±1			±1			±1			±1			mA
Full Power Bandwidth (Note 10)	+25°C		63			63			63			63		kHz
Output Resistance (Note 11)	+25°C		300			300			300			300		Ω
TRANSIENT RESPONSE (Note 12)														
Rise Time (10% TO 90%)	+25°C		80			80			80			80		nsec
Slew Rate	+25°C	2	4		2	4		2	4		2	4		V/µsec
Settling Time (Note 13)	+25°C		3.5			3.5			3.5			3.5		µsec
POWER SUPPLY CHARACTERISTICS														
Supply Current	+25°C			.8			.8			.8			1	mA
P. S. R. R. (Note 14)	Full	80			80			80			70			dB

HARRIS

HA-5082 Series

JFET Input Dual Operational Amplifiers

Preliminary

FEATURES

- HIGH INPUT IMPEDANCE $10^{12}\Omega$
- LOW INPUT BIAS CURRENT 200pA
- LOW INPUT OFFSET CURRENT 100pA
- LOW POWER CONSUMPTION TYPICAL SUPPLY CURRENT 3.5mA
- HIGH SLEW RATE 15V/μs
- PIN COMPATIBLE WITH LM1458
- DIRECT REPLACEMENT FOR TL082

APPLICATIONS

- ACTIVE FILTERS
- INSTRUMENTATION AMPLIFIERS
- AUDIO AMPLIFIERS
- SIGNAL CONDITIONING

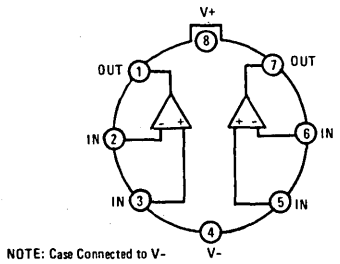
DESCRIPTION

The HARRIS HA-5082 operational amplifiers are a series of dual monolithic JFET-input amplifiers featuring low input bias and offset currents, high input impedance and, high slew rate. In addition to being a direct replacement for the TL082 series, the HA-5082 series offers improved performance with an input offset voltage of 2mV, a slew rate of 15V/μs, and bandwidths of 4MHz.

This improved performance is a result of the HARRIS FET/Bipolar technology and makes the HA-5082 series of amplifiers ideally suited for applications in industrial control, communication, and computer peripheral equipment.

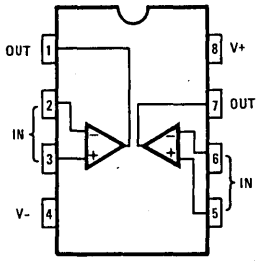
The HA-5082-2 is characterized for operation over the full military temperature range of -55°C to +125°C. The HA-5082A-5, HA-5082B-5 and HA-5082-5 are all characterized over the commercial temperature range of 0°C to +75°C.

PINOUT

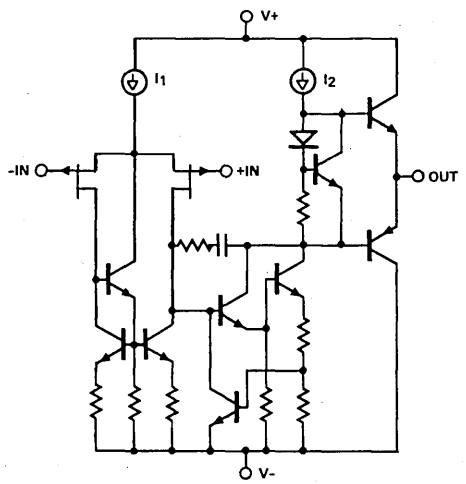


NOTE: Case Connected to V-

TOP VIEWS



SIMPLIFIED SCHEMATIC



(ONE HALF ONLY)

See Pages 3287-3291 for Package Information.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V- Terminals	±20V	Power Dissipation	600mW*
Differential Input Voltage	±40V	Operating Temperature Range:	
Input Voltage (Note 2)	±15.0V	HA-5082-2	$-55^oC \leq T_A \leq +125^oC$
Output Short Circuit Duration	Indefinite	HA-5082-5	$0^oC \leq T_A \leq +75^oC$
		Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

* To-99 Derate by 6.75mW/°C above +85°C
Dip Derate by 5.57mW/°C above +65°C

ELECTRICAL CHARACTERISTICS

V+ = 15V V- = -15V

Parameters are guaranteed at indicated ambient temperature after warm-up.

		HA-5082-2 -55°C to +125°C			HA-5082A-5 0°C to 75°C			HA-5082B-5 0°C to 75°C			HA-5082-5 0°C to +75°C			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS														
Offset Voltage (Note 3)	+25°C		3	5		3	5			2		5	15	mV
	Full			8			7			4			20	mV
Av. Offset Voltage Drift	Full		10			10			10			10		µV/°C
Bias Current	+25°C		30	200		30	200		30	200		30	400	pA
	Full			50			8			4			10	nA
Offset Current	+25°C		5	100		5	100		5	100		5	200	pA
	Full			20			4			2			5	nA
Common Mode Range	Full	±10	±12		±10	±12		±10	±12		±10	±12		V
Input Resistance	+25°C		10^{12}			10^{12}				10^{12}		10^{12}		MΩ
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Note 4)	+25°C	50K	200K		50K	200K		50K	200K		25K	200K		V/V
	Full	15K			25K			25K			15K			V/V
Common Mode Rejection Ratio (Note 5)	+25°C	80	86		80	86		80	86		70	76		dB
Unity Gain Bandwidth	+25°C		4			4			4			4		MHz
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note 6)	+25°C	±10	±12		±10	±12		±10	±12		±10	±12		V
	Full	±10			±10			±10			±10			V
Output Current (Note 7)	Full	±5			±5			±5			±5			mA
Full Power Bandwidth (Note 8)	+25°C		240			240			240			240		KHz
TRANSIENT RESPONSE														
Rise Time (Note 9)	+25°C		60			60			60			60		nsec
Overshoot (Note 9)	+25°C		10			10			10			10		%
Slew Rate (Note 10)	+25°C		15			15			15			15		V/µs
Settling Time (Note 11)	+25°C		2			2			2			2		µsec
POWER SUPPLY CHARACTERISTICS														
Supply Current (Note 12)	+25°C		3.5	5.6		3.5	5.6		3.5	5.6		3.5	5.6	mA
Power Supply Rejection Ratio (Note 13)	+25°C	80	86		80	86		80	86		70	76		dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. $R_S = 50\,\Omega$.
4. $R_L \geq 2K\,\Omega$, $V0 = \pm 10V$.
5. $\Delta V_{IN} = \pm 10V$.
6. $R_L = 2K\Omega$.
7. $V_{OUT} = \pm 10V$
8. $R_L = 2K$; Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{SLEW\ RATE}{2\pi V_{PEAK}}$.
9. $V_{IN} = 50mV$, $C_L = 100pF$, $R_L = 2K\,\Omega$.
10. $V_{IN} = 10V$, $C_L = 100pF$, $R_L = 2K\,\Omega$.
11. Settling time is measured to 0.1% of final value for a 10 volt output step and $A_V = -1$.
12. No load, No signal.
13. $V_{SUPP} = \pm 5V$ D.C. to ±15 V.D.C.

HARRIS

HA-5084 Series

JFET Input Quad Operational Amplifiers

Preliminary

FEATURES

- LOW INPUT BIAS CURRENT 200pA
- HIGH SLEW RATE 15V/μs
- WIDE BANDWIDTH 4MHz
- LOW DRIFT 10μV/°C
- HIGH INPUT IMPEDANCE $10^{12}\Omega$
- LOW SUPPLY CURRENT 7.2mA
- SUPPLY RANGE ±5V TO ±20V

APPLICATIONS

- HIGH Q, WIDEBAND FILTERS
- INTEGRATORS
- TONE DETECTORS
- SAMPLE/HOLD CIRCUITS
- DATA ACQUISITION SYSTEMS
- ABSOLUTE VALUE CIRCUITS

DESCRIPTION

The Harris HA-5084 is a JFET input, monolithic, quad operational amplifier featuring low input bias and offset currents, high input impedance, and high slew rate. Manufactured using FET/Bipolar technology coupled with advanced layout considerations, these devices also feature excellent channel separation and offset voltage drift specifications.

High slew rate (15V/μs) coupled with excellent input bias (30pA) and offset current (3pA) make the HA-5084 ideally suited for high speed analog designs such as integrators, fast D/A converters, and sample-and-hold circuits.

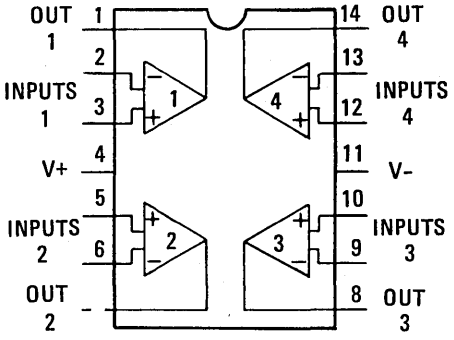
The HA-5084 is available in ceramic and plastic 14 pin DIP's and is pin compatible with the LM324, LM348, and MC3403 quad operational amplifier pinout.

The HA-5084-2 is specified from -55°C to +125°C while the HA-5084-5 operates from 0°C to +75°C.

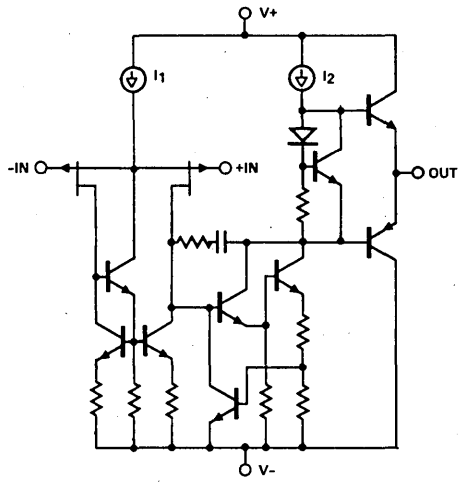
PINOUT

Section 11 for Packaging

TOP VIEW



SIMPLIFIED SCHEMATIC



(ONE FOURTH ONLY)

See Pages 3287-3291 for Package Information.

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V-	40V
Differential Input Voltage (Note 2)	±40V
Output Current (Note 3)	Full Short Circuit Protection
Internal Power Dissipation (Note 4)	500mW
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS

V+ = 15VDC; V- = -15VDC

		HA-5084-2 -55°C to +125°C			HA-5084A-5 0°C to +75°C			HA-5084B-5 0°C to +75°C			HA-5084-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS														
Offset Voltage	+25°C			5			5			2			15	mV
	Full			8			7			4			20	mV
Offset Voltage Average Drift	Full		8.3			8.3			8.3			8.3		µV/°C
Bias Current	+25°C			200			200			200			400	pA
	Full			50			8			4			10	nA
Offset Current	+25°C			100			100			100			200	pA
	Full			20			4			2			5	nA
Input Resistance	+25°C		10^{12}			10^{12}			10^{12}			10^{12}		Ω
Common Mode Range	Full	±10			±10			±10			±10			V
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Note 5)	+25°C	25K			50K			50K			25K			V/V
	Full	15K			25K			25K			15K			V/V
Common Mode Rejection Ration (Note 6)	Full	70			80			80			70			dB
Unity Gain Bandwidth	+25°C		4			4			4			4		MHz
Channel Separation (Note 7)			-120			-120			-120			-120		dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note8)	+25oC	10			10			10			10			V
	Full	10			10			10			10			V
Output Current (Note 9)	Full	±5			±5			±5			±5			mA
Full Power Bandwidth (Note 10)	+25°C		240			240			240			240		kHz
Output Resistance (Note 11)	+25°C		300			300			300			300		Ω
TRANSIENT RESPONSE (Note 12)														
Rise Time	+25oC		60			60			60			60		nsec
Slew Rate	+25°C		15			15			15			15		V/µsec
Settling Time (Note 13)	+25°C		2			2			2			2		µsec
POWER SUPPLY CHARACTERISTICS														
Supply Current	+25°C		7.2	11		7.2	11		7.2	11		7.2	12	mA
P. S. R. R. (Note 14)	Full	80			80			80			70			dB

HA-5100/5105

Wideband, JFET Input Operational Amplifier

FEATURES

- LOW INPUT OFFSET VOLTAGE 0.5mV
- LOW OFFSET DRIFT . . . . . 5μV/°C
- LOW INPUT BIAS CURRENT 50pA
- LARGE VOLTAGE GAIN . . . . . 150K V/V
- WIDE BANDWIDTH 18MHz
- HIGH SLEW RATE 8V/μsec
- FAST LARGE SIGNAL SETTLING TIME: 1.7μsec

APPLICATIONS

- PRECISION, HIGH SPEED, DATA ACQUISITION SYSTEMS
- PRECISION SIGNAL GENERATION
- PULSE AMPLIFICATION

GENERAL DESCRIPTION

The HA-5100/5105 are monolithic wideband operational amplifiers manufactured with FET/Bipolar technologies and dielectric isolation. Precision laser trimming of the input stage complements the amplifier high frequency capabilities with excellent input characteristics.

The HA-5100/5105 offer a number of important advantages over similar FET input op amps from other manufacturers. In addition to superior bandwidth and settling characteristics the Harris devices have quite constant slew rate, bandwidth, and settling characteristics over the operating range. This provides the user predictable performance in applications where settling time, full power bandwidth, closed loop bandwidth, or phase shift is critical. The slewing waveform is symmetrical to provide reduced distortion. Note also that Harris specifies all parameters at ambient (rather than junction) temperature to provide the designer meaningful data to predict actual operating performance.

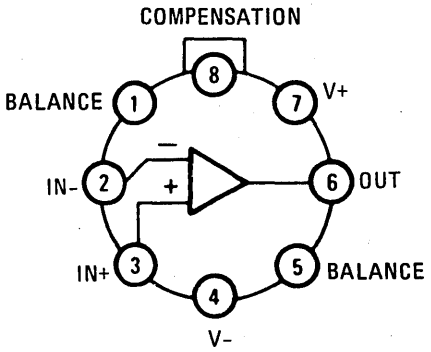
Complementing HA-5100/5105's predictable and excellent dynamic characteristics are very low input offset voltage, very low input bias current, and extremely high input impedance. This ideal combination of features make these amplifiers most suitable for precision, high speed, data acquisition system designs and for a wide variety of signal conditioning applications.*

* -2 denotes a range of -55°C to +125°C and -5 denotes a 0°C to +75°C range.

PINOUT

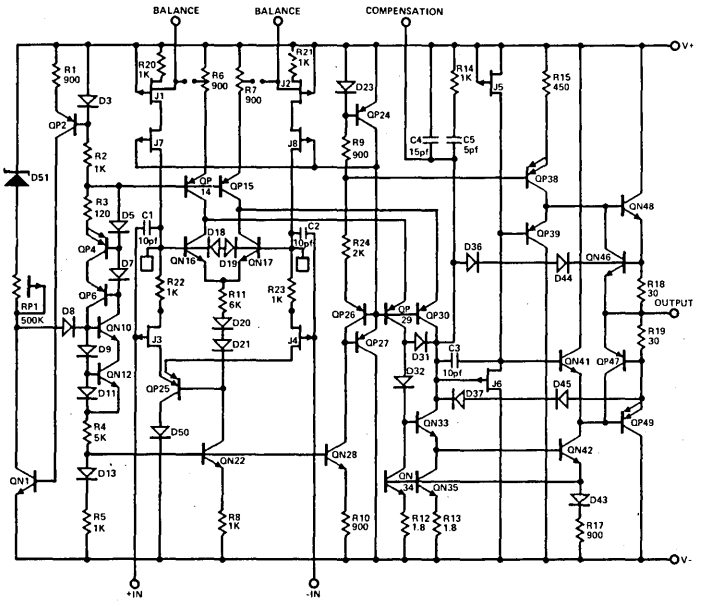
Section 11 for Packaging

TOP VIEW



CASE CONNECTED TO V-

SCHEMATIC DIAGRAM



See Pages 3287-3291 for Package Information.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V-	40V
Differential Input Voltage	±40V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation (Note 2)	510mW
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS

		HA-5100-2 -55°C to +125°C			HA-5100-5 0°C to +75°C			HA-5105-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		0.5	1.0		0.5	1.0		0.5	1.5	mV
	Full		0.50	2.0		0.50	2.0		0.75	3.5	mV
Offset Voltage Average Drift	Full		5			10			15		µV/°C
Bias Current	+25°C		20	50		20	50		50	100	pA
	Full		5	10			10		10	20	nA
Offset Current	+25°C		2	10		2	10		5	50	pA
	Full		2	5		2	5		5	10	nA
Input Resistance	+25°C		10^{12}			10^{12}			10^{12}		Ω
Common Mode Range	Full	±10	±11		±10	±11		±10	±10.5		V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 3)	+25°C	75K	150K		75K	150K		50K	100K		V/V
	Full	60K	100K		60K	100K		40K	80K		V/V
Common Mode Rejection Ratio (Note 4)	Full	80	86		80	86		80	86		dB
Gain Bandwidth Product at A_V = 10	Full		18			18			18		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 5)	+25°C	±12	±13		±12	±13		±11	±12		V
	Full	±12	±13		±12	±13		±11	±12		V
Short Circuit Output Current (Note 6)	Full	±10	±15		±10	±15		±8	±15		mA
Full Power Bandwidth (Note 7)	+25°C	90	150		90	150		75	125		kHz
Output Resistance (Note 8)	+25°C		30			30			40		Ω
TRANSIENT RESPONSE (Note 9)											
Rise Time	+25°C		15	35		15	35		20		nsec
Slew Rate	+25°C	6	8		6	8		5	8		V/µsec
Settling Time (Note 10)	+25°C		1.7			1.7			2.0		µsec
POWER SUPPLY CHARACTERISTICS											
Supply Current	Full		5	7		5	7		6	8	mA
P.S.R.R. (Note 11)	Full	80	86		80	86		80	86		dB

HARRIS

HA-5110/5115

Wideband, JFET Input, Uncompensated, Operational Amplifier

FEATURES

- WIDE GAIN BANDWIDTH 60MHz
- HIGH SLEW RATE 50V/μs
- SETTLING TIME 850ns
- POWER BANDWIDTH 800KHz
- OFFSET VOLTAGE 0.5mV
- BIAS CURRENT 50pA

APPLICATIONS

- VIDEO AND RF AMPLIFIERS
- DATA ACQUISITION
- PULSE AMPLIFIERS
- PRECISION SIGNAL GENERATION

DESCRIPTION

HA-5110/5115 are wideband, uncompensated, operational amplifiers manufactured with FET/Bipolar technologies and dielectric isolation. These monolithic amplifiers feature superior high frequency capabilities further enhanced by precision laser trimming of the input stage to provide excellent input characteristics. These devices are controlled at closed loop gains greater than 10 without compensation.

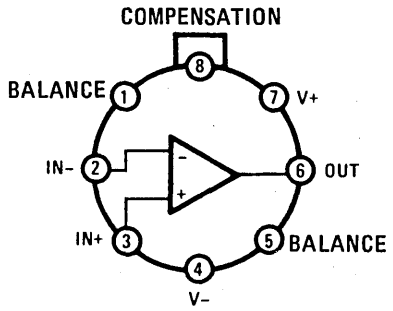
With excellent dynamic and input characteristics, HA-5110/5115 are well suited for many wideband, pulse, and video applications. These amplifiers are ideal components for video and RF circuitry requiring up to 60MHz gain-bandwidth-product and 800KHz power bandwidth. 50V/μs slew rate and 850ns settling time make these devices useful in pulse amplification and data acquisition designs. HA-5110/5115's 0.5mV offset voltage, 10pA offset current, and extremely high impedance coupled with excellent AC parameters make these amplifiers ideal selections for accurate signal conditioning designs. For applications requiring less critical input characteristics, HA-5115 is available in untrimmed form.

HA-5110/5115 are available in metal can (TO-99) packages. Suffix -2 denotes a range to -55°C to +125°C and -5 denotes a 0°C to +75°C range.

PINOUT

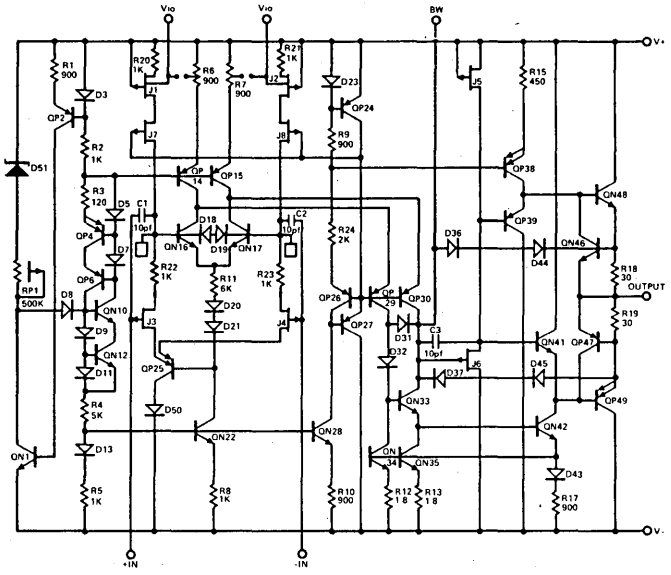
Section 11 for Packaging

TOP VIEW



CASE CONNECTED TO V-

SCHEMATIC



See Pages 3287-3291 for Package Information.

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^-	40V	Internal Power Dissipation (Note 2)	510mW
Differential Input Voltage	±40V	Storage Temperature Range	-65°C to +150°C
Peak Output Current	Full Short Circuit Protection		

ELECTRICAL CHARACTERISTICS

V+ = 15VDC; V- = -15VDC
Parameters are guaranteed at indicated ambient temperature after warm-up.

		HA-5110-2 -55°C to +125°C			HA-5110-5 0°C to +75°C			HA-5115-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		0.5	1.0		0.5	1.0		0.5	1.5	mV
	Full		0.50	2.0		0.50	2.0		0.75	3.5	mV
Offset Voltage Average Drift	Full		5			10			15		µV/°C
Bias Current	+25°C		20	50		20	50		50	100	pA
	Full		5	10			10		10	20	nA
Offset Current	+25°C		2	10		2	10		5	50	pA
	Full		2	5		2	5		5	10	nA
Input Resistance	+25°C		10^{12}			10^{12}			10^{12}		Ω
Common Mode Range	Full	±10	±11		±10	±11		±10	±10.5		V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 3)	+25°C	75K	150K		75K	150K		50K	100K		V/V
	Full	60K	100K		60K	100K		40K	80K		V/V
Common Mode Rejection Ratio (Note 4)	Full	80	86		80	86		80	86		dB
Gain Bandwidth Product (A_V = 10)	Full		60			60			50		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 5)	+25°C	±12	±13		±12	±13		±11	±12		V
	Full	±12	±13		±12	±13		±11	±12		V
Output Current (Note 6)	+25°C	±10	±15		±10	±15		±8	±15		mA
Full Power Bandwidth (Note 7)	+25°C	550	625		550	625		550	625		kHz
Output Resistance (Note 8)	+25°C		30			30			40		Ω
TRANSIENT RESPONSE (Note 9)											
Rise Time (A_V = 10)	+25°C		20			20			20		nsec
Slew Rate (A_V = 10)	+25°C	35	50		35	50		35	40		V/µsec
Settling Time (Note 10)	+25°C		.85			.85			1.0		µsec
POWER SUPPLY CHARACTERISTICS											
Supply Current	Full		5	7		5	7		6	8	mA
Power Supply Rejection Ratio (Note 11)	+25°C	80	94		80	94		80	94		dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 6.8mW/°C for operation at ambient temperatures above +75°C.
3. V_{OUT} = ±10V. R_L = 2K
4. V_{CM} = ±10 V.D.C.
5. R_L = 10K
6. V_{OUT} = 0V
7. R_L = 2K; Full power bandwidth guaranteed, based on slew rate measurement using $FPBW = \frac{SLEW\ RATE}{2\pi V_{PEAK}}$
8. Output resistance measured under open loop conditions.
9. Refer to Test Circuits section of the data sheet.
10. Settling Time is measured to 0.1% of final value for a 10 volt output step and A_V = -10.
11. V_{SUPP} = ±10 V.D.C. to ±20 V.D.C.

HARRIS

HA-5130/5135

Precision Operational Amplifier

FEATURES

- LOW OFFSET VOLTAGE — 25μV
- LOW OFFSET VOLTAGE DRIFT — 0.4μV/^{o}C
- LOW NOISE — 9nV/$\sqrt{Hz}$
- OPEN LOOP GAIN — 10^7
- BANDWIDTH (UNITY GAIN) — 2.5MHz
- ALL BIPOLAR CONSTRUCTION

APPLICATIONS

- HIGH GAIN INSTRUMENTATION
- PRECISION DATA ACQUISITION
- PRECISION INTEGRATORS
- BIOMEDICAL AMPLIFIERS
- PRECISION THRESHOLD DETECTORS

DESCRIPTION

HA-5130/5135 are precision operational amplifiers manufactured using a combination of key technological advancements to provide outstanding input characteristics.

A Super Beta input stage is combined with laser trimming, dielectric isolation, and matching techniques to produce 25μV (Max.) input offset voltage and 0.4μV/^{o}C input offset voltage average drift. Other features enhanced by this process include 9nV (Typ.) Input Noise Voltage, 1nA Input Bias Current, and 140dB Open Loop Gain.

These features coupled with 120dB CMRR and PSRR make HA-5130/5135 an ideal device for precision DC instrumentation amplifiers. Excellent input characteristics in conjunction with 2.5MHz bandwidth and 0.8V/μs slew rate, makes this amplifier extremely useful for precision integrator and biomedical amplifier designs. These amplifiers are also well suited for precision data acquisition and for accurate threshold detector applications.

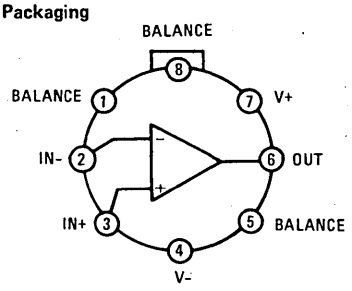
HA-5130/35 is packaged in an 8 pin (TO-99) can and an 8 lead Cerdip and is pin compatible with many existing op amp configurations.

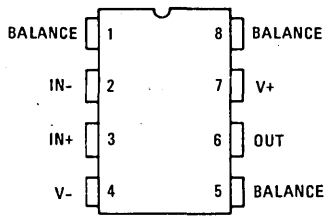
HA-5130/5135-2 is specified for -55^{o}C to +125^{o}C operation while HA-5130/5135-5 operate from 0^{o}C to +75^{o}C.

PINOUT

Section 11 for Packaging

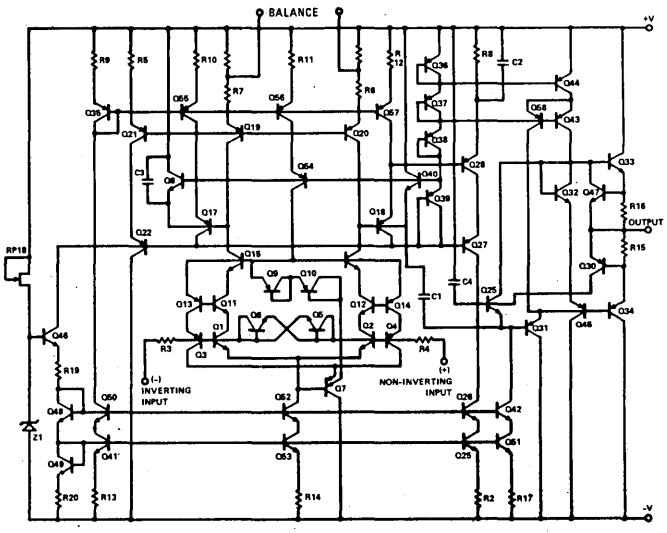
TOP VIEW





* Pins 5 and 8 are internally connected

SCHEMATIC



See Pages 3287-3291 for Package Information.

ABSOLUTE MAXIMUM RATINGS (Note 1)

T_A = +25°C Unless otherwise stated

Voltage Between V+ and V- Terminals	40.0V	Power Dissipation (Note 2)	300mW
Differential Input Voltage	±15.0V	Operating Temperature Range	
		HA-5130/5135-2	$-55^oC \leq T_A \leq +125^oC$
		HA-5130/5135-5	$0^oC \leq T_A \leq +75^oC$
Output Short Circuit Duration	Indefinite	Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS V+ = 15V, V- = -15V

PARAMETER	TEMP.	HA-5130-2/-5 MIN.	HA-5130-2/-5 TYP.	HA-5130-2/-5 MAX.	HA-5135-2/-5 MIN.	HA-5135-2/-5 TYP.	HA-5135-2/-5 MAX.	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		10	25		10	75	μV
	Full		50	60		50	130	μV
Average Offset Voltage Drift	Full		0.4	0.6		0.4	1.3	μV/°C
Bias Current	+25°C		±1	±2		±1	±4	nA
	Full			±4			±6	nA
Bias Current Average Drift	Full		0.02	0.04		0.02	0.04	nA/°C
Offset Current	+25°C			2			4	nA
	Full			4			5.5	nA
Offset Current Average Drift	Full		0.02	0.04		0.02	0.04	nA/°C
Common Mode Range	Full	±12			±12			V
Differential Input Resistance	+25°C	20	30		20	30		MΩ
Input Noise Voltage 0.1Hz to 10Hz (Note 3)	+25°C			0.6			0.6	μV_{p-p}
Input Noise Voltage Density (Note 3)	+25°C							$nV/\sqrt{Hz}$
f_O = 10Hz			13.0	18.0		13.0	18.0	
f_O = 100Hz			10.0	13.0		10.0	13.0	
f_O = 1000Hz			9.0	11.0		9.0	11.0	
Input Noise Current (Note 3) 0.1Hz to 10Hz	+25°C		15	30		15	30	pA_{p-p}
Input Noise Current Density (Note 3)	+25°C							$pA/\sqrt{Hz}$
f_O = 10Hz			0.4	0.8		0.4	0.8	
f_O = 100Hz			0.17	0.23		0.17	0.23	
f_O = 1000Hz			0.14	0.17		0.14	0.17	
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 4)	+25°C	120	140		120	140		dB
	Full	120			120			dB
Common Mode Rejection Ratio (Note 5)	Full	110	120		106	120		dB
Closed Loop Bandwidth (A_{VCL} = +1)	+25°C	0.6	2.5		0.6	2.5		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 6)	+25°C	±10	±12		±10	±12		V
	Full	±10			±10			V
Full Power Bandwidth (Note 7)	+25°C	8	10		8	10		kHz
Output Current (Note 8)	+25°C	±25	±30		±25	±30		mA
Output Resistance (Note 9)	+25°C		45			45		Ω
TRANSIENT RESPONSE (Note 10)								
Rise Time	+25°C		340			340		ns
Slew Rate	+25°C	0.5	0.8		0.5	0.8		V/μs
Settling Time (Note 11)	+25°C		11			11		μs
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full		1.0	1.3		1.0	1.7	mA
Power Supply Rejection Ratio (Note 12)	Full	100	130		94	130		dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 6.8mW/°C for operation at ambient temp.'s above +75°C.
3. Not tested. 90% of units meet or exceed these specifications.
4. V_{OUT} = ±10V; R_L = 2k. Gain dB = 20 $\log_{10}$ Average
   ∴ 120dB = 1000V/mV
   140dB = 10,000V/mV
5. V_{CM} = ±10V DC
6. R_L = 600Ω
7. R_L = 2k; Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{SLEW\ RATE}{2\pi V_{PEAK}}$
8. V_{OUT} = 10V
9. Output resistance measured under open loop conditions (f = 100Hz)
10. Refer to test circuits section of the data sheet.
11. Settling time is measured to 0.1% of final value for a 10V output step and A_V = -1.
12. V_{SUPP} = ±5V DC to ±20V DC.

HARRIS

ADVANCE

HA-5141/42/44

Ultra-Low Power Operational Amplifier

FEATURES

- LOW SUPPLY CURRENT 60μA
- WIDE OPERATING VOLTAGE RANGE 2V to 30V
- SINGLE SUPPLY OPERATION
- HIGH SLEW RATE 1.5V/μs
- HIGH GAIN 100K V/V
- AVAILABLE IN SINGLES, DUALS AND QUADS

APPLICATIONS

- PORTABLE INSTRUMENTS
- METER AMPLIFIERS
- TELEPHONE HEADSETS
- MICROPHONE AMPLIFIERS
- INSTRUMENTATION

DESCRIPTION

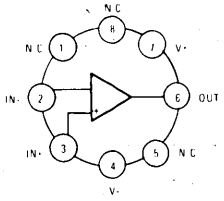
The HA-5141/42/44 ultra-low power operational amplifiers provide AC and DC performance characteristics similar to or better than most general purpose amplifiers while only drawing 1/30 of the supply current of most general purpose amplifiers. These amplifiers are well suited to applications which require low power dissipation and good electrical characteristics.

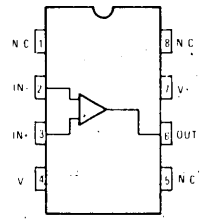
The HA-5141/42/44 provides accurate signal processing by virtue of its low input offset voltage (0.5mV), low input bias current (50nA), high open loop gain (100KV/V) and low noise, for low power operational amplifiers (20nV/$\sqrt{Hz}$). These characteristics coupled with 1.5V/μs slew rate and 400KHz bandwidth make the HA-5141/42/44 ideal for use in low power instrumentation, audio amplifier and active filter designs. The wide range of supply voltages (2V to 30V) also allow these amplifiers to be very useful in low voltage battery powered equipment.

These amplifiers are available in singles (HA-5141, can or minidip), duals (HA-5142, can or minidip) or quads (HA-5144, 14 pin dip) with industry standard pinouts which allow the HA-5141/42/44's to be interchangeable with most other operational amplifiers.

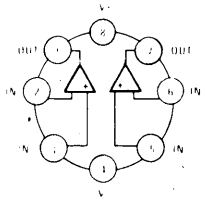
PINOUTS

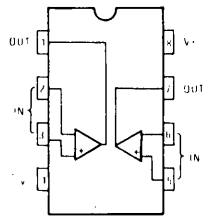
TOP VIEW



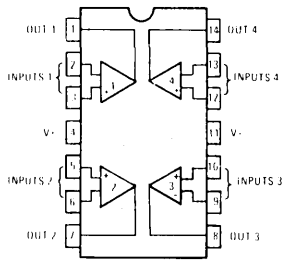


TOP VIEW



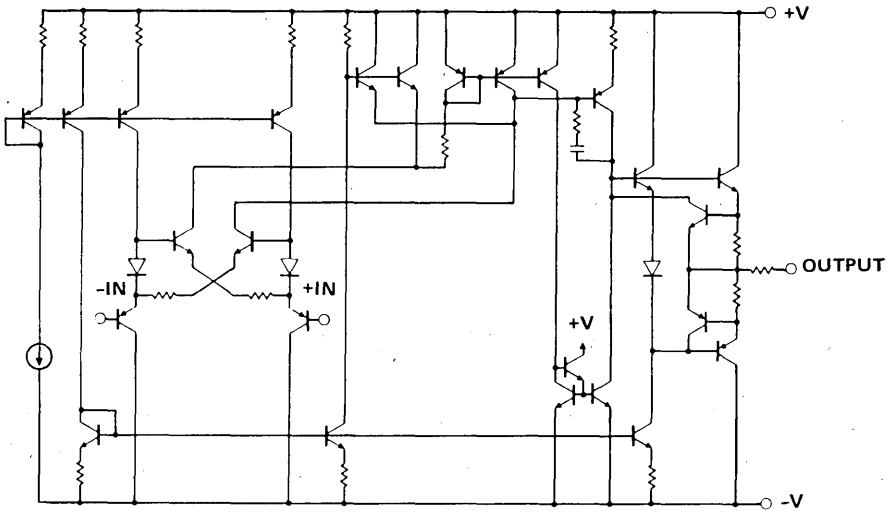


TOP VIEW



See Pages 3287-3291 for Package Information.

SCHEMATIC



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	40V	Operating Temperature Range	$0^oC \leq T_A \leq +75^oC$
Differential Input Voltage	±7V		$-55^oC \leq T_A \leq +125^oC$
Output Current	S/C Protected	Storage Temperature Range	$-65^o \leq T_A \leq +150^oC$
Internal Power Dissipation	500mW		

ELECTRICAL CHARACTERISTICS V+ = +5V

		HA-5141/42/44A			HA-5141/42/44			
PARAMETER	TEMP.	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		0.5	6		0.7	7	mV
	Full			8			9	mV
Bias Current	+25°C		45	75		45	100	nA
	Full			100			125	nA
Offset Current	+25°C		0.3	10		0.3	10	nA
	Full			15			20	nA
Common Mode Range	Full	0 to 4			0 to 3			V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain	+25°C	50	100		20	100		KV/V
(Note 1)	Full	30			15			KV/V
Common Mode Rejection	Full	80	105		77	105		dB
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 1)	Full	0 to 4			0 to 3			V
TRANSIENT RESPONSE								
Slew Rate (Notes 1,2,3)	+25°C	1	1.5		0.5	1		V/μs
POWER SUPPLY CHARACTERISTICS								
Supply Current (per Amplifier)	+25°C		45	65		50	80	μA
	Full			75			100	μA
Power Supply Rejection Ratio	Full	80	105		77	105		dB

NOTES:
1. RL = 50K
2. CL = 50pf
3. VIN = +3V Pulse

HARRIS HA-5160/5162

Wideband, JFET Input, High Slew Rate, Uncompensated, Operational Amplifier

FEATURES

- WIDE GAIN BANDWIDTH 100MHz
- HIGH SLEW RATE 120V/μs
- SETTLING TIME (0.2%) 280ns
- POWER BANDWIDTH 1000kHz
- OFFSET VOLTAGE 1.0mV
- BIAS CURRENT 20pA

APPLICATIONS

- VIDEO AND RF AMPLIFIERS
- DATA ACQUISITION
- PULSE AMPLIFIERS
- PRECISION SIGNAL GENERATION

DESCRIPTION

The HA-5160/5162 is a wideband, uncompensated, operational amplifier manufactured with FET/Bipolar technologies and dielectric isolation. This monolithic amplifier features superior high frequency capabilities further enhanced by precision laser trimming of the input stage to provide excellent input characteristics. This device has excellent phase margin at a closed loop gain of 10 without external compensation.

The HA-5160/5162 offers a number of important advantages over similar FET input op amps from other manufacturers. In addition to superior bandwidth and settling characteristics, the HARRIS devices have nearly constant slew rate, bandwidth, and settling characteristics over the operating temperature range. This provides the user predictable performance in applications where settling time, full power bandwidth, closed loop bandwidth, or phase shift is critical. Note also that HARRIS specified all parameters at ambient (rather than junction) temperature to provide the designer meaningful data to predict actual operating performance.

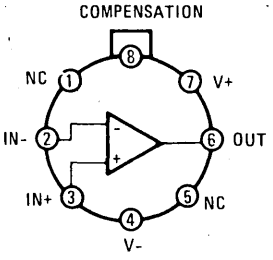
Complementing the HA-5160/5162's predictable and excellent dynamic characteristics are very low input offset voltage, very low input bias current, and extremely high input impedance. This ideal combination of features make these amplifiers most suitable for precision, high speed, data acquisition system designs and for a wide variety of signal conditioning applications.* The HA-5160 provides excellent performance for applications which require both precision and high speed performance. The HA-5162 meets or exceeds the performance specifications of National's hybrid op amp, the LH0062.

* -2 denotes a range of -55°C to +125°C and -5 denotes a 0°C to +75°C range.

PINOUT

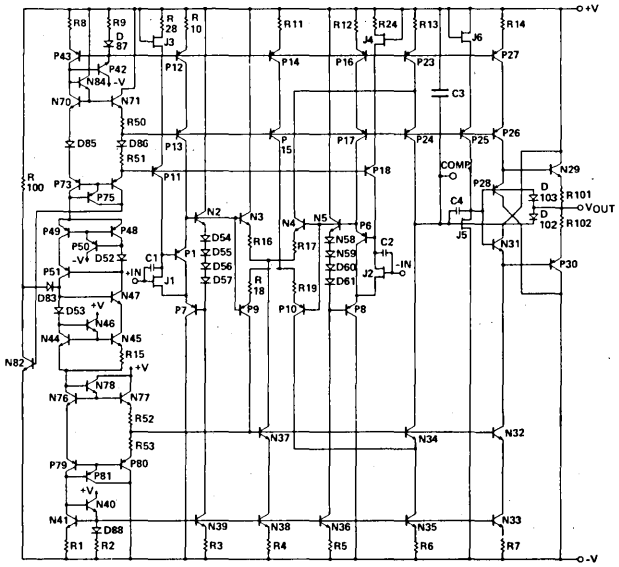
Section 11 for Packaging

TOP VIEW



Case connected to V-

SCHEMATIC



See Pages 3287-3291 for Package Information.

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V-	40V
Differential Input Voltage	±40V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation (Note 2)	675mW
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS V+ = +15V, V- = -15V

		HA-5160-2 -55°C to +125°C			HA-5160-5 0°C to +75°C			HA-5162-5 0°C to 75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	TYP	UNITS
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		1.0	3.0		1.0	3.0		3	15	mV
	Full		3.0	5.0		3.0	5.0		5	20	mV
Offset Voltage Average Drift	Full		10			20			20	35	µV/°C
Bias Current	+25°C		20	50		20	50		20	65	pA
	Full		5	10			10			10	nA
Offset Current	+25°C		2	10		2	10		2	10	pA
	Full		2	5		2	5		2	5	nA
Input Resistance	+25°C		10^{12}			10^{12}			10^{12}		Ω
Common Mode Range	Full	±10	±11		±10	±11		±10	±11		V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 3)	+25°C	75K	150K		75K	150K		25K	100K		V/V
	Full	60K	100K		60K	100K		25K	75K		V/V
Common Mode Rejection Ratio (Note 4)	Full	74	80		74	80		70	80		dB
Gain Bandwidth Product (A_V = 10)	Full		100			100			100		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 5)	+25°C	±10	±11		±10	±11		±10	±11		V
	Full	±10	±11		±10	±11		±10	±11		V
Output Current (Note 6)	+25°C	±15	±20		±15	±20		±15	±20		mA
Full Power Bandwidth (Note 7)	+25°C		1000			1000			1000		kHz
Output Resistance (Note 8)	+25°C		50			50			50		Ω
TRANSIENT RESPONSE (Note 9)											
Rise Time (A_V = 10)	+25°C		20			20			20		ns
Slew Rate (A_V = 10)	+25°C	100	120		100	120		50	70		V/µs
Settling Time (Note 10)	+25°C		280			280			400		ns
POWER SUPPLY CHARACTERISTICS											
Supply Current	Full		8.0	10		8.0	10		8.0	12	mA
Power Supply Rejection Ratio (Note 11)	+25°C	74	86		74	86		70	86		dB

HARRIS

HA-5170

Precision JFET Input Operational Amplifier

Preliminary

FEATURES

- LOW OFFSET VOLTAGE — 100μV
- LOW OFFSET VOLTAGE DRIFT — 3μV/°C
- LOW NOISE — $12nV/\sqrt{Hz}$
- OPEN LOOP GAIN — 100K
- BANDWIDTH (UNITY GAIN) — 5MHz

APPLICATIONS

- HIGH GAIN INSTRUMENTATION
- PRECISION DATA ACQUISITION
- PRECISION INTEGRATORS
- PRECISION THRESHOLD DETECTORS

DESCRIPTION

The Harris HA-5170 is a precision, JFET input, operational amplifier which features low noise, low offset voltage and low offset voltage drift. Constructed using FET/Bipolar technology, the Harris Dielectric Isolation (DI) process, and laser trimming this amplifier offers low input bias and offset currents. This operational amplifier design also completely eliminates the troublesome errors due to warm-up drift.

Complementing these excellent input characteristics are dynamic performance characteristics never before available from precision operational amplifiers. An 8V/μs slew rate and 5MHz bandwidth allow the designer to extend precision instrumentation applications in both speed and bandwidth. These characteristics make the HA-5170 well suited for precision integrator amplifier designs.

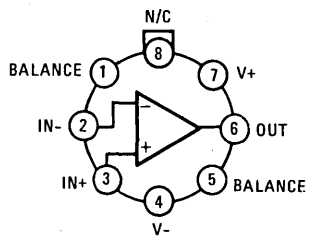
The superior input characteristics also make the HA-5170 ideally suited for transducer signal amplifiers, precision voltage followers and precision data acquisition systems.

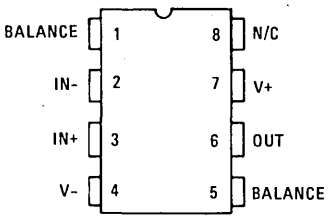
Packaged in an 8-pin (TO-99) can or an 8 lead Minidip, the HA-5170 is pin compatible with most existing op amp configurations.

PINOUT

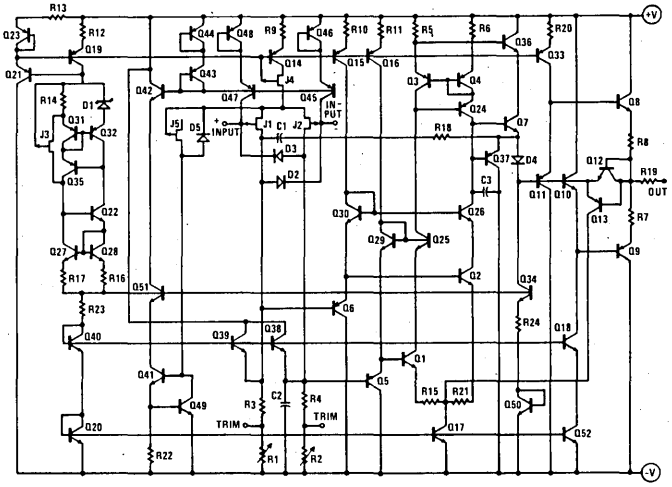
Section 11 for Packaging

TOP VIEW





SCHEMATIC



See Pages 3287-3291 for Package Information.

ABSOLUTE MAXIMUM RATINGS (Note 1)

T_A = +25°C Unless otherwise stated

Voltage Between V+ and V-Terminals	44.0V	Power Dissipation (Note 2)	675mW
Differential Input Voltage	±30.0V	Operating Temperature Range	
		HA-5170-2	$-55^oC \leq T_A \leq +125^oC$
		HA-5170-5	$0^oC \leq T_A \leq +75^oC$
Output Short Circuit Duration	Indefinite	Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS V+ = 15V, V- = -15V

PARAMETER	TEMP.	HA-5170-2 MIN	HA-5170-2 TYP	HA-5170-2 MAX	HA-5170-5 MIN	HA-5170-5 TYP	HA-5170-5 MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		0.1	0.5		0.1	0.5	mV
	Full			1			0.75	mV
Average Offset Voltage Drift	Full		3	5		3	5	µV/°C
Bias Current	+25°C		20	30		20	60	pA
	Full		3	10		0.04	0.1	nA
Bias Current Average Drift	Full						3	pA/°C
Offset Current	+25°C			30			60	pA
	Full			5			0.1	nA
Offset Current Average Drift	Full						1	pA/°C
Common Mode Range	Full	±10			±10			V
Differential Input Resistance	+25°C		6×10^{10}			6×10^{10}		MΩ
Input Noise Voltage (f = 1kHz)	+25°C		12			12		$nV/\sqrt{Hz}$
Input Noise Current (f = 1kHz)	+25°C		0.01			0.01		$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 3)	+25°C	100K			80K			V/V
	Full	80K			50K			V/V
Common Mode Rejection Ratio (Note 4)	Full	100			90			dB
Closed Loop Bandwidth (A_{VCL} = +1)	+25°C		5			5		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 5)	+25°C	±10			±10			V
Full Power Bandwidth (Note 6)	+25°C		110			110		kHz
Output Current (Note 7)	+25°C	±10			±10			mA
Output Resistance (Note 8)	+25°C		45			45		Ω
TRANSIENT RESPONSE								
Rise Time	+25°C		45	100		45	100	ns
Slew Rate	+25°C	5	8		5	8		V/µs
Settling Time (Note 9)	+25°C		1			1		µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full		1.9	2.1		1.9	2.1	mA
Power Supply Rejection Ratio (Note 10)	Full	100			90			dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 6.8 mW/°C for operation at ambient temperatures above +75°C.
3. V_{OUT} = ±10V; R_L = 2k.
4. V_{CM} = ±10V D. C.
5. R_L = 2kΩ.
6. R_L = 2k; Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{SLEW\ RATE}{2\pi V_{PEAK}}$
7. V_{OUT} = 10V.
8. Output resistance measured under open loop conditions (f = 100Hz).
9. Settling time is measured to 0.1% of final value for a 10V output step and A_V = -1.
10. V_{SUPP} = ±5V D. C. to ±20V D. C.

HA-5180/5180A

Low Bias Current, Low Power JFET Input Operational Amplifier

APRIL 1982 **Preliminary**

FEATURES

• ULTRA LOW BIAS CURRENT	250fA
• LOW POWER SUPPLY CURRENT	0.8mA
• LOW OFFSET VOLTAGE	0.5mV (max.)
• BANDWIDTH	2 MHz
• SLEW RATE	7V/ μs

APPLICATIONS

- ELECTROMETER AMPLIFIER DESIGNS
- PHOTO CURRENT DETECTORS
- PRECISION, LONG-TERM INTEGRATORS
- LOW DRIFT SAMPLE & HOLD CIRCUITS
- VERY HIGH IMPEDANCE BUFFERS
- HIGH IMPEDANCE BIOLOGICAL MICRO PROBES

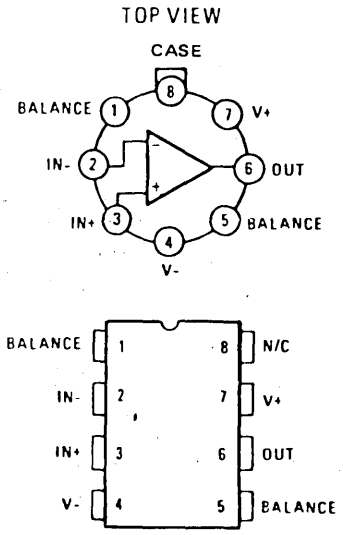
DESCRIPTION

The HARRIS HA-5180/5180A is an ultra low input bias current, JFET input, monolithic operational amplifier which also features low power, low offset voltage and excellent AC characteristics. Employing FET/Bipolar construction coupled with dielectric isolation this operational amplifier offers the lowest input bias currents (250fA typ.) available in any monolithic operational amplifier. The HA-5180/5180A has another unique feature in which the offset bias current may be nulled by externally adjusting the offset voltage. For applications which require precision performance the HA-5180A offers an input offset voltage of 0.5 mV (max) while the HA-5180 offers 3 mV (max.)

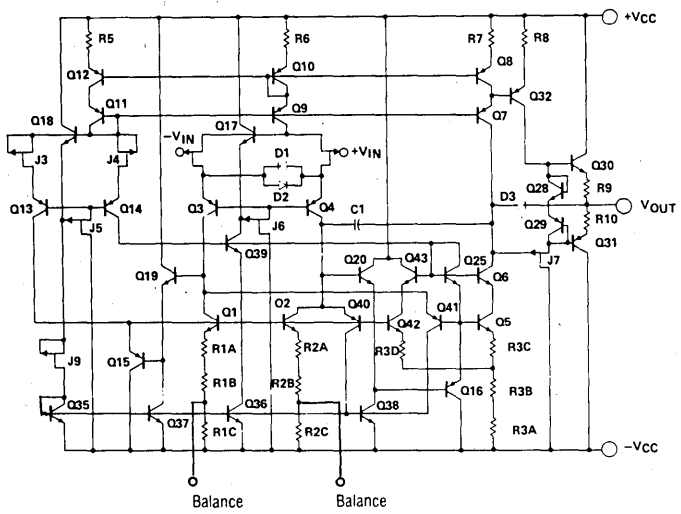
The HA-5180/5180A also offers excellent AC performance not previously available in similar hybrid or monolithic op amp designs. The 2 MHz bandwidth and 7V/μs slew rate of the HA-5180/5180A extends the bandwidth and speed for applications such as very low drift sample and hold amplifiers and photo-current detectors. Other applications include use in electrometer designs, pH/Ion sensitive electrodes, low current oxygen sensors, long term precision integrators and very high impedance buffer measurement designs.

The HA-5180/5180A is packaged in an 8-pin (TO-99) can and an 8-lead cerdip and is pin compatible with most existing op amp configurations. The case of the TO-99 package is internally connected to pin 8 so that it may be connected to the same potential as the input. This feature helps minimize stray leakage to the case, helps shield the amplifier from external noise and reduces common mode input capacitance.

PINOUT



SCHEMATIC



See Pages 3287-3291 for Package Information.

ABSOLUTE MAXIMUM RATINGS (Note 1)

$T_A = +25°C$ Unless otherwise stated

Voltage Between V+ and V− Terminals	40.0V	Power Dissipation (Note 2)	300mW
Differential Input Voltage	±40V	Operating Temperature Range	
		HA-5180/5180A-2	$-55°C \leq T_A \leq +125°C$
		HA-5180/5180A-5	$0°C \leq T_A \leq +75°C$
Output Short Circuit Duration	Indefinite	Storage Temperature Range	$-65°C \leq T_A \leq +150°C$

ELECTRICAL RATINGS V+ = 15V, V− = −15V

PARAMETER	TEMP.	5180A-2 MIN	5180A-2 TYP	5180A-2 MAX	5180A-5 MIN	5180A-5 TYP	5180A-5 MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		**0.1**	0.5		**0.1**	0.5	mV
	Full			1			1	mV
Average Offset Voltage Drift	Full		5			5		µV/°C
Bias Current (Note 3)	+25°C		250	1000		250	1000	fA
	Full		100	500		6	**30**	pA
Offset Current (Note 3)	+25°C		30	200		30	200	fA
	Full		6	30		1	5	pA
Common Mode Range	Full	±10	±12		±10	±12		V
Differential Input Resistance	+25°C		10^{12}			10^{12}		Ω
Input Noise Voltage (f = 1kHz)	+25°C		70			70		$nV/\sqrt{Hz}$
Input Noise Current (f = 1kHz)	+25°C		0.01			0.01		$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 4)	+25°C	200k	1M		200k	1M		V/V
	Full	150k			150k			V/V
Common Mode Rejection Ratio (Note 5)	Full	90	110		90	110		dB
Closed Loop Bandwidth ($A_{VCL} = +1$)	+25°C		2			2		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 6)	+25°C	±10	±12		±10	±12		V
	Full	±10			±10			V
Full Power Bandwidth (Note 7)	+25°C		110			110		kHz
Output Current (Note 8)	+25°C	±10	±15		±10	±15		mA
Output Resistance (Note 9)	+25°C		25			25		Ω
TRANSIENT RESPONSE								
Rise Time	+25°C		75			75		ns
Slew Rate	+25°C	4	7		4	7		V/µs
Settling Time (Note 10)	+25°C		2			2		µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full		0.7	1		0.8	1	mA
Power Supply Rejection Ratio (Note 11)	Full	85	105		85	105		dB

ELECTRICAL RATINGS $V+ = 15V, V- = -15V$

PARAMETER	TEMP.	5180A-2 MIN	5180A-2 TYP	5180A-2 MAX	5180A-5 MIN	5180A-5 TYP	5180A-5 MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		1	3		1	3	mV
	Full			4			4	mV
								mV
								mV
Average Offset Voltage Drift	Full		5			5		μV/°C
Bias Current (Note 3)	+25°C		250	1000		250	1000	fA
	Full		100	500		6	**30**	pA
Offset Current (Note 3)	+25°C		30	200		30	200	fA
	Full		6	30		1	5	pA
Common Mode Range	Full	±10	±12		±10	±12		V
Differential Input Resistance	+25°C		10^{12}			10^{12}		Ω
Input Noise Voltage (f = 1kHz)	+25°C		70			70		$nV/\sqrt{Hz}$
Input Noise Current (f = 1kHz)	+25°C		0.01			0.01		$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 4)	+25°C	200k	1M		200k	1M		V/V
	Full	150k			**150k**			V/V
Common Mode Rejection Ratio (Note 5)	Full	90	110		90	110		dB
Closed Loop Bandwidth ($A_{VCL} = +1$)	+25°C		2			2		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 6)	+25°C	±10	±12		±10	±12		V
	Full	±10			±10			V
Full Power Bandwidth (Note 7)	+25°C		110			110		kHz
Output Current (Note 8)	+25°C	±10	±15		±10	±15		mA
Output Resistance (Note 9)	+25°C		25			25		Ω
TRANSIENT RESPONSE								
Rise Time	+25°C		75			75		ns
Slew Rate	+25°C	4	7		4	7		V/μs
Settling Time (Note 10)	+25°C		2			2		μs
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full		0.7	1		0.8	1	mA
Power Supply Rejection Ratio (Note 11)	Full	85	105		85	105		dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 6.9 mW/°C for operation at ambient temperatures above +75°C.
3. This parameter is guaranteed by design and is not 100% tested.
4. $V_{OUT} = \pm 10V$; $R_L = 2k$. Gain dB = $20 \log_{10} Av$.
5. $V_{CM} = \pm 10V$ D.C.
6. $R_L = 2k$
7. $R_L = 2k$; Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{SLEW\ RATE}{2\pi V_{PEAK}}$
8. $V_{OUT} = \pm 10V$.
9. Output resistance measured under open loop conditions (f = 100Hz)
10. Settling time is measured to 0.1% of final value for a 10V output step and $A_V = -1$.
11. $V_{SUPP} = +5V$ D.C. to ±20V D.C.

HARRIS

HA-5190/5195

Wideband, Fast Settling Operational Amplifier

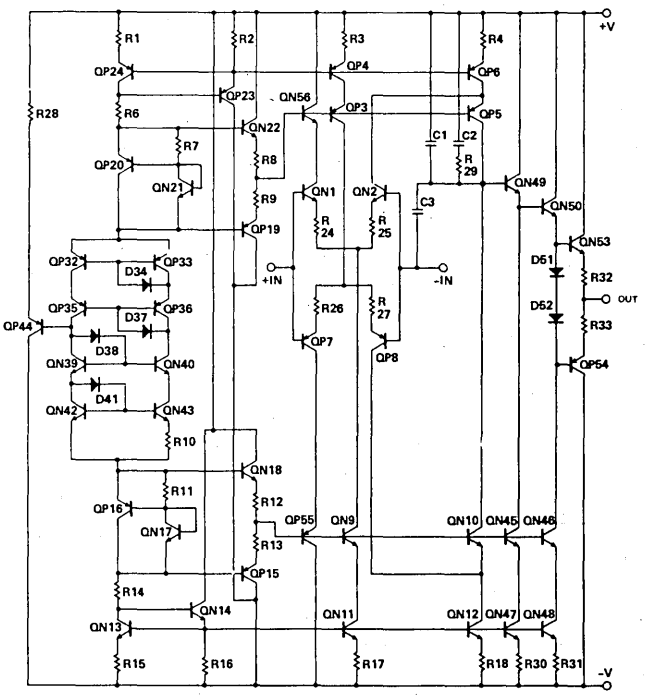
FEATURES

- FAST SETTLING TIME — 70ns
- VERY HIGH SLEW RATE — 200V/μs
- WIDE GAIN-BANDWIDTH — 150MHz
- POWER BANDWIDTH — 6.5MHz
- LOW OFFSET VOLTAGE — 5mV
- INPUT VOLTAGE NOISE — 15nV/$\sqrt{Hz}$
- MONOLITHIC BIPOLAR CONSTRUCTION

APPLICATIONS

- FAST, PRECISE D/A CONVERTERS
- HIGH SPEED SAMPLE-HOLD CIRCUITS
- PULSE AND VIDEO AMPLIFIERS
- WIDEBAND AMPLIFIERS
- REPLACE COSTLY HYBRIDS

SCHEMATIC



GENERAL DESCRIPTION

HA-5190/5195 are monolithic operational amplifiers featuring an ultimate combination of speed, precision, and bandwidth. Employing monolithic bipolar construction coupled with dielectric isolation, these devices are capable of delivering an unparalleled 200V/μs slew rate with a settling time of 70ns (0.1%, 5V output step). These truly differential amplifiers are designed to operate at gains ≥ 5 without the need for external compensation. Other outstanding HA-5190/5195 features are 150MHz gain-bandwidth-product and 6.5MHz full power bandwidth. In addition to these dynamic characteristics, these amplifiers also have excellent input characteristics such as 5mV offset voltage and 15nV input voltage noise (at 1kHz).

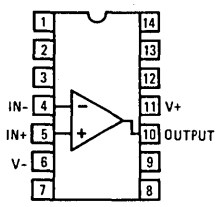
With 200V/μs slew rate and 70ns settling time, these devices make ideal output amplifiers for accurate, high speed D/A converters or the main components in high speed sample/hold circuits. 150MHz gain-bandwidth-product, 6.5MHz power bandwidth, and 5mV offset voltage make HA-5190/5195 ideally suited for a variety of pulse and wideband video amplifier applications.

At temperatures above +75°C, a heat sink is required for HA-5190. (See note 2). HA-5190 is specified over the -55°C to +125°C range while HA-5195 is specified from 0°C to +75°C.

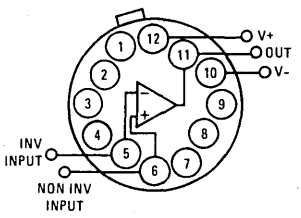
PINOUTS

Section 11 for Packaging

TOP VIEW



TOP VIEW



CASE TIED TO V-

LH0032 PINOUT

LINEAR

Harris Semiconductor

See Pages 3287-3291 for Package Information.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage between V+ and V- Terminals	35V
Differential Input Voltage	6V
Output Current	50mA (Peak)
Internal Power Dissipation (Note 2)	870mW (Cerdip); 1W (TO-8) Free Air
Operating Temperature Range: (HA-5190)	$-55^{o}C \leq T_A \leq +125^{o}C$
(HA-5195)	$0^{o}C \leq T_A \leq +75^{o}C$
Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS $V_{SUPPLY} = \pm 15$ Volts; R_L = 1K ohms, unless otherwise specified.

		HA-5190 -55°C to +125°C			HA-5195 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		3.0	5.0		3.0	6	mV
	FULL			10.0			10.0	mV
Average Offset Voltage Drift	FULL		20			20		µV/°C
Bias Current	+25°C		5	15		5	15	µA
	FULL			20			20	µA
Offset Current	+25°C		1	4		1	4	µA
	FULL			6			6	µA
Input Resistance	+25°C		10			10		Kohms
Input Capacitance	+25°C		1.0			1.0		pF
Common Mode Range	FULL	±5			±5			V
Input Noise Voltage (f = 1kHz, R_g = 0Ω)	+25°C		15			15		nV/√Hz
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 3)	+25°C	15K	30K		10K	30K		V/V
	FULL	5K			5K			V/V
Common-Mode Rejection Ratio (Note 4)	FULL	74			74			dB
Gain-Bandwidth-Product (Notes 5 & 6)	+25°C		150			150		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 3)	FULL	±5	±8		±5	±8		V
Output Current (Note 3)	+25°C	25	30		25	30		mA
Output Resistance	+25°C		30			30		Ohms
Full Power Bandwidth (Note 3 & 7)	+25°C	5	6.5		5	6.5		MHz
TRANSIENT RESPONSE (Note 8)								
Rise Time	+25°C		13	18		13	18	ns
Overshoot	+25°C		8			8		%
Slew Rate	+25°C	160	200		160	200		V/µs
Settling Time:								
5V Step to 0.1%	+25°C		70			70		ns
5V Step to 0.01%	+25°C		100			100		ns
2.5V Step to 0.1%	+25°C		50			50		ns
2.5V Step to 0.01%	+25°C		80			80		ns
POWER REQUIREMENTS								
Supply Current	FULL		19	28		19	28	mA
Power Supply Rejection Ratio (Note 9)	FULL	70	90		70	90		dB

HARRIS

HA-5320

High Speed Precision Monolithic Sample and Hold Amplifier

JULY 1982

FEATURES

- GAIN, dc — 2×10^6 V/V
- ACQUISITION TIME — 1.0 µs (0.01%)
- DROOP RATE — 0.08 µV/µs (25°C); 17 µV/µs (FULL TEMP)
- APERTURE TIME — 25ns
- PEDESTAL ERROR — 1.0 mV
- INTERNAL HOLD CAPACITOR
- FULLY DIFFERENTIAL INPUT
- TTL COMPATIBLE

APPLICATIONS

- PRECISION DATA ACQUISITION SYSTEMS
- D/A CONVERTER DEGLITCHING
- AUTO-ZERO CIRCUITS
- PEAK DETECTORS

DESCRIPTION

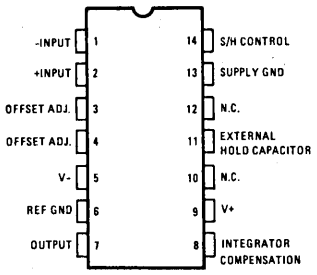
The HA-5320 was designed for use in precision, high speed data acquisition systems.

The circuit consists of an input transconductance amplifier capable of providing large amounts of charging current, a low leakage analog switch, and an output integrating amplifier. The analog switch sees virtual ground as its load; therefore, charge injection on the hold capacitor is constant over the entire input/output voltage range. The pedestal voltage resulting from this charge injection can be adjusted to zero by use of the offset adjust inputs. The device includes a hold capacitor. However, if improved droop rate is required at the expense of acquisition time, additional hold capacitance may be added externally.

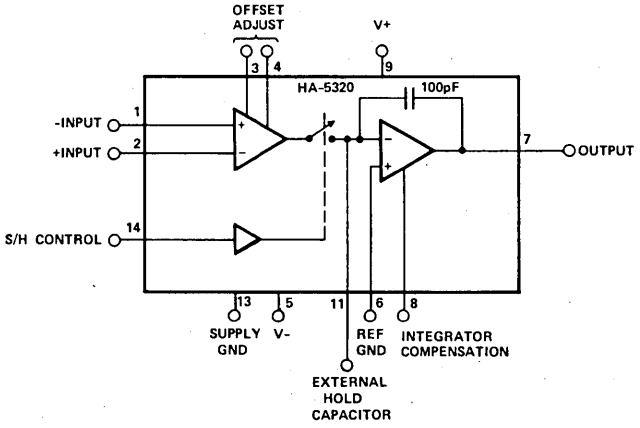
This monolithic device is manufactured using the Harris dielectric isolation process, minimizing stray capacitance and eliminating SCR's. This allows higher speed and latch-free operation. The HA-5320 requires ±15V, and is available in a ceramic or plastic 14-pin DIP.

PINOUT

TOP VIEW



FUNCTIONAL DIAGRAM



LINEAR

Harris Semiconductor

See Pages 3287-3291 for Package Information.

ABSOLUTE MAXIMUM RATINGS

Voltage between V^+ and V^- terminals	40V	Internal Power Dissipation	450mW (Note 2)
Differential Input Voltage	±24V	Operating Temperature Range	
Digital Input Voltage (Pin 14)	+8V, −15V	HA-5320-2/8	$-55^oC \leq TA \leq +125^oC$
Output Current, continuous	±20mA (Note 1)	HA-5320-5	$0^oC \leq TA \leq +75^oC$
		Storage Temperature Range	$-65^oC \leq TA \leq +150^oC$

ELECTRICAL CHARACTERISTICS Test Conditions (unless otherwise specified)

V Supply = ±15V; C_H - Internal; Digital Input (Pin 14), V_{AL} = +0.8V (sample), V_{AH} = +2.0V (hold).

PARAMETER	TEMP	HA-5320-2/8 MIN	HA-5320-2/8 TYP	HA-5320-2/8 MAX	HA-5320-5 MIN	HA-5320-5 TYP	HA-5320-5 MAX	UNITS
INPUT CHARACTERISTICS								
Input Voltage Range	Full	±10			±10			V
Input Resistance	25°C	1	5		1	5		MΩ
Input Capacitance	25°C			3			3	pF
Offset Voltage	25°C		0.2	0.5		0.5	1.0	mV
	Full			2.0			1.5	mV
Bias Current	25°C		70	200		100	300	nA
	Full			200			300	nA
Offset Current	25°C		30	100		30	300	nA
	Full			100			300	nA
Common Mode Range	Full	±10			±10			V
CMRR (Note 3)	25°C	80	90		72	90		dB
Offset Voltage T.C.	Full		5	15		5	20	µV/°C
TRANSFER CHARACTERISTICS								
Gain, dC	25°C	10^6	$2x10^6$		$3x10^5$	$2x10^6$		V/V
Gain Accuracy, Av = +1	25°C		$.5x10^{-4}$			$.5x10^{-4}$		%FSR
Gain Accuracy, T.C.	Full		±.6			±.6		ppm/°C
Gain Bandwidth Product	25°C							
(Note 4, 5) CH = 100pF			2.0			2.0		MHz
CH = 1000pF			.18			.18		MHz
OUTPUT CHARACTERISTICS								
Output Voltage	Full	±10			±10			V
Output Current	25°C	±10			±10			mA
Full Power Bandwidth (Note 4, 6)	25°C		600			600		KHz
Output Resistance (Hold mode)	25°C		1.0			1.0		Ω
Total Output Noise, DC to 10 MHz								
Sample	25°C		125	200		125	200	µV RMS
Hold	25°C		125	200		125	200	µV RMS

PARAMETER	TEMP	HA-5320-2/8 MIN	HA-5320-2/8 TYP	HA-5320-2/8 MAX	HA-5320-5 MIN	HA-5320-5 TYP	HA-5320-5 MAX	UNITS
TRANSIENT RESPONSE								
Rise Time	25°C		100			100		nS
Overshoot	25°C		15			15		%
Slew Rate (Note 7)	25°C		45			45		V/µs
DIGITAL INPUT CHARACTERISTICS								
Input Voltage (High), V_{AH}	Full	2.0			2.0			V
Input Voltage (Low), V_{AL}	Full			0.8			0.8	V
Input Current (V_{AL} = 0V)	Full			4			4	µA
Input Current (V_{AH}= +5V)	Full			0.1			0.1	µA
SAMPLE/HOLD CHARACTERISTICS								
Acquisition Time (.1%) (Note 7)	25°C		.8			.8		µS
Acquisition Time (.01%) (Note 7)	25°C		1.0			1.0		µS
Aperture Time	25°C		25			25		nS
Aperture Delay Time	25°C		30			30		nS
Aperture Uncertainty	25°C		1			1		nS
Droop Rate	25°C		.08			.08		µV/us
Droop Rate	Full		17			1.2		µV/us
Drift Current (Note 8)	25°C		8			8		pA
Drift Current (Note 8)	Full		1.7			.12		nA
Charge Transfer (Note 8)	25°C		0.1			0.1		pC
Hold Mode Settling Time (.01%)	Full		185			185		nS
Hold Mode Feedthrough (10Vp-p, 100KHz)	Full		2			2		mV
POWER SUPPLY CHARACTERISTICS								
Positive Supply Voltage	Full	+14.5	+15	+16	+14.5	+15	+16	V
Negative Supply Voltage	Full	−14.5	−15	−16	−14.5	−15	−16	V
Positive Supply Current	25°C		11	13		11	13	mA
Negative Supply Current	25°C		−11	−13		−11	−13	mA
Power Supply Rejection V^+	Full	80			80			dB
(Note 9) V^-	Full	65			65			dB

NOTES:
1. Internal Power Dissipation may limit Output Current below +20 mA.
2. Derate power dissipation by 4.3 mW/°C above 105°C ambient.
3. Vcm = +5VDC
4. A_V = +1; R_L = 1KΩ ; C_L = 50pF
5. V_O = 100mVpp.
6. V_O = 20Vpp.
7. V_O = 10V step.
8. V_{in} = OV, V_{AH} = +3.5V, t_r < 50ns (V_{AL} to V_{AH}).
9. Based on a one volt delta in each supply, ie: 15V ± 0.5VDC.

WARNING: This device cannot tolerate even a momentary short circuit to ground or either supply.

The HA-5320 has the uncommitted differential inputs of an op amp, allowing the Sample/Hold function to be combined with many conventional op amp circuits. See Harris' Application Note #AN517 for a collection of circuit ideas. (Note, however, these apply to a different Sample/Hold amplifier. The HA-5320 is not necessarily plug-in compatible.)

LAYOUT

A printed circuit board with ground plane is recommended for best performance. Bypass capacitors (.01 to 0.1μF, ceramic) should be provided from each power supply terminal to the Power Gnd terminal on pin 13.

The ideal ground connections are pin 6 (Reference Ground) directly to the system Signal Ground, and pin 13 (Supply Ground) directly to the system Supply Common.

HOLD CAPACITOR

The HA-5320 includes a 100 pF MOS hold capacitor, sufficient for most high speed applications (the Electrical Characteristics section is based on this internal capacitor). Additional capacitance may be added between pins 7 and 11. This external hold capacitance will reduce droop rate at the expense of acquisition time, and provide other trade-offs as shown in the Performance Curves.

If an external hold capacitor C_H is used, then a noise bandwidth capacitor of value $0.1C_H$ should be connected from pin 8 to ground. Exact value and type are not critical.

The hold capacitor C_H should have high insulation resistance and low dielectric absorption, to minimize droop errors. Polystyrene dielectric is a good choice for operating temperatures up to +85°C. Teflon and glass dielectrics offer good performance to +125°C and above.

The hold capacitor terminal (pin 11) remains at virtual ground potential. Any PC connection to this terminal should be kept short and "guarded" by the ground plane, since nearby signal lines or power supply voltages will introduce errors due to drift current.

POWER SUPPLIES

The HA-5320 is designed for operation with ±15V supplies, and these levels should be maintained within ±0.5V. It will not function properly with ±12V supplies.

APPLICATIONS

Figure 6 shows the HA-5320 connected as a unity gain noninverting amplifier – its most widely used configuration. As an input device for a fast successive – approximation A/D converter, it offers the highest throughput rate available from a monolithic IC sample/hold amplifier. Also, the HA-5320's pedestal error is adjustable to zero using the Offset Adjust potentiometer, to deliver a 12 bit accurate output from the converter.

The application may call for an external hold capacitor C_H as shown. As mentioned earlier, $0.1C_H$ is then required at pin 8 to maintain stability in the output buffer. The RC network on pin 14 introduces a delay to insure that the sample-to-hold transient has settled before a conversion begins.

The HA-5320 output circuit does not include short circuit protection, and consequently its output impedance remains low at high frequencies. Thus, the step changes in load current which occur during an A/D conversion are absorbed at the S/H output with minimum voltage error. However, the unprotected output cannot tolerate even a brief short circuit to ground or either supply.

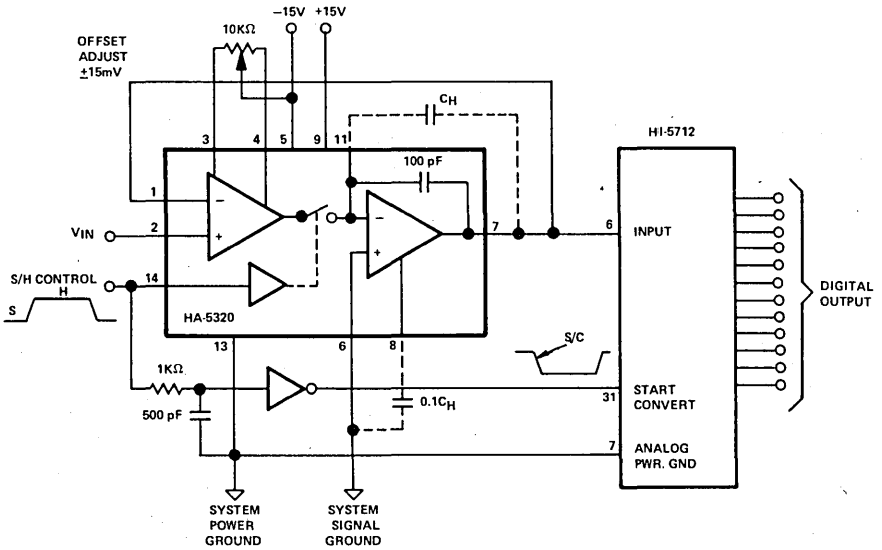
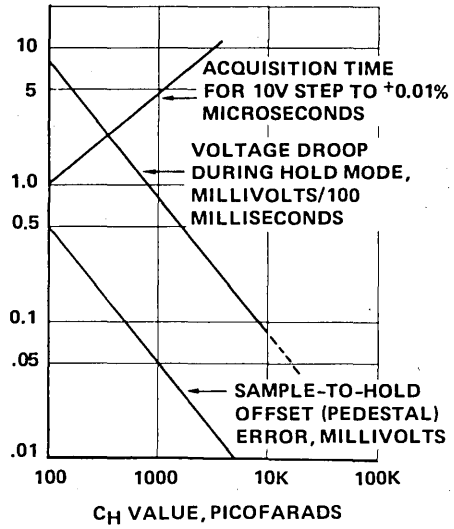


Figure 6

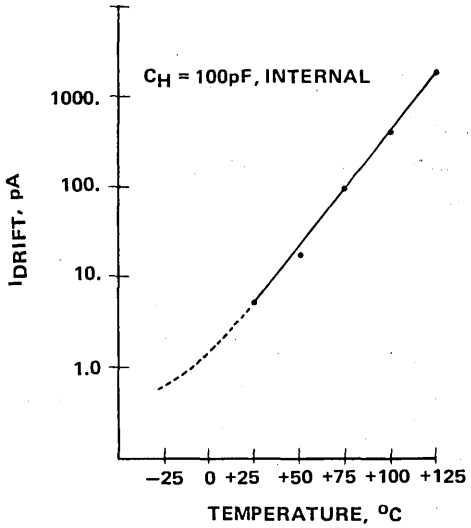
TYPICAL HA-5320 CONNECTIONS; NONINVERTING UNITY GAIN MODE.

V_{SUPPLY} = ±15VDC

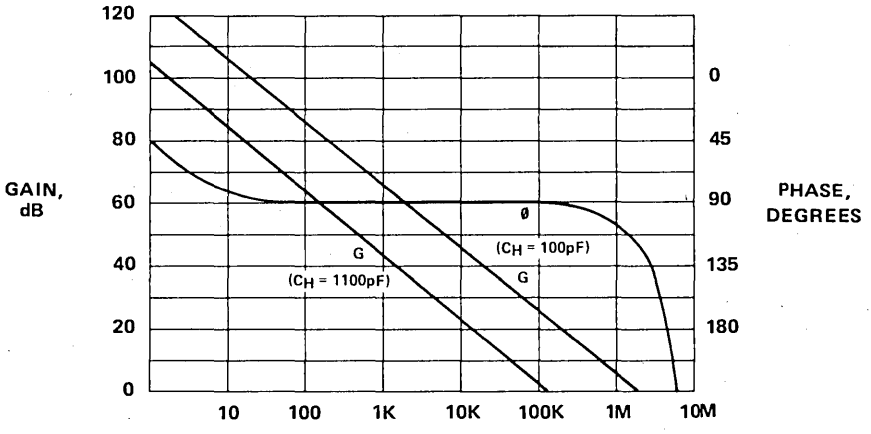
TYPICAL SAMPLE AND HOLD PERFORMANCE AS FUNCTION OF HOLDING CAPACITOR



DRIFT CURRENT VS. TEMPERATURE

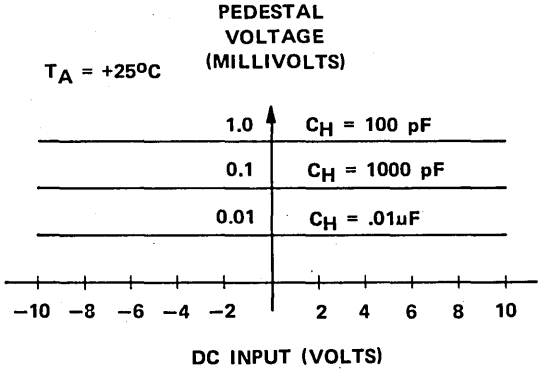


OPEN LOOP GAIN AND PHASE RESPONSE

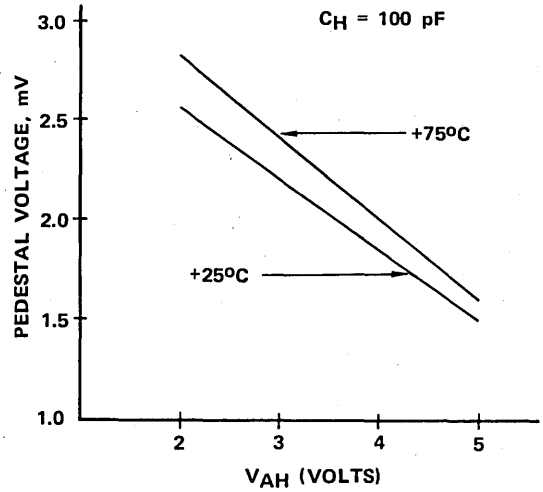


TYPICAL SAMPLE-TO-HOLD OFFSET (PEDESTAL) ERROR

PEDESTAL VS. INPUT VOLTAGE



PEDESTAL VS. LOGIC (V_{AH}) VOLTAGE



HARRIS

HA-8023

Triple Low Power Programmable Operational Amplifier

Preliminary

FEATURES

- LOW INPUT OFFSET VOLTAGE (MAX) 3mV
- LOW INPUT BIAS CURRENT (MAX) 30nA
- WIDE POWER SUPPLY RANGE ±2V TO ±18V
- INTERNALLY COMPENSATED

APPLICATIONS

- BATTERY-POWERED EQUIPMENT
- CURRENT CONTROLLED OSCILLATORS
- ACTIVE FILTERS
- VARIABLE ACTIVE FILTERS

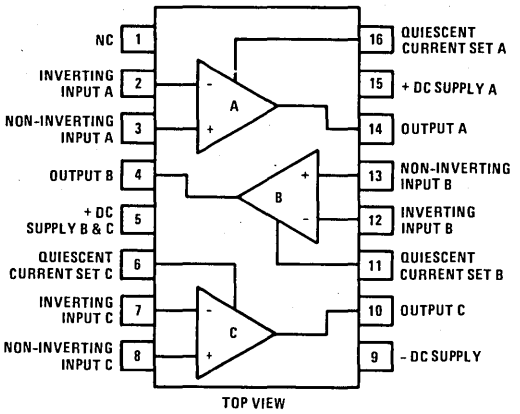
DESCRIPTION

The HA-8023 triple programmable amplifiers are internally compensated, monolithic devices which offer a wide range of performance characteristics that can be controlled by adjusting the circuits' "SET" current. Each amplifier on the chip can be adjusted independently, and by adjusting an external resistor or current source, the electrical characteristics can be programmed to the desired levels. This versatile adjustment capability enables the HA-8023 to provide optimum design solutions by delivering the required level of performance with minimum power dissipation.

The HA-8023-2 performance specifications are guaranteed over the -55°C to +125°C temperature range and the HA-8023-5 over the 0°C to +75°C temperature range.

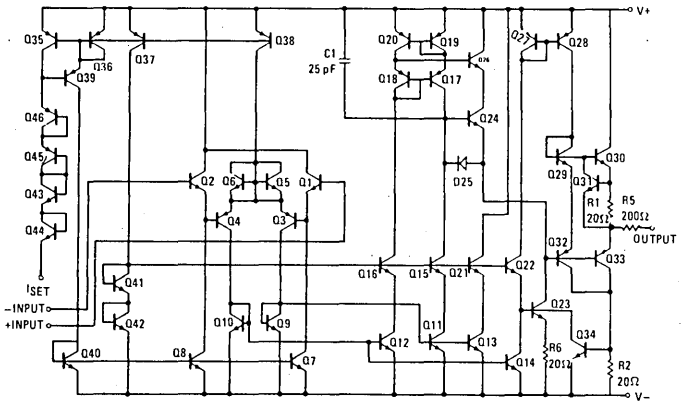
PINOUT

Section 11 for Packaging



TOP VIEW

SCHEMATIC



See Pages 3287-3291 for Package Information.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V-	±22V
Differential Input Voltage	±15V
Input Voltage (Note 2)	±15V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation	300mW
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS $V_S = \pm 6V$, $I_Q = 30\mu A$, unless otherwise specified I_Q = Quiescent Supply Current

		HA-8023-2 -55°C to +125°C			HA-8023-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage (Note 3)	+25°C		2	3.0		2	6	mV
	Full		2	4		2	7.5	mV
Offset Voltage Average Drift	Full		5			5		µV/°C
Bias Current	+25°C		3	30		3	30	nA
	Full		5	50		5	50	nA
Offset Current	+25°C		3	10		3	10	nA
	Full		1	15		1	15	nA
Input Resistance	+25°C	3	10		3	10		MΩ
Input Voltage Range (Note 4)	+25°C	±12	±13		±12	±13		V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 5)	Full	5K	10K		5K	10K		V/V
Channel Separation (Note 6)	+25°C		105			105		dB
Common Mode Rejection Ratio (Note 7)	+25°C	70	100		70	100		dB
Unity Gain Bandwidth (Note 8)	+25°C		270			270		kHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 9)	+25°C	±11	±13		±11	±13		V
	Full	±10	±13		±10	±13		V
Output Voltage Swing (Note 10)	+25°C	±12	±14		±12	±14		V
Output Voltage Swing (Note 11)	+25°C	±4	±5		±4	±5		V
	Full	±4	±5		±4	±5		V
Output Short Circuit Current	+25°C		±4			±4		mA
Full Power Bandwidth (Note 12)	+25°C		3.5			3.5		kHz
Output Resistance	+25°C		2			2		KΩ
TRANSIENT RESPONSE (Note 13)								
Rise Time	+25°C		700			700		ns
Slew Rate	+25°C		.1			.1		V/µs
Overshoot	+25°C		12			12		%
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		30	40		30	50	µA
Power Consumption (Note 14)	+25°C		360	480		360	600	µW
Power Supply Rejection Ratio (Note 15)	+25°C	76	100		76	100		dB

HARRIS

HA-4900/02/05

Precision Quad Comparator

FEATURES

- FAST RESPONSE TIME 130ns
- LOW OFFSET VOLTAGE 2.0mV
- LOW OFFSET CURRENT 10nA
- SINGLE OR DUAL-VOLTAGE SUPPLY OPERATION
- SELECTABLE OUTPUT LOGIC LEVELS
- ACTIVE PULL-UP/PULL-DOWN OUTPUT CIRCUIT - NO EXTERNAL RESISTORS REQUIRED

APPLICATIONS

- THRESHOLD DETECTOR
- ZERO-CROSSING DETECTOR
- WINDOW DETECTOR
- ANALOG INTERFACES FOR MICROPROCESSORS
- HIGH STABILITY OSCILLATORS
- LOGIC SYSTEM INTERFACES

DESCRIPTION

The HA-4900 series are monolithic, quad, precision comparators offering fast response time, low offset voltage, low offset current, and virtually no channel-to-channel crosstalk for applications requiring accurate, high speed, signal level detection. These comparators can sense signals at ground level while being operated from either a single +5 volt supply (digital systems) or from dual supplies (analog networks) up to ±15 volts. The HA-4900 series contains a unique current driven output stage which can be connected to logic system supplies (V_{Logic}+ and V_{Logic}-) to make the output levels directly compatible (no external components needed) with any standard logic or special system logic levels. In combination analog/digital systems, the design employed in the HA-4900 series input and output stages prevents troublesome ground coupling of signals between analog and digital portions of the system.

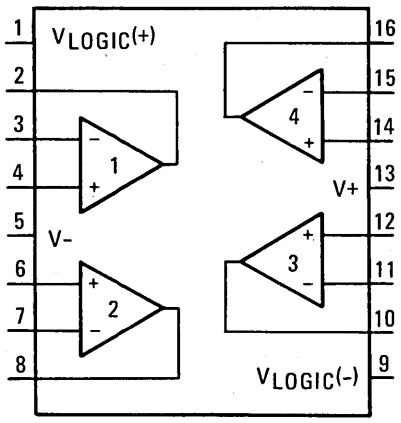
These comparators' combination of features makes them ideal components for signal detection and processing in data acquisition systems, test equipment, and microprocessor/analog signal interface networks.

All devices are available in 16 pin dual-in-line ceramic packages. The HA-4900/4902-2 operates from -55°C to +125°C and the HA-4905-5 operates over a 0°C to +75°C temperature range.

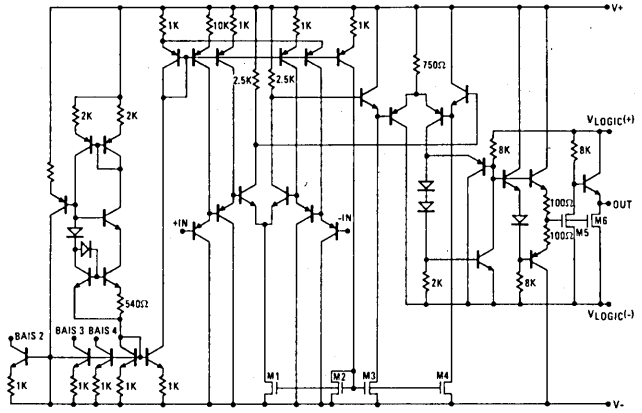
PINOUT

Section 11 for Packaging

Top View



SCHEMATIC



ONE FOURTH ONLY (HA-4900 SERIES)

See Pages 3287-3291 for Package Information.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V-	33V
Voltage Between V_{Logic}(+) and V_{Logic}(-)	18V
Differential Input Voltage	±15V
Peak Output Current	±50mA
Internal Power Dissipation (Note 7, 8)	880mW
Storage Temperature Range	$-65^oC \leq T_A \leq 150^oC$

ELECTRICAL CHARACTERISTICS V+ = +15.0V, V- = -15.0V, V_{Logic}(+) = 5.0V, V_{Logic}(-) = GND.

PARAMETER	TEMP	HA-4900-2 -55°C to +125°C			HA-4902-2 -55°C to +125°C			HA-4905-5 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage (Note 2)	25°C		2	3		2	5		4	7.5	mV
	Full			4			8			10	mV
Offset Current	25°C		10	25		10	35		25	50	nA
	Full			35			35			70	nA
Bias Current (Note 3)	25°C		50	75		50	150		100	150	nA
	Full			150			200			300	nA
Input Sensitivity (Note 4)	25°C			Vio +.3			Vio +.5			Vio +.5	mV
	Full			Vio +.4			Vio +.6			Vio +.7	mV
Common Mode Range	Full	V-		V+ -2.4	V-		V+ +2.4	V-		V+ +2.4	V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain	25°C		400K			400K			400K		V/V
Response Time ($T_{pd}0$) (Note 5)	25°C		130	200		130	200		130	200	ns
Response Time ($T_{pd}1$) (Note 5)	25°C		180	215		180	215		180	215	ns
OUTPUT CHARACTERISITICS											
Output Voltage Level											
Logic "Low State" (V_{OL}) (Note 6)	Full		0.2	0.4		0.2	0.4		0.2	0.4	V
Logic "High State" (V_{OH}) (Note 6)	Full	3.5	4.2		3.5	4.2		3.5	4.2		V
Output Current											
I_{Sink}	Full	3.0			3.0			3.0			mA
I_{Source}	Full	3.0			3.0			3.0			mA
POWER SUPPLY CHARACTERISTICS											
Supply Current, I_{ps} (+)	25°C		6.5	20		6.5	20		7	20	mA
Supply Current , I_{ps} (-)	25°C		4	8		4	8		5	8	mA
Supply Current, I_{ps} (Logic)	25°C		2.0	4		2.0	4		2.0	4	mA
Supply Voltage Range											
V_{Logic} (+) (Note 7)	Full	0		+15.0	0		+15.0	0		+15.0	V
V_{Logic} (-) (Note 7)	Full	-15.0		0	-15.0		0	-15.0		0	V

Harris Selection Guide to Industry Standard Operational Amplifiers

LM108/LM308*
LM118/LM318*
LM143/LM343*
LM146/LM346
LM148/LM348*
LM1458/LM1558*
LM4250/LM4250C
LF155 Series
LF156 Series
LF157 Series
LF347
OP 07

*Harris also offers these product types with improved electrical specifications. Improved versions are identified by an "A" suffix, i.e. LM143A/LM343A.

Harris Analog Package Selection Guide

PART NO.	PACKAGE CONFIGURATION (See Note)				
	CAN	PLASTIC	CERDIP	SIDE BRAZE	LEADLESS CHIP CARRIER
HA-1608	R	G	L		
HA-2400/04/05				B	
HA-2420/25		H	D		X
HA-2500/02/05	R	G	L		
HA-2510/12/15	R	G	L		
HA-2520/22/25	R	G	L		
HA-2530/35	R				
HA-2539		H	D		X
HA-2540		H	D		
HA-2600/02/05	R	G	L		
HA-2620/22/25	R	G	L		
HA-2630/35	V				
HA-2640/45	R		L		
HA-2650/55	R	G	L		
HA-2720/25	R		L		
HA-2730/35			D		
HA-2740		J	E		
HA-4156		H	D		
HA-4600/02/05		H	D		
HA-4620/22/25		H	D		
HA-4741		H	D		X
HA-4900/02/05			E		X
HA-5062	R	G	L		
HA-5064		H	D		
HA-5082	R	G	L		
HA-5084		H	D		
HA-5100/05	R	G	L		
HA-5102/5112		G	L		
HA-5104/5114		H	D		X
HA-5107E	R	G	L		
HA-5110/15	R	G	L		
HA-5130/35	R	G	L		X
HA-5160/62	R				
HA-5170	R	G	L		X
HA-5180	R	G	L		
HA-5190/95	V		D		
HA-8023		J	E		
HC-5502			M		
HC-5510			M		
HC-5511		*			
HC-5512/5512A			E		
HC-55516				A	
HD-0165			M		
HI-200	T	H	D		
HI-201		J	E		X
HI-201HS		J	E		
HI-300/301/304/305	T	H	D		

NOTE: "Package Configuration" references drawings on the following pages. Package designations to be used in constructing the part number are explained in the Ordering Information in the Part number guide.

Plastic DIP packages are not available for military temperature range.

Consult factory for information on ordering and availability of products with package configurations other than those indicated in the chart.

Solder-dipped parts add +0.003 inches to "dimension B" in plastic DIP and "dimension G" in metal cans.

* Contact factory for packaging.

PART NO.	PACKAGE CONFIGURATION (See Note)				
	CAN	PLASTIC	CERDIP	SIDE BRAZE	LEADLESS CHIP CARRIER
HI-302/303/306/307		H	D		
HI-381/384/387/390					
381/387	T	J	E		
384/390		J	E		
HI-506/507		P	N		Y
HI-506A/507A		P	N		Y
HI-508/509		J	E		X
HI-508A/509A		J	E		X
HI-516		P	N		Y
HI-518		K	F		
HI-524		K	F		
HI-539		J	E		
HI-562A				C	Y
HI-1818A/1828A		J	E		
HI-5040 thru 5051		J	E		
HI-5043/5045			E		X
HI-5610				C	
HI-5618A/18B		K	F		
HI-5712/12A	(MC) LCC's on Ceramic Substrate				
HI-5900	(MB) LCCs on Ceramic Substrate				
HI-5901	(MB) LCCs on Ceramic Substrate				
HI-7541		K		Z	X
HV-1000/05/10		J			
LF353	R	G	L		
LF155/155A/355/355A/355B	R	G	L		
LF156/156A/356/356A/356B	R	G	L		
LF157/157A/357/357A/357B	R	G	L		
LF347		D	H		
LM108/308	R	G	L		
LM108A/308A	R	G	L		
LM118/318	R	G	L		
LM118A/318A	R	G	L		
LM143/343	R	G	L		
LM143A/343A	R	G	L		
LM146/346		J	E		
LM148/348		H	D		
LM148A/348A		H	D		
LM1458/1558A	R	G	L		
LM2908		H	D		
LM4250/4250C	R	G	L		
OP-07	R	G	L		

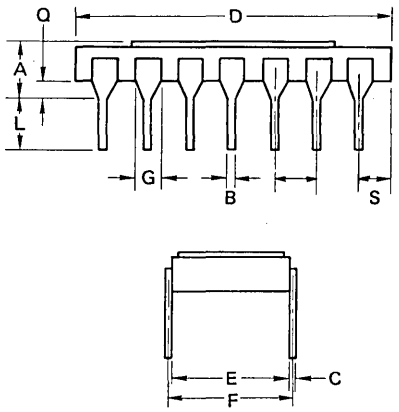
NOTE: "Package Configuration" references drawings on the following pages. Package designations to be used in constructing the part number are explained in the Ordering Information in the Part number guide.

Plastic DIP packages are not available for military temperature range.

Consult factory for information on ordering and availability of products with package configurations other than those indicated in the chart.

Solder-dipped parts add +0.003 inches to "dimension B" in plastic DIP and "dimension G" in metal cans.

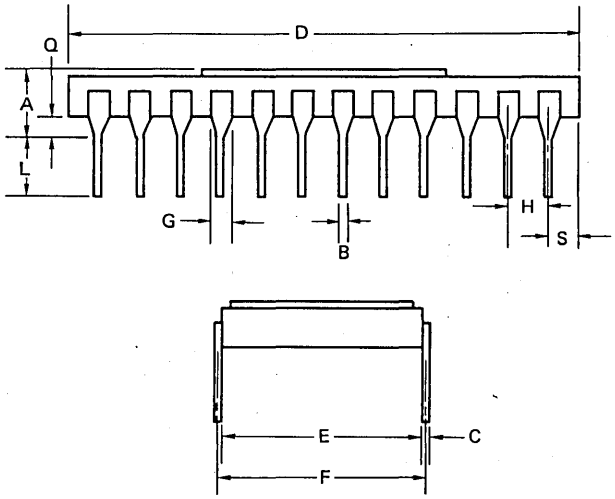
A B Z D TYPE SIDE BRAZED CERAMIC



PKG. TYPE	LEAD COUNT	DIM. A	DIM. B	DIM. C	DIM. D	DIM. E	DIM. F	DIM. G	DIM. H	DIM. L	DIM. Q	DIM. S
A	14	– / .200	.014 / .023	.008 / .015	– / .785	.220 / .310	.290 / .320	.030 / .070	.100 BSC	.125 / .200	.015 / .060	– / .098
B	16	– / .200	.014 / .023	.008 / .015	– / .840	.220 / .310	.290 / .320	.030 / .070	.100 BSC	.125 / .200	.015 / .060	– / .098
Z	18	– / .200	.014 / .023	.008 / .015	– / .950	.220 / .310	.290 / .320	.030 / .070	.100 BSC	.125 / .200	.015 / .060	– / .098

NOTE: MIN. / MAX. DIMENSIONS IN INCHES

C D TYPE SIDE BRAZED CERAMIC



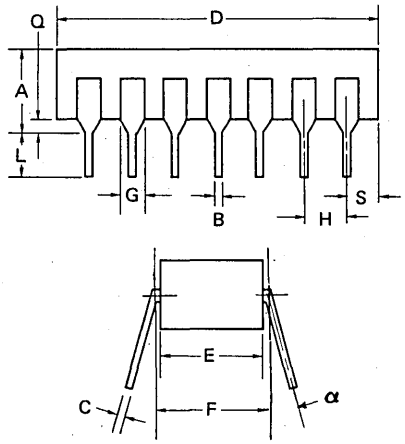
PKG. TYPE	LEAD COUNT	DIM. A	DIM. B	DIM. C	DIM. D	DIM. E	DIM. F	DIM. G	DIM. H	DIM. L	DIM. Q	DIM. S
C	24	– / .225	.014 / .023	.008 / .015	– / 1.290	.500 / .610	.590 / .620	.030 / .070	.100 BSC	.120 / .200	.015 / .075	– / .098

NOTE: MIN. / MAX. DIMENSIONS IN INCHES

D E F J TYPE CERDIP DUAL-IN-LINE

G H J K N TYPE PLASTIC DUAL-IN-LINE

L J-8 TYPE 8 PIN MINI-CERDIP

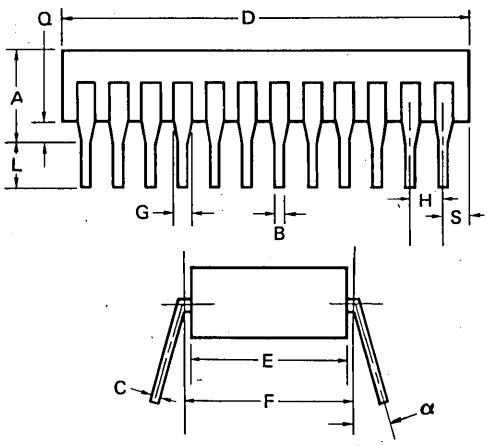


PKG. TYPE	LEAD COUNT	DIM. A	DIM. B	DIM. C	DIM. D	DIM. E	DIM. F	DIM. G	DIM. H	DIM. L	DIM. Q	DIM. S	DIM. α
G, L	8	– / .200	.014 / .023	.008 / .015	– / .395	.220 / .310	.290 / .320	.030 / .070	.100 BSC	.125 / .200	.015 / .060	– / .060	0° / 15°
D, H	14	– / .200	.014 / .023	.008 / .015	– / .790	.220 / .310	.290 / .320	.030 / .070	.100 BSC	.125 / .200	.015 / .060	– / .098	0° / 15°
E, J	16	– / .200	.014 / .023	.008 / .015	– / .790	.220 / .310	.290 / .320	.030 / .070	.100 BSC	.125 / .200	.015 / .060	– / .060	0° / 15°
F, K	18	– / .200	.014 / .023	.008 / .015	– / .950	.220 / .310	.290 / .320	.030 / .070	.100 BSC	.125 / .200	.015 / .060	– / .060	0° / 15°

NOTE: MIN. / MAX. DIMENSIONS IN INCHES

M N J TYPE CERDIP DUAL-IN-LINE

P N TYPE PLASTIC DUAL-IN-LINE

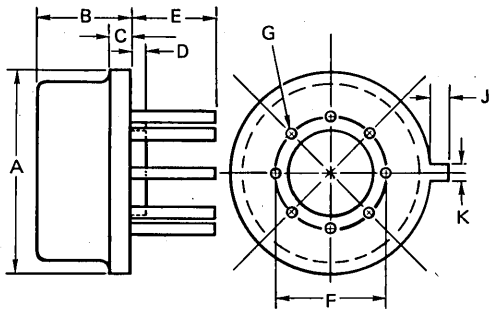


PKG. TYPE	LEAD COUNT	DIM. A	DIM. B	DIM. C	DIM. D	DIM. E	DIM. F	DIM. G	DIM. H	DIM. L	DIM. Q	DIM. S	DIM. α
M	24	– .225	.014 .023	.008 .015	– 1.290	.500 .610	.590 .620	.030 .070	.100 BSC	.120 .200	.015 .075	– .098	0° 15°
N, P	28	– .225	.014 .023	.008 .015	– 1.490	.500 .610	.590 .620	.030 .070	.100 BSC	.120 .200	.015 .075	– .098	0° 15°

NOTES: MIN./MAX.

DIMENSIONS IN INCHES

R T H TYPE METAL CAN, TO-99 (8 PIN) OR TO-100 (10 PIN)

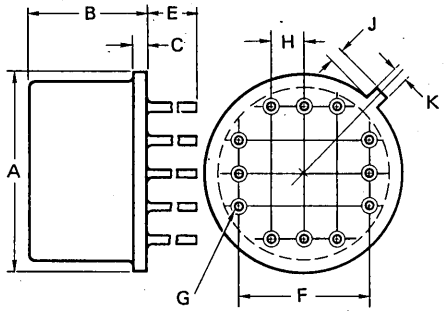


PKG. TYPE	LEAD COUNT	DIM. A	DIM. B	DIM. C	DIM. D	DIM. E	DIM. F	DIM. G	DIM. J	DIM. K
R	8	.335 .370	.165 .185	– .040	.010 .045	.500 .550	.200 BSC	.016 .021	.027 .045	.027 .034
T	10	.335 .370	.165 .185	– .040	.010 .045	.500 .550	.230 BSC	.016 .021	.027 .045	.027 .034

NOTE: MIN./MAX.

DIMENSIONS IN INCHES

V H TYPE METAL CAN, TO-8
(HA-5190/95 AND HA-2630/35 ONLY)

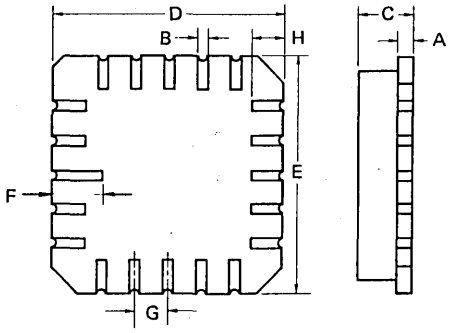


PKG. TYPE	LEAD COUNT	DIM. A	DIM. B	DIM. C	DIM. E	DIM. F	DIM. G	DIM. H	DIM. J	DIM. K
V	12	.585 .615	.130 .150	– .040	.500 .550	.400 BSC	.016 .021	.100 BSC	.027 .045	.027 .034

NOTES: MIN./MAX.

DIMENSIONS IN INCHES

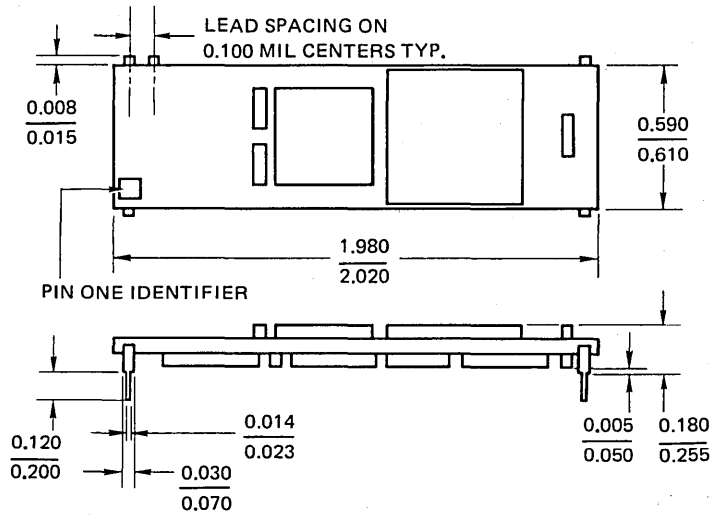
X Y LEADLESS CARRIER



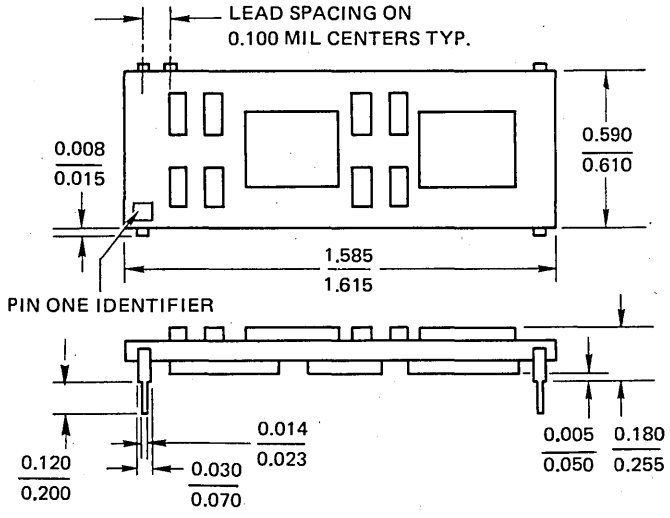
PKG. TYPE	LEAD COUNT	DIM. A	DIM. B	DIM. C	DIM. D	DIM. E	DIM. F	DIM. G	DIM. H
X	20	.017/.066	.020/.034	.064/.100	.342/.358	.342/.358	.060/0.090	.050/BSC	.040/.055
Y	28	.017/.066	.020/.034	.064/.100	.442/.458	.442/.458	.060/0.090	.050/BSC	.040/.055

NOTE: MIN./MAX. DIMENSIONS IN INCHES

MC HI-5712/12A MODULE



MB HI-5900/5901 MODULE



MICRO POWER SYSTEMS

Op Amps & Volt References

Note: See other MPS parts in Interface and Military Sections.

Precision Operational Amplifiers

- ☐ Second source to PMI
- ☐ Lowest noise in the industry
- ☐ Improved long-term stability
- ☐ High slew rate DAC follower

Model	Type	V_{OS} (Max)	I_B (Max)	Noise ($nV/\sqrt{Hz}$ at 10 Hz)	Gain (Min)	CMRR (Min)	Slew Rate (typ)	Replaces
MP4136	Quad (741 Type)	6 mV	1.5 μA		50 V/mV	70 dB	1.5 V/μsec	PM4136
MP5501/OP01	DAC Follower, Hi-speed	1 mV	50 nA		30 V/mV	85 dB	18 V/μsec	OP01
MP5502/OP02	Low Noise, Gen. Purpose	.5 mV	30 nA	25	100 V/mV	85 dB	.5 V/μsec	OP02
MP5505/OP05	Low Noise, Instrumentation	.24 mV	4 nA	10 (max)	200 V/mV	110 dB	.1 V/μsec	OP05
MP5507/OP07	Low Noise, Low V_{os} Instrumentation	60 μV	4 nA	10 (max)	200 V/mV	106 dB	.1 V/μsec	OP07
MP5508/OP08	Low Bias Current	.35 mV	3 nA	22	300 V/mV	104 dB	.12 V/μsec	OP08
MP5509/OP09	Quad Matched	1 mV	40 nA	18	50 V/mV	100 dB	0.7 V/μsec	OP09
MP5510/OP10	Dual 5505/OP05	.3 mV	6 nA	10 (max)	200 V/mV	110 dB	.1 V/μsec	OP10
MP5511/OP11	Quad Matched	1 mV	40 nA	18	50 V/mV	100 dB	0.7 V/μsec	OP11
MP5512/OP12	Low Bias Current	.35 mV	2 nA	22	300 V/mV	104 dB	.12 V/μsec	OP12
MP5524/OP24	Ultra Low Noise	170 mV	85 nA	9.5 (max)	500 V/mV	100 dB	2.8 V/μsec	OP24
MP5527/OP27	Ultra Low Noise	25 μV	40 nA	4.5 (max)	1000 V/mV	114 dB	2.8 V/μsec	OP27
MP5534/OP34	Ultra Low Noise	170 mV	85 nA	9.5 (max)	500 V/mV	100 dB	17 V/μsec	OP34
MP5537/OP37	Ultra Low Noise, High Speed	25 μV	40 nA	4.5 (max)	1000 V/mV	114 dB	17 V/μsec	OP37

Note: All specifications: -55°C to +125°C

Precision Voltage References

- ☐ Second source to PMI
- ☐ Low temperature coefficient
- ☐ Guaranteed long-term stability
- ☐ Low noise

Model	Packages	Output Voltage	Regulating Current	Temp Coefficient (max, full temp)	Reverse Dynamic Impedance	Noise	Replaces
MP5010	All	1.22V	50 μA – 500 μA	50 ppm/C°	2 ohm	5 μV	ICL8069 LM113 ZN423
MP5532/REF 01	All	10V	1.4 mA – 10 mA	8.5 ppm/C°	–	20 μV P-P	REF 01
MP5531/REF 02	All	5V	1.4 mA – 10 mA	8.5 ppm/C°	–	20 μV P-P	REF 02

All Micro Power Systems' IC's are available with 883B processing, in dice form, or to customer's specifications.

MICRO POWER SYSTEMS
3100 Alfred Street
Santa Clara, CA 95050
(408) 727-5350

MOTOROLA
SEMICONDUCTORS
P.O. BOX 20912 • PHOENIX, ARIZONA 85036

TRIMFET FAMILY OF JFET INPUT OPERATIONAL AMPLIFIERS

MC34001, MC35001
MC34002, MC35002
MC34004, MC35004

This family of low-cost TRIMFET operational amplifiers combines two state-of-the-art linear technologies on a single monolithic integrated circuit. Each internally compensated operational amplifier has well matched high voltage JFET input devices with a laser trimmed input offset voltage. The BIFET technology provides wide bandwidths and fast slew rates with low input bias currents, input offset currents, and supply currents. The laser trimming technology provides input offset voltage specification options which range from 2.0 to 10 millivolts maximum.

The Motorola TRIMFET family offers single, dual and quad operational amplifiers which are pin-compatible with the industry standard MC1741, MC1458, and the MC3403/LM324 bipolar devices. The MC35001/35002/35004 series are specified over the military operating temperature range of -55° C to +125° C and the MC34001/34002/34004 series are specified from 0° C to +70° C.

Features

- Laser Trimmed Input Offset Voltage Options of 2.0, 5.0, and 10 mV Maximum
- Low Input Bias Current — 40 pA
- Low Input Offset Current — 10 pA
- Low Input Noise Voltage — 16 nV/$\sqrt{Hz}$
- Wide Gain Bandwidth — 4 MHz
- High Slew Rate — 13 V/μs
- Low Supply Current — 1.8 mA per Amplifier
- High Input Impedance — 10^{12} Ω
- High Common-Mode and Supply Voltage Rejection Ratios — 100 dB
- Industry Standard Pinouts

GENERAL OP-AMP SELECTOR GUIDE

General Purpose Op-Amps

	Single	Dual	Quad
Compensated	MC1741 LM107 LF155 LF156 LF157 MC34001	MC1458 MC1747 MC34002 LM158 MC3458 MC4558	MC4741 LM124 MC3403 MC34004
Uncompensated	MC1709 MC1748 LM101A	MC1537	

JFET (BIFET) INPUT — High Impedance		
Single	Dual	Quad
LF355 LF356 LF357 MC34001	MC34002 MC34022	MC34004

High Slew Rate

Slew Rate (V/μs)			
5.0	13	15–17	50
LF355A	MC34022 LF356A	MC34001 MC34002 MC34004 MC1741S MC1558S **OP-37**	LF357A

Programmable

Adjustable bias current varies noise bandwidth, power consumption, etc.

Single	Quad
MC1776 **MC3476**	TCA3002 TCA3003

TRIMFET is a trademark of Motorola Inc.

Bold Part Numbers Indicate New Products

Wide Bandwidth

Bandwidth (MHz)				
100	20	5.0	4.0	3.0
NE592 MC1733	LF357A	MC3401 MC34001 MC34002 MC34004 LF356A	MC34022	MC4558

Low Offset Voltage

V_{IO} Max (μV)		
≤500	2000	
MC34022A LM308A **LM11** **OP-27** **OP-37**	MC34001A MC34002A MC34004A	LM101A LF355A LF356A LF357A LM107 LM108

Low Drift Over Temperature (TCV_{IO})

TCV_{IO} ≤ 5 μV/°C Max*	
MC34022 LF355A LF356A	LF357A LM308A **LM11** **OP-27** **OP-37**

*Input offset voltage temperature coefficient

Single-Supply

Dual	Quad
LM358 LM2904 MC3458 MC3405	LM324 LM2902 MC3301 MC3401 MC3403

Low Noise

Input Noise Voltage ≤ 0.25 μV p-p
OP-27 **OP-37**

VOLTAGE REGULATOR SELECTOR GUIDE

Fixed Voltage, 3-Terminal Regulators for Positive or Negative Polarity Power Supplies

V_{out} Volts	Tol.† Volts	I_O mA Max	Device Type Positive Output	Device Type Negative Output
3	±0.15	100	—	MC79L03AC
	±0.3			MC79L03C
5	±0.5	100	MC78L05C	MC79L05C
	±0.25		MC78L05AC	MC79L05AC
		500	MC78M05C	—
	±0.4	1500	LM109*	—
			LM209	—
	±0.25		LM309	—
	±0.35		MC7805*	—
	±0.25		MC7805C	MC7905C
	±0.2		MC7805A*	—
			MC7805AC	MC7905AC
	±0.25		LM140-5*	—
			LM340-5	—
	±0.25	3000	**MC78T05***	—
			MC78T05C	—
	±0.2		**MC78T05A***	—
			MC78T05AC	—
	±0.4		**LM123,A**	—
			LM223,A	—
	±0.25		**LM323,A**	—
5.2	±0.26	1500	—	MC7905.2C
6	±0.3	500	MC78M06C	—
	±0.35	1500	MC7806*	—
	±0.3		MC7806C	MC7906C
	±0.24		MC7806A*	—
			MC7806AC	—
	±0.3		LM140-6*	—
			LM340-6	—
	±0.3	3000	**MC78T06***	—
			MC78T06C	—
8	±0.8	100	MC78L08C	—
			MC78L08AC	—
	±0.4	500	MC78M08C	—
		1500	MC7808*	—
			MC7808C	MC7908C
	±0.3		MC7808A*	—
			MC7808AC	—
	±0.4		LM140-8*	—
			LM340-8	—
	±0.4	3000	**MC78T08***	—
			MC78T08C	—

V_{out} Volts	Tol.† Volts	I_O mA Max	Device Type Positive Output	Device Type Negative Output
12	±1.2	100	MC78L12C	MC79L12C
	±0.6		MC78L12AC	MC79L12AC
		500	MC78M12C	—
		1500	MC7812*	—
			MC7812C	MC7912C
	±0.5		MC7812A*	—
			MC7812AC	MC7912AC
	±0.6		LM140-12*	—
			LM340-12	—
	±0.6	3000	**MC78T12***	—
			MC78T12C	—
			MC78T12A*	—
	±0.5		**MC78T12AC**	—
15	±1.5	100	MC78L15C	MC79L15C
	±0.75		MC78L15AC	MC79L15A
		500	MC78M15C	—
		1500	MC7815*	—
			MC7815C	MC7915C
	±0.6		MC7815A*	—
			MC7815AC	MC7915AC
	±0.75		LM140-15*	—
			LM340-15	—
	±0.75	3000	**MC78T15***	—
			MC78T15C	—
	±0.6		**MC78T15A***	—
			MC78T15AC	—
18	±1.8	100	MC78L18C	MC79L18C
	±0.9		MC78L18AC	MC79L18AC
		500	MC78M18C	—
		1500	MC7818*	—
			MC7818C	MC7918C
	±0.7		MC7818A*	—
			MC7818AC	—
	±0.9		LM140-18*	—
			LM340-18	—
	±0.9	3000	**MC78T18***	—
			MC78T18C	—
20	±1.0	500	MC78M20C	—
24	±2.4	100	MC78L24C	MC79L24C
	±1.2		MC78L24AC	MC79L24AC
		500	MC78M24C	—
		1500	MC7824*	—
			MC7824C	MC7924C
	±1.0		MC7824A*	—
			MC7824AC	—
	±1.2		LM140-24*	—
			LM340-24	—
	±1.2	3000	**MC78T24***	—
			MC78T24C	—

*T_J = −55 to +150°C
†Output Voltage Tolerance for Worst Case
Bold Part Numbers Indicate New Products

MOTOROLA

Variable Output Voltage Regulators

Positive Output Regulators

I_O mA Max	Device Type	SUFFIX	V_{out} Volts Min	V_{out} Volts Max	V_{in} Volts Min	V_{in} Volts Max	V_{in} — V_{out} Differential Volts Min	P_D Watts Max T_C = 25° C	P_D Watts Max T_C = 25°C	Regulation % V_{out} @ T_A = 25°C Typ Line	Regulation % V_{out} @ T_A = 25°C Typ Load	TC V_{out} Typ %/°C	T_J = °C Max	Case
100	LM317L	H,Z	1.2	37	5.0	40	3.0	Internally Limited		0.04	0.5	0.006	125	29,79
	LM217L									0.02	0.3	0.004	150	
	LM117L*											0.003		
150	MC1723	CP	2.0	37	9.5	40	3.0	0.65	—	0.1	0.3	0.003	150	646
		CG						0.8	2.1	0.1		0.003		603C
		G								0.2		0.002		
		CL						1.0	—	0.1		0.003	175	632
		L							—	0.2		0.002		
250	MC1469	G	2.5	32	9.0	35	3.0	0.68	1.8	0.03	0.13	0.002	150	603
	MC1569*			37	8.5	40	2.7			0.015				
500	LM317M	T	1.2	37	5.0	40	3.0	Internally Limited		0.02	0.1	0.0056	125	221A
	LM317M	R												080
	LM217M											0.004	150	
	LM117M*											0.0036		
600	MC1469	R	2.5	32	9.0	35	3.0	3.0	14.0	0.03	0.05	0.002	150	614
	MC1569*			37	8.5	40	2.7			0.015				
1500	LM317	T	1.2	37	5.0	40	3.0	Internally Limited		0.07	1.5	0.006	125	221A
	LM317	H, K												79,1
	LM217											0.004	150	
	LM117*									0.05	1.0	0.003		
3000	LM350	T	1.2	33	5.0	36	3.0	Internally Limited		0.02	0.1	0.008	125	221A
	LM350	K												
	LM250											0.0057	150	1
	LM150*											0.0051		

* T_J = −55°C to +150°C.

Negative Output Regulators

I_O mA Max	Device Type	SUFFIX	V_{out} Volts Min	V_{out} Volts Max	V_{in} Volts Min	V_{in} Volts Max	V_{in} — V_{out} Differential Volts Min	P_D Watts Max T_C = 25° C	P_D Watts Max T_C = 25°C	Regulation % V_{out} @ T_A = 25°C Typ Line	Regulation % V_{out} @ T_A = 25°C Typ Load	TC V_{out} Typ %/°C	T_J = °C Max	Case
250	MC1463	G	−3.8	−32	−9.0	−35	3.0	0.68	1.8	0.03	0.05	0.002	150	603
	MC1563*		−3.6	−33	−8.5	−40	2.7			0.015	0.13			
600	MC1463	R	−3.8	−34	−9.0	−35	3.0	2.4	9.0	0.03	0.05	0.002	150	614
	MC1563*		−3.6	−37	−8.5	−40	2.7			0.015				
1500	LM337	T	−1.2	−37	−5.0	−40	3.0	Internally Limited		0.02	0.3	0.0048	125	221A
	LM337	H, K												79,1
	LM237											0.0034	150	
	LM137*											0.0031		

* T_J = −55°C to +150°C

SPECIAL REGULATORS

Floating Voltage and Current Regulators

Designed for laboratory type power supplies. Voltage is limited only by the breakdown voltage of associated, external, series-pass transistors.

V_{out} Volts		I_O mA	Device	SUFFIX	V_{aux} Volts		P_D Watts	$\Delta V_{ref}/V_{ref}$ %		$\Delta I_L/I_L$ %	TCV_{out} %/°C	Case
Min	Max	Max	Type		Min	Max	Max	Line	Load	Max	Typ	
0	•	•	MC1466	L	21	30	0.75	0.015	0.015	0.2	0.01	632
			MC1566	L	20	35		0.004	0.004	0.1	0.006	

* Dependent on characteristics of external series pass elements.

Dual ± 15 V Tracking Regulators

Internally, the device is set for ±15 V, but an external adjustment can change both outputs simultaneously, from 8.0 V to 20 V.

V_{out} Volts		I_O mA	V_{in} Volts		Device	SUFFIX	P_D Watts	Reg_{line}	Reg_{load}	TC %/°C (T_{low} to T_{high})	T_A	Case
Min	Max	Max	Min	Max	Type		Max	mV	mV	Typ	°C	
14.8	15.2	±100	17	30	MC1468	G	0.8	10	10	3.0	0 to +75	603C
						L	1.0					632
						R	2.4					614
					MC1568	G	0.8				−55 to +125	603C
						L	1.0					632
						R	2.4					614

SWITCHING REGULATORS

Used as the control circuit in PWM, push-pull, bridge and series type switchmode supplies. The devices include the reference, oscillator, pulse-width modulator, phase splitter and output sections. Frequency and duty cycle are independently adjustable.

I_O ±mA Max	V_{CC} Volts		f_o kHz		Device Number	Suffix	T_A °C	Case
	Min	Max	Min	Max				
40	10	30	2.0	100	MC3420	P	0 to +70	648
						L		620
					MC3520	L	-55 to +125	620
250	7.0	40	1.0	300	**MC34060**	P	0 to +70	646
						L		632
					MC35060	L	-55 to +125	632
	7.0	40	1.0	300	TL494	CN	0 to +70	648
						CJ		620
						IN	-25 to +85	648
						IJ		620
						MJ	-55 to +125	620
250		>40*	1.0	300	TL495	CN	0 to +70	701
						CJ	-25 to +85	726
						IN		701
						IJ		726
±400	8.0	40	0.1	400	**SG3525A**	N	0° to +70	648
					SG3525A	J		620
					SG2525A	N	-25 to +85	648
					SG2525A	J		620
					SG1525A	J	-55 to +125	620
	8.0	40	0.1	400	**SG3527A**	N	0 to +70	648
					SG3527A	J		620
					SG2527A	N	-25 to +85	648
					SG2527A	J		620
					SG1527A	J	-55 to +125	620
±200	8.0	40	0.001	400	**SG3526**	N	0 to +70	701
					SG3526	J		726
					SG2526	N	-25 to +85	701
					SG2526	J		726
					SG1526	J	-55 to +125	726
1500	5.0	40	1.0	40	**μA78S40**	PC	0 to +70	648
					μA78S40	DC		620
					μA78S40	DM	-55 to +125	

*TL495 features a 39 V zener for high voltage operation.

Bold Part Numbers Indicate New Products

MOTOROLA

SEMICONDUCTORS

3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MOS Telecommunications Products

MC14400/01/02/03/05 Monocircuit
- On-Board Reference
- A-Law/Mu-Law Companding and D3/D4/CCITT Format
- Synchronous and Asynchronous Operation
- 16/18/22 Pin Packages

MC14404/06/07 PCM Codec
- Per-Channel Full-Duplex Capability
- Power-Down Input
- Mu-Law Digital Format (MC14406/07)
- A-Law CCITT Digital Format (MC14404)

MC14408/09 Binary to Pulse Dialer
- On-Chip Oscillator
- Dialing of Numbers Up to 16 Digits
- Memory Storage and Re-Dialing of Last Telephone Number

MC14410 Tone Encoder
- Single-Tone Capability
- Fast Oscillator Turn-On and Turn-Off Times

MC14411 Baud Rate Generator
- Sixteen Different Output Clock Rates
- Programmable Time Bases for One-of-Four Multiple Output Rates
- Buffered Outputs Compatible with Low-Power TTL

MC14412 0-600 Baud Modem
- Originate and Answer Mode
- Simplex, Half-Duplex and Full-Duplex Operation

MC14413/14/145414 PCM Low Pass/Bandpass Filter
- Transmit Bandpass and Received Low Pass (MC14413)
- Transmit and Receive Low Pass (MC14414/5414)
- Single-Supply Capability
- ±5 to ±8 Volt Power Supply Ranges
- Two Operational Amplifiers Available

MC14416/17/18 Time Slot Assigner Circuit
- Independent Transmit and Receive Frame Syncs and Enables
- Up to 64 Time Slots Per Frame
- TTL and CMOS Level Compatibility

MC14419 2-of-8 Tone Encoder
- Suppressed Output for Illegal Input Codes
- Codes for Numbers 0-9 Produce a Strobe Pulse

MC142100/5100 Crosspoint Switch
- Power-On Reset (MC145100 Only)
- Large Analog Range

MC145431 Tuneable Low Pass/Bandpass Filter
- Contains a 7-Pole Elliptic Low Pass Filter and a 4-Pole Bandpass Filter which can be Independently Tuned with the Externally-Applied Clock Frequency
- TTL or CMOS Compatible Digital Inputs

MC145433/34 Tuneable Notch/Bandpass Filter
- Independently Tuneable Notch and Bandpass Filter
- Clock Output Pin
- Includes an Uncommitted Op Amp Capable of Driving 600 Loads
- TTL or CMOS Compatible Digital Inputs
- On Board Crystal Oscillator or External Clocks

MC145440/441 300 Baud Modem Filter (Bell 103/CCITT)
- Answer or Originate Mode
- Low Band Bandpass Filter
- High Band Bandpass Filter

MC6860 0-600 bps Digital Modem
- Originate and Answer Modes
- Crystal or External Reference Control
- Full-Duplex or Half-Duplex Operation
- Automatic Answer and Disconnect

MC6172 2400 bps Digital Modulator (Formerly 6862)
- 511-Bit CCITT Test Pattern
- CCITT and U.S. Phase Options (Bell 201)
- 1200/2400 bps Operation
- Answer-Back Tone

MC6173 2400 bps Demodulator
- Compatible with 6172 Modulator
- CCITT and U.S. Phase Options
- Compatible Functions for 201 B/C Data Sets

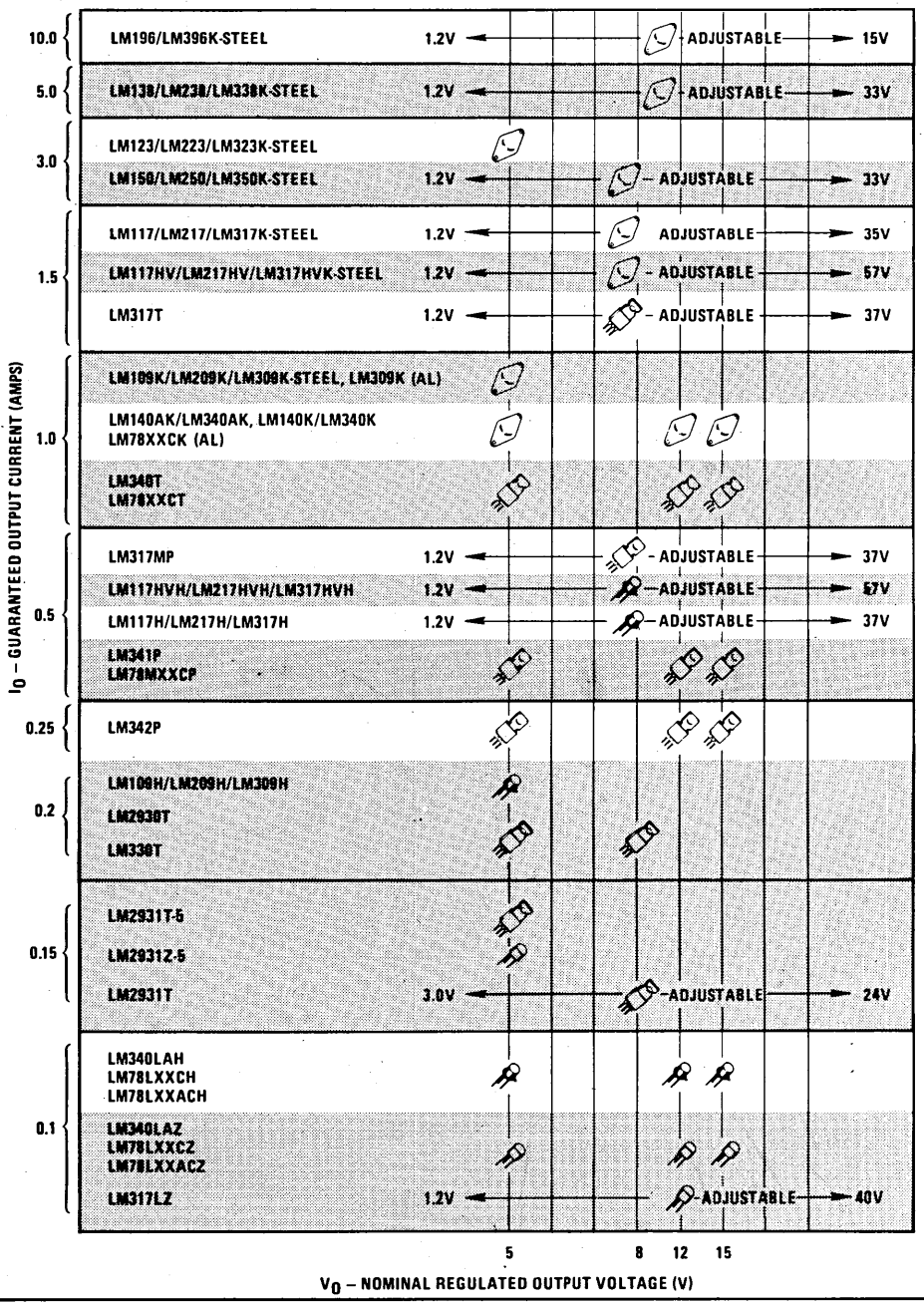
Mono-Circuit	Codec	Filters	TSAC	Crosspoint Switches	Modems	Dialers
MC14400	MC14404	MC14413	MC14416	MC142100	MC14411	MC14408
MC14401	MC14406	MC14414	MC14417	MC145100	MC14412	MC14409
MC14402	MC14407	MC145414	MC14418		MC6860	MC14410
MC14403		MC145431			MC6862	MC14419
MC14405		MC145433			MC6172	
		MC145434			MC6173	
		MC145440				
		MC145441				

3-TERMINAL POSITIVE VOLTAGE REGULATORS

Output Current (A)	Device	Available V_{OUT} (V)	V_{OUT} Tol. (±%)	Regulation		V_{IN} (V) Max	Ripple Rejection (dB)
				Line (Note 1) % V_{OUT}/V_{IN}	Load (Note 2) % V_{OUT}/V_{IN}		
10	LM196, LM396	1.25 to 15 (Adjustable)	N/A	0.005	0.1	20	74
5	LM138, LM238	1.2 to 32 (Adjustable)	N/A	0.005	0.1	35	86
	LM338	1.2 to 32 (Adjustable)	N/A	0.005	0.1	35	86
3	LM150, LM250	1.2 to 32 (Adjustable)	N/A	0.005	0.1	35	86
	LM350	1.2 to 32 (Adjustable)	N/A	0.005	0.1	35	86
	LM123K, LM223K	5	6	0.01	0.5	20	75
	LM323K	5	4	0.01	0.5	20	75
1.5	LM117, LM217	1.2 to 37 (Adjustable)	N/A	0.01	0.1	40	80
	LM317	1.2 to 37 (Adjustable)	N/A	0.01	0.1	40	80
	LM117HV, LM217HV	1.2 to 57 (Adjustable)	N/A	0.01	0.1	60	80
	LM317HV	1.2 to 57 (Adjustable)	N/A	0.01	0.1	60	80
	LM109K, LM209K	5	6	0.004	1.0	35	80
	LM309K	5	4	0.004	1.0	35	80
	LM140K	5, 12, 15	4	0.02	0.5	35	66–80
	LM140AK	5, 12, 15	2	0.002	0.1	35	66–80
	LM340	5, 12, 15	4	0.02	0.5	35	66–80
	LM340A	5, 12, 15	2	0.002	0.1	35	66–80
	LM78XXC	5, 12, 15	4	0.03	0.5	35	66–80
0.5	LM117H, LM217H	1.2 to 37 (Adjustable)	N/A	0.01	0.1	40	80
	LM317H	1.2 to 37 (Adjustable)	N/A	0.01	0.1	40	80
	LM117HVH, LM217HVH	1.2 to 37 (Adjustable)	N/A	0.01	0.1	40	80
	LM317HVH	1.2 to 37 (Adjustable)	N/A	0.01	0.1	40	80
	LM317M	1.2 to 37 (Adjustable)	N/A	0.01	0.1	40	80
	LM341	5, 12, 15	4	0.02	0.5	35	
	LM78MXX	5, 12, 15	4	0.03	0.5	35	
0.25	LM342	5, 12, 15	4	0.03	0.5	35	53–64
0.20	LM109H, LM209H	5	6	0.004	0.4	35	80
	LM309H	5	4	0.004	0.4	35	80
	LM2930T	5, 8	±10			26V	56
	LM330T	5	±6			26V	56
0.15	LM2931	5 and Adjustable	±5	0.008	0.02	26	80
0.10	LM140L, LM240L	5, 12, 15	2	0.02	0.25	35	48–62
	LM317L	1.2 to 37 (Adjustable)	N/A	0.01	0.1	40V	65
	LM340L	5, 12, 15	2	0.02	0.25	35	48–62
	LM78LXXA	5, 12, 15	4	0.03	0.25	35	45–60

Note 1: Line regulation is the change in output voltage for a change in input voltage.

Note 2: Load regulation is the change in output voltage due to a change in load current from no load to full load.



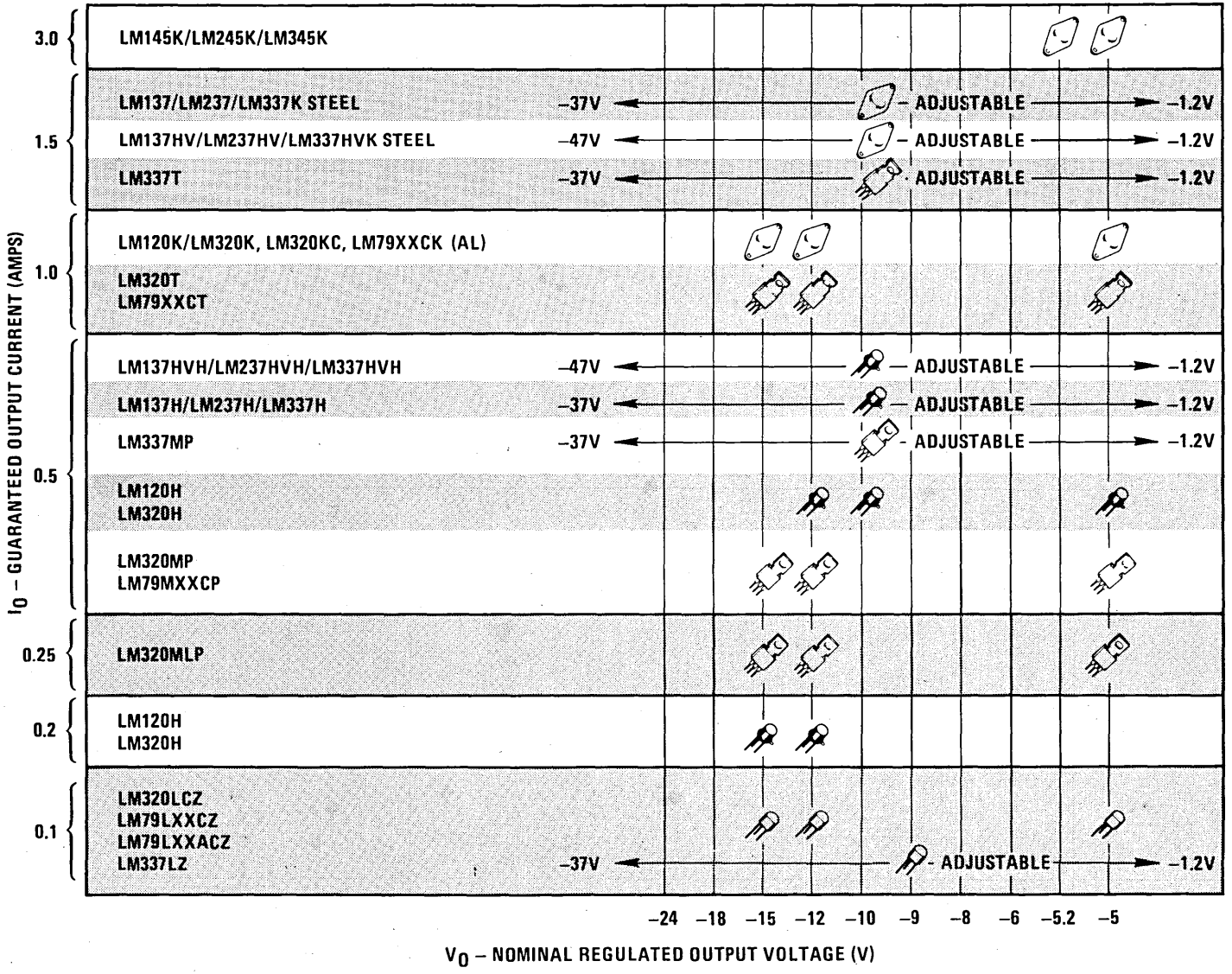
	PACKAGE DESIGNATOR	PACKAGE TYPE
	K KC K STEEL	TO-3* HERMETIC
	T	TO-220 PLASTIC
	P	TO-202 PLASTIC
	H	TO-5, TO-39 HERMETIC
	Z	TO-92 PLASTIC

*All devices with TO-3 package designators (K or K STEEL) are supplied in steel TO-3 packages unless otherwise designated as (AL) aluminum TO-3 package. All KC designated devices are supplied in aluminum TO-3.

Voltage Regulator Guide

3-TERMINAL NEGATIVE VOLTAGE REGULATORS

Output Current (A)	Device	Available V_{OUT} (V)	V_{OUT} Tol. (±%)	Regulation		V_{IN} (V) Max	Ripple Rejection (dB)
				Line (Note 1) % V_{OUT}/V_{IN}	Load (Note 2) % V_{OUT}/V_{IN}		
3	LM145K, LM245K	−5.0, −5.2	2	0.008	0.6	20	68
	LM345K	−5.0, −5.2	4	0.008	0.6	20	68
1.5	LM137, LM237	−1.2 to −37 (Adjustable)	N/A	0.006	0.3	40	77
	LM337	−1.2 to −37 (Adjustable)	N/A	0.007	0.3	40	77
	LM137HV, LM237HV	−1.2 to −47 (Adjustable)	N/A	0.006	0.3	50	77
	LM337HV	−1.2 to −47 (Adjustable)	N/A	0.007	0.3	50	77
	LM120K	−5	2	0.02	0.3	25	64
		−12, −15				35 (12V)	80
						40 (15V)	75
							70
	LM320K	−5	4	0.02	0.3	25	64
		−12, −15				35 (12V)	80
						40 (15V)	75
							70
	LM320T	−5	4	0.02	0.3	25	64
		−12, −15				35 (12V, 15V)	75–80
							70
	LM79XXC	−5	4	0.03	0.4	35	66–70
		−12, −15					
0.5	LM137H, LM237H	−1.2 to −37 (Adjustable)	N/A	0.006	0.3	40	77
	LM337H	−1.2 to −37 (Adjustable)	N/A	0.007	0.3	40	77
	LM137HVH, LM237HVH	−1.2 to −47 (Adjustable)	N/A	0.006	0.3	50	77
	LM337HVH	−1.2 to −47 (Adjustable)	N/A	0.007	0.3	50	77
	LM337M	−1.2 to −37 (Adjustable)	N/A	0.007	0.3	40	77
	LM120H	−5.0	2	0.02	0.6	25	64
	LM320H	−5.0	4	0.02	0.6	25	64
	LM320M	−5	4	0.02	0.6	25	60–64
		−12, −15	4			35 (12V, 15V)	70–80
	LM79MXX	−5, −12, −15	4	0.03	0.7	35	58–60
0.25	LM320ML	−5	4	0.01	0.5	35	50–60
		−12, −15					
0.20	LM120H	−12	2	0.02	0.1	35 (12V)	70–80
	LM320H	−15	4	0.02	0.1	40 (15V)	
0.10	LM320L	−5	4	0.01	0.5	35	60–65
		−12, −15					
	LM337LZ	−1.2 to −37	N/A	0.01	0.1	40	65
	LM79LXXA	−5, −12, −15	4	0.02	0.6	35	50–55



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	H	TO-5, TO-39 HERMETIC
	Z	TO-92 PLASTIC

*All devices with TO-3 package designators (K or K STEEL) are supplied in steel TO-3 packages unless otherwise designated as (AL) aluminum TO-3 package. All KC designated devices are supplied in aluminum TO-3.

National Semiconductor

Precision Regulator Guide

Function	Features	Line Reg	Load Reg	I_{OUT} (mA)	V_{OUT} Toler. @ 25°C (Max)	Drift (Max)	Part Number −55°C to 125°C	Part Number −25°C to 85°C	* Page Number
Positive Programmable Voltage Regulator	Internal programming resistors, adjustable current limit, V_{OUT} = 5, 6, 8, 10, 12, 15, 18V	0.008%	0.055%	0.1–200	0.5% 1%		LH0075	LH0075C	7-8
Negative Programmable Voltage Regulator					0.5% 1%		LH0076	LH0076C	7-13

*Refers to Hybrid Products Databook, 1982 edition

Reverse Breakdown Voltage V_R at I_R	Device	Voltage Tolerance Max, $T_A = 25°C$	Voltage Temperature Drift-ppm/°C Max or mV Max Change Over Temperature Range		Current Range, I_R	Output Dynamic Impedance (Max)
			Drift (Max)	Temperature Range		
1.22	LM113	±5%	100 ppm typ	−55°C to +125°C	500 μA to 20 mA	0.8Ω
1.22	LM313	±5%	100 ppm typ	0°C to 70°C	500 μA to 20 mA	0.8Ω
1.22	LM113-1	±1%	50 ppm typ	−55°C to +125°C	500 μA to 20 mA	0.8Ω
1.22	LM113-2	±2%	50 ppm typ	−55°C to +125°C	500 μA to 20 mA	0.8Ω
1.235	LM185	±1%	20 ppm typ	−55°C to +125°C	1 mA to 20 mA	0.6Ω
1.235	LM285	±1%	20 ppm typ	−25°C to +85°C	1 mA to 20 mA	0.6Ω
1.235	LM385B	±1%	20 ppm typ	0°C to +70°C	1 mA to 20 mA	1Ω
1.235	LM385	−2.5, +2	20 ppm typ	0°C to +70°C	1 mA to 20 mA	1Ω
2.49	LM136	±2%	18 mV	−55°C to +125°C	400 μA to 10 mA	0.6Ω
2.49	LM136A	±1%	18 mV	−55°C to +125°C	400 μA to 10 mA	0.6Ω
2.49	LM236	±2%	9 mV	−25°C to +85°C	400 μA to 10 mA	0.6Ω
2.49	LM236A	±1%	9 mV	−25°C to +85°C	400 μA to 10 mA	0.6Ω
2.49	LM336	±4%	6 mV	0°C to +70°C	400 μA to 10 mA	1Ω
2.49	LM336B	±2%	6 mV	0°C to +70°C	400 μA to 10 mA	1Ω
2.5	LM185-2.5	±1.5%	20 ppm typ	−55°C to +125°C	20 μA to 20 mA	0.6Ω
2.5	LM285-2.5	±1.5%	20 ppm typ	−25°C to +85°C	20 μA to 20 mA	0.6Ω
2.5	LM385-2.5	±3%	20 ppm typ	0°C to +70°C	20 μA to 20 mA	1Ω
2.5	LM385B-2.5	±1.5%	20 ppm typ	0°C to +70°C	20 μA to 20 mA	1Ω
5.0	LM136-5.0	±2%	36 mV	−55°C to +125°C	400 μA to 10 mA	0.6Ω
5.0	LM136A-5.0	±1%	36 mV	−55°C to +125°C	400 μA to 10 mA	0.6Ω
5.0	LM236-5.0	±2%	18 mV	−25°C to +85°C	400 μA to 10 mA	0.6Ω
5.0	LM236A-5.0	±1%	18 mV	−25°C to +85°C	400 μA to 10 mA	0.6Ω
5.0	LM336-5.0	±4%	12 mV	0°C to +70°C	400 μA to 10 mA	1Ω
5.0	LM336B-5.0	±2%	12 mV	0°C to +70°C	400 μA to 10 mA	1Ω
6.90	LM129A	+3%, −2%	10 ppm	−55°C to +125°C	0.6 mA to 15 mA	1Ω
6.90	LM129B	+3%, −2%	20 ppm	−55°C to +125°C	0.6 mA to 15 mA	1Ω
6.90	LM129C	+3%, −2%	50 ppm	−55°C to +125°C	0.6 mA to 15 mA	1Ω
6.90	LM329B	±5%	50 ppm	0°C to +70°C	0.6 mA to 15 mA	2Ω
6.90	LM329C	±5%	20 ppm	0°C to +70°C	0.6 mA to 15 mA	2Ω
6.90	LM329D	±5%	100 ppm	0°C to +70°C	0.6 mA to 15 mA	2Ω
6.95	LM199A	+1%, −2%	0.5 ppm	−55°C to +125°C	0.5 mA to 10 mA	1Ω
6.95	LM199A	+1%, −2%	10 ppm	85°C to +125°C	0.5 mA to 10 mA	1Ω
6.95	LM199	+1%, −2%	1 ppm	−55°C to +85°C	0.5 mA to 10 mA	1Ω
6.95	LM199	+1%, −2%	15 ppm	85°C to +125°C	0.5 mA to 10 mA	1Ω
6.95	LM299A	+1%, −2%	0.5 ppm	−25°C to +85°C	0.5 mA to 10 mA	1Ω
6.95	LM299	+1%, −2%	1 ppm	−25°C to +85°C	0.5 mA to 10 mA	1Ω
6.95	LM399A	±5%	1 ppm	0°C to +70°C	0.5 mA to 10 mA	1.5Ω
6.95	LM399	±5%	2 ppm	0°C to +70°C	0.5 mA to 10 mA	1.5Ω
6.95	LM3999	±5%	5 ppm	0°C to +70°C	0.6 mA to 10 mA	2.2Ω
10.00	LH0070-0	0.1%	20 mV	−25°C to +85°C	0 mA to 20 mA	1Ω
10.00	LH0070-1	0.1%	10 mV	−25°C to +85°C	0 mA to 20 mA	1Ω
10.00	LH0070-2	0.05%	4 mV	−25°C to +85°C	0 mA to 20 mA	1Ω
10.24	LH0071-0	0.1%	20 mV	−25°C to +85°C	0 mA to 20 mA	1Ω
10.24	LH0071-1	0.1%	10 mV	−25°C to +85°C	0 mA to 20 mA	1Ω
10.24	LH0071-2	0.05%	4 mV	−25°C to +85°C	0 mA to 20 mA	1Ω
Adjustable— 5V, 6V, 10V, 12V, 15V	LH0075	±0.5%	0.003%/°C typ	−55°C to +125°C	1 mA to 200 mA	1Ω
Adjustable— 5V, 6V, 10V, 12V, 15V	LH0075C	±1%	0.003%/°C typ	0°C to +70°C	1 mA to 200 mA	1Ω
Adjustable— −5V, −6V, −10V, −12V, −15V	LH0076	±0.5%	0.003%/°C typ	−55°C to +125°C	1 mA to 200 mA	1Ω
Adjustable— −5V, −6V, −10V, −12V, −15V	LH0076C	±1%	0.003%/°C typ	0°C to +70°C	1 mA to 200 mA	1Ω

National Semiconductor

PRELIMINARY
August 1982

MF4 Monolithic 4th Order Switched Capacitor Butterworth LP Filter

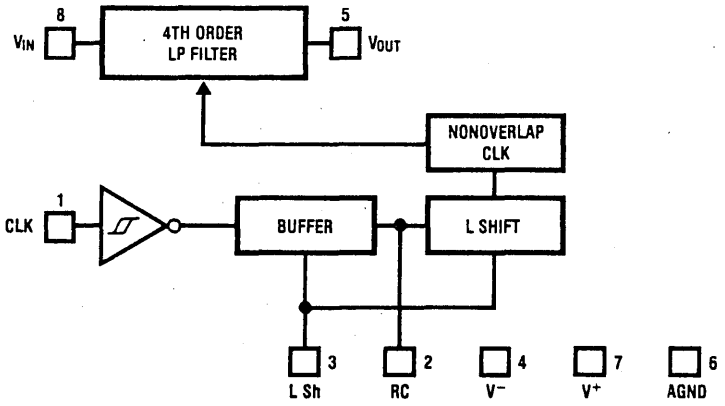
General Description

The MF4 consists of an extremely easy to use 4th order maximally flat lowpass filter packaged in an 8-pin miniDIP. Only an external clock (or an R and a C) is needed to tune the LP filter. The filter cutoff frequency is directly dependent on the clock frequency. The ratio of the clock frequency to the filter cutoff frequency is approximately 50:1 (MF4-50) or 100:1 (MF4-100). A CMOS Schmitt trigger is also included in the MF4 package to be used in the self oscillating mode. The maximally flat response of the MF4 allows cascading them for higher order filter applications.

Features

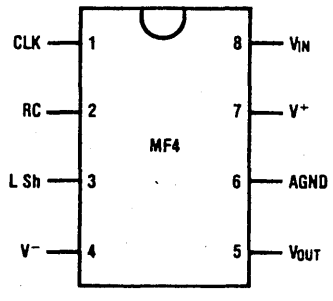
- Low cost
- Very easy to use
- No external components required
- 8-pin miniDIP
- Clock to cutoff frequency ratio accuracy 0.6%
- Operation up to 20 kHz
- Passband ripple less than 0.1 dB
- Self oscillating

System Block Diagram



Connection Diagram

Dual-In-Line Package



TOP VIEW

National Semiconductor

PRELIMINARY
August 1982

MF5 Universal Monolithic Switched Capacitor Filter

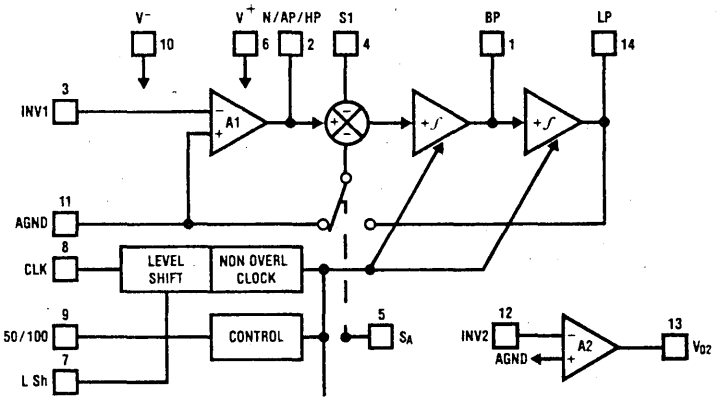
General Description

The MF5 consists of an extremely easy to use, general purpose CMOS active filter building block and an uncommitted op amp. The filter building block, together with an external clock and a few resistors, can produce various second order functions. The filter building block has 3 output pins. One of the output pins can be configured to perform highpass, allpass or notch functions and the remaining 2 output pins perform bandpass and lowpass functions. The center frequency of the filter can be directly dependent on the clock frequency or it can depend on both clock frequency and external resistor ratios. The uncommitted op amp can be used for cascading purposes, or for obtaining additional allpass and notch functions or for various other applications. Higher order filter functions can be obtained by cascading several MF5s or by using the MF5 in conjunction with the MF10 (dual switched capacitor filter building block). The MF5 is functionally compatible with the MF10. Any of the classical filter configurations (such as Butterworth, Bessel, Cauer and Chebyshev) can be formed.

Features

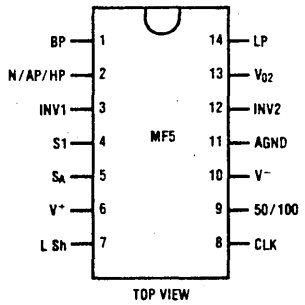
- Low cost
- 14-pin DIP
- Easy to use
- Clock to center frequency ratio accuracy 0.6%
- Filter cutoff frequency stability directly dependent on external clock quality
- Low sensitivity to external component variations
- Separate highpass (or notch or allpass), bandpass, lowpass outputs
- $f_O \times 0$ range up to 200 kHz
- Operation up to 30 kHz
- Uncommited op amp available

System Block Diagram



Connection Diagram

Dual-In-Line Package



TOP VIEW

National Semiconductor

PRELIMINARY
August 1982

MF6 Monolithic 6th Order Switched Capacitor Butterworth LP Filter

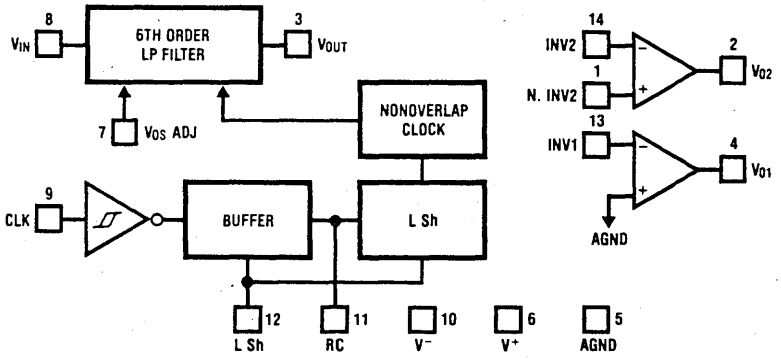
General Description

The MF6 consists of an extremely easy to use 6th order maximally flat lowpass filter and 2 uncommitted op amps. Only an external clock (or an R and a C) is needed to tune the LP filter. The filter cutoff frequency is directly dependent on the clock frequency. The ratio of the clock frequency to the filter cutoff frequency is approximately 50:1 (MF6-50) or 100:1 (MF6-100). The 2 external op amps can be used for pre or post filtering, or for any additional filtering the user's application may require. A CMOS Schmitt trigger is also included in the MF6 package to be used in the self oscillating mode (where cutoff frequency accuracy is not required). The maximally flat response of the MF6 allows cascading them for higher order filter applications.

Features

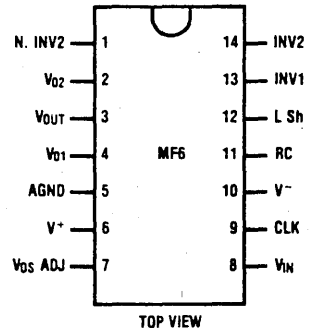
- Low cost
- Very easy to use
- No external components
- 14-pin DIP
- Clock to cutoff frequency ratio accuracy 0.6%
- Operation up to 20 kHz
- Two uncommitted op amps available
- Passband ripple less than 0.1 dB
- Self oscillating

System Block Diagram



Connection Diagram

Dual-In-Line Package



TOP VIEW

National Semiconductor

MF10 Universal Monolithic Dual Switched Capacitor Filter

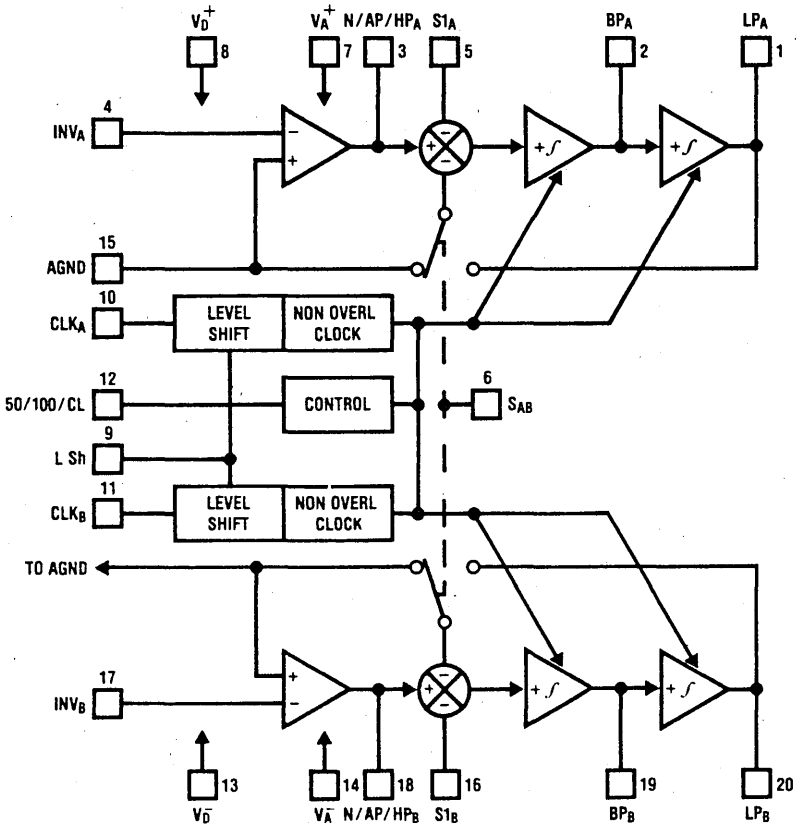
General Description

The MF10 consists of 2 independent and extremely easy to use, general purpose CMOS active filter building blocks. Each block, together with an external clock and 3 to 4 resistors, can produce various 2nd order functions. Each building block has 3 output pins. One of the outputs can be configured to perform either an allpass, highpass or a notch function; the remaining 2 output pins perform lowpass and bandpass functions. The center frequency of the lowpass and bandpass 2nd order functions can be either directly dependent on the clock frequency, or they can depend on both clock frequency and external resistor ratios. The center frequency of the notch and allpass functions is directly dependent on the clock frequency, while the highpass center frequency depends on both resistor ratio and clock. Up to 4th order functions can be performed by cascading the two 2nd order building blocks of the MF10; higher than 4th order functions can be obtained by cascading MF10 packages. Any of the classical filter configurations (such as Butterworth, Bessel, Cauer and Chebyshev) can be formed.

Features

- Low cost
- 20-pin 0.3" wide package
- Easy to use
- Clock to center frequency ratio accuracy = 0.6%
- Filter cutoff frequency stability directly dependent on external clock quality
- Low sensitivity to external component variation
- Separate highpass (or notch or allpass), bandpass, lowpass outputs
- $f_o \times Q$ range up to 200 kHz
- Operation up to 30 kHz

System Block Diagram



IM-B15M42/Printed in U.S.A.

BI-FET™/BI-FET II™ Op Amp Selection Guide

National Semiconductor

COMPARISON OF ELECTRICAL CHARACTERISTICS

	DC Electrical Characteristics				AC Electrical Characteristics	
Part Number	V_{OS}—Max Offset Voltage (mV) ($T_A = 25°C$)	$\Delta V_{OS}/\Delta T$—TC of V_{OS} ($\mu V/°C$) Typ	I_B—Max Bias Current (pA) ($T_J = 25°C$)	A_{VOL} Large Signal Voltage Gain (V/mV) Min ($T_A = 25°C$)	SR—Slew Rate (V/μs)	e_n—Equiv. Input Noise Voltage (nV/$\sqrt{Hz}$) (Note 2)
MILITARY BI-FET OP AMP (Note 1)						
LF155	5	5	100	50	5	20
LF155A	2	5 (max)	50	50	5	20
LF156	5	5	100	50	12	12
LF156A	2	5 (max)	50	50	12	12
LF157	5	5	100	50	50	12
LF157A	2	5 (max)	50	50	50	12
LF411A	0.5	10 (max)	200	50	10 (min)	25
LF411	2	10	200	50	8 (min)	25
LF441A (low power)	0.5	10 (max)	50	50	1	40
LF412A Dual	1	10 (max)	200	50	10 (min)	25
LF412	3	10	200	50	8 (min)	25
LF442A Dual (low power)	1	10	50	50	1	40
LF444 Quad (low power)	5	10	50	50	1	40
INDUSTRIAL BI-FET OP AMP (Note 1)						
LF255	5	5	100	50	5	20
LF256	5	5	100	50	12	12
LF257	5	5	100	50	50	12
COMMERCIAL BI-FET AND BI-FET II OP AMP (Note 3)						
LF351	10	10	200	25	13	16
LF355	10	5	200	25	5	25
LF355A	2	5 (max)	50	25	5	25
LF356	10	5	200	25	12	15
LF356A	2	5 (max)	50	25	12	15
LF357	10	5	200	25	50	15
LF357A	2	5 (max)	50	25	50	15
LF13741	15	10	200	25	0.5	37
LF411A	0.5	10 (max)	200	50	10	25
LF411	2.0	20	200	50	8	25
LF441A (low power)	0.5	10 (max)	50	50	1	40
LF441 (low power)	5	10	100	50	1	40
BI-FET II DUAL OP AMPS (CHARACTERISTICS FOR EACH AMPLIFIER) (Note 3)						
LF353	10	10	200	25	13	16
LF412A	1	10 (max)	200	50	10 (min)	25
LF412	3	20	200	50	8 (min)	25
LF442A (low power)	1	10 (max)	50	50	1	40
LF442 (low power)	3	20	100	50	1	40
BI-FET II QUAD OP AMPS (CHARACTERISTICS FOR EACH AMPLIFIER) (Note 3)						
LF347	10	10	200	25	13	16
LF347B	5	10	200	25	13	16
LF444A (low power)	5	10	50	50	1	40
LF444 (low power)	10	10	100	25	1	40

BI-FET™ and BI-FET II™ are trademarked terms by National Semiconductor who invented the technology in 1974.

Note 1: DC electrical characteristics are −55°C to +125°C for Military and −25°C to +85°C for Industrial unless otherwise noted; AC electrical characteristics are $T_A = 25°C$, typical specifications unless noted.

Note 2: f = 1000 Hz.

Note 3: DC electrical characteristics are 0°C to +70°C unless otherwise noted; AC electrical characteristics are $T_A = 25°C$, typical specifications unless noted.

National Semiconductor

Voltage Comparators

LF111/LF211/LF311 Voltage Comparators

General Description

The LF111, LF211 and LF311 are FET input voltage comparators that virtually eliminate input current errors. Designed to operate over a 5.0V to ±15V range the LF111 can be used in the most critical applications.

The extremely low input currents of the LF111 allows the use of a simple comparator in applications usually requiring input current buffering. Leakage testing, long time delay circuits, charge measurements, and high source impedance voltage comparisons are easily done.

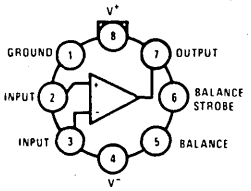
Further, the LF111 can be used in place of the LM111 eliminating errors due to input currents. See the "application hints" of the LM311 for application help.

Advantages

- Eliminates input current errors
- Interchangeable with LM111
- No need for input current buffering

Connection Diagram

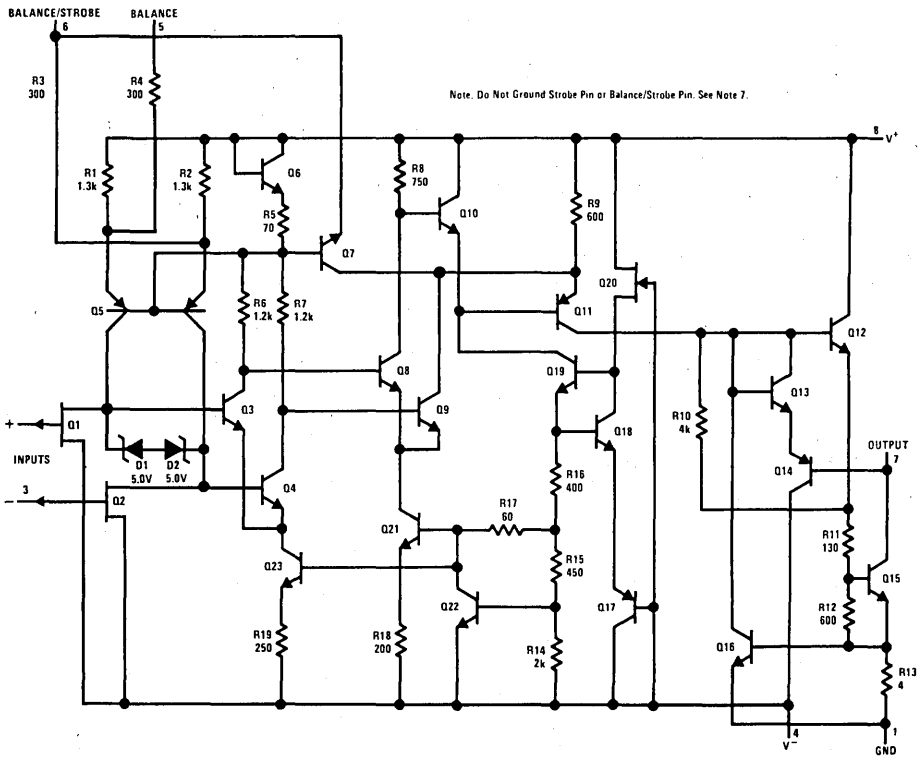
Metal Can Package

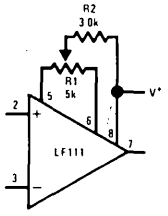


TOP VIEW

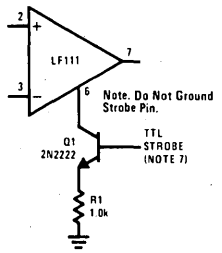
Order Number LF111H, LF211H or LF311H
See NS Package H08C

Schematic Diagram and Auxiliary Circuits

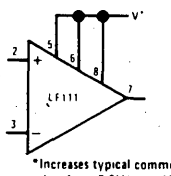




Offset Balancing



Strobing

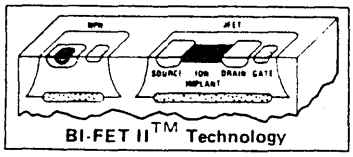


*Increases typical common mode slew from 7.0V/μs to 18V/μs.

Increasing Input Stage Current*

National Semiconductor

March 1982



LF411A/LF411 Low Offset, Low Drift JFET Input Operational Amplifier

General Description

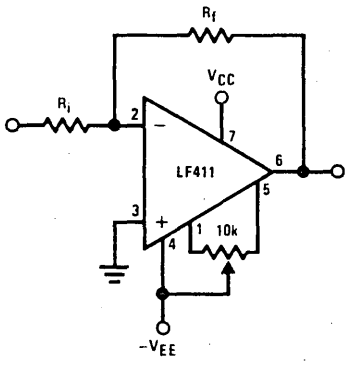
These devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and guaranteed input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF411 is pin compatible with the standard LM741 allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

■ Internally trimmed offset voltage	0.5 mV (max)
■ Input offset voltage drift	10 μV/°C (max)
■ Low input bias current	50 pA
■ Low input noise current	0.01 pA/√Hz
■ Wide gain bandwidth	3 MHz (min)
■ High slew rate	10V/μs (min)
■ Low supply current	1.8 mA
■ High input impedance	$10^{12}\Omega$
■ Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz-20 kHz	< 0.02%
■ Low 1/f noise corner	50 Hz
■ Fast settling time to 0.01%	2 μs

Typical Connection



Ordering Information

LF411XYZ

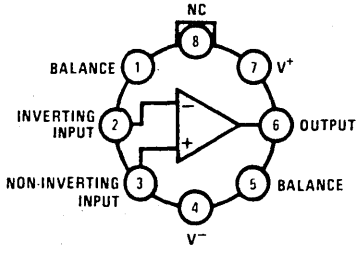
X indicates electrical grade

Y indicates temperature range
"M" for military
"C" for commercial

Z indicates package type
"H" or "N"

Connection Diagrams

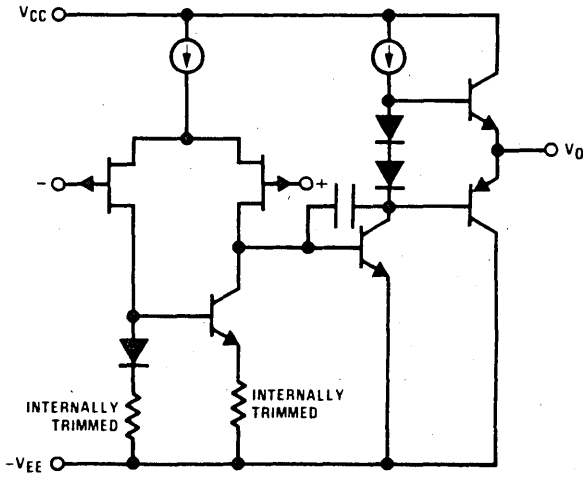
LF411AMH/LF411MH, LF411ACH/LF411CH
Metal Can Package



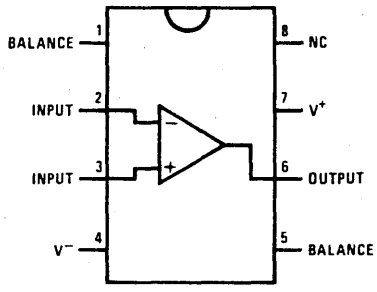
TOP VIEW

Note. Pin 4 connected to case.

Simplified Schematic



LF411ACN, LF411CN
Dual-In-Line Package



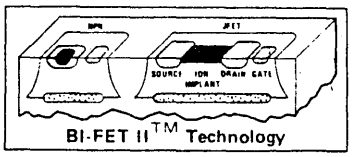
TOP VIEW

BI-FET II™ is a trademark of National Semiconductor Corp.

IM-B20M32/Printed in U.S.A.

National Semiconductor

March 1982



LF412A/LF412 Low Offset, Low Drift Dual JFET Input Operational Amplifier

General Description

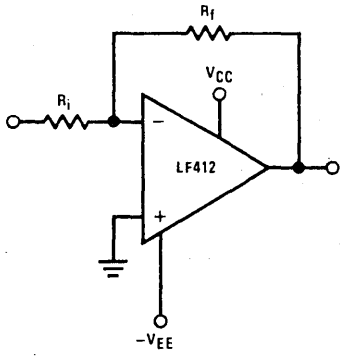
These devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and guaranteed input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. LF412 dual is pin compatible with the LM1558, allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

■ Internally trimmed offset voltage	1 mV (max)
■ Input offset voltage drift	10 μV/°C (max)
■ Low input bias current	50 pA
■ Low input noise current	0.01 pA/√Hz
■ Wide gain bandwidth	3 MHz (min)
■ High slew rate	10V/μs (min)
■ Low supply current	1.8 mA/Amplifier
■ High input impedance	$10^{12}\Omega$
■ Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz-20 kHz	<0.02%
■ Low 1/f noise corner	50 Hz
■ Fast settling time to 0.01%	2 μs

Typical Connection



Ordering Information

LF412XYZ

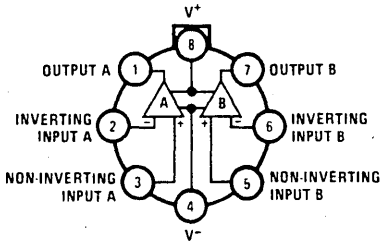
X indicates electrical grade

Y indicates temperature range
"M" for military
"C" for commercial

Z indicates package type
"H" or "N"

Connection Diagrams

LF412AMH/LF412MH, LF412ACH/LF412CH
Metal Can Package

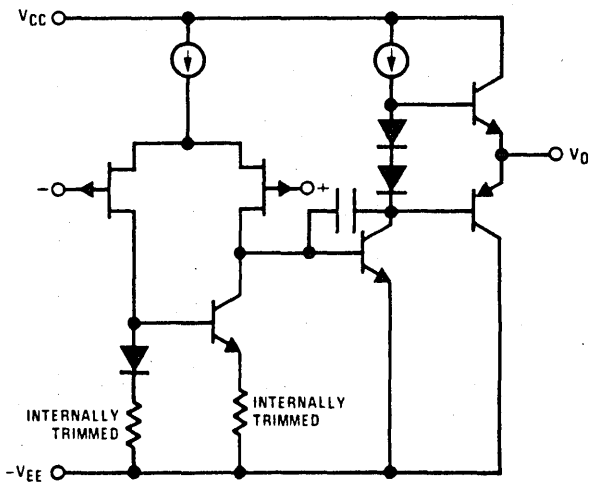


Note. Pin 4 connected to case.

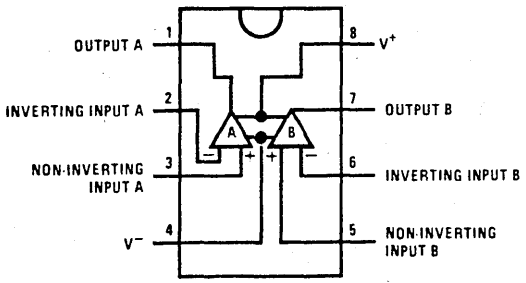
TOP VIEW

Simplified Schematic

1/2 Dual



LF412ACN, LF412CN
Dual-In-Line Package



TOP VIEW

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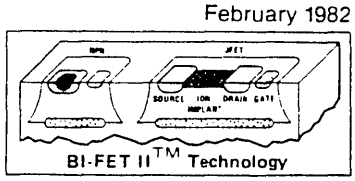
IM-B20M32-Printed in U.S.A.

National Semiconductor

February 1982

LF441A/LF441 Low Power JFET Input Operational Amplifier



General Description

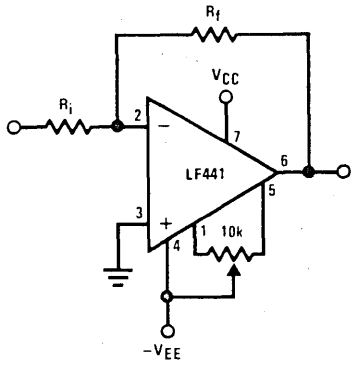
The LF441 low power operational amplifier provides many of the same AC characteristics as the industry standard LM741 while greatly improving the DC characteristics of the LM741. The amplifier has the same bandwidth, slew rate, and gain (10 kΩ load) as the LM741 and only draws one tenth the supply current of the LM741. In addition the well matched high voltage JFET input devices of the LF441 reduce the input bias and offset currents by a factor of 10,000 over the LM741. A combination of careful layout design and internal trimming guarantees very low input offset voltage and voltage drift. The LF441 also has a very low equivalent input noise voltage for a low power amplifier.

The LF441 is pin compatible with the LM741 allowing an immediate 10 times reduction in power drain in many applications. The LF441 should be used where low power dissipation and good electrical characteristics are the major considerations.

Features

1/10 supply current of a LM741	200 μA (max)
Low input bias current	50 pA (max)
Low input offset voltage	0.5 mV (max)
Low input offset voltage drift	10 μV/°C (max)
High gain bandwidth	1 MHz
High slew rate	1 V/μs
Low noise voltage for low power	35 nV/√Hz
Low input noise current	0.01 pA/√Hz
High input impedance	$10^{12}\Omega$
High gain $V_O = \pm 10V$, $R_L = 10k$	50k (min)

Typical Connection



Ordering Information

LF441XYZ

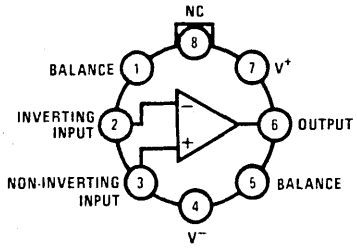
X indicates electrical grade

Y indicates temperature range
"M" for military,
"C" for commercial

Z indicates package type
"H" or "N"

Connection Diagrams

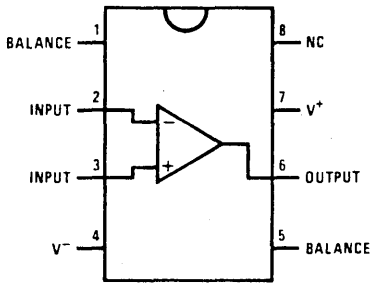
LF441AMH, LF441ACH/LF441CH
Metal Can Package



TOP VIEW

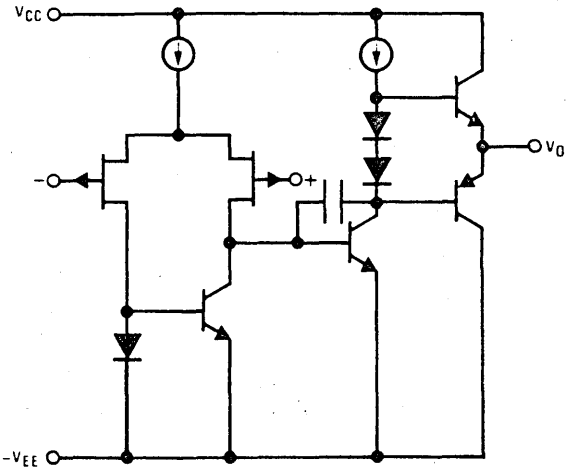
Note. Pin 4 connected to case.

LF441ACN/LF441CN
Dual-In-Line Package



TOP VIEW

Simplified Schematic



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IM B30M22/Printed in the U.S.A.

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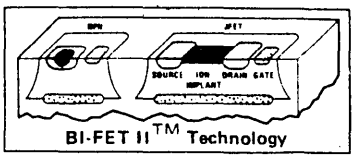
March 1982



LF442A/LF442 Dual Low Power JFET Input Operational Amplifier

General Description

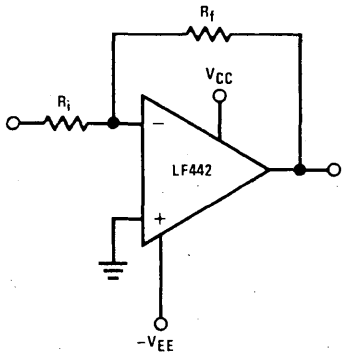
The LF442 dual low power operational amplifiers provide many of the same AC characteristics as the industry standard LM1458 while greatly improving the DC characteristics of the LM1458. The amplifiers have the same bandwidth, slew rate, and gain (10 kΩ load) as the LM1458 and only draw one tenth the supply current of the LM1458. In addition the well matched high voltage JFET input devices of the LF442 reduce the input bias and offset currents by a factor of 10,000 over the LM1458. A combination of careful layout design and internal trimming guarantees very low input offset voltage and voltage drift. The LF442 also has a very low equivalent input noise voltage for a low power amplifier.

The LF442 is pin compatible with the LM1458 allowing an immediate 10 times reduction in power drain in many applications. The LF442 should be used where low power dissipation and good electrical characteristics are the major considerations.

Features

■ 1/10 supply current of a LM1458	400 μA (max)
■ Low input bias current	50 pA (max)
■ Low input offset voltage	1 mV (max)
■ Low input offset voltage drift	10 μV/°C (max)
■ High gain bandwidth	1 MHz
■ High slew rate	1 V/μs
■ Low noise voltage for low power	35 nV/√Hz
■ Low input noise current	0.01 pA/√Hz
■ High input impedance	10^{12} Ω
■ High gain $V_O = \pm 10V$, $R_L = 10k$	50k (min)

Typical Connection



Ordering Information

LF442XYZ

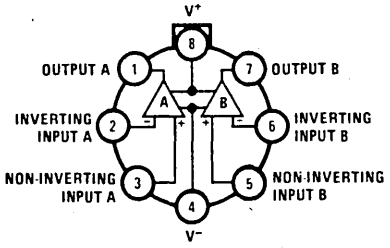
X indicates electrical grade

Y indicates temperature range
"M" for military
"C" for commercial

Z indicates package type
"H" or "N"

Connection Diagrams

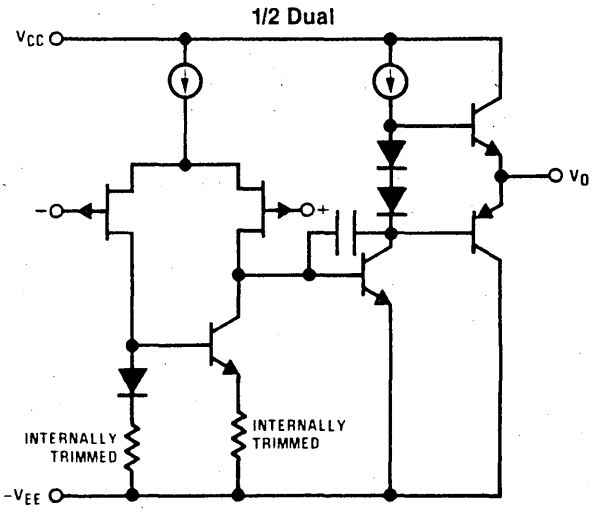
LF442AMH, LF442ACH, LF442CH
Metal Can Package



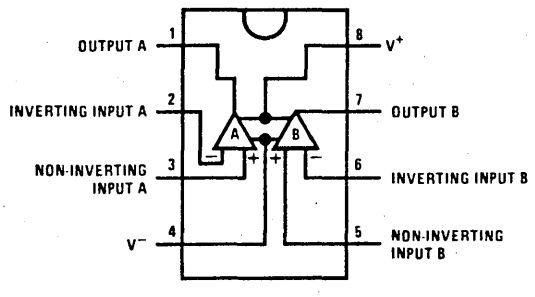
TOP VIEW

Note. Pin 4 connected to case.

Simplified Schematic



LF442ACN, LF442CN
Dual-In-Line Package



TOP VIEW

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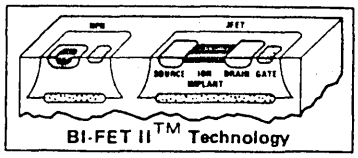
March 1982



LF444A/LF444 Quad Low Power JFET Input Operational Amplifier

General Description

The LF444 quad low power operational amplifier provides many of the same AC characteristics as the industry standard LM148 while greatly improving the DC characteristics of the LM148. The amplifier has the same bandwidth, slew rate, and gain (10 kΩ load) as the LM148 and only draws one fourth the supply current of the LM148. In addition the well matched high voltage JFET input devices of the LF444 reduce the input bias and offset currents by a factor of 10,000 over the LM148. The LF444 also has a very low equivalent input noise voltage for a low power amplifier.

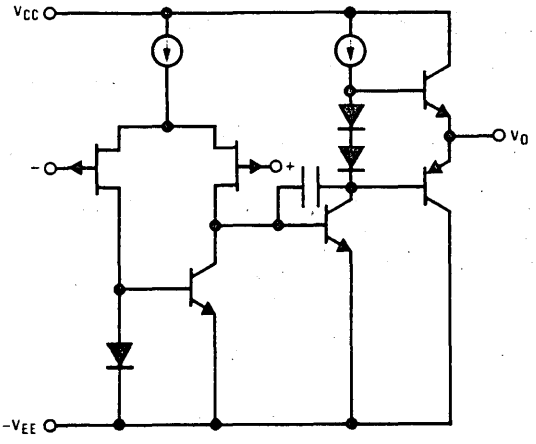
The LF444 is pin compatible with the LM148 allowing an immediate 4 times reduction in power drain in many applications. The LF444 should be used wherever low power dissipation and good electrical characteristics are the major considerations.

Features

■ 1/4 supply current of a LM148	200 μA/Amplifier (max)
■ Low input bias current	50 pA (max)
■ High gain bandwidth	1 MHz
■ High slew rate	1V/μs
■ Low noise voltage for low power	35 nV/√Hz
■ Low input noise current	0.01 pA/√Hz
■ High input impedance	$10^{12}\Omega$
■ High gain $V_O = \pm 10V, R_L = 10k$	50k (min)

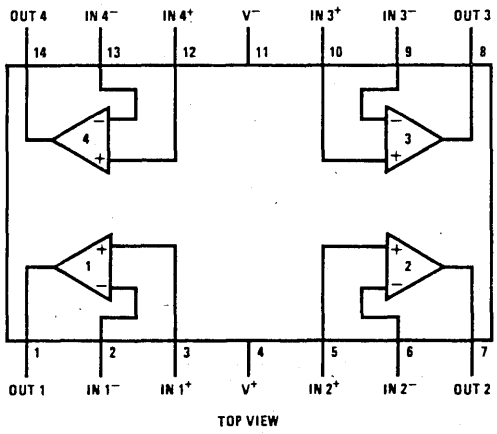
Simplified Schematic

1/4 Quad



Connection Diagram

LF444AMD/LF444CD/LF444ACN/LF444CN
Dual-In-Line Package



TOP VIEW

Ordering Information

LF444XYZ

X indicates electrical grade

Y indicates temperature range
"M" for military, "C" for commercial

Z indicates package type "D" or "N"

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National Semiconductor

PRELIMINARY
October 1982

LP165/LP365 Micropower Programmable Quad Comparator

General Description

The LP165 series consists of four independent voltage comparators. The comparators can be programmed, four at the same time, for various supply currents, input currents, response times and output current drives. This is accomplished by connecting a single resistor between the V_{CC} and I_{SET} pins.

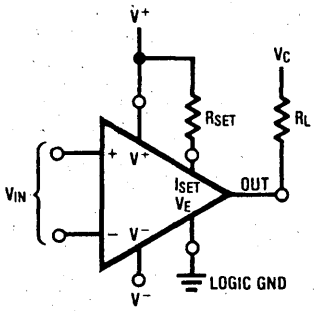
These comparators can be operated from split power supplies or from a single power supply over a wide range of voltages. The input can sense signals at ground level even with single supply operation. The unique output NPN transistor stages are uncommitted to either power supply. They can be connected directly to various logic system supplies so that they are highly flexible to interface with various logic families.

Application areas include battery power circuits, threshold detectors, zero crossing detectors, simple serial A/D converters, VCO, multivibrators, voltage converters, power sequencers, and high performance V/F converters, and RTD linearization.

Features

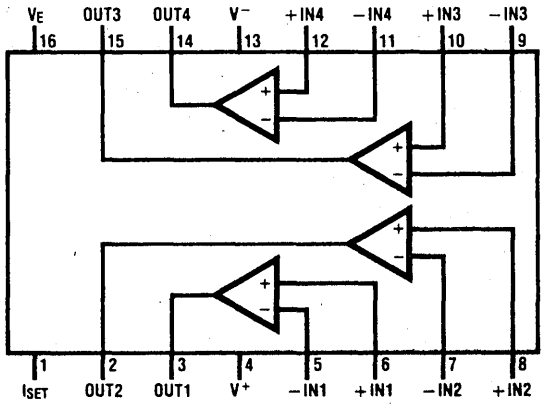
- Single programming resistor to tailor power consumption, input current, speed and output current drive capability
- Wide single supply voltage range or dual supplies (4 V_{DC} to 36 V_{DC} or ± 2.0 V_{DC} to ± 18 V_{DC})
- Low supply current drain (10 μA) and low power consumption (10 μW/comparator)@I_{SET} = 0.5 μA V_{CC} = 5 V_{DC}
- Uncommitted output stage — selectable output levels
- Output directly compatible with DTL, TTL, CMOS, MOS or other special logic families
- Input common-mode range includes ground
- Differential input voltage equal to the power supply voltage

Typical Connection



Connection Diagram

Dual-In-Line Package



TOP VIEW

Programming Equation

$$I_{SET} = \frac{(V^+) - (V^-) - 1.3V}{R_{SET}}$$

$$I_{SUPPLY} \approx 22 \times I_{SET}$$

Device	Temperature Range*	DTL/TTL Fanout	Supply Voltage Typ (V)	Input Bias Current (25°C) Max (μA)	Input Offset Current (25°C) Max (μA)	Input Offset Voltage (25°C) Max (mV)	Response Time† Typ (ns)	Voltage Gain Typ	Package Type	Comments
LM106	Military	10	$V^+ = 12$	20	3	2	40 max	40k	TO-5	Single comparator with strobe, high speed and sensitivity, large fanout
LM206	Industrial	10	$V^- = -3$	20	3	2	40 max	40k	TO-5	
LM306	Commercial	10	To −12	25	5	5	40 max	40k	TO-5	
LF111	Military	2	36	0.05	0.000025	4	200	200k	TO-5	FET front-end inputs
LF211	Industrial	2	36	0.05	0.000025	4	200	200k	TO-5	
LF311	Commercial	2	36	0.15	0.000075	10	200	200k	TO-5	
LM111	Military	5	±15	0.1	0.04	0.7	200	200k	TO-5 DIP	Single, with strobe, will work from single supply, low bias current
LH2111 Dual (Note 1)	Military	5	±15	0.1	0.04	0.7	200	200k	TO-5 DIP F.P.	
LM211	Industrial	5	To 5	0.1	0.04	0.7	200	200k	To-5 DIP	
LH2211 Dual (Note 1)	Industrial	5	To 5	0.1	0.04	0.7	200	200k	TO-5 DIP F.P.	
LM311	Commercial	5	And GND	0.25	0.06	2	200	200k	TO-5 DIP	
LH2311 Dual (Note 1)	Commercial	5	And GND	0.25	0.06	2	200	200k	TO-5 DIP F.P.	
LM119	Military	2 (Each Side)	±15	0.5	0.075	4	80	40k	TO-5 DIP	High speed dual comparator
LM219	Industrial	2 (Each Side)	To 5	0.5	0.075	4	80	40k	TO-5 DIP	
LM319	Commercial	2 (Each Side)	And GND	1	0.2	8	80	40k	TO-5 DIP	
LM139 Quad	Military	1	±1	0.1	0.025	5	1.3μs	200k	DIP	Quad comparator designed for single supply operation; input common mode range includes ground
LM239 Quad	Industrial	1	To ±18 Or From 2 To 36 And GND	0.25	0.050	5	1.3μs	200k	DIP	
LM339 Quad	Commercial	1		0.25	0.050	5	1.3μs	200k	DIP	
LM139A Quad	Military	1		0.1	0.025	2	1.3μs	200k	DIP	Low offset voltage Quad comparator with DTL/TTL logic levels
LM239A Quad	Industrial	1		0.25	0.050	2	1.3μs	200k	DIP	
LM339A Quad	Commercial	1		0.25	0.050	2	1.3μs	200k	DIP	
LM160	Military	2	±4.5	10	2	2	16	3k	TO-5 DIP	Very high speed, outputs compatible with DTL/TTL logic levels
LM260	Industrial	2	To	10	2	2	16	3k	TO-5 DIP	
LM360	Commercial	2	±6.5	15	4	4	16	3k	TO-5 DIP	
LM161 (LM529)	Military	2	±5	10	2	2	12	3k	TO-5 DIP	Very high speed, with individual strobes, DTL/TTL compatible
LM261	Industrial	2	To ±15	10	2	2	12	3k	TO-5 DIP	
LM361 (LM529C)	Commercial	2	And 5	15	4	4	12	3k	TO-5 DIP	
LM193	Military	1	±1	0.1	0.025	5	1.3μs	200k	TO-5	Dual comparator designed for single supply operation; input common-mode range includes ground
LM293	Industrial	1	To ±18 Or From 2 To 36 And Gnd	0.25	0.050	5	1.3μs	200k	TO-5	
LM393	Commercial	1		0.25	0.050	5	1.3μs	200k	TO-5, DIP	
LM193A	Military	1		0.1	0.025	2	1.3μs	200k	TO-5	Low offset voltage dual comparator with DTL/TTL logic levels
LM293A	Industrial	1		0.25	0.050	2	1.3μs	200k	TO-5	
LM393A	Commercial	1		0.25	0.050	2	1.3μs	200k	TO-5, DIP	
LM710	Military	1	$V^+ = 12$	20	3	2	40	1750	TO-5	Single, differential in, single output
LM710C	Commercial	1	$V^- = -6$	25	5	5	40	1500	TO-5 DIP	
LM711 Dual	Military	1	$V^+ = 12$	75	10	3.5	40	1500	TO-5	Dual differential, common output, individual strobes
LM711C Dual	Commercial	1	$V^- = -6$	100	15	5	40	1500	TO-5 DIP	
LM1514 Dual	Military	1	$V^+ = 14$	20	3	3	30	1250	DIP	Dual LM710 with separate strobes, individual outputs
LM1414 Dual	Commercial	1	$V^- = -7$	25	5	4	30	1000	DIP	
LM2901 Quad	Industrial	1	±1 (2V) to ±18 (36)	0.25	0.05	7	1.3	200k	DIP	Quad comparator designed for single supply operation; input common-mode range includes ground
LM2903	Automotive	1	±1 (2V) to ±18 (36)	0.25	0.050	7	1.3μs	200k	DIP	Dual comparator designed for single supply operation; input common-mode range includes ground

Note 1: Dual version of device. †Response time is specified for 100 mV step input with 5 mV overdrive.
*Military: −55°C to +125°C; Industrial: −25°C to +85°C; Commercial: 0°C to +70°C; Automotive: −40°C to +85°C

National Semiconductor

Analog Switches/Multiplexers Selection Guide

R_{ON} (Ω)*	V_A/I (V)†	Part Number	Logic Input	V_S (V) Typ	t_{ON}/t_{OFF} Typ
QUAD SPST					
100	15 mA	AH5011	15V TTL, CMOS		150/300 ns
150	5 mA	AH5012	TTL, CMOS		150/300 ns
200	± 10	LF11201	TTL	± 15	90/500 ns
200	± 10	LF11202	TTL	± 15	90/500 ns
200	± 10	LF11331	TTL	± 15	90/500 ns
200	± 10	LF11332	TTL	± 15	90/500 ns
200	± 10	LF11333	TTL	± 15	90/500 ns
250	± 10	LF13201	TTL	± 15	90/500 ns
250	± 10	LF13202	TTL	± 15	90/500 ns
250	± 10	LF13331	TTL	± 15	90/500 ns
250	± 10	LF13332	TTL	± 15	90/500 ns
250	± 10	LF13333	TTL	± 15	90/500 ns
280	± 7.5	CD4066	CMOS	± 7.5	50/50 ns
850	± 7.5	CD4016	CMOS	± 7.5	20/20 ns
TRIPLE SPDT					
280	± 7.5	CD4053	CMOS	± 7.5	150/150 ns
4-CHANNEL					
100	15 mA	AH5009	15V TTL, CMOS		150/300 ns
150	5 mA	AH5010	TTL, CMOS		150/300 ns
4-CHANNEL DIFFERENTIAL					
280	± 7.5	CD4052	CMOS	± 7.5	150/150 ns
350	12, − 15	LF11509	TTL	± 15	1/0.2 μs
270	± 7.5	CD4529B	CMOS	± 7.5	50/50 ns
8-CHANNEL					
250-400	± 5	AM3705	TTL	− 15, 5	300/600 ns
350	12, − 15	LF11508	TTL	± 15	1/0.2 μs
270	± 7.5	CD4529B	CMOS	± 7.5	50/50 ns
280	± 7.5	CD4501	CMOS	± 7.5	150/150 ns

*R_{ON} max @ $T_A = 25°C$

†V_A/I = maximum voltage or current to be safely switched

A/D Converter/DVM Selection Guide

National Semiconductor

Part No.	Resolution (Bits)	Absolute Accuracy (Max)	Conversion Time	Input Voltage Range	Output Logic Levels	Supplies (V)	Temperature Range*			Package	Comments
							M	I	C		
A/D CONVERTER											
ADC0800	8	±2 LSB	50 μs	±5V	TTL, TRI-STATE®	+5, −12	•		•	18-Pin DIP	
ADC0801	8	±1/4 LSB	110 μs	5V	TTL, TRI-STATE	+5	•	•	•	20-Pin DIP	Differential Input
ADC0802	8	±1/2 LSB	110 μs	5V	TTL, TRI-STATE	+5	•	•	•	20-Pin DIP	Differential Input
ADC0803	8	±1/2 LSB	110 μs	5V	TTL, TRI-STATE	+5		•	•	20-Pin DIP	Differential Input
ADC0804	8	±1 LSB	110 μs	5V	TTL, TRI-STATE	+5			•	20-Pin DIP	Differential Input
ADC0805	8	±1 LSB	110 μs	5V	TTL, TRI-STATE	+5		•	•	20-Pin DIP	Works with 5V Reference
ADC0808	8	±1/2 LSB	100 μs	5V	TTL, TRI-STATE	+5	•	•	•	28-Pin DIP	8-Channel MUX
ADC0809	8	±1 LSB	100 μs	5V	TTL, TRI-STATE	+5		•	•	28-Pin DIP	8-Channel MUX
ADC0816	8	±1/2 LSB	100 μs	5V	TTL, TRI-STATE	+5	•	•	•	40-Pin DIP	16-Channel MUX
ADC0817	8	±1 LSB	100 μs	5V	TTL, TRI-STATE	+5		•	•	40-Pin DIP	16-Channel MUX
†ADC0831B	8	±1/2 LSB	80 μs	5V	TTL	+5 to +9		•	•	8-Pin DIP	Serial I/O
†ADC0831C	8	±1 LSB	80 μs	5V	TTL	+5 to +9		•	•	8-Pin DIP	Serial I/O
†ADC0832B	8	±1/2 LSB	80 μs	5V	TTL	+5 to +9		•	•	8-Pin DIP	2-Channel MUX Serial I/O
†ADC0832C	8	±1 LSB	80 μs	5V	TTL	+5 to +9		•	•	8-Pin DIP	2-Channel MUX Serial I/O
ADC0833B	8	±1/2 LSB	80 μs	5V	TTL	+5 to +9		•	•	14-Pin DIP	4-Channel MUX Serial I/O
ADC0833C	8	±1 LSB	80 μs	5V	TTL	+5 to +9		•	•	14-Pin DIP	4-Channel MUX Serial I/O
†ADC0834B	8	±1/2 LSB	80 μs	5V	TTL	+5 to +9		•	•	14-Pin DIP	4-Channel MUX Serial I/O
†ADC0834C	8	±1 LSB	80 μs	5V	TTL	+5 to +9		•	•	14-Pin DIP	4-Channel MUX Serial I/O
†ADC0838B	8	±1/2 LSB	80 μs	5V	TTL	+5 to +9		•	•	20-Pin DIP	8-Channel MUX Serial I/O
†ADC0838C	8	±1 LSB	80 μs	5V	TTL	+5 to +9		•	•	20-Pin DIP	8-Channel MUX Serial I/O
†ADC1001B	10	±1/2 LSB	200 μs	5V	TTL, TRI-STATE	+5		•	•	20-Pin DIP	Differential Input
ADC1001C	10	±1 LSB	200 μs	5V	TTL, TRI-STATE	+5		•	•	20-Pin DIP	Differential Input
†ADC1021B	10	±1/2 LSB	200 μs	5V	TTL, TRI-STATE	+5		•	•	24-Pin DIP	Differential Input
ADC1021C	10	±1 LSB	200 μs	5V	TTL, TRI-STATE	+5		•		24-Pin DIP	Differential Input
†ADC1080	10	±1/2 LSB	18 μs	±10V	TTL	+5, ±12 to ±15		•		32-Pin DIP	With Reference and Clock

Part No.	Resolution (Bits)	Linearity @ 25°C (Max)	Internal Reference	Output Op Amp	Settling Time (+1/2 LSB)	Supplies (V)	Temperature Range*			Package	Comments
							M	I	C		
DAC0800	8	0.19			100 ns	±5 to ±15	•		•	16-Pin DIP	High Speed Multiplying
DAC0801	8	0.39			100 ns	±5 to ±15	•		•	16-Pin DIP	High Speed Multiplying
DAC0802	8	0.10			100 ns	±5 to ±15	•		•	16-Pin DIP	High Speed Multiplying
DAC0806	8	0.78			150 ns	±5 to ±15			•	16-Pin DIP	Multiplying
DAC0807	8	0.39			150 ns	±5 to ±15			•	16-Pin DIP	Multiplying
DAC0808	8	0.19			150 ns	±5 to ±15	•		•	16-Pin DIP	Multiplying
DAC0830	8	0.05			1 μs	5 to 15	•	•	•	20-Pin DIP	μP Compatible 4-Quadrant Multiplying
DAC0831	8	0.10			1 μs	5 to 15		•	•	20-Pin DIP	μP Compatible 4-Quadrant Multiplying
DAC0832	8	0.20			1 μs	5 to 15		•	•	20-Pin DIP	μP Compatible 4-Quadrant Multiplying
DAC1000	10	0.05			500 ns	5 to 15	•	•	•	24-Pin DIP	μP Compatible Double Buffered
DAC1001	10	0.1			500 ns	5 to 15		•	•	24-Pin DIP	μP Compatible Double Buffered
DAC1002	10	0.2			500 ns	5 to 15		•	•	24-Pin DIP	μP Compatible Double Buffered
DAC1006	10	0.05			500 ns	5 to 15	•	•	•	20-Pin DIP	μP Compatible Double Buffered
DAC1007	10	0.1			500 ns	5 to 15		•	•	20-Pin DIP	μP Compatible Double Buffered
DAC1008	10	0.2			500 ns	5 to 15		•	•	20-Pin DIP	μP Compatible Double Buffered
DAC1020	10	0.05			500 ns	5 to 15	•	•	•	16-Pin DIP	4-Quadrant Multiplying
DAC1021	10	0.1			500 ns	5 to 15	•	•	•	16-Pin DIP	4-Quadrant Multiplying
DAC1022	10	0.2			500 ns	5 to 15	•	•	•	16-Pin DIP	4-Quadrant Multiplying
DAC1200	12	0.012	•	•	300 ns – I_{OUT} 2.5 μs – V_{OUT}	±15	•	•		24-Pin DIP	Current or Voltage Mode
DAC1201	12	0.049	•	•	300 ns – I_{OUT} 2.5 μs – V_{OUT}	±15	•	•		24-Pin DIP	Current or Voltage Mode
DAC1208	12	0.012			1 μs	5 to 15		•	•	24-Pin DIP	μP Compatible 4-Quadrant Multiplying
DAC1209	12	0.024			1 μs	5 to 15		•	•	24-Pin DIP	μP Compatible 4-Quadrant Multiplying

National Semiconductor

June 1982

ADC0820 8-Bit High Speed μP Compatible A/D Converter with Track/Hold Function

General Description

The ADC0820 is a CMOS 8-bit A/D converter which uses a half-flash technique consisting of 32 comparators, a most significant 4-bit ADC and a least significant 4-bit ADC.

This converter's input acquisition time is much faster than its conversion time and is capable of measuring many analog signals without the aid of a sample-and-hold.

This A/D is designed to appear as memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

Key Specifications

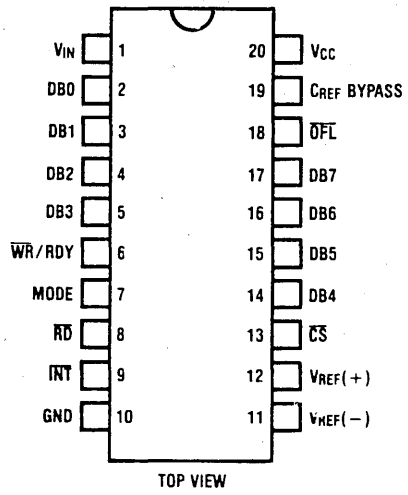
- Resolution — 8 Bits
- Conversion Time — 2.5 μs Max (RD Mode); 1.2 μs Max (WR-RD Mode)
- Input signals with slew rate of 100 mV/μs converted without external sample-and-hold to 8 bits
- Low Power — 35 mW
- Total Unadjusted Error — ± 1/2 LSB and ± 1 LSB

Features

- Built-in track-and-hold function
- No missing codes
- No external clocking
- Easy interface to all microprocessors, or operates stand-alone
- Logic inputs and outputs meet both MOS and T^2L voltage level specifications
- Operates ratiometrically or with any reference value equal to or less than V_{CC}.
- 0V to 5V analog input voltage range with single 5V supply
- No zero or full-scale adjust required
- Overflow output available for cascading
- 0.3" standard width 20-pin DIP

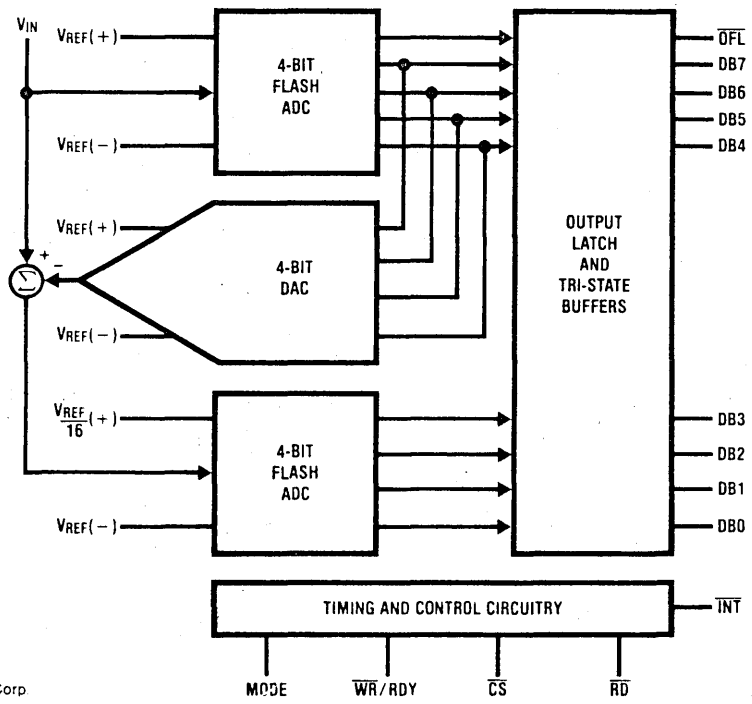
Connection Diagram

Dual-In-Line Package



TOP VIEW

Functional Diagram



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National Semiconductor

ADC0831, ADC0832, ADC0834 and ADC0838 (COP431, COP432, COP434 and COP438) 8-Bit Serial I/O A/D Converters with Multiplexer Options

General Description

The ADC0831 series are 8-bit successive approximation A/D converters with a serial I/O and configurable input multiplexers with up to 8 channels. The serial I/O is configured to comply with the NSC MICROWIRE™ serial data exchange standard for easy interface to the COPS™ family of processors, and can interface with standard shift registers or μPs.

The 2-, 4- or 8-channel multiplexers are software configured for single-ended or differential inputs as well as channel assignment.

The differential analog voltage input allows increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

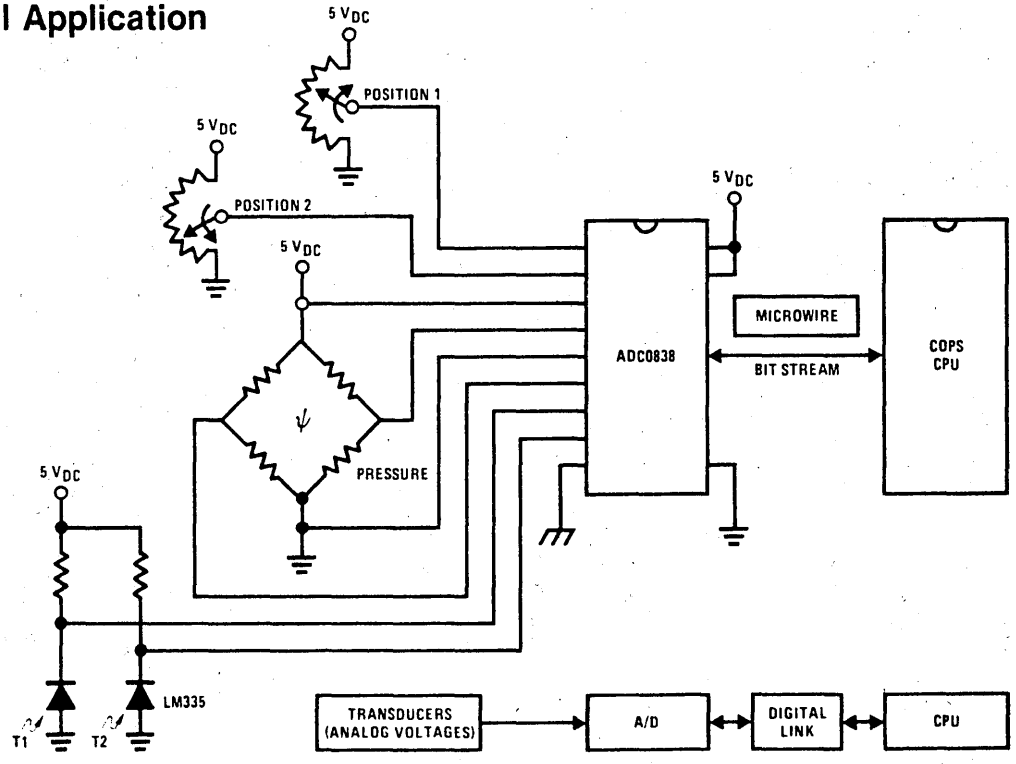
Features

- NSC MICROWIRE compatible—direct interface to COPS family processors
- Easy interface to all microprocessors, or operates "stand-alone"
- Operates ratiometrically or with 5 V_{DC} voltage reference
- No zero or full-scale adjust required
- 2-, 4- or 8-channel multiplexer options with address logic
- Shunt regulator allows operation with high voltage supplies
- 0V to 5V input range with single 5V power supply
- Remote operation with serial digital data link
- T^2L/MOS input/output compatible
- 0.3″ standard width 8-, 14- or 20-pin DIP package

Key Specifications

Resolution	8 Bits
Total Unadjusted Error	±1/2 LSB and ±1 LSB
Single Supply	5 V_{DC}
Low Power	15 mW
Conversion Time	32 μs

Typical Application



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IM-B25M62/Printed in U.S.A.

National Semiconductor

October 1982

ADC0833 8-Bit Serial I/O A/D Converter with 4-Channel Multiplexer

General Description

The ADC0833 series is an 8-bit successive approximation A/D converter with a serial I/O and configurable input multiplexer with 4 channels. The serial I/O is configured to comply with the NSC MICROWIRE™ serial data exchange standard for easy interface to the COPS™ family of processors, as well as with standard shift registers or μPs.

The 4-channel multiplexer is software configured for single-ended or differential inputs when channel assigned by a 4-bit serial word.

The differential analog voltage input allows increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

Features

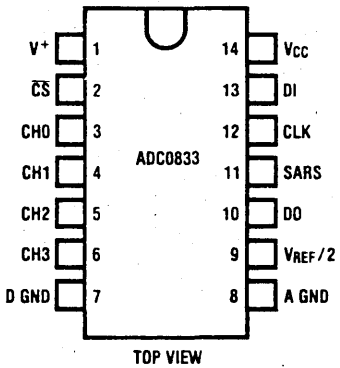
- NSC MICROWIRE compatible—direct interface to COPS family processors
- Easy interface to all microprocessors, or operates "stand alone"
- Works with 2.5V (LM336) voltage reference
- No full-scale or zero adjust required
- Differential analog voltage inputs
- 4-channel analog multiplexer
- Shunt regulator allows operation with high voltage supplies
- 0V to 5V input range with single 5V power supply
- Remote operation with serial digital data link
- T²L/MOS input/output compatible
- 0.3″ standard width 14-pin DIP package

Key Specifications

■ Resolution	8 Bits
■ Total Unadjusted Error	± 1/2 LSB and ± 1 LSB
■ Single Supply	5 V_{DC}
■ Low Power	25 mW
■ Conversion Time	32 μs

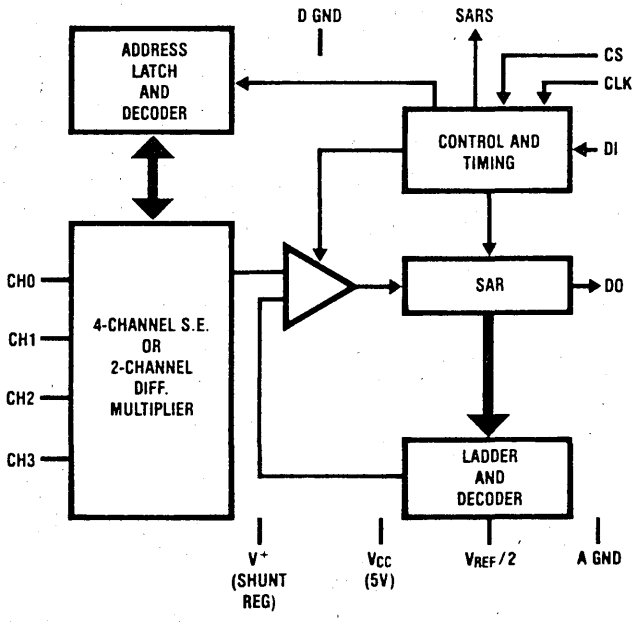
Connection Diagram

Dual-In-Line Package



TOP VIEW

Functional Diagram



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National Semiconductor

May 1982

ADC0844 8-Bit μP Compatible A/D Converter with 4-Channel Multiplexer

General Description

The ADC0844 is a CMOS 8-bit successive approximation A/D converter with configurable input multiplexers of 4 channels. The 4-channel multiplexer is software configured for single-ended, differential or pseudo-differential.

The differential analog voltage input allows increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

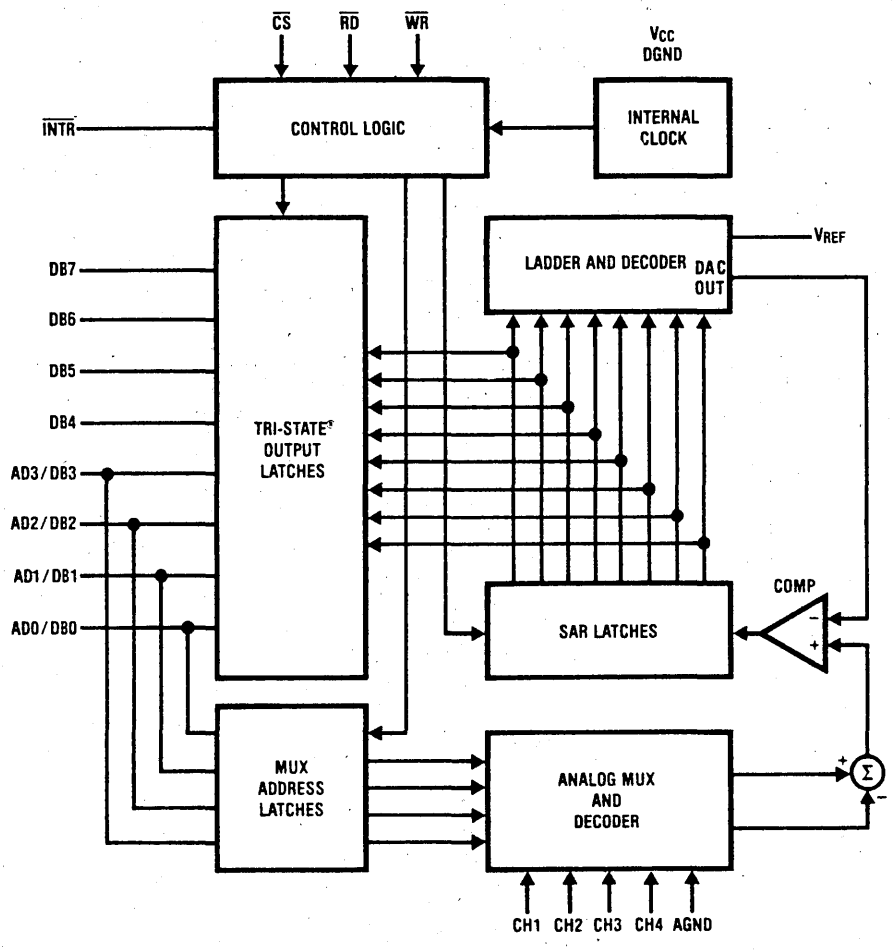
Features

- Compatible with 8080 μP derivatives—no interface logic needed
- Easy interface to all microprocessors
- Operates ratiometrically or with 5 V_{DC} voltage reference
- No zero or full-scale adjust required
- 4-channel multiplexer with address logic
- Internal clock
- 0V to 5V input range with single 5V power supply
- T^2L/MOS input/output compatible
- 0.3" standard width 20-pin DIP

Key Specifications

Resolution	8 Bits
Total Unadjusted Error	± 1/2 LSB and ± 1 LSB
Single Supply	5 V_{DC}
Low Power	10 mW
Conversion Time	40 μs

Block Diagram



TRI-STATE® is a registered trademark of National Semiconductor Corp.

National Semiconductor

Audio/Radio Selection Guide

AM RF/IF/DETECTOR

	Application			Package	Voltage Range	Input Sensitivity	Overall AM THD	Signal to Noise	Notes
	Portable	Home	Auto						
LM1866	●	●	●	N20	3V-15V	9 μV	0.3%	50 dB	Also FM
LM1868	●	●		N20	4.5V-15V	12 μV	1.1%	50 dB	Also FM, audio
LM3820	●	●	●	N14	4.5V-16V	35 μV			External detector

AM STEREO DECODER

	Application			Package	Voltage Range	Separation	THD	Signal to Noise	Notes
	Portable	Home	Auto						
LM1981		●	●	N20	8V-18V	30 dB	1.0%	55 dB	Decodes all systems

Note: Availability of the LM1981 in production quantities is dependent upon FCC system selection.

FM IF/DETECTOR

	Application			Package	Voltage Range	Input Sensitivity	Signal to Noise	THD	Mute Control	AGC Outputs	AFC	Meter Drive
	Portable	Home	Auto									
LM1865		●	●	N20	7V-16V	6 μV	84 dB	0.15%	●	●	●	●
LM1866	●	●	●	N20	3V-15V	12 μV	76 dB	0.5%	●		●	●
LM1868	●	●		N20	4.5V-15V	15 μV	64 dB	1.1%				
LM3011	●	●		H10	6V-15V	300 μV						
LM3075	●	●	●	N14	8.5V-12.5V	250 μV		1.5%				
LM3089		●	●	N16	8V-16V	12 μV	70 dB	0.5%	●	●	●	●
LM3189		●	●	N16	8V-16V	12 μV	80 dB	0.5%	●	●	●	●
TBA120	●	●	●	N14	6V-18V	30 μV		0.5%				

FM STEREO DECODER

	Application			Package	Voltage Range	THD	Channel Separation	Blend	High Cut	Lamp Driver	Output Buffer	ARI Interface Rejection
	Portable	Home	Auto									
LM1310		●		N14	10V-18V	0.3%	45 dB			●		
LM1800		●		N16	10V-18V	0.1%	45 dB			●	●	
LM1870	●	●	●	N20	7V-15V	0.25%	45 dB	●	●	●	●	
LM4500A	●	●	●	N16	8V-16V	0.1%	40 dB	●		●	●	●

PREAMPLIFIERS

	Application			Package	Voltage Range	Equivalent Input Noise	THD	PSR	Input Coupling	Notes
	Portable	Home	Auto							
LM381	●	●		N14	9V-40V	0.5 μV	0.1%	120 dB	AC	Stereo
LM382	●	●	●	N14	9V-40V	0.8 μV	0.1%	120 dB	AC	Stereo
LM387	●	●	●	N08	9V-30V	0.65 μV	0.1%	110 dB	AC	Stereo
LM1303		●		N14	10V-30V	0.8 μV			AC	Stereo
LM1818	●	●	●	N20	3.5V-18V	0.85 μV	0.05%	85 dB	AC	Tape system
LM1837	●	●	●	N18	4V-18V	0.6 μV†	0.03%	105 dB	DC	Autoreverse
LM1897	●	●	●	N16	4V-18V	0.6 μV†	0.03%	105 dB	DC	Few externals

†CCIR/ARM in DIN circuit referred to gain at 1 kHz.

*Note that all values shown are typical. Please refer to data sheets for test conditions.

Audio/Radio Selection Guide

National Semiconductor

AUDIO CONTROLS

	Application			Package	Voltage Range	Volume Control Range	Signal to Noise	THD	Separation	Notes
	Portable	Home	Auto							
LM1035	●	●	●	N20	8V-18V	80 dB	80 dB	0.05%	70 dB	Dual DC tone/volume/balance
LM1037	●	●	●	N18	5V-30V		100 dB	0.04%	100 dB	DC audio switch
LM1038	●	●	●	N18	5V-30V		100 dB	0.04%	100 dB	BCD input
LM13600 LM13700	●	●	●	N16	± 2V- ± 18V			0.5%	100 dB	Transconductance amplifiers

NOISE REDUCTION

	Application			Package	Voltage Range	NR Type	NR Effect	Encoding Required	Single/ Dual	Decode S/N	Notes
	Portable	Home	Auto								
LM1111	●	●	●	N16	6V-18V	Dolby	10 dB	Yes	Single	83 dB	Tightened spec
LM1121	●	●	●	N16	6V-18V	Dolby	10 dB	Yes	Single	82 dB	DC switched
LM1131	●	●	●	N18	6V-18V	Dolby	10 dB	Yes	Dual	87 dB	DC switched
LM1894	●	●	●	N14	4.5V-18V	DNR	12 dB	No	Dual	76 dB	NSC system
LM13700		●		N16	± 15V	C-X	20 dB	Yes	**		Phono
LF347		●		N14	± 15V	C-X	20 dB	Yes	**		Phono
LF353		●		N08	± 15V	C-X	20 dB	Yes	**		Phono

**The C-X system requires one LM13700 and 8-10 op amps for stereo phono noise reduction.

AUDIO POWER AMPLIFIERS

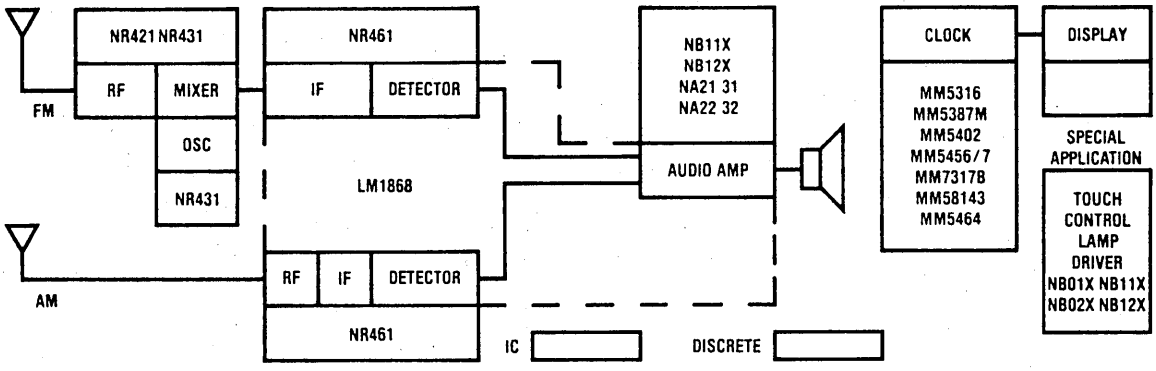
	Application			Package	Power			@ Voltage	Bridgeable	THD	Input Noise	Single/ Dual	Notes
	Portable	Home	Auto		8Ω	4Ω	2Ω						
LM378		●		N14	5W			24V	Yes	0.1%	3 μV	Dual	See AN-125
LM379		●		S14	6W			28V	Yes	0.2%	3 μV	Dual	See AN-125
LM380		●		N14/N08	2.5W			18V		0.2%		Single	See AN-69
LM383	●		●	TO-5		5.5W	8.6W	14.4V	Yes	0.2%	2 μV	Single	Protected
LM384		●		N14	5.5W			22V		0.25%		Single	Fixed gain
LM386	●	●		N08		0.33W		6V		0.2%		Single	4V operation
LM388	●			N14	2.2W			12V	Yes	0.1%		Single	Minimum externals
LM389	●			N18		0.33W		6V		0.2%		Single	Includes Transistor array
LM390	●			N14		1W		6V	Yes	0.2%		Single	Battery operation
LM391		●		N16				60V-100V		0.01%	3 μV	Single	Power driver
LM1868	●	●		N20	0.7W			9V		0.2%		Single	With AM/FM
LM1877	●	●	●	N14	2W			20V		0.05%	25 μV	Dual	6V-24V
LM2877	●	●	●	P11	4.5W			20V		0.1%	2.5 μV	Dual	Single-in-line package
LM1895	●	●	●	N08		1.1W		6V		0.2%	14 μV	Single	Low AM radiation
LM2895	●	●	●	P11		4.3W		12V		0.15%	1.4 μV	Single	3V-15V
LM1896	●	●	●	N14		1.1W		6V	Yes	0.1%	1.4 μV	Dual	Low AM radiation
LM2896	●	●	●	P11		2.5W		9V	Yes	0.1%	1.4 μV	Dual	No pops
LM2002	●		●	TO-5		5.2W	8W	14.4V	Yes	0.1%	2 μV	Single	Protected
LM2878		●		P11	5.5W			22V		0.15%	2.5 μV	Dual	6V-32V

*Note that all values shown are typical. Please refer to data sheets for test conditions.

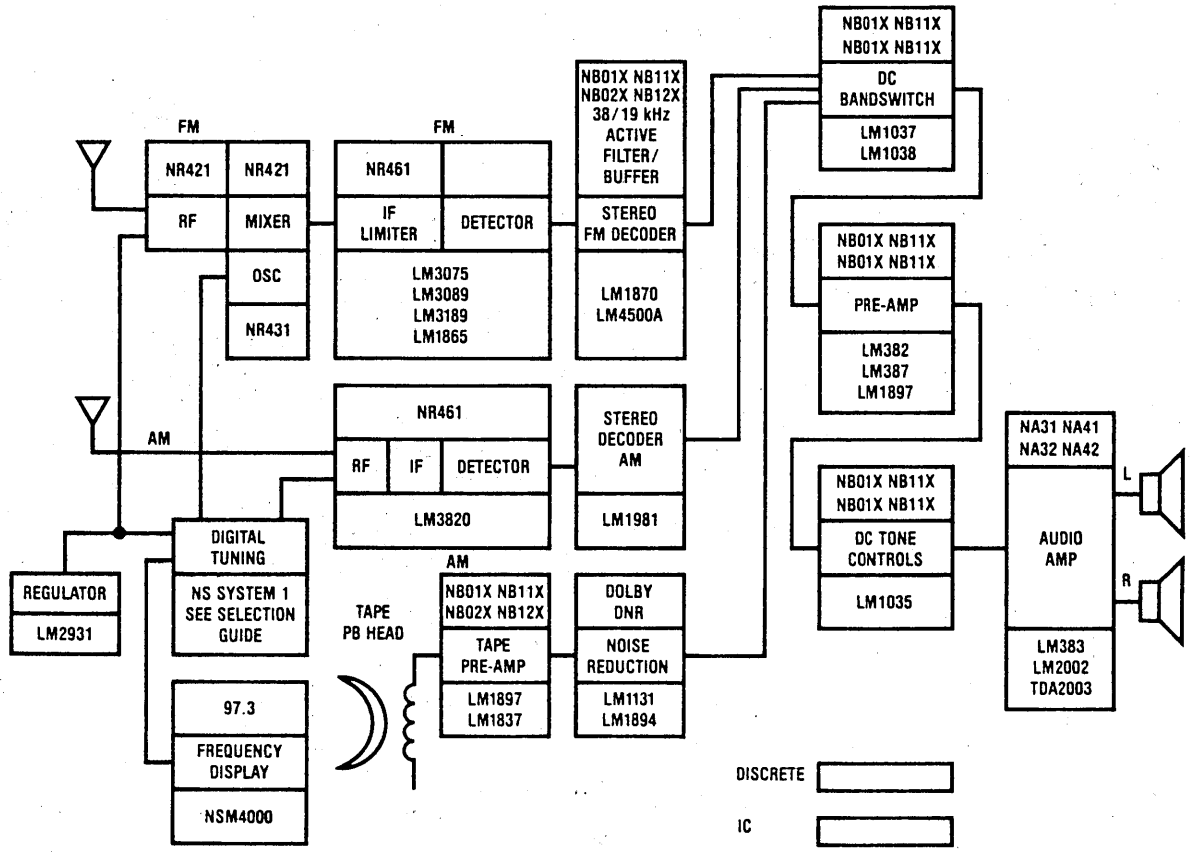
National Semiconductor

Audio/Radio Selection Guide

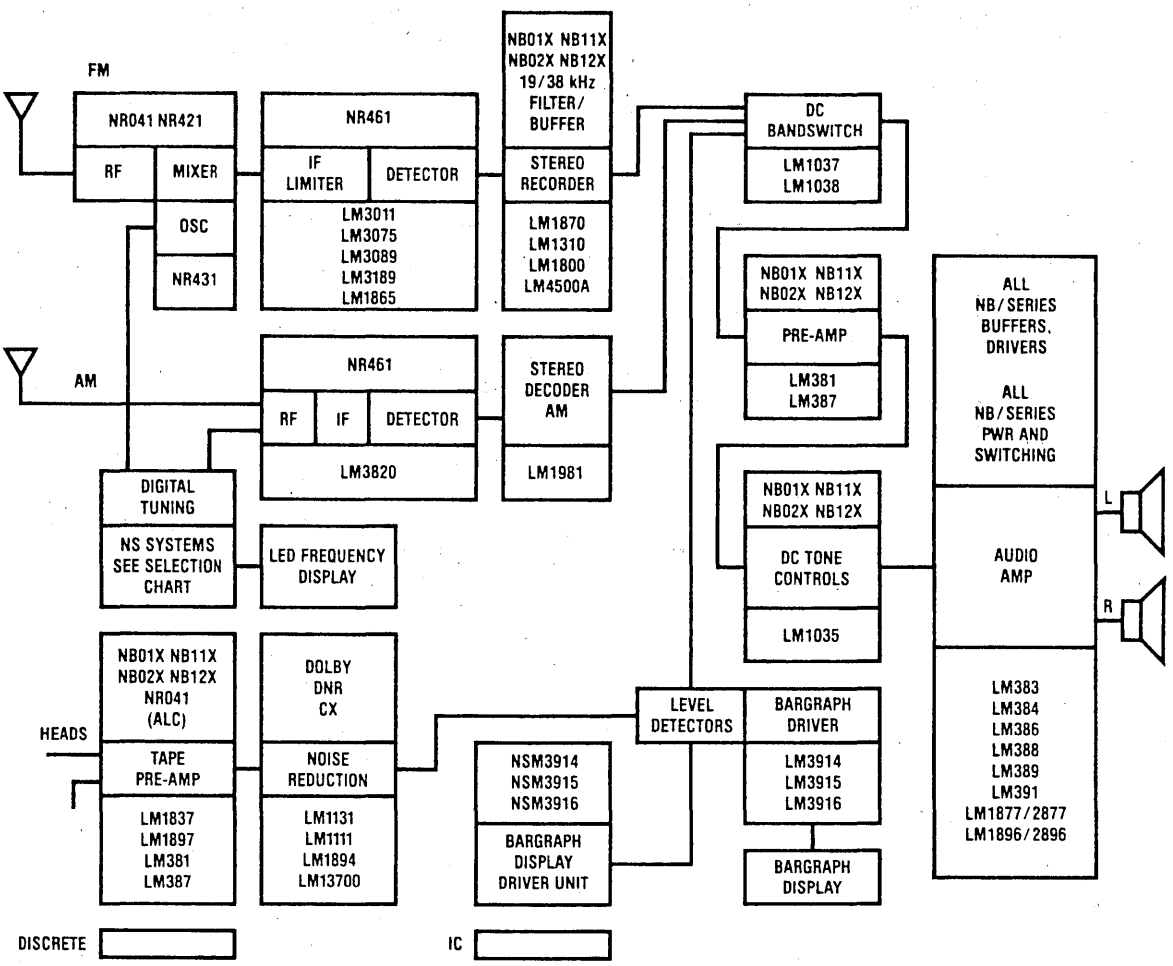
Clock Radio



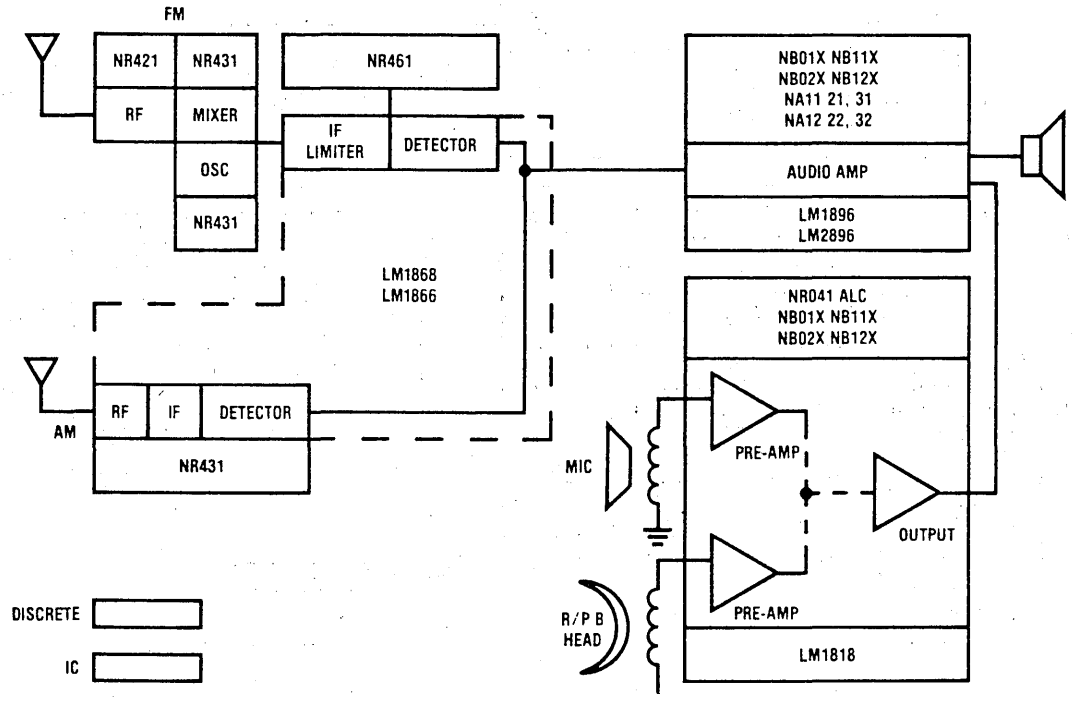
Car Stereo



Home Music System



Portable Mono Cassette Radio



National Semiconductor

June 1982

LM1822 Video IF Amplifier/PLL Detector System

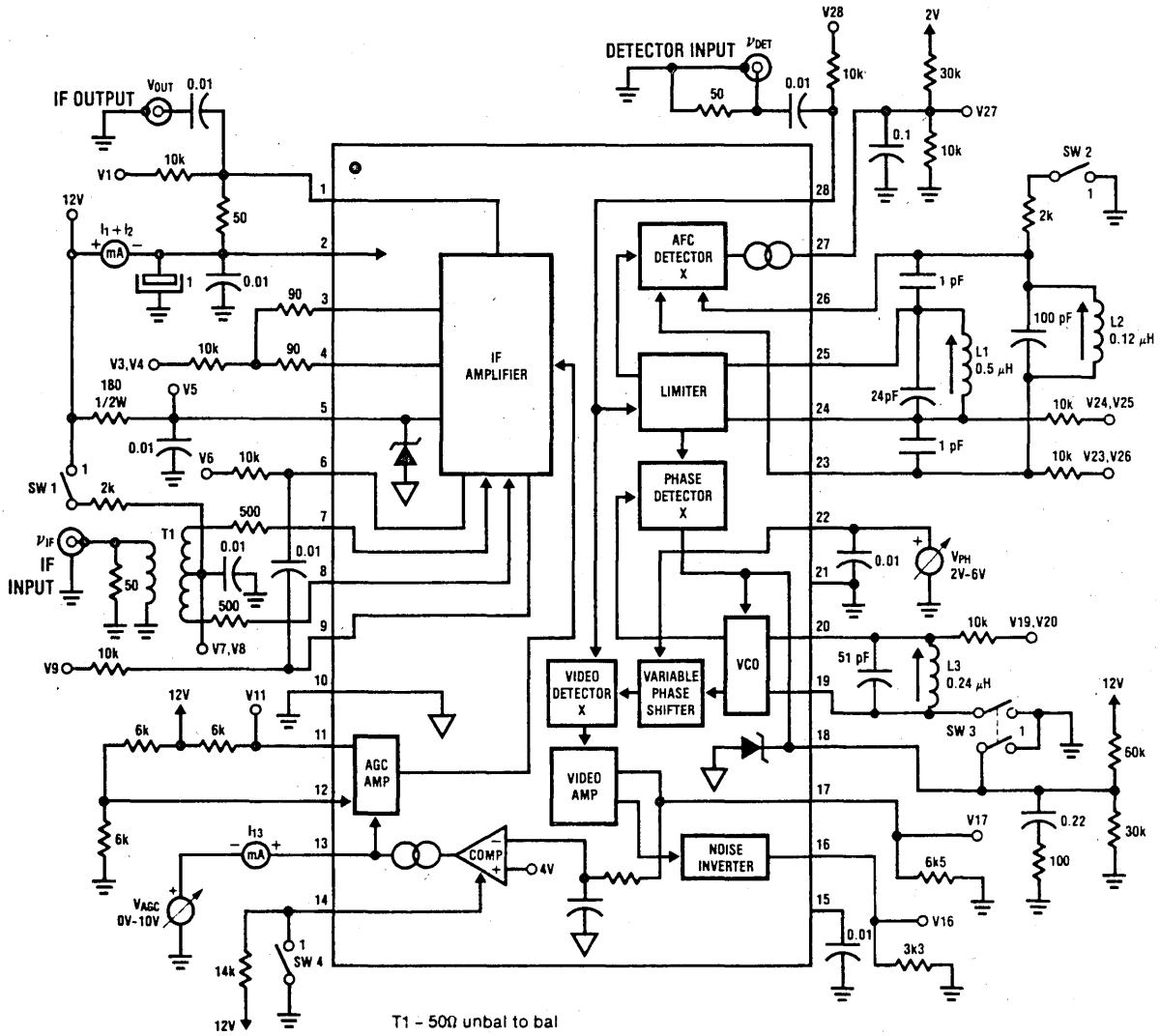
General Description

The LM1822 is a complete video IF signal processing system on a chip. It contains a 5-stage gain-controlled IF amplifier, a PLL synchronous detector with noise inversion, a flexible AFC detector, and gated AGC. This device is suitable for all home receiver and cable IF applications requiring high quality video recovery, including systems operating at 38.9 MHz, 45.75 MHz, 58.75 MHz, and 61.25 MHz.

Features

- Common-base IF inputs for SAW filters
- True synchronous video detector using PLL
- Excellent stability at high system gains
- Noise-averaged gated AGC system
- Superior small-signal detector linearity
- AFC detector with adjustable output bias
- System operation to 70 MHz
- All NPN video amplifiers
- White spot noise inversion
- Adjustable output zero carrier level
- Reverse tuner AGC output

Test Circuit Measure parameters at indicated test points



T1 - 50Ω unbal to bal
Mini-Circuits Lab TM01-1T

L1 - 9 1/2T
L2 - 4 1/2T
L3 - 6 1/2T
#22 wire on 3/16" form with HF core, shielded

All caps in µF unless noted

IM B25M02 Printed in U.S.A.

National Semiconductor

PRELIMINARY
August 1982

LM1875 20 Watt Power Audio Amplifier

General Description

The LM1875 is a monolithic power amplifier offering very low distortion and high quality performance for consumer audio applications.

The LM1875 delivers 20 watts into a 4Ω or 8Ω load on ±22V supplies. Using an 8Ω load and ±30V supplies, over 30 watts of power may be delivered. The amplifier is designed to operate with a minimum of external components. Device overload protection consists of both internal current limit and thermal shutdown.

The LM1875 design takes advantage of circuit techniques and processing to achieve extremely low levels of distortion even at high levels of output power. Other outstanding features include high gain, fast slew rate and a wide power bandwidth, large output voltage swing, high current capability, and a very wide supply range. The amplifier is also internally compensated and stable for gains of 10 or greater.

Features

- 30 watts of output power
- A_{VO} typically 90 dB
- Low distortion 0.05%, 1 kHz, 20W
- Wide power bandwidth 70 kHz
- Short circuit protection
- Thermal protection with parole circuit
- High current capability 3A
- Wide supply range 20V–60V
- Internal compensation
- 94 dB ripple rejection
- Plastic power package TO-220

Applications

- High performance audio systems
- Bridge amplifiers
- Stereo phonographs
- Servo amplifiers
- Instrument systems

Typical Applications

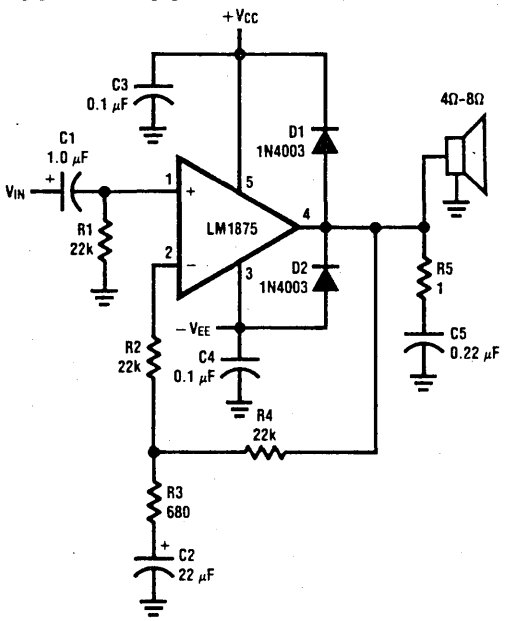
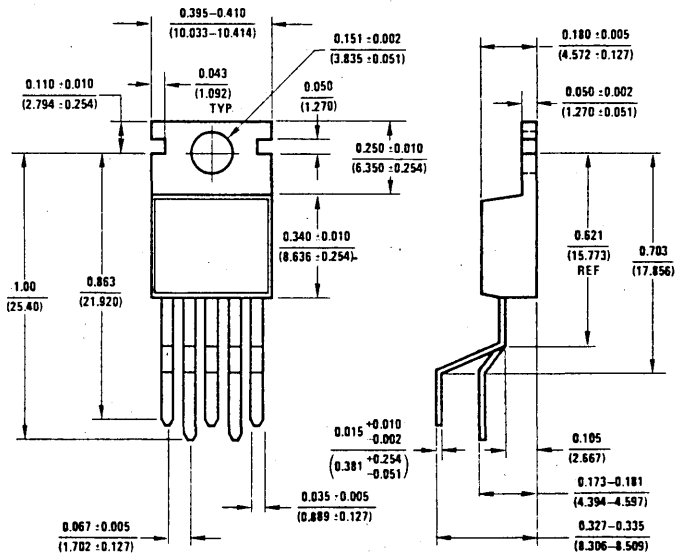


FIGURE 1. Test Circuit and Typical Split Supply Operation

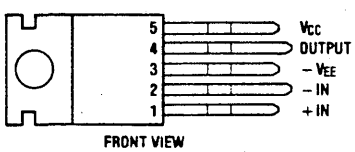
Physical Dimensions inches (millimeters)



TO-220 Power Package (T)
Order Number LM1875T
NS Package Number T05B

Connection Diagram

TO-220 Power Package (T)



FRONT VIEW

IM-B25M82/Printed in U.S.A.

National Semiconductor

LM1893 2-Wire Bidirectional Communication System

Technical Description

The LM1893 is a bipolar transceiver IC for interfacing to the power lines (AC or DC) in a carrier current system. An external logic command to the TX/RX SELECT pin puts the chip in either the transmit or receive mode. In the transmit mode, a sinusoidal current at the carrier center frequency is modulated to produce an FSK signal to drive the power line via a small (10 mm × 10 mm) inexpensive tuned transformer. Serial data fed into the DATA IN pin modulates the low TC current controlled oscillator (ICO). The triangle wave output of the oscillator is passed through a sine shaper circuit to the power current amplifier. Automatic level control (ALC) circuitry maintains output waveform purity despite wide changes in power line impedance.

In the receive mode, a tuned transformer attenuates 60 Hz and noise while stepping up signal voltage to the limiter amplifier. A PLL demodulates the signal which then passes through a 3-stage, low pass filter on its way to the offset cancel circuit. The comparator separates the ones from the zeroes and drives the time domain filter, which is particularly effective against impulse noise. The output is available at the DATA OUT pin in the form of the free collector of an NPN transistor.

Features

- Self-contained transmitter and receiver in one 18-pin package.
- Half-duplex (bidirectional) operation.
- Handles serial digital data of virtually any coding.
- Compatible with TTL or MOS logic and μPs.
- Handles analog signals.
- Employs noise resistant FSK modulation.
- Programmable carrier frequency.
- Programmable impulse noise filtering.
- Built-in transient protection.
- Low distortion (low harmonic) transmitter output minimizes potential RFI.
- Regulated voltage available to power logic.

Typical Performance

General

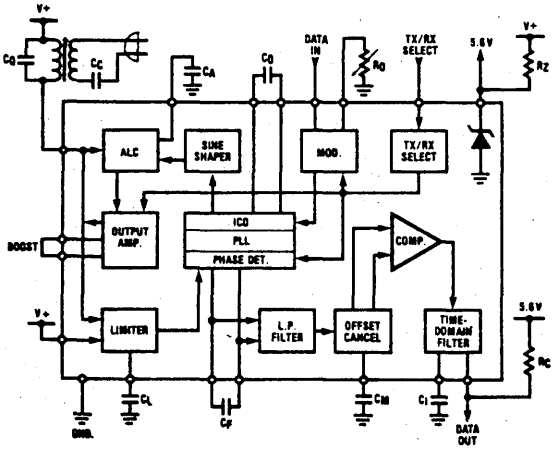
Supply Voltage	18 V
Programmable Carrier Freq., F_o	50 to 300 kHz
Oscillator TC of F_o	±100 ppm/°C

Transmitter

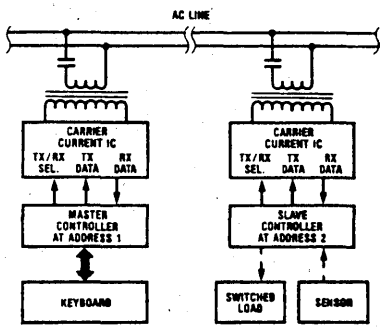
FSK Deviation	±2.5%
Output Current	60 mApp
Output Voltage (Line Z = 10Ω)	4.0 Vpp
Output Voltage Distorton (Q = 10 tank)	0.1%
Power Output (Line Z = 10Ω)	200 mW
RX to TX Switchover Time	40 μs
Supply Current	38 mA

Receiver

Sensitivity	1 mV rms
Data Rate	0 to 4 k Baud
TX to RX Switchover Time	2 Bits
Supply Current	13 mA



Block diagram of the LM1893 showing the typical complement of external parts.



A typical application may use LM1893's and low cost μP's in an energy management system.

National Semiconductor

October 1982

TP3020/TP3021 Monolithic CODECs

General Description

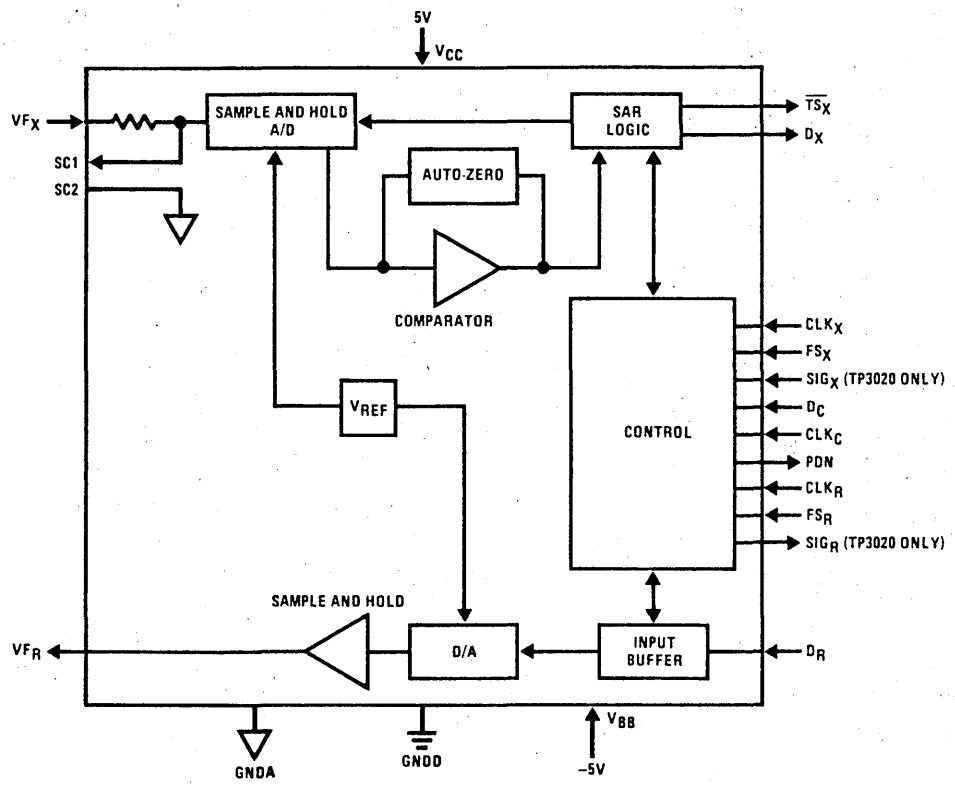
The TP3020 and TP3021 are monolithic PCM CODECs implemented with double-poly CMOS technology. The TP3020 is intended for μ-law applications and contains logic for μ-law signaling insertion and extraction. The TP3021 is intended for A-law applications.

Each device contains separate D/A and A/D circuitry, all necessary sample and hold capacitors, a precision voltage reference and internal auto-zero circuit. A serial control port allows an external controller to individually assign the PCM input and output ports to one of up to 32 time slots or to place the CODEC into a power-down mode. Alternately, the TP3020/TP3021 may be operated in a fixed time slot mode. Both devices are intended to be used with the TP3040 monolithic PCM filter which provides the input anti-aliasing function for the encoder and smoothes the output of the decoder and corrects for the sin x/x distortion introduced by the decoder sample and hold output.

Features

- Low operation power—45 mW typical
- Low standby power—1 mW typical
- ±5V operation
- TTL compatible digital interface
- Time slot assignment or alternate fixed time slot modes
- Internal precision reference
- Internal sample and hold capacitors
- Internal auto-zero circuit
- TP3020—μ-law coding with signaling capabilities
- TP3021—A-law coding
- Synchronous or asynchronous operation

Simplified Block Diagram



National Semiconductor

October 1982

TP3040/TP3040A PCM Monolithic Filter

General Description

The TP3040/TP3040A filter is a monolithic circuit containing both transmit and receive filters specifically designed for PCM CODEC filtering applications in 8 kHz sampled systems.

The filter is manufactured using double-poly silicon gate CMOS technology. Switched capacitor integrators are used to simulate classical LC ladder filters which exhibit low component sensitivity.

TRANSMIT FILTER STAGE

The transmit filter is a fifth order elliptic low pass filter in series with a fourth order Chebyshev high pass filter. It provides a flat response in the passband and rejection of signals below 200 Hz and above 3.4 kHz.

RECEIVE FILTER STAGE

The receive filter is a fifth order elliptic low pass filter designed to reconstruct the voice signal from the decoded/demultiplexed signal which, as a result of the sampling process, is a stair-step signal having the inherent sin x/x frequency response. The receive filter approximates the function required to compensate for the degraded frequency response and restore the flat passband response.

Features

- Exceeds all D3/D4 and CCITT specifications
- +5V, −5V power supplies
- Low power consumption:
  45 mW (0 dBm0 into 600Ω)
  30 mW (power amps disabled)
- Power down mode: 0.5 mW
- 20 dB gain adjust range
- No external anti-aliasing components
- Sin x/x correction in receive filter
- 50/60 Hz rejection in transmit filter
- TTL and CMOS compatible logic
- All inputs protected against static discharge due to handling

Block and Connection Diagrams

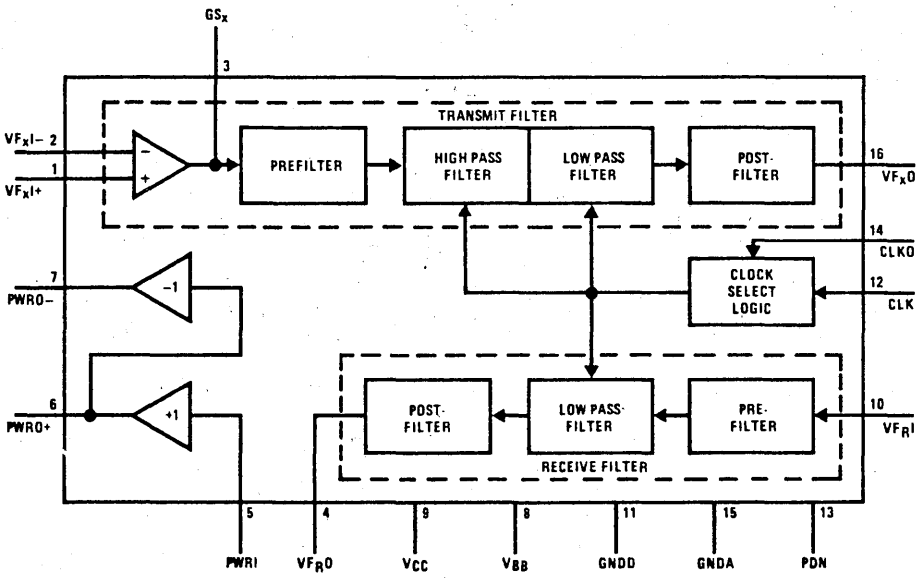
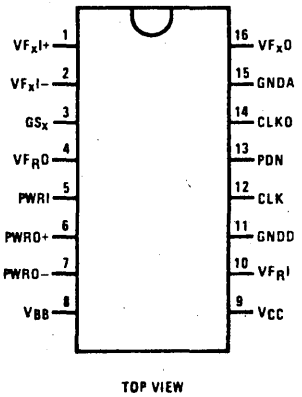


FIGURE 1

Dual-In-Line Package



TOP VIEW

National Semiconductor

PRELIMINARY
October 1982

TP3051, TP3056 Monolithic Parallel Data Interface CMOS CODEC/Filter Family

General Description

The TP3051, TP3056 family consists of a μ-law and A-law monolithic PCM CODEC/filter set utilizing the A/D and D/A conversion architecture shown in *Figure 1*, and a parallel I/O data bus interface. The devices are fabricated on National's advanced double-poly CMOS process (P^2CMOS).

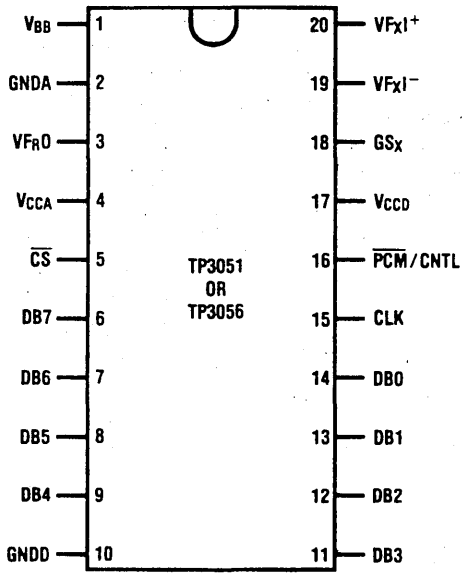
The transmit section consists of an input gain adjust amplifier, an active RC pre-filter, and a switched-capacitor bandpass filter that rejects signals below 200 Hz and above 3400 Hz. A compressing coder samples the filtered signal and encodes it in the μ-255 law or A-law PCM format. Auto-zero circuitry is included on-chip. The receive section consists of an expanding decoder which reconstructs the analog signal from the compressed μ-law or A-law code, and a low pass filter which corrects for the sin x/x response of the decoder output and rejects signals above 3400 Hz. The receive output is a single-ended power amplifier capable of driving low impedance loads. The TP3051 μ-law and TP3056 A-law devices are pin compatible parallel interface CODEC/filters for bus-oriented systems. They are ideally suited for use with the TP3100 family of digital line interface controllers (DLIC) in switching system applications. The DLIC communicates with the main switch controller via integrated data, signaling and control channels, and provides local time-slot and space switching capability for up to 32 TP3051 or TP3056 CODECs.

Features

- Complete CODEC and filtering system including:
  - -Transmit high pass and low pass filtering
  - -Receive low pass filter with sin x/x correction
  - -Receive power amplifier
  - -Active RC noise filters
  - -μ-255 law COder and DECoder—TP3051
  - -A-law COder and DECoder—TP3056
  - -Internal precision voltage reference
  - -Internal auto-zero circuitry
- Meets or exceeds all D3/D4 and CCITT specifications
- ±5V operation
- Low operating power—typically 60 mW
- Power-down standby mode—typically 3 mW
- High speed TRI-STATE® data bus
- 2 loopback test modes

Connection Diagram

Dual-In-Line Package



TOP VIEW

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IM-B25M52/Printed in U.S.A.

National Semiconductor

PRELIMINARY
October 1982

TP3052, TP3053, TP3054, TP3057 Monolithic Serial Interface CMOS CODEC/FILTER Family

General Description

The TP3052, TP3053, TP3054, TP3057 family consists of μ-law and A-law monolithic PCM CODEC/filters utilizing the A/D and D/A conversion architecture shown in *Figure 1*, and a serial PCM interface. The devices are fabricated using National's advanced double-poly CMOS process (P^2CMOS^{TM}).

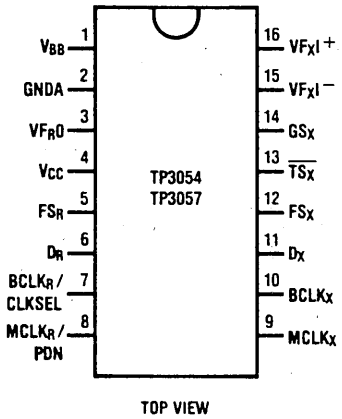
The encode portion of each device consists of an input gain adjust amplifier, an active RC pre-filter which eliminates very high frequency noise prior to entering a switched-capacitor band-pass filter that rejects signals below 200 Hz and above 3400 Hz. Also included are auto-zero circuitry and a companding coder which samples the filtered signal and encodes it in the companded μ-law or A-law PCM format. The decode portion of each device consists of an expanding decoder, which reconstructs the analog signal from the companded μ-law or A-law code, a low-pass filter which corrects for the sin x/x response of the decoder output and rejects signals above 3400 Hz and is followed by a single-ended power amplifier capable of driving low impedance loads. The devices require two 1.536 MHz, 1.544 MHz or 2.048 MHz transmit and receive master clocks, which may be asynchronous, transmit and receive bit clocks, which are synchronous with the master clocks but may vary from 64 kHz to 2.048 MHz, and transmit and receive frame sync pulses. The timing of the frame sync pulses and PCM data is compatible with both industry standard formats.

Features

- Complete CODEC and filtering system (COMBO) including:
  - -Transmit high-pass and low-pass filtering
  - -Receive low-pass filter with sin x/x correction
  - -Active RC noise filters
  - -μ-law or A-law compatible COder and DECoder
  - -Internal precision voltage reference
  - -Serial I/O interface
  - -Internal auto-zero circuitry
- μ-law with signaling, TP3020 timing—TP3052
- μ-law with signaling, TP5116A family timing—TP3053
- μ-law without signaling, 16-pin—TP3054
- A-law, 16-pin—TP3057
- Meets or exceeds all D3/D4 and CCITT specifications
- ±5V operation
- Low operating power—typically 60 mW
- Power-down standby mode—typically 3 mW
- TTL or CMOS compatible digital interfaces
- Maximizes line interface card circuit density

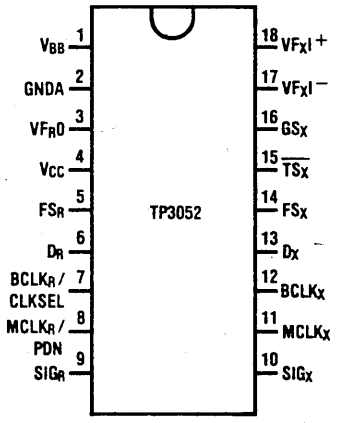
Connection Diagrams

Dual-In-Line Package



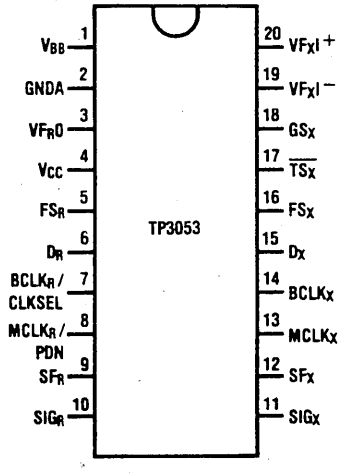
TOP VIEW

Dual-In-Line Package



TOP VIEW

Dual-In-Line Package



TOP VIEW

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PRELIMINARY
October 1982

TP3110, TP3120 Digital Line Interface Controllers (DLIC)

General Description

The TP3110, TP3120 Digital Line Interface Controllers (DLIC) are general purpose switching components primarily intended to serve as controllers of subscriber line, service and trunk circuit cards of a digital switching system. They are also useful as general purpose data controllers for data switching and multiplexing applications.

The DLIC performs a three-way control function when used for digital switching applications. The block diagram *(Figure 1)* displays this tri-port arrangement. First, the DLIC controls the space and time switching function between subscriber line PCM CODECs and filters and the switching system time division multiplex (TDM) highways. Second, the DLIC controls the flow of information between the per line circuit devices and the line card's local processor. Last, it performs all protocol control functions, using the HDLC protocol format, for information passing between the local line card processor and the main switching system processor (or any other system processor).

The DLIC is configured with a parallel interface for the per line and local processor circuits and with full duplex multiple port serial highways for the system interface. All system related communications with the DLIC controlled circuit card are handled via channel assignments on the serial TDM interface. In this way, all system data communications, subscriber PCM, data, signaling and system control information are transported and switched with a single network. This approach improves the overall flexibility and modularity of the total system design.

The DLIC contains a time-slot memory map for up to 128 duplex TDM channels, four high speed serial port transceivers, interface logic to allow the local processor to communicate with the per line circuit devices (combination CODEC/filter circuits and the SLIC), a complete HDLC protocol controller for system control messages, a vectored interrupt controller for the HDLC protocol, signaling and timing control and finally, a buffer memory for per line signaling data.

Features

- A complete interface controller for up to 32 subscribers of a digital switching system
- Performs all time division multiplex (TDM) channel assignments for the circuit card it controls
- Provides two (TP3110) or four (TP3120) full duplex serial TDM highways for the system interface
- Interfaces TP3051, TP3056 parallel CODEC/Filters
- Performs the first stage space and time switching function to minimize hardware requirements and switching delay
- Assignable addressing plus a "broadcast" address allows up to 255 controllers per subsystem control group without address field overlap
- System control uses the HDLC protocol with all zero insertion/deletion, checksum and flag control functions performed by the DLIC
- Single 5V power supply operation

Block Diagram

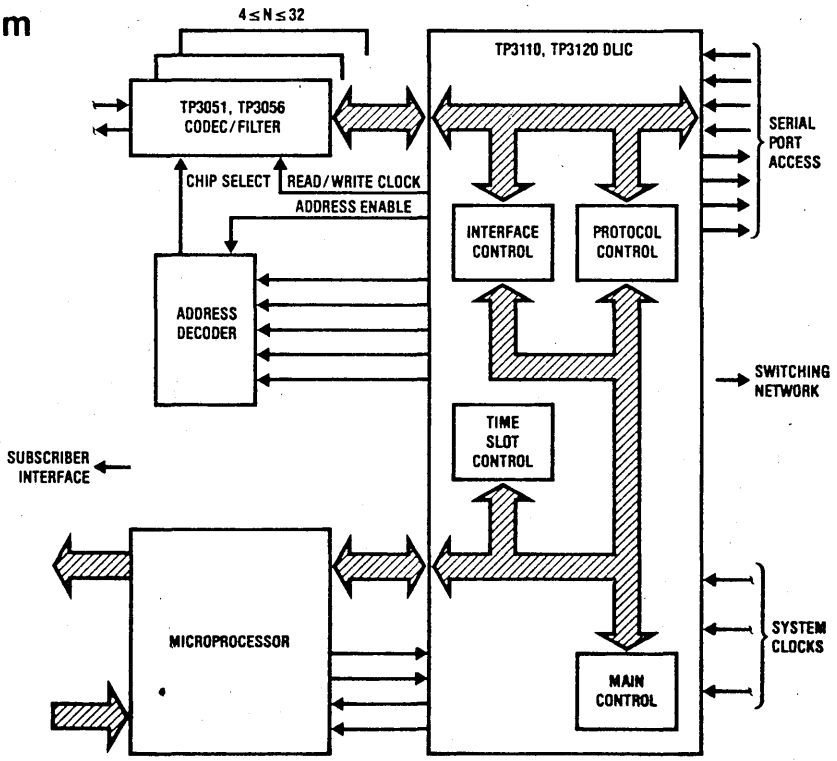


FIGURE 1. DLIC Signal Flows

National Semiconductor

October 1982

TP5116A, TP5117A, TP5156A Monolithic CODECs

General Description

The TP5116A, TP5117A and TP5156A are monolithic PCM CODECs implemented with double-poly CMOS technology. The TP5116A and TP5117A are intended for μ-law applications and the TP5156A is for A-law applications. The TP5117A has a D3 compatible format for line card compatibility with the TP5156A.

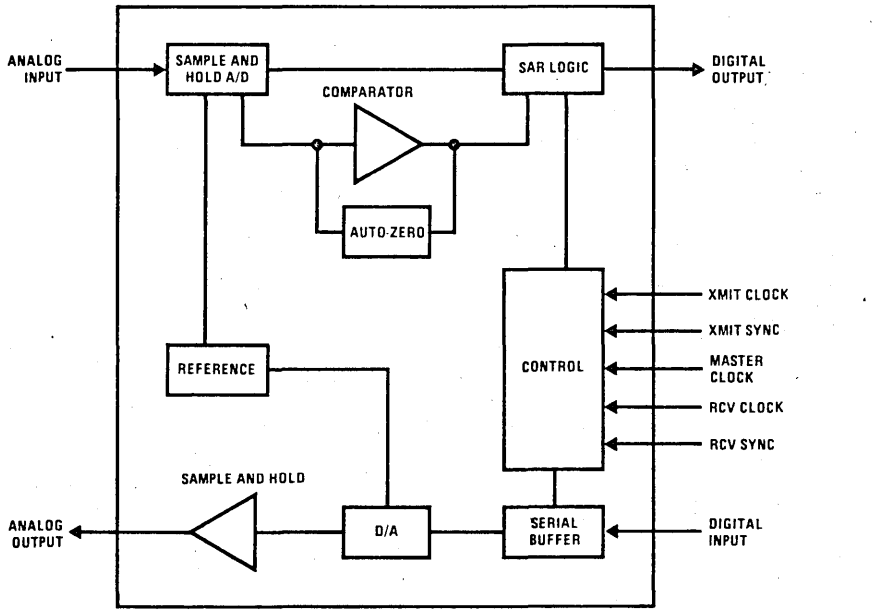
Each device contains separate D/A and A/D circuitry, all necessary sample and hold capacitors, and internal auto-zero circuits. Each device also contains a precision internal voltage reference, eliminating the need for an external reference. There are no internal connections to pins 15 or 16, making them directly interchangeable with CODECs using external reference components.

All devices are intended to be used with the TP3040 monolithic PCM filter which provides the input anti-aliasing function for the encoder and smooths the output of the decoder and corrects for the sin x/x distortion introduced by the decoder sample and hold output.

Features

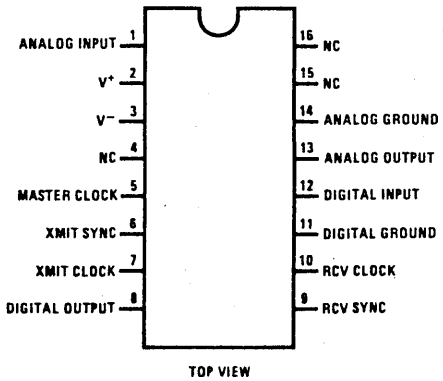
- Low operation power—40 mW typical
- ±5V operation
- TTL compatible digital interface
- Precision voltage reference on-chip
- Internal sample and hold capacitors
- Internal auto-zero circuit
- TP5116A—μ-law coding (sign plus magnitude format)
- TP5117A—μ-law, D3 compatible format
- TP5156A—A-law coding
- Synchronous or asynchronous operation

Simplified Block Diagram



Connection Diagram

Dual-In-Line Package



TOP VIEW

DT1000 DIGITALKER™ Speech Synthesis Evaluation Board

General Description

The DIGITALKER™ (DT1000) speech synthesis evaluation board is an extremely easy to use device for understanding the operation and application of the DIGITALKER chip set in an end product.

The DT1000 contains all components required to output speech upon demand: a speech processor chip (SPC), 2 MAXI-ROMs® containing 138 individual words, linear filter, audio amplifier, keyboard, and a COPS™ microcontroller complete with stored data programmed to provide the various functions on the board. The only external hardware required for complete operation are a single 7V–11V power supply, a speaker of your choice for size and quality, and this instruction sheet.

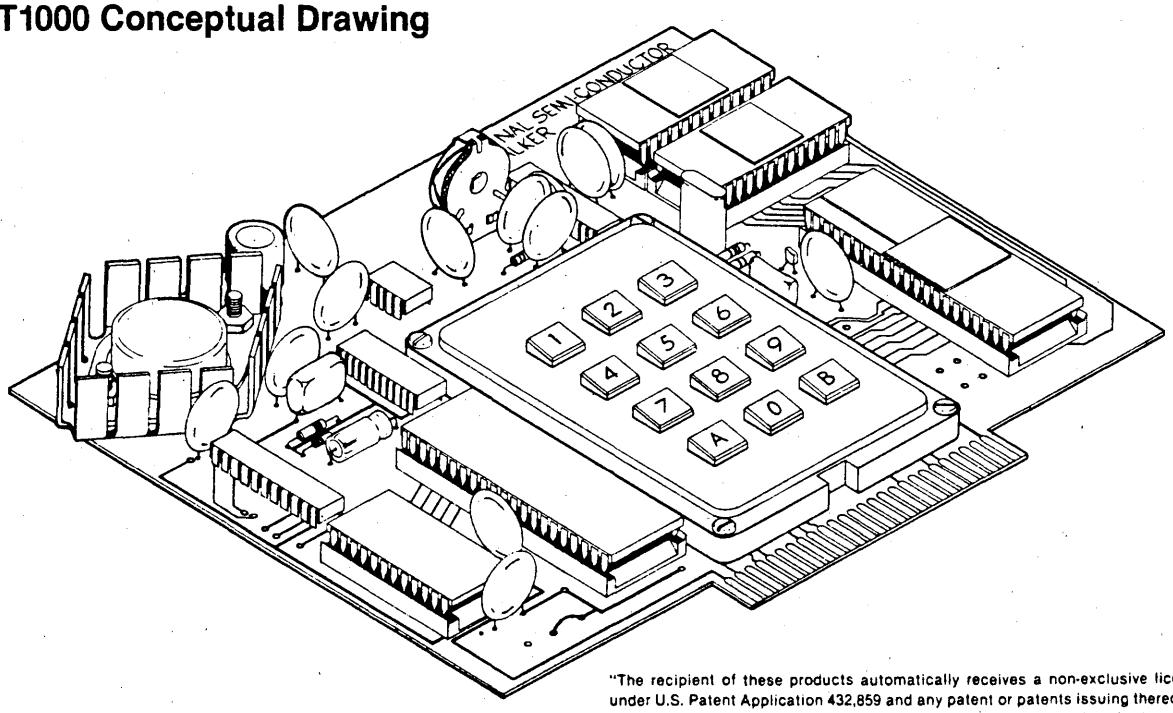
The 2 speech MAXI-ROMs employed on the board contain a brief introductory phrase, 138 separate and individual words consisting of numbers and letters of the alphabet, assorted useful nouns, verbs and tones; and 5 different individual silence durations. (In constructing a phrase, different silence durations between different words significantly affect the overall quality of the phrase.)

A COPS program is provided which permits the user to: 1) sequentially output each word automatically; 2) repeat any desired word; 3) build and store several short phrases for outputting when desired; 4) output a "canned" phrase which permits insertions and changing of a word in the phrase; 5) play a simple game which requires some interaction between the keyboard and the user; and 6) output hex equivalent decimal number inputs.

Features

- Only a single 7V–11V power supply and inexpensive loudspeaker required for total operation
- 138 individually addressable words, applicable to many products
- Programmed COPS processor permits 6 individual program modes
- Demonstrates the extreme flexibility and ease of application of the DIGITALKER chip set
- 1/2 watt audio amplifier on-board
- Edge connector facilitates tying in to external processor system (3M Company connector part number #3415)

DT1000 Conceptual Drawing



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DT1000 Master Word List

Word	Keyboard Address	8-Bit Binary Address SW8 SW1
THIS IS DIGITALKER	000	00000000
ONE	001	00000001
TWO	002	00000010
THREE	003	00000011
FOUR	004	00000100
FIVE	005	00000101
SIX	006	00000110
SEVEN	007	00000111
EIGHT	008	00001000
NINE	009	00001001
TEN	010	00001010
ELEVEN	011	00001011
TWELVE	012	00001100
THIRTEEN	013	00001101
FOURTEEN	014	00001110
FIFTEEN	015	00001111
SIXTEEN	016	00010000
SEVENTEEN	017	00010001
EIGHTEEN	018	00010010
NINETEEN	019	00010011
TWENTY	020	00010100
THIRTY	021	00010101
FORTY	022	00010110
FIFTY	023	00010111
SIXTY	024	00011000
SEVENTY	025	00011001
EIGHTY	026	00011010
NINETY	027	00011011
HUNDRED	028	00011100
THOUSAND	029	00011101
MILLION	030	00011110
ZERO	031	00011111
A	032	00100000
B	033	00100001
C	034	00100010
D	035	00100011
E	036	00100100
F	037	00100101
G	038	00100110
H	039	00100111
I	040	00101000
J	041	00101001
K	042	00101010
L	043	00101011
M	044	00101100
N	045	00101101
O	046	00101110
P	047	00101111
Q	048	00110000
R	049	00110001
S	050	00110010
T	051	00110011
U	052	00110100
V	053	00110101
W	054	00110110
X	055	00110111
Y	056	00111000
Z	057	00111001
AGAIN	058	00111010
AMPERE	059	00111011
AND	060	00111100
AT	061	00111101
CANCEL	062	00111110
CASE	063	00111111
CENT	064	01000000
400HERTZ TONE	065	01000001
80HERTZ TONE	066	01000010
20MS SILENCE	067	01000011
40MS SILENCE	068	01000100
80MS SILENCE	069	01000101
160MS SILENCE	070	01000110
320MS SILENCE	071	01000111
CENTI	072	01001000
CHECK	073	01001001
COMMA	074	01001010
CONTROL	075	01001011
DANGER	076	01001100
DEGREE	077	01001101
DOLLAR	078	01001110
DOWN	079	01001111
EQUAL	080	01010000
ERROR	081	01010001
FEET	082	01010010
FLOW	083	01010011
FUEL	084	01010100
GALLON	085	01010101
GO	086	01010110
GRAM	087	01010111
GREAT	088	01011000
GREATER	089	01011001
HAVE	090	01011010
HIGH	091	01011011
HIGHER	092	01011100
HOUR	093	01011101
IN	094	01011110
INCHES	095	01011111
IS	096	01100000
IT	097	01100001
KILO	098	01100010
LEFT	099	01100011
LESS	100	01100100
LESSER	101	01100101
LIMIT	102	01100110
LOW	103	01100111
LOWER	104	01101000
MARK	105	01101001
METER	106	01101010
MILE	107	01101011
MILLI	108	01101100
MINUS	109	01101101
MINUTE	110	01101110
NEAR	111	01101111
NUMBER	112	01110000
OF	113	01110001
OFF	114	01110010
ON	115	01110011
OUT	116	01110100
OVER	117	01110101
PARENTHESIS	118	01110110
PERCENT	119	01110111
PLEASE	120	01111000
PLUS	121	01111001
POINT	122	01111010
POUND	123	01111011
PULSES	124	01111100
RATE	125	01111101
RE	126	01111110
READY	127	01111111
RIGHT	128	10000000
SS (Note 1)	129	10000001
SECOND	130	10000010
SET	131	10000011
SPACE	132	10000100
SPEED	133	10000101
STAR	134	10000110
START	135	10000111
STOP	136	10001000
THAN	137	10001001
THE	138	10001010
TIME	139	10001011
TRY	140	10001100
UP	141	10001101
VOLT	142	10001110
WEIGHT (Note 2)	143	10001111

Note 1: "SS" makes any singular word plural.

Note 2: Address 143 is the last legal address in this particular word list. Exceeding address 143 in an external processor application will produce pieces of unintelligible invalid speech data.

Note 3: The above vocabulary can also be purchased in a discrete component kit, called the DT1050 Standard Vocabulary Kit.

National Semiconductor

DIGITALKER™ Speech Synthesis

DT1056/DT1057 DIGITALKER™ Standard Vocabulary Kit

General Description

The DIGITALKER™ is a speech synthesis system consisting of several N-channel MOS integrated circuits. It contains a speech processor chip (SPC) and speech ROM and when used with external filter, amplifier, and speaker, produces a system which generates high quality speech including the natural inflection and emphasis of the original speech. Male, female, and children's voices can be synthesized.

The SPC communicates with the speech ROM, which contains the compressed speech data as well as the frequency and amplitude data required for speech output. Up to 128k bits of speech data can be directly accessed.

With the addition of an external resistor, on-chip debounce is provided for use with a switch interface.

An interrupt is generated at the end of each speech sequence so that several sequences or words can be cascaded to form different speech expressions.

The DT1056/DT1057 is a standard DIGITALKER kit encoded with 131 separate and useful words (see the Master Word List Table I) and when used with the DT1050 Standard Vocabulary Kit, provides a library of 274 useful words. The words have been assigned discrete addresses, making it possible to output single words or words concatenated into phrases or even sentences.

The "voice" output of the DT1056/DT1057 is a highly intelligible male voice. The vocabulary is chosen so that it is applicable to many products and markets.

Features

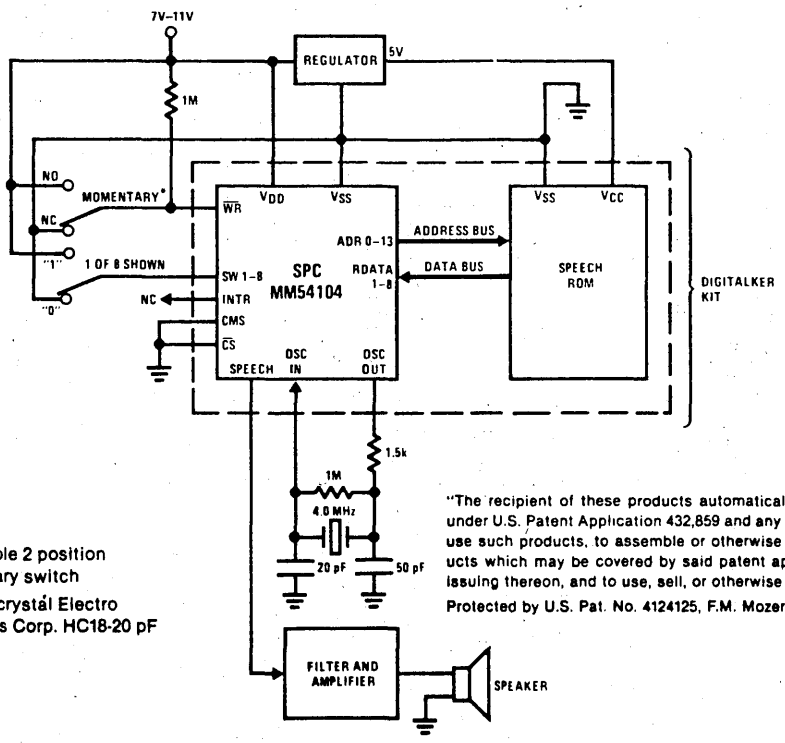
- Easily adaptable to DT1050 Standard Vocabulary Kit
- 131 useful words
- COPS™ and MICROBUS™ compatible
- Designed to be easily interfaced to other popular microprocessors
- Natural inflection and emphasis of original speech
- Addresses 128k bits of ROM directly
- TTL compatible
- On-chip switch debounce for interfacing to manual switches independent of a microprocessor
- Interrupt capability for cascading words or phrases
- Crystal controlled or externally driven oscillator
- Available in complete kit (DT1056) or speech ROMs only (DT1057)

Applications

- Telecommunications
- Appliance
- Automotive
- Teaching aids
- Consumer products
- Clocks
- Language translation
- Annunciators

Typical Applications

Minimum Configuration Using Switch Interface



*Single pole 2 position momentary switch

**4.0 MHz crystal Electro Dynamics Corp. HC18-20 pF

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DT1056/DT1057* Master Word List

Word	8-Bit Binary Address SW8 SW1	Word	8-Bit Binary Address SW8 SW1	Word	8-Bit Binary Address SW8 SW1
ABORT	00000000	FARAD	00101100	PER	01011000
ADD	00000001	FAST	00101101	PICO	01011001
ADJUST	00000010	FASTER	00101110	PLACE	01011010
ALARM	00000011	FIFTH	00101111	PRESS	01011011
ALERT	00000100	FIRE	00110000	PRESSURE	01011100
ALL	00000101	FIRST	00110001	QUARTER	01011101
ASK	00000110	FLOOR	00110010	RANGE	01011110
ASSISTANCE	00000111	FORWARD	00110011	REACH	01011111
ATTENTION	00001000	FROM	00110100	RECEIVE	01100000
BRAKE	00001001	GAS	00110101	RECORD	01100001
BUTTON	00001010	GET	00110110	REPLACE	01100010
BUY	00001011	GOING	00110111	REVERSE	01100011
CALL	00001100	HALF	00111000	ROOM	01100100
CAUTION	00001101	HELLO	00111001	SAFE	01100101
CHANGE	00001110	HELP	00111010	SECURE	01100110
CIRCUIT	00001111	HERTZ	00111011	SELECT	01100111
CLEAR	00010000	HOLD	00111100	SEND	01101000
CLOSE	00010001	INCORRECT	00111101	SERVICE	01101001
COMPLETE	00010010	INCREASE	00111110	SIDE	01101010
CONNECT	00010011	INTRUDER	00111111	SLOW	01101011
CONTINUE	00010100	JUST	01000000	SLOWER	01101100
COPY	00010101	KEY	01000001	SMOKE	01101101
CORRECT	00010110	LEVEL	01000010	SOUTH	01101110
DATE	00010111	LOAD	01000011	STATION	01101111
DAY	00011000	LOCK	01000100	SWITCH	01110000
DECREASE	00011001	MEG	01000101	SYSTEM	01110001
DEPOSIT	00011010	MEGA	01000110	TEST	01110010
DIAL	00011011	MICRO	01000111	TH (NOTE 2)	01110011
DIVIDE	00011100	MORE	01001000	THANK	01110100
DOOR	00011101	MOVE	01001001	THIRD	01110101
EAST	00011110	NANO	01001010	THIS	01110110
ED (NOTE 1)	00011111	NEED	01001011	TOTAL	01110111
ED (NOTE 1)	00100000	NEXT	01001100	TURN	01111000
ED (NOTE 1)	00100001	NO	01001101	USE	01111001
ED (NOTE 1)	00100010	NORMAL	01001110	UTH (NOTE 3)	01111010
EMERGENCY	00100011	NORTH	01001111	WAITING	01111011
END	00100100	NOT	01010000	WARNING	01111100
ENTER	00100101	NOTICE	01010001	WATER	01111101
ENTRY	00100110	OHMS	01010010	WEST	01111110
ER	00100111	ONWARD	01010011	SWITCH	01111111
EVACUATE	00101000	OPEN	01010100	WINDOW	10000000
EXIT	00101001	OPERATOR	01010101	YES	10000001
FAIL	00101010	OR	01010110	ZONE	10000010
FAILURE	00101011	PASS	01010111		

*DT1056 is a complete kit including MM54104 SPC; DT1057 is SSR5 and SSR6 speech ROMs only.

Note 1: "ED" is a suffix that can be used to make any present tense word become a past tense word. The way we say "ED," however, does vary from one word to the next. For that reason, we have offered 4 different "ED" sounds. It is suggested that each "ED" be tested with the desired word for best quality results. Address 31 "ED" or 32 "ED" should be used with words ending in "T" or "D," such as exit or load. Address 34 "ED" should be used with words ending with soft sounds such as ask. Address 33 "ED" should be used with all other words.

Note 2: "TH" is a suffix that can be added to words like six, seven, eight to form adjective words like sixth, seventh, eighth.

Note 3: "UTH" is a suffix that can be added to words like twenty, thirty, forty to form adjective words like thirtieth, fortieth, etc.

Note 4: Address 130 is the last legal address in this particular word list. Exceeding address 130 will produce pieces of unintelligible invalid speech data.

Operational Amplifiers

Features	Input Offset Voltage Max. (mV)	Input Offset Voltage Drift Typ. (μV/°C)	Input Offset Current Max. (nA)	Input Bias Current Max. (nA)	Voltage Gain Min. (Volts/mV)	Bandwidth $A_V = 1$ Typ. (MHz)	Slew Rate $A_V = 1$ Typ. (V/μs)	Output Current (mA)	Supply Voltage Min. (V)	Supply Voltage Max. (V)	Temperature Range −55°C to 125°C	Temperature Range −25°C to 85°C	Temperature Range 0°C to 70°C
Wideband	3.0	4.0	200	2000	15	30	30	±100	±5.0	±20	LH0003	LH0003C	
High Voltage	1.0	4.0	20	100	30	1.0	0.25	±15	±5.0	±45	LH0004		
	1.5	4.0	45	120		1.0	0.25	±15	±5.0	±45		LH0004C	
Wideband	3.0	10	5.0	25	4.0	30(1)	20(1)	±50	±9.0	±20	LH0005A		
	10	20	20	50	2.0	30(1)	20(1)	±50	±9.0	±20	LH0005		
	10	25	25	100	2.0	30(1)	20(1)	±50	±9.0	±20		LH0005C	
High Gain Medium Power	2.5	10	50	250	100	1.0	0.25	±40	±5.0	±22	LH0020		
	6.0	10	200	500	50	1.0	0.25	±40	±5.0	±22		LH0020C	
High Power	3.0	3.0	100	300	100	1.0	3.0	±1000	±5.0	±18	LH0021		
	6.0	5.0	200	500	100	1.0	3.0	±1000	±5.0	±18		LH0021C	
	3.0	3.0	100	300	100	1.0	3.0	±200	±5.0	±18	LH0041		
	6.0	5.0	200	500	100	1.0	3.0	±200	±5.0	±18		LH0041C	
	4.0	5.0	100	300	50	15	70	±500	±5.0	±18	LH0061		
	10	5.0	200	500	25	15	70	±500	±5.0	±18		LH0061C	
	10	10	0.25	1.0	50	5.0	10	±2000	±5.0	±22	LH0101		
	10	10	0.25	1.0	50	5.0	10	±2000	±5.0	±22		LH0101C	
	3.0	5.0	0.075	0.3	50	5.0	10	±2000	±5.0	±22	LH0101A		
	3.0	5.0	0.075	0.3	50	5.0	10	±2000	±5.0	±22		LH0101AC	
General Purpose FET Input	4.0	5.0	0.002	0.01	100	1.0	3.0	±10	±5.0	±22	LH0022		
	6.0	5.0	0.005	0.025	75	1.0	3.0	±10	±5.0	±22		LH0022C	
	20	5.0	0.005	0.025	50	1.0	3.0	±10	±5.0	±22	LH0042		
	20	10	0.01	0.05	25	1.0	3.0	±10	±5.0	±22		LH0042C	
	0.5	2.0	0.0005	0.0025	100	1.0	3.0	±10	±5.0	±22	LH0052		
	1.0	5.0	0.001	0.005	75	1.0	3.0	±10	±5.0	±22		LH0052C	
Wideband High Slew Rate	4.0	20	5000	30000	4.0	50	500	±10	±9.0	±18	LH0024		
	8.0	25	15000	40000	3.0	50	400	±10	±9.0	±18		LH0024C	
Wideband FET Input	5.0	25	0.025	0.1	1.0	70	500	±10	±5.0	±18	LH0032		
	15	25	0.05	0.2	1.0	70	500	±10	±5.0	±18		LH0032C	
Precision FET Input	0.05	0.2	5.0	30	500	0.4	0.06	±1.3	±3.0	±20	LH0044		
	0.1	0.2	5.0	30	500	0.4	0.06	±1.3	±3.0	±20		LH0044C	
	0.025	0.1	2.5	15	1000	0.4	0.06	±1.3	±3.0	±20	LH0044A		
	0.025	0.1	2.5	15	1000	0.4	0.06	±1.3	±3.0	±20		LH0044AC	
	0.05	0.2	5.0	30	500	0.4	0.06	±1.3	±3.0	±20		LH0044B	
Medium Speed FET Input	5.0	5.0	0.002	0.01	50	15	70	±6.0	±5.0	±20	LH0062		
	15	10	0.005	0.065	25	15	70	±6.0	±5.0	±20		LH0062C	
Dual Precision	0.3	1.0	0.010	0.050	250	0.8	0.3	±15	±2.5	±20	LH2011		
	0.6	2.0	0.010	0.100	250	0.8	0.3	±15	±2.5	±20	LH2011B		
	1.0	3.0	0.025	0.180	90	0.8	0.3	±15	±2.5	±20		LH2011C	
	2.0	15	10	75	50	1.0	0.5	±5.0	±3.0	±22	LH2101A		
	2.0	15	10	75	50	1.0	0.5	±5.0	±3.0	±22		LH2201A	
	7.5	30	50	250	25	1.0	0.5	±5.0	±3.0	±22			LH2301A
	0.5	5.0	0.2	2.0	80	1.0	0.3	±1.0	±2.0	±20	LH2108A		
	0.5	5.0	0.2	2.0	80	1.0	0.3	±1.0	±2.0	±20		LH2208A	
	0.5	5.0	1.0	7.0	80	1.0	0.3	±1.0	±2.0	±20			LH2308A
	2.0	15	0.2	2.0	50	1.0	0.3	±1.0	±2.0	±20	LH2108		
	2.0	15	0.2	2.0	50	1.0	0.3	±1.0	±2.0	±20		LH2208	
	7.5	30	1.0	7.0	50	1.0	0.3	±1.0	±2.0	±20			LH2308A
Dual Low Power	3.0	—	5.0	15	100	0.25	0.16	±0.75	±1.0	±18	LH2250	LH2250C	
	6.0	—	10	30	75	0.25	0.16	±0.75	±1.0	±18	LH24250	LH24250C	

Note 1: Specified for $A_V = -10$

Buffer Amplifiers

Features	Voltage Gain (min.)	Output Current	Slew Rate	Input Impedance	Part Number −55°C to 125°C	Part Number −25°C to 85°C
Bipolar input, medium speed	0.95	±100 mA	200 V/μs	180 kΩ	LH0002H	LH0002CH LH0002CN
FET input, high speed	0.97	±100 mA	1000 V/μs	10^{10} Ω	LH0033G	LH0033CG LH0033CJ
FET input, very high speed	0.95	±250 mA	6000 V/μs	10^{10} Ω	LH0063K	LH0063CK
Bipolar input, dual	0.999	±24 mA	30 V/μs	10^{10} Ω	LH2110	LH2210

Instrumentation Amplifiers

All of the amplifiers in this section are true differential input instrumentation amplifiers with very high common mode rejection and adjustable gain.

Features	I_B Max.	V_{IOS} Max.	Characteristics: $\frac{\Delta V_{IOS}}{\Delta T}$	Characteristics: Gain Lin.	Gain Tempco	Gain Error	Part Number: −25°C to 85°C	Part Number: −55°C to 125°C
90μW dissipation, wide supply range, one external gain set resistor	125nA 100nA	2mV 1mV	10μV/°C 10μV/°C	0.03% 0.03%	*	3% max. 1% max.	LH0036C	LH0036
Low cost, one external gain set resistor	500nA	2mV 1mV	10μV/°C 10μV/°C	0.03% 0.03%	* *	1% 0.3%	LH0037C	LH0037
Ultra low drift, all gain set resistors internal, very low noise, very linear, guard drive amplifier included	100nA	150μV 100μV	1μV/°C max. 0.25μV/°C max.	1ppm 1ppm	7ppm/°C 7ppm/°C	0.1% 0.1%	LH0038C	LH0038
Programmable gain fast settling	500pA 500pA	10mV 5mV	10μV/°C 10μV/°C	20ppm 20ppm	1ppm/°C 1ppm/°C	0.3% max. 0.3% max.	LH0084C	LH0084
Digitally programmable gain amplifier	500pA 500pA	10mV 5mV	10μV/°C 10μV/°C	20ppm 20ppm	1ppm/°C 1ppm/°C	0.3% max. 0.2% max.	LH0086C	LH0086

*Dependent upon external resistors.

Sample & Hold Amplifiers

Each of these circuits includes input and output buffer amplifiers and analog switches for a complete sample and hold function.

Features	Accuracy (Max)	Drift Rate (T_A = 25°C)	Acquisition Time	Aperture Time	Part Number: −55°C to 125°C	Part Number: −25°C to 85°C
Low Drift	±0.01% ±0.02%	2mV/s (Note 2)	50μs (Note 2)	150ns	LH0023G	LH0023CG
Medium Speed	±0.1% ±0.3%	25mV/s (Note 1)	10μs (Note 1)	20ns	LH0043G	LH0043CG
High Speed	±0.2% ±0.3%	30mV/s (Note 1)	5μs (Note 1)	25ns	LH0053G	LH0053CG

Note 1: C_S = 1000pF. Note 2: C_S = 0.01μF.

Non-Linear Functions

Function	Characteristics	Transfer Characteristics	Part Number: −55°C to 125°C	Part Number: −25°C to 85°C
True RMS to DC Converter	0.05% accuracy, 100KHz bandwidth, crest factor 5 minimum	$E_{OUT} = \sqrt{\frac{1}{T}\int_0^T E_{IN}^2(t)dt}$	LH0091D	LH0091CD
Multifunction Converter	0.05% accuracy, device multiplies, divides, square roots, raises to fractional powers	$E_{OUT} = V_Y\left(\frac{V_Z}{V_X}\right)^m$	LH0094D	LH0094CD

Precision References and Regulators

Function	Features	Line Reg.	Load Reg.	I_{OUT} (mA)	V_{OUT} Toler. @25°C (Max.)	Drift (Max.)	Part Number: −55°C to 125°C	Part Number: −25°C to 85°C
Positive Programmable Voltage Regulator	Internal programming resistors, adustable current limit V_{OUT} = 5, 6, 8, 10, 12, 15, 18V	0.008%	0.055%	0.1-200	0.5% 1.0%		LH0075	LH0075C
Negative Programmable Voltage Regulator					0.5% 1.0%		LH0076	LH0076C
10.000V Precision BCD Reference	Three-terminal buffered zener reference, 0.1Ω output 12.5 to 40V input, 20μV p−p noise	0.02% 0.02% 0.02%	0.01% 0.02% 0.02%	0-5	0.1% 0.1% 0.05%	20mV* 10mV 4.0mV	LH0070-0 LH0070-1 LH0070-2	
10.024V Precision Binary Reference		0.02% 0.02% 0.02%	0.01% 0.02% 0.02%	0-5	0.1% 0.1% 0.05%	20mV* 10mV 4.0mV	LH0071-0 LH0071-1 LH0071-2	
Switching Regulator 100kHz Rate 10-35V Input	5A output at 75% efficiency V_{OUT} = 3.0 to 30V	0.05%		5A			LH1605	LH1605C

*These specifications apply for −25°C to +85°C.

Note: Refer to the *Linear Databook* for information on other regulators and references.

Analog Switches

Function		Drain-Source "On" Resistance	Drain-Gate Leakage Current	t_{ON}	t_{OFF}	Part Number	
Type	Style					−55°C to 125°C	−25°C to 85°C
PMOS	DPDT	200Ω	200pA	350ns	600ns	AH0014	AH0014C
PMOS	DPDT	200Ω	200pA	100ns	600ns	AH0015	AH0015C
PMOS	Dual DPST	200Ω	200pA	100ns	600ns	AH0019	AH0019C
NJFET	Dual SPDT	10Ω	10nA	1.0μs	2.5μs	AH0140	AH0140C
NJFET	Dual SPDT	15Ω	10nA	1.0μs	2.5μs	AH0153	AH0153C
NJFET	Dual SPDT	30Ω	1nA	0.8μs	1.0μs	AH0129	AH0129C
NJFET	Dual SPDT	50Ω	1nA	0.8μs	1.0μs	AH0153	AH0153C
NJFET	Dual SPDT	80Ω	1nA	0.8μs	1.0μs	AH0126	AH0126C
NJFET	Dual SPDT	10Ω	10nA	1.0μs	2.5μs	AH0141	AH0141C
NJFET	Dual SPST	15Ω	10nA	1.0μs	2.5μs	AH0151	AH0151C
NJFET	Dual SPST	30Ω	1nA	0.8μs	1.0μs	AH0133	AH0133C
NJFET	Dual SPST	50Ω	1nA	0.8μs	1.0μs	AH0152	AH0152C
NJFET	Dual SPST	80Ω	1nA	0.8μs	1.0μs	AH0134	AH0134C
NJFET	DPDT	10Ω	10nA	1.0μs	2.5μs	AH0145	AH0145C
NJFET	DPDT	15Ω	10nA	1.0μs	2.5μs	AH0163	AH0163C
NJFET	DPDT	30Ω	1nA	0.8μs	1.0μs	AH0139	AH0139C
NJFET	DPDT	50Ω	1nA	0.8μs	1.0μs	AH0164	AH0164C
NJFET	DPDT	80Ω	1nA	0.8μs	1.0μs	AH0142	AH0142C
NJFET	SPDT	10Ω	10nA	1.0μs	2.5μs	AH0146	AH0146C
NJFET	SPDT	15Ω	10nA	1.0μs	2.5μs	AH0161	AH0161C
NJFET	SPDT	30Ω	1nA	0.8μs	1.0μs	AH0144	AH0144C
NJFET	SPDT	50Ω	1nA	0.8μs	1.0μs	AH0162	AH0162C
NJFET	SPDT	80Ω	1nA	0.8μs	1.0μs	AH0143	AH0143C
NJFET	Dual SPST	100Ω	1nA	1.5μs	0.75μs	AH2114	AH2114C

Digital Drivers

These devices accept TTL or DTL input and provide extended output capability for actuators and displays

Typical Application Function	I_{OUT}	V_{SAT}	LV_{CEO}	t_{ON}	t_{OFF}	Part Number	
						−55°C to 125°C	−25°C to 85°C
Motor, Relay, Current Sourcing	1.6A	1.5V	45V	0.40μs	7.0μs	DH0006H	DH0006CH DH0006CN
Lamps, Relay, Current Sourcing	0.25A	0.4V	40V	0.16μs	0.22μs	DH0008H	DH0008CH DH0008CN
Lamp Driver, Current Sinking	0.4A	1.0V	40V	0.26μs	2.2μs	DH0011H	DH0011CH DH0011CN
Lamp Driver, Current Sinking	0.5A	0.6V	50V	0.16μs	0.22μs	DH0011AH	
Relay, Display, Current Sinking	0.25A	0.6V	70V	50ns	500ns		DH0016CN
Display, Current Sinking	0.50A	0.6V	50V	50ns	1.5μs		DH0017CN
Display, Current Sinking	0.05A	0.6V	100V	50ns	1.5μs		DH0018CN
Hammer Driver	5.0A	2.0V	45V	0.4μs	7.0μs	DH0028H	DH0028CH DH0028CN
Level Translator	100mA	0.5V	−25V	25ns	75ns	DH0034D DH0034H	DH0034CD DH0034CH
Pin Diode	±0.5A	1.0V	30V	10ns	30ns	DH0035G	DH0035CG
Electrostatic Print-head Driver,	20mA		425	12μs	1.8μs		DH0069CJ

Analog-to-Digital Converters

Resolution (Bits)	Supplies (V)	Maximum Non-Linearity	Conversion Time	Part Number	
				−55°C to +125°C	−25°C to +85°C
12	+5 to ±15	±½LSB	100μs	ADC1210	ADC1210C
12	+5 to ±15	±2LSB	100μs	ADC1211	ADC1211C
12	+5, ±12, ±15	±½LSB	20μs	—	ADC1280
12	+5, ±15	±2LSB	21μs	—	ADC1080

Digital-to-Analog Converters

Resolution (Bits)	NSC Part No.	Alternate Source Part No.	Non-Linearity @ 25°C (Max.) (%)	Internal Reference	Output Op Amp	Supplies (V)	Temp. Ranges Available (°C)	Comments
12	DAC1200	—	±0.0122	•	•	+5, ±15	−25 to +85, −55 to +125	
12	DAC1201	—	±0.0488	•	•	+5, ±15		
12	DAC1242	—	±0.0244	•	•	+5, +12		4-20mA Current Sink
12	DAC1243	—	±0.0244	•	•	+5, +12		4-20mA Current Source
12	DAC1280	—	±0.0244	•	•	+5, ±15	0 to 70	
12	DAC1280A	DAC80-CBI-V	±0.0122	•	•	±12 to ±15	0 to 70	
12	DAC1285	DAC85-CBI-V	±0.0122	•	•	+5, ±15	−25 to +85, −55 to +125	
12	DAC1285A	DAC85LD-CBI-V, DAC87-CBI-V	±0.0122	•	•	±12 to ±15	−25 to +85 −55 to +125	

Fiber-Optic Product

Function	Features				−55°C to +125°C	−25°C to +85°C
	Bandwidth	Drive Current	Coupled Power	λ		
Complete Transmitter with LED	DC to 20 Mbits	100mA (max.)	65μW	820nm		FOT180B
Monolithic Self Contained Emitter	DC to 10 Mbits	140 mA (peak)	30μW	820nm		FOE380B-1
			65μW			FOE380B-2

Function	Features			−55°C to +125°C	−25°C to +85°C
	Bandwidth	Sensitivity	Coupled Power Required for Max. Bit Rate		
Receiver	5 Mbits	−55 dBm		LH0082D	LH0082CD
Complete Receiver with Photodiode	5 Mbits	−45 dBm	2μW		FOR100B
Monolithic Receiver with Integral Photodiode	DC to 10 Mbits	−18 dBm	15μW		FOR261F-1
			20μW		FOR261F-2
Monolithic Self Contained Receiver	DC to 10 Mbits	−18 dBm	15μW		FOR36 B-1
			20μW		FOR361B-2

Active Filters (Building Blocks)

Function	Features	Frequency Accuracy	Q Accuracy	Q × F_C	Part Number −55°C to 125°C	Part Number −25°C to 85°
Universal Active Filter	State Variable Building Block	±2.5%	±7.5%	50k	AF100-1	AF100-1C
		±1.0%	±7.5%	50k	AF100-2	AF100-2C
Universal Active Filter	State Variable Building Block Wide Bandwidth	±2.5%	±7.5%	200k		AF150-1C
		±1.0%	±7.5%	200k		AF150-2C
Dual Universal Active Filter	State Variable Building Block Two AF100 in one package	±2.5%	±7.5%	50k		AF151-1C
		±1.0%	±7.5%	50k		AF151-2C
Universal Wideband	FET-Input Amplifier Pin Compatible with AF100J	±2.5%	±7.5%	200k	AF160-1	AF160-1C
		±1.0%	±7.5%	200k	AF160-2	AF160-2C
Dual Universal Wideband	FET-Input Amplifier Pin Compatible with AF151J	±2.5%	±7.5%	200k		AF161-1C
		±1.0%	±7.5%	200k		AF161-2C
		Resistor Accuracy	Resistor Match	Resistor Tempco (ppm/°C)		
General Impedance Converter (GIC)	Matched Resistors 7.5k and Controlled TC	1.0%	±0.2%/ 0.1%	±110 ±30	AF120H	
		2.0%	±0.4%/ 0.2%	±110 ±60		AF120CH

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BIPOLAR OPERATIONAL AMPLIFIERS
FET OPERATIONAL AMPLIFIERS
VOLTAGE FOLLOWER/CURRENT BOOSTER
LOW NOISE PRE-AMPLIFIER
ANALOG COMPARATOR
ABSOLUTE VALUE
LOGARITHMIC AMPLIFIERS
PHASE DETECTORS
V–F
SAMPLE AND HOLD

BIPOLAR Operational Amplifier

MODEL	SLEW RATE	WIDE BAND WIDTH RANGE	FAST SETTLING	HIGH VOLT	OPEN LOOP GAIN AT DC dB typ.	SLEW RATE V/μsec min.	SETTLING TIME @0.1% nsec max.	GAIN BANDWIDTH PRODUCT @G = 100 MHz min.	MAX. OUTPUT FREQ. MHz min.	OUTPUT VOLTAGE V min.	OUTPUT CURRENT mA min.	NOISE SPECTRAL DENSITY VOLTAGE nV/√Hz max.	NOISE SPECTRAL DENSITY CURRENT pA/√Hz max.	VOLTAGE OFFSET mV max.	OFFSET DRIFT μV/°C max.	BIAS CURRENT μA max.	POWER SUPPLY V nom.	SUPPLY CURRENT mA max.	WORKING TEMPERATURE °C	M T B F x1000 hours	CASE STYLE
9406		●			60	± 300	105	1,000	5	±10	± 3	25	3	± 10	± 125	±10	±15	±20	−55~+ 85	664	MODULE
9412				●	54	± 200	50	300	3	±10	±200	35	10	± 7.5	± 150	±30	±15	±35	−55~+ 75	566	MODULE
9491A	●	●	●		63	±1,000	12	1,000	30	± 5	± 3	20	50	± 20	± 50	±50	±15	±12	−55~+ 85	352	MODULE
9697				●	80	± 100	500	100	0.3	±50	± 20	45	20	± 20	± 400	±5	± 60	±14	−25~+ 75	412	MODULE
9804					52	± 250	60	500	4	±10	±200	50	10	± 5	± 100	±20	±15	±33	−55~+ 75	275	MODULE
9808	●				126	±1,800	50	200	28	±10	±100	50	1	± 1	± 2	±0.1	±15	±30	−55~+ 85	171	MODULE
9826	●	●	●		64	±1,000	12	1,000	30	± 5	± 50	20	10	± 20	± 50	±50	±15	±18	−55~+ 85	180	MODULE
9906					60	± 250	150	300	4	±10	± 4.5	30	5	± 10	± 150	±10	±15	±20	−65~+125	1,015	DIP
9909	●	●			70	±2,500	200	1,000	40	±10	± 50	30	10	± 30	±1,000	±50	±15	±60	−55~+ 85	316	DIP
9912					63	± 600	150	800	10	±10	± 20	30	40	± 25	±1,000	±40	±15	±30	−65~+125	485	DIP
9914	●	●			75	±1,000	100	3,000	15	±10	± 50	10	10	± 30	± 100	±50	±15	±40	−55~+ 85	316	DIP
9916					63	± 300	50	200	10	± 5	± 5	20	50	± 30	± 150	±30	±15	±15	−65~+125	390	DIP
9918		●	●			± 300	40	1000	10	± 5	± 50	20	10	± 20	30	±50	±15	±30	−55 to 85°C	270	DIP

FET Operational Amplifier

MODEL	SLEW RATE	WIDE BAND WIDTH RANGE	SETTLING TIME	HIGH OUTPUT	OPEN LOOP GAIN AT DC dB typ.	SLEW RATE V/μsec min.	SETTLING TIME nsec max.	GAIN BAND-WIDTH PRODUCT MHz min.	MAX. OUTPUT FREQ. MHz min.	OUTPUT VOLTAGE V min.	OUTPUT CURRENT mA min.	NOISE SPECTRAL DENSITY VOLTAGE nV/√Hz max.	NOISE SPECTRAL DENSITY CURRENT fA/√Hz max.	VOLTAGE OFFSET mV max.	OFFSET DRIFT μV/°C max.	BIAS CURRENT PA max.	POWER SUPPLY V nom.	SUPPLY CURRENT mA max.	WORKING TEMPERATURE °C	M T B F x1000 hours	CASE STYLE
9725			●		50	± 300	60	400	5	±10	±200	45	100	± 20	± 150	− 30	±15	±35	−55~+ 75	288	MODULE
9740	●	●			120	±3,000	100	300	50	±10	± 50	50	50	± 10	± 20	− 30	±15	±33	−55~+ 85	109	MODULE
9908	●				60	± 200	300	100	3	±10	$^{+20}_{-5}$	10	50		±3,000	− 300	±15	±12	−65~+125	409	DIP
AH0605	●	●		●	86	± 200	300	400	3	±10	± 30	20	—	± 5	± 50	− 100	± 15	±19	0 ~ +70	—	DIP
9932			●		52	± 600	100	150	10	±10	± 10	20	200		± 500	− 300	±15	±30	−65~+ 85	314	DIP

Voltage Follower/Current Booster

MODEL	GAIN typ.	SLEW RATE V/μsec min.	SETTLING TIME @0.1% nsec max.	MIN. FREQUENCY BAND MHz min.	MAX. OUTPUT FREQUENCY MHz max.	OUTPUT VOLTAGE V min.	OUTPUT CURRENT mA min.	VOLTAGE OFFSET mV max.	OFFSET DRIFT μV/°C max.	BIAS CURRENT max.	POWER SUPPLY V nom. nom.	SUPPLY CURRENT mA max. max.	WORKING TEMPERATURE °C	M T B F x1000 hours	CASE STYLE
9910	0.97	±2,000	80	60	30	±10	±100	±20	±100	± 20μA	±15	± 5	−65~+125	858	DIP
9911	0.97	±1,000	50	200	15	±10	±500	±20	±100	± 5mA	±15	±35	−65~+125	397	DIP
9963	0.96	±3,000	50	200	50	±10	±200	±50	±400	±100pA	±15	±35	−55~+125	370	DIP

Low Noise Pre-Amplifier

MODEL	GAIN max.	SLEW RATE V/μsec min.	GAIN BANDWIDTH PRODUCT MHz min.	MAX. OUTPUT FREQUENCY MHz min.	OUTPUT VOLTAGE Vp-p max.	OUTPUT CURRENT mA min.	NOISE SPECTRAL DENSITY VOLTAGE nV/√Hz max.	NOISE SPECTRAL DENSITY CURRENT fA/√Hz max.	BIAS CURRENT pA max.	POWER SUPPLY V nom.	SUPPLY CURRENT mA max.	WORKING TEMPERATURE °C	M T B F x1000 hours	CASE STYLE
AH0013	60	±400	100	20	3	±5	1.5 TYP	10	+50	+15	+10	−65 + 125	692	DIP

Analog Comparator

MODEL	GAIN dB min.	NOISE SPECTRAL DENSITY VOLTAGE max.	NOISE SPECTRAL DENSITY CURRENT max.	VOLTAGE OFFSET mV max.	DRIFT μV/°C max.	BIAS CURRENT μA max.	MAX CURRENT mA	MAX SINK CURRENT mA	SLEW RATE V/μsec min.	RESPONSE TIME @1V nsec max.	WORKING TEMPERATURE °C	POWER SUPPLY V	SUPPLY CURRENT mA max.	M T B F x1000 hours	CASE STYLE
9050	60	20	10	±20	±100	50	+4	−10	±1,000	5	−55~+ 85	±15	±12	322	MODULE
9915	40	20	10	±30	±300	50	+3	−10	±1,000	15	−55~+125	+ 5	+20	1,015	DIP

Absolute Value

MODEL	GAIN mA/V	DYNAMIC RANGE	DRIFT +V/°C max.	BIAS CURRENT μA max.	MIN INPUT VOLTAGE V f. s.	OUTPUT CURRENT mA f. s.	MAX OUTPUT VOLTAGE V min.	FREQ. RANGE MHz min.	SLEW RATE mA/μsec min.	POWER SUPPLY V	SUPPLY CURRENT mA max.	WORKING TEMP. °C	M T B F x1000 hours	CASE STYLE
9014	0.4	40dB	200	25	±10	4	+10	30	± 20	±15	±8	−55~+100	302	MODULE
9934	1.0	40dB	800	25	±10	10	±10	10	±20	±15	±1	−55~+100	450	DIP

Bipolar Log Amplifier

MODEL	DYNAMIC RANGE dB min.	MAX LOG ERROR % max.	INPUT DYNAMIC RANGE	VOLTAGE OFFSET mV max.	DRIFT μV/°C max.	BIAS CURRENT μA max.	BIAS DRIFT nA/°C max.	VARIABLE CONSTANT V/dec typ.	POLARITY	FREQ. CHARACTER MHz min.	WORKING TEMP. °C	POWER SUPPLY V	SUPPLY CURRENT mA max.	M T B F x1000 hours
2531A	70	± 3	±3mV~±10V	± 1	±300	±5	±100	2	non;inv	10	−25~+ 75	±15	± 65	176MODULE
2540	60,100	± 3	±10mV~±10V	± 0.03	—	−30	—	1.5	inv/n.inv	10	−55~+ 75	±15	±135	87MODULE
2910	80	± 3	± 1mV~± 10V	ADJ	±100	±20	±500	0.075	inv	10	−65~+125	±15	± 12	423MODULE

Phase Detector

MODEL	ACCURACY	INPUT VOLTAGE RANGE	INPUT VOLTAGE OFFSET mV max.	OUTPUT VOLTAGE V f. s.	VOLTS/ DEGREE	MAX. FREQ. MHz min.	OUTPUT TIME CONSTANT mS nom.	WORKING TEMP. °C	POWER SUPPLY V	SUPPLY CURRENT mA max.	M T B F x1000 hours	CASE STYLE
3420	± 0.1°	± 10mV~ ± 10V	± 10	+ 9.00	.1/θ	3.0	16	−55~+100	± 15	± 18	300	MODULE
3421	± 3.0°	± 2 V~ ± 10V	± 10	+ 9.00	.1/θ	10.0	5.0	−55~+ 85	± 15	+150 −80	134	MODULE

$E_o = \frac{\theta}{10}$ (V)

Coordinate Converter (Polar-to-Cartesian)

MODEL	ACCURACY % max.	ACCURACY MULTIPLE % max.	INPUT ANGLE V	INPUT VOLTAGE V	OUTPUT VOLTAGE V min.	OUTPUT CURRENT mA min.	TRG FUNCTION kHz min.	SMALL SIGNAL BAND-WIDTH MHz min.	SLEW RATE V/μsec min.	WORKING TEMP. °C	POWER SUPPLY V	SUPPLY CURRENT mA max.	M T B F x1000 hours	CASE STYLE
5090A	± 3	± 0.5	−10~ + 10	0~ + 10	± 10	± 10	300	1	± 30	−55~ + 85	± 15	± 60	117	MODULE

Voltage-to-Frequency Converter

MODEL	NON-LINEARITY % max.	INPUT VOLTAGE RANGE V	INPUT DYNAMIC RANGE decade min.	OUTPUT FREQ. RANGE MHz	MAX SINK CURRENT mA	RESPONSE TIME cycle max.	FM FREQ. BAND kHz	TEMP. CO-EFFICIENT %/°C	WORKING TEMP. °C	POWER SUPPLY V	SUPPLY CURRENT mA max.	M T B F x1000 hours	CASE STYLE
3930	± 3.0	0~ + 10	1.5	0~1	15	1	0~100	± 0.2	−55~ + 125	± 15	+ 25 − 8	739	DIP

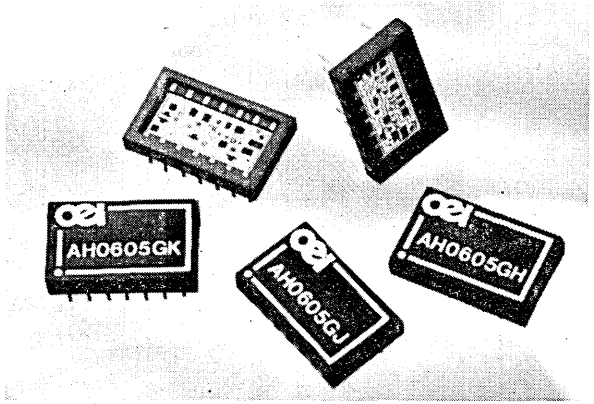
Sample & Hold Analog Memory

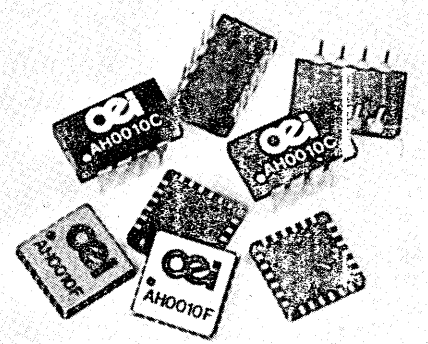
MODEL	NON-LINEARITY % max.	INPUT VOLTAGE V min.	APERTURE TIME nsec max.	AQUIS. TIME nsec	MEMORY LEAKAGE CURRENT nA max.	TRACKING MODE FREQ. MHz	WORKING TEMP. °C	POWER SUPPLY V	SUPPLY CURRENT mA max.	MTBF x1000 hours	CASE STYLE
5021	2%	± 10	3	1,000	1	0~10	−55~ + 85	± 15	± 30	133	MODULE
5025	2%	± 10	3	30	100	0~10	−55~ + 85	± 15	± 90	133	MODULE

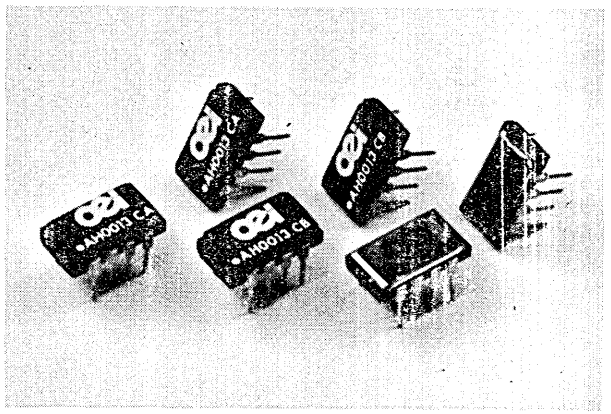
Peak Sense & Hold Analog Memory

MODEL	SENSE ACCURACY	GAIN ACCURACY % max.	INPUT VOLT V min.	DECADE RATE V/msec max.	ACQUISITION TIME nsec max.	GATE TURN ON TIME nsec max.	GATE TURN OFF TIME nsec max.	WORKING TEMP. °C	POWER SUPPLY V	SUPPLY CURRENT mA max.	MTBF x1000 hours	CASE STYLE
5030A	± 1%or20mV	± 0 1	+10	1	30	1000	500	−55~+ 85	± 15	± 8	376	MODULE
5032A	± 2%or20mV	± 0 2	+10	10	20	30	30	−55~+ 85	± 15	± 15	281	MODULE
5902	± 1mV	1± 0.03	+10	100	100	50	500	−65~+125	± 15	± 9	467	DIP
5905	±50mV	1± 0.03	+5	150	20	50	500	−65~+125	±15	± 9	467	DIP

oei
P.O. Box 11140·Tucson, Az. 85734
TWX-910-952·1283







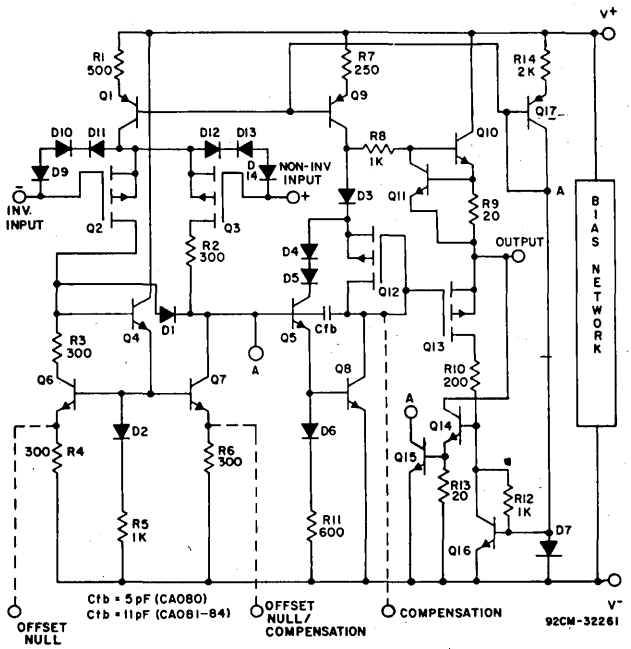
Optical Electronics

LINEAR

BiMOS Operational Amplifiers

CA080 CA081 CA082 CA083 CA084 Series

BiMOS Replacements for Industry TL080 Series BIFET Types



Schematic diagram of the CA080, CA081, CA082, CA083, and CA084

The CA080 series of operational amplifiers are more than just BiMOS versions of the industry BIFET TL080 series. The CA080 series offer lower input bias and offset currents, higher input impedances, and wider bandwidth than their BIFET counterparts and other pin-compatible op amps.

Features:

- Very low input bias current (50 pA max) and offset current (30 pA max.)
- Input impedance typically $10^{12}\Omega$
- Low input offset voltage (2mV typ.)
- Wide common-mode input voltage range
- Low power consumption: 42mW (single amp. channel)
- High slew rate: 13v/us typ.
- Unity-gain bandwidth = 5 MHz (typ.)
- Wide output voltage swing: 25 volts
- Low distortion
- Short-circuit protection
- Noise voltage (1 kHz): 40 nV/$\sqrt{Hz}$
- Direct replacement for industry type TL080 series in most applications

Applications:

- Inverters
- High-Q notch filters
- IC preamplifiers
- Unity-gain absolute value amplifiers
- Sample and hold amplifiers
- Active filters
- Low-current amplification circuits
- Data acquisition equipment
- AC voltmeters (front end)

Type Series	No. of Amplifiers	Frequency Compensation	Offset Control
CA080	Single	External	External
CA081	Single	Internal	External
CA082	Dual	Internal	—
CA083	Dual	Internal	External
CA084	Quad	Internal	—

Characteristics T_A = 25°C	CA080 CA081 CA082 CA083 CA084	CA080A CA081A CA082A CA083A CA084A	CA080B CA081B CA082B CA083B CA084B	CA080 CA081 CA082	CA080A CA081A CA082A	Units
T_A Range	0-70	0-70	0-70	−55 to 125 °C		
V_{IO} (max.)	15	6	3	6	3V	V
I_I (max.)	50	40	30	40	40	pA
I_{IO} (max.)	30	20	10	20	20	pA
I^+ (max.)	2.8*	2.8*	2.8*	2.8*	2.8*	mA
V_{ICR} (min.)	±10	±12	±12	±12	±12	V
A_{OL} (min.)	25K	50K	50K	50K	50K	V/V
f_T (typ.)	5	5	5	5	5	MHz
SR (typ.)	13	13	13	13	13	V/μs

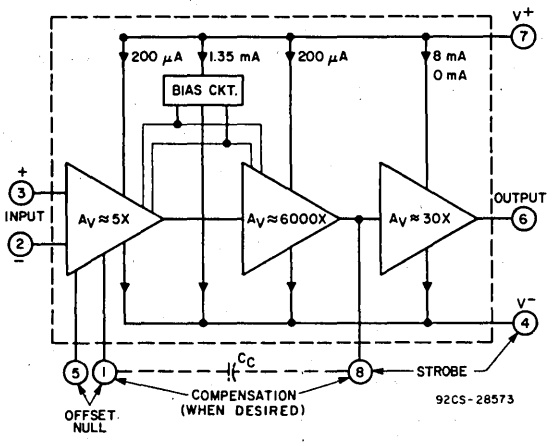
*Per ampl CA3082, CA3083, CA3084

Package Selection Chart

Type No.	Package Type & Suffix					CHIP
	8L TO-5	8L TO-5	DIL-CAN	Mini-DIP	14L DIP	
	−55 to + 25°C	0 to + 70°C		0 to + 70°C		
CA080	T	—	S	E	—	H
CA080A	T	—	S	E	—	—
CA080B	—	—	—	E	—	—
CA080C	—	T	—	—	—	—
CA081	T	—	S	E	—	H
CA081A	T	—	S	E	—	—
CA081B	—	—	—	E	—	—
CA081C	—	T	—	—	—	—
CA082	T	—	S	E	—	H
CA082A	T	—	S	E	—	—
CA082B	—	—	—	E	—	—
CA082C	—	T	—	—	—	—
CA083	—	—	—	—	E	H
CA083A	—	—	—	—	E	—
CA083B	—	—	—	—	E	—
CA084	—	—	—	—	E	H
CA084A	—	—	—	—	E	—
CA084B	—	—	—	—	E	—

BiMOS Operational Amplifiers

CA3130, CA3130A, CA3130B | MOS/FET Input, CMOS Output
CA3160, CA3160A, CA3160B | Frequency Compensated Version of CA3130
CA3260, CA3260A, CA3260B | Dual Version of CA3160



Type No.	Package	Operating Temp. Range
CA3130S, AS, BS CA3160S, AS, BS CA3260S, AS, BS	8-Lead DIL-CAN	
CA3130T, AT, BT CA3160T, AT, BT CA3260T, AT, BT	8-Lead TO-5	
CA3130E, AE CA3160E, AE CA3260E, AE	8-Lead Mini-DIP	−55 to +125° C
CA3130H CA3160H CA3260H	Chip	

Gate-protected p-channel MOS/FET (PMOS) transistors in the input circuit provide very-high-input impedance, very-low-input current, exceptional speed performance, and common-mode input-voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute in single-supply applications.

Features:

- MOS/FET input stage provides:
  very high Z_I = 1.5 TΩ (1.5 x 10^{12}Ω) typ.
  very low I_I = 5 pA typ. at 15-V operation
  = 2 pA typ. at 5-V operation
- Common-mode input-voltage range includes negative supply rail; input terminals can be swung 0.5 V below negative supply rail
- COS/MOS output stage permits signal swing to either (or both) supply rails
- Wide BW: 15 MHz typ. (unity-gain bandwidth) - CA3130
  4 MHz typ. (unity-gain bandwidth) - CA3160, CA3260
- High SR: 10 V/μs typ. (unity-gain follower)
- High output current (I_O): 20 mA typ.
- High A_{OL}: 320,000 (110 dB) typ.
- Compensation with single external capacitor - CA3130
- Internal phase compensation for unity gain (With terminal access for supplementary external phase compensation network if desired) - CA3160
- Low V_{IO}: 2 mV max. (CA3160, CA3260)

Applications:

- Ground-referenced single-supply amplifiers
- Fast sample-hold amplifiers
- Long-duration timers/monostables
- High-input-impedance comparators
- High-input-impedance wideband amplifiers
- Voltage followers
- Voltage regulators
- Peak detectors - CA3130
- Single-supply full-wave precision rectifiers - CA3130
- Photo-diode sensor amplifiers
- Wien-Bridge oscillators
- Voltage-controlled oscillators
- Ideal interface with digital COS/MOS

A complementary-symmetry MOS (COS/MOS) transistor-pair, capable of swinging the output voltage to within 10 millivolts of either supply-voltage terminal (at very high values of load impedance), is employed as the output circuit.

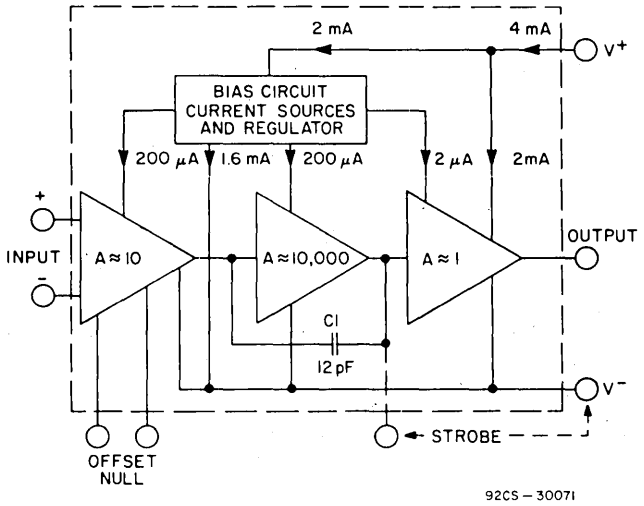
Electrical Characteristics: T_A = 25°C, V^+ = 7.5V, V^- = − 7.5V

Type	R_I (Typ) TΩ	I_I (Max) pA	I_{IO} (Max) pA	V_{IO} (Max) mV	SR (Typ) V/μs	f_T (Typ) MHz	Output Swing (Typ)-V	Compensation	A_{OL} (min.) V/V	A_{OL} (min.) dB	Supply Voltage Range V
CA3130	1.5	50	30	15	10	4	−0.002 to + 13	External	50K	94	4.5 to 16
CA3130A	1.5	30	20	5	10	4	−0.002 to + 13	External	50K	94	4.5 to 16
CA3130B	1.5	20	10	2	10	4	−0.002 to + 13	External	100K	100	4.5 to 16
CA3160	1.5	50	30	15	10	4	−0.002 to + 13	Internal	50K	94	4.5 to 16
CA3160A	1.5	30	20	5	10	4	−0.002 to + 13	Internal	50K	94	4.5 to 16
CA3160B	1.5	20	10	2	10	4	−0.002 to + 13	Internal	100K	100	4.5 to 16
CA3260*	1.5	50	30	15	10	4	−0.002 to + 13	Internal	50K	94	4 to 16
CA3260A*	1.5	30	20	5	10	4	−0.002 to + 13	Internal	50K	94	4 to 16
CA3260B*	1.5	20	10	2	10	4	−0.002 to + 13	Internal	100K	100	4 to 16

*Characteristics are for each amplifier.

BiMOS Operational Amplifiers

CA3140, CA3140A, CA3140B | MOS/FET Input, Bipolar Output
CA3240, CA3240A | Dual Version of CA3140



Type No.	Package	Operating Temp. Range
CA3140S, AS, BS	8-Lead DIL-CAN	−55 to + 125° C
CA3140T, AT, BT	8-Lead TO-5	−55 to + 125° C
CA3140E, AE	8-Lead Mini-DIP	−55 to + 125° C
CA3240E, AE		−40 to + 85° C
CA3240E1, AE1	14-Lead DIP	−40 to + 85°C
CA3140H	Chip	−55 to + 125° C
CA3240H		−40 to + 85° C

The CA3140 and CA3240 Series of BiMOS op amps give you the big advantage of MOS/FET input . . . **plus** bipolar speed and high supply voltage operating capability: 4 to 44V, dual or single supply. Wide common-mode input voltage range - can be swung 0.5 V below negative rail. Output swing complements input common-mode range, permitting full utilization of low supply voltages (down to 4V). And PMOS input devices are protected by rugged bipolar diodes.

Features:

- MOS/FET Input Stage
  - (a) Very high input impedance (Z_{IN}) - 1.5 T Ω typ.
  - (b) Very low input current (I_I) - 10 pA typ. at ± 15V
  - (c) Low input-offset voltage (V_{IO}) - to 2 mV max.
  - (d) Wide common-mode input-voltage range (V_{ICR}) - can be swung 0.5 volt below negative supply-voltage rail
  - (e) Output swing complements input common-mode range
- Rugged input stage - bipolar diode protected
- Directly replaces industry type 741 (CA3140) or 747 (CA3240) in most applications
- Includes numerous industry operational amplifier categories such as general-purpose, FET input, wideband (high slew rate)
- Operation from 4-to-44 volts
- Single or Dual supplies
- Internally compensated
- Characterized for ± 15-volt operation and for TTL supply systems with operation down to 4 volts
- Wide bandwidth - 4.5 MHz unity gain at ± 15V or 30V; 3.7 MHz at 5V
- High voltage-follower slew rate - 9 V/μs
- Fast settling time - 1.4μs typ. to 10 mV with a 10-V_{p-p} signal
- Output swings to within 0.2 volt of negative supply
- Strobable output stage

Applications

- Ground-referenced single-supply amplifiers in automobile and portable instrumentation
- Sample-and-hold amplifiers
- Long-duration timers/multivibrators (microseconds-minutes-hours)
- Photocurrent instrumentation
- Peak detectors
- Active filters
- Comparators
- Interface in 5-V TTL systems & other low-supply voltage systems
- All standard operational amplifier applications
- Function generators
- Tone controls
- Power supplies
- Portable instruments
- Intrusion alarm systems

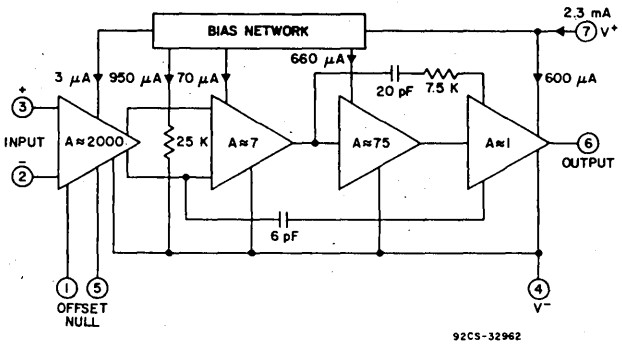
Electrical Characteristics: T_A = 25°C, V^+ = 15V, V^- = −15V

Type	R_I (Typ) TΩ	I_I (Max) pA	I_{IO} (Max) pA	V_{IO} (Max) mV	SR (Typ) V/μs	f_T (Typ) MHz	Output Swing (Typ)-V	Compensation	A_{OL} (min.) V/V	A_{OL} (min.) dB	Supply Voltage Range V
CA3140	1.5	50	30	15	9	4.5	−14 to + 13	Internal	20K	86	4 to 36
CA3140A	1.5	40	20	5	9	4.5	−14 to + 13	Internal	20K	86	4 to 36
CA3140B	1.5	30	10	2	9	4.5	−14 to + 13	Internal	50K	94	4 to 44
CA3240	1.5	50	30	15	9	4.5	−14 to + 13	Internal	20	86	4 to 36
CA3240A	1.5	40	20	5	9	4.5	−14 to + 13	Internal	20	86	4 to 36

BiMOS Operational Amplifiers

CA3193, CA3193A, CA3193B
CA3493, CA3493A, CA3493B

Ultra-Stable
Precision, Instrumentation-Grade Types



Package Type & Suffix Letter Type No.	T_A Range °C
CA3193/3493H CA3193S/3493S CA3193/3493S CA3193BS/3493BS	−55 to +125 0 to +70 −25 to +85 −55 to +125
CA3193T/3493T CA3193AT/3493AT CA3193BT/3493BT	0 to +70 −25 to +85 −55 to +125
CA3193E/3493E CA3193AE/3493AE CA3193BE/3493AE	0 to +70 −25 to +85 −55 to +125

E = Mini DIP T = 8-Lead TO-5
S = DIL-CAN H = CHIP

Features:

- Low V_{10}: 75μV max. (CA3193B, CA3493B)
  200μV max. (CA3193A, CA3493A)
  500μV max. (CA3193, CA3493)
- Low Δ V_{10}/ ΔT: 2μV/°C max. (CA3193B, CA3493B)
  3μV/°C max. (CA3193A, CA3493A)
  5μV/°C max. (CA3193, CA3493)
- Low I_{10} and I_{1B}
- Low Δ I_{10}/ ΔT: 50 pA/°C max. (CA3193B, CA3493B)
  150 pA/°C max. (CA3193, CA3493)
- Low $\Delta I_1/\Delta T$: 0.5 nA/°C max. (CA3193B, CA3493B)
  3.7 nA/°C max. (CA3193, CA3493)
- Extremely high gain: 120 dB min. (CA3193B, CA3493B)
- Low V_{10} vs. time
- High CMRR and PSRR
- Internally compensated: 1.2-MHz f_T
- Low input noise voltage: 0.36μV p-p typ.
- Functional replacements for op-amp types 725, 108A, OP-5, OP-7, LM-11, LM714

Applications:

- Thermocouple preamplifiers
- Strain-gauge bridge amplifiers
- Summing amplifiers
- Differential amplifiers
- Bilateral current sources
- Log amplifiers
- Differential voltmeters
- Precision voltage references
- Active filters
- Buffers
- Integrators
- Sample-and-hold circuits
- Low frequency filters

CA3193- and CA3493-series op amps are ultra-stable, precision, instrumentation operational amplifiers that employ both PMOS and bipolar transistors on a single monolithic chip. The SE amplifiers are internally phase-compensated and provide a gain-bandwidth product of 1.2 MHz.

They are pin-compatible with the industry 741 series and many other IC op amps, and may be used as replacements for 741-series types in most applications.

Because of their low offset voltage and low offset voltage-versus-temperature coefficient, the CA3193- and CA3493-series amplifiers have a wider range of applications than most op amps and are particularly well suited for use in the applications listed above.

Electrical Characteristics: T_A = 25°C, V^+ +15V, V^- = −15V

Type	Max V_{10} at Max. T(μV)	I_{1B} (Max.) nA	I_{10} (Max.) nA	CMRR (Min.) db	PSRR (Min.) db	SR (Typ) V/μs	f_T (Typ) MHz	Supply Voltage Range V
CA3193, CA3493	725	40	10	100	100	0.25	1.2	± 3.5 to ± 18
CA3193A, CA3493A	380	20	5	110	100	0.25	1.2	± 3.5 to ± 18
CA3193B, CA3493B	275	15	3	120	110	0.25	1.2	± 3.5 to ± 22

CA3420B, CA3420A, CA3420 Preliminary Data

Low-Supply Voltage, Low-Input Current BiMOS OP-AMPS

The RCA-CA3420B, CA3420A, and CA3420 are integrated-circuit operational amplifiers that combine PMOS transistors and BiPolar transistors on a single monolithic chip. The CA3420B, CA3420A, and CA3420 BIMOS operational amplifiers feature gate-protected PMOS transistors in the input circuit to provide very high input impedance, very low input currents (less than 1 pA). The internal bootstrapping network features a unique guard-banding technique for reducing the doubling of leakage current for every 10° C increase in temperature. The CA3420 series operates at total supply voltages from 2 to 20 volts either single or dual supply. These operational amplifiers are internally phase compensated to achieve stable operation in the unity gain follower configuration. Additionally, they have access terminals for a supplementary external capacitor if additional frequency roll-off is desired. Terminals are also provided for use in applications requiring input offset voltage nulling. The use of PMOS in the input stage results in common-mode input voltage capability down to 0.45 volt below the negative supply terminal, an important attribute for single-supply application. The output stage uses a feedback OTA type amplifier that can swing essentially from rail-to-rail. The output driving current of 1.5 mA MIN is provided by using non-linear current mirrors.

The CA3420-series has the same 8-lead pin-out used for the industry standard 741. They are supplied in the standard 8-lead TO-5 style package (S suffix, and T suffix); in the standard 8-lead dual-in-line plastic package (Minidip - E suffix), and are also available in chip form (H suffix).

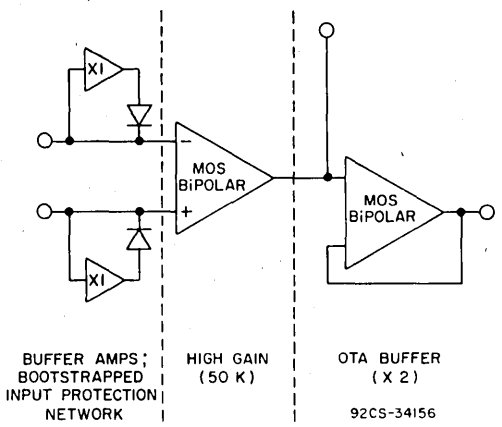


Fig. 1 - Functional diagram for CA3420.

Features:

- *2 V Supply at 300 μA Supply Current*
- *1 pA (typ) Input Current (Essentially Constant to 85° C)*
- *Rail-to-Rail Output Swing (Drive ±2 mA into 1 KΩ Load)*
- *Pin Compatible with 741 Op-Amp*
- *Low Cost 8-Lead Minidip, TO-5*

Applications:

- *pH Probe Amplifiers*
- *Picoammeters*
- *Electrometer (High Z) instruments*
- *Portable Equipment*
- *Inaccessible Field Equipment*
- *Battery Dependent Equipment (Medical and Military)*

ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN

At V+ = 1V, V- = -1V, TA = 25° C unless otherwise specified

Characteristic	Limits									Units
	CA3420B			CA3420A			CA3420			
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage $\|V_{IO}\|$	—	0.8	2	—	2	5	—	5	10	mV
Input Offset Current $\|I_{IO}\|$	—	0.13	0.7	—	0.13	2	—	0.25	2	pA
Input Current $\|I_I\|$	—	0.5	1	—	0.5	3	—	1	3	pA
Large-Signal Voltage Gain	20K	100K	—	20K	100K	—	10K	100K	—	V/V
AOL (R_L = 10 KΩ)	86	100	—	86	100	—	80	100	—	dB
Common-Mode	—	560	1800	—	560	3200		560	—	μV/V
Rejection Ratio CMRR	55	65	—	50	65	—		65	—	dB
Common-Mode Input VICR +	+0.2	+0.5	—	+0.2	+0.5	—		+0.5	—	V
Voltage Range VICR -	-1	-1.3	—	-1	-1.3	—		-1.3	—	V
Power Supply Rejection	—	20	180	—	32	320	—	32	320	μV/V
Ratio PSRR ΔVIO/ΔV	75	94	—	70	90	—	70	90	—	dB
Max Output Voltage VOM +	+0.90	+0.95	—	+0.90	+0.95	—	+0.90	+0.95	—	V
RL = 00 VOM -	-0.85	-0.91	—	-0.85	-0.91	—	-0.85	-0.91	—	V
Supply Current I+	—	350	550	—	350	550	—	350	550	μA
Device Dissipation P_D	—	0.7	1.1	—	0.7	1.1	—	0.7	1.1	mW
Input Offset Voltage Temp. Drift ΔVIO/ΔT	—	4	—	—	4	—	—	4	—	μV/°C

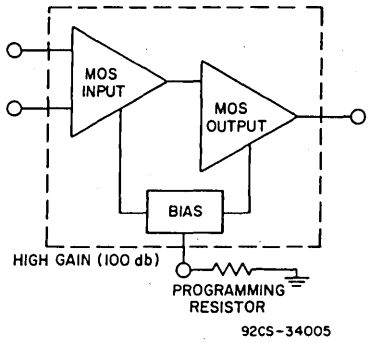
CA3440B, CA3440A, CA3440
Nanopower BiMOS Op Amp

The RCA-CA3440B, CA3440A, and CA3440 are integrated circuit operational amplifiers that combine the advantages of MOS and bipolar transistors on a single monolithic chip.

The CA3440-series BiMOS Op Amp features gate-protected PMOS transistors in the input circuit to provide very-high-input impedance and very-low-input current (10 pA). These devices operate at total supply voltages from 4 to 15 volts and can be operated over the temperature range from −55°C to +125°C. Their virtues are programmability and very low standby power consumption (300 nW). These operational amplifiers are internally phase-compensated to achieve stable operation in the unity-gain follower configuration. Terminals are also provided for use in applications requiring input offset-voltage nulling. The use of PMOS in the input stage results in common-mode input voltage capability down to 0.5 volts below the negative-supply terminal, an important attribute for single-supply applications. The output stage uses MOS complementary source-follower form which permits moderate load driving capability (10 KΩ) at very low total standby currents (50 nA).

The CA3440-series has the same 8-lead terminal pin-out used for "741" and other industry-standard op amps with two exceptions: terminals one and five must be connected to the negative supply or to a potentiometer if nulling is required. Terminal 8 must be programmed through an external resistor returned to the negative supply.

These devices are supplied in either the standard 8-lead TO-5 style package (T suffix), 8-lead dual-in-line formed-lead TO-5 style "DIL-CAN" package (S suffix), or in the 8-lead dual-in-line plastic package "Mini-DIP" (E suffix). They are also available in chip form (H suffix).



Functional diagram for CA3440 series.

Features:

- *300-nW (typ.) standby power at $V^+ = 5$ V*
- *Supply current, BW, slew rate programmable using external resistor*
- *10-pA (typ.) input current*
- *4.0 to 15-V supply*
- *Output drives typical bipolar-type loads*
- *Low-cost 8-lead Mini-DIP, TO-5*

ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN

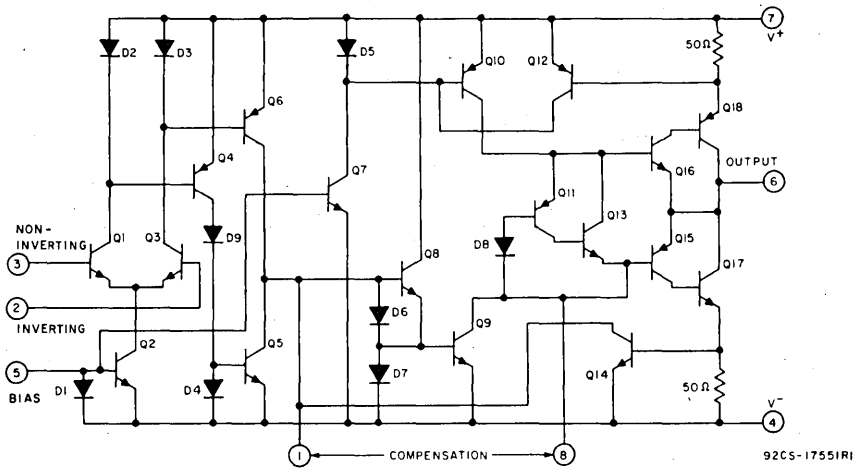
At V^+ +5 V, V^- -5 V, T_A 25°C Unless Otherwise Specified, R_{SET} 10 MΩ

CHARACTERISTIC	LIMITS									UNITS
	CA3440B			CA3440A			CA3440			
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\|V_{IO}\|$	—	0.8	2	—	2	5	—	5	10	mV
Input Offset Current, $\|I_{IO}\|$	—	2.5	10	—	2.5	20	—	2.5	30	pA
Input Current, $\|I_I\|$	—	10	30	—	10	40	—	10	50	pA
Large-Signal Voltage Gain, AOL	32K	100K	—	10K	100K	—	10K	100K	—	V/V
(R_L = 10 KΩ)	90	100	—	80	100	—	80	100	—	dB
Common-Mode	—	32	180	—	100	320	—	100	320	μV/V
Rejection Ratio, CMRR	75	90	—	70	80	—	70	80	—	dB
Common-Mode Input, $VICR^+$	+3.5	+3.7	—	+3.5	+3.7	—	+3.5	+3.7	—	V
Voltage Range, $VICR^-$	−5.0	−5.3	—	−5.0	−5.3	—	−5.0	−5.3	—	V
Power Supply Rejection Ratio, ΔVIO/ΔV	—	20	180	—	32	320	—	32	320	μV/V
PSRR	75	94	—	70	90	—	70	90	—	dB
Maximum Output Voltage, VOM^+	+3	+3.2	—	+3	+3.2	—	+3	+3.2	—	V
VOM^-	−3	−3.2	—	−3	−3.2	—	−3	−3.2	—	V
Supply Current, I^+	—	10	17	—	10	17	—	10	17	μA
Device Dissipation, P_D	—	100	170	—	100	170	—	100	170	μW
Input Offset Voltage Temperature Drift, ΔVIO/ΔT	—	4	—	—	4	—	—	4	—	μV/°C

Variable Operational Amplifiers

CA3078, CA3078A, CA6078A

Micropower Op Amps Deliver milliamperes with microwatt standby operation.



Type No.	Package	Operating Temp. Range
CA3078T	8-lead TO-5	0 to +70°C
CA3078AT		−55 to +125°C
CA6078AT		−55 to +125°C
CA3078S	8-lead TO-5 DIL-CAN	0 to +70°C
CA3078AS		−55 to +125°C
CA6078AS		
CA3078E	8-lead Mini-Dip	0 to +70°C
CA3078AE		−55 to +125°C
CA6078AE		
CA3078H	Chip	0 to +70°C
CA6078AH		−55 to +125°C

Low standby power consumption is what makes these op amps particularly suited for operation from a single 1.5 V battery. A programmable input terminal provides the designer with an opportunity to tailor the frequency response and improve the slew rate without sacrificing power.

Characteristics at T_A = 25 °C, V ± = ± 6V	Limits CA3078 R_{SET} = 1MΩ, I_Q = 100 μA Min	Typ	Max	Limits CA3078A CA6078A R_{SET} = 5.1MΩ, I_Q = 20 μA Min	Typ	Max	Units
Input Offset Voltage, V_{IO}	—	1.3	4.5	—	0.7	3.5	mV
Input Offset Current, I_{IO}	—	6	32	—	0.5	2.5	nA
Input Bias Current, I_{IB}	—	60	170	—	7	12	nA
Open-Loop Diff. Voltage Gain, A_{OL}	88	92	—	92	100	—	dB
Total Quiescent Current, I_Q	—	100	130	—	20	25	μA
Device Dissipation, P_D	—	1200	1560	—	240	300	μW
Maximum Output Voltage, V_{OM}	± 5.1	± 5.3	—	± 5.1	± 5.3	—	V
Common-Mode Input Voltage Range, V_{ICR}	—	+5.8 to −5.5	—	—	+5.8 to −5.5	—	V
Common-Mode Rej. Ratio, CMRR	80	110	—	80	115	—	dB
Maximum Output Current, I_{OM}±	—	12	—	—	12	—	mA
"Popcorn" (Burst) Noise	CA6078A	Device is rejected if total noise voltage (burst + 1/f), referred to input, exceeds 20μV peak during 30 sec. test period.					

CA3078, CA3078A Features:

- Low standby power: as low as 700 nW
- Wide supply voltage range: 0.75 to ± 15V
- High peak output current: 6.5mA min.
- Adjustable quiescent current
- Output short-circuit protection

CA6078A Features:

- Low noise (burst + l/f)
- Open-loop voltage gain: 40,000 (92 dB) min.
- Input offset voltage: 3.5 mV max.
- Operates with low total supply voltage: 1.5 min. (± 0.75 V)
- Low quiescent operating current: ajustable for application optimization
- Input bias current: adjustable to below 1 nA

Applications (All Types):

- Portable electronics
- Medical electronics
- DC amplifier
- Narrow-band or band-pass filter
- Integrator or differentiator
- Instrumentation
- Telemetry
- Summing amplifier

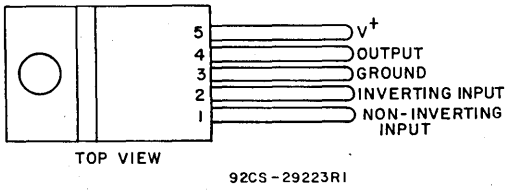
CA3105 Objective Data
Power Operational Amplifier

The RCA CA3105 Power Operational Amplifier has built-in drive capability which will help minimize PC boards parts count. Applications include direct solenoid, relay, motor, lamp, driver, pulse width modulator, positive voltage regulator, negative voltage regulator, audio power amplifier, servo controls, telephone amplifier, and windshield-wiper motor control.

Features

- *2.5 A Continuous output current*
- *VERSA VI Package with provision for heat sink mounting*
- *Thermal shutdown*
- *Peak output current up to 3.5 A*
- *1 MHz Bandwidth*

Terminal Assignment



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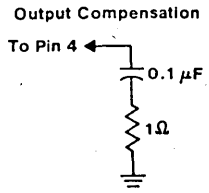
Output Compensation



Characteristics @ ± 12 Volts

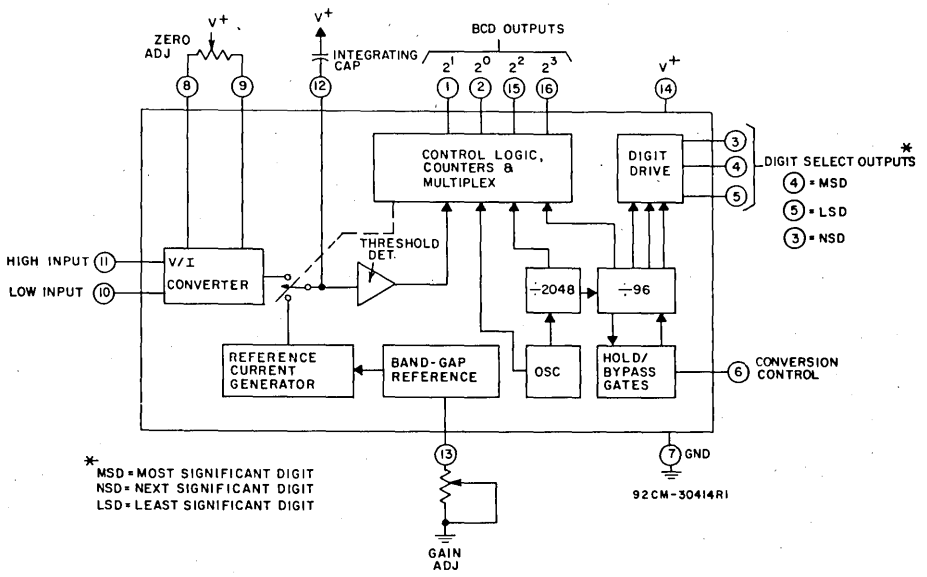
	Type	Max.	
V_{IO}	5mV	20mV	
I_{IO}	500nA	3000nA	
I_I	1 μA	10 μA	
V_{ICR}		V^- to V^+ –3V	
CMRR		65db	
PSRR	46db	40db (min)	
AOL @ RL = 8Ω	75db	70db (min)	
V_{OUT}, RL = 24Ω		V^- + 1.5 V to V^+ –2.0 V	
I_{OUT} SOURCE (Peak)*		2.5A	Continuous
I_{OUT} SINK (Peak)*		2.5A	Continuous
Slew Rate, RL = 8Ω, ACL = 100X		0.5 V/μSEC	
BW, ACL = 30X; ACL = 100X		1MHz	
Supply Current		80mA	

*Thermal Shutdown Occurs

Data-Conversion Circuits

CA3162 A/D Converter

For 3-digit digital readout system



Type No.	Package	Operating Temp. Range
CA3162E	16-Lead DIP	0 to + 75° C
CA3162H	Chip	

The CA3162E analog-to-digital converter is specially designed for use in low-cost digital readout systems. This integrated circuit and a companion type, the CA3161E BCD-to-seven-segment decoder/driver (see page 41), can be used to implement a 2-chip 3-digit readout system that features simplicity of operation and a minimum of external parts. The CA3162E A/D converter provides highly accurate conversions, exceptional temperature stability, and other features that make it particularly well suited for use in such applications.

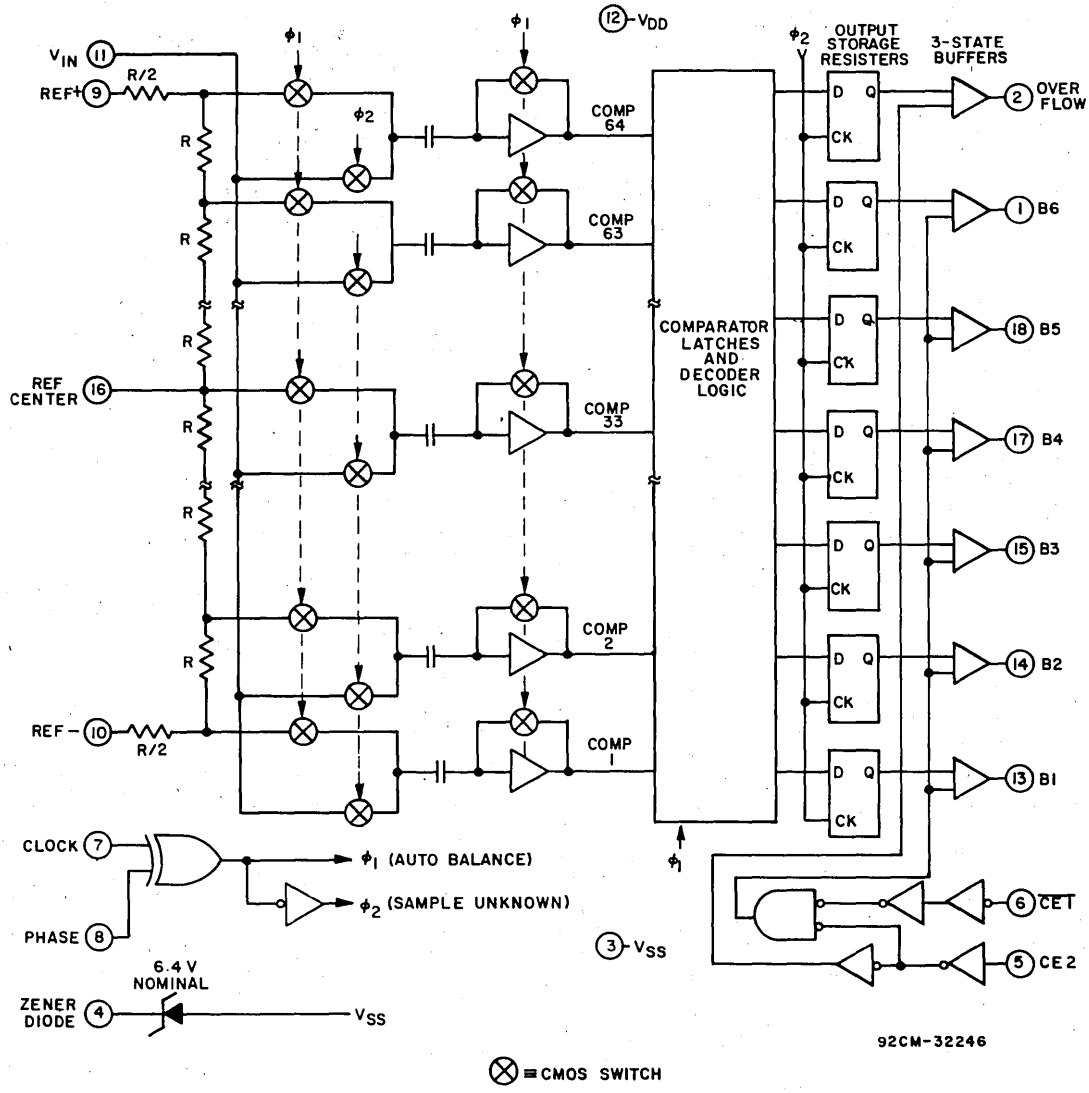
Features:

- Dual-slope A/D conversion
- Ultra-stable internal band-gap voltage reference
- Capable of reading 99 mV below ground with single supply
- Internal timing - no external clock required
- Choice of low-speed (4-Hz) or high-speed (96-Hz) conversion rate
- "Hold" inhibits conversion but maintains display
- Multiplexed operation for high efficiency
- Overload indication "EEE" for reading greater than + 999 mV, "---" for reading more negative than −99 mV

Characteristics T_A = 25°C, V^+ = 5V	Min.	Limits Typ.	Max.	Units
Operating Supply Voltage Range, V^+	4.5	5	5.5	V
Supply Current, I^+	—	—	17	mA
Input Impedance, Z_I	—	100	—	MΩ
Input Bias Current, I_{IB}	—	−80	—	nA
Unadjusted Zero Offset	−12	—	+ 12	mV
Unadjusted Gain	846	—	954	mV
Linearity	−1	—	+ 1	Count
Conversion Rate: Slow Mode	—	4	—	Hz
Fast Mode	—	96	—	
Common-Mode Input Voltage Range, V_{ICR}	−0.2	—	+ 0.2	V
BCD Sink Current at terms. 1, 2, 15, 16	0.4	1.6	—	mA
Digit Select Sink Current at terms. 3, 4, 5	1.6	2.5	—	mA

Data-Conversion Circuits

CA3300 Video CMOS/SOS 6-Bit A/D Flash Converter



The CA3300 is a 6-bit, 50-mW parallel (FLASH) analog-to-digital converter capable of accurately digitizing high-speed video signals and transient events. It is particularly useful in applications requiring sampling rates in excess of 15 mega samples/second (conversion time 66 ns.)

The CA3300 consists of 64 auto-balanced comparators, resistive ladder network, zener reference diode, decoder, and seven buffer storage registers. Two or more chips may be wired in series to increase the resolution of the conversion system. Also, two chips may be wired in parallel to increase the speed of conversion by a factor of two.

The CA3300 employs an optional diode reference circuit. An external resistor, however, is required to use this reference.

Features:

- Parallel conversion technique
- 15-MHz sampling rate (66 ns conversion time)
- 6-bit latched output
- ± ½ LSB accuracy
- 50 mW operation (+ 5-V supply)
- Overflow bit — allows cascading of units for greater resolution
- Single supply voltage (4-12V)
- Internal V_{REF} with external V_{REF} option
- CMOS/SOS process
- 3-state outputs
- TTL/CMOS compatible
- 18-lead dual-in-line ceramic package

Data-Conversion Circuits

CA3300 Video CMOS/SOS 6-Bit A/D Flash Converter (cont'd)

Applications:

- Video A/D converters:
  - digitize analog signal from TV Camera using flash A/D
  - process digital data (delayed, compressed, stretched)
- High-energy physics and nuclear physics research:
  - change and time digitizers for drift chambers
  - processing of photomultiplier signals
  - calorimeter experiments
- Radar signature analysis
- Distortion analyzers
- Motion detectors

Type No.	Package	Operating Temp. Range
CA3300	18-Lead DIC	−40 to + 85° C

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		MIN.	TYP.	MAX.	
Resolution		—	—	6	Bits
Linearity Error	V_{DD}=8 V, V_{REF}=7.68 V CLK=15 MHz, gain adjusted	—	±0.5	±0.8	LSB
Differential Linearity Error	V_{DD}=8, V_{REF}=7.68 V CLK=15 MHz	—	±0.5	±0.8	
Quantizing Error		-1/2	—	1/2	
Analog Input: Full Scale Range	V_{DD}=8 V CLK=15 MHz	2.4	—	V_{DD} +0.5	V
Input Capacitance		—	50	—	pF
Input Current		—	600	1000	μA
Gain Temperature Coefficient	V_{DD}=8 V, CLK=15 MHz	—	0.016	—	LSB/° C
Maximum Conversion Speed	V_{DD}=5 V	—	12M	—	SPS
	V_{DD}=8 V	15M	19M	—	
Device Current (Excludes I_{REF}, I_Z)	V_{DD}=5 V (CLK=11 MHz)	—	7	—	mA
	V_{DD}=8 V (CLK=15 MHz)	—	22	—	
	V_{DD}=5 V (Auto Balance State)	—	6.4	16	
	V_{DD}=8 V (Auto Balance State)	—	24	40	
Ladder Impedance		1000	1400	1800	Ω
Digital Inputs:					
Low Voltage	V_{DD}=5 V	—	—	1.5	V
	V_{DD}=8 V	—	—	2.5	V
High Voltage	V_{DD}=5 V	3.5	—	—	V
	V_{DD}=8 V	5.5	—	—	V
Input Current	V_{DD}=8 V	—	±1	—	μA
Digital Outputs:					
Output Low (Sink) Current	V_{DD}=5 V, V_O=0.4 V	1.6	10	—	mA
	V_{DD}=8 V, V_O=0.5	3.2	15	—	
Output High (Source) Current	V_{DD}=5 V, V_O=4.6 V	-0.8	6	—	
	V_{DD}=8 V, V_O=7.5 V	-1.6	9	—	
Zener Voltage	I_Z=10 mA	6.2	6.8	7.4	V
Zener Dynamic Impedance	I_Z=10 mA	—	10	30	Ω
Zener Temperature Coefficient		—	0.5	—	mV/° C
Digital Output Delay, t_d	V_{DD}=8 V	—	20	—	ns
Aperture Time	V_{DD}=8 V	—	25	—	

CA3308 Preliminary
CMOS Video Speed 8-Bit Flash Analog-to-Digital Converter

For Use in Low-Power Consumption, High-Speed Digitization Applications

The RCA CA3308 is a CMOS 250 mV parallel (FLASH) analog-to-digital converter designed for applications demanding both low-power consumption and high-speed digitization.

The CA3308 operates over a wide dynamic input-voltage range of 2.5 volts up to the dc supply voltage with maximum power consumptions as low as 250 mW, depending upon the clock frequency selected. When operated from a 5-volt supply at a clock frequency of 15 MHz, the power consumption of the CA3308 is less than 250 mW. When operated from an 8-volt supply at a frequency of 18 MHz, the power consumption is less than 750 mW.

The intrinsic high conversion rate makes the CA3308 ideally suited for digitizing high-speed signals. The overflow bit makes possible the connection of two or more CA3308s in series to increase the resolution of the conversion system. A series connection of two CA3308s may be used to produce a 9-bit high-speed converter. Operation of two CA3308s in parallel doubles the conversion speed (i.e., increases the sampling rate from 15 to 30 MHz). CA3308s in parallel may be combined with a high-speed 6-bit D/A converter, a binary adder, control logic, and an op amp to form a very high-speed A/D converter.

256 paralleled auto-balanced voltage comparators measure the input voltage with respect to a known reference to produce the parallel-bit outputs in the CA3308.

Features:

- *CMOS low power with SOS speed*
- *Parallel conversion technique*
- *15-MHz sampling rate (66-ns conversion time)*
- *8-bit latched 3-state output with overflow bit*
- *± ½ LSB accuracy*
- *Single supply voltage (4 to 8 V)*
- *2 units in series allow 9-bit output*
- *2 units in parallel allow 30-MHZ sampling rate*
- *Internal V_{REF} with ext V_{REF} option*

Applications

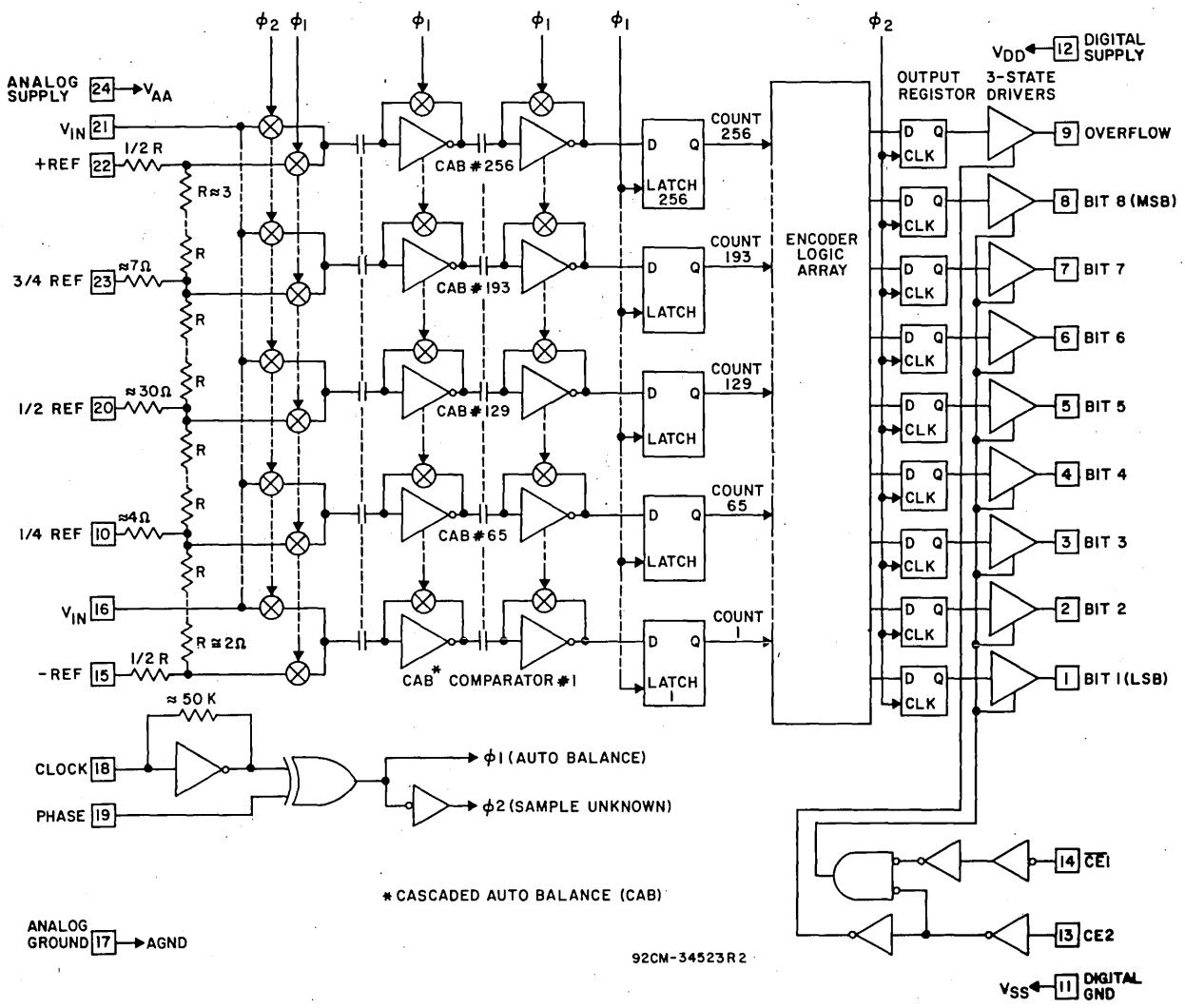
- *The CA 3308 is especially suited for high-speed conversion applications where low power is also important*
- *TV video digitizing (industrial/security/broadcast)*
- *High-speed A/D conversion*
- *Ultrasound signature analysis*
- *Transient signal analysis*
- *High-energy physics research*
- *High-speed oscilloscope storage/display*
- *General-purpose hybrid ADCs*
- *Optical character recognition*
- *Radar pulse analysis*
- *Motion signature analysis*

255 comparators are required to quantize all input voltage levels in this 8-bit converter, and the additional comparator is required for the overflow bit.

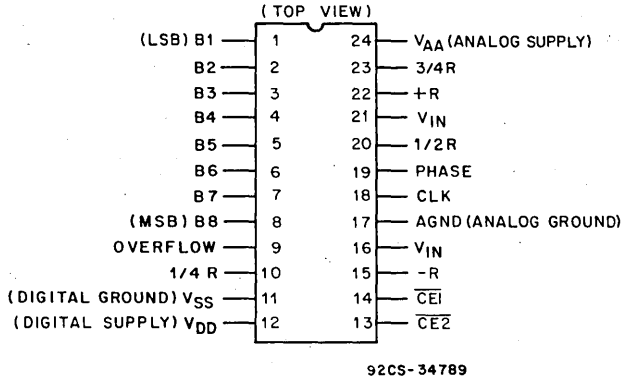
The CA3308 type is available in a 24-lead dual-in-line ceramic package (D suffix) or in chip form (H suffix).

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Resolution		—	—	8	Bits
Linearity Error	V_{DD} = 5V, V_{REF} = 7.68 V CLK = 15 MHz, gain-adjusted	—	±0.5	±0.8	LSB
Differential Linearity Error	V_{DD} = 8, V_{REF} = 7.68 V CLK = 15 MHz	—	±0.5	±0.8	
Quantizing Error		-1/2	—	1/2	
Analog Input: Full Scale Range Input Capacitance, Input Current	V_{DD} = 5 V CLK = 15 MHz	 2.4 — —	 — 50 1000	 10 — 2000	 V pF μA
Maximum Conversion Speed	V_{DD} = 5 V V_{DD} = 8 V	15M 18M	17M 20M	— —	SPS
Device Current (Excludes I_{REF}, I_Z)	V_{DD} = 5 V (CLK=15 MHz) V_{DD} = 8 V (CLK=18 MHz) V_{DD} = 5 V (Auto Zero State) V_{DD} = 8 V (Auto Zero State)	— — — —	50 22 2 —	— — 100 300	mA

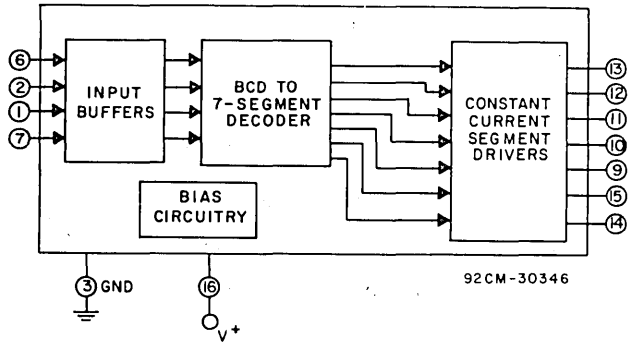


Block diagram for the CA3308



TERMINAL ASSIGNMENT

CA3161 BCD-to-Seven-Segment Decoder/Driver



The CA3161E decoder/driver decodes the multiplexed BCD signals from the A/D converter into seven line outputs that represent a decimal number from 0 to 9 on a 7-segment digital readout device. The decoder/driver circuit includes seven constant-current segment drivers that eliminate the need for any current-limiting resistors.

Type No.	Package	Operating Temp. Range
CA3161E	16-Lead DIP	0 to + 75° C
CA3161H	Chip	

Features:

- TTL-compatible input logic levels
- 15-mA (typ.) constant-current segment outputs
- Eliminates need for output current-limiting resistors
- Pin compatible with other industry standard decoders
- Low standby power dissipation: 18 mW (typ.)

Characteristics T_A = 25°C	Limits Min.	Typ.	Max.	Units
Supply Voltage Operating Range, V^+	4.75	5	5.25	V
Supply Current, I^+ (all inputs high)	—	3.5	8	mA
Output Low Current (V_O = 2V)	18	25	32	mA
Input Voltage High, V_{IH}	2	—	—	V
Input Voltage Low, V_{IL}	—	—	0.8	V

Objective Data

CA3999 3 3/4-Digit ADC Display System

Features

- Direct-current drive for LED
- No external active parts required
- 60/50 HZ filtering of input signal
- Full BiPolar input ± 2V for ± 3999 display
- Single 5V supply operation

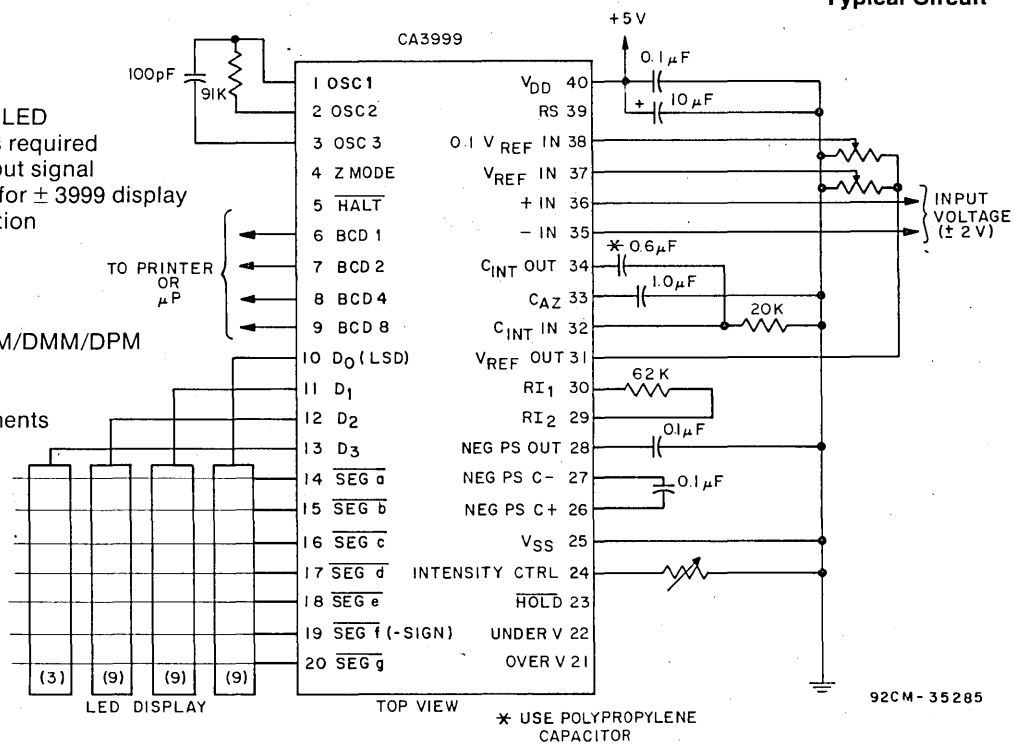
Applications

- Instrument readout DVM/DMM/DPM
- Industrial monitoring
- Weight scales
- Temperature measurements

Package

- 40L DIP

Typical Circuit



Special-Function Circuits

CA3169 Solenoid and Motor Driver (½ H Driver)

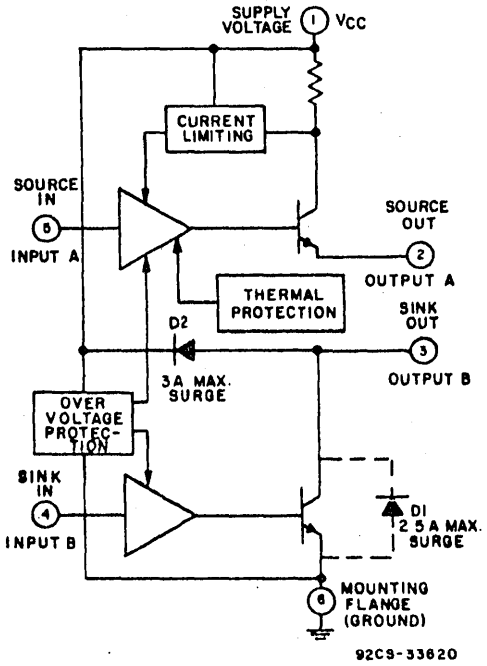


Fig. 1 - 1/2 H driver function diagram.

Features:

- Separate sink circuit and source circuit each individually controlled
- Inputs can be driven by TTL logic levels
- 600 mA (typ) output sink and source current
- Output short-circuit protection
- Thermal overload protection
- Solenoid inductive "kick" protection with thermal-clamp diodes
- Hermetic chip encapsulated in a 5-lead plastic TO-220-style package (Versa-VI)
- Horizontal and vertical mounting packages available

Applications:

- Latching solenoid driver (single and multiple)
- Non-latching solenoid driver
- Relay driver
- Lamp controller
- Lamp driver
- Motor controller (forward and reverse)
- Stepping motor controller
- On-off logic controllers (TTL logic)
- Intermediate power driver
- Triac, SCR, and transistor drivers

The CA3169 solenoid and motor driver is capable of driving lamps and other devices that can be changed between two states (on and off). This device can control relays, solenoids (latching or non-latching), motors (dc forward and reverse, dc stepping motors, and solid state power devices such as transistors, SCR's, and triacs.

The CA3169 operates with TTL logic levels on the input. The source and sink outputs are in the off condition (non-conducting) when their respective inputs are in a high state or open-circuited. The outputs are in an on state (conducting) when their respective inputs are low.

Type No.	Package	Operating Temp. Range
CA3169	5-Lead TO-220 pkg. with vertical mount	−40 to + 85° C
CA3169M	5-Lead TO-220 pkg. with horizontal mount	

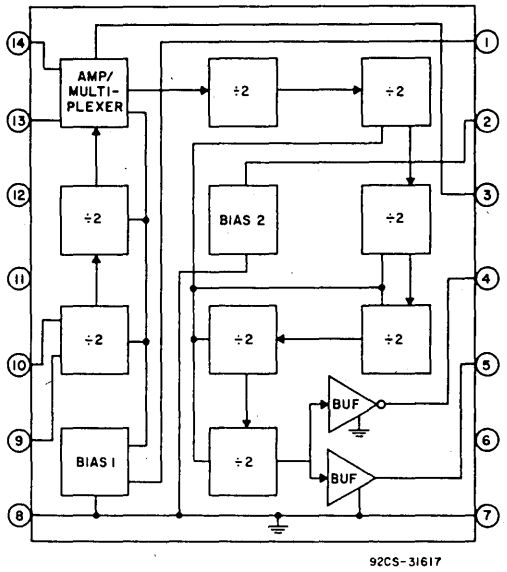
Electrical Characteristics: T_A = 25°C, V^1 = 10.5 to 18V

Characteristics	Limits Min	Limits Typ.	Limits Max	Units
Output Leakage Current (Pin 2 or Pin 3)	−110	±0.5	110	μA
Quiescent Current (Pin 1): Input Terminals Shorted	—	60	90	mA
Input Terminals Open	—	17	40	
Overvoltage Shutdown Circuit (Pin 1): Upper Trip Point	20	25	27	V
Lower Trip Point	18	21.4	23	
Input Logic Levels: Source Input (Pin 5) Sink Input (Pin 4): Threshold Voltage: Inputs Low (V_{IL})	—	0.4	0.85	V
Inputs High (V_{IH})	2	2.3	—	
Source Output: Short-Circuit Current (Pin 2-G)	0.65	1.11	2.6	A
Sink Output: (I_{SINK} = 600 mA) Output Saturation Voltage (V_3)	—	0.3	0.85	V

Special-Function Circuits

CA3179 — 1.25-GHz Prescaler

For Communications and Instrumentation Systems



92CS-31617

The RCA CA3179G performs division by 256 in the uhf mode and division by 64 in the vhf mode.

The mode of operation is selected by means of the bandswitch and the separate uhf and vhf input terminals provided. Either single- or double-ended inputs can be applied.

In the uhf mode, which is activated by applying a high level (logical 1) to the bandswitch input terminal, all eight divider stages are operative, resulting in division by 256. In the vhf mode, activated by a low level (logical 0) at the vhf input terminal, two divider stages are bypassed, resulting in division by 64. An internal amplifier/multiplexer provides this control while isolating both inputs, amplifying the input signal, and improving sensitivity.

Type No.	Package	Operating Temp. Range
CA3179G	14-Lead DIP	−55 to + 125° C
CA3179GH	CHIP	

Features:

- Broadband operation - DC to 1.25 GHz
- High sensitivity - 5mV typ.
- Standard T^2L or ECL power supply
- Dual mode operation - VHF/UHF (÷ 64/ ÷ 256)
- Power Dissipation - 325 mW typ.
- Requires only a single power supply.
- Complementary ECL outputs
- Independent VHF and UHF input terminals

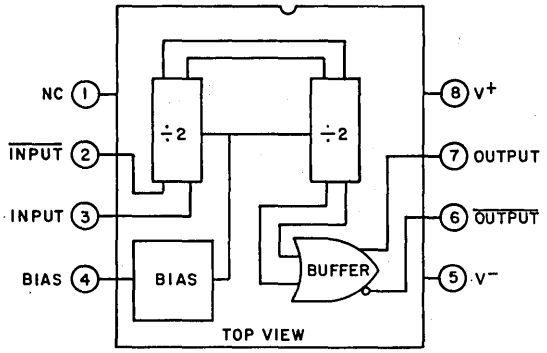
Applications:

- Digital frequency synthesizers for:
  VHF/UHF receivers
  Satellite communications
  instrumentation
- High-frequency divider for:
  UHF frequency counters
  UHF timers
  High-speed computers
  Frequency standards
  SHF second IF local-oscillator injection
  PCM communications
  Satellite communications
  Radar ranging systems
- High-frequency up-converters

Characteristics T_A = 25°C, V^+ = 5V, V^- 0V		Limits Min.	Typ.	Max.	Units
Supply Current, I^+		30	65	100	mA
Bandswitch: Voltage	V_{BL}	2.4	—	—	V
	V_{BH}	—	—	0.8	
Current	I_{BL}	−1	—	—	mA
	I_{BH}	—	—	0.5	
Sine Wave Sensitivity (f_{IN} = 90 to 275 MHz)		—	5	40	mV_{RMS}
Output Voltage:	V_{OL}	—	4.2	—	V
	V_{OH}	—	3	—	
	V_{OP-P}	0.65	1.1	1.6	
Output Rise or Fall Time: t_r, t_f		40	70	100	ns

Special-Function Circuits

CA3199 1.25 GHz ÷ 4 Prescaler



92CS-32245

Features:

- Broadband operation - DC to 1.25 GHz
- High sensitivity
- Standard T^2L or ECL power supply
- Complementary ECL outputs

Applications:

- Digital frequency synthesizers for:
  VHF/UHF receivers
  Satellite communications
  Instrumentation
- High-frequency divider for:
  UHF frequency counters
  UHF timers
  High-speed computers
  Frequency standards
  SHF second IF local-oscillator injection
  PCM communications
  Satellite communications
  Radar ranging systems
- High-frequency up-converters

Type No.	Package	Operating Temp. Range
CA3199	8-lead MINIDIP	0 to + 85° C

The CA3199 is a bipolar integrated fixed-ratio counter (divide-by-four) circuit which operates over the VHF/UHF frequency band (DC to 1000 MHz). The CA3199 accepts either single or double-ended ac-coupled input signals and provides complementary emitter-follower outputs at standard ECL logic levels.

Characteristics: T_A = 25°C, V^+ = 5V, V_5 = Ground	Conditions	Limits Min.	Typ.	Max.	Units
Output Voltage:					
High-Level ("1") V_{OH}	Outputs unloaded	—	4.2	—	V
Low-Level ("O") V_{OL}		—	3.4	—	
Internal Bias Voltage, V_{BIAS}	Pin 4, floating	—	2.3	—	V
Power Supply Drain Current, I_D		35	60	85	mA
Input Sensitivity (sinusoidal)	Single-ended input 1000 MHz	—	400	—	mV_{p-p}
Output Voltage Swing, V_{OP-P}	V_6, V_7	0.6	—	—	V_{P-P}
Transition Time:					
High-level ("1")	Outputs unloaded	—	0.6	—	ns
Low-level ("O")		—	0.6	—	
Input Capacitance, C_I		—	2.5	—	pF
Input Resistance, R_I		—	400	—	Ω

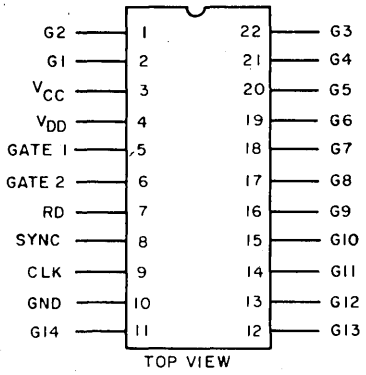
CA3207E, CA3208E
Sequencer Driver and Segment Latch-Driver for Vacuum Fluorescent Displays

The RCA-CA3207E and CA3208E are sequence-driver and segment latch-driver used in combination to drive vacuum fluorescent display devices of up to 14 segments with up to 14 characters of display. The CA3207E selects the digit or character to be displayed in sequence and the CA3208E turns on the required number of segments of the character selected.

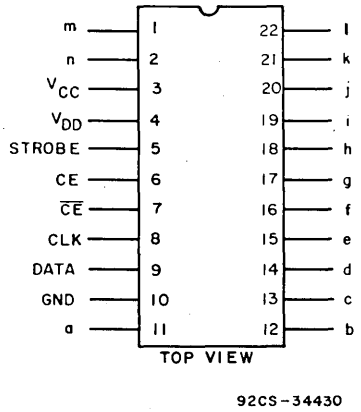
At any one time, only 1 character is lit and 13 characters are "off", but to the eye, all characters appear lit at once.

Each sequencer-driver will turn "on" 14 characters at one time. The sequencer-driver clock line may be used to drive the cross-coupled CE and CE inputs of 2 segment-latch drivers to provide for the display of up to 28 characters (see Fig. 12). The logic portion of both circuits use CMOS technology. They operate at 5 volts. The output drivers use bipolar technology and operate at supply voltages up to 55 volts. The CA3207E will source 40-mA per character and the CA3208E will source 7.5-mA per segment.

Both types are supplied in the 22-lead dual-in-line plastic package (E suffix), and they are also available in chip form (H suffix).



TERMINAL ASSIGNMENT CA3207E



TERMINAL ASSIGNMENT CA3208E

Features:
- *Serial input, parallel output*
- *Total of 14 outputs*
- *CMOS and T^2L compatible inputs*
- *Low-power CMOS Logic-Bipolar high-voltage output*

Sequencer Driver (CA3207E)
- *Sequentially turns on 1 of 14 characters (or 2 of 28 when used with 2 CA3208E's)*
- *Signal dimming through Gates 1 or 2*
- *Use with vacuum fluorescent display or any display that will work within its limits of 35 V to 55 V*
- *Will operate in an output voltage range of 35 V to 55 V*

Latch Driver (CA3208E)
- *Choose which of 14 segments of alphanumeric display are to light*
- *Two devices may be run in parallel to control a total of 28 characters by means of the CE and $\overline{CE}$ pins*

STATIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{CC} = +55 V, V_{DD} = +5 V, C_L = 50 pF

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			CA3207E		CA3208E		
			Min.	Max.	Min.	Max.	
V_{CC} Supply Current	I_{CC}	No inputs "On"	—	10	—	—	mA
		Half inputs HIGH	—	—	—	65	
V_{DD} Supply Current	I_{DD}	All inputs HIGH	—	1	—	—	mA
		All inputs LOW	—	—	—	800	μA
		All inputs HIGH	—	—	—	1	
Input Current, Low-Level	I_{IL}	V_{IN} = 0 V	—	1	—	1	μA
Input Current, High-Level	I_{IH}	V_{IN} = 5 V	—	1	—	1	
Output Voltage, Low-Level	V_{OL}	R_L = 1.335K	—	1	—	—	V
		R_L = 7.1K	—	—	—	1	
Output Voltage, High-Level	V_{OH}	I_{OH} = 40 mA	53	—	—	—	
		I_{OH} = 7.5 mA	—	—	53	—	
Input Low Voltage	V_{IL}		—	1.5	—	1.5	V
Input High Voltage	V_{IH}		3.5	—	4.5	—	

CA3211E

Preliminary Data

VHF/UHF Prescaler

The RCA-CA3211E* is an integrated-circuit prescaler intended for use in TV frequency synthesis tuning systems over an input frequency range of 90 to 1000 MHz. It performs division by 256 in the UHF and VHF mode.

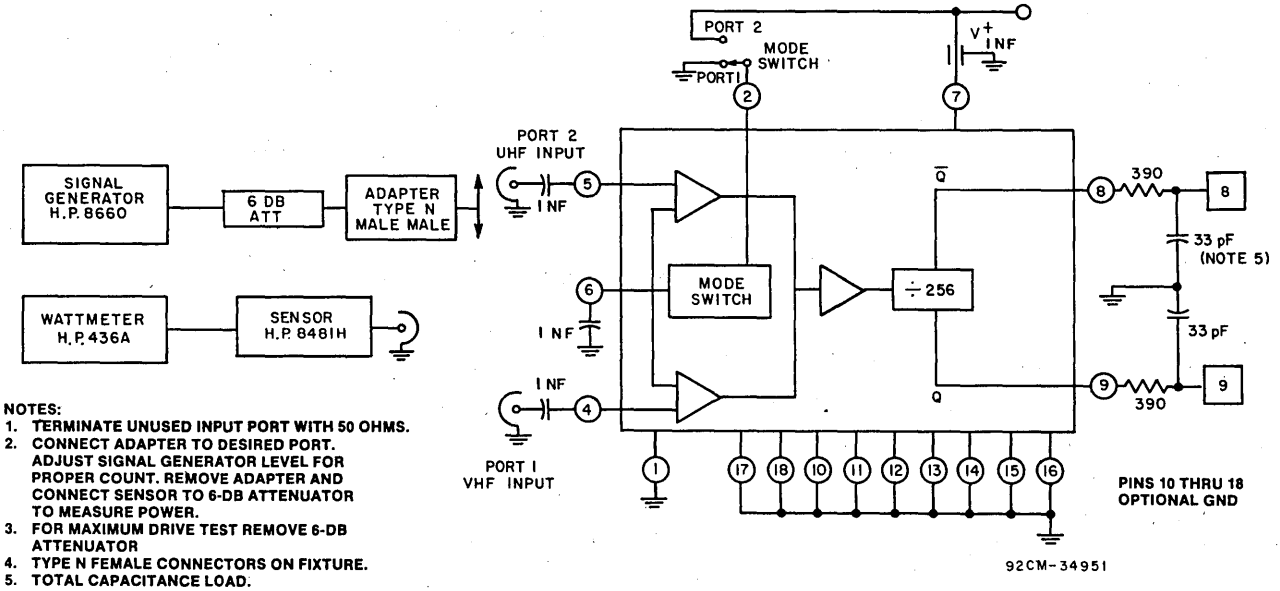
The mode of operation can be selected by means of the bandswitch and the separate UHF and VHF input terminals provided. The output is a complementary emitter-coupled stage with controlled slew rate for harmonic suppression.

The CA3211E is supplied in an 18-lead dual-in-line plastic package.

Features

- *Divide by 256*
- *Input frequency to 1 GHz*
- *Dual input ports electrically selectable*
- *Input sensitivity*
  < 10 μW typical
  (Generator available power into a 50-Ω load)
- *5-V power supply*
- *Balanced output ports*

CHARACTERISTIC T_A=25°C, V+=5.0 V	LIMITS Min.	Typ.	Max.	UNITS
Supply Current, Terminal 7	30	65	110	mA
Band Change Voltage:				
Port 1 Select (VHF)	−0.5	0	0.6	V
Port 2 Select (UHF)	3	5	18	
Band Change Current, Terminal 2:				
At 0 Volts	—	—	−1	mA
At 18 Volts	—	—	2	
Input Sensitivity, f_{IN}:				
40 MHz	—	15	—	mV rms
80 MHz	—	10	35	
150-800 MHz	—	10	20	
900 MHz	—	10	35	
1000 MHz	—	15	45	
Output at Terminal 9 or 8:				
Mean Value	—	3.5	—	V dc
Peak-Peak Swing	0.75	1	—	V_{p-p}
Rise or Fall Time	—	70	—	ns



NOTES:
1. **TERMINATE UNUSED INPUT PORT WITH 50 OHMS.**
2. **CONNECT ADAPTER TO DESIRED PORT. ADJUST SIGNAL GENERATOR LEVEL FOR PROPER COUNT. REMOVE ADAPTER AND CONNECT SENSOR TO 6-DB ATTENUATOR TO MEASURE POWER.**
3. **FOR MAXIMUM DRIVE TEST REMOVE 6-DB ATTENUATOR**
4. **TYPE N FEMALE CONNECTORS ON FIXTURE.**
5. **TOTAL CAPACITANCE LOAD.**

Block diagram and test circuit of the CA3211E.

CA3219E Preliminary Data
Quad Power NAND Driver For Interfacing Low Level Logic and High Current Loads

The RCA-CA3219E quad power NAND driver contains four NAND gate switches for interfacing low-level logic to inductive and resistive loads such as: relays, solenoids, AC and DC motors, heaters, incandescent lamps, and segment drivers.

Diodes in the outputs match the IC to inductive loads.

To allow for maximum heat transfer from the sub-chips, the two center leads are directly connected to the die substrate and to the ground bond pads. In free air, junction-to-air thermal coefficient (θ_{J-A}) is 62°C/W* (typical).

The CA3219E is supplied in the 16-lead dual-in-line (E suffix) plastic package.

*This coefficient can be lowered to 45°C/W (typical) by suitable design of the PC board to which the CA3219E is soldered.

Features:

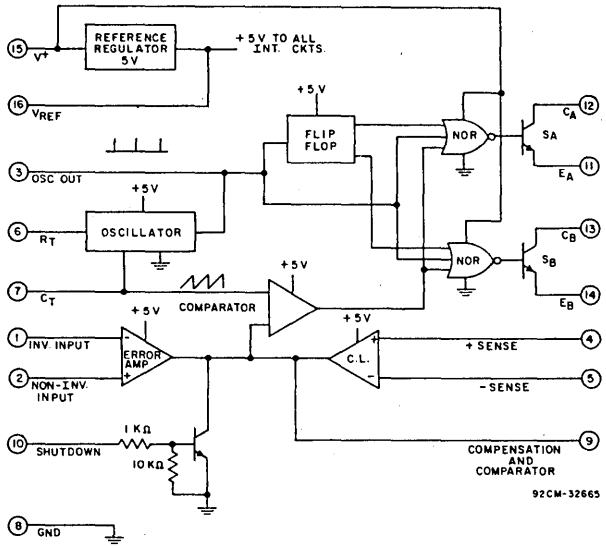
- *Driven outputs capable of switching 600-mA load currents*
- *Inputs compatible with TTL or 5-V CMOS logic*
- *Maximum amount of heat transfer from the sub-chips*
- *Suitable for resistive or inductive loads*

ELECTRICAL CHARACTERISTICS at T_A = 25°C; V_{CC} = 5V

CHARACTERISTIC	LIMITS MIN.	LIMITS MAX.	UNITS
Output Leakage Current (Icex) V_{CE} = 50 V V_{IN} = 0.8V	—	100	μA
Output Sustaining Voltage V_{CE}(sus) I_c = 100MA V_{IN} = 0.8V	25	—	V
Coll.-Emitter Saturation Voltage V_{CE}(sat) I_c = 100mA V_{in} 2.4V I_c = 400mA V_{in} 2.4V I_c = 600mA V_{in} 2.4V	 — — —	 0.3 0.5 0.7	 V V V
Input Low Voltage V_{IL} Inputs and enable	—	0.8	V
Input Low Current I_{IL} V_{IN} = 0.8V	—	+10	μA
Input High Threshold V_{IH} I_c = 600mA	2	—	V
Input High Current I_c = 700mA V_{IN} = 5.5V	—	40	μA
Supply Current all Outputs on I_{CC} (ON) I_c = 0.0 to 700mA, V_{cc} = V_{IH} = 5.5V	—	80	mA
Supply Current all Outputs off I_{CC} (OFF)	—	5	mA
Clamp Diode Leakage Current IR VR = 50V	—	100	μA
Clamp Diode Forward Voltage UF IF=1A IF=1.5A	 — —	 1.5 2	 V V

Power Control Circuits

CA1524, CA2524, CA3524 | For Pulse-Width Modulated Switching Regulators



Features:

- Complete PWM power-control circuitry
- Separate outputs for single-ended or push-pull operation
- Line and load regulation of 0.2% typical
- Internal reference supply with 1% max. voltage variation over full temperature range
- Standby current of less than 10 mA
- Frequency of operation beyond 100 kHz
- Variable output dead time of 0.5 to 5 μs
- Low V_{CE}(sat) over temperature range
- Alternate source for the industry standard SG1524 series

Applications:

- Positive and negative regulated supplies
- Dual-output regulators
- Flyback converters
- DC-dc transformer-coupled regulating converters
- Single-ended dc-dc converters
- Variable power supplies
- Electronic scales

Type No.	Package	Operating Temp. Range
CA1524E	16-Lead DIP	−55 to + 125°C
CA2524E		0 to + 70°C
CA3524E		
CA3524H	Chip	

The CA1524 series (CA1524, CA2524, and CA3524) of pulse-width-modulated IC switching regulators offers designers of off-line switching power supplies exceptional design flexibility, high operating efficiency, low parts count, and regulation performance rivaling that of linear regulator supplies.

Separate outputs for single-ended and push-pull operation, an operating frequency greater than 100 kHz, and a variable-output dead time of from 0.5 to 5 μs make the CA1524 series types highly versatile. The output transistors of this series of IC regulators are operated with low collector saturation voltage to assure higher operating efficiency and low on-chip temperature.

The CA1524 Series, in addition to having all the necessary control circuits for switching regulator applications, employs two output n-p-n transistors. These transistors are internally current-limited and can be used in a variety of switching regulator configurations. Three of which are:

1. Single-ended/single-stage configurations such as those used in forward and flyback converters.
2. Single-ended/parallel-output stages for switching regulators.
3. Dual or individual stage mode for push-pull, ½ bridge, etc.

Electrical characteristics: T_A = −55 to + 125°C for CA1524; 0 to + 70°C for CA2524, CA3524, V^+ = 20V, f = 20 kHz

Type	V^+ Range V	V_O Range V	Load Regulation % V_O (Typ)	Ripple Rejection db (Typ)	Temp. Stability % (Max)	Total Standby Current Ma (Max)	V_{CE} (sat) V (Typ)	Short-Circuit Current Limit mA (Typ)
CA1524	8 to 40	4.8 to 5.2	0.2	66	1	10	0.8	100
CA2524	8 to 40	4.8 to 5.2	0.2	66	1	10	0.8	100
CA3524	8 to 40	4.6 to 5.4	0.2	66	1	10	0.8	100

CA3227E, CA3246E Preliminary Data
High-Frequency N-P-N Transistor Arrays

For Low-Power Applications at

Frequencies up to 1.5 GHz

The RCA-CA3227E and CA3246E* consist of five general-purpose silicon n-p-n transistors on a common monolithic substrate. Each of the transistors exhibits a value of f_T in excess of 3 GHz, making them useful from dc to 1.5 GHz. The monolithic construction of these devices provides close electrical and thermal matching of the five transistors.

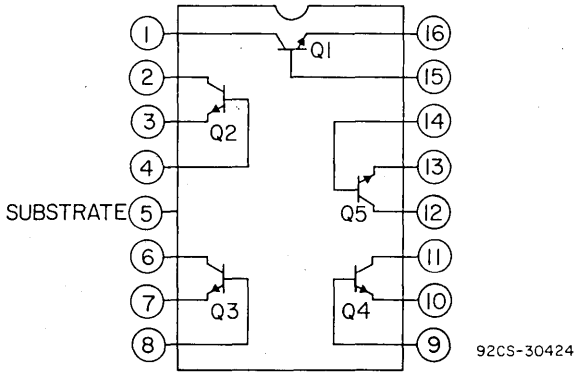
The CA3227E is supplied in a 16-lead dual-in-line plastic package and the CA3264E is supplied in a 14-lead dual-in-line plastic package.

Features:

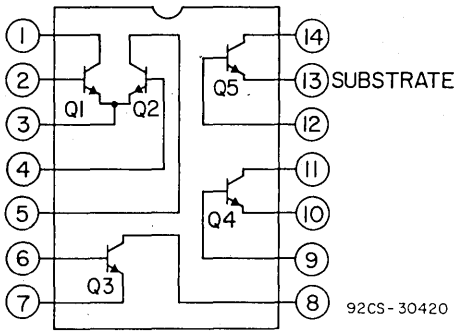
- *Gain-Bandwidth Product (f_T) > 3 GHz*
- *Five transistors on a common substrate*

Applications

- *VHF amplifiers*
- *VHF mixers*
- *Multifunction combinations — RF/mixer/oscillator*
- *IF Converter*
- *IF amplifiers*
- *Sense amplifiers*
- *Synthesizers*
- *Synchronous detectors*
- *Cascade amplifiers*



CA3227E Schematic Diagram (Top View)



CA3246E Schematic Diagram (Top View)

STATIC ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
For Each Transistor:							
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0		12	20	—	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0		8	10	—	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	*$_{C1}$ = 10 μA, I_B = 0, I_E = 0		20	—	—	V
Emitter-Cutoff-Current*	I_{EBO}	V_{EB} = 4.5 V, I_C = 0		—	—	10	μA
Collector-Cutoff-Current	I_{CEO}	V_{CE} = 5 V, I_B = 0		—	—	1	μA
Collector-Cutoff-Current	I_{CBO}	V_{CB} = 8 V, I_E = 0		—	—	100	nA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 6 V	I_C = 10 mA		110	—	
			I_C = 1 mA	40	150	—	
			I_C = 0.1 mA	—	150	—	
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 6 V	I_C = 1 mA	0.62	0.71	0.82	V
Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$	I_C = 10 mA, I_B = 1 mA		—	0.13	0.50	V
Base-to-Emitter Saturation Voltage	$V_{BE(sat)}$	I_C = 10mA, I_B = 1 mA		0.74	—	0.94	V

*On small geometry, high frequency transistors, it is very good practice never to take the Emitter Base Junction into reverse breakdown. To do so may permanently degrade the h_{FE}. Hence the use of I_{EBO} rather than $V_{(BR)EBO}$.

Product Classification Chart

Industrial Circuits

OPERATIONAL AMPLIFIERS

General Purpose

Single Unit	Dual Unit
CA101	CA082*
CA201	CA083*
CA301A	CA158
CA307	CA258
CA741	CA358
CA748	CA747
CA3105	CA1458
CA3152*	CA1558
CA3193*	CA2904
CA3420*	Quad Unit
CA3493*	CA084*
CA6741•	CA124
	CA224
	CA324
	CA3401

General Purpose Wideband

- Single Unit
  - CA080*
  - CA081*
  - CA3008
  - CA3010
  - CA3015
  - CA3016
  - CA3029
  - CA3030
  - CA3037
  - CA3038
  - CA3100*
  - CA3130*
  - CA3140*
  - CA3160*
- Dual Unit
  - CA3240*
  - CA3260*

Variable

- High Current
  - CA3094
- Micropower
  - CA3060
  - CA3078
  - CA3080
  - CA3440*
  - CA6078A•
- Dual Unit
  - CA3280

DIFFERENTIAL AMPLIFIERS

- CA3000
- CA3001
- CA3004
- CA3005
- CA3006
- CA3007
- CA3026
- CA3028
- CA3040
- CA3049
- CA3050
- CA3051
- CA3053
- CA3054
- CA3102

ARRAYS

Amplifier/Diode

- Amplifier
  - CA3026
  - CA3035
  - CA3048
  - CA3049
  - CA3052
  - CA3054
  - CA3060
  - CA3102
- Diode
  - CA3019
  - CA3039
  - CA3141

Transistor

CA1724	CA3096
CA1725	CA3097
CA3018	CA3118
CA3036	CA3127
CA3045	CA3128
CA3046	CA3138
CA3050	CA3146
CA3051	CA3183
CA3081	CA3227
CA3082	CA3246
CA3083	▲CA3600
CA3084	
CA3086	
CA3093	

POWER CONTROL CIRCUITS

- Voltage Regulators
  - CA723
  - CA1524
  - CA2524
  - CA3085
  - CA3524
- Zero-Voltage Switches
  - CA3058
  - CA3059
  - CA3079
- Programmable Schmitt Triggers
  - CA3098
  - CA3099
- Solenoid & Motor Drivers
  - CA3169
  - CA3219
- Power Amplifiers
  - CA3020
  - CA3105
- Automotive Ignition Switch
  - CA3165
- Universal Controller
  - CA3228

DATA CONVERSION

- A/D Converters
  - CA3162
  - CA3300
  - CA3308
  - CA3999
- Display Drivers
  - CA3161
  - CA3168
  - CA3081
  - CA3082
  - CA3207*
  - CA3208*

VOLTAGE COMPARATORS

- Single Unit
  - CA311
  - CA3098+
  - CA3099+
- Dual Unit
  - CA3290*
- Quad Unit
  - CA139
  - CA239
  - CA339

SPECIAL FUNCTION CIRCUITS

- Timer
  - CA555
- Four Quadrant Multiplier
  - CA3091
- Single-Chip Detector Alarm Systems
  - CA3164*
- Prescalers
  - CA3179
  - CA3199
  - CA3211

Automotive Circuits

- CA3105
- CA3130*
- CA3160*
- CA3161
- CA3165
- CA3168
- CA3169
- CA3207*
- CA3208*
- CA3219
- CA3228
- CA3260*
- CA3290*

Broadband (Video) Amplifiers

- CA080*
- CA081*
- CA082*
- CA083*
- CA084*
- CA3001
- CA3002
- CA3020
- CA3021
- CA3022
- CA3023
- CA3040
- CA3071
- CA3100*
- CA3130*
- CA3140*
- CA3160*
- CA3240*
- CA3260*

MOS/FET's

Single Gate

3N128	3N153
3N138	3N154
3N139	40467A
3N142	40468A
3N143	40559A
3N152	

Dual Gate

3N140	40600
3N141	40601
3N159	40602
	40603
	40604

Dual Gate Protected

3N187	40673
3N200	40819
3N204	40820
3N205	40821
3N206	40822
3N211	40823
3N212	40841
3N213	

•Low-noise versions of CA741 and CA3078 *BiMOS types ▲CMOS types +Programmable

Product Classification Chart

Consumer Circuits

TV/CATV CIRCUITS

AFT
- CA3064
- CA3139

Chroma Systems
- CA1398
- CA3070
- CA3071
- CA3072
- CA3121
- CA3126
- CA3128**
- CA3137
- CA3145
- CA3151
- CA3158
- CA3170
- CA3172
- CA3194**
- CA3201
- CA3217
- CA3221

Horizontal/Vertical Systems
- CA920A
- CA1391
- CA1394
- CA3154
- CA3159
- CA3190***
- CA3202
- CA3210
- CA3223***

Sync/AGC Circuits
- CA3120
- CA3142

Luminance Processors
- CA3135
- CA3143
- CA3144
- CA3156

Multiplex Decoders
- CA758
- CA1310A
- CA3090A
- CA3195

PIX IF
- CA270
- CA1352
- CA3068
- CA3136
- CA3153
- CA3191
- CA3192
- CA7607
- CA7611

Remote Control
- CA3035

Sound IF
- CA1190
- CA1191
- CA2111A
- CA2136A
- CA3011
- CA3012
- CA3013
- CA3014
- CA3041
- CA3042
- CA3065
- CA3134

Tuning
- CA3140
- CA3152*
- CA3163
- CA3166
- CA3168
- CA3199
- CA3211

Videodisc Circuits
- CA2111A
- CA3215
- CA3216
- CD3226▲

AUDIO CIRCUITS

Drivers
- CA3094

Power Amplifiers
- CA2002
- CA2004

Preamplifiers
- CA3036
- CA3048
- CA3052

RADIO CIRCUITS

AM/FM Communications Circuits
- CA2111A
- CA2136A
- CA3011
- CA3012
- CA3013
- CA3014
- CA3043
- CA3075
- CA3076
- CA3088
- CA3089
- CA3123
- CA3143
- CA3179
- CA3189
- CA3199
- CA3209

FM IF Circuits

Gain Blocks
- CA3011
- CA3012
- CA3076

Subsystems
- CA2111A
- CA2136A
- CA3013
- CA3014
- CA3075
- CA3089
- CA3189
- CA3209

MOS/FET's

Single Gate
- 3N128
- 3N138
- 3N139
- 3N142
- 3N143
- 3N152
- 3N153
- 3N154
- 40467A
- 40468A
- 40559A

Dual Gate
- 3N140
- 3N141
- 3N159
- 40600
- 40601
- 40602
- 40603
- 40604

Dual Gate Protected
- 3N187
- 3N200
- 3N204
- 3N205
- 3N206
- 3N211
- 3N212
- 3N213
- 40673
- 40819
- 40820
- 40821
- 40822
- 40823
- 40841

▲CMOS types *BiMOS types **PAL ***625 Line

LVDT SIGNAL CONDITIONER NE/SE5520

Preliminary

DESCRIPTION

The NE/SE5520 is a signal conditioning circuit for use with Linear Variable Differential Transformers (LVDT). The chip includes a low distortion amplitude stable sine wave oscillator with programmable frequency to drive the primary of the LVDT; a synchronous demodulator to convert the LVDT output amplitude and phase to position information; and an output amp to provide gain and filtering.

FEATURES

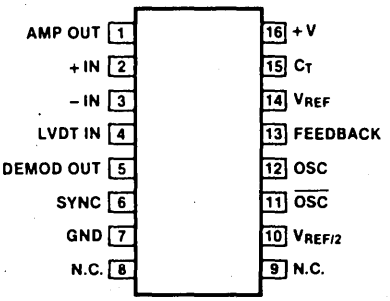
- Oscillator frequency: 1kHz to 20kHz
- Low distortion
- Capable of ratiometric operation
- Single supply operation 5V to 20V or dual supply ±2.5V to ±10V
- Low power consumption

APPLICATIONS

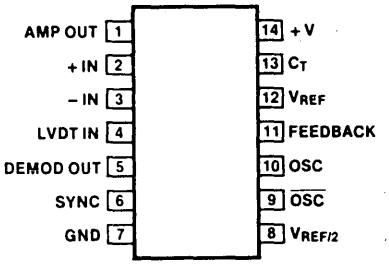
- LVDT signal conditioning
- RVDT signal conditioning

PIN CONFIGURATION

F PACKAGE



N PACKAGE

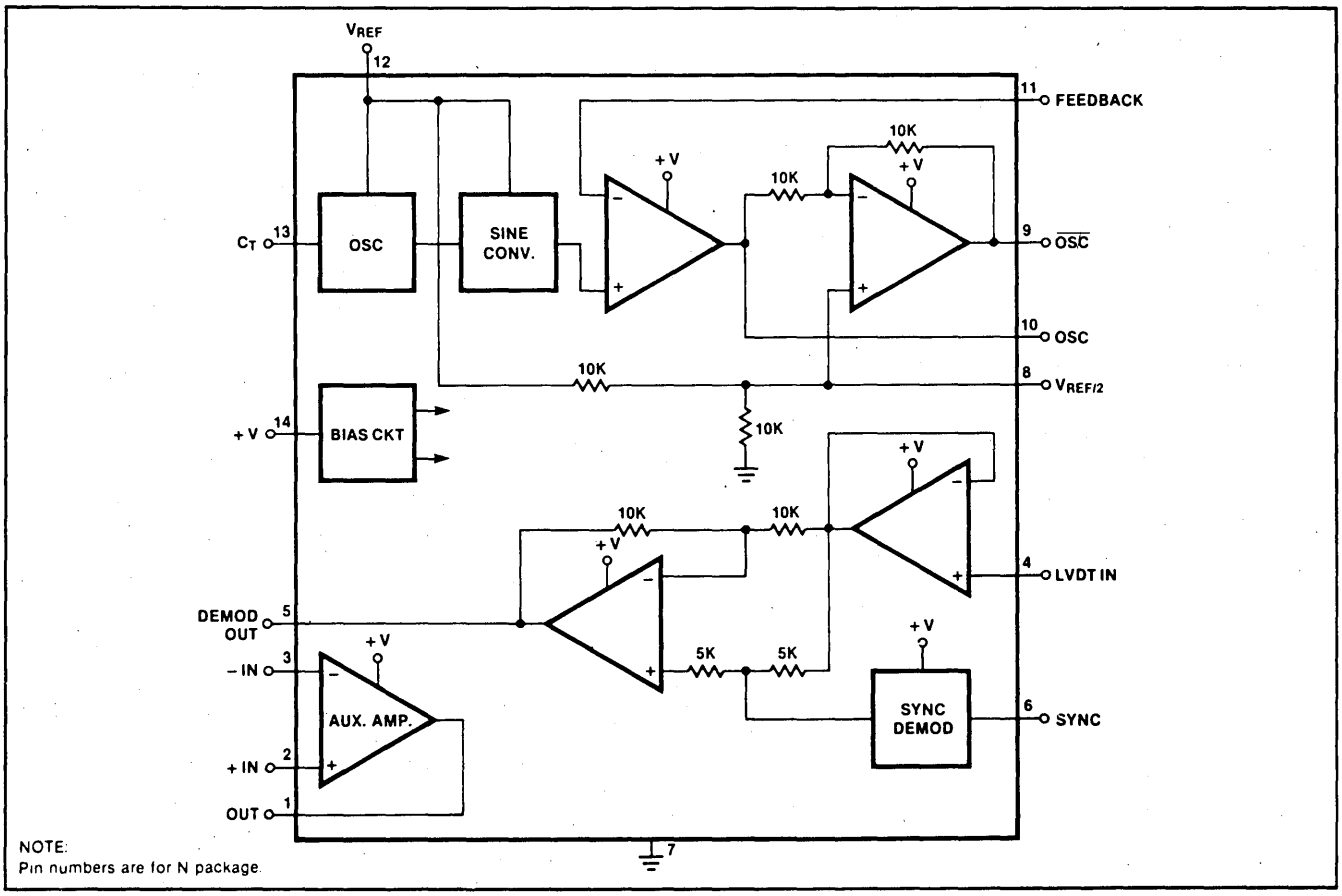


TOP VIEWS
ORDER NUMBERS
NE5520F, SE5520F (16-Pin)
NE5520N (14-Pin)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	+ 25	V
Split supply voltage	± 12.5	V
Operating temperature range		
SE5520	– 55 to + 125	°C
NE5520	0 to + 70	°C
Storage temperature range	– 65 to 150	°C
Power Dissipation (Note 1)	840	mW

BLOCK DIAGRAM



NOTE:
Pin numbers are for N package.

Signetics

LVDT SIGNAL CONDITIONER NE/SE5520

Preliminary

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_R = V+ = 10V$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE5520			NE5520			UNIT
		Min	Typ	Max	Min	Typ	Max	
Supply current	Over temp.		7.0	10		7.0	10	mA
Reference current	Over temp.		5.5	10		5.5	10	mA
Reference voltage range	Over temp.	5		V+	5		V+	V
Power Dissipation			120	220		120	220	mW
Oscillator section								
Oscillator output			$\frac{V_R}{8.7}$			$\frac{V_R}{8.7}$		Vrms
Sine wave distortion			4			4		%
Initial amplitude error				±3			±3	%
Tempco of amplitude				0.05			0.05	%/°C
Voltage coef. of amplitude error				2.5			2.5	%/V
Initial accuracy of osc. frequency				20			20	%
Tempco of frequency error			0.05			0.05		%/°C
Voltage coef. of frequency			2.5			2.5		%/V(V_R)
Oscillator output load current			15			15		mA (rms)
	Over temp.	5			8			mA (rms)
Demodulator section								
Linearity error	Over temp.		0.05	0.1		0.05	.1	%
Maximum demodulator input	Over temp. range	$\frac{V_R}{2} - 0.4$		$\frac{V_R}{2} - 0.4$	$\frac{V_R}{2} - 0.5$		$\frac{V_R}{2} + 0.5$	V
Demodulator offset voltage	Over temp. range			65			65	mV
Demodulator input current	Over temp.	−500	−300		−500	−300		nA
$V_R/2$ accuracy	Over temp.	−3	±0.5	+3	−3	±0.5	+3	%
Output amplifier								
Input offset voltage	Over temp.	−7.5		+7.5	−10		10	mV
Input bias current	Over temp. range	−500	−300		−500	−300		nA
Input offset current		−100		100	−100		100	nA
Gain	R_L= 10kΩ over temp.	30	250			100		V/mV
Slew rate			1.5			1.5		V/μsec
Gain bandwidth	$A_V = 1$		1			1		MHz
Output voltage swing	R_L= 10K over temp.	1.8		V+ −1.5	1.5		V+ −1.5	V
Output short circuit current				50			50	mA

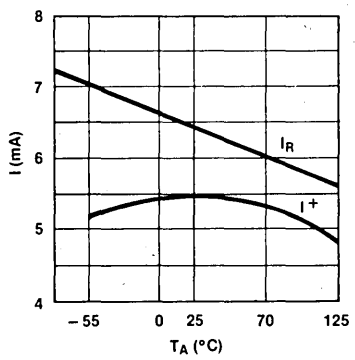
NOTE
Rating applies to ambient temperatures up to 70°C. Above 70°C derate linearly at 7.6 mW/°C for the plastic package and 7.3 mW/°C for the cerdip package.

LVDT SIGNAL CONDITIONER NE/SE5520

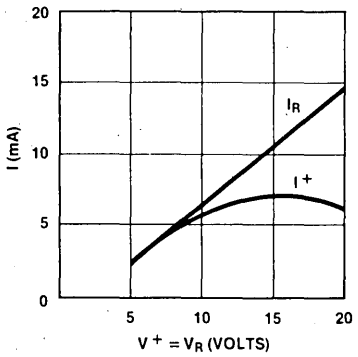
Preliminary

TYPICAL PERFORMANCE CHARACTERISTICS

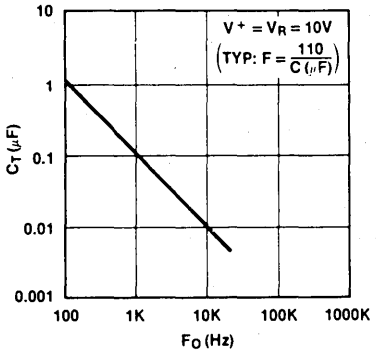
I_R AND I^+ vs TEMPERATURE



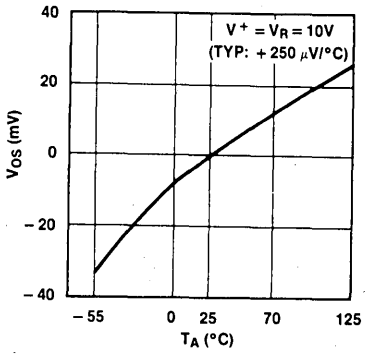
I_R AND I^+ vs VOLTAGE



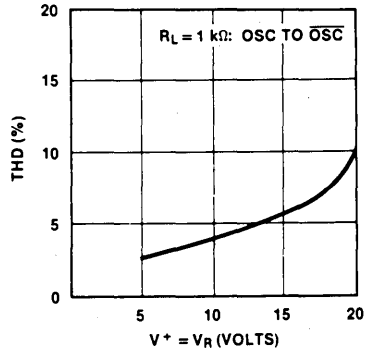
F_O vs C_T



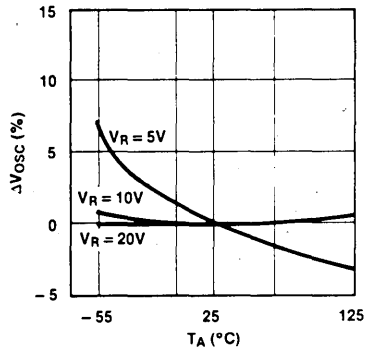
DEMODULATOR OFFSET vs TEMPERATURE (NORMALIZED TO 25°C)



DISTORTION OF SINE WAVE vs REFERENCE VOLTAGE



OSCILLATOR AMPLITUDE VARIATION WITH TEMPERATURE



LINEAR

Signetics

LVDT SIGNAL CONDITIONER NE/SE5520

Preliminary

ALL PIN NUMBERS REFER TO N PACKAGE

INTRODUCTION

An LVDT is an electromechanical transducer which makes possible the measurement of very small motion in a structure or mechanical device. Mechanical motion is translated to an electrical signal which contains position information much as a radio frequency carrier contains sound information. The position information from the LVDT is contained in the phase and amplitude of the output AC waveform. In order to remove the position information (demodulation), a system such as is shown in block form in Figure 1 must be used. Once signal demodulation is achieved the position data may be read out on a meter or digital display in addition to being processed by microprocessor or computer. The Signetics NE5520 is a new *Monolithic LVDT Driver-Demodulator* designed to interface with most LVDT's presently being used in the industry.

Uses will range over a large number of potential applications including the accurate measurement of position, pressure, load weight, angular position and even acceleration. Historically, LVDT's have been used in the following applications:

- Load cell
- Linear motion
- Torque cell
- Vibration
- Fluid pressure
- Accelerometer
- Inclinometer
- Seismic load cell

MOTION MAY BE

- Linear
- Rotary

The NE5520 provides sinusoidal drive to the Linear Variable Differential Transformer (LVDT), the output of which is buffered, rectified and phase demodulated to obtain both direction and displacement information in the form of a DC output signal (Figure 2).

THE LVDT WITH SINEWAVE EXCITATION AND SYNCHRONOUS DEMODULATION

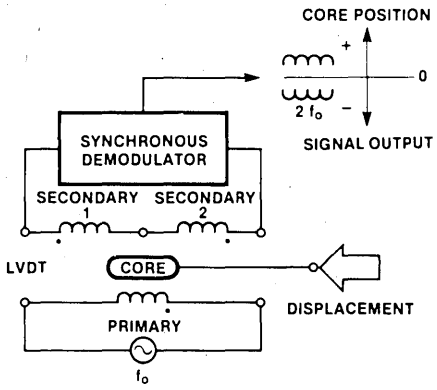


Figure 1

LVDT SYSTEM TRANSFER FUNCTION

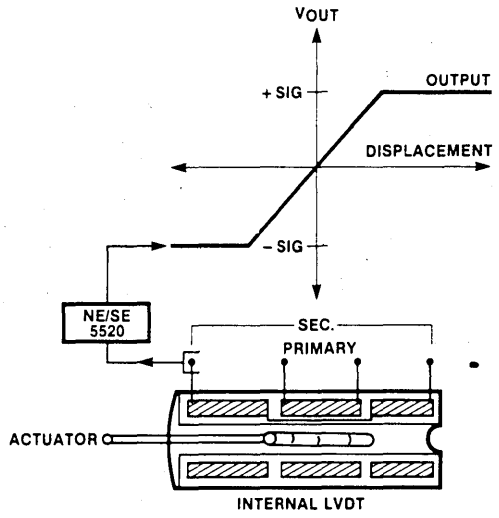


Figure 2

LVDT LOADING

Due to the loosely coupled characteristics of the typical LVDT, loading effects versus frequency may be critical to a successful design. The graph (Figure 3A) shows this relationship in the form of a family of curves relative to LVDT core displacement for 400Hz and 2500Hz. From the curves it is obvious that the linearity and output level versus displacement is superior for an LVDT operated at 2000Hz with a very high impedance load (0.5 meg ohm). The NE/SE5520 demodulator presents a very high input impedance to the LVDT secondary for maximum linearity. (Fig. 3B)

LVDT INTERFACING: SIGNAL CONDITIONING IS REQUIRED

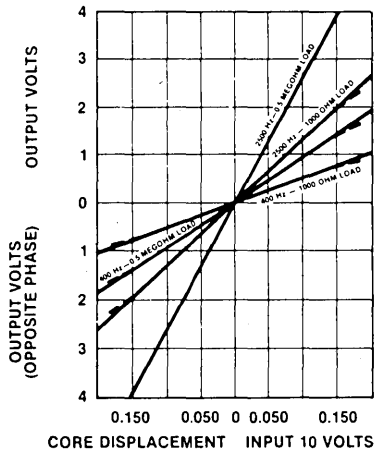
In order to obtain usable information from the LVDT a series of signal conditioning circuit operations are required. First, a stable source of constant frequency excitation voltage must be applied to the primary of the LVDT.

Next some form of demodulator is needed to extract position information from the LVDT secondary output signal. A full wave rectifier will provide usable amplitude information when adequately filtered, however, relative phase information is lacking. In order to obtain both phase and amplitude information synchronous demodulation is needed. This type of demodulator

LVDT SIGNAL CONDITIONER NE/SE5520

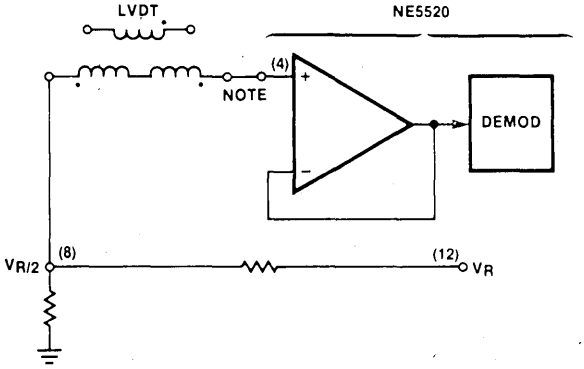
Preliminary

OUTPUT CHARACTERISTICS OF A TYPICAL LVDT FOR VARIOUS LOADS AND EXCITATION FREQUENCIES



BY PERMISSION SCHAEVITZ ENGINEERING
"HANDBOOK OF MEASUREMENT AND CONTROL" BY HERCEG.

Figure 3a



NOTE: INTERNAL BUFFER AMP PROVIDES HIGH IMPEDANCE LOAD TO SECONDARY.

Figure 3b

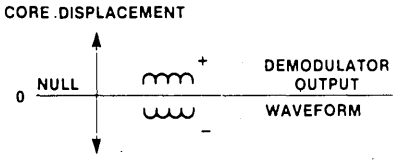


Figure 3c

exists in the Signetics NE5520. Once phase and amplitude information is obtained in the form of a polar full wave rectified signal (see Figure 3C) from the synchronous demodulator, the carrier component (actually 2nd harmonic of the carrier plus higher order spectral components) must be filtered out leaving only the true position information. This is accomplished by passing the demodulated signal through a low-pass active filter. An auxiliary operational amplifier is provided for this purpose within the NE5520, in addition to adjustable signal gain for proper full scale output (span adjustment). In addition, DC offsets are nulled by a simple offset adjustment at the auxiliary amplifier. The resulting system is a complete LVDT signal conditioner. Figure 4 shows a block diagram of the NE5520. The device will operate in a single supply range from 5 to 25 volts DC or with split supplies of ± 5 to ± 12 volts DC. A device current, I_{CC}, of 10 milliamperes at an operating voltage of 10 volts is typical.

DESCRIPTION OF THE NE5520 (Figure 4)

The NE5520 oscillator consists of a triangle wave generator, a current source-sink circuit which switches when the capacitor voltage reaches discrete levels at 1/4 and 3/4 V_{REF}. The total swing being $V_{REF/2}$ volts p-p. The triangle wave is fed into a non-linear load which generates a sinusoidal waveform with low distortion. The sine wave output is then buffered by two op amps, the output of which appear on pins 9 and 10 in phase opposition. This then is the excitation signal for the LVDT primary.

The second major functional portion of the NE5520 is the synchronous demodulator and this section performs full wave rectification in phase synchronism (pin 6) with the above oscillator output. In order to extract true position information, the phase relationship of the LVDT secondary must be obtained. This means that as the LVDT core passes through null an abrupt 180° phase change occurs. Once full wave rectification is accomplished, the resulting signal carrier frequency must be removed by filtering. Demodulator output appears on pin 5. This is accomplished by an active filter incorporating the auxiliary op amp (pins 1, 2, 3). The original position information then appears ripple free on pin 1 of the auxiliary amplifier.

LVDT SIGNAL CONDITIONER NE/SE5520

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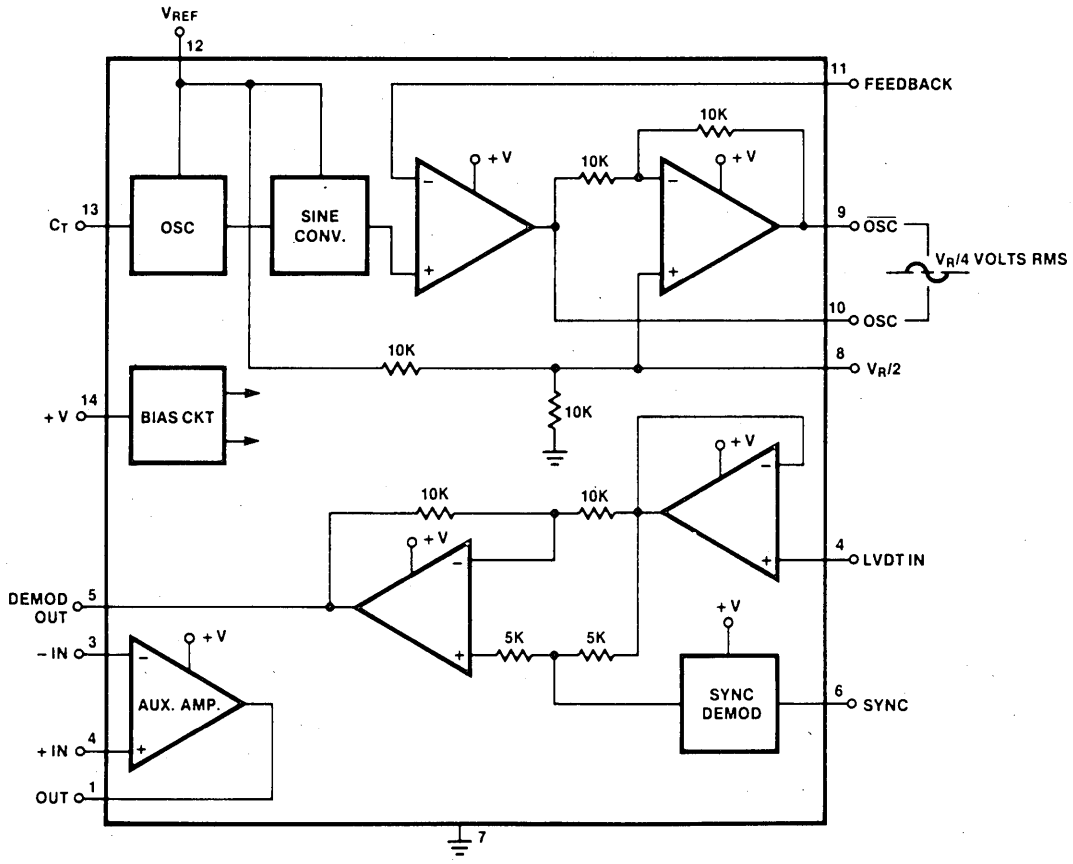
BLOCK DIAGRAM



NOTE:
Pin numbers for for N package.

Figure 4

Other functions include buffer amplifier feedback in the oscillator circuit. The loop is closed with negative feedback around both amplifiers (pin 10 to 11) operating at unity gain.

The oscillator timing capacitor controls the frequency as shown in the graph, Figure 5. The frequency is related by the equation $f_{OSC} = 110/C_{\mu F}$ Absolute output frequency will vary slightly with supply voltage.

OSCILLATOR FREQUENCY vs CAPACITANCE

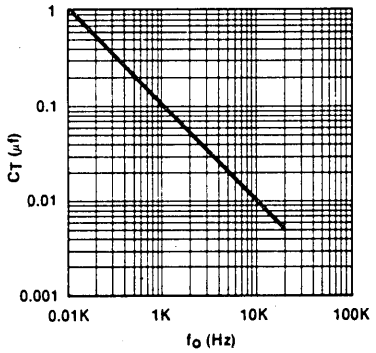


Figure 5

BIASING THE REFERENCE V_{REF} (PIN 12)

The manner in which the V_R pin is biased will effect the output voltage function of the NE5520 and consideration must be given to this in order to arrive at an optimum system design. There are two basic modes of operation involved as listed below:

1) Ratiometric
2) Fixed Reference

With the *ratiometric mode*, pin 12 (V_{REF}) is connected to pin 14 (+V). Since V_R controls the DC common mode voltage of the demodulator and the oscillator rms output, these magnitudes will now change with supply voltage. The DC output from pin 1, using a single ground referenced supply, will be ratiometric with the supply voltage and centered within the common mode range of the output amplifier when the LVDT transducer is at null. Single or dual supply operation will be ratiometric when +V is connected to V_R.

The alternate method of biasing is the *fixed reference* mode with pin 12 (V_R) connected to a fixed reference voltage such as +10 volts and pin 14 (+V) allowed to vary with an incoming poorly regulated supply. This might occur in automotive applications where battery voltage may vary from 10 to 14 volts. However, with a fixed reference driving V_R, DC voltage at the output will not vary with supply but will vary within the common mode limits

LVDT SIGNAL CONDITIONER NE/SE5520

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of the amplifier as the LVDT core traverses its path. Output voltage of pin 1 at LVDT null will be $V_R/2$. Thus, for the case mentioned with $V_R = 10$ volts, the null voltage will be +5 volts. The maximum linear swing would be 1.5-8.5 volts around this value. The fixed reference mode may be used with single or dual supply operation.

DUAL SUPPLY OPERATION

When connected to a typical LVDT transducer as shown in Figure 6, the NE5520 will exhibit an extremely linear transfer function. Very important to precision position measurement is the inherent repeatability of the system. The graphs in Figure 7A, B illustrate the highly linear transfer function and its repeatable accuracy with different supply voltages, in this case ±6 and ±10 volts. The transducer motion was over a range of ±150 milli-inches each side of the LVDT null. Typical DC output signal is shown with an output amplifier gain of X10 in both cases. Note that linearity remains constant, however, full scale output varies with supply voltage. This is due to the increased excitor drive to the LVDT with increased supply voltage. LVDT output is a linear function of excitor amplitude on the primary winding. The addition of a single gain control may easily be added between pins 1 and 3 to reduce gain in order to retain constant output for different supply voltages (see Figure 8) or V_R may be connected to a fixed voltage. (See 'Biasing.')

TRANSFER FUNCTION ±6V

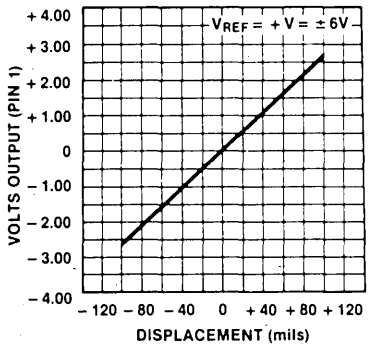

Figure 7a

±10V

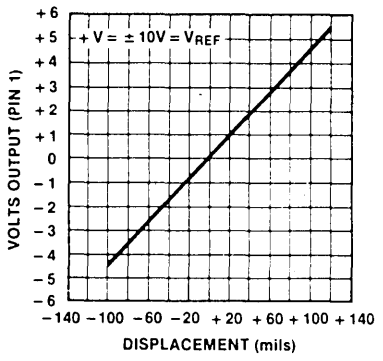

Figure 7b

TYPICAL GAIN ADJUST CIRCUIT

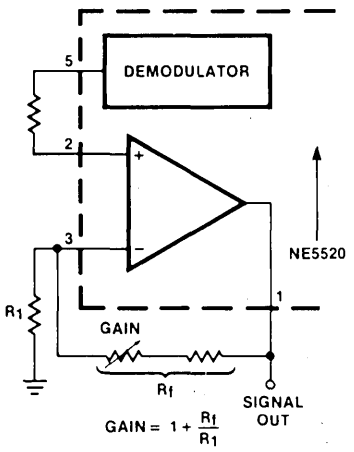

Figure 8

It is strongly recommended that dual output tracking regulated supplies be used in this type of application in order to minimize system DC offset and impaired measurement accuracy due to power supply unbalance. An optional circuit capable of automatically tracking and nulling power supply offset is shown in Figure 9. The bipolar output signal is referenced to ground.

TYPICAL MEASURING SYSTEM
(RATIOMETRIC MODE)

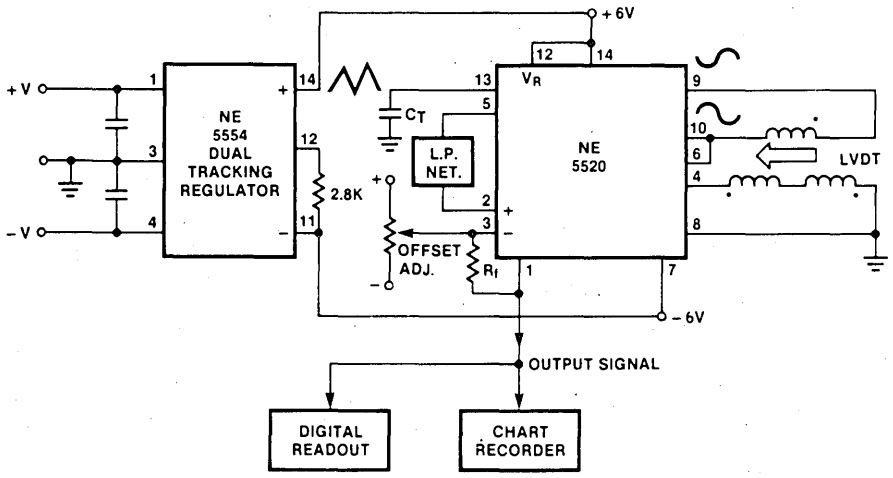

Figure 6

LVDT SIGNAL CONDITIONER NE/SE5520

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AUTO PSRR FOR USE WITH NON-TRACKING SUPPLIES

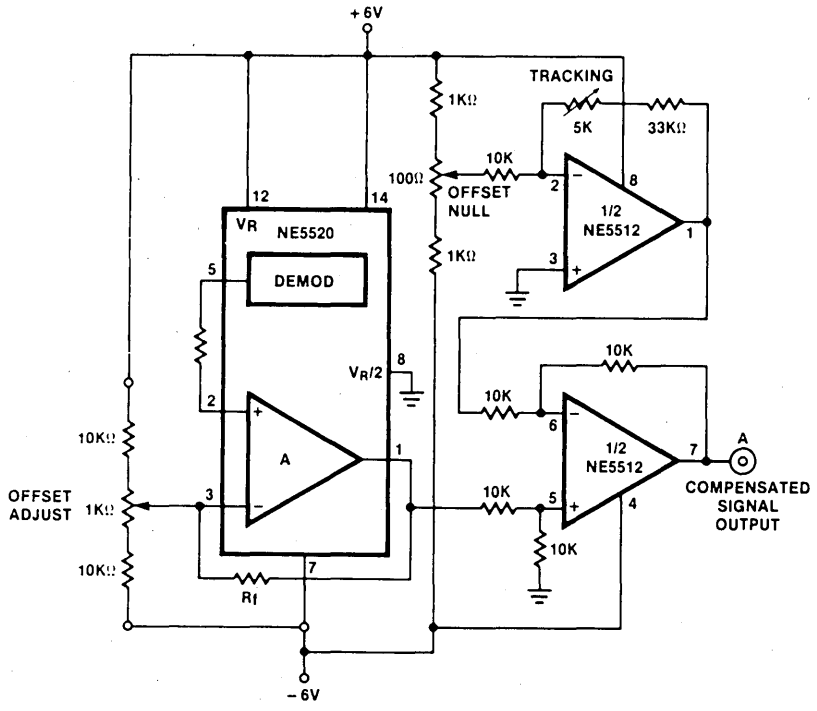

Figure 9

NULLING PROCEDURE (Ref Fig. 9)

1. Null transducer position by observing pin 4 waveform. Set supply voltage for ± 6.00 volts.
2. Set offset adjust pot (feeds pin 3 of NE5520) for 0.00 volts and DC at pin 1 of NE5520.
3. Adjust offset null pot (NE5512) for zero output on Terminal A.
4. Check for equal voltage ± deflection when transducer is displaced equal distances from physical null position.
5. Adjust tracking control for minimum DC output change when either supply is varied over operating range at 'A'.

SINGLE SUPPLY OPERATION

Single ended supply operation requires a different circuit approach to obtain measurement system interface. Figure 10 shows a typical circuit using a single 10-volt supply. Note that the output (pin 1) of the NE5520 is now floating above ground at approximately $V_R/2$. Simple measuring circuits may be realized (Figures 11A, B, C) by placing a DC microammeter between pin 1 and a resistive divider

TYPICAL SINGLE SUPPLY LVDT CIRCUIT

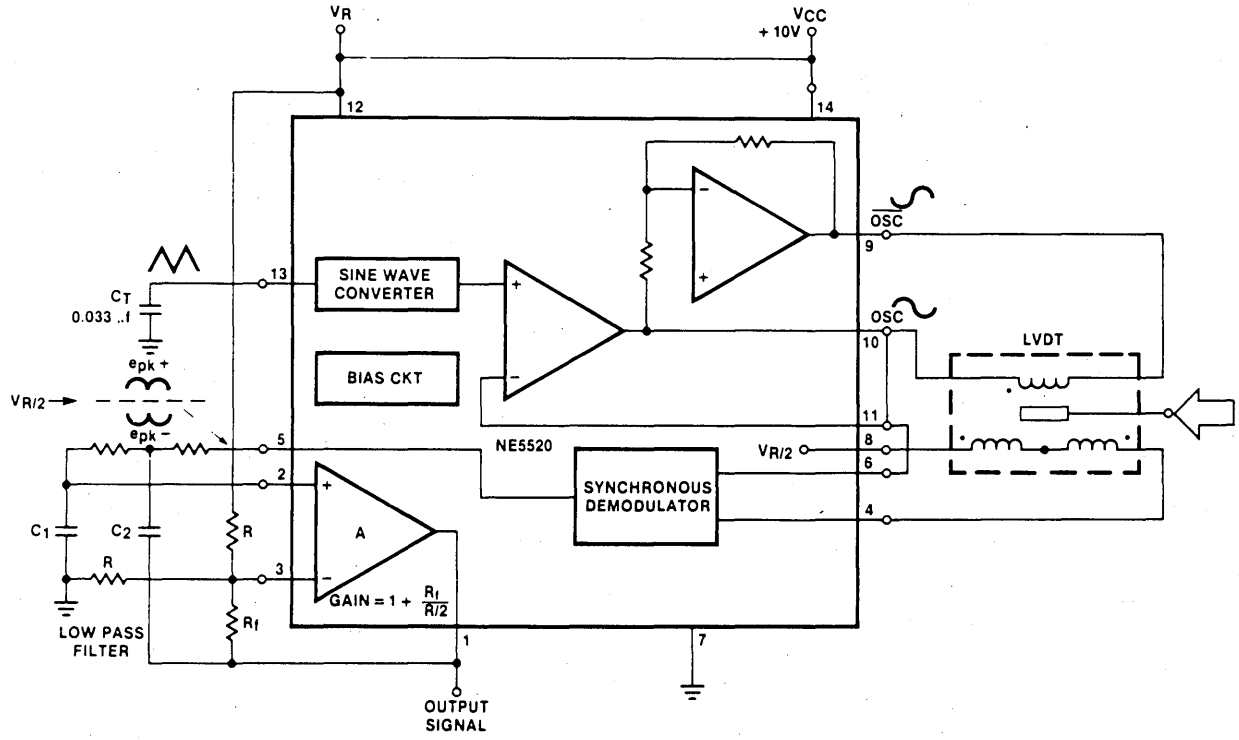

Figure 10

LVDT SIGNAL CONDITIONER NE/SE5520

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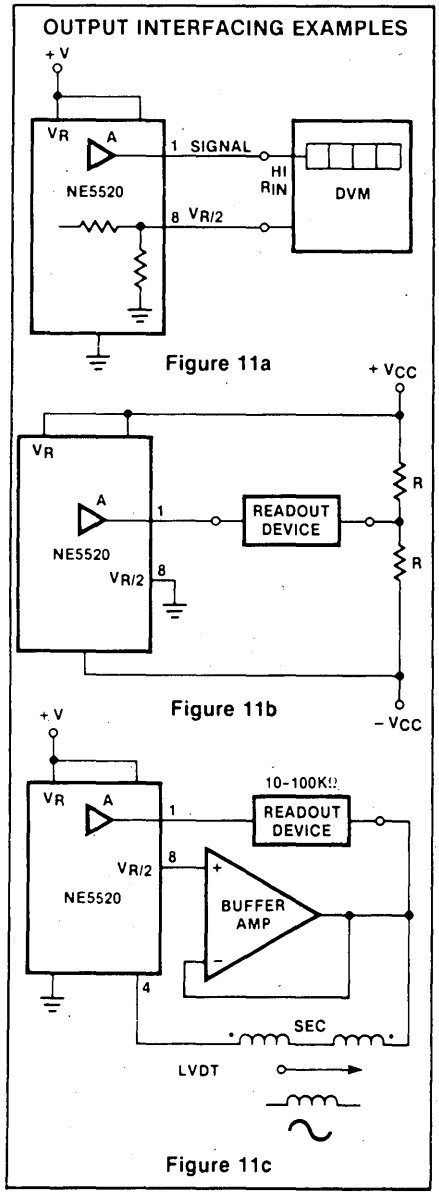
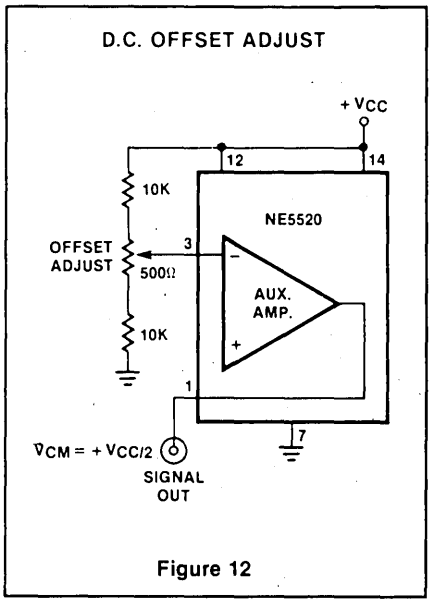
creating a bridge readout which is ratiometric with supply voltage variations. In case more precision is necessary, a buffer amplifier may be added between the voltage divider or $V_R/2$ and the readout circuit in order to minimize offset due to measuring circuit loading. DC offset due to internal tracking error in the NE5520 may be reduced by using the nulling circuit shown in Figure 12. Offset sensitivity and its effect on system accuracy will be inversely proportional to full scale signal output of the NE5520 which is a function of the DC gain of the auxiliary amplifier and LVDT output. A typical full scale output with 10-volt supply operation is $V_R/2 \pm 3.5$ volts with gain equal to 10.





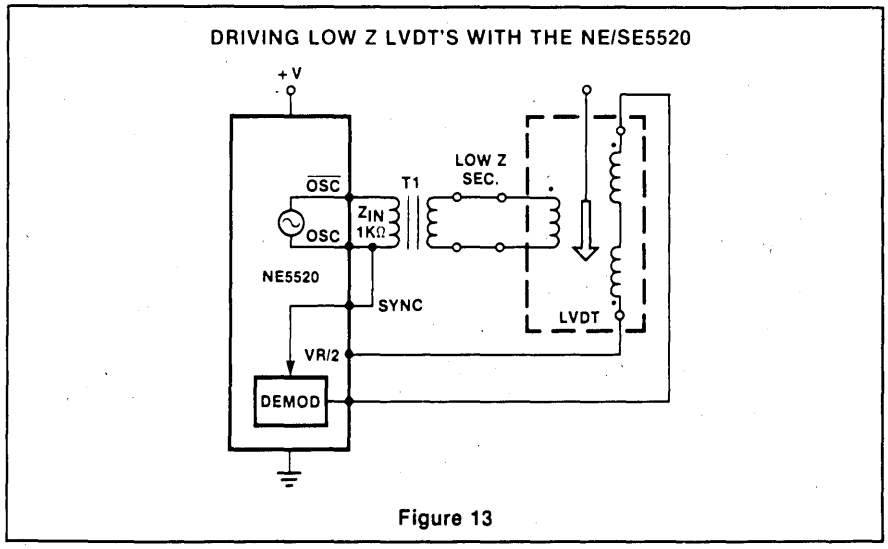
MATCHING THE NE/SE5520 TO LOW IMPEDANCE LVDT's

The NE5520 exciter output is capable of driving LVDT primary windings with a minimum impedance of 1K ohm. When a significantly lower impedance primary is driven by the device some form of step-down impedance matching or a power buffer is recommended. Figure 13 shows a step-down matching transformer approach. A transformer with primary impedance of approximately 1K ohm (audio type) with the proper secondary impedance to match the LVDT primary is used to couple oscillator excitation. Depending on the output efficiency of the LVDT, output signal losses may occur with a corresponding loss in measuring sensitivity. The auxiliary amplifier gain may be increased to offset this loss.

A second approach makes use of a power buffer amplifier constructed from discrete transistors (2N2222, 2N3644). This circuit (Figure 14) results in less signal loss and is inexpensive. A DC decoupling capacitor must be used to prevent DC offset currents from flowing in the LVDT primary winding. A 3dB signal reduction is noted when driving a 15-ohm load to 6 volts peak to peak (10-volt operation); and 12 volts peak to peak for 20-volt supply.

NE5520 TEMPERATURE COMPENSATION

Internal offset voltages originating in the NE5520 synchronous demodulator require external compensation to obtain best measurement accuracy when operating over the full temperature range. The circuits shown (Figures 15A, B) give a simple approach using a thermistor inserted in series with the offset null resistors to reduce voltage drift to a reasonable level. These tolerances are based on ± 3.5 volts full scale output for LVDT displacements each side of physical null. A thermistor having a positive coefficient of +0.7%/°C is used. Obviously, if the total divider resistance is changed a different thermistor resistance will be required.



LVDT SIGNAL CONDITIONER NE/SE5520

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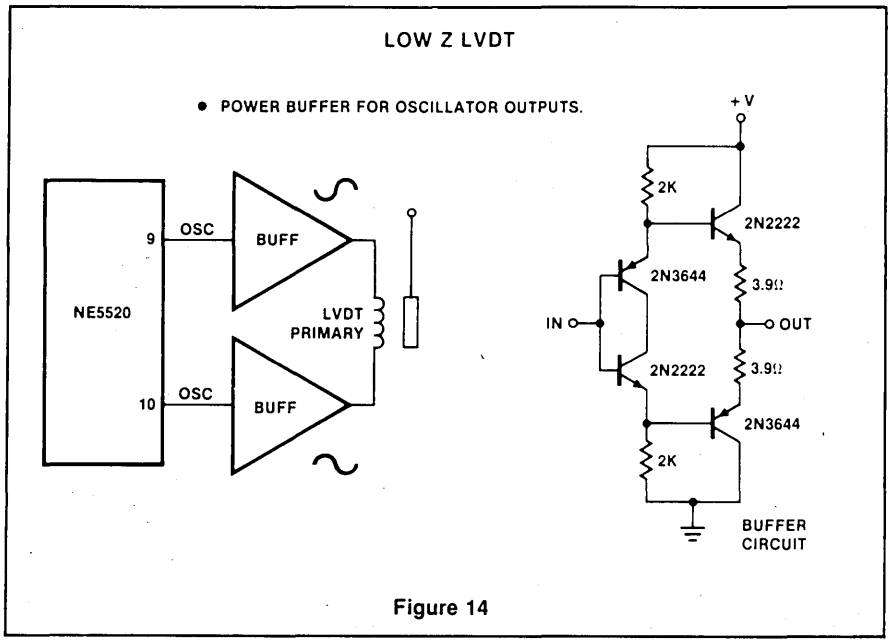

Figure 14

DEMODULATOR DISTORTION (OVERDRIVE)

When the demodulator input exceeds 2 volts peak to peak clipping distortion will increase and must be avoided by controlling oscillator drive to the primary of the LVDT. Figure 16 shows an example of a circuit for attenuating primary excitation using a 1K ohm potentiometer.

The procedure for adjusting the level is simply to:

1. Set LVDT core position for maximum output from the secondary.
2. Monitor the waveform on (pin 5 demodulator output) and adjust oscillator level for the amplitude just below clipping. Normally this should result in a maximum of 2 volts peak to peak at pin 4 of the NE5520 (25°C).

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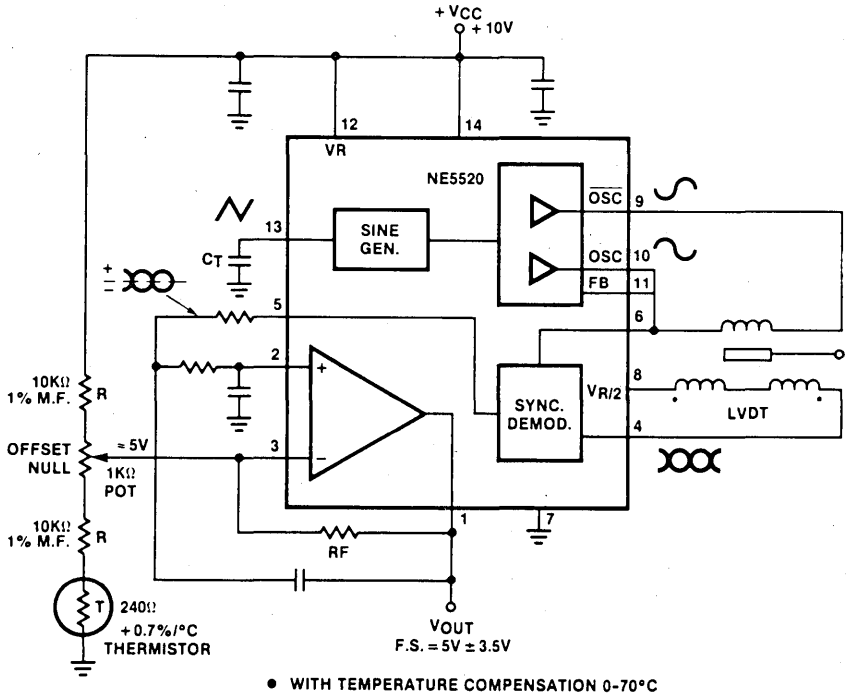
LVDT DRIVER DEMODULATOR



• WITH TEMPERATURE COMPENSATION 0-70°C

Figure 15a

THERMISTOR TEMPERATURE COMPENSATION

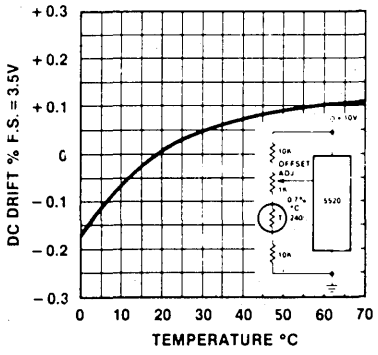


Figure 15b.

LVDT SIGNAL CONDITIONER NE/SE5520

Preliminary

LVDT SECONDARY PHASE ANGLE COMPENSATION BY EXCITATION FREQUENCY

The LVDT has a frequency dependent phase shift associated with the particular characteristics of the device and its excitation frequency. This phase shift is in addition to the 180° shift which occurs when passing through null position.

By adjusting the frequency of the sine wave excitation a condition results which causes secondary voltage to be in phase with primary excitation. The adjustment of relative primary and secondary phase angles has several effects. First, if the primary excitation is referenced to the synchronous demodulator, as in the NE5520, optimum rectification occurs at zero phase differential between secondary AC phase and demodulator switching relative to the waveform zero crossings. Second, "Exciting an LVDT at its zero phase angle frequency results in minimum sensitivity to frequency and temperature variations" (Schaevitz Handbook of Measurement and Control, 1976).

DEMODULATOR SYNC PHASE

A second method of phase compensation of the NE5520 versus the LVDT is to use a variable phase shift network between the *oscillator* output and the *sync* input to the NE5520. This is shown in Figure 17. The oscillator frequency remains fixed and the pot is tuned for optimum demodulator phasing.

It is emphasized that an external phasing adjustment as outlined above is not always necessary. Some LVDT's operating in the 1-5kHz range will be near zero phase and will need no phase compensation. Experimental evaluation of the prototype design combined with system specifications will be the best means of making this decision.

Waveform photo in Figure 18A-B, shows the demodulator output signal when phasing of the synchronous demodulator is correct (A) and improperly adjusted (B).

Proper phasing of the sync signal to the demodulator results in optimum sensitivity and linearity.

LIMITING LVDT EXCITATION TO PREVENT DEMODULATOR DISTORTION

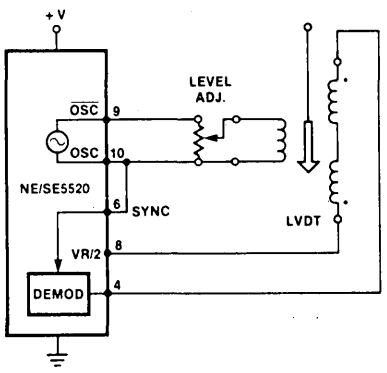


Figure 16

EXTERNAL PHASE ADJUSTMENT

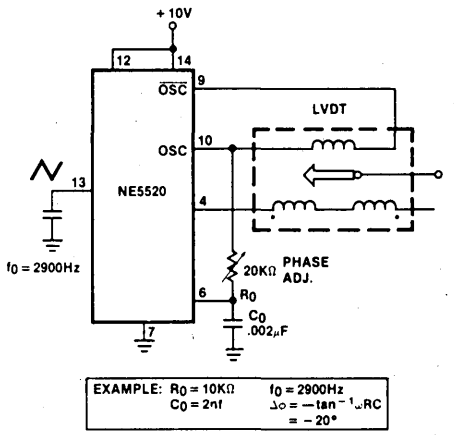


Figure 17

NE/SE5520 DEMODULATOR PHASING

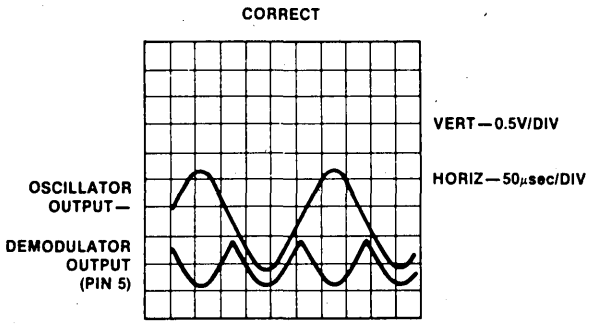


Figure 18a

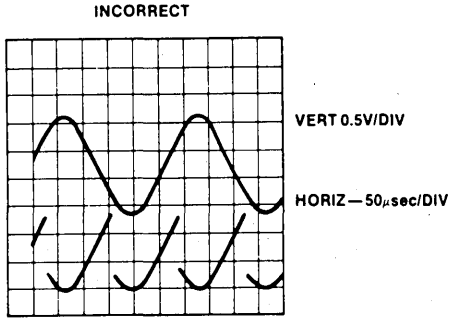


Figure 18b

12-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER Am6012

Preliminary

DESCRIPTION

The Am6012 12-Bit multiplying Digital-to-Analog converter provides high speed and 0.025% differential nonlinearity over its full commercial temperature range.

The D/A converter uses a 3-bit segment generator for the MSBs in conjunction with a 9-bit R-2R diffused resistor ladder to provide 12-bit resolution without costly trimming processes. This technique guarantees a very uniform step size (up to ± ½ LSB from the ideal), monotonicity to 12 bits and integral nonlinearity to 0.05% at its differential current outputs.

The dual complementary outputs of the Am6012 increase its versatility, and effectively double the peak-to-peak output swing. Digital inputs, in addition, can be configured to accept all popular logic families.

While the device requires a reference input of 1mA for a 4mA full scale current, operation is nearly independent of power supply voltage shifts. The power supply rejection ratio is ±0.001%FS/% ΔV. The devices will work from +5, −12V to ±18V rails, with as low as 230mW power consumption typical.

FEATURES

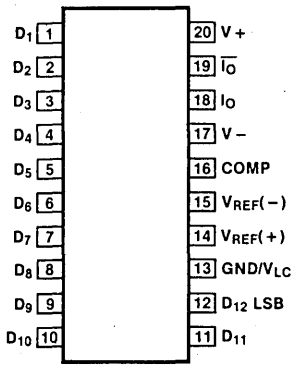
- 12-bit resolution
- Accurate to within ±0.025%
- Monotonic over temperature
- Fast settling time, 250ns typical
- Trimless design for low cost
- Differential current outputs
- High-speed multiplying capability
- Full scale current, 4mA (with 1mA reference)
- High output compliance voltage, −5 to +10V
- Low power consumption, 230mW

APPLICATIONS

- CRT displays, computer graphics
- Robotics, and machine tools
- Automatic test equipment
- Programmable power supplies
- CAD/CAM systems
- Data acquisition and control systems
- Analog-to-Digital converter systems

PIN CONFIGURATION

F PACKAGE



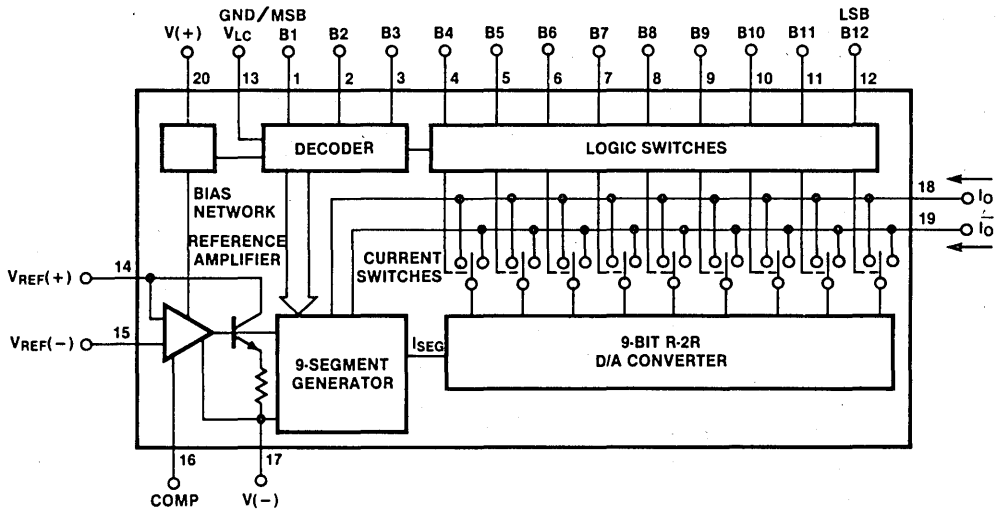
TOP VIEW

ORDER NUMBER
AM6012F

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	
Am6012F	0°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C
Power Supply Voltage	±18V
Logic Inputs	−5V to +18V
Voltage Across Current Outputs	−8V to +12V
Reference Inputs V_{14}, V_{15}	V− to V+
Reference Input Differential Voltage (V_{14} to V_{15})	±18V
Reference Input Current (I_{14})	1.25mA

BLOCK DIAGRAM



LINEAR

Signetics

12-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER Am6012

Preliminary

ELECTRICAL CHARACTERISTICS: $V+ = +15V$, $V- = -15V$, $I_{REF} = 1.0mA$, $0°C \leq T_A \leq 70°C$

Parameter	Description	Test Conditions	Am6012F			Units
			Min.	Typ.	Max.	
	Resolution		12			Bits
	Monotonicity		12			Bits
D.N.L.	Differential Nonlinearity	Deviation from ideal step size	—	—	±.025	%FS
			12	—	—	Bits
N.L.	Nonlinearity	Deviation from ideal straight line	—	—	±.05	%FS
I_{FS}	Full Scale Current	$V_{REF} = 10.000V$ $R_{14} - R_{15} = 10.000k\Omega$ $T_A = 25°C$	3.935	3.999	4.063	mA
TCI_{FS}	Full Scale Tempco		—	±10	±40	ppm/°C
				±.001	±.004	%FS/°C
V_{OC}	Output Voltage Compliance	D.N.L. Specification guaranteed over compliance range R_{OUT} > 10 megohms typ.	−5	—	+10	Volts
I_{FSS}	Symmetry	$I_{FS} - I_{\overline{FS}}$	—	±0.4	±2.0	μA
I_{ZS}	Zero Scale Current		—	—	0.10	μA
t_S	Settling Time	To ±1/2 LSB, all bits ON or OFF, $T_A = 25°C$	—	250	500	nsec
t_{PLH} t_{PHL}	Propagation Delay — all bits	50% to 50%	—	25	50	nsec
C_{OUT}	Output Capacitance		—	20	—	pF
V_{IL}	Logic Input Levels — Logic "0"		—	—	0.8	Volts
V_{IH}	Logic Input Levels — Logic "1"		2.0	—	—	Volts
I_{IN}	Logic Input Current	$V_{IN} = -5$ to $+18V$	—	—	40	μA
V_{IS}	Logic Input Swing	$V- = -15V$	−5	—	+18	Volts
I_{REF}	Reference Current Range		0.2	1.0	1.1	mA
I_{15}	Reference Bias Current		0	−0.5	−2.0	μA
dI/dt	Reference Input Slew Rate	$R_{14(eq)} = 800\Omega$ $CC = 0pF$	4.0	8.0	—	mA/μs
$PSSI_{FS+}$	Power Supply Sensitivity	$V+ = +13.5V$ to $+16.5V$, $V- = -15V$	—	±0.0005	±.001	%FS/%
$PSSI_{FS-}$		$V- = -13.5V$ to $-16.5V$, $V+ = +15V$	—	±.00025	±.001	
$V+$	Power Supply Range	$V_{OUT} = 0V$	4.5	—	18	Volts
$V-$			−18	—	−10.8	
$I+$	Power Supply Current	$V+ = +5V$, $V- = -15V$	—	5.7	8.5	mA
$I-$			—	−13.7	−18.0	
$I+$		$V+ = +15V$, $V- = -15V$	—	5.7	8.5	
$I-$			—	−13.7	−18.0	
P_D	Power Dissipation	$V+ = +5V$, $V- = -15V$	—	234	312	mW
		$V+ = +15V$, $V- = -15V$	—	291	397	

12-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER Am6012

Preliminary

CIRCUIT DESCRIPTION

The Am6012 is a 12-bit DAC which uses diffused resistors and requires no trimming to guarantee monotonicity over the temperature range. A segmented DAC design guarantees a more uniform step size over the temperature range than is normally available with trimmed 12-bit converters. The converter features differential high compliance current outputs, wide supply range, and a multiplying reference input.

In many converter applications, uniform step size is more important than conformance to an ideal straight line. Many 12-bit converters are used for high resolution rather than high linearity, since few transducers are more linear than ±0.1%. All classic binarily weighted converters require ±1/2 LSB (±.012%) linearity in order to guarantee monotonicity, which requires very tight resistor matching and tracking. The Am6012 uses conventional bipolar processing to achieve high differential linearity and monotonicity without requiring correspondingly high linearity, or conformance to an ideal straight line.

One design approach which provides monotonicity without requiring high linearity is the MOS switch-resistor string. This circuit is actually a full complement to a current switched R-2R DAC since it is slower, has a voltage output, and if implemented at the 12-bit level would use 4096 low tolerance resistors rather than a minimum number of high tolerance resistors as in the R-2R network. Its lack of speed and density for 12 bits are its drawbacks.

With the segmented DAC approach, the 4096 required output levels are composed of 8 groups of 512 steps each. Each step group is generated by a 9-bit DAC, and each of the segment slopes is determined by one of 8 equal current sources. The resistors which determine monotonicity are in the 9-bit DAC. The major carry of the 9-bit DAC is repeated in each of the 8 segments, and requires eight times lower initial resistor accuracy and tracking to maintain a given differential nonlinearity over temperature.

The operation of the segmented DAC may be visualized by assuming an input code of all zeroes. The first segment current I_O is divided into 512 levels by the 9-bit multiplying DAC and fed to the output, I_{OUT}. As the input code increases, a new segment current is selected for each 512 counts. The previous segment is fed to output I_{OUT} where the new step group is added to it, thus ensuring monotonicity independent of segment resistor values. All higher order segments feed $\overline{I_{OUT}}$.

With the segmented DAC approach, the precision of the 8 main resistors determines linearity only. The influence of each of these resistors on linearity is four times lower than that of the MSB resistor in an R-2R DAC. Hence, assuming the same resistor tolerances for both, the linearity of the segmented approach would actually be higher than that of an R-2R design.

The step generator or 9-bit DAC is composed of a master and a slave ladder. The slave ladder generates the four least significant bits from the remainder of the master ladder by active current splitting utilizing scaled emitters. This saves ladder resistors and greatly reduces the range of emitter scaling required in the 9-bit DAC. All current switches in the step generator are high speed fully differential switches which are capable of switching low currents at high speed. This allows the use of a binary scaled network all the way to the least significant bit which saves power and simplifies the circuitry.

Diffused resistors have advantages over thin film resistors beyond simple economy and bipolar process compatibility. The resistors are fabricated in single crystal rather than amorphous material which gives them better long term stability and tracking and much higher moisture resistance. They are diffused at 1000°C and so are resistant to changes in value due to thermal and chemical causes. Also, no burn-in is required for stability. The contact resistance between aluminum and silicon is more predictable than between aluminum and an amorphous thin film, and no sandwich metals are required to enhance or protect the contact or limit alloying. The initial match between two diffused resistors is similar to that of thin film since both are defined by photomasks and chemical etching. Since the resistors are not trimmed or altered after fabrication, their tracking and long term characteristics are not degraded.

DIFFERENTIAL vs INTEGRAL NONLINEARITY

Integral nonlinearity, for the purposes of the discussion, refers to the "straightness" of the line drawn through the individual response points of a data converter. Differential nonlinearity, on the other hand, refers to the deviation of the spacing of the adjacent points from a 1 LSB ideal spacing. Both may be expressed as either a percentage of full scale output or as fractional LSBs or both. The graphs in Figure 1 define the manner in which these parameters are specified. The left graph shows a portion of the transfer curve of a DAC with 1/2 LSB INL and the (implied) DNL spec of 1LSB. Below this is a graphic representation of the way this would appear on a CRT screen where the Am6012 is used as a display driver. On the right is a portion of the transfer curve of a DAC specified for 2LSB INL with 1/2 LSB DNL specified and the graphic display below it.

One of the characteristics of an R-2R DAC in standard form is that any transition which causes a zero LSB change (i.e. the same output for two different codes) will exhibit the same output each time that transition occurs. The same holds true for transitions causing a 2LSB change. These two problem transitions are allowable for the standard definition of monotonicity and also allow the device to be specified very tightly for INL. The major problem arising from this error type is in A/D converter implementations. Inputs producing the same output are now represented by ambiguous output codes for an identical input. Also, 2LSB gaps can cause large errors at those input levels (assuming 1/2 LSB quantizing levels). It can be seen from the two figures that the DNL specified D/A converter will yield much finer grained data than the INL specified part, thus improving the ability of the A/D to resolve changes in the analog input.

ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided where $I_O + \overline{I_O} = I_{FR}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at pin 18 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 18 and turned on at pin 19. A decreasing logic count increases $\overline{I_O}$ as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FR}; do not leave an unused output pin open.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 25V above V− and is independent of the positive supply. Negative compliance is +10V above V−.

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DIFFERENTIAL LINEARITY COMPARISON

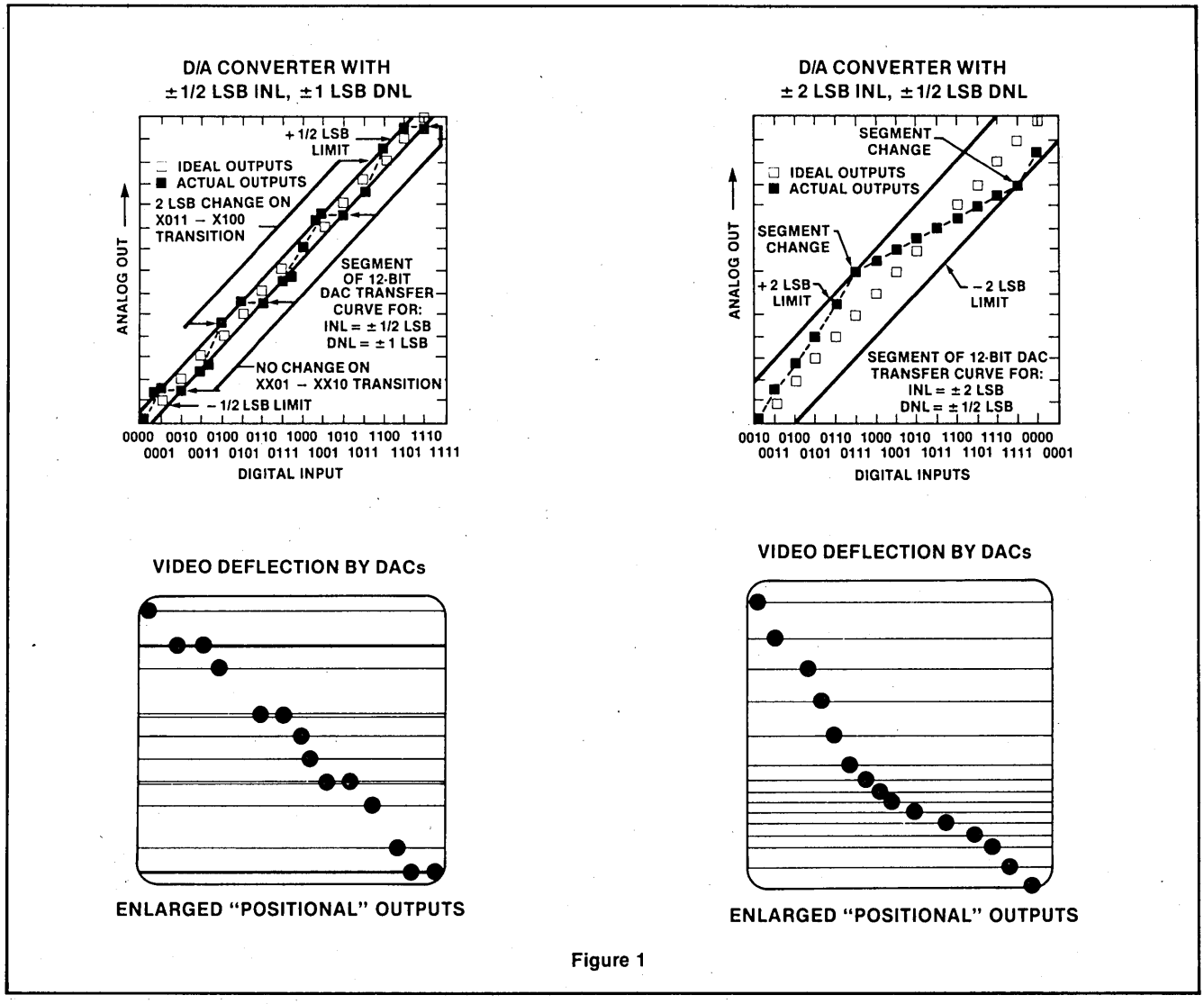

Figure 1

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

POWER SUPPLIES

The Am6012 operates over a wide range of power supply voltages from a total supply of 20V to 36V. When operating with V– supplies of –10V or less, $I_{REF} \leq 1mA$ is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at –9V with $I_{REF} = 1mA$ is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the Am6012 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required; however, an artificial ground may be used to insure logic swings, etc. remain between acceptable limits.

TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specifications of the Am6012 are guaranteed to apply over the entire rated operating temperature range. Full scale output current drift is tight, typically ±10ppm/°C, with zero scale output current and drift essentially negligible compared to 1/2 LSB.

The temperature coefficient of the reference resistor R14 should match and track that of the output resistor for minimum overall full scale drift.

SETTLING TIME

The Am6012 is capable of extremely fast settling times, typically 250ns at

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I_{REF} = 1.0mA. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 25ns for each of the 12 bits. Settling time to within 1/2 LSB of the LSB is therefore 25ns, with each progressively larger bit taking successively longer. The MSB settles in 250ns, thus determining the overall settling time of 250ns. Settling to 10-bit accuracy requires about 90 to 130ns. The output capacitance of the Am6012 including the package is approximately 20pF; therefore, the output RC time constant dominates settling time if R_L > 500Ω.

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 0.5mA, with gradual increases for lower I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of settling time requires the ability to accurately resolve ± 2μA, therefore a 2.5kΩ load is needed to provide adequate drive for most oscilloscopes. At I_{REF} values of less than 0.5mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 011111111111 to 100000000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within ± 0.1% of the final value, and thus settling times may be observed at lower values of I_{REF}.

Am6012 switching transients or "glitches" are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference, and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; 0.1μF capacitors at the supply pins provide full transient protection.

APPLICATIONS INFORMATION

REFERENCE AMPLIFIER SETUP

The Am6012 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to + 1.0mA. The full range output current is a linear function of the reference current and is given by:

$$I_{FR} = \frac{4095}{4096} \times 4 \times (I_{REF}) = 3.999\ I_{REF},$$

where $I_{REF} = I_{14}$

In positive reference applications, an external positive reference voltage forces current through R14 into the $V_{REF(+)}$ terminal (pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$ at pin 15. Reference current flows from ground through R14 into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 15. The voltage at pin 14 is equal to and tracks the voltage at pin 15 due to the high gain of the internal reference amplifier. R15 (nominally equal to R14) is used to cancel bias current errors. (Figure 2a)

Bipolar references may be accommodated by offsetting V_{REF} or pin 15. The negative common-mode range of the reference amplifier is given by: $V_{CM-} = V-$ plus ($I_{REF} \times 3k\Omega$) plus 1.8V. The positive common-mode range is V+ less 1.23V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R14 should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.

For most applications the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full scale trimming may be accomplished by adjusting the value of R14, or by using a potentiometer for R14. An improved method of full scale trimming which eliminates potentiometer T.C. effects in the Recommended Full Scale Adjustment circuit.

MULTIPLYING OPERATION

The Am6012 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 1mA to 1μA. Monotonic operation is maintained over a typical range of I_{REF} from 100μA to 1.0mA.

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to V−. The value of this capacitor depends on the impedance presented to pin 14. For R14 values of 1.0, 2.5 and 5.0kΩ; minimum values of C_C are 5, 10, and 25pF. Larger values of R14 require proportionately increased values of C_C for proper phase margin. (See Figure 2b).

For fastest response to a pulse, low values of R14 enabling small C_C values should be used. If pin 14 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R14 = 1kΩ and C_C = 5pF, the reference amplifier slews at 4mA/ms enabling a transition from I_{REF} = 0 to I_{REF} = 1mA in 250ns.

Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme. This technique provides lowest full scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff (I_{REF} = 0) condition. Full scale transition (0 to 1mA) occurs in 62.5ns when the equivalent impedance at pin 14 is 800Ω and C_C = 0. This yields a reference slew rate of 8mA/μs which is relatively independent of R_{IN} and V_{IN} values.

LOGIC INPUTS

The Am6012 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 40μA logic input current, and completely adjustable logic threshold voltage. For V− = − 15V, the logic inputs may swing between − 5 and + 10V. This enables direct interface with + 15V CMOS logic, even when the Am6012 is powered from a + 5V supply. Minimum input logic swing and minimum logic threshold voltage are given by: V− plus ($I_{REF} \times 3k\Omega$) plus 1.8V. The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (pin 13, V_{LC}). For TTL interface, simply ground pin 13. When interfacing ECL, an $I_{REF} \leq$ 1mA is recommended.

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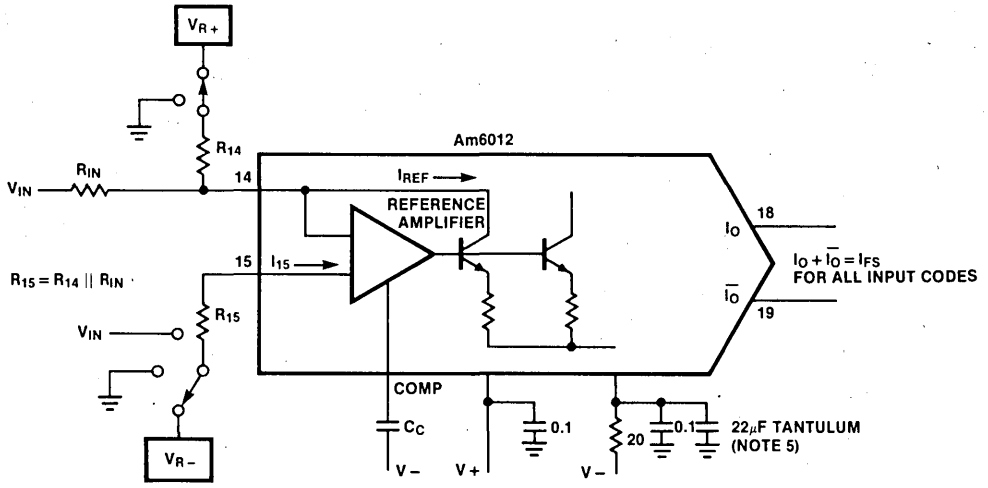
REFERENCE AMPLIFIER BIASING



Reference Configuration	R_{14}	R_{15}	R_{IN}	C_C	I_{REF}
Positive Reference	V_{R+}	0V	N/C	.01μF	V_{R+}/R_{14}
Negative Reference	0V	V_{R-}	N/C	.01μF	$-V_{R-}/R_{14}$
Lo Impedance Bipolar Reference	V_{R+}	0V	V_{IN}	(Note 1)	$(V_{R+}/R_{14}) + (V_{IN}/R_{IN})$ (Note 2)
Hi Impedance Bipolar Reference	V_{R+}	V_{IN}	N/C	(Note 1)	$(V_{R+} - V_{IN})/R_{14}$ (Note 3)
Pulsed Reference (Note 4)	V_{R+}	0V	V_{IN}	No Cap	$(V_{R+}/R_{14}) + (V_{IN}/R_{IN})$

Notes:
1. The compensation capacitor is a function of the impedance seen at the $+V_{REF}$ input and must be at least $5pF \times R_{14(eq)}$ in kΩ. For $R_{14} < 800\Omega$ no capacitor is necessary.
2. For negative values of V_{IN}, V_{R+}/R_{14} must be greater than $-V_{IN}$ Max/R_{IN} so that the amplifier is not turned off.
3. For positive values of V_{IN}, V_{R+} must be greater than V_{IN} Max so the amplifier is not turned off.
4. For pulsed operation, V_{R+} provides a DC offset and may be set to zero in some cases. The impedance at pin 14 should be 800Ω or less.
5. For optimum settling time, decouple V− with 20Ω and bypass with 22μF tantulum capacitor.
6. Reference current and reference resistor — there is a 1 to 4 scale factor between the reference current (I_{REF}) and the full scale output current (I_{FS}). If $V_{REF} = +10V$ and $I_{FS} = 4mA$, the value of the R_{14} is:

$$R_{14} = \frac{4 \times 10\ Volt}{4mA} = 10k\Omega \qquad R_{14} = R_{15}$$

Figure 2a

MINIMUM SIZE COMPENSATION CAPACITOR ($I_{FS} = 4mA$, $I_{REF} = 1.0mA$)

$R_{14(EQ)}(k\Omega)$	C_C (pF)
10	50
5	25
2	10
1	5
.5	0

Note: A 0.01μF capacitor is recommended for fixed reference operation.

REFERENCE AMPLIFIER FREQUENCY RESPONSE

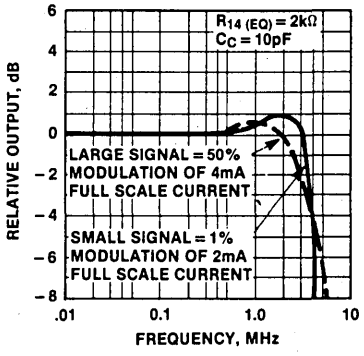


Figure 2b

12-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER Am6012

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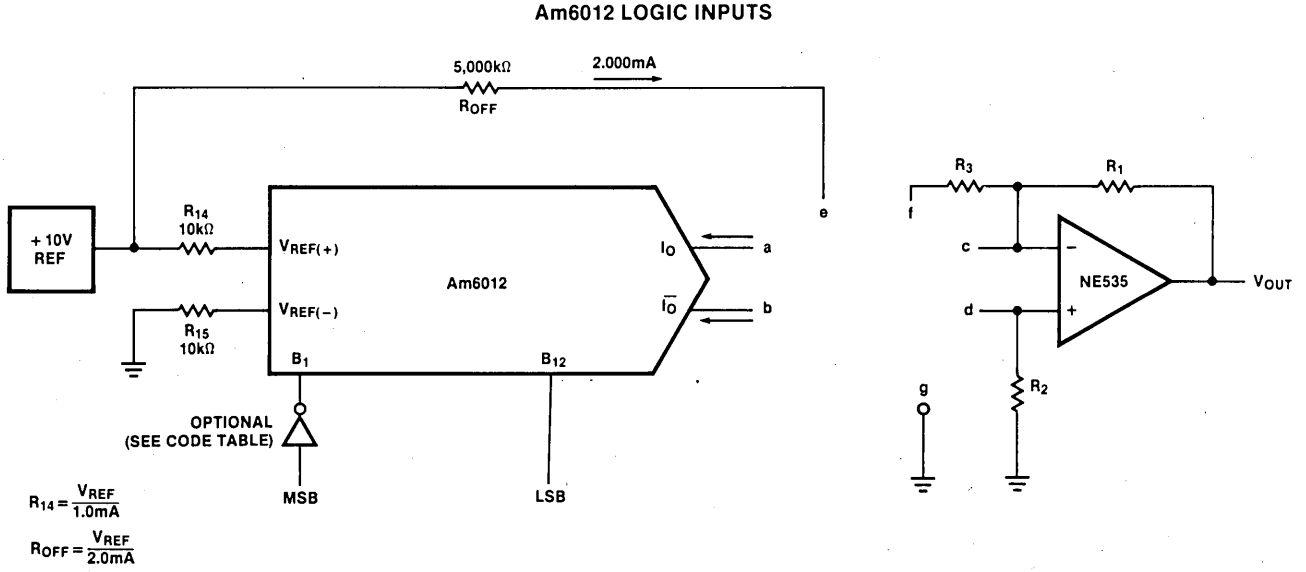
APPLICATION CIRCUITS



Code Format		Connections	Output Scale	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	I_0 (mA)	$\overline{I_0}$ (mA)	V_{OUT}
Unipolar	Straight binary; one polarity with true input code, true zero output.	a-c	Positive full scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	9.9976
		b-g	Positive full scale — LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9951
		R1 = R2 = 2.5K	Zero scale	0	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	.0000
	Complementary binary; one polarity with complementary input code, true zero output.	a-g	Positive full scale	0	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	9.9976
		b-c	Positive full scale — LSB	0	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	9.9951
		R1 = R2 = 2.5K	Zero scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	.0000
Symmetrical Offset	Straight offset binary; offset half scale, symmetrical about zero, no true zero output.	a-c	Positive full scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	9.9976
		b-d	Positive full scale — LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9927
		f-g	(+) Zero scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	.0024
		R1 = R3 = 2.5K	(−) Zero scale	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	− .0024
		R2 = 1.25K	Negative full scale — LSB	0	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	− 9.9927
			Negative full scale	0	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	− 9.9976
	1's complement; offset half scale, symmetrical about zero, no true zero output, MSB complemented (need inverter at B1).	a-c	Positive full scale	0	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	9.9976
		b-d	Positive full scale — LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9927
		f-g	(+) Zero scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	.0024
		R1 = R3 = 2.5K	(−) Zero scale	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	− .0024
		R2 = 1.25K	Negative full scale — LSB	1	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	− 9.9927
			Negative full scale	1	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	− 9.9976
Offset with True Zero	Offset binary; offset half scale, true zero output.	e-a-c	Positive full scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	9.9951
		b-g	Positive full scale — LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9902
		R1 = R2 = 5K	+ LSB	1	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	.0049
			Zero Scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	.000
			− LSB	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	− .0049
			Negative full scale + LSB	0	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	− 9.9951
			Negative full scale	0	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	− 10.000
	2's complement; offset half scale, true zero output, MSB complemented (need inverter at B1).	e-a-c	Positive full scale	0	1	1	1	1	1	1	1	1	1	1	1	3.999	.006	9.9951
		b-g	Positive full scale — LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9902
		R1 = R2 = 5K	+ 1 LSB	0	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	.0049
			Zero scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	.000
			− 1 LSB	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	− 0.049
			Negative full scale + LSB	1	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	− 9.9951
			Negative full scale	1	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	− 10.000

Figure 4

ADDITIONAL CODE MODIFICATIONS

1. Any of the offset binary codes may be complemented by reversing the output terminal pair.

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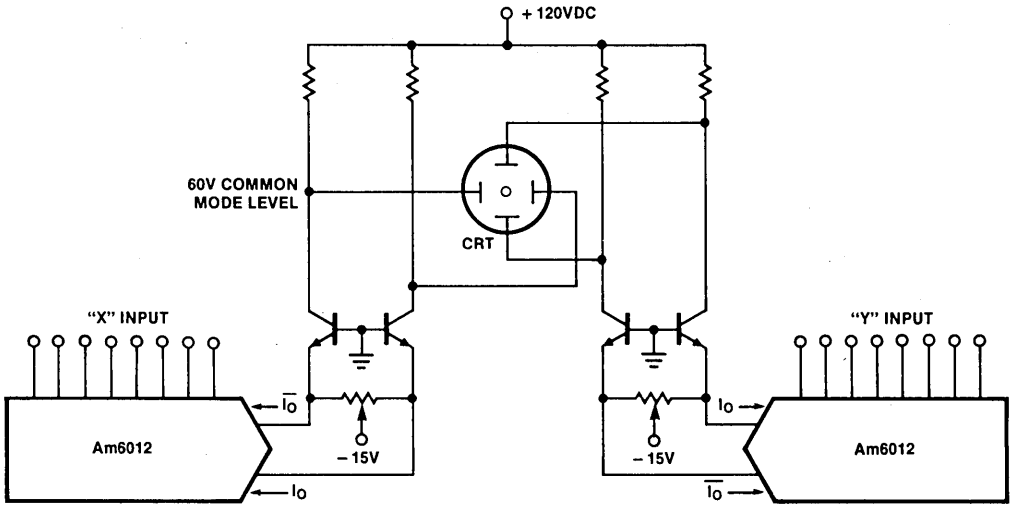
APPLICATION CIRCUITS

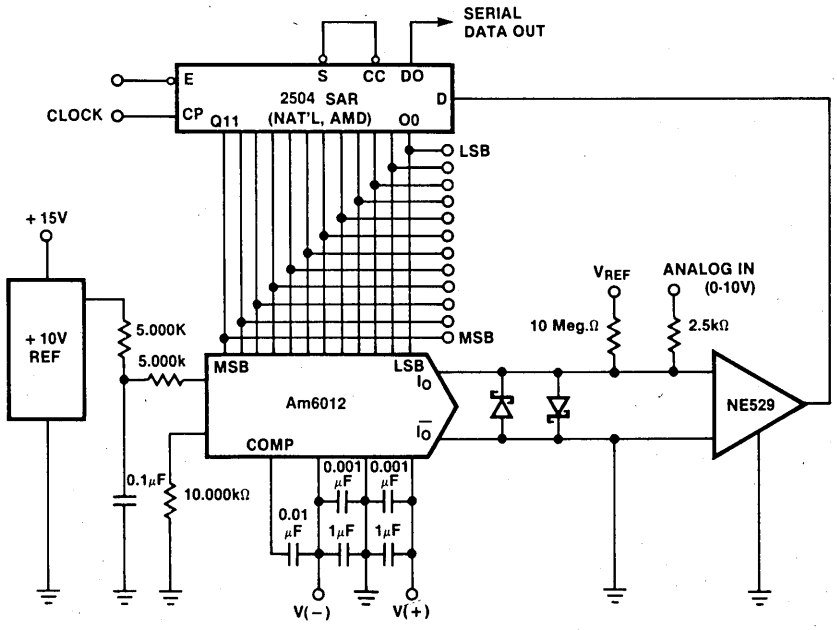
CRT DISPLAY DRIVER

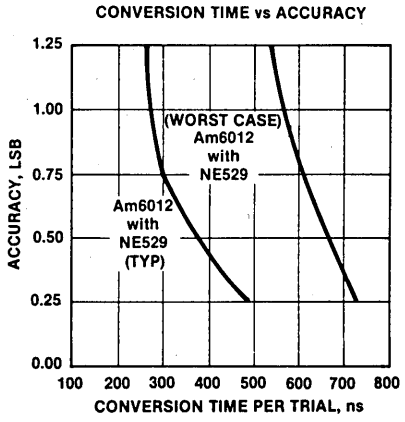


NOTES: 1. FULL DIFFERENTIAL DRIVE LOWERS POWER SUPPLY VOLTAGE.
2. ELIMINATES INVERTING AMPLIFIERS AND TRANSFORMERS.
3. INDEPENDENT BEAM CENTERING CONTROLS.

Figure 5

12-BIT HIGH-SPEED A/D CONVERTER





CONVERSION TIME (ns)	TYP	WORST CASE
SAR	33	55
NE529	100	150
TOTAL	383ns	705ns
× 13	5.0μs	9.1μs

Figure 6

COMPANDOR NE570/571/SA571

DESCRIPTION

The NE570/571 is a versatile low cost dual gain control circuit in which either channel may be used as a dynamic range compressor or expandor. Each channel has a full wave rectifier to detect the average value of the signal; a linerarized, temperature compensated variable gain cell; and an operational amplifier.

The NE570/571 is well suited for use in telephone subscriber and trunk carrier systems, communications systems and hi-fi audio systems.

FEATURES

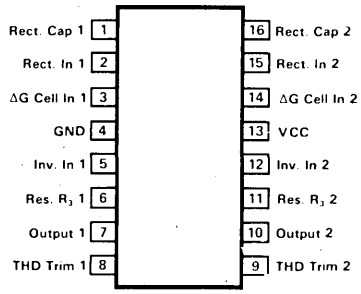
- **Complete compressor and expandor in 1 IC**
- **Temperature compensated**
- **Greater than 110dB dynamic range**
- **Operates down to 6Vdc**
- **System levels adjustable with external components**
- **Distortion may be trimmed out**

APPLICATIONS

- **Telephone trunk compandor—570**
- **Telephone subscriber compandor—571**
- **High level limiter**
- **Low level expandor—noise gate**
- **Dynamic noise reduction systems**
- **Voltage controlled amplifier**
- **Dynamic filters**

PIN CONFIGURATION

F, N PACKAGE



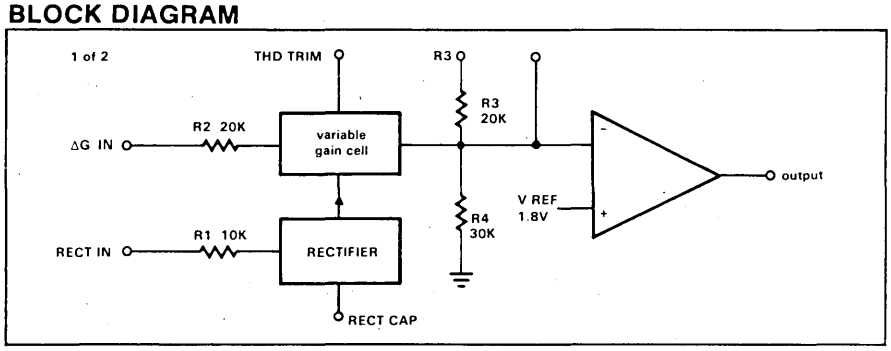
TOP VIEW

ORDER NUMBERS
NE570F,N NE571F,N
SA571F,N

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
	Positive supply		Vdc
	570	24	
	571	18	
T_A	Operating temperature range		
	NE	0 to 70	°C
	SA	-40 to +85	°C
P_D	Power dissipation	400	mW

BLOCK DIAGRAM



CIRCUIT DESCRIPTION

The NE570/571 compandor building blocks, as shown in the block diagram, are a full wave rectifier, a variable gain cell, an operational amplifier and a bias system. The arrangement of these blocks in the IC result in a circuit which can perform well with few external components, yet can be adapted to many diverse applications.

The full wave rectifier rectifies the input current which flows from the rectifier input, to an internal summing node which is biased at V_{REF}. The rectified current is averaged on an external filter capacitor tied to the C_{RECT} terminal, and the average value of the input current controls the gain of the variable gain cell. The gain will thus be proportional to the average value of the input signal for capacitively coupled voltage inputs as shown in the following equation. Note that for capacitively coupled inputs there is no offset voltage capable of producing a gain error. The only error will come from the bias current of the rectifier (supplied internally) which is less than .1μA.

$$G \propto \frac{|V_{IN} - V_{REF}|_{ave}}{R_1}$$

or

$$G \propto \frac{|V_{IN}|_{ave}}{R_1}$$

The speed with which gain changes to follow changes in input signal levels is determined by the rectifier filter capacitor. A small capacitor will yield rapid response but will not fully filter low frequency signals. Any ripple on the gain control signal will modulate the signal passing through the variable gain cell. In an expandor or compressor application, this would lead to third harmonic distortion, so there is a tradeoff to be made between fast attack and decay times, and distortion. For step changes in amplitude, the change in gain with time is shown by this equation.

$$G(t) = (G_{initial} - G_{final})\ e^{-t/\tau} + G_{final};\ \tau = 10K \times C_{RECT}$$

The variable gain cell is a current in, current out device with the ratio I_{OUT}/I_{IN} controlled by the rectifier. I_{IN} is the current which flows from the ΔG input to an internal summing node biased at V_{REF}. The following equation applies for capacitively coupled inputs. The output current, I_{OUT}, is fed to the summing node of the op amp.

$$I_{IN} = \frac{V_{IN} - V_{REF}}{R_2} = \frac{V_{IN}}{R_2}$$

A compensation scheme built into the ΔG cell compensates for temperature, and cancels out odd harmonic distortion. The only distortion which remains is even harmonics, and they exist only because of internal offset voltages. The THD trim terminal provides a means for nulling the internal offsets for low distortion operation.

The operational amplifier (which is internally compensated) has the non-inverting input tied to V_{REF}, and the inverting input connected to the ΔG cell output as well as brought out externally. A resistor, R_3, is brought out from the summing node and allows compressor or expandor gain to be determined only by internal components.

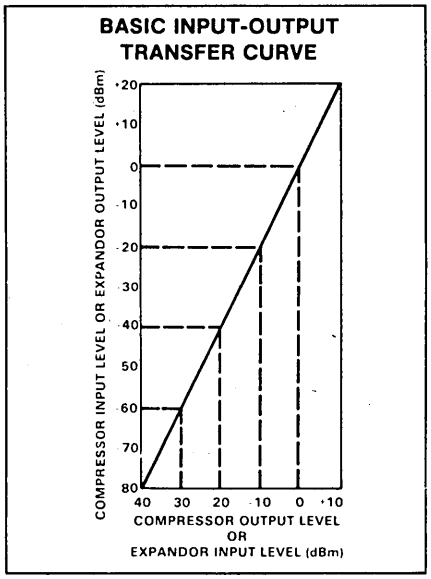
COMPANDOR NE570/571/SA571

The output stage is capable of ±20mA output current. This allows a +13dBm (3.5V rms) output into a 300Ω load which, with a series resistor and proper transformer, can result in +13dBm with a 600Ω output impedance.

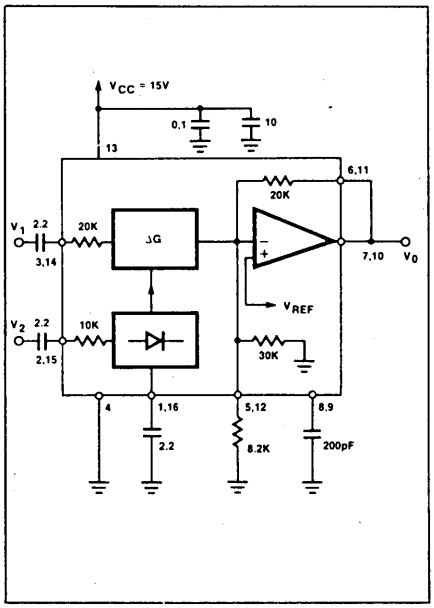
A band gap reference provides the reference voltage for all summing nodes, a regulated supply voltage for the rectifier and ΔG cell, and a bias current for the ΔG cell. The low tempco of this type of reference provides very stable biasing over a wide temperature range.

The typical performance characteristics illustration shows the basic input-output transfer curve for basic compressor or expandor circuits.

TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL TEST CIRCUIT



DC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 15V[1]

PARAMETER	TEST CONDITIONS	NE570			NE/SA571[6]			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{CC} Supply voltage		6		24	6		18	V
I_{CC} Supply current	No signal		3.2	4.0		3.2	4.8	mA
Output current capability		±20						mA
Output slew rate			±.5					V/us
Gain cell distortion[2]	Untrimmed		.3	1.0		.5	2.0	%
	Trimmed		.05			.1		
Resistor tolerance			±5	±15				%
Internal reference voltage		1.7	1.8	1.9	1.65	1.8	1.95	V
Output dc shift[3]	Untrimmed		±20	±50		±30	±100	mV
Expandor output noise	No signal, 20Hz-20kHz		20					μV
			-15					dBRNC
Unity gain level		-1	0	+1	-1.5	0	+1.5	dBm
Gain change[2,4]	-40°C < T < 70°C		±.1			±.1		dB
	0°C < T < 70°C		±.1	±.2		±.1	±.4	
Reference drift[4]	-40°C < T < 70°C		+2, -25	-10, -40		+2, -25	+20, -50	mV
	0°C < T < 70°C		±5	±10		±5	±20	
Resistor drift[4]	-40°C < T < 70°C		+8,-0					%
	0°C < T < 70°C		+1,-0					
Tracking error [5], input	Rectifier input, V_2 =							dB
V_1 = OdBm	+6dBm		±.2					
	-10dBm		+.2	-.2,+.4		+.2	-.2,+.5	
	-20dBm		+.2	-.3,+.6		+.2	-.4,+.7	
	-30dBm		+.2	-.5,+1		+.2	-1,+1.5	
	-40dBm		+.2,-.4			+.2,-.4		

NOTES

1. Except where indicated, the 571 specifications are identical to the 570
2. Measured at OdBm,1kHz
3. Expandor ac input change from no signal to OdBm
4. Relative to value at T_A = 25°C
5. Relative to OdBm
6. Electrical characteristics for the SA571 only are specified over -40 to +85°C temperature range.

DUAL LOW-NOISE PREAMP NE542

DESCRIPTION

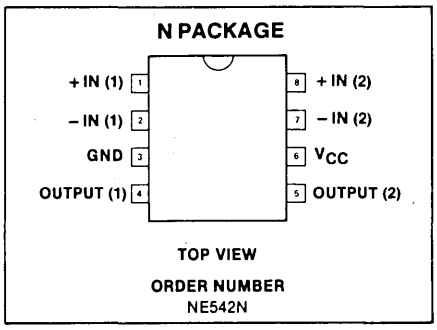
The NE542 is a dual preamplifier for the amplification of low level signals in applications requiring optimum noise performance. Each of the two amplifiers is completely independent, with individual internal power supply decoupler-regulator, providing 110dB supply rejection and 70dB channel separation. Other outstanding features include high gain (104dB), large output voltage swing (V_{CC} – 2Vp-p), and internal compensation to 10dB. The NE542 operates from a single supply across the wide range of 9 to 24V.

The NE542 is ideal for use in stereo phono, tape, or microphone preamps and other applications requiring low noise amplification of small signals.

FEATURES

- **Low noise—.7μV total input noise**
- **High gain—104dB open loop**
- **Single supply operation**
- **Wide supply range 9 to 24V**
- **Power supply rejection 110dB**
- **Large output voltage swing (V_{CC} -2V p-p)**
- **Wide bandwidth 15MHz unity gain**
- **Power bandwidth 100kHz (15V p-p)**
- **Internally compensated (stable at 10dB)**
- **Short circuit protected**
- **High slew rate 5V/μs**

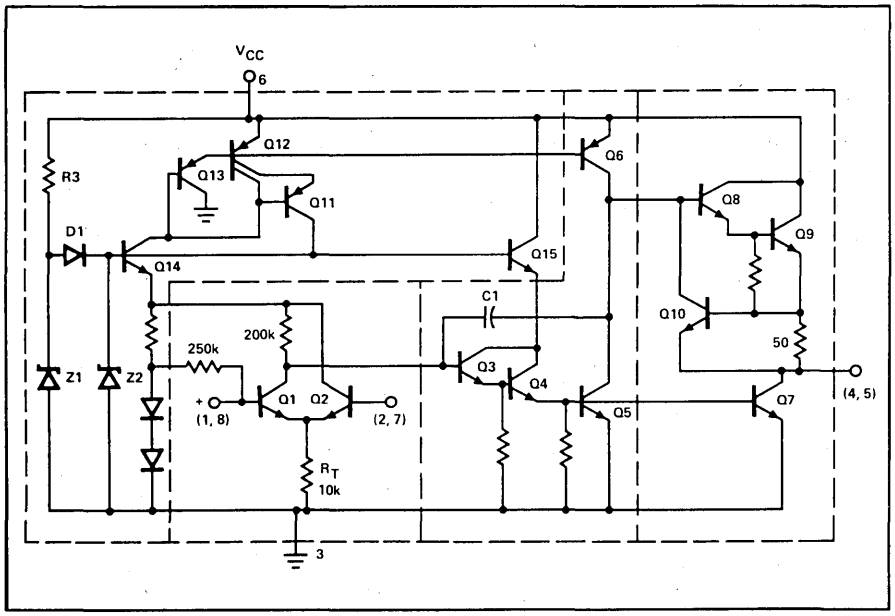
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	+24	V
Power dissipation	500	mW
Operating temperature range	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60 sec)	+300	°C

EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = 14V$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	NE542			UNIT
		Min	Typ	Max	
Supply voltage		9		24	V
Supply current	V_{CC} = 9 to 18V, $R_L = \infty$		9	15	mA
Input resistance					
Positive input			100		kΩ
Negative input			200		kΩ
Output resistance	Open loop		150		Ω

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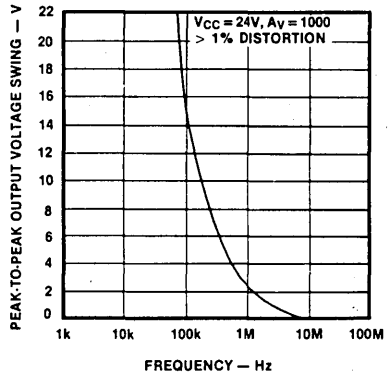
DUAL LOW-NOISE PREAMP NE542

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 14V$ unless otherwise specified.

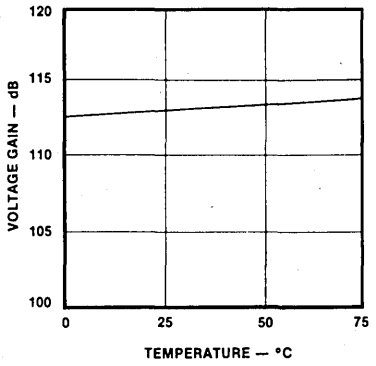
PARAMETER	TEST CONDITIONS	NE542			UNIT
		Min	Typ	Max	
Voltage gain	Open loop		160,000		V/V
Input current Negative input			 .5		 μA
Output current	Source Sink (linear operation)	8 2	14 3		mA mA
Output voltage swing Small signal bandwidth Slew rate Power bandwidth	 15V p-p	V_{CC} -2.5	V_{CC} -2 15 5 100		V MHz V/μs kHz
Maximum input voltage	Linear operation			300	mVrms
Supply rejection ratio Channel separation	f = 60, 120Hz f = 1kHz f = 1kHz		100 110 70		dB dB dB
Total harmonic distortion Total equivalent input Noise	75dB gain, f = 1kHz RS = 600Ω, 100 - 10,000Hz		.1 .7	 1.2	% μVrms
Noise figure	RS = 50kΩ, 10 - 10,000Hz RS = 20kΩ, 10 10,000Hz RS = 10kΩ, 10 - 10,000Hz RS = 5kΩ, 10 - 10,000Hz		1.2 1.2 1.5 2.4		dB dB dB dB

TYPICAL PERFORMANCE CHARACTERISTICS

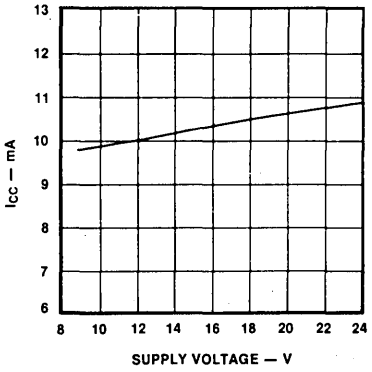
LARGE SIGNAL FREQUENCY RESPONSE



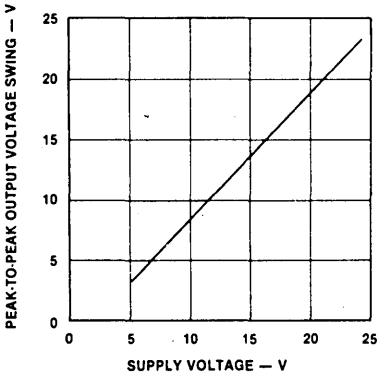
GAIN vs TEMPERATURE



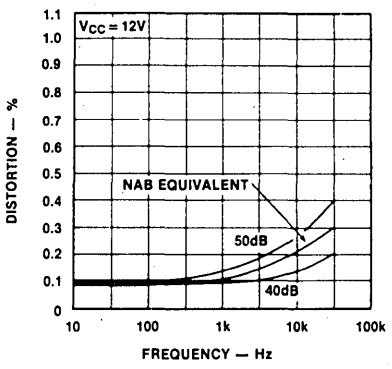
V_{CC} vs I_{CC}



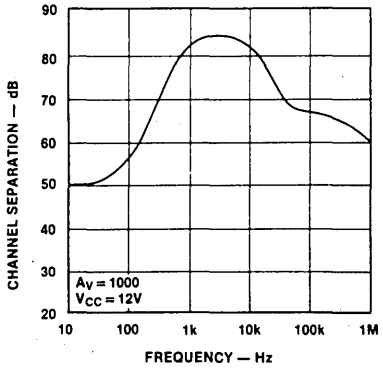
P-P OUTPUT VOLTAGE SWING vs V_{CC}



% DISTORTION



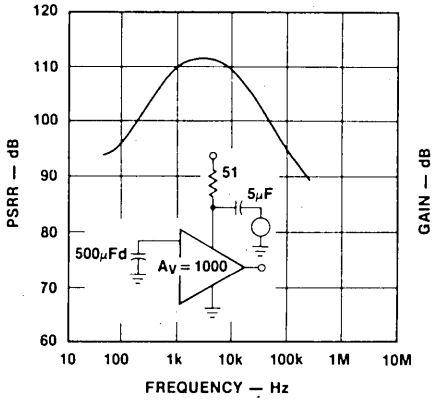
CHANNEL SEPARATION



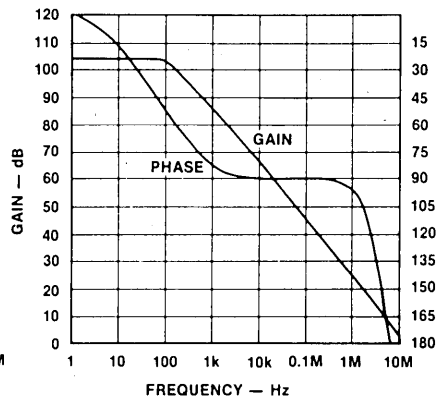
DUAL LOW-NOISE PREAMP NE542

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

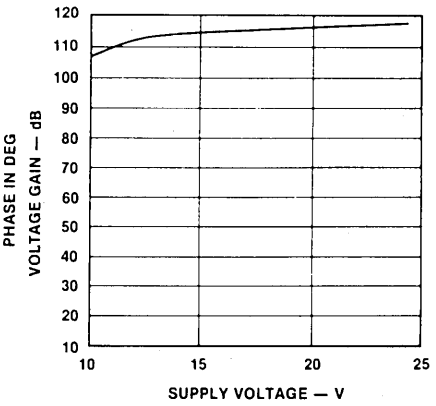
PSRR vs FREQUENCY



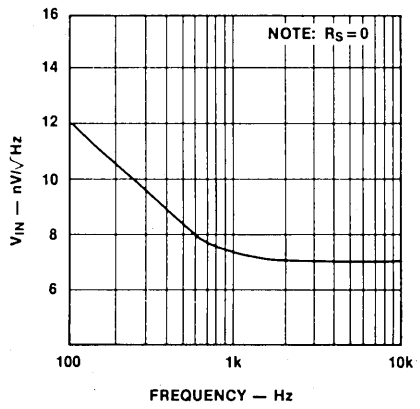
GAIN AND PHASE RESPONSE



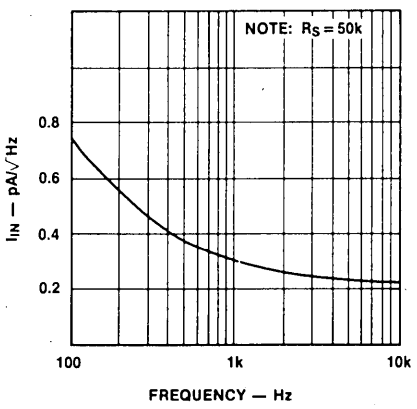
VOLTAGE GAIN vs SUPPLY VOLTAGE



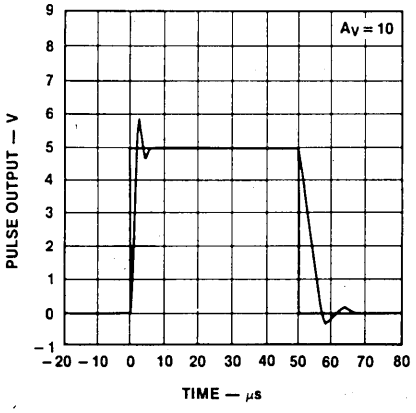
NOISE VOLTAGE vs FREQUENCY



NOISE CURRENT vs FREQUENCY

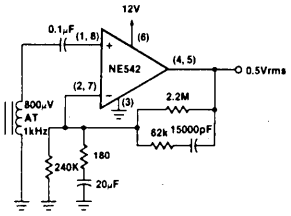


PULSE RESPONSE

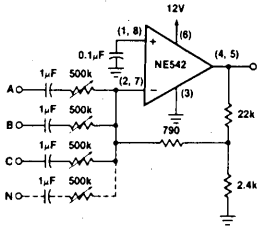


TYPICAL APPLICATIONS

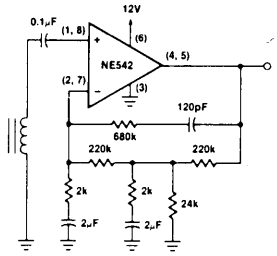
TYPICAL TAPE PLAYBACK AMPLIFIER



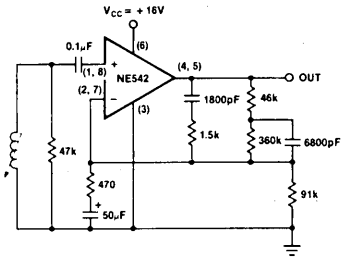
AUDIO MIXER



TWO-POLE FAST TURN-ON NAB TAPE PREAMP



RIAA MAGNETIC PHONO PREAMP



NOTE: All resistors values are typical and in ohms.

LINEAR

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8-BIT GENERAL PURPOSE A/D CONVERTER NE5034

DESCRIPTION

The NE5034 is a high-speed microprocessor-compatible 8-bit Analog-to-Digital converter. It uses the successive approximation conversion technique, and includes the comparator, reference DAC, SAR, an internal clock and three-state buffers all on the same chip.

The converter can accommodate a wide analog input voltage range, bipolar or unipolar, selectable through external input resistors. An external capacitor controls the internal clock frequency, providing conversion times down to 17μs. Faster conversion times are possible using an external clock.

Microprocessor interfacing requirements are simple, allowing analog-to-digital conversion with a minimum of external components.

FEATURES

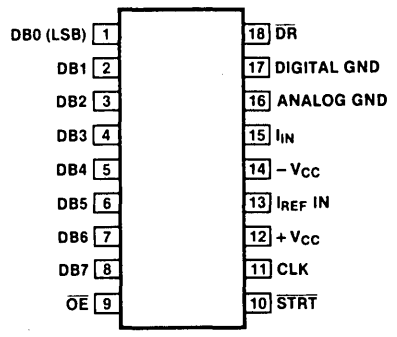
- **8-bit resolution and accuracy**
- **Accepts unipolar or bipolar inputs**
- **Three-state output buffers for easy microprocessor interface**
- **Choice of internal or external clocking**
- **Short conversion time, 17μs typical using internal clock**

APPLICATIONS

- **All microprocessor-based monitoring and control systems requiring analog signal inputs.**
- **Typical applications include: Automated process control, machine tools, robots, test and measurement instruments, environmental controls**
- **Other applications include: Ratiometric A/D conversion, very high resolution A/D conversion systems requiring high speed 8-bit building blocks**

PIN CONFIGURATION

F PACKAGE



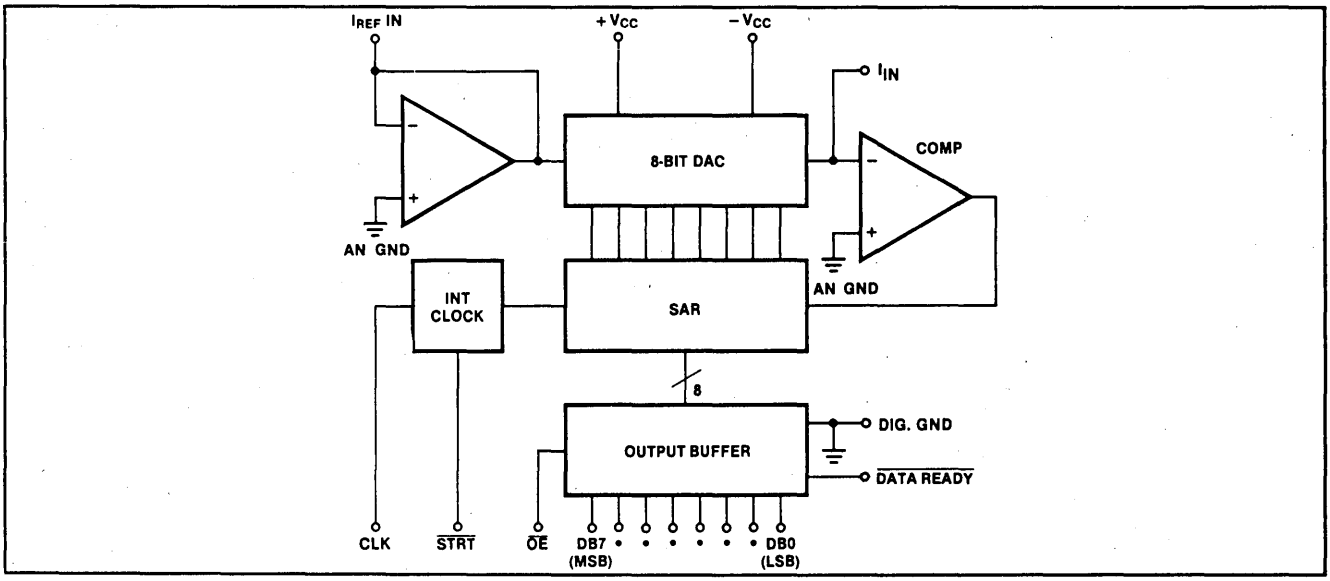
TOP VIEW

ORDER NUMBERS
NE5034F, NE5034N

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
$V_{CC}+$	Positive supply voltage	0 to +6	V
$V_{CC}-$	Negative supply voltage	0 to −15	V
I_{REF}	Reference current	1.5	mA
I_{IN}	Analog input current	5.0	mA
V_O	Data output voltage	6.0	V
Analog GND to Digital GND		1.0	V
V_L	Logic input voltage	−1 to $V_{CC}+$	V
P_D	Power dissipation		
	F package	1000	mW
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

BLOCK DIAGRAM



LINEAR

Signetics

8-BIT GENERAL PURPOSE A/D CONVERTER NE5034

DC ELECTRICAL CHARACTERISTICS $+V_{CC} = 5.0V$, $-V_{CC} = -12V$, $0°C \leq T_A \leq 70°C$ unless otherwise specified

SYMBOL AND PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution		8	8	8	Bits
	Relative accuracy error[1, 2]				± 1/2	LSB
$V_{CC}+$	Positive supply range		4.75	5.0	5.25	V
$V_{CC}-$	Negative supply range		−11.4	− 12	−12.6	V
E_{FS}	Full scale gain error	$I_{REF} = 1.0mA$, $T_A = 25°C$		± 2	± 5	LSB
E_{ZS}	Zero scale offset error	$I_{REF} = 1.0mA$, $T_A = 25°C$		± 0.5	± 1	LSB
Psr	Power supply rejection[3]	$I_{REF} = 1.0$ mA, V_{CC} + 4.75 to + 5.25V, V_{CC} − 11.4 to − 12.6V			± 1/2	LSB
V_{IH}	Logic 1 input voltage ($\overline{STRT}$ and $\overline{OE}$)		2.0			V
V_{IH}	Logic 1 input voltage ext. clock		2.4			V
V_{IL}	Logic 0 input voltage ($\overline{STRT}$ and $\overline{OE}$)				0.8	V
V_{IL}	Logic 0 input voltage ext clock				0.7	V
I_{IH}	Logic 1 input current ($\overline{STRT}$ and $\overline{OE}$)	$V_{IN} = 2.4V$			20	μA
I_{IH}	Logic 1 input current ext clock	$V_{IN} = 2.4V$		100		μA
I_{IL}	Logic 0 input current ($\overline{STRT}$ and $\overline{OE}$)	$V_{IN} = 0.4V$		− 20	− 100	μA
I_{IL}	Logic 0 input current ext. clock	$V_{IN} = 0.7V$		− 100		μA
V_{OL}	Logic 0 output voltage	$I_{OL} = 1.6mA$, $\overline{OE} = 0.8V$			0.4	V
V_{OH}	Logic 1 output voltage	$I_{OH} = 400\mu A$, $\overline{OE} = 0.8V$	2.4			V
I_{OZ}	Three-state leakage	$\overline{OE} = 2.0V$, $V_{OL} = 0V$ or 5V		± 10		μA
$I_{CC}+$	Positive supply current	$V_{CC} + 5V$, $V_{CC} - 12V$		18	36	mA
I_{CC}	Negative supply current	$V_{CC} + 5V$, $V_{CC} - 12V$		− 11	− 22	mA

NOTES
1. Relative accuracy is defined as the deviation of the code transition points from the ideal code transition points on a straight line drawn from zero scale to full scale of the device.
2. Specifications given in LSBs refer to the weight of the least significant bit at the 8-bit level which is 0.39% of the full scale voltage.
3. MAX change in full scale.

AC ELECTRICAL CHARACTERISTICS $V+ = +5V$, $V- = -12V$, $T_A = 25°C$

SYMBOL & PARAMETER	TO	FROM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Internal clock frequency			$C_L = 60pF$ (See Figure 1)		500		KHz
External clock frequency						700	KHz
Tw $\overline{STRT}$ pulse width			Clock freq. = 500KHz	400			ns
External clock pulse width positive/negative				600			ns
Set up time[1]			See Figure 3	300			ns
tp (out data) propagation delay	data out	$\overline{OE}$	See Figure 2		50	200	ns
tp (out $\overline{DR}$) propagation delay	data ready out	8th clock	See Figure 3		700		ns
tp (3-state) propagation delay 3-state	high impedance o/p	$\overline{OE}$	See Figure 2		60	200	ns
tp (DB0) propagation delay	DB0	$\overline{DR}$	See Figure 3			500	ns
tp (SDR) $\overline{STRT}$ low to $\overline{DR}$ high	data ready high	$\overline{STRT}$ low	See Figure 3		700		ns

NOTE
1. See description of "Set up time".

8-BIT GENERAL PURPOSE A/D CONVERTER NE5034

TYPICAL PERFORMANCE CHARACTERISTICS

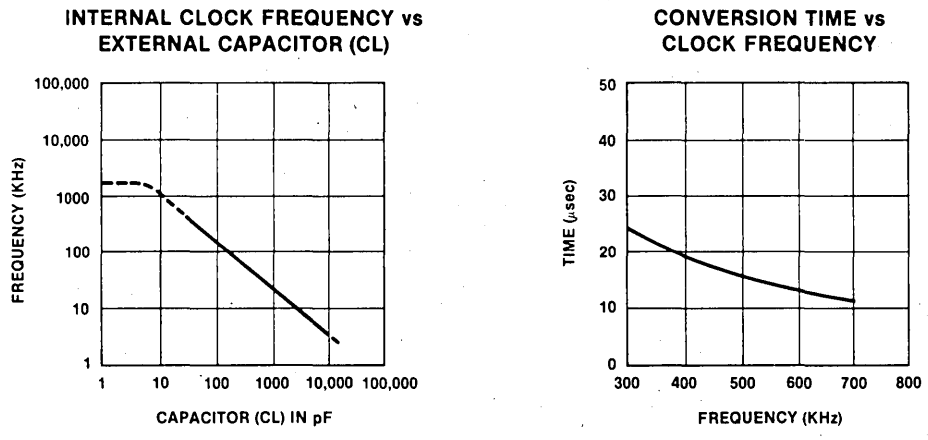


FIGURE 1

TEST LOAD CIRCUITS

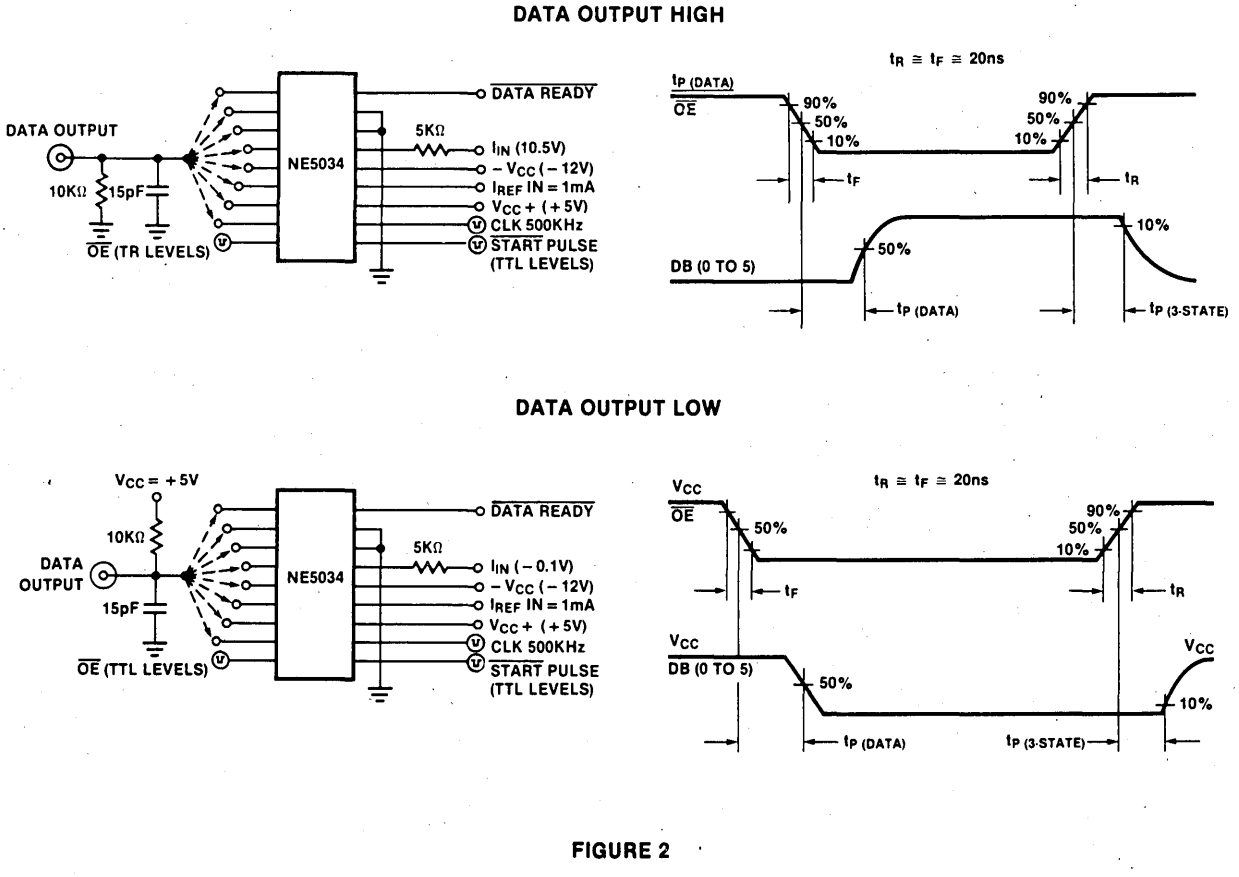


FIGURE 2

8-BIT GENERAL PURPOSE A/D CONVERTER NE5034

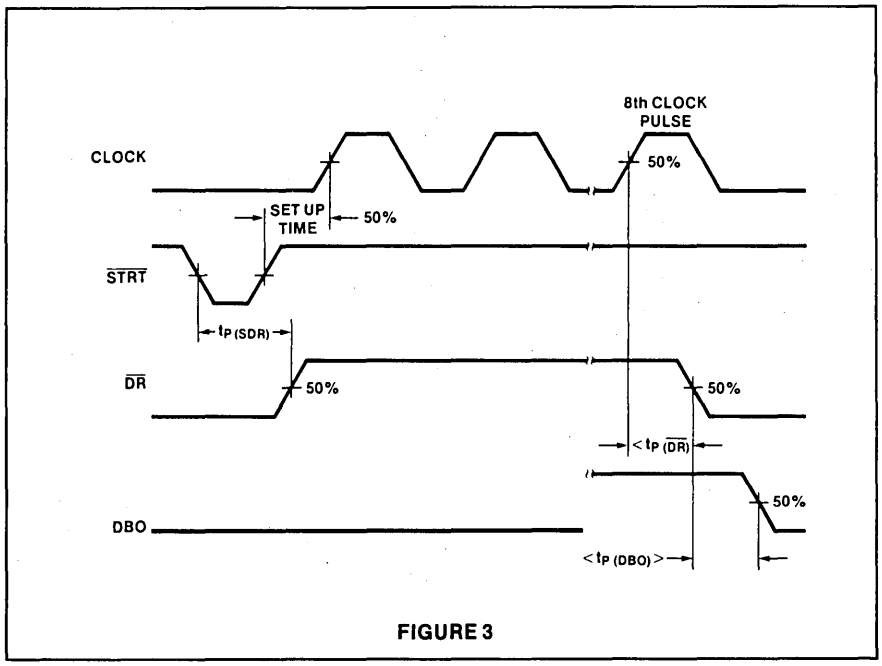


FIGURE 3

FUNCTIONAL PIN DEFINITIONS

DATA READY (DR)

This is an output pin used to indicate that a conversion is in progress. DR goes to a logic "1" when STRT is at a logic "0". At the completion of a conversion DR returns to a logic "0". There is a delay (MAX 0.5μs) from the time DR goes to "0" to the time DB0 data is valid.

DB0-DB7

Eight three-state data outputs each with a drive capability of one TTL load. DB0 is the LSB and DB7 is the MSB.

OE

Output enable input. When OE is at a logic "1" the data outputs assume a high impedance state. With OE at a logic "0", data is placed on the outputs. Data appearing on the outputs is only valid if both OE and DR are at logic "0" (see note on DR timing).

STRT

This pin is used to reset the converter and start a new conversion. A logic "0" applied to this pin for a minimum of 400ns will reset the converter to a condition with DB7 at a logic "1" and all other Data outputs at logic "0". It will also cause DR to go to a logic "1" (see timing diagrams for delay times). Conversion will start with the 1st clock pulse after STRT returns to a logic "1" (see notes on set up time required). A STRT pulse while a conversion is taking place will cause the conversion to be aborted and the converter will reset. (See notes on short-cycle operation.)

CLK IN

An external capacitor between this pin and ground generates the internal clock pulses. (See diagram for clock frequency vs capacitor value). In order to synchronize the internal clock, to the start pulse a diode (small signal type e.g., 1N914) should be connected between STRT and CLK IN (see Figures 4 and 5). Without this diode the start pulse could occur at a time which could cause one of the conditions described in the Note on "set up" time. Applying an external TTL-or MOS-compatible clock to this pin slaves the NE5034 to external clock frequency. In this case, the diode is not required but the "set up" time requirements should be noted.

BASIC CIRCUIT DESCRIPTION

The NE5034 is an 8-bit A/D converter which incorporates the successive-approximation conversion method. Upon receipt of the STRT pulse, successive bits, beginning with the MSB (DB7), are applied to the input of the internal 8-bit current output DAC by the I^2L successive-approximation register (SAR) (see Block Diagram).

The comparator determines whether the output current of the DAC is greater or less than the input current converted from the unknown analog input voltage through an external input resistor. If the DAC output current is greater, the data latch for the trial bit is reset to a '0'; if it is less, the trial data bit stays at '1'. After all the bits from DB7 to DB0 have been tried, the SAR contains a valid 8-bit binary output code which accurately represents the unknown analog input to within ± 1/2 LSB (± 0.2%). This binary output will now remain in the SAR until another STRT pulse is applied.

During the successive-approximation sequence, the DATA READY signal remains at '1'. Upon completion of the conversion, the signal goes to a '0', indicating that data is valid and ready. If the OE input is left at a '0' during the conversion, the DATA OUTPUT shows the conversion sequence (see short cycle section). When the OE line is made a logic '1', the output buffers will go to a high impedance state and will remain so until the OE is returned to a '0' state.

TIMING DESCRIPTION

The timing diagram shown in Figure 7 shows the successive trial and decisions for each data bit.

With STRT at a logic "0" the converter is reset to a condition with DB7 at a logic "1", DR at a logic "1" and DB0-DB6 at logic "0".

Conversion starts after STRT returns to a logic "1". Starting with DB7 each bit is tried in turn, with the decision point being at the time of the positive going edge of the clock. Starting with the first positive edge after STRT returns to logic "1" (see note on "set up" time). The 8th positive going edge makes the decision on DB0 (LSB) and also causes DR to return to a logic "0" to indicate the conversion is complete. (See note on DR timing.)

SHORT-CYCLE OPERATION

In applications where less than 8 bits of resolution are required the NE5034 can be operated to achieve shorter conversion times. No hard wire changes are required to perform "short-cycling".

Conversion to X number of bits is completed at the end of X + 0.5 clock cycles (after a start pulse) DR will still be at a logic "1" state.

OE can be used to 3-state the outputs even during short-cycle operation.

8-BIT GENERAL PURPOSE A/D CONVERTER NE5034

BASIC SET-UP DIAGRAM
UNIPOLAR INPUT VALUES (0–10V)

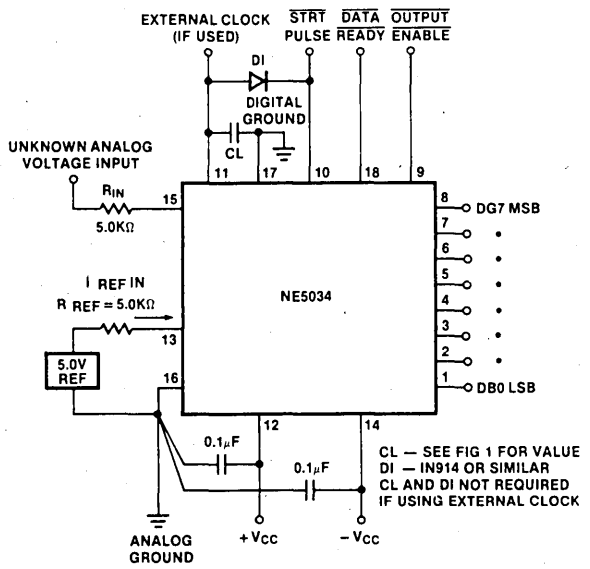


FIGURE 4.

BASIC SET-UP DIAGRAM
BIPOLAR INPUT VALUES (± 10V RANGE)

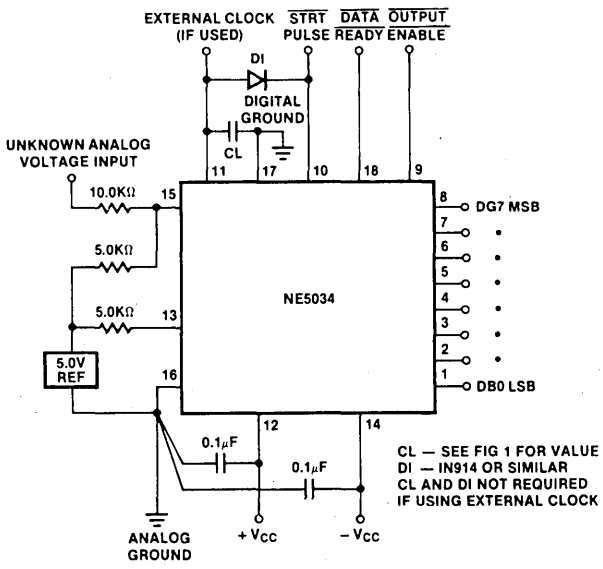


FIGURE 5.

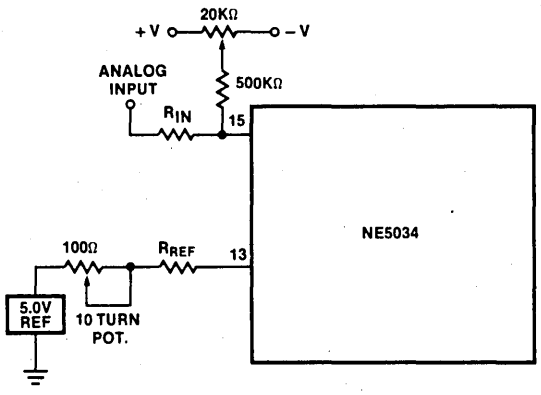


FIGURE 6. SUGGESTED ZERO/FULL SCALE ADJUST CIRCUIT

8-BIT GENERAL PURPOSE A/D CONVERTER NE5034

SET UP TIME

When using an external clock, the positive going edge of the start pulse must be synchronized to the clock pulse. There is a "set up" time of 300ns required between the time of the start pulse returning to a logic "1" and the next positive going edge of the clock.

If the positive edge of the start pulse occurs less than 300ns prior to the positive clock edge, one of the following conditions will occur:

a) The converter recognizes the clock pulse and converts as normal.
b) The conversion starts one clock pulse later.
c) The conversion never starts, this will be indicated by the fact that $\overline{DR}$ does not return to logic "0". In this case a new start pulse will be required.

DATA READY ($\overline{DR}$) TIMING

After $\overline{DR}$ returns to a logic "0" indicating a conversion is complete there is a time delay of 500ns before the data at DB0 output (the Least Significant Bit) is valid.

ZERO OFFSET (NEGATIVE FULL SCALE) CALIBRATION PROCEDURES

1. Apply continuous start pulses to the $\overline{STRT}$ input.
2. Apply 1/2 LSB in the case of unipolar operation, or 1/2 LSB above – FS in the case of bipolar operation to the analog input.
3. Observe all data outputs after each conversion is completed.
4. Adjust the potentiometer connected to I_{IN} (see Figure 6) until the LSB flickers between '0' and '1', and all other data outputs remain '0' following each conversion.

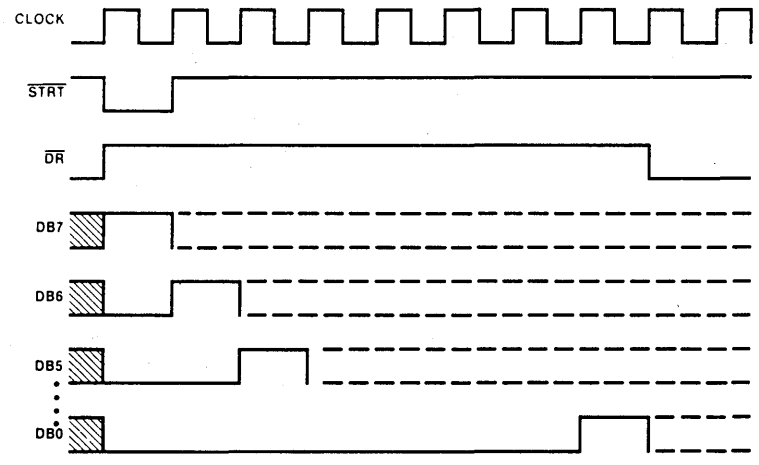
FULL SCALE (POSITIVE FULL SCALE) CALIBRATION:

1. Apply continuous start pulses to the $\overline{STRT}$ input.
2. Apply full scale minus 1 1/2 LSB to the analog input.
3. Observe all data outputs after each conversion is completed.
4. Adjust the voltage applied to $V_{REF\ IN}$ (Figure 4) until the LSB varies between '0' and '1', and all other data outputs stay '1' after each conversion.

NOTE:
1. Where an input of 1/2 LSB is called for, the voltage is equal to $\frac{FS}{256}$.
2. The sequence of calibration should be:
   a. Zero offset
   b. Full scale adjust
   c. Zero offset
   d. Full scale adjust

OPERATING PRECAUTIONS:

Analog and digital grounds should have separate returns. Noise and jitter on digital ground will degrade accuracy unless the input is referenced to a 'clean' analog ground.



NOTE
1. $\overline{OE}$ = Logic "0"
2. See "Short-Cycle" section

FIGURE 7. NE5034 TIMING DIAGRAM

UNIPOLAR BINARY OPERATION:

A standard connection for a 0 to 10V unipolar binary operation, with $V_{REF\ IN}$ equal to +5 volts, is shown in Figure 4. The NE5034 can quantize full scale ranges of 1V to 10V. It should be noted, however, that for smaller full scale ranges, the accuracy and speed will degrade.

The input voltage versus output code relationship for unipolar operation is shown in Table 1. The full scale range is 2 times $I_{REF\ IN}$.

Table 1. Unipolar—Binary

ANALOG INPUT	DIGITAL OUTPUT CODE	
NOTES 1, 2, 3	MSB	LSB
FS—1 LSB	1 1 1 1 1 1 1 1	
FS—2 LSB	1 1 1 1 1 1 1 0	
3/4 FS	1 1 0 0 0 0 0 0	
1/2 FS + 1 LSB	1 0 0 0 0 0 0 1	
1/2 FS	1 0 0 0 0 0 0 0	
1/2 FS – 1 LSB	0 1 1 1 1 1 1 1	
1/4 FS	0 1 0 0 0 0 0 0	
1 LSB	0 0 0 0 0 0 0 1	
0	0 0 0 0 0 0 0 0	

Table 2. Bipolar—Offset Binary

ANALOG INPUT	DIGITAL OUTPUT CODE	
NOTES 1, 3, 4	MSB	LSB
+ (FS – 1 LSB)	1 1 1 1 1 1 1 1	
+ (FS – 2 LSB)	1 1 1 1 1 1 1 0	
+ (1/2 FS)	1 1 0 0 0 0 0 0	
+ (1 LSB)	1 0 0 0 0 0 0 1	
0	1 0 0 0 0 0 0 0	
– (1 LSB)	0 1 1 1 1 1 1 1	
– (1/2 FS)	0 1 0 0 0 0 0 0	
– (FS – 1 LSB)	0 0 0 0 0 0 0 1	
– FS	0 0 0 0 0 0 0 0	

BIPOLAR (OFFSET BINARY) OPERATION:

A standard connection for a – 5 to + 5V or – 10 to + 10V bipolar operation is shown in Figure 5.

NOTES:
1. Analog inputs shown are nominal center values of code.
2. "FS" is full scale; i.e., $2I_{REF\ IN}$ (Unipolar mode).
3. 1 LSB equals (2^{-8}) (FS).
4. "FS" is full scale; i.e., $I_{REF\ IN}$ (Bipolar mode).

SWITCHED-MODE POWER SUPPLY CONTROL CIRCUIT NE/SE5560

DESCRIPTION

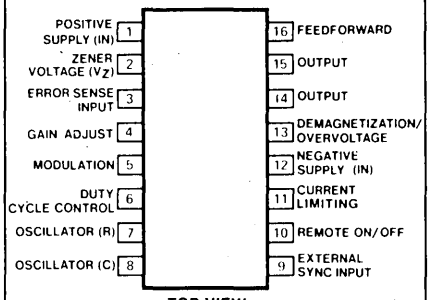
The NE/SE5560 is a control circuit for use in switched mode power supplies. This single monolithic chip incorporates all the control and housekeeping (protection) functions required in switched mode power supplies, including an internal temperature compensated reference source, internal Zener reference, sawtooth generator, pulse width modulator, output stage and various protection circuits.

FEATURES

- **Stabilized power supply**
- **Temperature compensated reference source**
- **Sawtooth generator**
- **Pulse width modulator**
- **Remote on/off switching**
- **Current limiting**
- **Low supply voltage protection**
- **Loop fault protection**
- **Demagnetization/overvoltage protection**
- **Maximum duty cycle adjustment**
- **Feed forward control**
- **External synchronization**

PIN CONFIGURATION

D,F,N PACKAGE



TOP VIEW

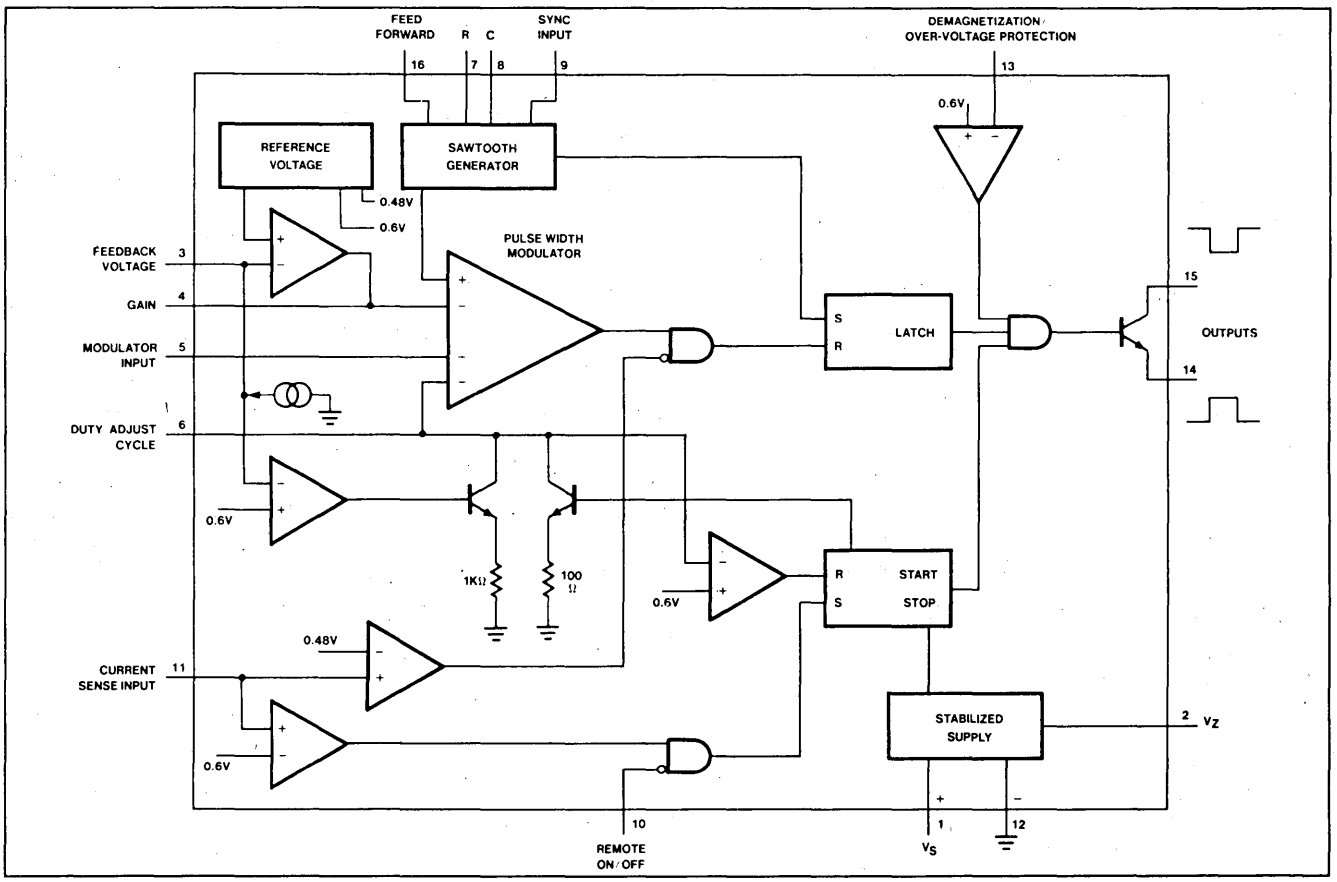
ORDER NUMBERS

NE5560N SE5560F
NE5560D SE5560N
NE5560F

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply		
Voltage sourced	+18	V
Current sourced	30	mA
Output transistor		
Output current	40	mA
Collector voltage (Pin 15)	+18	V
Max. emitter voltage (Pin 14)	+5	V
Operating temperature (ambient)		
SE5560	−55 to +125	°C
NE5560	0 to 70	°C
Storage temperature range	−65 to +150	°C

BLOCK DIAGRAM



SWITCHED-MODE POWER SUPPLY CONTROL CIRCUIT NE/SE5560

DC ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V_{CC} = 12V$ unless otherwise specified)

PARAMETER	TEST CONDITIONS	SE5560			NE5560			UNIT
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Reference Sections	Over temp.	3.65		3.85	3.53		4.00	V
Internal reference voltage (V_{ref})	25°C	3.69	3 76	3.81	3.57	3.76	3.95	V
Internal Zener reference (V_Z)	$I_L = 7mA$	7.8	8.4	9.0	7.8	8.4	9.0	V
Oscillator Section								
Frequency range	Over temp.	50		100k	50		100k	Hz
Modulator								
Modulator input current	Voltage at Pin 5 = 1V over temp.		0.2	20		0.2	20	μA
Housekeeping Function								
*Pin 6, input current	Over temp.		0.2	20		0.2	20	μA
*Pin 6, duty cycle limit control	(for 50% maximum duty cycle) 15kHz to 50kHz/41% of V_Z	40	50	60	40	50	60	% of duty cycle
*Pin 1, low supply voltage protection thresholds		V_Z+ 0.2	V_Z+ 0.7V	V_Z+ 1.7V	V_Z+ 0.2	V_Z+ 0.7V	V_Z+ 1.7V	V
*Pin 3, feedback loop protection trip threshold		470	600	720	470	600	720	mV
*Pin 3, pull up current	Over temp.		−15	−35		−15	−35	μA
*Pin 13, demagnetization/over voltage protection trip on threshold		470	600	720	470	600	720	mA
*Pin 13, input current	25°C		0.6	10		0.6	10	μA
	Over temp.			20			20	μA
Pin 16, feed forward duty cycle[2] control	Voltage at Pin 16 = $2V_Z$		0.4			0.4		original duty cycle
*Pin 16, feed forward input current	25°C		0.2	5		0.2	5	μA
	Over temp.			10			10	μA
External Synchronization								
Pin 9 off		0		0.8	0		0.8	V
on		2		V_Z	2		V_Z	V
sink current	Voltage at Pin 9 = 0V, 25°C		−65	−100		−65	−125	μA
	Over temp.			−125			−125	μA
Remote								
*Pin 10 off		0	0.8		0	0.8		V
on		2	V_Z		2	V_Z		V
sink current	25°C		−85	−100		−85	−125	μA
	Over temp.			−125			−125	μA
Current Limiting								
*Pin 11, I_{IN}	Voltage at Pin 11 = 250mV, 25°C		−2	−10		−2	−10	μA
	Over temp.			−20			−	
Trip Levels:								
Shut down, slow start		0.560	0.600	0.700	0.560	0.600	0.700	V
Current limit		0.400	0.48	0.500	0.400	0.48	0.500	V
Error Amplifier								
Output voltage swing (maximum)		6.2			6.2			V
Output voltage swing (minimum)				0.7		0.7		V
Open loop gain			60			60		dB
Feedback resistor		10k		10k				Ω
Small signal bandwidth			3			3		MHz
Output Stage								
$V_{CE}(SAT)$ $I_C = 40mA$				0.5		0.5		V
Output Current (Pin 15)		40			40			mA
Max emitter voltage (Pin 14)		5	6		5	6		V

SWITCHED-MODE POWER SUPPLY CONTROL CIRCUIT NE/SE5560

DC ELECTRICAL CHARACTERISTICS (Continued)

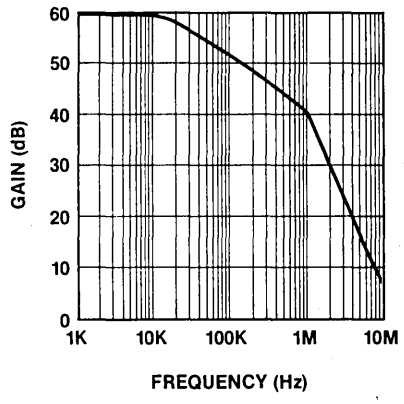
PARAMETER	TEST CONDITIONS	SE5560			NE5560			UNIT
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply Voltage/Current								
I_{CC}	$I_Z = 0$, voltage fed, $V_{CC} = 12V$, 25°C			10			10	mA
	Over temp.			15			15	mA
V_{CC}	$I_{CC} = 10mA$, current feed	20		23	19		24	V
V_{CC}	$I_{CC} = 30mA$, current feed	20		30	20		30	V
Temperature coefficient of V_{ref}			+75			+75		ppm/°C
Temperature coefficient of V_Z			+150			+150		ppm/°C
Initial accuracy	$R = 5k\Omega$		5			5		%
Duty cycle range[1]	fo = 20kHz	0		98	0		98	%
Single pulse inhibit delay	Inhibit delay time for 20% overdrive at 40mA I_{OUT}		0.7	0.8		0.7	0.8	μs

NOTES:
1. See graph.
2. See graph.

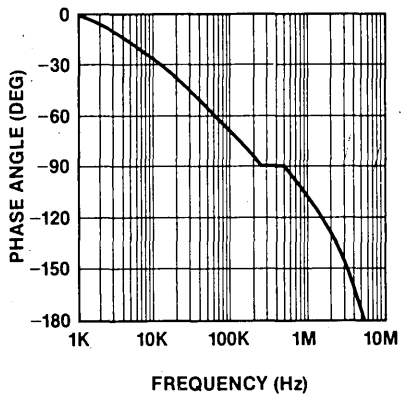
TYPICAL PERFORMANCE CHARACTERISTICS

ERROR AMPLIFIER

OPEN LOOP GAIN



OPEN LOOP PHASE



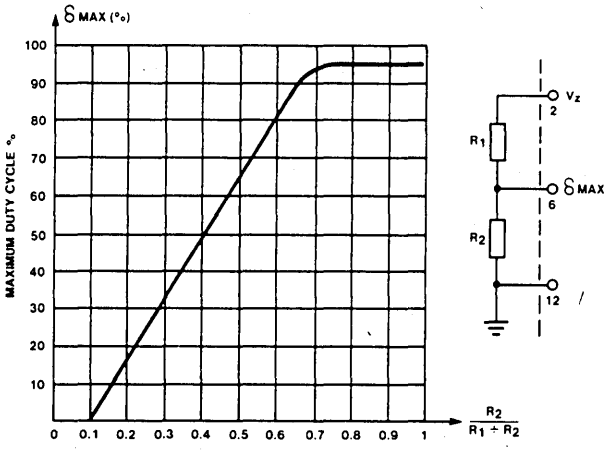
LINEAR

Signetics

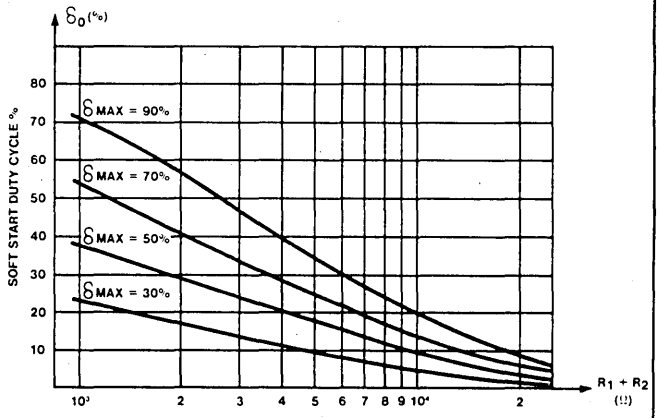
SWITCHED-MODE POWER SUPPLY CONTROL CIRCUIT NE/SE5560

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

GRAPH FOR DETERMINING δ MAX

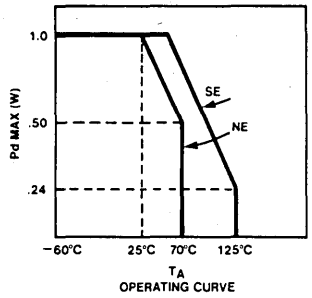


SOFT-START MIN DUTY CYCLE vs $R_1 + R_2$

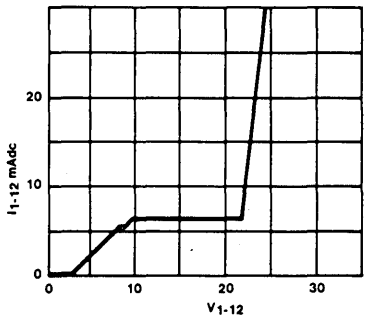


POWER DERATING CURVE

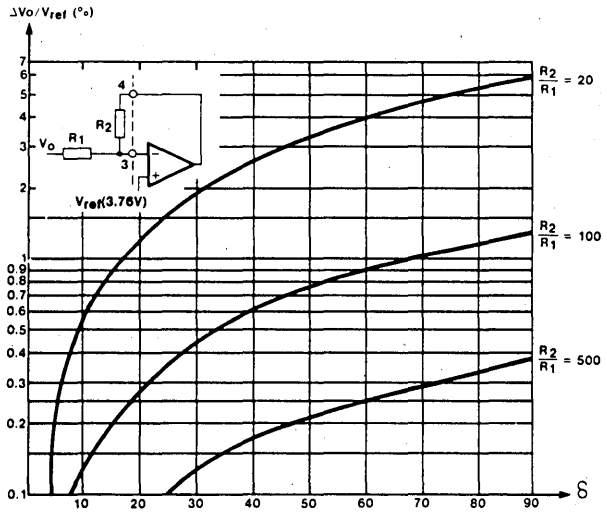
$Pd = V_{CC} I_{CC} + (V_{CC} - V_Z) I_Z + [(V_{15} - V_{14}) I_{15} \times \text{DUTY CYCLE}]$



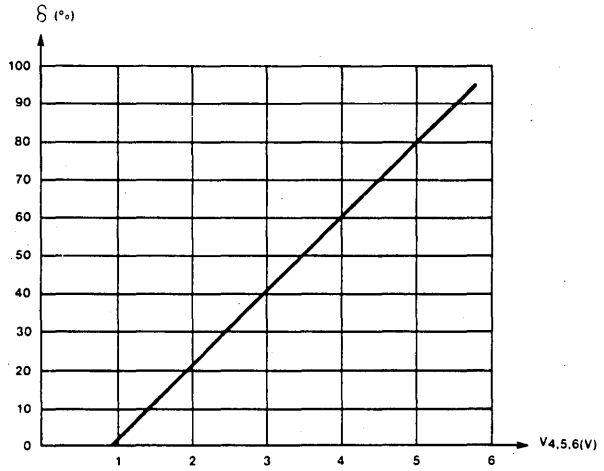
NE5560 VOLTAGE/CURRENT FED SUPPLY CHARACTERISTICS



REGULATION vs ERROR AMP CLOSED LOOP GAIN



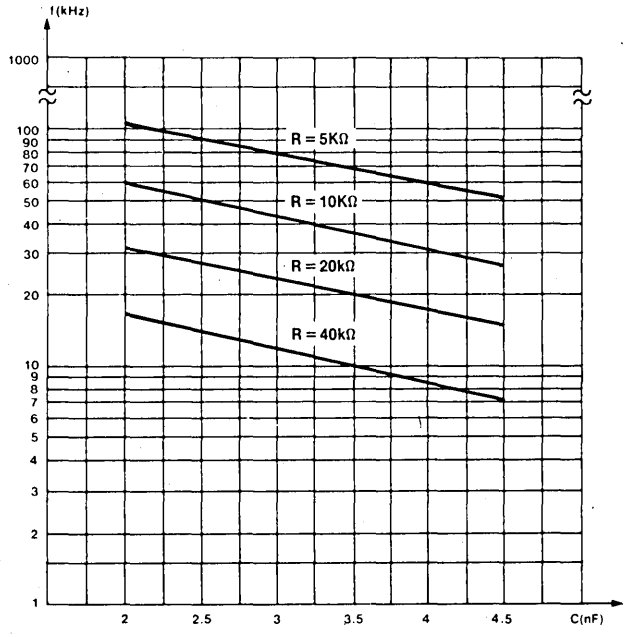
TRANSFER CURVE OF PULSE WIDTH MODULATOR DUTY CYCLE vs INPUT VOLTAGE



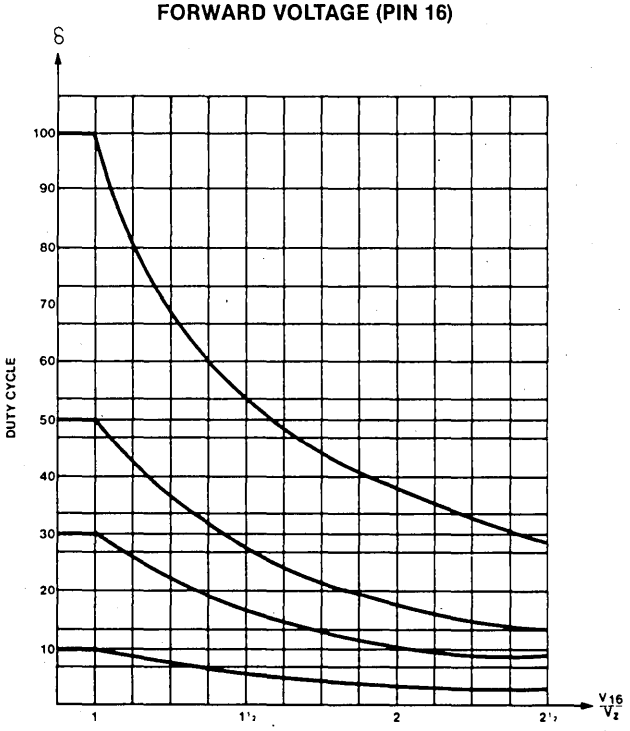
SWITCHED-MODE POWER SUPPLY CONTROL CIRCUIT NE/SE5560

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

TYPICAL FREQUENCY PLOT vs R_T AND C_T



DUTY CYCLE SENSITIVITY TO FEED FORWARD VOLTAGE (PIN 16)



DESCRIPTION of the NE5560 BLOCK DIAGRAM

The following functions are incorporated:

- A temperature compensated reference source.
- An error amplifier with pin 3 as input. The output is connected to pin 4 so that the gain is adjustable with external resistors.
- A sawtooth generator with a TTL-compatible synchronization input (pins 7,8,9).
- A pulse-width modulator with a duty-cycle range from 0 to 95%.

The PWM has two additional inputs:

Pin 6 can be used for a precise setting of δ max.

Pin 5 gives a direct access to the modulator, allowing for real constant current operation:

- A gate at the output of the PWM provides a simple dynamic current limit.
- A latch that is set by the flyback of the sawtooth and reset by the output pulse of the above-mentioned gate prohibits double pulsing.
- Another latch functions as a start-stop circuit; it provides a fast switch-off and a slow start.
- A current protection circuit that operates via the start-stop circuit. This is a combined function with the current limit circuit, therefore pin 11 has two trip-on levels; the lower one for cycle-by-cycle current limiting, the upper one for current protection by means of switch-off and slow-start.
- A TTL-compatible remote on/off input at pin 10, also operating via the start-stop circuit.
- An inhibit input at pin 13. The output pulse can be inhibited immediately.
- An output gate that is commanded by the latches and the inhibit circuit.
- An output transistor of which both the collector (pin 15) and the emitter (pin 14) are externally available. This allows for normal or inverse output pulses.
- A power supply that can be either voltage or current driven (pins 1 and 12). The internally generated stabilized output voltage V_Z is connected to pin 2.
- A special function is the so-called feed-forward at pin 16. The amplitude of the sawtooth generator is modulated in such a way that the duty cycle becomes inversely proportional to the voltage on this pin: $\delta \sim C/V16$.
- Loop fault protection circuits assure that the duty-cycle is reduced to zero or a low value for open or short-circuited feedback loops.

Stabilized Power Supply (Pins 1, 2, 12)

The power supply of the NE5560 is of the well known series regulation type and provides a stablized output voltage of typically 8.5 volts.

This voltage V_Z is also present at pin 2 and can be used for precise setting of δ max. and to supply external circuitry. Its maximum current capability is 5mA.

The circuit can be fed directly from a DC voltage source between 10.5V and 18V or can be current driven via a limiting resistor. In the latter case, internal pinch-off resistors will limit the maximum supply voltage; typical 23V for 10mA and maximum 30V for 30mA.

The low supply voltage protection is active when V(1-12) is below 10.5V and inhibits the output pulse.

When the supply voltage surpasses the 10.5V level, the IC starts delivering output pulses via the slow-start function.

The current consumption at 12V is less than 10mA, provided that no current is drawn from V_Z and R(7-12) ≥ 20kΩ.

SWITCHED MODE POWER SUPPLY CONTROL CIRCUIT NE/SE5560

The Sawtooth Generator

Figure 2 shows the principal circuitry of the oscillator. A resistor between pin 7 and pin 12 (ground) determines the constant current that charges the timing capacitor C(8-12).

This causes a linear increasing voltage on pin 8 until the upper level of 5.6V is reached. Comparator H sets the RS bistable and Q1 discharges C(8-12) down to 1.1V, where comparator L resets the bistable. During this flyback time, Q2 inhibits the output.

Synchronization at a frequency lower than the free-running frequency is accomplished via the TTL gate on pin 9. By activating this gate ($V^9 < 2V$), the setting of the sawtoothis prevented. This is indicated in Figure 3.

Figure 4 shows a typical plot of the oscillator frequency against the timing capacitor. The frequency range of the NE5560 goes from <50Hz up to >100kHz.

Reference Voltage Source

The interal reference voltage source is based on the bandgap voltage of silicon. Good design practice assures a temperature dependency < ±100ppm/°C. The reference voltage is connected to the positive input of the error amplifier and has a typical value of 3.72V.

Error Amp Compensation

For closed loop gains less than 40 dB, it is necessary to add a simple compensation capacitor as shown in Figures 4, 5.

SAWTOOTH GENERATOR

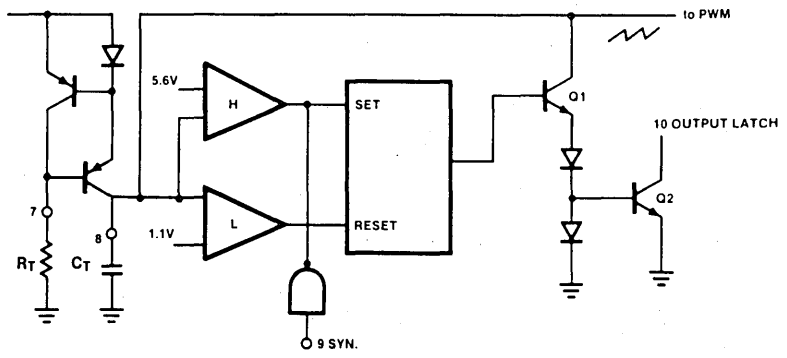


Figure 2

SAWTOOTH OSCILLATOR SYNCHRONIZATION

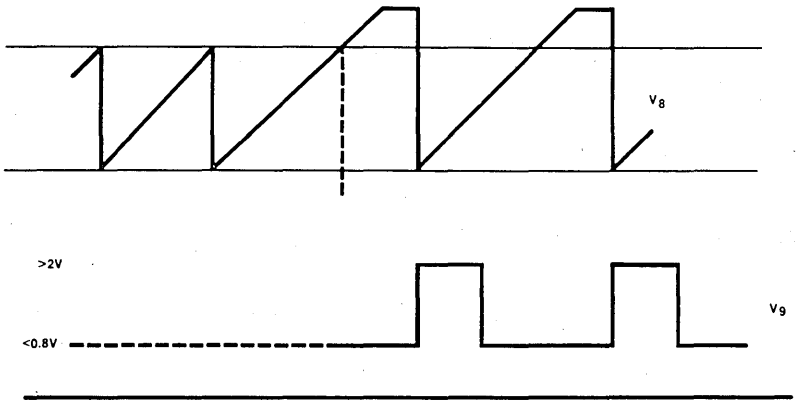


Figure 3

ERROR AMPLIFIER COMPENSATION

OPEN LOOP GAIN

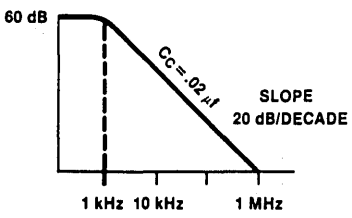


Figure 4

ERROR AMPLIFIER

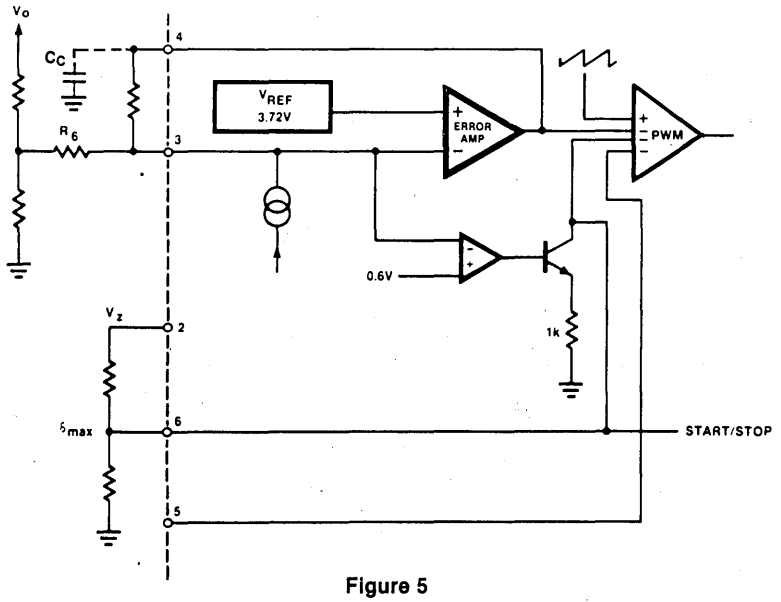


Figure 5

Error Amplifier with Loop-Fault Protection Circuits

This operational amplifier is of a generally used concept and has an open loop gain of typically 60dB. As can be seen in Figure 5, the inverting input is connected to pin 3 for a feedback information proportional to V_O.

The output goes to the PWM circuit, but is also connected to pin 4, so that the required gain can be set with R_S and R(3-4). This is indicated in Figure 5, showing the relative change of the feedback voltage as a function of the duty cycle. Additionally, pin 4 can be used for phase shift networks that improve the loop stability.

When the SMPS feedback loop is interrupted, the error amplifier would settle in the middle of its active region because of the feedback via R(3-4). This would result in a large duty cycle. A current source on pin 3 prevents this by pushing the input voltage high via the voltage drop over R(3-4). As a result, the duty cycle will become zero, provided that R(3-4)>100k. When the feedback loop is shortcircuited, the duty cycle would jump to the adjusted maximum duty cycle. Therefore, an additional comparator is active for feedback voltages at pin 3 below 0.6V.

Now an internal resistor of typically 1k is shunted to the impedance on the δ_{max}-setting pin 6. Depending on this impedance, δ will be reduced to a value δo. This will be discussed further.

DUTY CYCLE —δ— % REGULATION

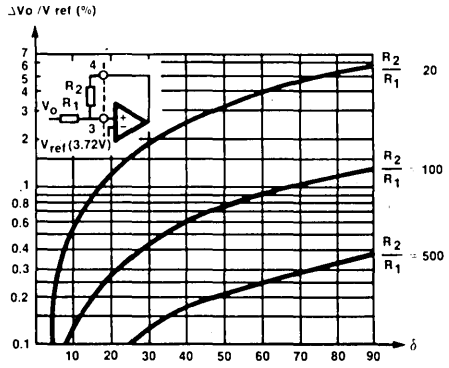


Figure 5

PULSE WIDTH MODULATION

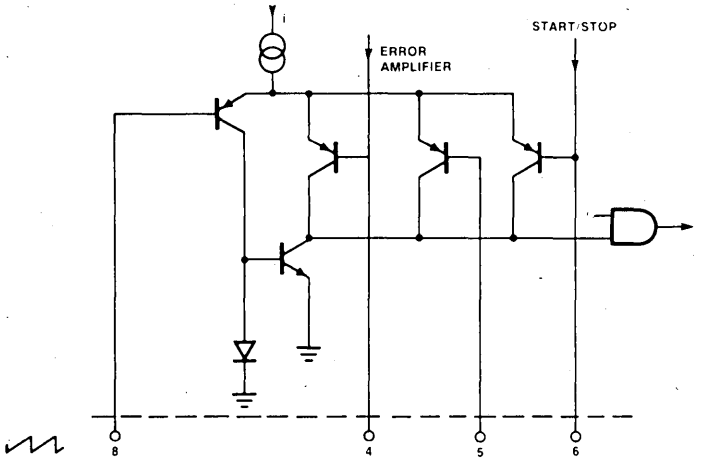


Figure 6

TRANSFER CURVE OF PULSE WIDTH MODULATOR DUTY CYCLE vs INPUT VOLTAGE

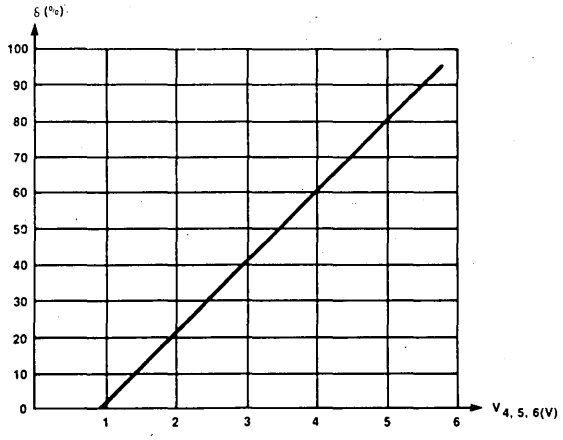


Figure 7

GRAPH FOR DETERMINING δ MAX

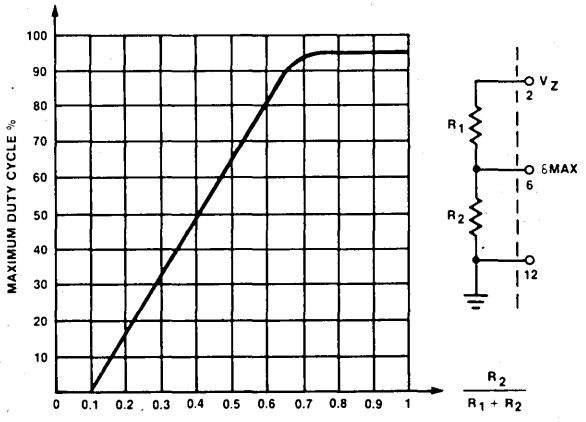


Figure 8

SWITCHED MODE POWER SUPPLY CONTROL CIRCUIT NE/SE5560

The Pulse-Width Modulator

The function of the PWM circuit is to translate a feedback voltage into a periodical pulse of which the duty cycle depends on that feedback voltage. As can be seen in Figure 6, the PWM circuit in the NE5560 is a long-tailed pair in which the sawtooth on pin 8 is compared with the LOWEST voltage on either pin 4 (error amplifier), pin 5, or pin 6 δ_{max} and slow-start). The transfer graph is given in Figure 7. The output of the PWM causes the resetting of the output bistable.

Limitation of the Maximum Duty Cycle

With pins 5 and 6 not connected and with a rather low feedback voltage on pin 3, the NE5560 will deliver output pulses with a duty cycle of ≈95%. In many SMPS applications, however, this high δ will cause problems. Especially in forward converters, where the transformer will saturate when δ exceeds 50%, a limitation of the maximum duty-cycle is a must.

A DC voltage applied to pin 6 (PWM input) will set δ_{max} at a value in accordance with Figure 7. For low tolerances of δ_{max}, this voltage on pin 6 should be set with a resistor divider from V_Z (pin 2). The upper and lower sawtooth levels are also set by means of an internal resistor divider from V_Z, so forming a bridge configuration with the δ_{max} setting is low because tolerances in V_Z are compensated and the sawtooth levels are determined by internal resistor matching rather than by absolute resistor tolerance. Figure 8 can be used for determining the tap on the bleeder for a certain δ_{max} setting.

As already mentioned, Figure 9 gives a graphical representation of this. The value δo is limited to the lower and the higher side;

- It must be large enough to ensure that at maximum load and minimum input voltage the resulting feedback voltage on pin 3 exceeds 0.6V.
- It must be small enough to limit the amount of energy in the SMPS when a loop-fault occurs. In practice a value of 10-15% will be a good compromise.

Extra PWM Input (Pin 5)

The PWM has an additional inverting input: pin 5. It allows for attacking the duty cycle via the PWM circuit, independently from the feedback and the δ_{max} information. This is necessary when the SMPS must have a real constant current behavior, possibly with a fold-back characteristic. However, the realization of this feature must be done with additional external components.

SOFT-START MIN DUTY CYCLE vs $R_1 + R_2$

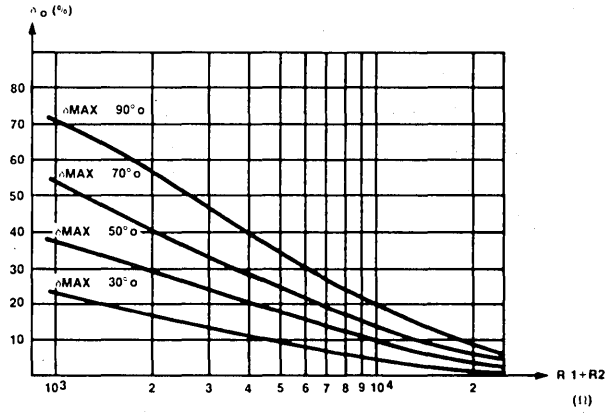


Figure 9

CURRENT PROTECTION INPUT

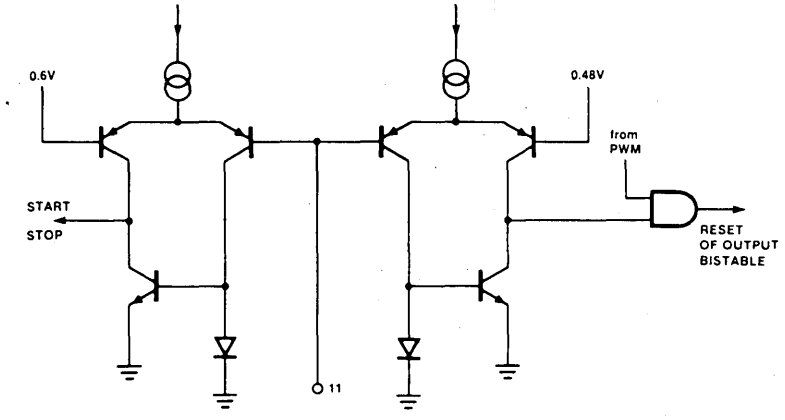


Figure 10

Dynamic Current Limit and Current Protection (Pin 11)

In many applications, it is not necessary to have a real constant current output of the SMPS.

Protection of the power transistor will be the prime goal. This can be realized with the NE5560 in a simple and cheap way. A resistor (or a current transformer) in the emitter of the power transistor gives a replica of the collector current. This signal must be connected to pin 11. As can be seen in Figure 10, this input has two comparators with different reference levels. The output of the comparator with the lower 0.48V reference is connected to the same gate as the output of the PWM.

OUTPUT CHARACTERISTIC

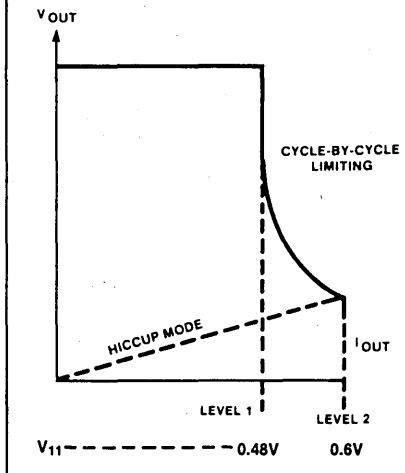


Figure 11

When activated, it will immediately reset the output bistable, so reducing the duty cycle. The effectiveness of this so-called cycle-by-cycle current limit diminishes at low duty cycle values. When δ becomes very small, the storage time of the power transistor become dominant. The current will now increase again, until it surpasses the reference of the second comparator. The output of this comparator activates the start/stop circuit and causes an immediate inhibit of the output pulses. After a certain dead-time, the circuit starts again with very narrow output pulses. The effect of this two-level current protection circuit is visualized in Figure 11.

The Start/Stop Circuit

The function of this protection circuit is to stop the output pulses as soon as a fault occurs and to keep the output stopped for several periods. After this dead time, the output starts with a very small, gradually increasing duty cycle. When the fault is persistent, this will cause a cyclic switch-off/switch-on condition. This "hiccup" mode limits effectively the energy during fault conditions. The realization and the working of the circuit is indicated in the Figures 12 and 13. The dead-time and the soft-start are determined by an external capacitor that is connected to pin 6 (δ_{max} setting).

A RS bistable can be set by three different functions:
1. Remote on/off on pin 10.
2. Overcurrent protection on pin 11.
3. Low supply voltage protection (internal).

As soon as one of these functions cause a setting of the bistable, the output pulses are blocked via the output gate. In the same time transistor Q1 is forward-biased, resulting in a discharge of the capacitor on pin 6.

The discharging current is limited by an internal 150Ω resistor in the emitter of Q1. The voltage at pin 6 decreases to below the lower level of the sawtooth. When V6 has dropped to 0.6V, this will activate a comparator and the bistable is reset. The output stage is no longer blocked and Q1 is cut-off. Now V_Z will charge the capacitor via R1 to the normal δ_{max} voltage. The output starts delivering very narrow pulses as soon as V6 exceeds the lower sawtooth level. The duty-cycle of the output pulse now gradually increases to a value determined by the feedback on pin 3, or by the static δ_{max} setting on pin 6.

START/STOP CIRCUIT

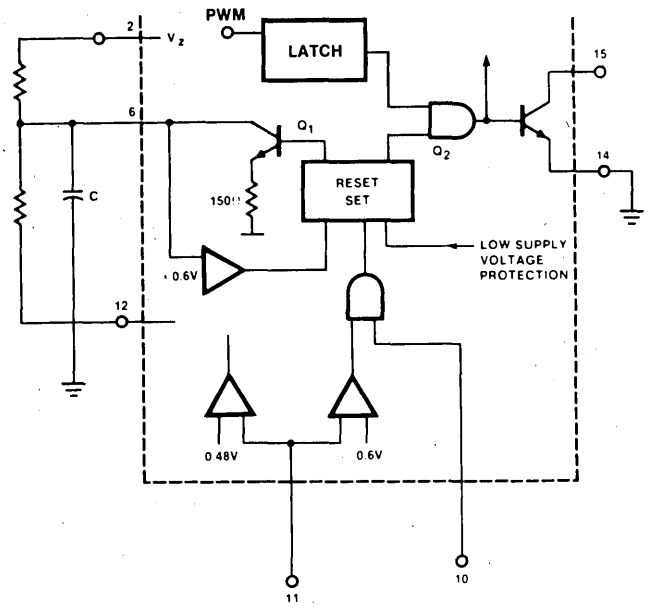


Figure 12

START/STOP CIRCUIT

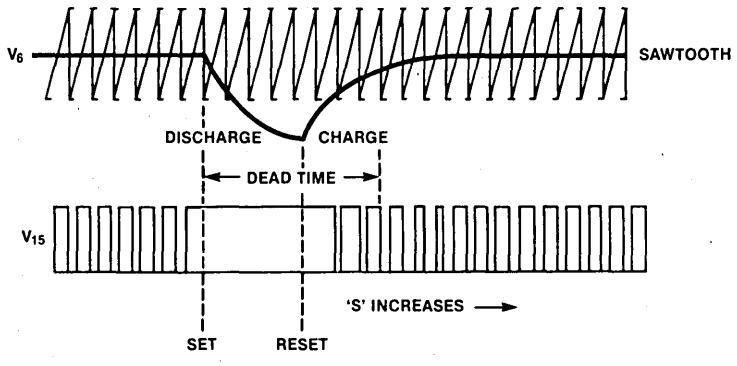


Figure 13

SWITCHED MODE POWER SUPPLY CONTROL CIRCUIT NE/SE5560

Remote On/Off Circuit (Pin 10)

In systems where two or more power supplies are used, it is often necessary to switch these supplies on and off in a sequential way. Furthermore, there are many applications in which a supply must be switched by a logical signal. This can be done via the TTL-compatible remote on/off input on pin 10. The output pulse is inhibited for levels below 0.8V. The output of the IC is no longer blocked when the remote on/off input is left floating or when a voltage >2V is applied. Starting up occurs via the slow-start circuit.

The Output Stage

The output stage of the NE5560 contains a bistable, a push-pull driven output transistor, and a gate, as indicated in Figure 14. The bistable is set by the flyback of the sawtooth. Resetting occurs by a signal either from the PWM or the current limit circuit. With this configuration, it is assured that the output is switched only once per period, thus prohibiting double pulsing. The collector and emitter of the output transistor are connected to respectively pin 15 and pin 14, allowing for normal or inverted output pulses. An internally grounded emitter would cause untolerable voltage spikes over the bonding wire, especially at high output currents.

This current capability of the output transistor is 40mA peak for $V_{CE} \alpha$ 0.4V. An internal clamping diode to the supply voltage protects the collector against overvoltages. The maximum voltage at the emitter (pin 14) must not exceed +5V. A gate, activated by one of the set or reset pulses, or by a command from the start-stop circuit will immediately switch-off the output transistor by short-circuiting its base. The external inhibitor (pin 13) operates also via this base.

Demagnetization Sense

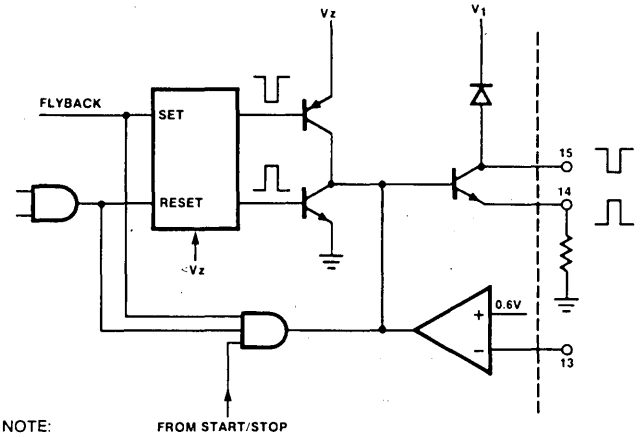
As indicated in Figure 14, the output of this NPN comparator will block the output pulse, when a voltage above 0.6V is applied to pin 13. A specific application for this function is to prevent saturation of forward converter transformers. This is indicated in Figure 15.

Feed-Forward (Pin 16)

The basic formula for a forward converter is

$$V_{OUT} = \frac{\delta V_{in}}{n} \text{ (n = transformer ratio)}$$

OUTPUT STAGE



NOTE:
The signal V_{13} can be derived from the demagnetizing winding in a forward converter.

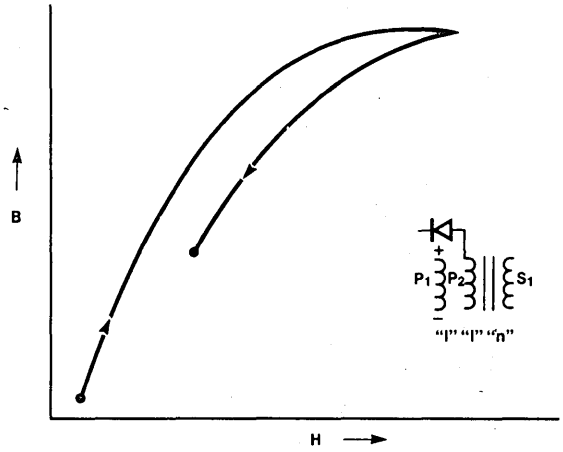


Figure 14

OUTPUT STAGE INHIBIT

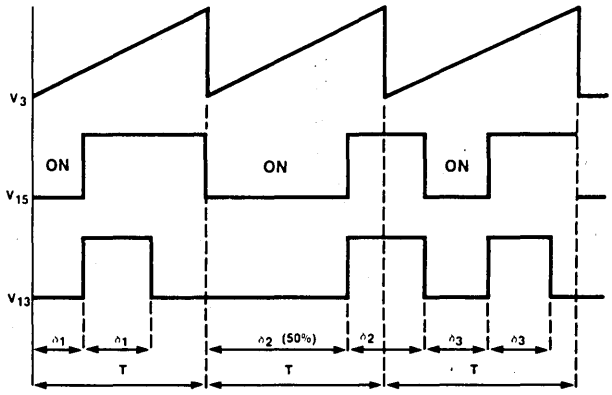


Figure 15

LINEAR

Signetics

This means that in order to keep V_{OUT} at a constant value, the duty cycle δ must be made inversely proportional to the input voltage. A preregulation (feed-forward) with the function $\delta \sim 1/V_{in}$ can ease the feedback-loop design.

This loop now only has to regulate for load variations, which require only a low feedback gain in the normal operation area. The transformer of a forward converter must be designed in such a way that it does not saturate, even under transient conditions, where the maximum inductance is determined by $\delta_{max} \times V_{IN}$ max. A regulation of $\delta_{max} \sim 1/V_{IN}$ will allow for a considerable reduction or simplification of the transformer. The function of $\delta \sim 1/V_{IN}$ can be realized by using pin 16 of the NE5560.

Figure 16 shows the electrical realization. When the voltage at pin 16 exceeds the stabilized voltage V_Z (pin 2), it will increase the charging current for the timing capacitor on pin 8.

The operating frequency is not affected, because the upper trip level for sawtooth increases also. Note that the δ_{max} voltage on pin 6 remains constant because it is set via V_Z. Figure 17 visualizes the effect on δ_{max} and the normal operating duty cycle δ. For V16 = 2xV_Z these duty cycles have halved. The graph for $\delta = f(V16)$ is given in Figure 18.

NE/SE5560 Push-Pull Regulator

This application describes the use of the Signetics NE/SE5560 adapted to function as a push-pull switched mode regulator, as shown in Figures 19 and 20.

Input voltage range is +12 to +18V for a nominal output of +30 and −30V at a maximum load current of 1A with an average efficiency of 81%.

Features include feed forward input compensation, cycle-to-cycle drive current protection and other voltage sensing, line (to positive output) regulation <1% for an input range of +13 to +18V and load regulation to positive output of <3% for $\Delta I_L(+)$ of 0.1 to 1 Amp.

The main pulse width modulator operates to 48 kHz with power switching at 24 kHz.

EXTERNAL δ MAXIMUM CONTROL

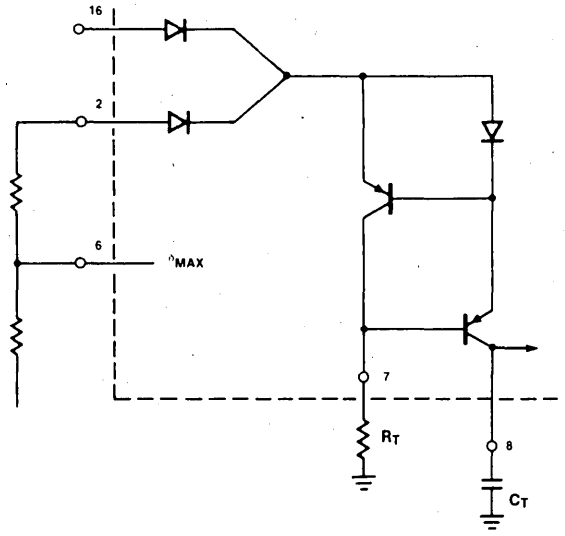


Figure 16

FEED FORWARD CIRCUITRY

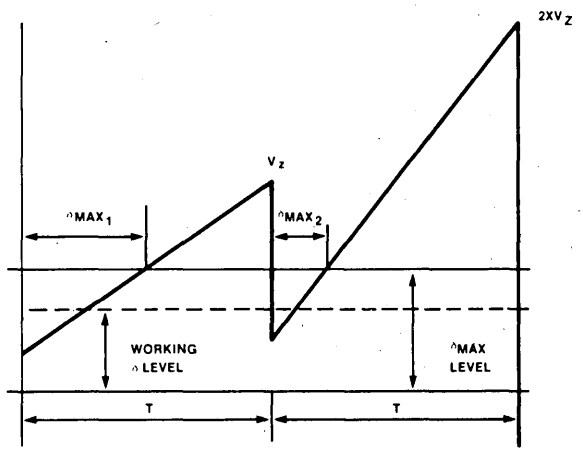


Figure 17

FEED-FORWARD REGULATION

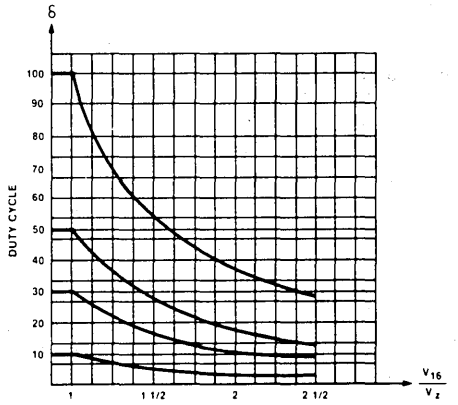


Figure 18

10-BIT HIGH-SPEED MULTIPLYING D/A CONVERTER NE5410/SE5410

Preliminary

DESCRIPTION

The NE5410/SE5410 are 10-Bit Multiplying Digital-to-Analog Converters pin-and-function compatible with the industry-standard MC3410, but with improved performance. These are capable of high-speed performance, and are used as general-purpose building blocks in cost-effective D/A systems.

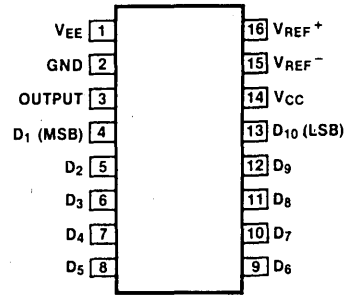
The NE/SE5410 provides complete 10-bit accuracy and differential nonlinearity over temperature, and a wide compliance voltage range. Segmented current sources, in conjunction with an R/2R DAC provides the binary weighted currents. The output buffer amplifier and voltage reference have been omitted to allow greater speed, lower cost, and maximum user flexibility.

FEATURES

- **Pin-and-function compatible with MC3410**
- **10-bit resolution and accuracy (±0.05%)**
- **Guaranteed differential non-linearity over temperature**
- **Wide compliance voltage range— −2.5 to +2.5V**
- **Fast settling time—250ns typical**
- **Digital inputs are TTL and CMOS compatible**
- **High-speed multiplying input slew rate —20mA/μs**
- **Reference amplifier internally compensated**
- **Standard supply voltages +5V and −15V**

PIN CONFIGURATION

N, F PACKAGES



TOP VIEW

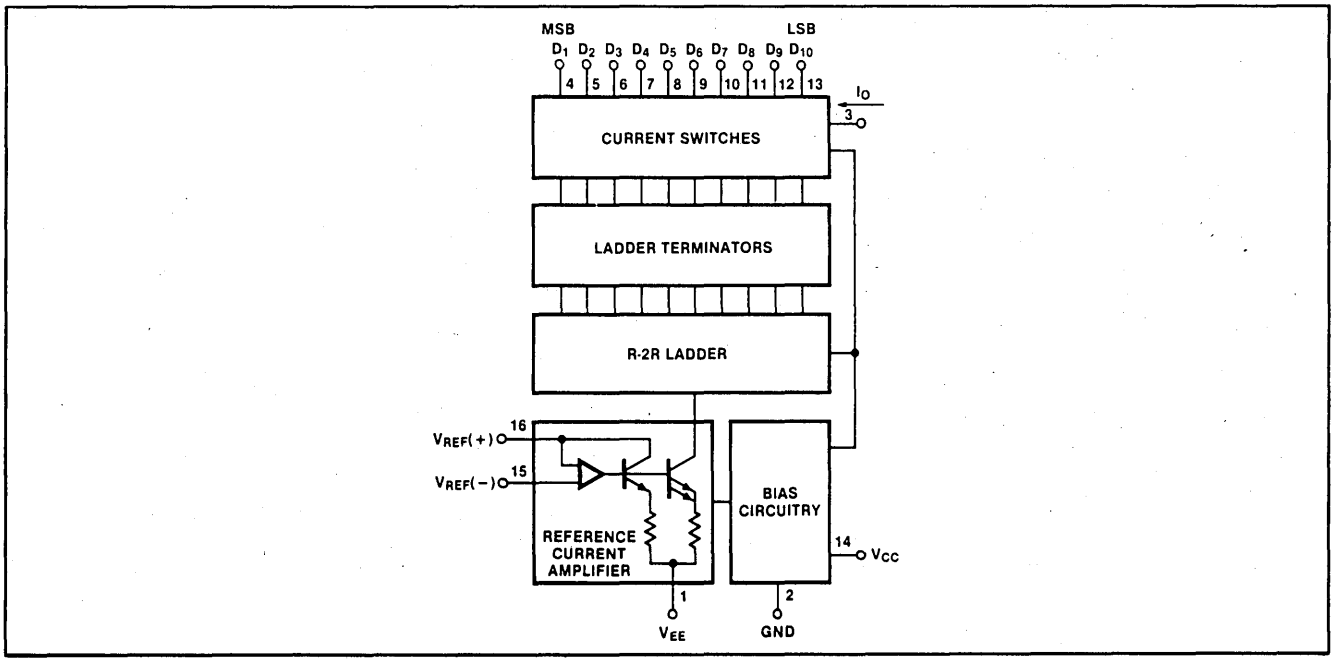
APPLICATIONS

- **Successive approximation A/D converters**
- **High-speed, automatic test equipment**
- **High-speed modems**
- **Waveform generators**
- **CRT displays**
- **Strip CHART and X-Y plotters**
- **Programmable power supplies**
- **Programmable gain and attenuation**

ABSOLUTE MAXIMUM RATINGS T_A = +25°C unless otherwise noted

SYMBOL	AND PARAMETER	RATING	UNIT
V_{CC}	Power Supply	+7.0	Vdc
V_{EE}		−18	Vdc
V_I	Digital Input Voltage	+15	Vdc
V_O	Applied Output Voltage	+4, −5.0	Vdc
$I_{REF(16)}$	Reference Current	2.5	mA
V_{REF}	Reference Amplifier Inputs	V_{CC}, V_{EE}	Vdc
$V_{REF(D)}$	Reference Amplifier Differential Inputs	0.7	Vdc
T_A	Operating Temperature Range		
	SE5410	−55 to +125	°C
	NE5410	0 to +70	°C
T_J	Junction Temperature		
	Ceramic Package	+175	°C
	Plastic Package	+150	°C

BLOCK DIAGRAM



10-BIT HIGH-SPEED MULTIPLYING D/A CONVERTER NE5410/SE5410

Preliminary

DC ELECTRICAL CHARACTERISTICS

$V_{CC} = +5.0Vdc$, $V_{EE} = -15Vdc$, $\frac{V_{REF}}{R16} = 2.0mA$, all digital inputs at high logic level.

SE5410: $T_A = -55°C$ to $+125°C$, NE5410 Series: $T_A = 0°C$ to $+70°C$

SYMBOL AND PARAMETER		TEST CONDITIONS	NE/SE5410			UNIT
			Min	Typ	Max	
E_r	Relative accuracy (Error relative to full scale I_O)	Over temperature		± 1/4	± 1/2	LSB
	Differential non-linearity '	Over temperature		± 1/4	± 1/2	LSB
t_s	Settling time to within ± ½ LSB (all bits low to high)	$T_A = 25°C$		250		ns
t_{PLH} t_{PHL}	Propagation delay time			35 20		ns
TCI_O	Output full scale current drift			20	40	ppm/°C
V_{IH}	Digital Input Logic Levels (All bits) High Level, Logic "1" Low Level, Logic "0"		2.0		 0.8	Vdc
I_{IH} I_{IL}	Digital Input Current (All bits) High Level, $V_{IH} = 5.5V$ Low Level, $V_{IL} = 0.8V$				20 −20	μA
$I_{REF(15)}$	Reference Input Bias Current (Pin 15)			−1.0	−5.0	μA
I_{OH}	Output Current (All bits high)	$V_{REF} = 2.000V$, $R_{16} = 1000\Omega$	3.937	3.996	4.054	mA
I_{OL}	Output Current (All bits low)	$T_A = 25°C$		0	0.4	μA
V_O	Output Voltage Compliance	$T_A = 25°C$ $E_r < 0.05\%$ relative to full scale			−2.5 +2.5	Vdc
SR I_{REF}	Reference Amplifier Slew Rate			20		mA/μs
ST I_{REF}	Reference Amplifier Settling Time	0 to 4.0mA, ± 0.1%		2.0		μs
PSRR(−)	Output Current Power Supply Sensitivity			0.003	0.01	%/%
C_O	Output Capacitance	$V_O = 0$		25		pF
C_I	Digital Input Capacitance (All bits high)			4.0		pF
I_{CC} I_{EE}	Power Supply Current (All bits low)			+2 −12	+4 −18	mA
V_{CC} V_{EE}	Power Supply Voltage Range	$T_A = 25°C$ $V_O = 0$	+4.75 −14.25	+5.0 −15	+5.25 −15.75	Vdc
	Power Consumption			190	300	mW

Preliminary

TYPICAL PERFORMANCE CHARACTERISTICS

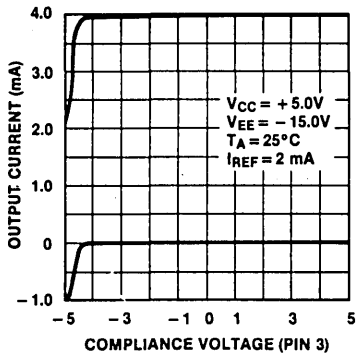


Figure 1. Output Current vs. Output Compliance Voltage

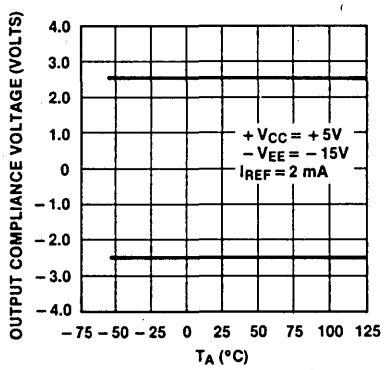


Figure 2. Maximum Output Compliance Voltage vs. Temperature

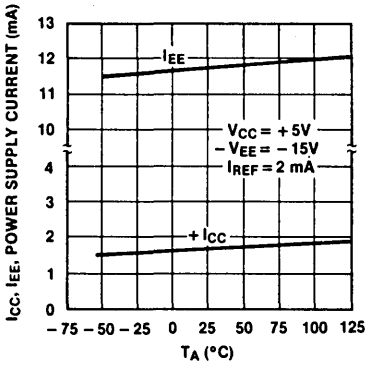


Figure 3. Power Supply Currents vs. Temperature

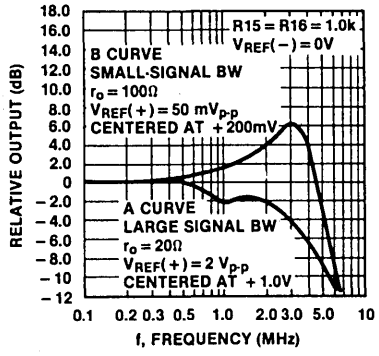


Figure 4. Reference Amplifier Frequency Response

10-BIT HIGH-SPEED MULTIPLYING D/A CONVERTER NE5410/SE5410

Preliminary

CIRCUIT DESCRIPTION

The NE5410 consists of four segment current sources which generate the 2 Most Significant Bits (MSBs), and an R/2R DAC implemented with ion implanted resistors for scaling the remaining 8 Least Significant Bits (LSBs). (See Figure 5.) This approach provides complete 10-bit accuracy without trimming.

The individual bit currents are switched ON or OFF by fully differential current switches. The switches use current steering for speed.

An on-chip high-slew reference current amplifier drives the R/2R ladder and segment decoder. The currents are scaled in such a way that, with all bits on, the maximum output current is two times 1023/1024 of the reference amplifier current, or nominally 3.996mA for a 2.000mA reference input current. The reference amplifier allows the user to provide a voltage input: Out-board resistor R16 (see Figure 6) converts this voltage to a usable current. A current mirror doubles this reference current and feeds it to the segment decoder and resistor ladder. Thus, for a reference voltage of 2.0 Volts and a 1kΩ resistor tied to Pin 16, the full scale current is approximately 4.0mA. This relationship will remain regardless of the reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 6a. For negative reference voltage inputs, or for bipolar reference voltage inputs in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. For a negative reference input, R16 should be grounded (Figure 6b). In addition, the negative voltage reference must be at least 3V above the V_{EE} supply voltage for best operation. Bipolar input signals may be handled by connecting R16 to a positive voltage equal to the peak positive input level at Pin 15.

When a dc reference voltage is used, capacitive bypass to ground is recommended. The 5V logic supply is not recommended as a reference voltage. If a well regulated 5.0V supply, which drives logic, is to be used as the reference, R16 should be decoupled by connecting it to the +5.0V logic supply through another resistor and bypassing the junction of the two resistors with a 0.1μF capacitor to ground.

The reference amplifier is internally compensated with a 10pF feed-forward capacitor, which gives it its high slew rate and fast settling time. Proper phase margin is maintained with all possible values of R16 and reference voltages which supply

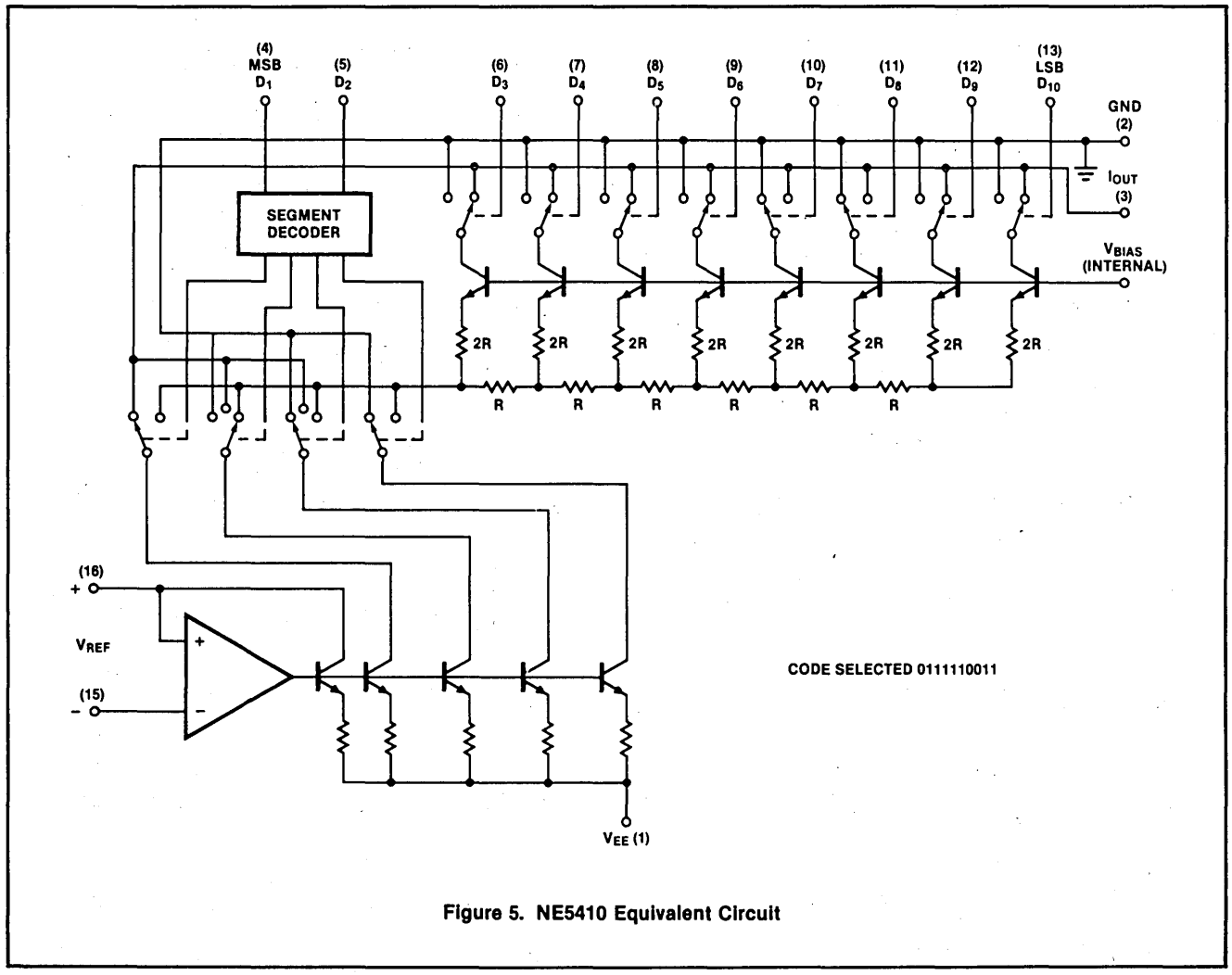
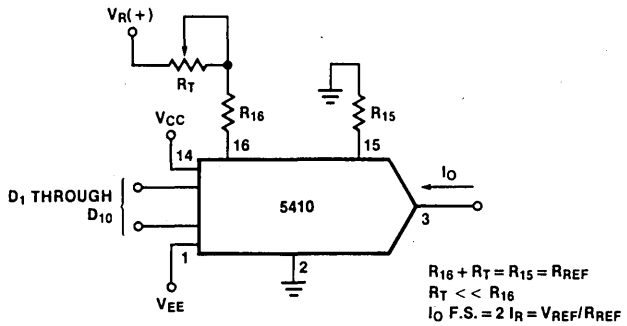
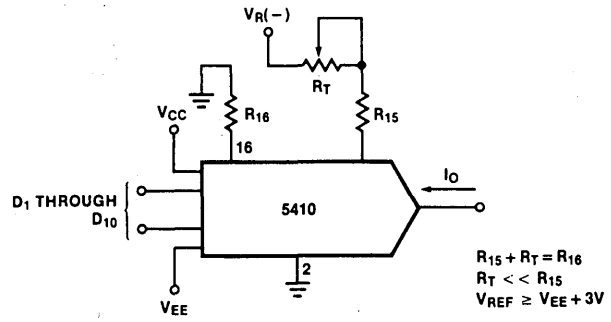


Figure 5. NE5410 Equivalent Circuit

Preliminary



a) POSITIVE REFERENCE VOLTAGE



b) NEGATIVE REFERENCE VOLTAGE

Figure 6. Basic Connections

2.0mA reference current into Pin 16. The reference current can also be supplied by a high impedance current source of 2.0mA. As R16 increases, the bandwidth of the amplifier decreases slightly and settling time increases. For a current source with a dynamic output impedance of 1.0MΩ, the bandwidth of the reference amplifier is approximately half what it is in the case of R16 = 1.0kΩ, and settling time is ≈10μs. The reference amplifier phase margin decreases as the current source value decreases in the case of a current source reference, so that the minimum reference current supplied from a current source is 0.5mA for stability.

OUTPUT VOLTAGE COMPLIANCE

The output voltage compliance ranges from −2.5 to +2.5V. As shown in Figure 1, this compliance range is nearly constant over temperature. At the temperature extremes, however, the compliance voltage may be reduced if $-V_{EE} > -15V$.

ACCURACY

Absolute accuracy is a measure of each output current level with respect to its intended value. It is dependent upon relative accuracy and full scale current drift. Relative accuracy, or linearity, is the measure of each output current with respect to its intended fraction of the full scale current. The relative accuracy of the NE5410 is fairly constant over temperature due to the excellent temperature tracking, of the implanted resistors. The full scale current from the reference amplifier may drift with temperature causing a change in the absolute accuracy. However, the NE5410 has a low full scale current drift with temperature.

The SE5410 and the NE5410 are accurate to within ± 1/2 LSB at 25°C with a reference current of 2.0mA on Pin 16.

MONOTONICITY

The NE5410 and SE5410 are guaranteed monotonic over temperature. This means that for every increase in the input digital code, the output current either remains the same or increases but never decreases. In the multiplying mode, where reference input current will vary, monotonicity can be assured if the reference input current remains above 0.5mA.

10-BIT HIGH-SPEED MULTIPLYING D/A CONVERTER NE5410/SE5410

Preliminary

SETTLING TIME

The worst case switching condition occurs when all bits are switched "on," which corresponds to a low-to-high transition for all bits. This time is typically 250ns for the output to settle to within ± 1/2 LSB for 10-bit accuracy, and 200ns for 8-bit accuracy. The turn-off time is typically 120ns. These times apply when the output swing is limited to a small (<0.7 Volt) swing and the external output capacitance is under 25pF.

The major carry (MSB off-to-on, all others on-to-off) settles in approximately the same time as when all bits are switched off-to-on.

If a load resistor of 625 Ohms is connected to ground, allowing the output to swing to −2.5 Volts, the settling time increases to 1.5μs.

Extra care must be taken in board layout as this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100μF supply bypassing, and minimum scope lead length are all necessary.

A typical test set-up for measuring settling time is shown in Figure 7. The same set-up for the most part can be used to measure the slew rate of the reference amplifier (Figure 9) by tying all data bits high, pulsing the voltage reference input between 0 and 2V, and using a 20Ω load resistor R_L.

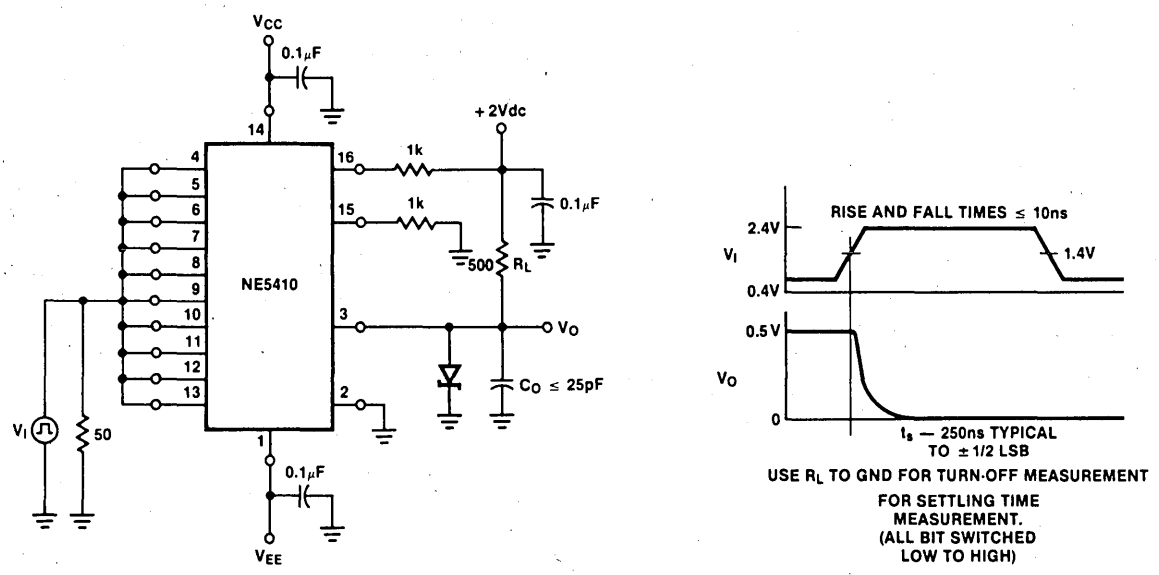


Figure 7. Settling Time

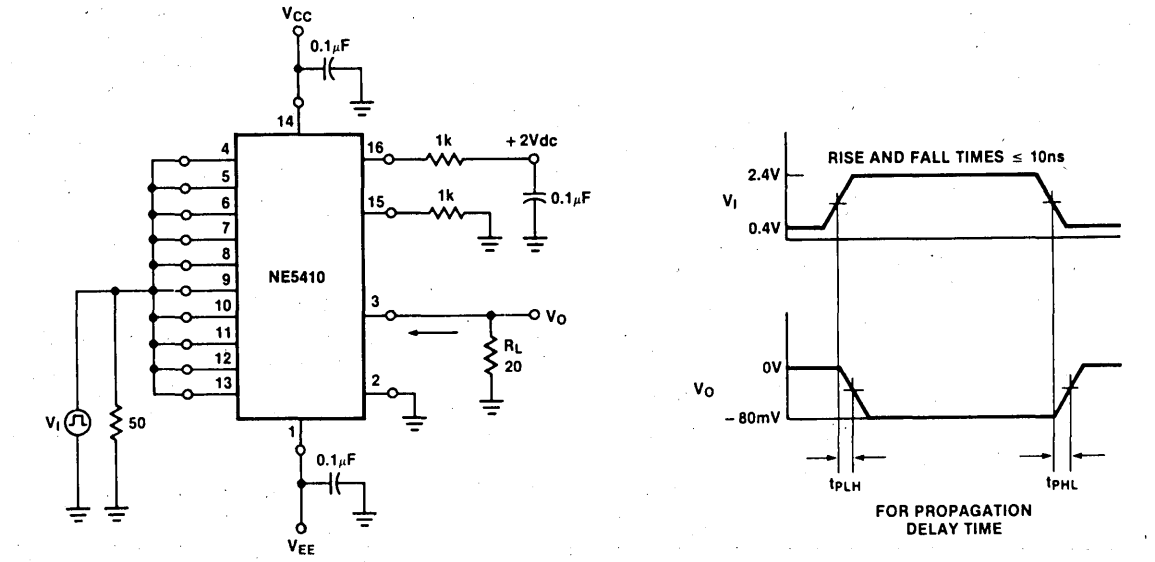


Figure 8. Propagation Delay Time

Preliminary

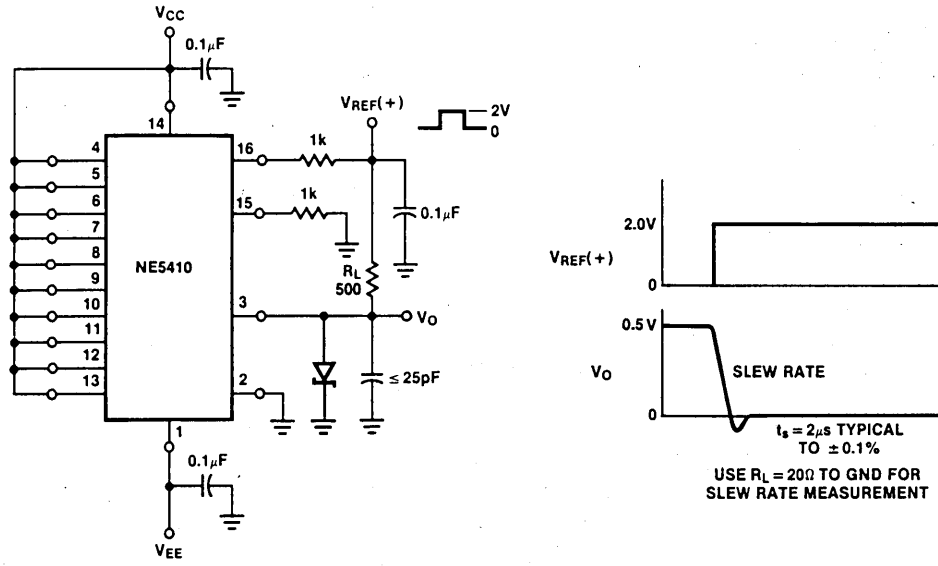
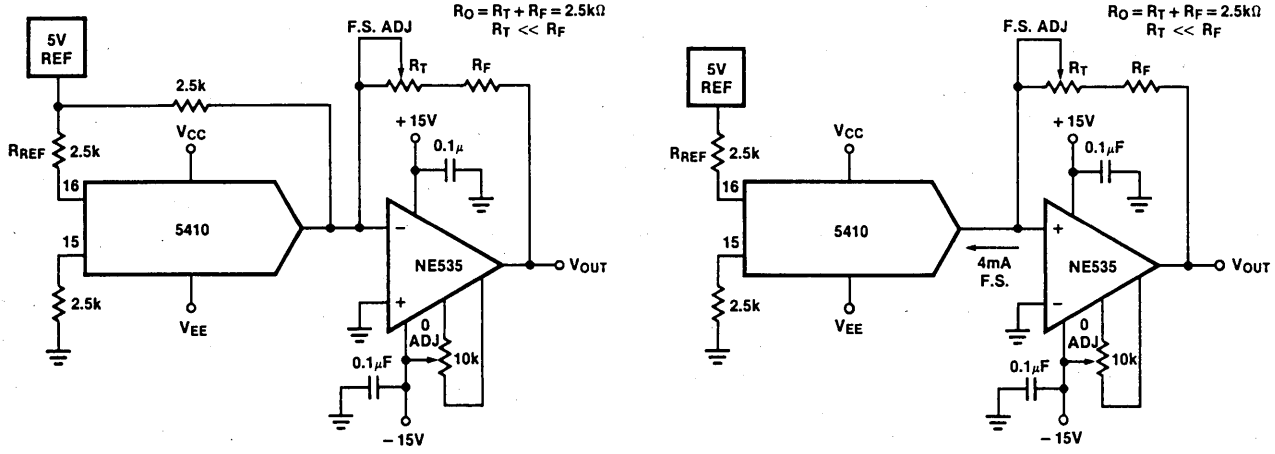


Figure 9. Reference Amplifier Settling Time and Slew Rate



a) Bipolar Output (-10 to +10V)

b) Unipolar Positive Output (0-10V)

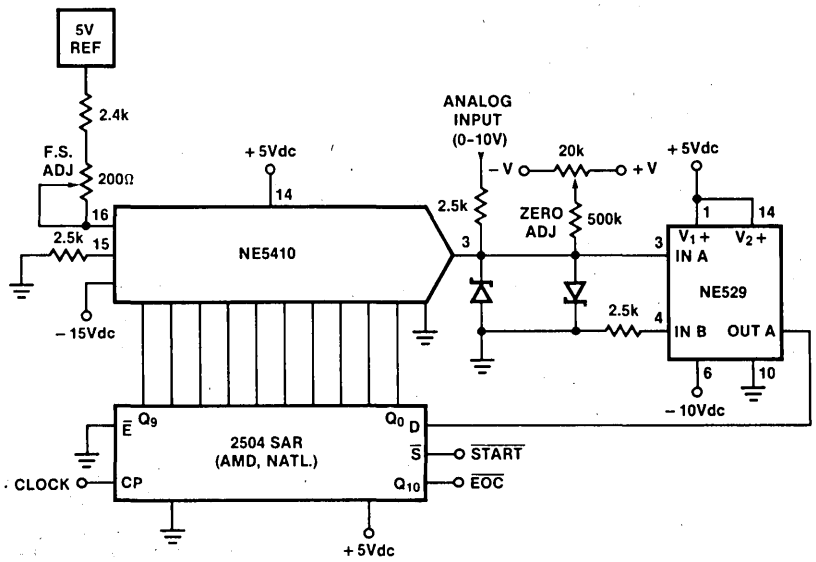
Figure 10. Voltage Output Circuits

LINEAR

Signetics

10-BIT HIGH-SPEED MULTIPLYING D/A CONVERTER NE5410/SE5410

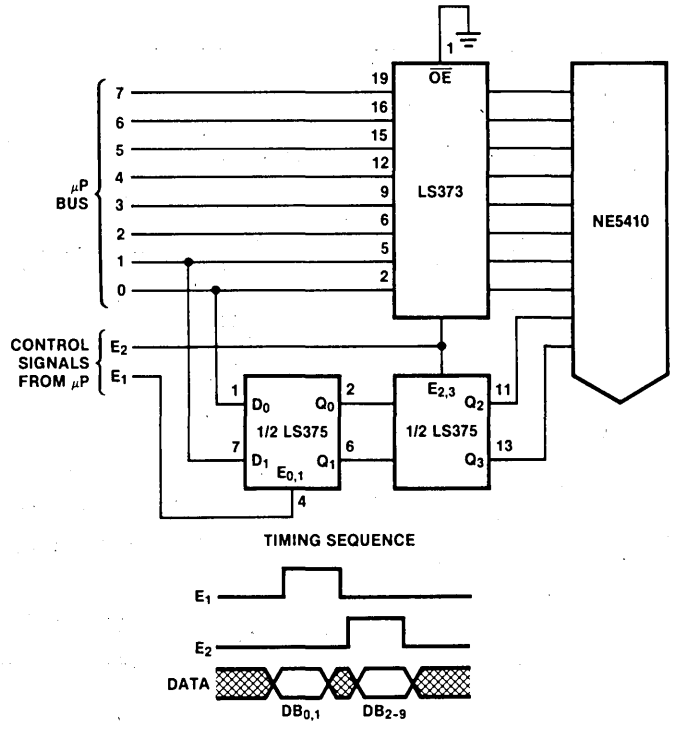
Preliminary



10-BIT CONVERSION TIME = 3.3μs WITH 3MHz CLOCK.

THIS CONVERTER USES A 2504 12-BIT SUCCESSIVE APPROXIMATION REGISTER IN THE SHORT CYCLE OPERATING MODE WHERE THE END OF CONVERSION SIGNAL IS TAKEN FROM THE FIRST UNUSED BIT OF THE SAR (Q_{10}).

Figure 11. Successive Approximation A/D Converter



WITH THIS DOUBLE LATCH TECHNIQUE, VALID DATA WILL BE LATCHED TO THE DAC UNTIL UPDATED WITH THE E_2 PULSE. TIMING WILL DEPEND ON THE PROCESSOR USED.

Figure 12. 8-Bit μP Bus Interface

10-BIT HIGH-SPEED MULTIPLYING D/A CONVERTER NE5410/SE5410

Preliminary

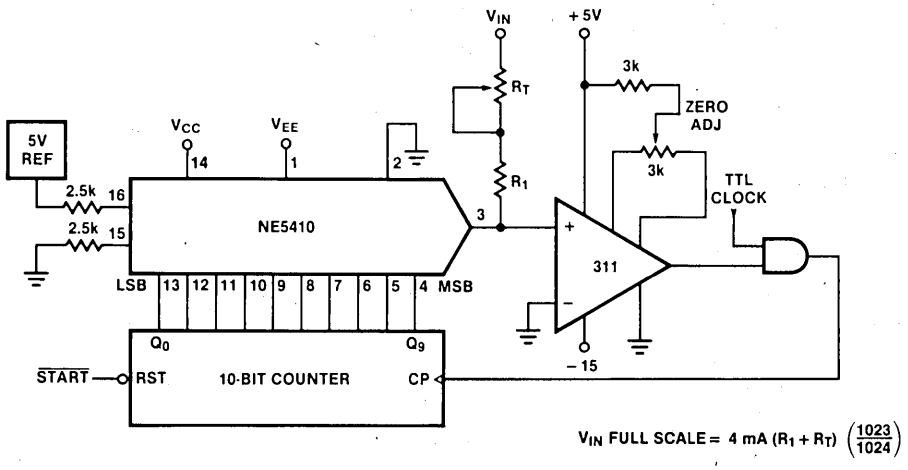


Figure 13. Staircase A/D

NE5410 TERMINOLOGY

RELATIVE ACCURACY — Maximum output deviation from the straight line connecting zero and full scale, expressed as a percentage of full scale.

DIFFERENTIAL NON-LINEARITY — The deviation of a measured step from the ideal difference expressed in LSB.

MONOTONICITY — For every increase in the input digital word, the output current either remains the same or increases.

SETTLING TIME — The elapsed time from the input transition until the output has settled within an error band about its final value (to 0.05% of its final value).

OUTPUT FULL SCALE CURRENT DRIFT— The average change in full scale current between 25°C and either temperature extreme, expressed in parts per million of full scale per degree C.

REFERENCE AMPLIFIER SLEW RATE — The maximum rate of change of the full scale output current expressed in milliamperes per microsecond.

OUTPUT VOLTAGE COMPLIANCE — The maximum voltage that can be applied to the output pin so that the specified change in output current is not exceeded.

POWER SUPPLY SENSITIVITY — The change in full scale current caused by a change in V_{EE}, expressed as a percent of full scale current per percent change in V_{EE}.

BIFET Products
from Texas Instruments

3-pin JFET-input voltage follower
Types TL068I, TL068C

Features

- 3-lead LP (TO-92) package
- Maximum quiescent supply current . . . 250 μA
- Wide input/output voltage range
- Low input bias currents
- Output short-circuit protection
- High impedance JFET input stage
- Internal frequency compensation
- Latch-up free operation.

Description

The TL068 is a low power JFET-input unity gain amplifier featuring high input impedance (10^{12} ohms typical), wide bandwidth (1MHz), and a low input bias current (30 pA typical). A current sourcing load, such as a pull up resistor (see fig. 1) is required for circuit operation.

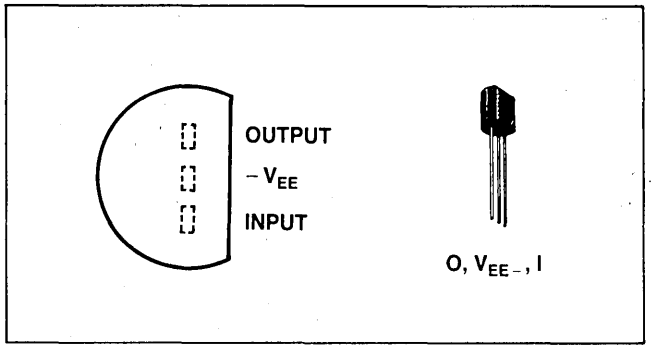
The TL068C is characterized for operation from 0°C to 70°C. The TL068I is characterized for operation from −25°C to 85°C.

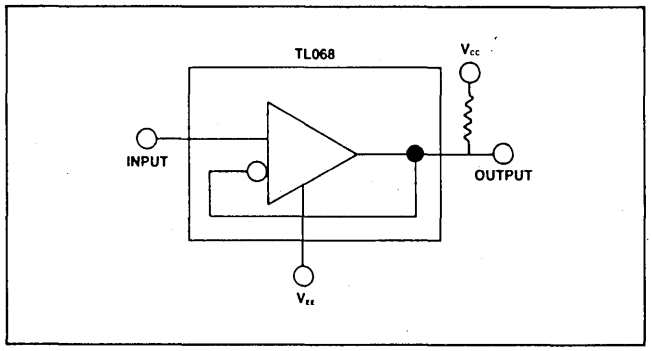
Absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	TL068
Voltage from output to $-V_{EE}$	36V
Voltage from input to $-V_{EE}$	36V
Voltage from input to output	30V
Duration of short circuit (see Note 1)	unlimited
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	775mW
Operating free-air temperature range . . . TL068C . . . TL068I	0°C to 70°C −25°C to 85°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds	260°C

Notes: 1. The output may be shorted to any point as long as the voltage from output to $-V_{EE}$ doesn't exceed 36V. Temperature and or $-V_{EE}$ must be limited to insure that dissipation rating is not exceeded.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Table.

TL068I, TL068C . . . LP
SILECT† PACKAGE





(FIG.1)

Dissipation derating table above 25°C

PACKAGE	POWER RATING	DERATING FACTOR
LP	775 mW	6.3 mW/°C

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225612 • DALLAS, TEXAS 75265

BIFET Products
from Texas Instruments

JFET-input operational amplifiers Types TL066I, TL066C, TL066AC, TL066BC adjustable low-power

Features

4 Devices cover commercial and industrial temperature ranges

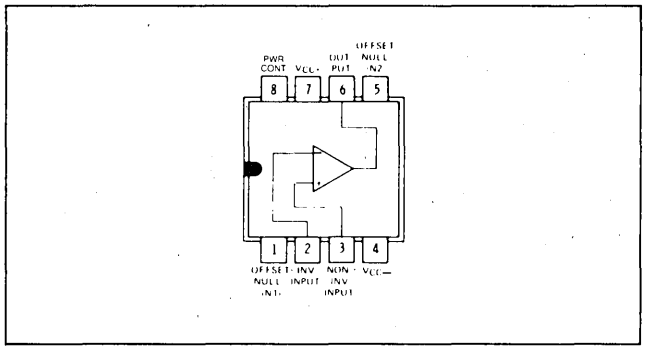
- Very low, adjustable ("programmable") power consumption
- Adjustable supply current ... 5 to 200 μA
- Very low input bias and offset currents
- Wide supply range ... ± 1.2 V to ± 18V
- Wide common-mode and differential voltage ranges
- Output short-circuit protection
- High input impedance ... JFET-input stage
- Typical unity-gain bandwidth ... 1 MHz (100 kHz at 25 μW)
- High slew rate ... 3.5 V / μs typ
- Internal frequency compensation
- Latch-up-free operation

Description

The TL066, TL066A, and TL066B are JFET-input operational amplifiers similar to the TL061 with the additional feature of being power-adjustable. They feature very low input offset and bias currents, high input impedance, wide bandwidth, and high slew rate. The power-control feature permits the amplifiers to be adjusted to require as little as 25 microwatts of power. This type of amplifier, which provides for changing several characteristics by varying one external element, is sometimes referred to as being "programmable". The JFET input stage combined with the adjustable-low-power feature results in superior bandwidth and slew rate performance compared to low-power bipolar-input devices.

The TL066I is characterized for operation from −25°C to 85°C, and the TL066C, TL066AC, and TL066BC are characterized for operation from 0°C to 70°C.

TL066, TL066A, TL066B
JG OR P DUAL-IN-LINE
PACKAGE (TOP VIEW)



Absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL066I	TL066C TL066AC TL066BC
Supply voltage, $V_{CC}+$ (see Note 1)		18V	18V
Supply voltage, $V_{CC}-$ (see Note 1)		−18V	−18V
Differential input voltage (see Note 2)		±30V	±30V
Input voltage (see Notes 1 and 3)		±15V	±15V
Voltage between power-control terminal and $V_{CC}-$		±0.5V	±0.5V
Duration of output short circuit (see Note 4)		Unlimited	Unlimited
Operating free-air temperature range		−25°C to 85°C	0°C to 70°C
Storage temperature range		−65°C to 150°C	−65° to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds	JG Package	300°C	300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds	P Package	260°C	260°C

Notes: 1. All voltage values, except differential voltages, are with respect to the midpoint between $V_{CC}+$ and $V_{CC}-$.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

Dissipation derating table above 25°C

PACKAGE	POWER RATING	DERATING FACTOR
JG (Glass-Mounted Chip)	825 mW	6.6 mW/°C
P	1000 mW	8.0 mW/°C

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225612 • DALLAS, TEXAS 75265

BIFET Products
from Texas Instruments

JFET-input operational amplifiers
Types TL087, TL088, TL287, TL288

Features

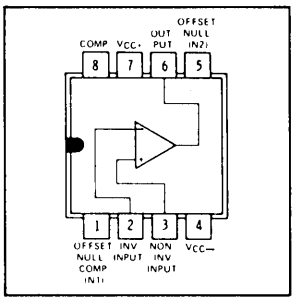
- Low input offset voltage . . . 0.5mV max for TL087 & TL287
  . . . 3.0mV max for TL088 & TL288
- Low power consumption
- Wide common-mode and differential voltage ranges
- Low input bias and offset currents
- Output short-circuit protection
- High input impedance . . . JFET-input stage
- Internal frequency compensation
- Latch-up-free-operation
- High slew rate . . . 13 V / μs typ

Description

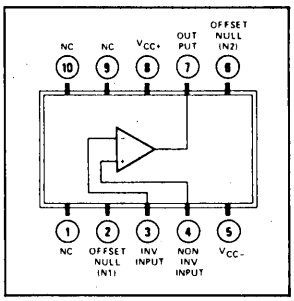
These JFET-input operational amplifiers incorporate well-matched high-voltage JFET and bipolar transistors in a monolithic integrated circuit. They feature low input offset voltage, high slew rate, low input bias and offset current, and low temperature coefficient of input offset voltage. Offset-voltage adjustment is provided for the TL087 and TL088.

Device types with an "M" suffix are characterized for operation over the full military temperature range of −55°C to 125°C, those with an "I" suffix are characterized for operation from −25°C to 85°C, and those with a "C" suffix are characterized for operation from 0°C to 70°C.

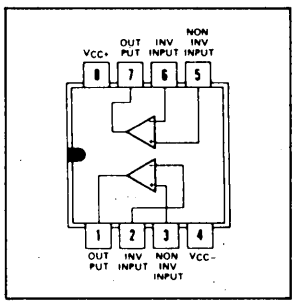
TL087, TL088
JG OR P DUAL-IN-LINE
PACKAGE (TOP VIEW)



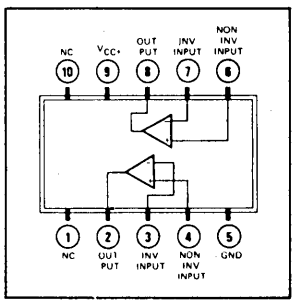
TL088
U FLAT PACKAGE
(TOP VIEW)



TL287, TL288
JG OR P DUAL-IN-LINE
PACKAGE (TOP VIEW)



TL288
U FLAT PACKAGE
(TOP VIEW)



Absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL088M TL288M	TL087I TL088I TL287I TL288I	TL087C TL088C TL287C TL288C
Supply voltage, $V_{CC}+$ (see Note 1)		18V	18V	18V
Supply voltage, $V_{CC}-$ (see Note 1)		−18V	−18V	−18V
Differential input voltage (see Note 2)		±30V	±30V	±30V
Input voltage (see Notes 1 and 3)		±15V	±15V	±15V
Duration of output short circuit (see Note 4)		Unlimited	Unlimited	Unlimited
Operating free-air temperature range		−55°C to 125°C	−25°C to 85°C	0°C to 70°C
Storage temperature range		−65°C to 150°C	−65°C to 150°C	−65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds	JG or U package	300°C	300°C	300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds	P package		260°C	260°C

Notes: 1. All voltage values, except differential voltages, are with respect to the midpoint between $V_{CC}+$ and $V_{CC}-$.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

Dissipation derating table above 25°C

PACKAGE	POWER RATING	DERATING FACTOR
JG (Alloy-Mounted Chip)	1050 mW	8.4 mW/°C
JG (Glass-Mounted Chip)	825 mW	6.6 mW/°C
P	1000 mW	8.0 mW°C
U	675 mW	5.4 mW/°C

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225612 • DALLAS, TEXAS 75265

BIFET Products
from Texas Instruments

Low-power JFET-input operational amplifiers
Types TL060, TL060A, TL061, TL061A, TL061B, TL062, TL062A, TL062B, TL064, TL064A, TL064B

Features

19 Devices cover commercial, industrial, and military temperature ranges

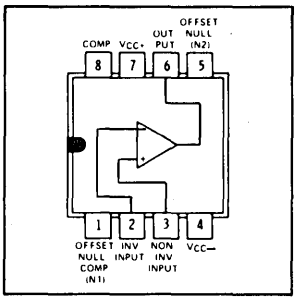
- Very low power consumption
- Typical supply current ... 200 μA
- Wide common-mode and differential voltage ranges
- Low input bias and offset currents
- Output short-circuit protection
- High input impedance ... JFET-input stage
- Internal frequency compensation
- Latch-up-free operation
- High slew rate ... 3.5V / μs typ

Description

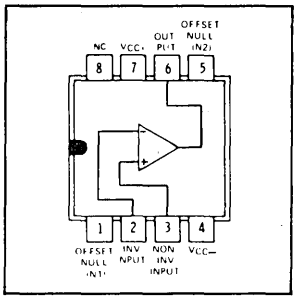
The JFET-input operational amplifiers of the TL061 series are designed as low-power versions of the TL081 series amplifiers. They feature high input impedance, wide bandwidth, high slew rate, and low input offset and bias currents. The TL061 series features the same terminal assignments as the TL071 and TL081 series. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit.

Device types with an "M" suffix are characterized for operation over the full military temperature range of −55°C to 125°C. Devices with an "I" suffix are characterized for operation from −25°C to 85°C, and those with a "C" suffix are characterized for operation from 0°C to 70°C.

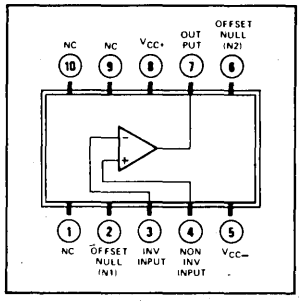
TL060, TL060A
JG OR P DUAL-IN-LINE
PACKAGE (TOP VIEW)



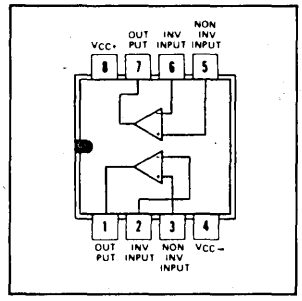
TL061, TL061A, TL061B
JG OR P DUAL-IN-LINE
PACKAGE (TOP VIEW)



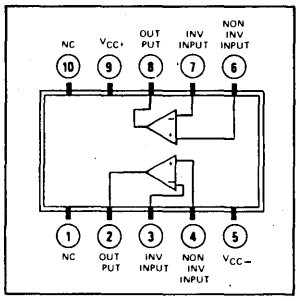
TL061
U FLAT PACKAGE
(TOP VIEW)



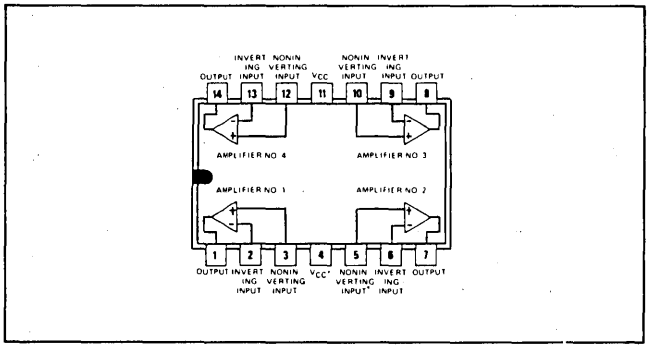
TL062, TL062A, TL062B
JG OR P DUAL-IN-LINE
PACKAGE (TOP VIEW)



TL062
U FLAT PACKAGE
(TOP VIEW)



TL064 . . . J, N, OR W PACKAGE
TL064A, TL064B . . . J OR N PACKAGE
(TOP VIEW)



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225612 • DALLAS, TEXAS 75265

JFET-input differential comparators with strobes Types TL311, TL311A

Features

- Fast response times
- Strobe capability
- Designed to replace LM311
- Common-mode input voltage range includes V_{CC}-
- N-channel JFET high-impedance input
- Can operate from single 5-V supply

Description

The TL311, and TL311A are high-speed voltage comparators. These devices use an N-channel JFET high-impedance input structure that extends the operating range of the common-mode input voltage to include the value of the $V_{CC}-$ supply. Designed for a wide variety of applications, the TL311, and TL311A can be operated over a wide range of supply voltage, including ± 15-volt supplies for operational amplifiers and single 5-volt supplies for logic systems. The uncommitted output transistor can drive loads referenced to ground, $V_{CC}+$, or $V_{CC}-$. Additionally, it is capable of driving loads that require switching up to 50 volts. Outputs can be wire-OR connected.

Offset balancing and strobe capability are available. If the strobe input is low (more negative than V_{IC} + 0.3 V), the output will be in the off state regardless of the differential input.

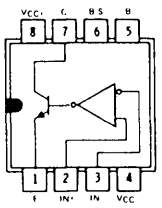
The TL 311 and TL311A are characterized for operation from 0°C to 70°C.

Absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		TL311, TL311A
Supply voltage, $V_{CC}+$ (see Note 1)		18V
Supply voltage, $V_{CC}-$ (see Note 1)		– 18V
Differential input voltage (see Note 2)		± 30V
Input voltage range (either input, see Notes 1 and 3)		$V_{CC}-$ to 15V
Voltage from emitter output to $V_{CC}-$		30V
Voltage from collector output to $V_{CC}-$		40V
Duration of output short circuit (see Note 4)		10 s
Operating free-air temperature range		0°C to 70°C
Storage temperature range		– 65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds	JG package	300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds	P package	260°C

Notes: 1. These voltage values are with respect to the midpoint between $V_{CC}+$ and $V_{CC}-$.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The input voltage must never be more positive than $V_{CC}+$ or 15 volts, whichever is less, or more negative than $V_{CC}-$.
4. The output may be shorted to ground or either power supply.

JG OR P DUAL-IN-LINE PACKAGE (TOP VIEW)



Dissipation derating table above 25°C

PACKAGE	POWER RATING	DERATING FACTOR
JG (Glass-Mounted Chip)	825 mW	6.6 mW/°C
P	1000 mW	8.0 mW/°C

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225612 • DALLAS, TEXAS 75265

BIFET Products
from Texas Instruments

Low-noise JFET-input operational amplifiers
Types TL070, TL070A, TL071, TL071A, TL071B, TL072, TL072A, TL072B, TL074, TL074A, TL074B, TL075

Features

20 Devices cover commercial, industrial, and military temperature ranges

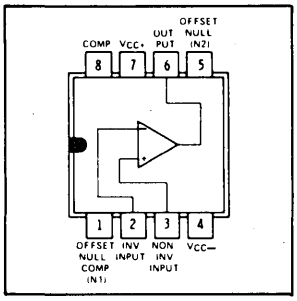
- Low noise ... V_n = 18 nV / $\sqrt{Hz}$ typ
- Low harmonic distortion ... 0.002% typ
- Wide common-mode and differential voltage ranges
- Low input bias and offset currents
- Output short-circuit protection
- High input impedance ... JFET-input stage
- Internal frequency compensation
- Latch-up-free operation
- High slew rate ... 13 V / μs typ

Description

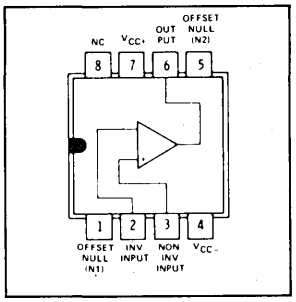
The JFET-input operational amplifiers of the TL071 series are designed as low-noise versions of the TL081 series amplifiers with low input bias and offset currents and fast slew rate. The low harmonic distortion and low noise make the TL071 series ideally suited as amplifiers for high-fidelity and audio preamplifier applications. Each amplifer features JFET inputs (for high input impedance) coupled with bipolar output stages, all integrated on a single monolithic chip.

Device types with an "M" suffix are characterized for operation over the full military temperature range of −55°C to 125°C. Devices with an "I" suffix are characterized for operation from −25°C to 85°C, and those with a "C" suffix are characterized for operation from 0°C to 70°C.

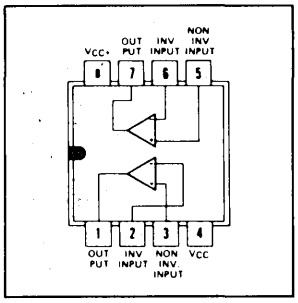
TL070, TL070A
JG OR P DUAL-IN-LINE
PACKAGE (TOP VIEW)



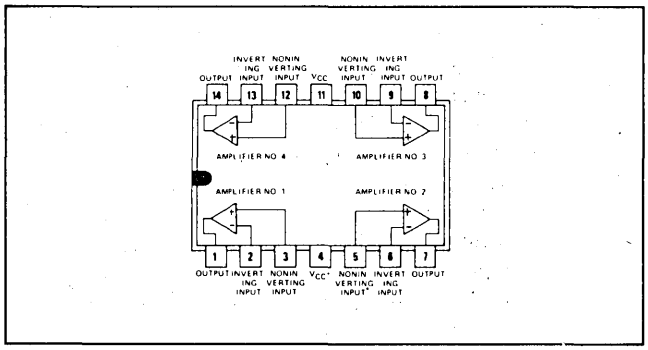
TL071, TL071A, TL071B
JG OR P DUAL-IN-LINE
PACKAGE (TOP VIEW)



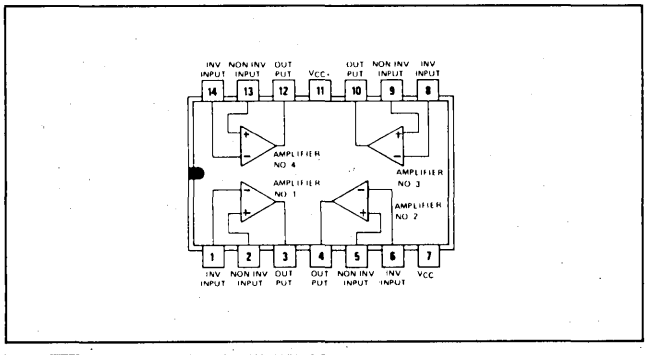
TL072, TL072A, TL072B
JG OR P DUAL-IN-LINE
PACKAGE (TOP VIEW)



TL074, TL074A, TL074B
J, N, OR W DUAL-IN-LINE
OR W PACKAGE (TOP VIEW)



TL075
N DUAL-IN-LINE
PACKAGE (TOP VIEW)



LINEAR

Texas Instruments

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225612 • DALLAS, TEXAS 75265

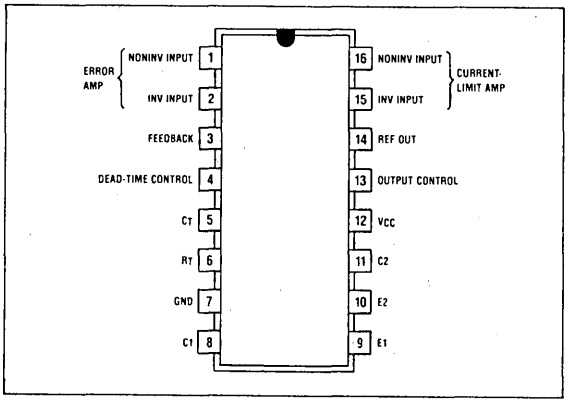
Voltage Regulators
from Texas Instruments

Pulse-Width-Modulation Controller Type TL593

Features

- Complete PWM Power Control Circuitry
- Uncommitted Outputs for 200 mA Sink or Source Capability
- Output Control Selects Single-Ended or Push-pull Operations
- Internal Under-Voltage Lockout Circuitry
- Internal Circuitry Prohibits Double Pulse at Either Output
- Variable Dead Time Provides Control Over Total Range
- Internal Regulator Provides a Stable (±1%) Reference Supply
- Circuit Architecture Provides Easy Synchronization

N PACKAGE CONNECTION DIAGRAM TOP VIEW

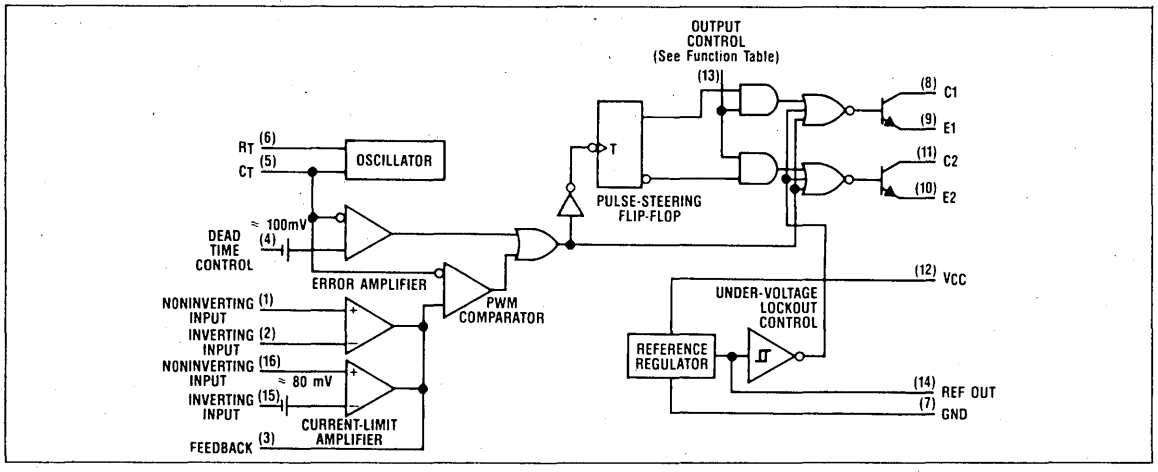


Description

The TL593 incorporates on a single monolithic chip all the functions required in the construction of a pulse-width-modulation control circuit. Designed primarily for power supply control, the TL593 contains an on-chip 5V regulator, an error amplifier, a current-limit sense amplifier, adjustable oscillator, dead-time control comparator, pulse-steering flip-flop, and output-control circuitry. The uncommitted output transistors provide either common-emitter or emitter-follower output capability. Push-pull or single-ended output operations may be selected through the output-control function.

The architecture of the TL593 prohibits the possibility of either output being pulsed twice during push-pull operation. The internal error amplifier exhibits a common-mode voltage range from −0.2 volt to VCC −2 volts. The current-limit sense amp has an 80 millivolt offset in series with the inverting input, eliminating the need for external offset components. The dead-time control comparator has a fixed offset that provides approximately 5% dead time unless externally altered. The on-chip oscillator may be by-passed by terminating RT (pin 6) to the reference output and providing a sawtooth input to CT (pin 5), or it may be used to drive the common TL593 circuitry and provide a sawtooth input for associated control circuitry in synchronous multiple-rail power supplies. The TL593 is designed to replace the TL493.

FUNCTION TABLE	
INPUT (OUTPUT-CONTROL)	OUTPUT FUNCTION
Grounded	Single-ended or parallel output
At Vref	Normal push-pull operation



TEXAS INSTRUMENTS
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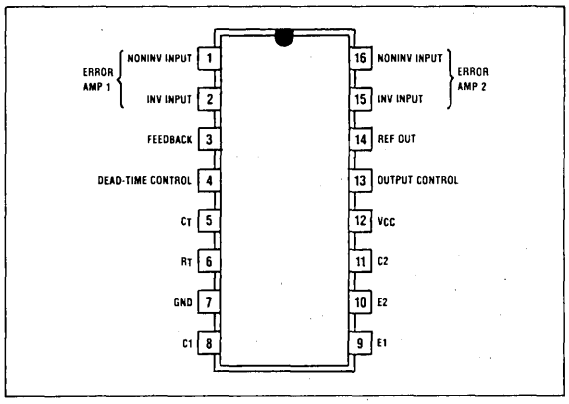
Pulse-Width-Modulation Controller Type TL594

Features

- Complete PWM Power Control Circuitry
- Uncommitted Outputs for 200-mA Sink or Source
- Output Control Selects Single-Ended or Push-Pull Operation
- Internal Circuitry Prohibits Double Pulse at Either Output
- Variable Dead-Time Provides Control Over Total Range
- Internal Regulator Provides a Stable 5-V Reference Supply (±1%)
- Circuit Architecture Provides Easy Synchronization
- Two Error Amplifiers for Greater Design Flexibility
- Internal Under-Voltage Lockout Circuitry

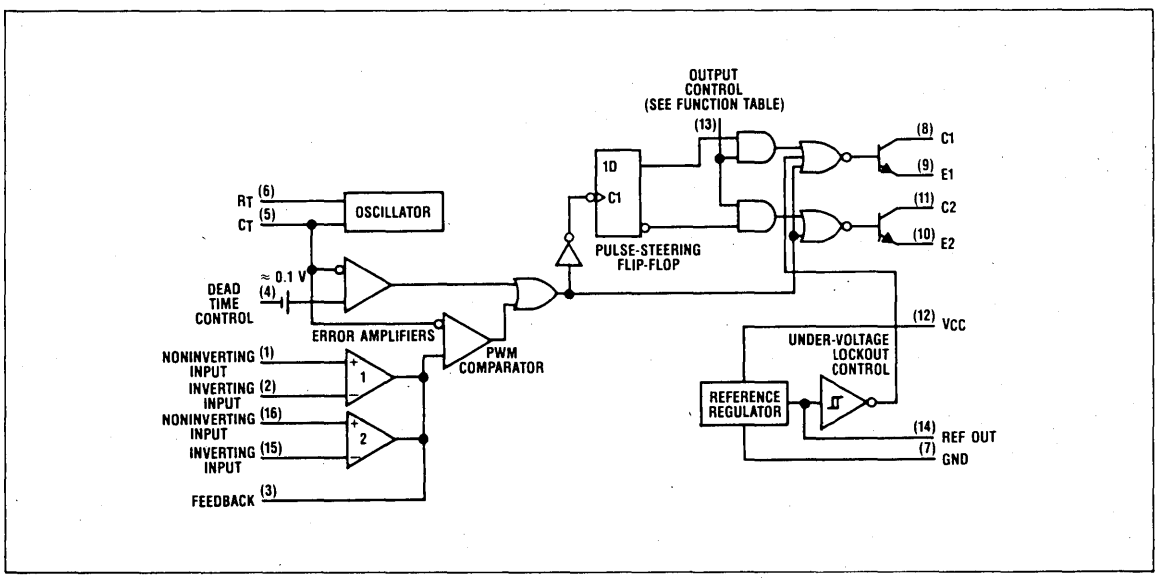
N OR J PACKAGE CONNECTION DIAGRAM TOP VIEW



Description

The TL594 provides the identical functions found in the TL593, except for the current-limit amplifier. The TL594 contains two error amplifiers for design flexibility. Both of these internal amplifiers exhibit a common-mode voltage range from −0.2 volt to VCC −2 volts. The rest of the functions, the on-board 5V reference, the adjustable oscillator, the dead-time comparator, pulse-steering flip-flop, output control circuitry, and the uncommitted output transistors are identical in both devices. The TL594 is designed to replace the TL494.

FUNCTION TABLE	
INPUT (OUTPUT-CONTROL)	OUTPUT FUNCTION
Grounded	Single-ended or parallel output
At Vref	Normal push-pull operation



Pulse-Width-Modulation Controller
Type TL595

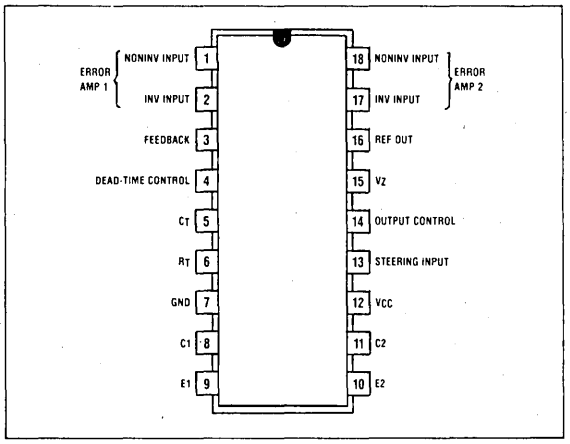
Features

- Complete PWM Power Control Circuitry
- Uncommitted Outputs for 200-mA Sink or Source
- Output Control Selects Single-Ended or Push-Pull Operation
- Internal Circuitry Prohibits Double Pulse at Either Output
- Variable Dead-Time Provides Control Over Total Range
- Internal Regulator Provides a Stable 5-V Reference Supply (±1%)
- Circuit Architecture Provides Easy Synchronization
- Two On-Board Error Amplifiers for Greater Design Flexibility
- Internal Under Voltage Lockout Circuitry
- On Chip 39-V Zener
- External Control of Output Steering

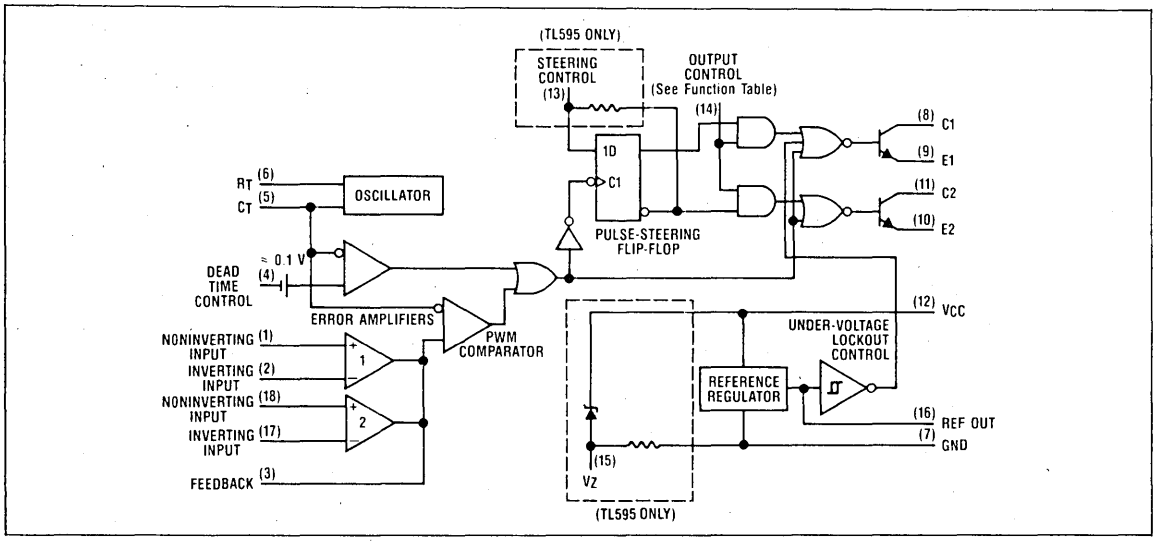
Description

The TL595 provides the identical functions found in the TL594. In addition the TL595 contains an on-chip 39-Volt zener diode for high voltage applications where VCC is greater than 40 volts, and an output steering control that overrides the internal control of the pulse-steering flip-flop. The TL595 is designed to replace the TL495.

N PACKAGE CONNECTION DIAGRAM TOP VIEW



FUNCTION TABLE		
INPUTS		
OUTPUT CONTROL	STEERING INPUT	OUTPUT FUNCTION
Grounded	Open	Single-ended or parallel output
At V_{ref}	Open	Normal push-pull operation
At V_{ref}	V_I<0.4V	PWM Output at Q1
At V_{ref}	V_I<2.4V	PWM Output at Q2



High-voltage adjustable regulator Type TL783C

Features

- Output Adjustable From 1.25 Volt to 125 Volt
- 700 mA Output Current
- Full Short-Circuit, Safe-Operating-Area, and Thermal Shutdown Protection
- 0.001%/V Typical Input Regulation
- 76 dB Typical Ripple Rejection
- 0.15% Typical Output Regulation
- Standard TO-220AB Package

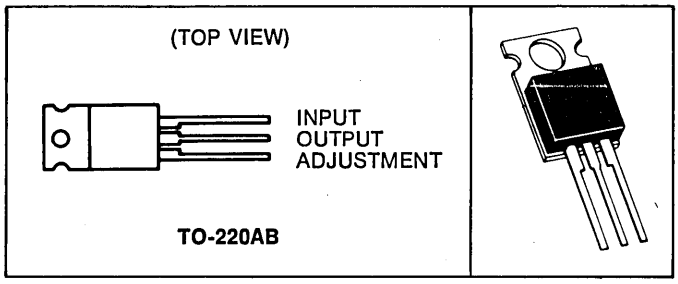
Description

The TL783 is an adjustable 3-terminal positive-voltage regulator with an output range of 1.25 volts to 125 volts and a DMOS output transistor capable of sourcing more than 700 milliamperes. It is designed for use in high-voltage applications where standard bipolar regulators cannot be used. Excellent performance specifications . . . superior to those of most bipolar regulators . . . are achieved through circuit design and advanced layout techniques.

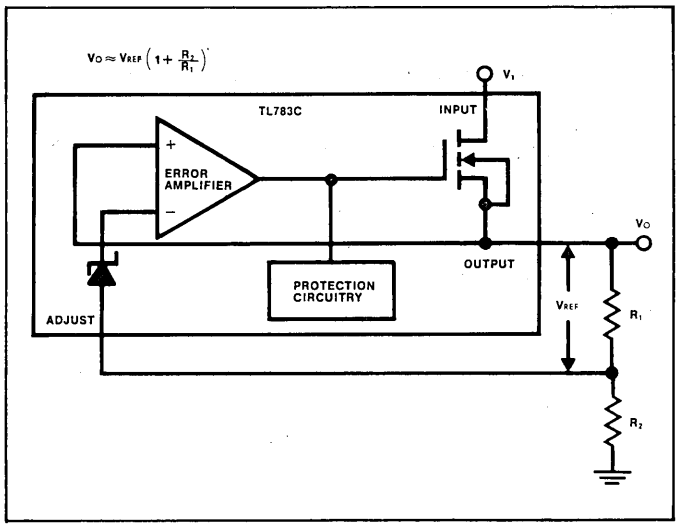
As a state-of-the-art regulator, the TL783 combines standard bipolar circuitry with high-voltage double-diffused MOS transistors on one chip to yield a device capable of withstanding voltages far higher than standard bipolar integrated circuits. Because of its lack of secondary breakdown and thermal runaway characteristics usually associated with bipolar outputs, the TL783 maintains full overload protection while operating at up to 125 volts from input to output. Other features of the device include current limiting, safe-operating-area (SOA) protection, and thermal shutdown. Even if the adjustment pin is inadvertently disconnected, the protection circuitry remains functional.

Only two external resistors are required to program the output voltage. An input bypass capacitor is necessary only when the regulator is situated far from the input filter. An output capacitor, although not required, will improve transient response and protection from instantaneous output short-circuits. Excellent ripple rejection can be achieved without a bypass capacitor at the adjustment terminal.

KC PACKAGE



FUNCTIONAL BLOCK DIAGRAM



TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225612 • DALLAS, TEXAS 75265

High-voltage adjustable regulator
Type TL783C

Absolute maximum ratings over operating temperature range (unless otherwise noted)

Input-to-output differential voltage, $V_I - V_O$	125V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 1)	2W
Continuous total dissipation at (or below) 25°C case temperature (see Note 1)	20W
Operating free-air, case, or virtual junction temperature range	0°C to 150°C
Lead temperature 1/16 inch (1,6mm) from case for 10 seconds	260°C

NOTE 1: For operation above 25°C free-air or case temperature, refer to the dissipation derating curves, Figures 1 and 2.

Recommended operating conditions

	MIN	MAX	UNIT
Input-to-output voltage differential, $V_I - V_O$		125	V
Output current, I_O	15	700	mA
Operating virtual junction temperature, T_J	0	125	°C

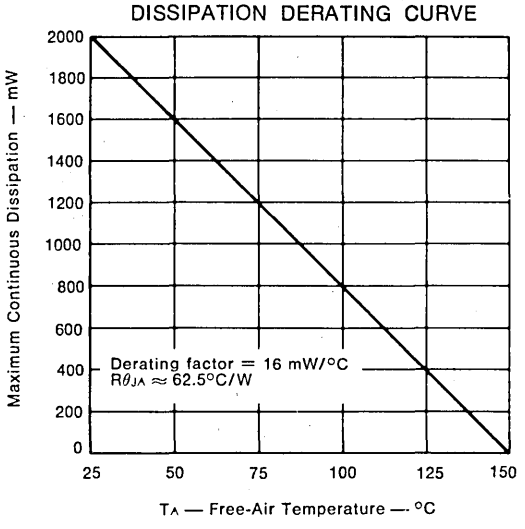


FIGURE 1

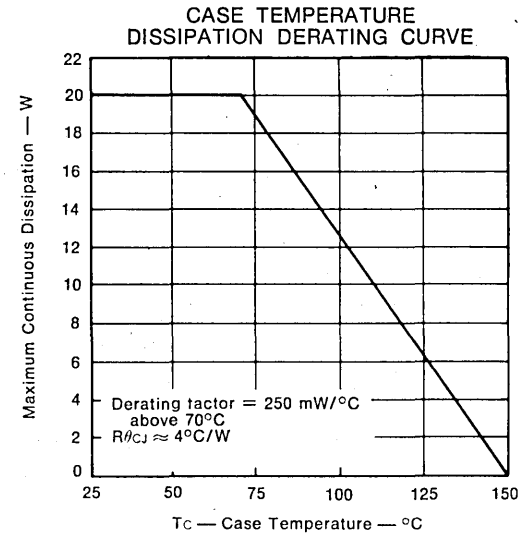


FIGURE 2

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225612 • DALLAS, TEXAS 75265

TL780 Series New Industry Heavyweight

TI's new TL780 series is a pin-for-pin replacement for the μA7800 series of voltage regulators with identical power handling capabilities.

Greatly improved output voltage tolerance, line regulation, load regulation and temperature coefficients are just a few of the key features. Features and enhancements accomplished by process techniques, rather than standard electrical screening.

You'll find TL780 series devices ideal for applications that require maximum output voltage tolerances tighter than the 4-5% generally available, or where multiple on-board regulators must maintain the 5% tolerance commonly required.

The new series consists of: • TL780-05: 5-volt regulator • TL780-12: 12 volt regulator • TL780-15: 15-volt regulator.

The TL780-05, TL780-12, and TL780-15 fixed three-terminal series pass regulators are greatly improved versions of the popular μA78XX series. The TL780 series offers significantly improved regulation performance, while maintaining the power handling capabilities of the μA78XX series. Consider replacing the μA7805, μA7812, or μA7815 with the TL780-05, TL780-12, or TL780-15 for all your critical applications.

TI780 vs. μA78 PERFORMANCE COMPARISON

DESCRIPTION	TL780-XX	μA78XX
Improved Output Voltage Tolerance @ 25°C	±1%	±4%
Over Full Operating Range	±2%	±5%
Improved Line Regulation V_{IN} = 7V to 25V	5 mV	100mV
Improved Load Regulation V_{OUT} = 5 mA to 1.5 A	25 mV	100mV
Improved Temperature Coefficient	0.25 mV/°C	1.1mV/°C
Identical Pinouts		
Identical Output Currents	1.5 A	1.5 A
Identical Drop Out Voltages	2V	2V
Identical Bias Currents	8 mA	8 mA

TL780-05C ELECTRICAL CHARACTERISTICS (V_I = 10V, I_O = 500 mA UNLESS OTHERWISE NOTED)

PARAMETER	TEST CONDITIONS*	TEMP	MIN	TYP	MAX	UNIT
Output Voltage	I_O = 5 mA to 1 A, V_I = 7V to 20V, P ≤ 15W	25°C 0°C to 125°C	4.95 4.9	5	5.05 5.1	V
Input Regulation	V_I = 7V to 25V V_I = 8V to 12V	25°C 25°C		0.5 0.5	5 5	mV
Ripple Rejection	V_I = 8V to 18V f = 120 KHz	0°C to 125°C	70	85		dB
Output Regulation	I_O = 5 mA to 1.5 A I_O = 250 mA to 750 mA	25°C 25°C		4 1.5	25 15	mV
Output Resistance	f = 1 KHz	0°C to 125°C		0.0035		Ω
Temperature Coefficient of Output Voltage	I_O = 5 mA	0°C to 125°C		0.25		mV/°C
Output Noise Voltage	f = 10 Hz to 100 KHz	25°C		75		μV
Dropout Voltage	I_O = 1 A	25°C		2		V
Bias Current		25°C		5	8	mA
Bias Current Change	V_I = 7V to 25V, I_O = 5 mA to 1 A	0°C to 125°C		0.7 0.03	1.3 0.5	mA
Short-Circuit Output Current	V_I = 35V	25°C		750		mA
Peak Output Current		25°C		2.2		A

*Note: All characteristics are measured with a capacitor across the input of 0.33 μF and a capacitor across the output of 0.22 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (t_w ≤ 10 ms, duty cycles ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225612 • DALLAS, TEXAS 75265

TL780 Series Voltage Regulators

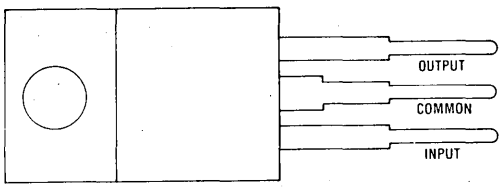
TL780-12C ELECTRICAL CHARACTERISTICS (V_I = 19V, I_O = 500 mA UNLESS OTHERWISE NOTED)

PARAMETER	TEST CONDITIONS*	TEMP	MIN	TYP	MAX	UNIT
Output Voltage	I_O = 5 mA to 1 A, V_I = 14.5V to 27V, P ≤ 15W	25°C 0°C to 125°C	11.88 11.76	12	12.12 12.24	V
Input Regulation	V_I = 14.5V to 30V V_I = 16V to 22V	25°C 25°C		1.2 1.2	12 12	mV
Ripple Rejection	V_I = 15V to 25V, f = 120 Hz	0°C to 125°C	65	80		dB
Output Regulation	I_O = 5 mA to 1.5 A I_O = 250 mA to 750 mA	25°C 25°C		6.5 2.5	60 36	mV
Output Resistance	f = 1 KHz	0°C to 125°C		0.0035		Ω
Temperature Coefficient of Output Voltage	I_O = 5 mA	0°C to 125°C		0.6		mV/°C
Output Noise Voltage	f = 10 Hz to 100 KHz	25°C		180		μV
Dropout Voltage	I_O = 1 A	25°C		2		V
Bias Current		25°C		5.5	8	mA
Bias Current Change	V_I = 14.5V to 30V I_O = 5 mA to 1 A	0°C to 125°C		0.4 0.03	1.3 0.5	mA
Short-Circuit Output Current	V_I = 35V	25°C		350		mA
Peak Output Current		25°C		2.2		A

TL780-15C ELECTRICAL CHARACTERISTICS (V_I = 23V, I_O = 500 mA UNLESS OTHERWISE NOTED)

PARAMETER	TEST CONDITIONS*	TEMP	MIN	TYP	MAX	UNIT
Output Voltage	I_O = 5 mA to 1 A, V_I = 17.5V to 30V,	25°C 0°C to 125°C	14.85 14.7	15	15.15 15.3	V
Input Regulation	V_I = 17.5V to 30V V_I = 20V to 26V	25°C 25°C		1.5 1.5	15 15	mV
Ripple Rejection	V_I = 18.5V to 28.5V, f = 120 Hz	0°C to 125°C	60	75		dB
Output Regulation	I_O = 5 mA to 1.5 A I_O = 250 mA to 750 mA	25°C 25°C		7 2.5	75 45	mV
Output Resistance	f = 1 KHz	0°C to 125°C		0.0035		Ω
Temperature Coefficient of Output Voltage	I_O = 5 mA	0°C to 125°C		0.62		mV/°C
Output Noise Voltage	f = 10 Hz to 100 KHz	25°C		225		uV
Dropout Voltage	I_O = 1 A	25°C		2		V
Bias Current		25°C		5.5	8	mA
Bias Current Change	V_I = 17.5V to 30V I_O = 5 mA to 1 A	0°C to 125°C		0.4 .02	1.3 0.5	mA
Short-Circuit Output Current	V_I = 35V	25°C		230		mA
Peak Output Current		25°C		2.2		A

*Note: All characteristics are measured with a capacitor across the input of 0.33 μF and a capacitor across the output of 0.22 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (t_w ≤ 10 ms, duty cycles ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.



KC Package (Top View)

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225612 • DALLAS, TEXAS 75265

Differential video amplifier
Type TL592

Features

- 8 Pin Version of NE592
- Adjustable Gain to 400
- No Frequency Compensation Required
- Adjustable Passband

Description

This device is a monolithic two-stage video amplifier with differential inputs and differential outputs.

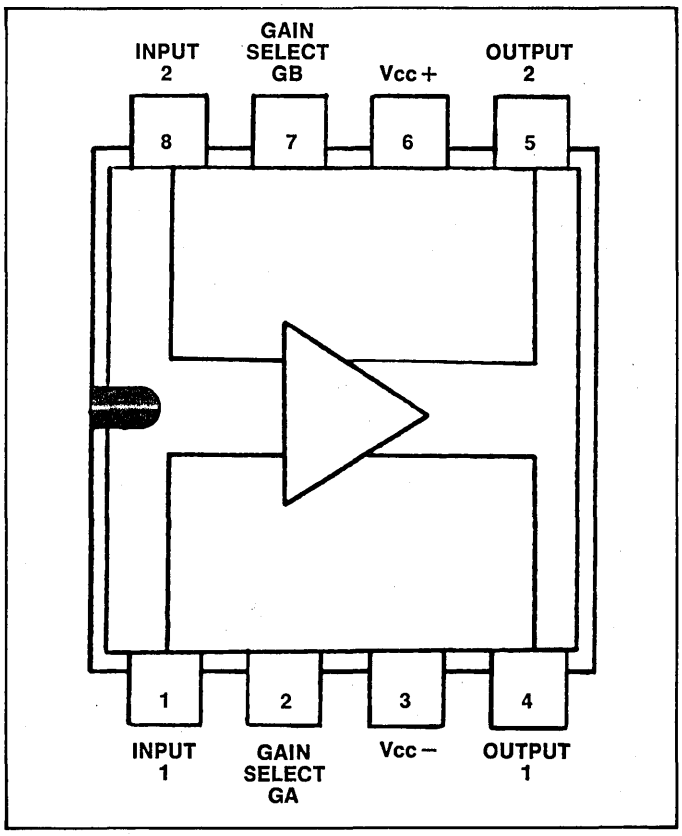
Internal series-shunt feedback provides wide bandwidth, low phase distortion, and excellent gain stability. Emitter-follower outputs enable the device to drive capacitive loads. All stages are current-source biased to obtain high common-mode and supply-voltage rejection ratios.

Fixed differential amplification of 400 may be selected without external components, or amplification may be adjusted from 0 to 400 by the use of a single external resistor connected between GA and GB. No external frequency-compensating components are required for any gain option.

The device is particularly useful in magnetic-tape or disc-file systems using phase or NRZ encoding and in high-speed thin-film or plated-wire memories. Other applications include general purpose video and pulse amplifiers where wide bandwidth, low phase shift, and excellent gain stability are required.

The TL592 is characterized for operation from 0°C to 70°C.

P DUAL-IN-LINE PACKAGE (Top view)



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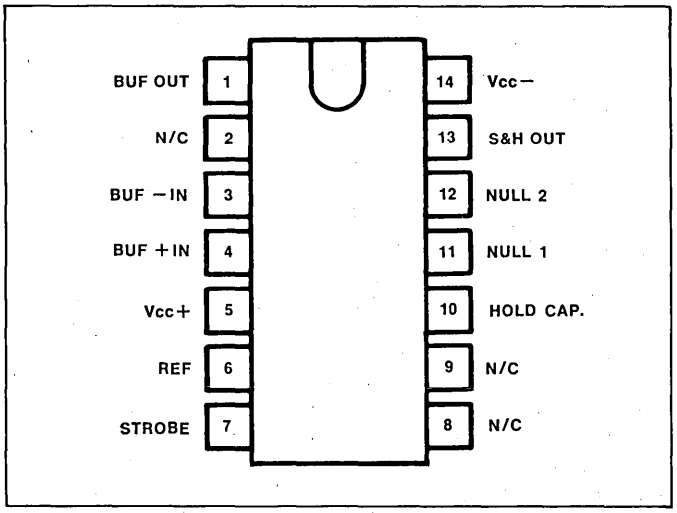
ADVANCE INFORMATION
This page contains information on a new product. Specifications are subject to change without notice.

Single supply NFET sample and hold circuit Type TL195CN

Features

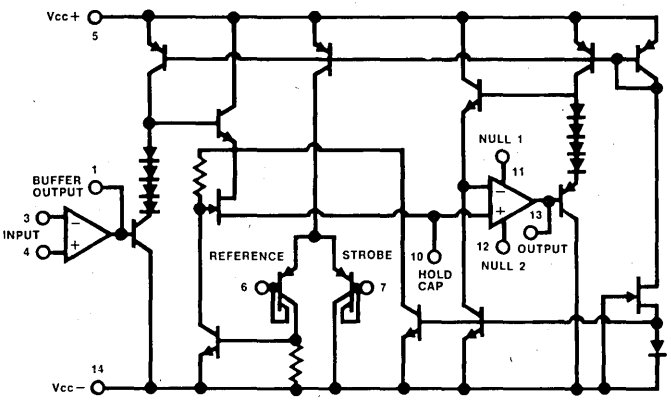
- Single Supply or Split Supply Operation
- Input and Output Common Mode Range Includes Vcc −
- N-Channel JFET Inputs for High Input Impedance (10 E12) Typical
- True Differential Inputs
- External Offset-Null Capabilities
- Fast Acquisition Time 10 μSec.
- Differential Strobe/Reference Inputs with Wide Common Mode Range
- Short Circuit Protection



Description

The TL195 is a sample and hold device utilizing N-Channel JFET (NFET) input transistors to achieve high input impedance (10 E12 ohms), very low input bias (0.4 na), and input offset (0.2 na) currents. This unique configuration allows the input common mode range to include the Vcc− rail for true single supply operations. Some additional features are: a full differential input amplifier (allowing gain configurations to be achieved without external amplifiers), differential strobe and reference inputs, offset null capabilities, and proper signal phasing to allow external hold step error compensation with a minimum of components.

CIRCUIT SCHEMATIC



TEXAS INSTRUMENTS
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Floppy disc write amplifier Type SN75251

Features

- Meets ANSI Standard X 379/846 for Floppy E Minifloppy Disc Systems
- Two Heads Independently Selectable Drive Capability with Erase Tunnel
- Chip Select with Write and Erase Enable
- External RC Programmable Delay
- Internal Warm Up Protection
- 16 Pin Dual In Line Package

Description

The SN75251C is an integrated circuit used for data byte recording on floppy or minifloppy disc.

Input data and control signals are TTL compatible.

The device drives two magnetic heads with erase's tunnel, each of which can be alternately selected by means of side one select input.

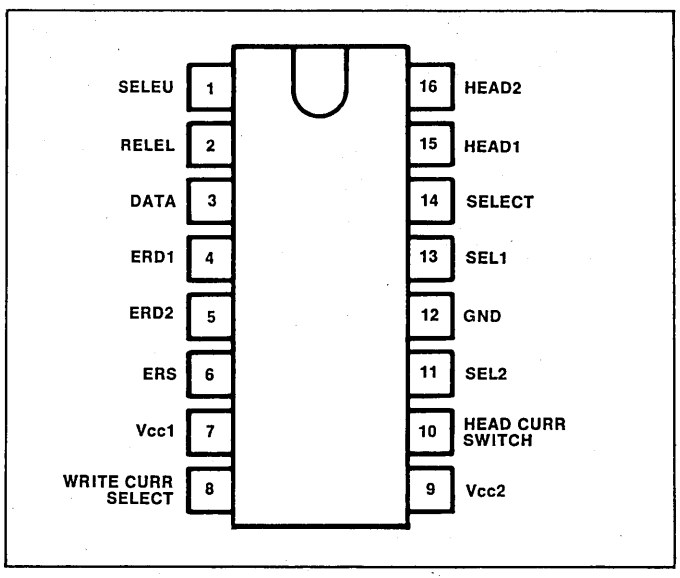
Two write level currents can be selected by means of head current switch input (SELCO).

Additional features are:

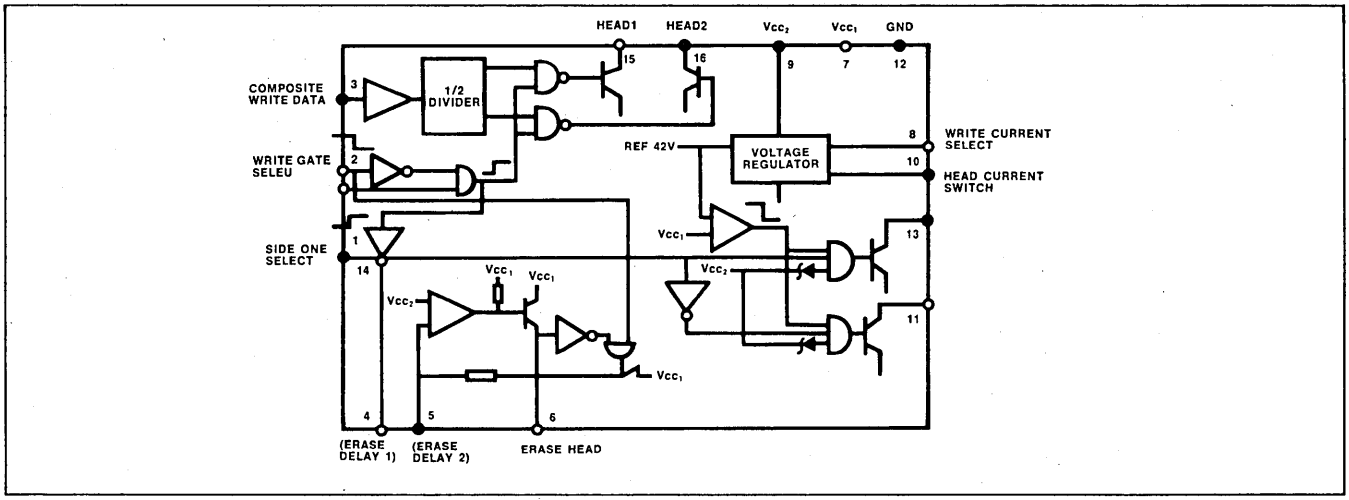
- An internal "Warm up" protection that disables the erase-write function for $Vcc_1 < 4,2V$ and/or $Vcc_2 < 8V$ (typical values). During operations, Vcc_2 has to be never less than Vcc_1.
- A built in circuit that provides a shorter delay between positive going write gate input and erase current (function of RELEL ERASE) in comparison to delay given by external timing components.

The SN75251 is encapsulated in a 16 pin plastic dual in line package.

N DUAL-IN-LINE PACKAGE (Top view)



CIRCUIT SCHEMATIC



A/D Converters

All TRW A/D converters, except the TDC1001 and TDC1002, are fully parallel "flash" types, which accurately sample and convert high-frequency input signals without a track-and-hold circuit. Resolutions from 4 to 9 bits and speeds from 10 to 60 MSPS (MegaSamples Per Second) offer the best choice for most signal processing requirements. The parts are TTL or ECL compatible, as required by the speed and resolution of the device.

Product	Resolution (bits)	Conversion Rate* (MSPS)	Power Dissipation* (watts)	Package	Extended Temperature Range Available	Available	Notes
TDC1001	8	2.5	0.6	J8	−20°C to 85°C	7/77	Successive approximation
TDC1002	8	1.0	0.6	J8	−20°C to 85°C	7/77	Successive approximation
TDC1007	8	20	2.6	J1, C1, L1	−30°C to 125°C	4/78	
				E1, P1	no	4/78	Evaluation boards
TDC1014	6	25	1.0	J7, C3	−55°C to 125°C	8/78	
				E1, P1	no	8/78	Evaluation boards
TDC1019	9	20	2.6	J1, C1, L1	1Q83	1/81	
				E1	no	1/81	Evaluation board
TDC1021	4	25	0.3	J9	−55°C to 125°C	11/78	
TDC1025	8	60	4.5	C1, L1	2Q83	3Q82	
				E1	no	7/81	Evaluation board
TDC1027	7	20	1.6	J7	4Q82	3Q82	
TDC1029	6	100	1.8	J7	1Q83	4Q82	
				E1	no	4Q82	Evaluation board

* Guaranteed, Worst Case, T_A=0°C to 70°C.

D/A Converters

These D/A converters offer 75-ohm, 1V outputs to drive video filters or transmission lines directly. On-chip data registers and careful internal timing to matched current sources result in output glitches that are so small (less than 100 picovolt-seconds worst case) that no resample circuit or deglitcher is necessary. The TDC1016 has 10 input data bits and is available in three integral linearity grades equivalent to ½ LSB error at 8, 9, and 10 bit resolution. The parts have dual-level input buffers which operate with TTL or ECL signals: In ECL mode, only a single −5V power supply is required. The TDC1016 in the J5 or C2 package can operate in a fully differential ECL mode, as well as single-ended ECL or TTL.

Product	Bits	Integral Linearity Error (%)	Conversion Rate* (MSPS)	Power Dissipation* (watts)	Package	Extended Temperature Range Available	Available	Notes
TDC1016	8**	0.20	20	0.7	J5, J7, C2	−55°C to 125°C	8/80	
	9**	0.10	20	0.7	J5, J7, C2	2Q82	8/80	
	10**	0.05	20	0.7	J5, J7, C2	2Q82	8/80	

* Guaranteed, Worst Case, T_A=0°C to 70°C.

**The TDC1016 has 10 bit resolution, and is available in three linearity grades to meet 8, 9, and 10 bit system requirements.

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40G00838 REV. A-7/82
Printed in the U.S.A.

TDC1019
Preliminary Information

Monolithic Video A/D Converter
9 Bit, 20 MSPS

The TRW TDC1019 is a 20 MegaSample Per Second (MSPS) full-parallel (flash) analog-to-digital converter, capable of converting an analog signal with full-power frequency components up to 7 MHz into 9-bit digital words. No sample-and-hold circuit is necessary. All digital inputs and outputs are ECL compatible.

The TDC1019 consists of 511 latching comparators, combining logic, and an output buffer register. A single convert signal controls the conversion operation. The unit can be connected to give outputs in either binary or offset two's complement coding.

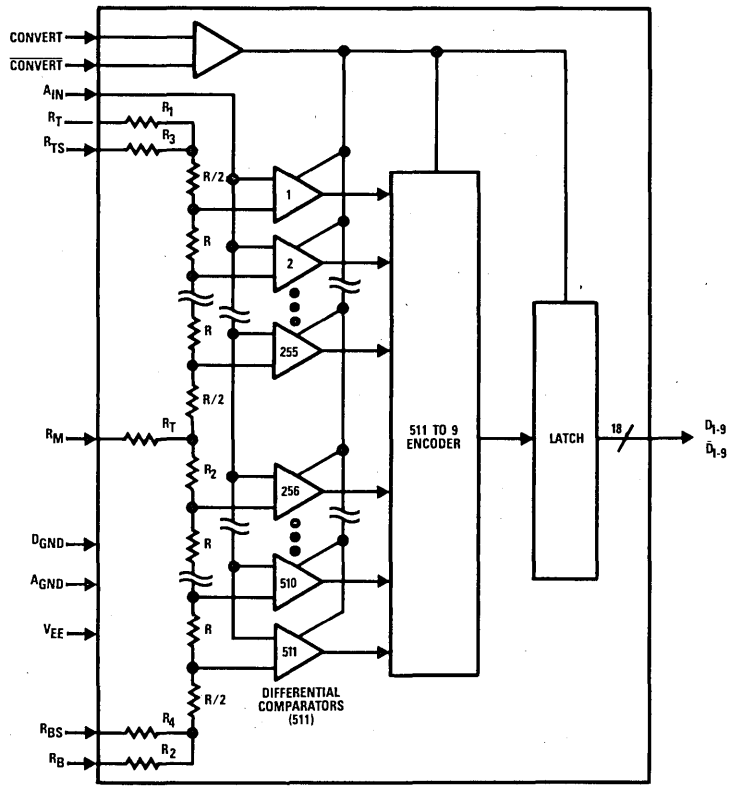
Features

- 9 Bit Resolution
- ½ LSB Linearity
- No Sample-And-Hold Circuit Required
- ECL Compatible
- 20 MSPS Conversion Rate
- Selectable Output Format
- Available In 64-Pin DIP And 68-Contact Leadless and Leaded Chip Carriers
- Complete Evaluation Board (TDC1019E1C) Available

Applications

- Video Data Conversion
  - 3X or 4X NTSC Color
  - 3X or 4X PAL Color
- Radar Data Conversion
- High-Speed Multiplexed Data Acquisition

Functional Block Diagram



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TDC1025
Advance Information

Monolithic Video A/D Converter
8 Bit, 60 MSPS

The TRW TDC1025 is a 60 MegaSample Per Second (MSPS) full-parallel (flash) analog-to-digital converter, capable of converting an analog signal with full-power frequency components up to 25 MHz into 8-bit digital words. No sample-and-hold circuit is necessary. All digital inputs and outputs are ECL compatible.

The TDC1025 consists of 255 latching comparators, combining logic, and an output buffer register. A single convert signal controls the conversion operation.

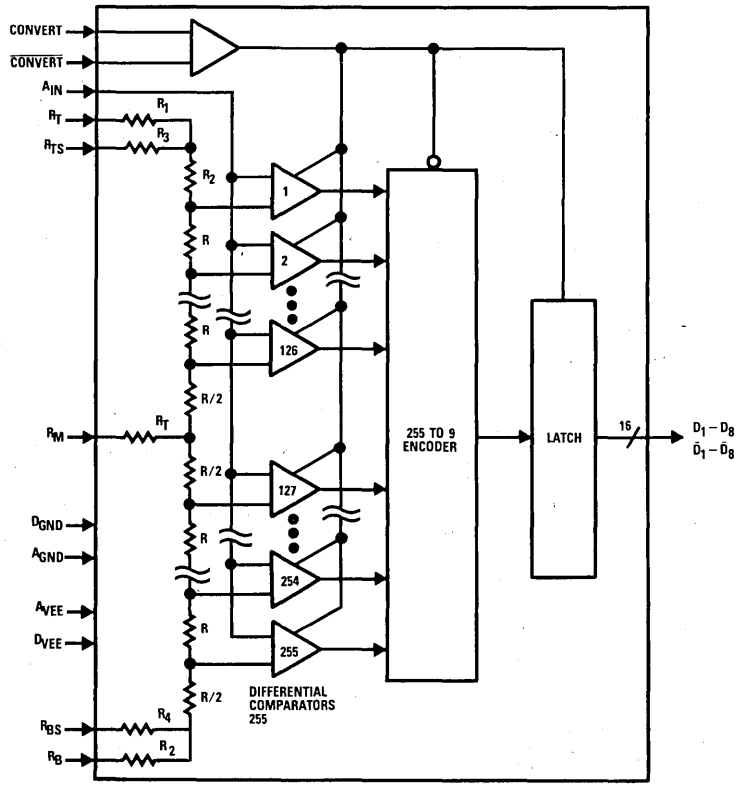
Features
- 8 Bit Resolution
- ½ LSB Linearity
- No Sample-And-Hold Circuit Required
- ECL Compatible
- 60 MSPS Conversion Rate
- Available in 68-Contact Leadless And Leaded Chip Carriers
- Advanced 1-micron (OMICRON-B™) Technology
- Fastest Monolithic 8-Bit A/D Converter Available
- Complete Evaluation Board (TDC1025E1C) Available

Applications
- Medical Electronics
- Fluid Flow Analysis
- Seismic Analysis
- Radar/Sonar
- Transient Analysis
- High-Speed Image Processing

LINEAR

TRW LSI Products

Functional Block Diagram



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TDC1027
Preliminary Information

Monolithic Video A/D Converter
7 Bit, 20 MSPS

The TRW TDC1027 is a 20 MegaSample Per Second (MSPS) full-parallel (flash) analog-to-digital converter, capable of converting an analog signal with full-power frequency components up to 6 MHz into 7-bit digital words. No sample-and-hold circuit is necessary. All digital inputs and outputs are TTL compatible.

The TDC1027 consists of 127 latching comparators, combining logic, and an output buffer register. A single convert signal controls the conversion operation. The unit can be connected to give either true or inverted outputs in binary or offset two's complement coding via F1 and F2.

Features

- 7 Bit Resolution
- ½ LSB Linearity
- No Sample-And-Hold Circuit Required
- TTL Compatible
- 20 MSPS Conversion Rate
- Selectable Output Format
- Available In 24-Pin DIP

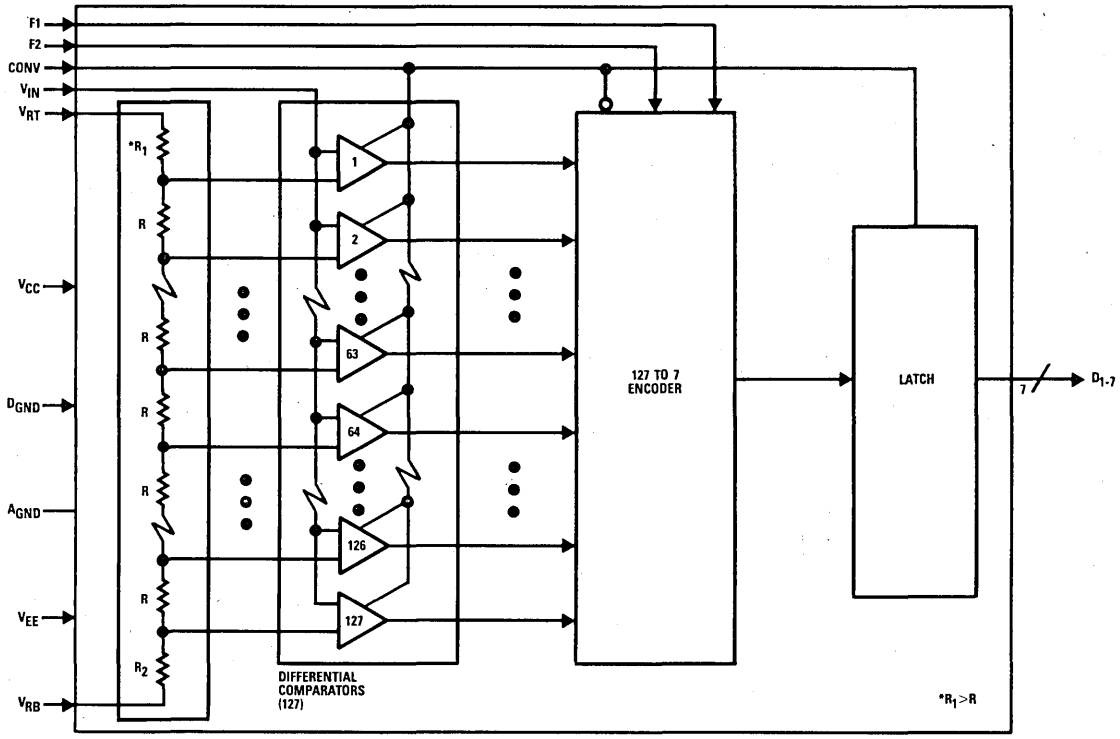
Applications

- Low-Cost Video Digitizing
- Medical Imaging
- Data Acquisition
- TV Special Effects
- Video Simulators
- Radar Data Conversion

LINEAR

TRW LSI Products

Functional Block Diagram



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TDC1029
Advance Information

Monolithic Video A/D Converter
6 Bit, 100 MSPS

The TRW TDC1029 is a 100 MegaSample Per Second (MSPS) full-parallel (flash) analog-to-digital converter, capable of converting an analog signal with full-power frequency components up to 50 MHz into 6-bit digital words. No sample-and-hold circuit is necessary. All digital inputs and outputs are ECL compatible.

The TDC1029 consists of 64 latching comparators, combining logic, and an output buffer register. A single convert signal controls the conversion operation. The unit can be connected to give outputs in either binary or offset two's complement coding.

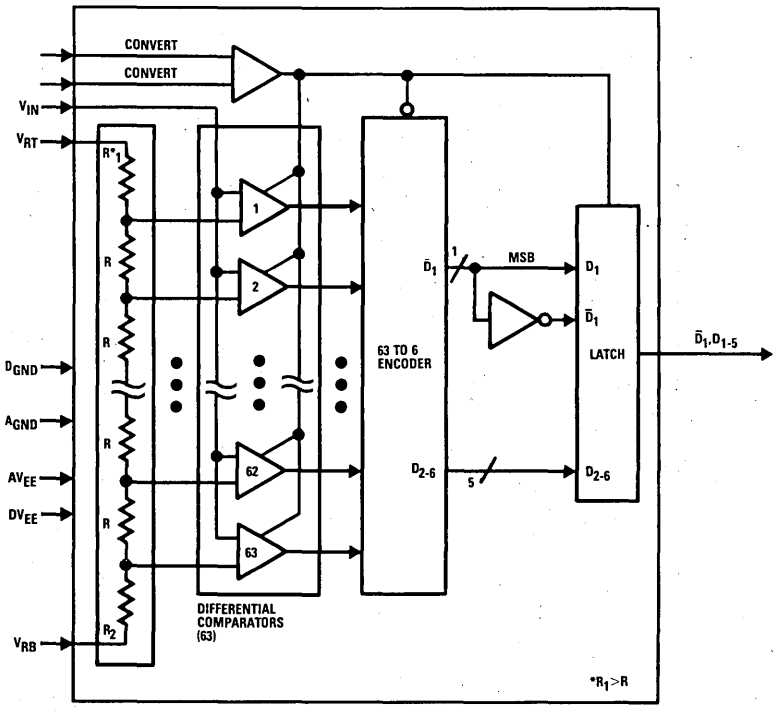
Features

- 6 Bit Resolution
- ½ LSB Linearity
- No Sample-And-Hold Circuit Required
- ECL Compatible
- 100 MSPS Conversion Rate
- Selectable Output Format
- Available In 24-Pin DIP
- Fastest 6-Bit Monolithic A/D Available
- Complete Evaluation Board Available 1st Quarter, 1983

Applications

- Telecommunications
- Radar Ultrasound Processing
- Medical Imaging
- High-Resolution Video Processing
- Optical Character Recognition

Functional Block Diagram



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40G00817 Rev. A–6/82
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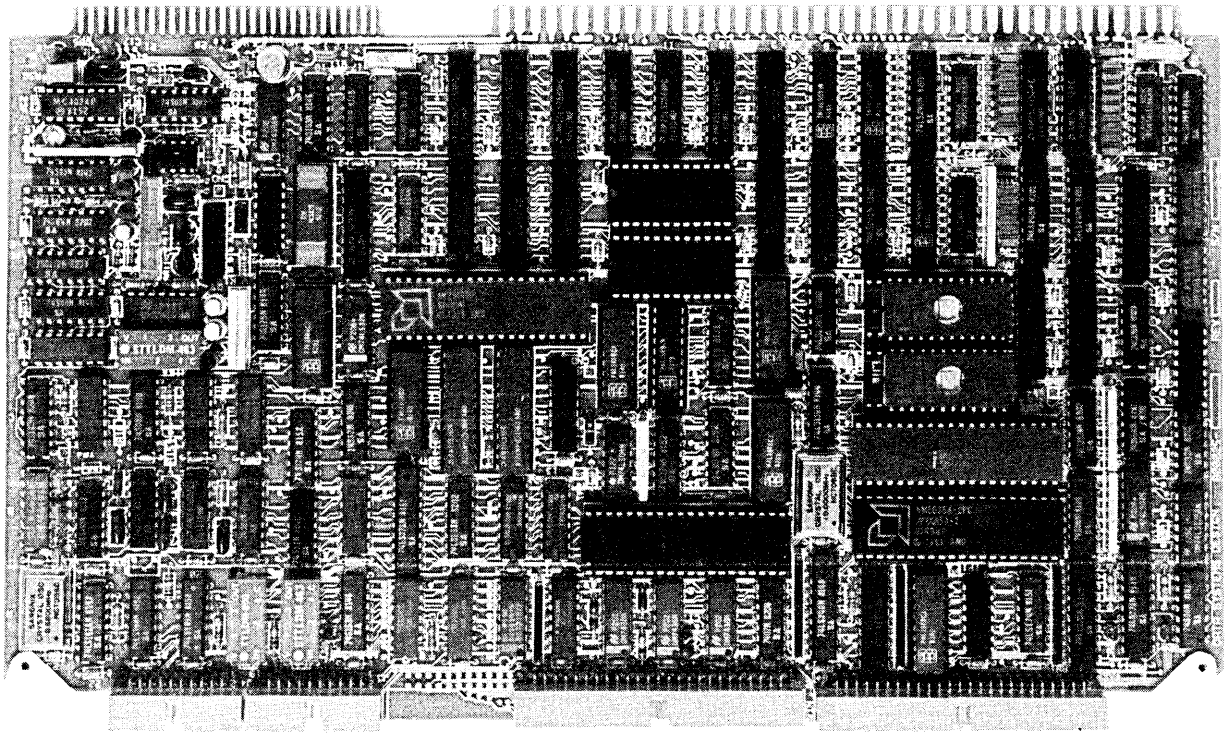
For Key Data On Every IC On This Board, The Place To Look Is...



The Data System Design 7215 is a single-board controller with pipelined architecture that can simultaneously control Winchester, streaming tape, and floppy drives.

Device No.	Description
AM25LS2569	Up-Down Binary Counter with Synchronous Preset
AM2910	Dual Retriggerable Monostable Multivibrator
AM26S02	Programmable Schottky Read-Only Memory
AM27S35	12-Bit Microprogram Controller
AM8085	Complete 8-Bit Parallel Central Processing Unit
CA3130	5-to-16-Volt Single Stash Supply Op Amp
2732	4096 x 8 TTL PROM
8237	DMA Controller
DM7438	Quad 2-Input TTL NAND Buffer
DM8334	8-Bit Addressable TTL Latch
DS75107	Differential Line Receiver
F74S132	Quad 2-Input NAND Schmitt-Trigger
MC4024	Dual Voltage-Controlled TTL Multivibrator
MK4802	2048 x 8 Static NMOS RAM
PAL16L8	Field Programmable Logic Array
PAL16R6	Field Programmable Logic Array
PAL16R8	Field Programmable Logic Array
7407	Hex Buffer/Driver
74123	Dual Retriggerable Monostable Multivibrator
74368	Hex Inverter, 3-State
74LS02	Quad 2-Input TTL NOR Gate
74LS04	Hex Inverter
74LS125	Quad Gated TTL Buffer, 3-State
74LS138	3 Line to 8 Line Decoder/Demultiplexer
74LS151	8-Input Multiplexer
74LS161	Binary Counter
74LS166	8-Bit Parallel-In, Serial-Out Shift Register with Clear

Device No.	Description
74LS174	Hex D-Type Edge-Triggered Flip-Flop with Clear
74LS240	Octal Bus Driver (Schmitt Trigger)
74LS244	Octal Bus Driver (Schmitt Trigger), Non-Inverting
74LS257	Quad 2-Input Multiplexer, Non-Inverting
74LS273	Octal D-Type Edge-Triggered Flip-Flop, 3-State
74LS299	8-Bit Universal Shift Register
74LS365	Hex Buffer, 3-State
74LS373	8-Bit Latch
74LS374	Octal D-Type Edge-Triggered Flip-Flop, 3-State
74LS393	Dual 4-Bit Binary Counter
74LS533	D-Type 8-Bit Latch
74LS670	16-Bit (4x4) Register File with Simultaneous Read/Write
74S00	Quad 2-Input NAND Gate
74S03	Quad 2-Input NAND Gate, Open Collector
74S04	Hex Inverter
74S112	Dual "J-K" Negative Edge-Triggered Flip-Flop
74S151	8-Input Multiplexer
74S153	Dual 4-Input Multiplexer
74S174	Hex D-Type Edge-Triggered Flip-Flop with Clear
74S175	Quad D-Type Edge-Triggered Flip-Flop with Clear
74S240	Line Driver, Single Ended, 3-State, Inverting
74S32	Quad 2-Input OR Gate
74S51	Dual 2-Wide 2-Input AND-OR-Invert Gate
74S64	4-2-3-2-Input AND-OR-Invert Gate
74S74	Dual D-Type Positive Edge-Triggered Flip-Flop
75110	Line Driver, Differential, Twisted Pair Level Shifting

Representative list of ICs on the Data Systems Design 7215 board.
Key specifications for all of these ICs can be found in IC MASTER.

IC MASTER

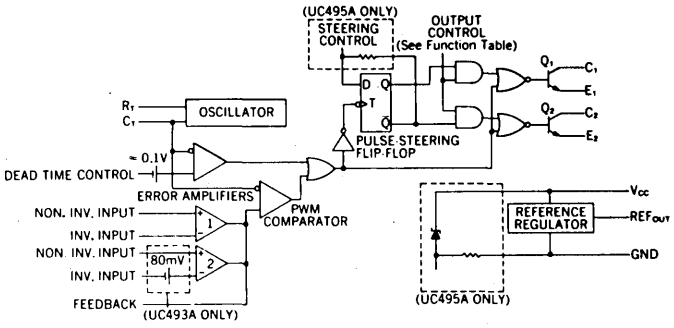
BE SURE. BEGIN WITH THE IC MASTER

LINEAR INTEGRATED CIRCUITS

Regulating Pulse Width Modulators

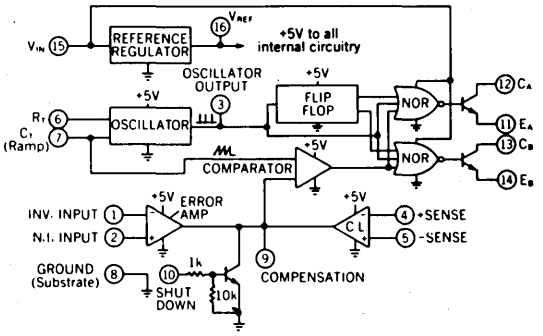
UC493A/UC494A/UC495A
UC493AC/UC494AC/UC495AC

- Fully Interchangeable, Advanced Version of 494 family.
- Uncommitted Outputs for Single-ended or Push-pull Applications
- Supply Voltage, V_{CC} ..... 7V to 40V
- Reference Voltage, V_{REF} ..... 5V to ±1%
- Dual Error Amplifiers
- Wide Range, Variable Deadtime
- Under-Voltage Lockout
- Double-pulse Protection
- Sawtooth Oscillator Operation to 300kHz
- High Performance Current Limit on UC493A
- Internal 39V Zener for Operation above 40V on UC495A
- Buffered Output Steering Control on UC495A



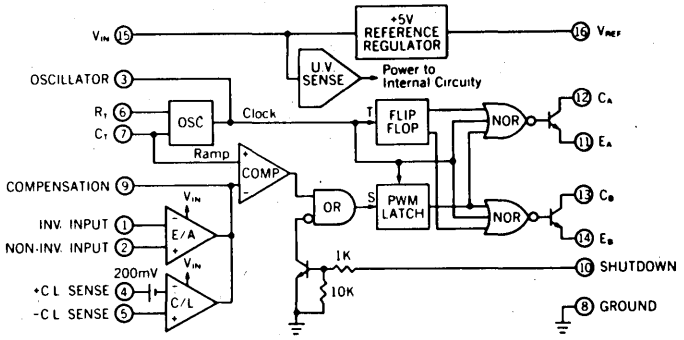
UC1524/UC2524/UC3524

- Complete PWM Power Control Circuitry
- Uncommitted Outputs for Single-ended or Push-pull Applications 100mA
- Output Voltage 40V
- Supply Voltage, V_{CC} ..... 8V to 40V
- Low Standby Current ..... 8mA Typical
- Reference Voltage, V_{REF} ..... 5V ± 4%
- Sawtooth Oscillator Operation to 300kHz
- Analog External Shutdown
- Analog Current Limiting
- 16 Pin Dual-in-line Package



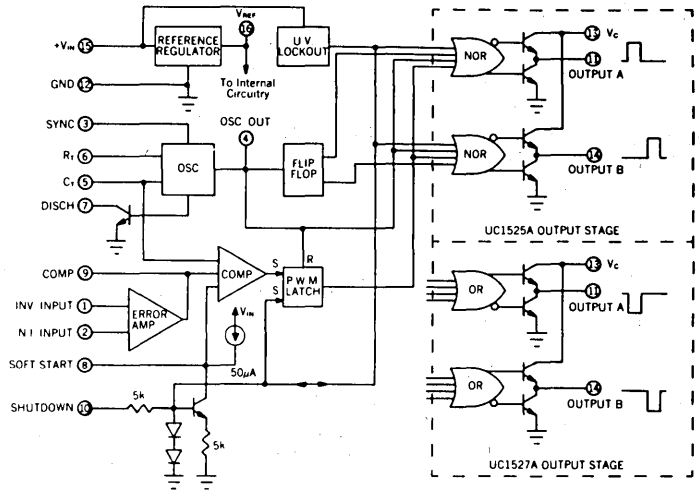
UC1524A/UC2524A/UC3524A

- Fully Interchangeable, Advanced Version of UC1524 family
- Output Current 200mA
- Output Voltage 60V
- High-Performance Current Limit
- Under-Voltage Lockout
- Low Standby Current ..... 5mA Typical
- Reference Voltage, V_{REF} ..... 5V ± 1%
- Wide Common-Mode Input Range for Both Error and Current Limit Amplifiers
- PWM Latch Insures Single Pulse per Period
- 100ns Shutdown
- Guaranteed Frequency Accuracy
- Sawtooth Oscillator Operation to 500kHz
- 16 Pin Dual-in-line Package



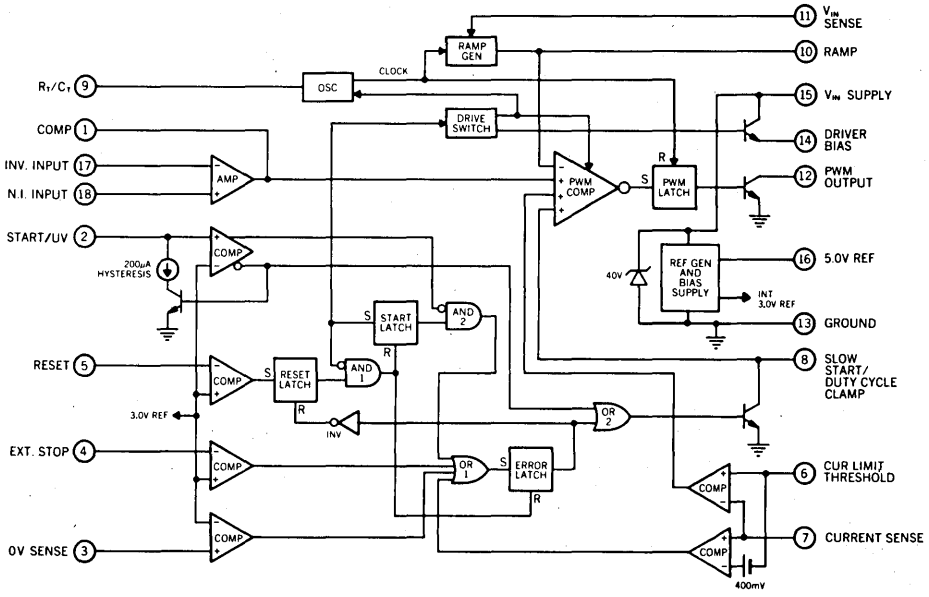
UC1525A/UC2525A/UC3525A
UC1527A/UC2527A/UC3527A

- 8V to 35V Operation
- Reference Voltage, V_{REF} ..... 5.1V ± 1%
- 100Hz to 500kHz Oscillator Range
- Separate Oscillator Sync Terminal
- Adjustable Deadtime Control
- Internal Soft-Start
- Under-Voltage Lockout
- Latching PWM to Prevent Multiple Pulses
- Dual Source/Sink Output Drivers 500mA
- 16 Pin Dual-in-line Package



UC1840/UC2840/UC3840

- All Control, Driving, Monitoring, and Protection Functions Included
- Feed-Forward Sensing for Constant Volt-Second Operation over a 4 to 1 Input Range
- Low Current, Off-Line Start
- Hysteresis for Separating Start and Run Levels
- Under-Voltage Lockout
- Slow Turn-on
- PWM Latch for Single-Pulse Operation
- Pulse-by-Pulse Current Limiting plus Shutdown for Over-Current Fault
- Shutdown upon Over or Under-Voltage Sensing
- Latch off or Continuous Retry Modes
- Remote, Pulse-Commandable Start/Stop
- Maximum PWM Limiting with External Divider
- 200mA PWM Output Switch
- Error Amp Reference Trimmed to ± 1%
- Operation to 500kHz
- 18 Pin Dual-in-line Package



POWER HYBRID CIRCUITS

Switching Regulator Power Output Circuits

The PIC600 through PIC672 series of devices consist of a driver transistor, a fast switching output transistor, a suitably matched fast recovery catch diode and thick film resistors in a hybrid circuit, designed, constructed and specified for use in high current switching regulator applications. Specific ratings for each type is summarized in this table.

Type	Output Current, Pk.	Input/Output Voltage	Polarity	Fall Time Volt. (ns)	Fall Time Cur. (ns)	On-State Voltage (V) @ (A)	Pkg.
PIC600-602 PIC610-612	5A 5A	60-80-100 60-80-100	Pos. Neg.	75 75	150 150	1.5 @ 2 1.5 @ 2	4 PIN TO-66 (Isolated)
PIC660-662 PIC670-672	10A 10A	60-80-100 60-80-100	Pos. Neg.	150 250	250 250	1.5 @ 5 1.5 @ 5	4 PIN TO-66 (Isolated)
PIC625-627 PIC635-637	15A 15A	60-80-100 60-80-100	Pos. Neg.	175 300	300 300	1.5 @ 7 1.5 @ 7	4 PIN TO-66 (Isolated)
PIC645-647 PIC655-657	20A 20A	60-80-100 60-80-100	Pos. Neg.	150 300	300 300	1.5 @ 7 1.5 @ 7	3 PIN TO-3

The PIC730 and 740 series offer a Schottky diode in place of the fast recovery PN catch diode, to permit higher operating efficiencies in switching regulator designs.

PIC730 PIC740	30A 30A	30 40	Pos. Pos.	350 350	300 300	1 @ 20 1 @ 20	3 PIN TO-3

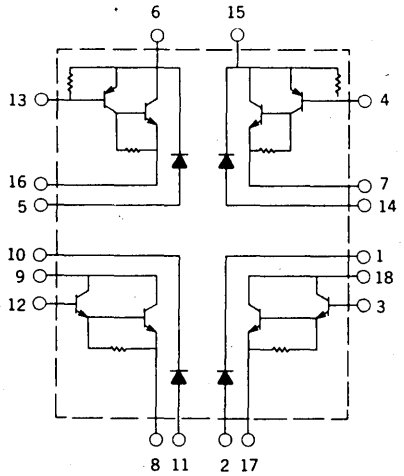
The PIC800 through 811 series are high voltage (up to 400V) versions of the PIC600 series. Applications include high voltage buck or flyback regulators, and, in combination, half bridge or full bridges, as well as deflection circuits and DC motor drives.

PIC800-801 PIC810-811	8A 8A	350-400 350-400	Pos. Neg.	200 200	200 200	1.5 @ 5 1.5 @ 5	4 PIN TO-66 (Isolated)

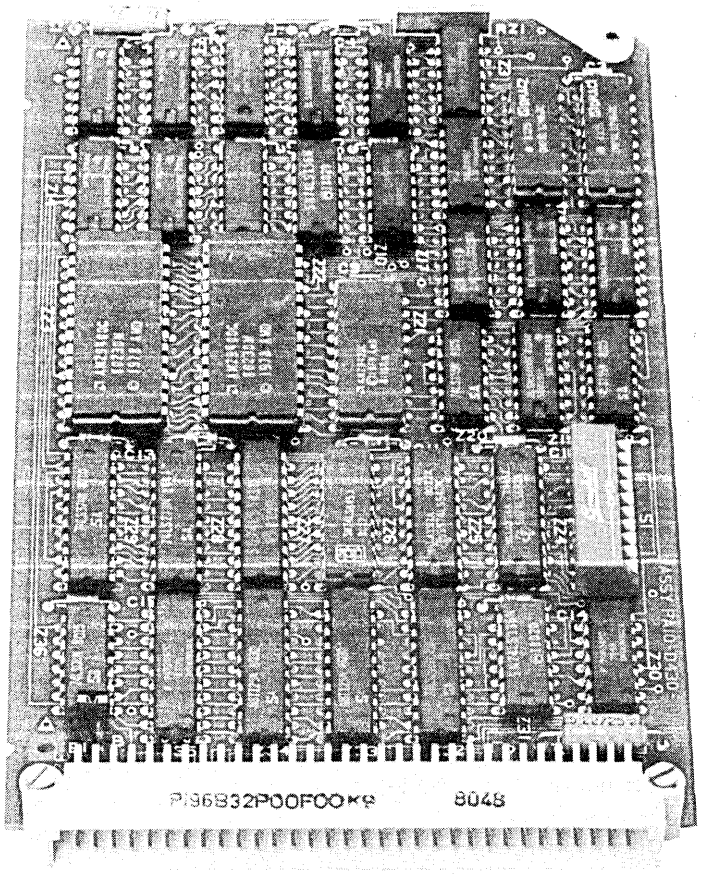
Motor Drive Circuits

PIC900

- Designed and characterized for inductive loads such as
  - Stepper Motor Drivers
  - DC Motor Drivers
  - Full Bridge DC Converters
- Fast switching times with low (5mA) drive current
- Electrically isolated 18 pin dual-in-line package with integral heat spreader
- Compatible with automatic insertion
- Output Current - 5A DC, 10A Peak
- Output Voltage - 80V



For Key Data On Every IC On This Board, The Place To Look Is...



This Rockwell RM65-5104(E) card is used to transfer data between memory and peripheral circuits.

Device No.	Description
74LS08	Quad 2-Input AND Gate
74F244	Octal Buffer/Line Driver
74LS240	Octal Bus Driver (Schmitt Trigger)
74LS136	Quad 2-Input Exclusive-OR Gate
74F04	Hex Inverter
74LS374	Octal D-Type Edge-Triggered Flip-Flop, 3-State
74LS273	Octal Edge-Triggered Flip-Flop with Clear
74LS541	Octal Bus Driver, Noninverting
74LS645	Octal Bus Transceiver
74LS540	Octal Bus Driver, Inverting

Device No.	Description
74LS682	8-Bit Magnitude Comparitor
AM2940	DMA Address Generator
AM2942	Programmable Timer
74LS155	Decoder/Demultiplexer
74LS148	Priority Encoder
74LS74	Dual D-Type Edge-Triggered Flip-Flop
74LS32	Quadruple 2-Input OR Gate
74LS112	Dual J-K Flip-Flop
74LS126	Quadruple Bus Buffer Gate
74LS00	Quadruple 2-Input NAND Gate
PAL12H6	Field Programmable Array

Representative list of ICs on Rockwell Direct Memory Access Card.
Key specifications for all of these ICs can be found in IC MASTER.

IC MASTER

BE SURE. BEGIN WITH THE IC MASTER

INTRODUCTION TO MEMORY

The Master Selection Guide provides sufficient information for making initial product selections. All devices that appear in this section, both in the initial selection guide and the data pages, are included in all indexes. These index listings lead to the page and line on that page where each device appears.

The Memory Section provides initial selection information and data on PROMs, RAMs, and ROMs as well as other memory devices. In these particular sections, the devices are characterized by organization (words and bits/word) and by access times. In order to assure that the access times are comparable, whenever possible the values have been shown in nanoseconds over the full rated temperature range for the devices (i.e., 0° to 70°C for commercial units and −55°C to 125°C for military units). The full temperature nanosecond value is marked "nsF." When this value isn't specified, the guaranteed nanosecond value at room temperature is listed followed by "nsR." In some cases a guaranteed value has not been established; then the typical value is shown followed by "ns*". "Typical" values are invariably much faster than the guaranteed ones so that such listings place these memories higher on the list than they otherwise would appear.

Detailed Product Information provided by:

The manufacturers listed above have provided detailed information on their latest and most significant products.

EINFÜHRUNG SPEICHER

Der Master Selection Guide für Speicher enthält alle Informationen, die Sie für die Erstauswahl Ihres Produkts benötigen. Die Bauteile, die in diesem Abschnitt erscheinen, sowohl im Selection Guide als auch auf den Datenblättern, sind in allen Master Indexes enthalten. Diese Register verweisen auf die Seite und Zeile, auf der das entsprechende Bauelement vorkommt.

Der Speicherteil bestert aus einem Selection Guide und Daten über PROMs, RAMs und ROMs sowie andere Speicher-Bauteile. In diesen einzelnen Abschnitten sind die Bauteile nach Organisation (Worte und Bits/Wort) und nach Zugriffszeiten eingeteilt. Um sicherzustellen, daß die Zugriffszeiten verglichbar sind, wurden die Werte nach Möglichkeit in Nanosekunden für de vollen zugfelassenen Temperaturbereich (d.h. 0° bis 70°C für kommerzielle Bauteile und —55° bis 125°C für militärische Bauteile) angegeben. Der nsec-Wert für den vollen Temperaturbereich ist mit "nsF" bezeichnet. Wenn dieser Wert nicht genannt ist, so ist der garantierte nsec-Wert bei Raumtemperatur mit "nsR" angegeben. In einigen Fällen wurde ein garantierter Wert nicht festgelegt. Dann wird der typische Wert mit einem nachfolgenden "ns*" markiert. "Typische" Werte sind durchwegs schneller als garantierte, so daß solche Eintragungen die Speicher weiter oben in der Liste erscheinen lassen als dies sonst der Fall wäre.

INTRODUCTION AUX MEMOIRES

Le Guide Général de Sélection fournit suffisamment de renseignements pour permettre des sélections initiales de produits. Tous les apareils énumérés dans cette section, tant dans le Premier Guide de Sélection que dans les feuilles de données, sont inclus dans tous les index. Ces index vous procurent la possibilité de retrouver à quelle page et à quelle ligne tel ou tel appareil a été mentionné.

La Section "Mémoires" contient des données et des renseignements de sélection initiale sur les PROMs, les RAMs et les ROMs, ainsi que sur d'autres appareils mémoires. Dans ces sous-sections, les appareils sont distingués par définition (mots et bit/mot) et par temps d'acces. Afin d'être sûr que les temps d'accès soient comparables, chaque fois que cela a été possible, les valeurs ont été indiquées en nanosecondes pour toute la fourchette de température (exemple: 0° à 70° pour les produits industriels, et —55°C à 125°C pour les produits militaires). La valeur entière de température en nanosecondes est désignée par "nsf". Lorsque cette valeur n'est pas donnée, une valeur garantie à température ambiante, exprimée en nanosecondes, est suivie par "nsR". Dans certains cas aucune valeur garantie en nanosecondes n'a pu être établie, la valeur "typique" est alors traduite par "ns". Les valeurs "typiques" sont invariablement beaucoup plus rapides que celles dites "garanties", de sorte que ces mémoires "typiques" apparaissent plus haut sur la liste qu'elles ne le seraient sur d'autres.

INTRODUCCIÓN A MEMORIA

La Guía Maestra de Selección provee suficiente información para hacer selecciones iniciales del producto. Todas las componentes que aparecen en esta sección, ya sea en la guía de selección inicial o en las páginas de datos, están incluídas en todos los otros índices. Estas listas de índices los conduce a la página y linea de aquella página donde se encuentra cada componente.

La Sección de Memoria provee información para la selección inicial y datos de PROMs, RAMs, and ROMs así como otras piezas de memoria. En estas secciones en particular, las componentes se caracterizan por organización (palabras y bits/palabras) y por tiempo de acceso. Con objeto de asegurar que los tiempos de acceso son comparables, cuando es posible, los valores aparecen en nanosegundos sobre el intérvalo completo de temperature para las componentes (en otras palabras, 0° to 70°C para piezas de uso comercial y —55° a 125°C para piezas de uso militar). El valor del intérvalo completo de temperatura esta marcado "nsF". Cuando este valor no está especificado, el valor de nanosegundon está garantizado para temperatura ambiental y aparece seguido por "nsR". En algunos casos el valor no ha sido establecido; entonces el valor tipico aparece seguido por "ns*". Valores "típocos" son sin falta más rápido que los garantizados de tal manera que las listas ubica estas memorias antes que normalmente los mostraría.

メモリーへの案内

マスターセレクションガイドは選択に取りかかる充分な資料を揃えています。セレクションガイド，データ掲載ページにのっている製品は全てのインデックスに入っており，そのインデックスによりページ数，行数はすぐ見つけられます。

このセクションにはPROM，RAM，ROM他のメモリーのデーターが入っています。製品はその構成（ワード，ビット／ワード）とアクセスタイム毎に分類されています。アクセスタイムが同等であるかどうか確認する為可能な限り夫々の全温度範囲（一般0℃～70℃；ミリタリ-55℃～125℃）でのアクセスタイムをナノセカンドで表示しています。全温度範囲でのアクセスタイムは"nsF"と表示，規定されていないものすなわち室温での保証値は"nsR"となっています。保証値が決められていない場合は代表的値として"ns★"がついています。"Typical"値は通常保証値よりも速くつけられるのでリスト上では他に記載されているものより高い場所に記載されています。

MEMORY–Character Generators

Character Generators

Format	Number of Output Lines	Input Logic levels	Supply Voltage, V	Device	Source	Line
5x7	1	TTL	5	DM76S128	† National	
				DM76S64	† National	
				DM8678	National	
				DM86S128	National	
				DM86S64	National	
	5	MOS	5	MM52116FDW	National	
		TTL	5	R03-2513	GI	
				5055	MMI	
				5155	MMI	
				6055	MMI	10
				6061	MMI	
				6155	MMI	
				6156	MMI	
				6161	MMI	
				6162	MMI	
				MCM6670	**Motorola** (3840)	
				MCM6674	**Motorola** (3840)	
			– 12,5	3258	Fairchild	
				32581	Fairchild	
				32582	Fairchild	20
	7	TTL	5	6056	MMI	
				6062	MMI	
			– 12,5	3257	Fairchild	
	35	TTL	5	**MSL9650**	**OKI** (3873)	
				MSL9651	OKI	
				MSL9653	OKI	
				MSL9662RS	**OKI** (3873)	
				MSL9663RS	**OKI** (3873)	
				MSL9664RS	**OKI** (3873)	
6x10	7	MOS	5	MCH-01	Motorola	30
7x9	1	TTL	5	DM76S128	† National	
				DM76S64	† National	
				DM8678	National	
				DM86S128	National	
				DM86S64	National	
	7	MOS	5	MM52116FDX	National	
		TTL	5	5290	† MMI	
				5291	† MMI	
				6071	MMI	
				6072	MMI	40
				6290	MMI	
				6291	MMI	
				MCM66700	**Motorola** (3840)	
				MCM66710	**Motorola** (3840)	
				MCM66714	**Motorola** (3840)	
				MCM66720	**Motorola** (3840)	
				MCM66730	**Motorola** (3840)	
				MCM66734	**Motorola** (3840)	
				MCM66740	**Motorola** (3840)	
				MCM66750	**Motorola** (3840)	50
				MCM66751	Motorola	
				MCM66760	**Motorola** (3840)	
				MCM66770	**Motorola** (3840)	
				MCM66780	**Motorola** (3840)	
				MCM66790	**Motorola** (3840)	
			– 12,5	3260	Fairchild	
7x11	1	TTL	5	CRT7004	SMC	
				CRT8002	SMC	
9x9	9	TTL	5	5292	† MMI	
				5293	† MMI	60
				6292	MMI	
				6293	MMI	
10x9	10	TTL	5	2670	Signetics	
14 Segments						
	14	TTL	5	**MSL9664**	**OKI** (3873)	
16 Segments						
	16	TTL	5	**MSL9662**	**OKI** (3873)	
				MSL9663	**OKI** (3873)	

† Military Temperature Range (–55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

MEMORY–Code Converters

Code Conversion From	To	Bits In	Bits Out	Process	Supply Voltage, V	Device	Source	Line
Code Converters								
BINARY-BCD		6	6	Bipolar	5	**SN54185A**	**† TI**	**(900)**
						SN74185A	**TI**	**(900)**
EBCDIC-ASCII		12	8	Bipolar	5	DM8576AAA	National	
Multiple ASCII-SELECTRIC, EBCID, HOLLERITH				NMOS	±5	MCM68316	Motorola	
						MCM68A316E-91	**Motorola**	**(3840)**
BCD-BINARY		6	6	Bipolar	5	**SN54184**	**† TI**	**(440,899)**
						SN74184	**TI**	**(899)**

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

MEMORY–EAROMs, FIFOs, LIFOs

Electrically Alterable ROMs

Words	Bits Per Word	Access Time (Max)	Output	Supply Voltage, V	Device	Source		Line
16	16	—	Serial	5	**NMC9306**	**National**	**(3867)**	
					X2444	Xicor		
		160 μsF	TS	5	NCR52801	NCR		
21	16	10 μsF	TS	−20,10	NCR7033	NCR		
			TS Serial					
				−20,10	NC7033	Nitron		
32	16	3 μsF	TS	−28,5	ER2051	GI		
		4 μsF	TS	−29,5	NCR2051	NCR		
					NC7051	Nitron		
50	14	10 msF	TS	5,−30	ER1451	GI		
64	4	10 μsF	TS					
				W6.5,−10,−33	MN1208	Panasonic		10
		300 nsF	TS	5	NCR52210	NCR		
					X2210	**Xicor**	**(3998)**	
					X2210DM	**† Xicor**	**(3998)**	
	8	4 μsF	TS	−29,5	ER2055	GI		
					NCR2055	NCR		
					NC7055	Nitron		
82	1	100 μsF	TS	5,−30	ER0082	GI		
100	14	3.4 msF	Serial	−35	ER1400	GI		
					NCR1400	NCR		
		2100 nsF						
			TS	−35	NCR1400	NCR		20
128	8	100 nsF	TS	5	**ER5901**	**GI**	**(3687)**	
					ER5901HR	**† GI**	**(3687)**	
		300 nsF	TS	5	NCR52001	NCR		
256	4	300 nsF	TS	5	NCR52212	NCR		
					X2212	**Xicor**	**(3998)**	
					X2212DM	**† Xicor**	**(3998)**	
	8	300 nsF	TS	5	NCR52002	NCR		
512	8	300 nsF	TS	5	NCR52004	NCR		
					X2804A	**Xicor**	**(3999)**	
		450 nsF	TS	5,±22	NCR4485	NCR		30
		5000 nsF						
			TS	5,−29	NCR2055	NCR		
1024								
	1	300 nsF	TS	5	NCR52201	NCR		
					X2201A	**Xicor**	**(3998)**	
					X2201ADM	**† Xicor**	**(3998)**	
	4	900 nsF	TS	−30,−12,5	ER3400	GI		
					NCR3400	NCR		
					NC7451	Nitron		
2048								
	4	1.6 μsF	TS	−24,−14,5	ER2810HR	† GI		
					ER2810IR	GI		
		1.65 μsF	TS	−23,−14,+5	NC7810	Nitron		40
		2 μsF	TS	−23,−14,5	NCR2811	NCR		
	8	6 μsF	TS	−29,−12,5	NCR2161	NCR		
					NCR2168	NCR		
		250 nsF	TS	5	**5213-250**	**SEEQ**	**(3882)**	
					5213H	**SEEQ**	**(3882)**	
					E5213	**SEEQ**	**(3889)**	
		300 nsF	TS	5	**ER5716**	**GI**	**(3683)**	
					ER5916	GI		
					ER5916HR	† GI		
					HN48016	**Hitachi**	**(3789)**	50
				21,5	ER5816	GI		
					ER5816HR	† GI		
		350 nsF	TS	5	**5213-350**	**SEEQ**	**(3882)**	
					M5213	**SEEQ**	**(3889)**	
2948								
	8	450 nsF	TS	5	NCR52817	NCR		
4096								
	8	250 nsF	TS	5	**5223**	**SEEQ**	**(3890)**	
		450 nsF	TS	5	NCR52832	NCR		

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature
OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY–EAROMs, FIFOs, LIFOs (Cont'd)

Words	Bits/ Word	Data Rate MHz (max)	Supply Voltage, V	Device	Source	Line
First-in First-out						
16	4	8.0 *	3-15	**CD40105B**	**†RCA (749)**	
				CD40105BE	**RCA (749)**	
		12.0	5	**SN54LS222**	**†TI (907)**	
				SN54LS224	**†TI (907)**	
				SN74LS222	**TI (907)**	
				SN74LS224	**TI (907)**	
		20.0	5	**SN54LS227**	**†TI (909)**	
				SN54LS228	**†TI (909)**	
				SN74LS227	**TI (909)**	
				SN74LS228	**TI (909)**	10
	5	10.0	5	SN75S225	TI	
24	4	2.5	5-16	MS618	† RTC	
32	8	0.5	– 12,5	AM2812C	AMD	
				AM2812L	AMD	
				MJ2812	Plessey	
				MJ2814	† Plessey	
		1.0	– 12,5	AM2812AC	AMD	
				AM2812AL	AMD	
	9	0.5	– 12,5	AM2813C	AMD	
				AM2813L	AMD	20
				MJ2813	Plessey	
		1.0	– 12,5	AM2813AC	AMD	
				AM2813AL	AMD	
40	9	0.5	– 12,5	FR1502-11	Western	
		1.0	– 12,5	33512	Fairchild	
				3351M	† Fairchild	
				FR1502-10	Western	
		1.5	– 12,5	3351-3	Fairchild	
		2.0	– 12,5	33511	Fairchild	
64	4	0.7	– 12,5	3341C	AMD	30
				3341	Fairchild	
				3341M	† Fairchild	
		1.0	– 12,5	AM2841C	AMD	
				AM2841M	† AMD	
				3341A	Fairchild	
				MJ2841	Plessey	
		1.2	– 12,5	2841A	AMD	
		7.0	5	**C57401**	**†MMI (722)**	
		8.0	5	9423C	Fairchild	
				9423M	† Fairchild	40
		10.0	5	**C57401A**	**†MMI (722)**	
				C67401	**MMI (722)**	
				C67401A	**MMI (722)**	
				C67401B	**MMI (722)**	
		20	12,5	**DM77S401**	**†National (3853)**	
				DM87S401	**National (3853)**	
	5	7.0	5	57402	† MMI	
				C57402	**MMI (722)**	
		10.0	5	**C57402A**	**MMI (722)**	
				C67402	**MMI (722)**	50
				C67402A	MMI	
				C67402B	**MMI (722)**	
		15.0	5	67401A	† MMI	
				C67402A	**MMI (722)**	
		20	12,5	**DM77S402**	**†National (3853)**	
				DM87S402	**National (3853)**	
	9	15.0	5	**TDC1030**	**TRW (813,816)**	
132/128						
	9	0.65	5	**WD1510-00**	**Western (3994)**	
		1.0	5	**WD1510-01**	**Western (3994)**	
Last-in First-out						
16	4	10.5	5	9406C	Fairchild	60
				9406M	Fairchild	
81	4	1.0	5	SR5018	SMC	
132/128						
	9	1.0	5	**WD1510-02**	**Western (3994)**	
133	4	1.0	5	SR5017	SMC	

† Military Temperature Range (– 55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

MEMORY–PLAs

PLAs

Organization	Propagation Time	Output	Supply Voltage, V	Device	Source		Line
Field Programmable Array Logic							
	12 ns *	TS	5	FP54ALS16R4†	TI		
				FP54ALS16R6†	TI		
				FP54ALS16R8†	TI		
				FP74ALS16R4	TI		
				FP74ALS16R6	TI		
				FP74ALS16R8	TI		
	25 ns *	TS	5	**PAL10H8C**	**MMI**	(4449)	
				PAL10H8M	**†MMI**	(4449)	
				PAL10L8C	**MMI**	(4449)	
				PAL10L8M	**†MMI**	(4449)	10
				PAL12H6C	**MMI**	(4449)	
				PAL12H6M	**†MMI**	(4449)	
				PAL12L6C	**MMI**	(4449)	
				PAL12L6M	**†MMI**	(4449)	
				PAL14H4C	**MMI**	(4449)	
				PAL14H4M	**†MMI**	(4449)	
				PAL14L4C	**MMI**	(4449)	
				PAL14L4M	**†MMI**	(4449)	
				PAL16A4C	**MMI**	(4449)	
				PAL16A4M	**†MMI**	(4449)	20
				PAL16C1C	**MMI**	(4449)	
				PAL16C1M	**†MMI**	(4449)	
				PAL16H2C	**MMI**	(4449)	
				PAL16H2M	**†MMI**	(4449)	
				PAL16L2C	**MMI**	(4449)	
				PAL16L2M	**†MMI**	(4449)	
				PAL16L8C	**MMI**	(4449)	
				PAL16L8M	**†MMI**	(4449)	
				PAL16R4C	**MMI**	(4449)	
				PAL16R4M	**†MMI**	(4449)	30
				PAL16R6C	**MMI**	(4449)	
				PAL16R6M	**†MMI**	(4449)	
				PAL16R8C	**MMI**	(4449)	
				PAL16R8M	**†MMI**	(4449)	
				PAL16X4C	**MMI**	(4449)	
				PAL16X4M	**†MMI**	(4449)	
				DMPAL10H8C	**National**	(737)	
				DMPAL10H8M	**†National**	(737)	
				DMPAL10L8C	**National**	(737)	
				DMPAL10L8M	**†National**	(737)	40
				DMPAL12H6C	**National**	(737)	
				DMPAL12H6M	**†National**	(737)	
				DMPAL12L6C	**National**	(737)	
				DMPAL12L6M	**†National**	(737)	
				DMPAL14H4C	**National**	(737)	
				DMPAL14H4M	**†National**	(737)	
				DMPAL14L4C	**National**	(737)	
				DMPAL14L4M	**†National**	(737)	
				DMPAL16A4C	National		
				DMPAL16A4M†	National		50
				DMPAL16C1C	**National**	(737)	
				DMPAL16C1M	**†National**	(737)	
				DMPAL16H2C	**National**	(737)	
				DMPAL16H2M	**†National**	(737)	
				DMPAL16L2C	**National**	(737)	
				DMPAL16L2M	**†National**	(737)	
				DMPAL16L8C	**National**	(737)	
				DMPAL16L8M	**†National**	(737)	
				DMPAL16R4C	**National**	(737)	
				DMPAL16R4M	**†National**	(737)	60
				DMPAL16R6C	**National**	(737)	
				DMPAL16R6M	**†National**	(737)	
				DMPAL16R8C	**National**	(737)	
				DMPAL16R8M	**†National**	(737)	
				DMPAL16X4C	National		
				DMPAL16X4M†	National		
				82S152	**Signetics**	(3919)	
				82S153	**Signetics**	(3919)	
						(Continued)	

Organization	Propagation Time	Output	Supply Voltage, V	Device	Source		Line
Field Programmable Array Logic						(Cont'd)	
	30 ns	OC	7	**82S150**	**Signetics**	(3917)	
		TS	7	**82S151**	**Signetics**	(3917)	70
Field Programmable Gate Array, 16 Inputs, 9 AND/NAND Gates, 9 Outputs, Field Programmable							
	40 nsF	OC	5	N82S102	Signetics		
		TS	5	N82S103	Signetics		
	50 nsF	OC	5	S82S102	† Signetics		
		TS	5	S82S103	† Signetics		
Field Programmable Gate Array, 6 Inputs, 12 AND Gates, 12 Outputs							
	20 ns*	OC	5	S82S150	† Signetics		
		TS	5	S82S151	† Signetics		
	25 nsF	OC	5	N8S150	Signetics		
		TS	5	N82S151	Signetics		
Field Programmable Logic Array, 8 Inputs, 32 AND Gates, 10 OR Gates, 10 Outputs							
	30 nsF	OC	5	N82S152A	Signetics		
		TS	5	N82S153A	Signetics		80
	40 nsF	OC	5	N82S152	Signetics		
		TS	5	N82S153	Signetics		
	45 nsF	OC	5	S82S152A	† Signetics		
		TS	5	S82S153A	† Signetics		
	60 nsF	OC	5	S82S152	† Signetics		
		TS	5	S82S153	† Signetics		
Field Programmable Logic Sequencer, 12 Inputs, 32 Product Terms							
	45 nsF *	OC	5	FP54LS335	† TI		
				FP74LS335	TI		
		TS	5	FP54LS333	† TI		
				FP73LS333	TI		90
Field Programmable Logic Sequencer, 4 Inputs, 32 AND Gates, 21 OR Gate							
	25 ns*	OC	5	S82S154	† Signetics		
				S82S156	† Signetics		
				S82S158	† Signetics		
		TS	5	S82S155	† Signetics		
				S82S157	† Signetics		
				S82S159	† Signetics		
Field Programmable Logic Sequencer, 4 Inputs, 32 AND Gates, 21 OR Gates							
	30 nsF	OC	5	N82S154	Signetics		
				N82S156	Signetics		
				N82S158	Signetics		
		TS	5	N82S155	Signetics		100
				N82S157	Signetics		
				N82S159	Signetics		
Field Programmable Logic Sequencer, 48 Transition Terms, 16 Inputs, 8 Outputs							
	30 nsF	OC	5	N82S104A	Signetics		
				S82S104	† Signetics		
				S82S104A	† Signetics		
		TS	5	N82S105A	Signetics		
				S82S105	† Signetics		
				S82S105A	† Signetics		
	90 nsF	OC	5	N82S104	Signetics		
				N82S104A	Signetics		110
				S82S104	† Signetics		
				S82S104A	† Signetics		
		TS	5	N82S105	Signetics		
				N82S105A	Signetics		
				S82S105	† Signetics		
Field Programmable Multiplexer, (10 inputs, four 10x8 programmable arrays, four 8:1 addressable multiplexers, four outputs)							
	55 nsF	TS	5	29693C	Raytheon		
	75 nsF	TS	5	29693M	† Raytheon		

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature
OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY-PLAs (Cont'd)

Organization	Propagation Time	Output	Supply Voltage, V	Device	Source		Line
PLAs						**(Cont'd)**	
Field Programmable ROM Patch, for Correcting or Changing the Program in Large ROMs							
	—	OC	5	N82S106	Signetics		
		TS	5	N82S107	Signetics		
32 Product Terms, Six Sum Terms, 14 Inputs							
	10 ns *	OC	5	FP54AS840	† TI		
				FP74AS840	TI		
		TS	5	FP54AS839	† TI		
				FP74AS839	TI		
32 Product Terms, 12 Inputs, Field Programmable							
	100 ns *	OC	5	SN54LS335	† TI		
				SN54LS336	† TI		
				SN74LS335	TI		
				SN74LS336	TI		10
		TS	5	SN54LS333	† TI		
				SN54LS334	† TI		
				SN74LS333	TI		
				SN74LS334	TI		
48 Product Terms, 14 Inputs, Field Programmable							
	100 nsF	OC	5	IM5200	Intersil		
48 Product Terms, 16 Inputs, Field Programmable							
	50 nsF	OC	5	**93458C**	**Fairchild**	**(3661)**	
				MC82S101C	Motorola		
				N82S101	Signetics		
		TS	5	**93458M**	**† Fairchild**	**(3661)**	
				93459C	**Fairchild**	**(3661)**	20
				MC82S100C	Motorola		
				N82S100	Signetics		
	80 nsF	OC	5	MC82S101M	† Motorola		
				S82S101	† Signetics		
		TS	5	MC82S100M	† Motorola		
				S82S100	† Signetics		
		OC	5	**93459M**	**† Fairchild**	**(3661)**	
50 Product Terms, 12 Inputs, 6 Outputs, Field Programmable							
	35 ns *	—	5	SN74S331	TI		
		TS	5	SN74S330	TI		
72 Product Terms, 24 Inputs, 16 Outputs, Field Programmable							
	200 nsF	TS	5	μPB450	NEC-Micro		30
96 Product Terms, 14 Inputs, Factory Programmable							
	150 nsF	—	5	DM7575	† National		
				DM7576	† National		
				DM8575	National		
				DM8576	National		

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

MEMORY-PROMs

PROMs

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	Line
16x16	—	Electrically Erasable	—	14	5	**MCM2801**	**Motorola (3839,3847)**	
32x32	15 μ5	Electrically Erasable	TS	14	5	**MCM2802**	**Motorola (3839)**	
32x8	15 nsF	TTL	OC	16	5	DM87S188	National	
			TS	16	5	DM87S288	National	
	20 nsF	TTL	OC	16	5	DM77S188	† National	
			TS	16	5	DM77S288	† National	
	20 nsR	ECL	OE	16	−5.2	SN10139	TI	
	22 nsF	ECL	OE	16	−5.2	10139	Signetics	
	25 nsF	ECL	OE	16	−5.2	MCM10139	Motorola	
		TTL	OC	16	5	AM27S18AC	AMD	10
						63S080	**MMI (3826)**	
			TS	16	5	AM27S19AC	AMD	
						63S081	**MMI (3826)**	
	35 nsF	TTL	OC	16	5	AM27S18AM	† AMD	
						53S080	**† MMI (3827)**	
						DM74S188	National	
						DM74S288	National	
			TS	16	5	AM27S19AM	† AMD	
						53S081	**† MMI (3827)**	
	40 nsF	TTL	OC	16	5	AM27S18C	AMD	20
						AM29750AC	AMD	
						HM7602-5	**Harris (3693)**	
						TBP18SA30	TI	
			TS	16	5	AM27S19C	AMD	
						AM29751AC	AMD	
						HM7603-5	**Harris (3693)**	
						TBP18S030	**TI (440,3965)**	
	45 nsF	TTL	OC	16	5	DM54S188	† National	
			TS	16	5	DM54S288	† National	
	50 nsF	TTL	OC	16	5	AM27LS18C	AMD	30
						AM27S18M	† AMD	
						AM29750AM	† AMD	
						HM7602-2	**† Harris (3693)**	
						6330-1	**MMI (3826)**	
						N82S23	Signetics	
						TBP18SA030M	**† TI (440,3965)**	
			TS	16	5	AM27LS19C	AMD	
						AM27S19M	† AMD	
						AM29751AM	† AMD	
						HM7603-2	**† Harris (3693)**	40
						6331-1	**MMI (3826)**	
						N82S123	Signetics	
						TBP18S030M	**† TI (440,3965)**	
	50 nsR	TTL	OC	16	5	SN54188A	† TI	
						SN74188A	TI	
	60 nsF	TTL	OC	16	5	JAN38510/ 207	† Harris	
						5330-1	† MMI	
			TS	16	5	5331-1	† MMI	
	65 nsF	TTL	—	16	5	IM5610C	Intersil	
			OC	16	5	IM5600C	Intersil	50
						S82S23	† Signetics	
			TS	16	5	AM27LS19M	† AMD	
						S82S123	† Signetics	
	75 nsF	TTL	—	16	5	IM5610M	† Intersil	
64x4	450 nsF	Electrically Erasable	TS	16	5	**SY2801**	**Synertek (3956)**	
						SY2801A	**Synertek (3956)**	
64x8	75 nsR	TTL	OC	24	5	SN74186	TI	
	140 nsF	TTL	TS	24	5	JAN-0512	† Harris	
						JAN38510/ 201	† Harris	
256x4	10 nsF	ECL	OE	16	−5.2	**F10Z416A**	**Fairchild (3619)**	60
	11 ns *	ECL	OE	16	−5.2	F10416C	Fairchild	
	12 ns *	ECL	OE	16	−5.2	GXB1049	Siemens	
	15 nsF	ECL	OE	16	−5.2	F100Z416	Fairchild	
						F10Z416	**Fairchild (3619)**	
	20 nsF	ECL	OE	16	4.5	100149	Signetics	
					5	100149	Signetics	
	20 nsR	ECL	OE	16	−5.2	10149	Signetics	
	24 nsF	ECL	OE	16	−5.2	**F100416C**	**Fairchild (3626)**	
	25 nsF	ECL	OE	16	−5.2	MCM10149	Motorola	
	30 nsF	TTL	OC	16	5	AM28S20AC	AMD	70
			TS	16	5	AM27S21AC	AMD	
	40 nsF	TTL	OC	16	5	AM27S20AM	† AMD	
						HM7610A-5	**Harris (3696)**	
			TS	16	5	AM27S21AM	† AMD	
						HM7611A-5	**Harris (3696)**	
	45 nsF	TTL	OC	16	5	AM27S20C	AMD	
						AM29760AC	AMD	
						93417C	Fairchild	
						63S140	**MMI (3826)**	
			TS	16	5	AM27S21C	AMD	80
						AM29761AC	AMD	
						93427C	Fairchild	
						63S141	**MMI (3826)**	
						29613A	† Raytheon	
						29613A	Raytheon	
	50 nsF	TTL	OC	16	5	DM74S387	National	
						N82S126	Signetics	
			TS	16	5	DM74S287	National	
						N82S129	Signetics	
	55 nsF	TTL	OC	16	5	53S140	† MMI	90
						6300-1	**MMI (3826)**	
						63LS140	**MMI (3826)**	
			TS	16	5	53S141	† MMI	
						6301-1	**MMI (3826)**	
						63LS141	**MMI (3826)**	
						TBP24S10	**TI (440,3967)**	
	60 nsF	TTL	OC	16	5	AM27S20M	† AMD	
						AM29760AM	AMD	
						93417M	† Fairchild	
						HM7610-5	**Harris (3696)**	100
						HM7610A-2	**† Harris (3696)**	
						DM54S387	† National	
						29613A	† Raytheon	
						29613A	Raytheon	
			TS	16	5	AM27S21M	† AMD	
						AM29761AM	† AMD	
						93427M	† Fairchild	
						HM7611-5	**Harris (3696)**	
						HM7611A-2	**† Harris (3696)**	
						DM54S287	† National	110
	65 nsF	TTL	OC	16	5	**TBP24SA10**	**TI (440,3967)**	
						TBP24SA10M	**† TI (440,3967)**	
			TS	16	5	**TBP24S10M**	**† TI (440,3967)**	
	70 nsF	TTL	OC	16	5	IM5603C	Intersil	
						S82S126	† Signetics	
			TS	16	5	IM5623C	Intersil	
						S82S129	† Signetics	
	75 nsF	TTL	OC	16	5	**HM7610-2**	**† Harris (3696)**	

(Continued)

† Military Temperature Range (−55° to 125°C)
ns*—Nanoseconds Typical
nsF—Nanoseconds over Full Temperature Range
nsR—Nanoseconds at Room Temperature
OC—Open Collector
TS—Three-State
OE—Open Emitter

MEMORY-PROMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source		Line
PROMs								**(Cont'd)**	
								(Cont'd)	
256x4	75 nsF	TTL	OC	16	5	JAN38510/ 301	† Harris		
						5300-1	† MMI		
						53LS140	† MMI		
						TBP247A10M	† TI		
			TS	16	5	**HM7611-2**	**† Harris**	**(3696)**	
						JAN38510/ 302	† Harris		
						5301-1	† MMI		
						53LS141	† MMI		
						TBP14S10M	**† TI**	**(3964)**	
	80 nsF	TTL	OC	16	5	IM5603M	† Intersil		10
						IM5623M	† Intersil		
	450 nsF	CMOS	TS	16	5	HM6611-2	† Harris		
						HM6611-9	Harris		
				18	5	HM6661	Harris		
	600 nsF	CMOS	TS	18	5	HM6661-5	Harris		
256x8	1 μs *	Erasable	TS	24	5	CDP18042CD	RCA		
	1 μsF	Erasable	TS	24	−9,5	1702A	AMD		
						1702AL	AMD		
	1.3 μsF	Erasable	TS	24	−9,5	8702A	AMD		
	1.5 μsF	Erasable	TS	24	−9,5	1702A-6	AMD		20
	1.7 μsF	Erasable	TS	24	−10,5	4702A	AMD		
	2.3 μsF	Erasable	TS	24	−9,5	MM8702A-4	National		
	60 nsF	TTL	TS	20	5	**DM74LS471**	**National**	**(3850)**	
	70 nsF	TTL	OC	20	5	**6308-1**	**MMI**	**(3826)**	
						TBP28LA22	**TI**	**(440,3969)**	
				24	5	**6335-1**	**† MMI**	**(3826)**	
			TS	20	5	**6309-1**	**MMI**	**(3826)**	
						DM54LS471	**† National**	**(3850)**	
						TBP28L22	**TI**	**(440,3969)**	
				24	5	**6336-1**	**MMI**	**(3826)**	30
	80 nsF	TTL	OC	20	5	5308-1	† MMI		
						TBP28LA22M	**† TI**	**(440,3969)**	
			TS	20	5	5309-1	† MMI		
						TBP28L22M	**† TI**	**(440,3969)**	
	110 nsF	Electrically Erasable	TS	18	5,21	**SY2802**	**Synertek**	**(3957)**	
	550 nsF	Erasable	TS	24	−9,5	1702A-1	AMD		
						1702AL-1	AMD		
	650 nsF	Erasable	TS	24	−9,5	1702A-2	AMD		
						1702AL-2	AMD		
	750 nsF	Erasable	TS	24	−9,5	9702A-1	AMD		40
		TTL	TS	16	5	HM76LS03-5	Harris		
512x4	30 nsF	TTL	OC	16	5	AM27S12AC	AMD		
			TS	16	5	AM27S13AC	AMD		
	40 nsF	TTL	OC	16	5	AM27S12AM	† AMD		
			TS	16	5	AM27S13AM	† AMD		
						29611A	Raytheon		
	45 nsF	TTL	OC	16	5	**HM7620A-5**	**Harris**	**(3699)**	
						63S240	**MMI**	**(3826)**	
			TS	16	5	**HM7621A-5**	**Harris**	**(3699)**	
						63S241	**MMI**	**(3826)**	50
	50 nsF	TTL	OC	16	5	AM27S12C	AMD		
						AM29770C	AMD		
						93436C	Fairchild		
						N82S130	Signetics		
			TS	16	5	AM27S13C	AMD		
						AM29771C	AMD		
						93446C	Fairchild		
								(Continued)	

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source		Line
								(Cont'd)	
512x4	50 nsF	TTL	TS	16	5	MCM7621A	Motorola		
						N82S131	Signetics		
				24	5	MCM7641A	Motorola		60
	55 nsF	TTL	OC	16	5	53S240	† MMI		
						DM74S570	National		
			TS	16	5	53S241	† MMI		
						DM74S571	National		
						DM74S571A	National		
						DM74S571B	National		
						29611	† Raytheon		
						29611	Raytheon		
	60 nsF	TTL	OC	16	5	AM27S12M	† AMD		
						AM29770M	† AMD		70
						93436M	† Fairchild		
						HM7620A-2	**† Harris**	**(3699)**	
						6305-1	**MMI**	**(3826)**	
						63LS240	**MMI**	**(3826)**	
			TS	16	5	AM27S13M	† AMD		
						AM29771M	† AMD		
						93446M	† Fairchild		
						HM7621A-2	**† Harris**	**(3699)**	
						6306-1	**MMI**	**(3826)**	
						63LS241	**MMI**	**(3826)**	80
						29613C	Raytheon		
	65 nsF	TTL	OC	16	5	DM54S570	† National		
			TS	16	5	DM54S571	† National		
						DM54S571A	† National		
						DM54S571B	† National		
	70 nsF	TTL	OC	16	5	**HM7620-5**	**Harris**	**(3699)**	
						S82S130	† Signetics		
			TS	16	5	**HM7621-5**	**Harris**	**(3699)**	
						MCM7621	Motorola		
						29611	† Raytheon		90
						29611	Raytheon		
						S82S131	† Signetics		
	75 nsF	TTL	OC	16	5	5305-1	† MMI		
						53LS240	† MMI		
			TS	16	5	5306-1	† MMI		
						53LS241	† MMI		
						29613M	† Raytheon		
	80 nsF	TTL	—	16	5	IM5624C	Intersil		
			OC	16	5	IM5604C	Intersil		
	85 nsF	TTL	OC	16	5	**HM7620-2**	**† Harris**	**(3699)**	100
						JAN38510/ 401	† Harris		
			TS	16	5	**HM7621-2**	**† Harris**	**(3699)**	
						JAN38510/ 402	† Harris		
	90 nsF	TTL	—	16	5	IM5624M	† Intersil		
			OC	16	5	IM5604M	† Intersil		
512x8	—	TTL	TS	22	5	AM27S27C	AMD		
						AM27S27M	† AMD		
				24	5	AM27S25AC	AMD		
						AM27S25AM	† AMD		
						AM27S25C	AMD		110
						AM27S25M	† AMD		
	20 ns *	TTL	TS	24	5	**TBP28R45**	**TI**	**(3974)**	
	35 ns *	TTL	TS	20	5	TBP28P42	TI		
				24	5	**TBP28P45**	**TI**	**(3973)**	
						TBP28S45	**TI**	**(3976)**	
	35 nsF	TTL	OC	20	5	AM27S28AC	AMD		
						MB7123H	**Fujitsu**	**(3679)**	
				24	5	AM27S30AC	AMD		
			TS	20	5	AM27S29AC	AMD		
						MB7124H	**Fujitsu**	**(3679)**	120
								(Continued)	

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

MEMORY–PROMs (Cont'd)

PROMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	Line
512x8	35 nsF	TTL	TS				(Cont'd)	
				24	5	AM27S31AC	AMD	
	40 nsF	TTL	OC	24	5	93438C	Fairchild	
			TS	24	5	93448C	Fairchild	
	45 nsF	TTL	OC	20	5	AM27S28AM	† AMD	
						MB7123E	**Fujitsu (3679)**	
						DM74S473A	National	
				24	5	AM27S30AM	† AMD	
						DM74S475A	National	
			TS	20	5	AM27S29AM	† AMD	
						MB7124E	**Fujitsu (3679)**	10
						HM7649A-5	**Harris (3708)**	
						DM74S472A	National	
						DM74S474B	National	
						N82S147A	Signetics	
				24	5	AM27S31AM	† AMD	
						DM74S474A	National	
	50 nsF	TTL	OC	24	5	**HM7640A-5**	**Harris (3702)**	
			TS	24	5	**HM7641A-5**	**Harris (3702)**	
	55 nsF	TTL	OC	20	5	AM27S28C	AMD	
				24	5	AM27S30C	AMD	20
						93438M	† Fairchild	
			TS	20	5	AM27S29C	AMD	
						6349-2	MMI	
				24	5	AM27S31C	AMD	
						93448M	† Fairchild	
						HM7649A-2	**Harris (3708)**	
						6341-2	**MMI (3826)**	
	60 ns *	TTL	TS	20	5	**TBP28L42**	**TI (440,3970)**	
				24	5	**TBP28L45**	**TI (3971)**	
	60 nsF	TTL	OC	20	5	HM7648-5	Harris	
						DM54S473A	† National	30
						DM74S473	National	
				24	5	DM54S475A	† National	
			TS	20	5	**HM7649-5**	**Harris (3708)**	
						DM54S472	† National	
						DM54S472A	† National	
						DM54S472B	† National	
						DM54S474A	† National	
						DM54S474B	† National	
						DM74S472	National	40
						TBP28S42	**TI (440,3975)**	
				24	5	AM27S15C	AMD	
						HM7647R-5	Harris	
						N82S115	Signetics	
						N82S141	Signetics	
						TBP28S46	**TI (440,3976)**	
	65 nsF	TTL	OC	20	5	AM27S28M	† AMD	
						DM54S473	† National	
						TBP28SA42	**TI (440,3976)**	
				24	5	DM54S475	† National	50
						DM74S475	National	
						TBP28SA46	**TI (440)**	
			TS	20	5	AM27S29M	† AMD	
				24	5	AM27S31M	† AMD	
						DM74S474	National	
	70 nsF	TTL	OC	20	5	**6348-1**	**MMI (3826)**	
				24	5	AM27S30M	† AMD	
						HM7640-5	**Harris (3702)**	
						HM7640A-2	**† Harris (3702)**	
						6340-1	**MMI (3826)**	60
			TS	20	5	**6349-1**	**MMI (3826)**	
						MCM7649	Motorola	
						29623	Raytheon	

(Continued)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	Line
512x8	70 nsF	TTL	TS	20	5		(Cont'd)	
						TBP28S42M	† TI	
						TBP28S42M	TI	
				24	5	**HM7641-5**	**Harris (3702)**	
						HM7641A-2	**† Harris (3702)**	
						5341-2	† MMI	
						6341-1	**MMI (3826)**	
						MCM7641	Motorola	70
						DM54S474	† National	
						TBP28S46M	**† TI (440,3976)**	
	80 nsF	TTL	OC	20	5	HM7648-2	Harris	
						5348-1	† MMI	
				24	5	5340-1	† MMI	
			TS	20	5	**HM7649-2**	**Harris (3708)**	
						5349-1	† MMI	
				24	5	HM7647R-2	† Harris	
						5341-1	† MMI	
	85 nsF	TTL	OC	20	5	**TBP28SA42M**	**† TI (440,3976)**	80
				24	5	**HM7640-2**	**† Harris (3702)**	
						TBP28SA46M	**† TI (440)**	
			TS	20	5	**TBP28S42M**	**† TI (440,3975)**	
						TBP28S42M	TI	
				24	5	**HM7641-2**	**† Harris (3702)**	
						JAN38510/ 208	† Harris	
	90 nsF	TTL	OC	24	5	5340-2	† MMI	
			TS	24	5	AM27S15M	† AMD	
						S82S115	† Signetics	
						S82S141	† Signetics	90
	200 nsF	CMOS	TS	24	5	**HM6641-2**	**† Harris (669,1333,3783)**	
						HM6641-9	**Harris (669,1333,3783)**	
	300 nsF	CMOS Erasable	TS	24	10	IM6654A	Intersil	
		TTL	TS	5		**X2804**	**Xicor (3999)**	
	450 nsF	CMOS Erasable	TS	24	5	IM6654-1	Intersil	
	550 nsF	CMOS Erasable	TS	24	5	IM6654	Intersil	
	600 nsF	CMOS Erasable	TS	24	5	IM6654M	† Intersil	
	650 nsF	Electrically Erasable	TS	24	5	HNVM3004	Hughes	
1024x4	30 ns *	TTL	OC	18	5	DM54S572A	† National	
						DM54S573A	† National	100
	35 nsF	TTL	OC	18	5	AM27S32AC	AMD	
						AM27S33AC	AMD	
						MB7121H	**Fujitsu (3679)**	
			TS	18	5	AM27S33AC	AMD	
						MB7122H	**Fujitsu (3679)**	
						63S441A	**MMI (3826,3830)**	
						N82S137B	Signetics	
	35 nsR	TTL	OC	18	5	**TBP24SA41**	**TI (440,3968)**	
						TBP24SA41M	**† TI (440,3968)**	
			TS	18	5	**TBP24S41**	**TI (440,3968)**	110
						TBP24S41M	**† TI (440,3968)**	
	40 nsF	TTL	OC	18	5	93452C	Fairchild	
			TS	18	5	93453C	Fairchild	
	45 nsF	TTL	OC	18	5	AM27S32AM	† AMD	
						MB7121E	**Fujitsu (3679)**	
						DM74S572A	National	
			TS	18	5	AM27S33AM	† AMD	
						MB7122E	**Fujitsu (3679)**	
						63S441	**MMI (3826,3830)**	

(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature
OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY-PROMs (Cont'd)

PROMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source		Line
1024x4	45 nsF	TTL	TS	18	5			(Cont'd)	
						DM74S573A	National		
						N82HS137	Signetics		
	50 nsF	TTL	OC	18	5	**HM7642A-5**	**Harris**	**(3705)**	
						HM7642P-5	**Harris**	**(3705)**	
			TS	18	5	**HM7643A-5**	**Harris**	**(3705)**	
						HM7643P-5	**Harris**	**(3705)**	
						63RA441	**MMI**	**(3826)**	
						MCM7643A	Motorola		
	55 nsF	TTL	OC	18	5	AM27S32C	AMD		
						93452M	† Fairchild		10
			TS	18	5	AM27S33C	AMD		
						93453M	† Fairchild		
						53S441	**† MMI**	**(3830)**	
						6353-2	MMI		
	60 nsF	TTL	—	16	5	HM7644-5	Harris		
			OC	18	5	**HM7642-5**	**Harris**	**(3705)**	
						6350-1	MMI		
						6352-1	**MMI**	**(3826)**	
						DM74S572	National		
			TS	18	5	**HM7643-5**	**Harris**	**(3705)**	20
						53RA441	† MMI		
						6351-1	MMI		
						6353-1	**MMI**	**(3826)**	
						DM74S573	National		
						N82S137	Signetics		
	65 nsF	TTL	OC	18	5	AM27S32M	† AMD		
			TS	18	5	AM27S33M	† AMD		
	70 nsF	TTL	OC	18	5	**HM7642A-2**	**† Harris**	**(3705)**	
						HM7642P-2	**† Harris**	**(3705)**	
			TS	18	5	**HM7643A-2**	**† Harris**	**(3705)**	30
						HM7643P-2	**† Harris**	**(3705)**	
						MCM7643	Motorola		
						S82S137A	† Signetics		
	75 nsF	TTL	OC	18	5	5350-1	† MMI		
						5352-1	† MMI		
						DM54S572	† National		
			TS	18	5	5351-1	† MMI		
						5353-1	† MMI		
						DM54S573	† National		
	80 nsF	TTL	TS	18	5	S82S137	† Signetics		40
	85 nsF	TTL	—	18	5	HM7644-2	† Harris		
						JAN38510/ 603	† Harris		
			OC	18	5	**HM7642-2**	**† Harris**	**(3705)**	
			TS	18	5	**HM7643-2**	**† Harris**	**(3705)**	
						JAN38510/ 602	† Harris		
	550 nsF	CMOS Erasable							
			TS	24	5	IM6653-1	Intersil		
	600 nsF	CMOS Erasable							
			TS	24	5	IM6653M	† Intersil		
1024x8	—	TTL	TS	24	5	AM27PS181	AMD		
						AM27PS181A	AMD		
						AM27PS281	AMD		50
						AM27PS281A	AMD		
						AM27S35AC	AMD		
						AM27S35AM	† AMD		
						AM27S35C	AMD		
						AM27S35M	† AMD		
						AM27S37A	AMD		

(Continued)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source		Line
1024x8								(Cont'd)	
	20 ns *	TTL	TS	24	5	**TBP28R85**	**TI**	**(3974)**	
	35 ns *	TTL	TS	24	5	**TBP28P85**	**TI**	**(3973)**	
						TBP28S85	**TI**	**(3977)**	
	35 nsF	TTL	OC	24	5	AM27S180AC	AMD		60
						AM27S280AC	AMD		
						AM27S37	AMD		
						93Z450A	**Fairchild**	**(3652)**	
			TS	24	5	AM27S181AC	AMD		
						AM27S281AC	AMD		
						93Z451A	**Fairchild**	**(3652)**	
						MB7132Y	**Fujitsu**	**(3679)**	
	40 nsF	TTL	REG	24	5	**DM77SR181**	**† National**	**(3852)**	
						DM87SR181	**National**	**(3852)**	
			TS	24	5	63RS881	MMI		70
	45 nsF	TTL	OC	24	5	93450C	Fairchild		
						93Z450	**Fairchild**	**(3652)**	
						MB7131H	**Fujitsu**	**(3679)**	
			TS	24	5	93451C	Fairchild		
						93Z451	**Fairchild**	**(3652)**	
						MB7132H	**Fujitsu**	**(3679)**	
						N82S181B	Signetics		
	50 nsF	TTL	OC	24	5	AM27S180AM	† AMD		
						AM27S280AM	† AMD		
						HM7680A-5	Harris		80
			TS	24	5	AM27S181AM	† AMD		
						AM27S281AM	† AMD		
						HM7681A-5	**Harris**	**(3711)**	
						3628A-1	Intel		
						82HS181	Intel		
						MCM7681A	Motorola		
	55 nsF	TTL	OE	24	5	**MB7131E**	**Fujitsu**	**(3679)**	
			TS	24	5	**MB7132E**	**Fujitsu**	**(3679)**	
						53RS881	MMI		
						6381-2	**MMI**	**(3826)**	90
						DM87S280	**National**	**(3851)**	
						DM87S281	**National**	**(3851)**	
						N82S181A	Signetics		
	60 nsF	TTL	OC	24	5	AM27S180C	AMD		
						AM27S280C	AMD		
						AM27S281C	AMD		
						93450M	† Fairchild		
						93460M	† Fairchild		
						93L450C	Fairchild		
						N82HS180	Signetics		100
						SN74S2708	TI		
						TBP28S86-60	**TI**	**(440,3977)**	
						TBP28SA86-60	**TI**	**(3978)**	
			TS	24	5	AM27S181C	AMD		
						93451M	† Fairchild		
						93L451C	Fairchild		
						29631A	† Raytheon		
						29631A	Raytheon		
						29633A	† Raytheon		
						29633A	Raytheon		110
						N82S183	Signetics		
	65 ns *	TTL	TS	24	5	TBP28L85	TI		
	70 nsF	TTL	OC	24	5	HM7680-5	Harris		
						HM7680P-5	Harris		
						HM7680R-5	Harris		
						HM7680RP-5	Harris		
						6380-2	**MMI**	**(3826)**	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

MEMORY-PROMs (Cont'd)

PROMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source		Line
1024x8	70 nsF	TTL	OC	24	5			(Cont'd)	
						MCM7680C	Motorola		
						MCM82707C	Motorola		
						DM87S180	National		
						N82S180	Signetics		
			TS	24	5	HM7608-5	Harris		
						HM7681-5	**Harris**	**(3711)**	
						HM7681A-2	**Harris**	**(3711)**	
						HM7681P-5	**Harris**	**(3711)**	
						HM7681R-5	**Harris**	**(3711)**	
						HM7681RP-5	**Harris**	**(3711)**	10
						3628A-3	Intel		
						82S181	Intel		
						5381-2	† MMI		
						MCM7681C	Motorola		
						MCM82708C	Motorola		
						DM87S181	National		
						29633A	† Raytheon		
						29633A	Raytheon		
						N82S181	Signetics		
	75 nsF	TTL	OC	24	5	93L450M	† Fairchild		20
						TBP28SA86M	**† TI**	**(3978)**	
			TS	24	5	93L451M	† Fairchild		
						DM77S280	**† National**	**(3851)**	
						DM77S281	**† National**	**(3851)**	
						29637	Raytheon		
						TBP24S86M	† TI		
						TBP28S2708	**† TI**	**(3980)**	
	80 ns *	TTL	TS	24	5	**TBP28L86**	**TI**	**(440,3972)**	
						TBP28L86M	**† TI**	**(440,3972)**	
	80 nsF	TTL	OC	24	5	AM27S180M	† AMD		30
						AM27S280M	† AMD		
						S82HS180	† Signetics		
			TS	24	5	AM27S181M	† AMD		
						AM27S281M	† AMD		
						S82HS181	† Signetics		
						S82S181A	† Signetics		
	85 nsF	TTL	OC	24	5	MCM7680M	† Motorola		
						MCM82707M	† Motorola		
			TS	24	5	MCM7681M	† Motorola		
						MCM82708M	† Motorola		40
	90 nsF	TTL	OC	24	5	HM7680-2	† Harris		
						HM7680P-2	† Harris		
						HM7680R-2	† Harris		
						HM7680RP-2	† Harris		
						5380-2	† MMI		
						6380-1	**MMI**	**(3826)**	
						DM77S180	† National		
						S82S180	† Signetics		
			TS	24	5	HM7608-2	† Harris		
						HM7681-2	**† Harris**	**(3711)**	50
						HM7681P-2	**† Harris**	**(3711)**	
						HM7681R-2	**† Harris**	**(3711)**	
						HM7681RP-2	**† Harris**	**(3711)**	
						3628A-4	Intel		
						6381-1	**MMI**	**(3826)**	
						DM77S181	† National		
						29635C	Raytheon		
						29637C	Raytheon		
						82PS181	Signetics		
						S82S181	† Signetics		60
						S82S183	† Signetics		
						S82S2708	† Signetics		

(Continued)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source		Line
1024x8								(Cont'd)	
	95 nsF	TTL	TS	24	5	29633C	Raytheon		
	120 nsF	TTL	TS	24	5	N82LS181	Signetics		
	125 nsF	TTL	OC	24	5	5380-1	† MMI		
			TS	24	5	5381-1	† MMI		
						29637M	† Raytheon		
	175 nsF	TTL	TS	24	5	S82LS181	† Signetics		
	300 nsF	Erasable	TS	24	5	HM6758-9	Harris		
					±5,12	MCM27A08	Motorola		
						MCM68A708	Motorola		70
	350 nsF	Erasable	TS	24	±5,12	2708-13	AMD		
						F2708-1	Fairchild		
						TMS2708-35	**TI**	**(442)**	
	450 nsF	CMOS Erasable							
			TS	24	5	IM6658	Intel		
						IM6658M	† Intel		
		Erasable	TS	24	5	MM2758	National		
						MSM2758	OKI		
					±5,12	2708	AMD		
						AM9708	† AMD		80
						F2708	Fairchild		
						F68708	Fairchild		
						MCM2708	Motorola		
						MCM68708	Motorola		
						INS8708	National		
						MSM2708	**OKI**	**(3873)**	
						MN2708	Panasonic		
						TMS2708-45	**TI**	**(442)**	
						TMS27L08-45	**TI**	**(442)**	
	650 nsF	Electrically Erasable							
			TS	24	5	HNVM3008	Hughes		90
						HNVM3708	Hughes		
2048x4	—	TTL	OC	20	5	MCM7688	Motorola		
			TS	20	5	MCM7689	Motorola		
						TBP28R165	**TI**	**(3975)**	
	35 nsF	TTL	OC	18	5	AM27S184AC	AMD		
			TS	18	5	AM27S185AC	AMD		
						63S841A	**MMI**	**(3826,3833)**	
	45 ns *	TTL	OC	18	5	SN54S455	† TI		
						SN74S455	TI		
						TBP24SA81	**TI**	**(440,3969)**	100
						TBP24SA81M	**† TI**	**(440,3969)**	
			TS	18	5	**TBP24S81**	**TI**	**(440,3968)**	
						TBP24S81M	**† TI**	**(440,3968)**	
	45 nsF	TTL	OC	18	5	AM27S184AM	† AMD		
						MB7127H	**Fujitsu**	**(3679)**	
			TS	18	5	AM27S185AM	† AMD		
						MB7128H	**Fujitsu**	**(3679)**	
						N82S185B	Signetics		
	50 nsF	TTL	OC	18	5	AM27S184C	AMD		
			TS	18	5	AM27S185C	AMD		110
						HM7685A-5	**Harris**	**(3714)**	
						53S841A	**† MMI**	**(3833)**	
						63S841	**MMI**	**(3826,3833)**	
						N82S185A	Signetics		
	55 nsF	TTL	OC	18	5	AM27S184M	† AMD		
			TS	18	5	AM27S185M	† AMD		
						MB7128E	**Fujitsu**	**(3679)**	
						MB7128E-W	**Fujitsu**	**(3679)**	
						53S841	**† MMI**	**(3833)**	
						6389-2	**MMI**	**(3826)**	120
	60 nsF	TTL	OC	18	5	AM27LS184C	AMD		
						DM87S184	National		

(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature
OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY–PROMs (Cont'd)

PROMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	Line
2048x4	60 nsF	TTL					(Cont'd)	
			TS	18	5	AM27LS185C	AMD	
						AM27PS185C	AMD	
						DM87S185	National	
						29651A	Raytheon	
						29653A	Raytheon	
				24	5	N82S191A	Signetics	
	65 nsF	TTL	OC	18	5	AM27LS184M†	AMD	
			TS	18	5	AM27LS185M†	AMD	
						AM27PS185M†	AMD	
	70 nsF	TTL	OC	18	5	HM7684-5	Harris	10
						HM7684P-5	Harris	
						6388-1	**MMI (3826)**	
						MCM7684C	Motorola	
			TS	18	5	**HM7685-5**	**Harris (3714)**	
						HM7685P-5	**Harris (3714)**	
						5389-2	† MMI	
						6389-1	**MMI (3826)**	
						MCM7685C	Motorola	
						MCM7686	Motorola	
						MCM7687	Motorola	20
						29651C	Raytheon	
	75 nsF	TTL	OC	18	5	DM77S184	† National	
			TS	18	5	DM77S185	† National	
						29653C	Raytheon	
	80 nsF	TTL	TS	18	5	S82HS185	† Signetics	
						S82S185A	Signetics	
				24	5	S82S191A	† Signetics	
	85 nsF	TTL	OC	18	5	MCM7684M	† Motorola	
			TS	18	5	MCM7685M	† Motorola	
	90 nsF	TTL	OC	18	5	HM7684-2	† Harris	30
						HM7684P-2	† Harris	
			TS	18	5	**HM7685-2**	**† Harris (3714)**	
						HM7685P-2	**† Harris (3714)**	
						29651M	† Raytheon	
	95 nsF	TTL	TS	18	5	29653M	† Raytheon	
	100 nsF	TTL	OC	18	5	5388-1	† MMI	
			TS	18	5	5389-1	† MMI	
						N82S185	Signetics	
	115 nsF	TTL	TS	18	5	S82S185	† Signetics	
	450 nsF	CMOS Erasable						
			TS	24	5	IM6657	Intersil	40
						IM6657M	† Intersil	
2048x8	—	TTL	TS	24	5	AM27S45	AMD	
						AM27S45A	AMD	
						AM27S47	AMD	
						AM27S47A	AMD	
	20 ns *	TTL	TS	24	5	**TBP28R166**	**† TI (440,3975)**	
	35 ns *	TTL	OC	24	5	**TBP28SA166**	**TI (440,3979)**	
			TS	24	5	**TBP28P166**	**† TI (3973)**	
						TBP28S166	**TI (440,3979)**	
	35 nsF	TTL	OC	24	5	AM27S190AC	AMD	50
						AM27S290AC	AMD	
			TS	24	5	AM27S191A	AMD	
						AM27S291A	AMD	
						3636B-1	Intel	
						63S1681A	MMI	
	45 nsF	TTL	OC	24	5	932510C	Fairchild	
						93510M	† Fairchild	
						93Z510C	**Fairchild (3655)**	
						MB7137H	**Fujitsu (3679)**	
			TS	24	5	932511C	Fairchild	60

(Continued)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	Line
2048x8	45 nsF	TTL	TS	24	5		(Cont'd)	
						93Z511C	**Fairchild (3655)**	
						MB7138H	**Fujitsu (3679)**	
						3636B-2	Intel	
	50 nsF	TTL	OC	24	5	AM27S190C	AMD	
						AM27S290AM†	AMD	
						AM27S290C	AMD	
			TS	18	5	MCM7685A	Motorola	
				24	5	AM27PS191C	AMD	
						AM27PS291AC	AMD	
						AM27PS291C	AMD	70
						AM27S191	AMD	
						AM27S191AM†	AMD	
						AM27S291	AMD	
						AM27S291AM†	AMD	
						HM76161A-5	**Harris (3717)**	
						HM7616A	**Harris (3720)**	
						82HS191	Intel	
						53S1681A	† MMI	
						63S1681	MMI	
						MCM76161A	Motorola	80
						29681A	† Raytheon	
						29681A	Raytheon	
						29683A	† Raytheon	
						29683A	Raytheon	
	55 nsF	TTL	OC	24	5	932510M	† Fairchild	
						93510C	Fairchild	
						93Z510M	**† Fairchild (3655)**	
			TS	24	5	93511C	Fairchild	
						93Z511M	**† Fairchild (3655)**	
						MB7138E	**Fujitsu (3679)**	90
	65 nsF	TTL	OC	24	5	AM27S190M	† AMD	
			TS	24	5	AM27PS191M†	AMD	
						AM27PS291AM†	AMD	
						AM27S291M	† AMD	
						93511M	† Fairchild	
						53S1681	† MMI	
						DM87S291	National	
	70 nsF	TTL	OC	24	5	DM87S190	National	
			TS	24	5	82S191	Intel	
						MCM76161	Motorola	100
						DM87S191	National	
						29681A	† Raytheon	
						29681A	Raytheon	
						29683A	† Raytheon	
						29683A	Raytheon	
	75 ns *	TTL	TS	24	5	**TBP28L166**	**TI (440)**	
	80 nsF	TTL	OC	24	5	HM76160-5	Harris	
						DM77S190	† National	
			TS	24	5	**HM7616-5**	**Harris (3720)**	
						HM76161-5	**Harris (3717)**	110
						M3636	† Intel	
						DM77S191	† National	
						DM77S291	† National	
						29681	Raytheon	
						N82S191	Signetics	
	85 nsF	TTL	TS	24	5	29683	Raytheon	
	100 nsF	TTL	OC	24	5	HM76160-2	† Harris	
			TS	24	5	**HM7616-2**	**† Harris (3720)**	
						HM76161-2	**† Harris (3717)**	
						S82S191	† Signetics	120
	175 nsF	CMOS	TS	24	5	**HM6616-2**	**† Harris (669,1333,3786)**	
						HM6616-9	**Harris (669,1333,3786)**	
	250 nsF	Electrically Erasable						
			TS	24	5	2815	Intel	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

MEMORY–PROMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	Line
PROMs						**(Cont'd)**		
2048x8	250 nsF	Electrically Erasable						
			TS	24	5			(Cont'd)
						2816	**Intel**	**(3824)**
						M2816	† Intel	
						NMC2816-25	**National**	**(3861,3863)**
						NMC2816E-25	**National**	**(3861,3863)**
						NMC2816M-25	**National**	**(3861,3863)**
						NMC9716-25	**National**	**(3868)**
						NMC9716E-25	**National**	**(3868)**
						NMC9716H-25	**National**	**(3868)**
					5,21	SY2816	Synertek	
				28	5	**2817**	**Intel**	**(3825)** 10
						MSM2816	OKI	
		Erasable	TS	24	5	MCM2716-25	Motorola	
						MCM27L16-25	Motorola	
	300 nsF	Erasable	TS	24	5	AM9716	AMD	
						MK2716-5	Mostek	
					±5,12	TMS27A16	Motorola	
		NMOS	TS	24	±5,12	TMS2716-30	TI	
		TTL	TS	5		**X2816**	**Xicor**	**(3999)**
	350 nsF	Electrically Erasable						
			TS	24	5	2815-3	Intel	
						2816-3	**Intel**	**(3824)** 20
						NMC2816-35	**National**	**(3861,3863)**
						NMC2816E-35	**National**	**(3861,3863)**
						NMC2816M-35	**National**	**(3861,3863)**
						NMC9716-35	**National**	**(3868)**
						NMC9716E-35	**National**	**(3868)**
						NMC9716H-35	**National**	**(3868)**
						M2716	SGS	
				28	5	**2817-3**	**Intel**	**(3825)**
				29	5	2816	Intel	
		Erasable	TS	24	5	AM2716-1	AMD	30
						F2716-1	Fairchild	
						MBM2716H	Fujitsu	
						HM6716-2	† Harris	
						HM6716-9	Harris	
						2716-1	**Intel**	**(3818,3822)**
						MK2716-6	Mostek	
						MKB2716-86	† Mostek	
						MCM2716-35	Motorola	
						MCM27L16-35	Motorola	
						MM2716-1	National	40
						NMC6716-1	National	
						SY2716-1	Synertek	
						TMM323-1	Toshiba	
	390 nsF	Erasable	TS	24	5	AM2716-2	AMD	
								(Continued)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	Line
2048x8	390 nsF	Erasable	TS	24	5			(Cont'd)
						HN462716-2	**Hitachi**	**(3789)**
						2716-2	**Intel**	**(3818,3822)**
						MK2716-7	Mostek	
						MKB2716-87	† Mostek	
						MM2716-2	National	
						NMC6716-2	National	50
						SY2716-2	Synertek	
	450 nsF	Electrically Erasable						
			TS	24	5	2815-4	Intel	
						NMC2816-45	**National**	**(3861,3863)**
						NMC2816E-45	**National**	**(3861,3863)**
						NMC2816M-45	**National**	**(3861,3863)**
						NMC9716	**National**	**(3868)**
						NMC9716-45	**National**	**(3868)**
						NMC9716E-45	**National**	**(3868)**
						NMC9716M-45	**National**	**(3868)**
				28	5	**2816-4**	**Intel**	**(3824)** 60
						2817-4	**Intel**	**(3825)**
						M2817	† Intel	
		Erasable	TS	24	5	AM2716	AMD	
						AM2716M	† AMD	
						F2716	Fairchild	
						F68716	Fairchild	
						MBM2716	Fujitsu	
						HN462716	**Hitachi**	**(3789)**
						2716	**Intel**	**(3818,3822)**
						M2716	Intel	70
						M2716M	† Intel	
						M5L2716	Mitsubishi	
						MK2716-8	Mostek	
						MKB2716	† Mostek	
						MKB2716-88	† Mostek	
						MCM2716	Motorola	
						MCM27L16	Motorola	
						MM2716	National	
						NMC2716E	National	
						NMC27C16-45	**National**	**(3864)** 80
						NMC6716	National	
						μPD2716	NEC-Micro	
						MSM2716	**OKI**	**(3873)**
						MN2716	Panasonic	
						SY2716	Synertek	
					±5,12	TMS2716	Motorola	
						TMS2716-45	TI	
	490 nsF	Erasable	TS	24	5	**2716-5**	**Intel**	**(3818,3822)**
	550 nsF	Erasable	TS	24	5	MKB2716-90	† Mostek	
						NMC27C16-55	**National**	**(3864)** 90
	650 nsF	Erasable	TS	24	5	**2716-6**	**Intel**	**(3818,3822)**
						MK2716-12	Mostek	
						NMC27C16-65	**National**	**(3864)**
4096x4	35 nsF	TTL	OC	20	5	AM27S40A	AMD	
			TS	20	5	AM27S41A	AMD	
						63S1641A	**MMI**	**(3826,3836)**
						N82HS195	Signetics	
	50 nsF	TTL	OC	20	5	AM27S40	AMD	
						AM27S40AM	† AMD	
			TS	20	5	AM27PS41	AMD	100
								(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature
OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY-PROMs (Cont'd)

PROMs

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	Line
4096x4	50 nsF	TTL	TS	20	5	AM27S41	AMD	
						AM27S41AM	† AMD	
						53S1641A	**† MMI (3836)**	
						63S1641	**MMI (3826,3836)**	
						S82HS195	† Signetics	
	60 nsF	TTL	TS	20	5	HM76165-5	Harris	
	65 nsF	TTL	OC	20	5	AM27S40M	† AMD	
			TS	20	5	AM27S41M	† AMD	
						53S1641	**† MMI (3836)**	
	80 nsF	TTL	TS	20	5	HM76165-2	Harris	10
	200 nsF	CMOS	TS	20	5	HM6646	Harris	
4096x8	—	TTL	TS	24	5	AM27PS43	AMD	
						AM27S43	AMD	
						AM27S43A	AMD	
	40 nsF	TTL	TS	24	5	3632-1	Intel	
						82HS321	Intel	
	50 nsF	TTL	TS	24	5	3632	Intel	
						82S321	Intel	
	55 nsF	TTL	OC	24	5	**MB7141H**	**Fujitsu (3679)**	
			TS	20	5	**MB7142H**	**Fujitsu (3679)**	20
	65 nsF	TTL	OC	24	5	**MB7141E**	**Fujitsu (3679)**	
			TS	20	5	**MB7142E**	**Fujitsu (3679)**	
				24	5	**HM76321-5**	**Harris (3726)**	
				28	5	MB7142E-W	† Fujitsu	
	70 nsF	TTL	TS	24	5	29671A	† Raytheon	
						29671A	Raytheon	
	75 nsF	TTL	TS	24	5	**HM76321-2**	**Harris (3726)**	
	80 nsF	TTL	TS	24	5	29671	† Raytheon	
						29671	Raytheon	
						29671A	† Raytheon	30
						29671A	Raytheon	
						N82S321	Signetics	
	85 nsF	TTL	TS	24	5	29673	† Raytheon	
						29673	Raytheon	
	100 nsF	TTL	TS	24	5	29671	† Raytheon	
						29671	Raytheon	
	105 nsF	TTL	TS	24	5	29673	† Raytheon	
						29673	Raytheon	
	200 nsF	Erasable	TS	24	5	MBM2732A-20	Fujitsu	
						2732A-2	Intel	40
						2732A-20	Intel	
	250 nsF	Erasable	TS	24	5	MBM2732A-25	Fujitsu	
						2732A	**Intel (3819,3822)**	
						2732A-25	Intel	
						MCM2532-25	Motorola	
						MCM25L32-25	Motorola	
						TMM2732-2	Toshiba	
	300 nsF	Erasable	TS	24	5	MBM2732A-30	Fujitsu	
						MBM2732A-30X	Fujitsu	
						2732A-3	Intel	50
						2732A-30	Intel	
	350 nsF	Erasable	TS	24	5	AM2732-1C	AMD	
						MBM2732A-35	Fujitsu	
						MCM2532-35	Motorola	
						NMC27C32-35	**National (3865)**	

(Continued)

PROMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	Line
4096x8	350 nsF	NMOS	TS	24	5	M58735	Mitsubishi	
	450 nsF	Erasable	TS	24	5	AM2732	AMD	
						AM2732M	† AMD	
						F2732	Fairchild	
						HN462532	**Hitachi (3789)**	60
						HN462732	**Hitachi (3789)**	
						2732A-4	Intel	
						M2732A	† Intel	
						M5L2732	Mitsubishi	
						MCM2532	Motorola	
						MCM25L32	Motorola	
						NMC2532	National	
						NMC27C32-45	**National (3865)**	
						μPD2732	NEC-Micro	
						MSM2732	OKI	70
						TMM2732	Toshiba	
	550 nsF	Erasable	TS	24	5	M2732/S8416	† Intel	
						NMC27C32-55	**National (3865)**	
	650 nsF	Erasable	TS	24	5	**NMC27C32-65**	**National (3865)**	
8192x8	45 nsF	TTL	OC	24	5	**93Z564**	**Fairchild (3658)**	
			TS	24	5	**93Z565**	**Fairchild (3658)**	
	55 nsF	TTL	OC	24	5	**MB7143H**	**Fujitsu (3678)**	
			TS	24	5	**MB7144H**	**Fujitsu (3678)**	
	85 nsF	TTL	TS	24	5	**HM76641-5**	**Harris (3729)**	
	95 nsF	TTL	TS	24	5	**HM76641-2**	**Harris (3729)**	80
	200 nsF	Electrically Erasable	TS	28	5	TMM2764	Toshiba	
		Erasable	TS	28	5	AM2764-2	AMD	
						AM2764-20	AMD	
						MBM2764-20	**Fujitsu (3674)**	
						2764-2	**Intel (3820,3822)**	
						TMM2764-2	Toshiba	
	250 nsF	CMOS, Erasable	TS	28	5	**MBM27C64-25**	**Fujitsu (3674)**	
		Erasable	TS	28	5	AM2764	AMD	
						AM2764-25	AMD	
						2764	Fairchild	90
						MBM2764-25	**Fujitsu (3674)**	
						2764	**Intel (3820,3822)**	
						2764-25	**Intel (3820,3822)**	
						M2764/S8460	† Intel	
						M2764/S8462	† Intel	
	300 nsF	CMOS, Erasable	TS	28	5	**MBM27C64-30**	**Fujitsu (3674)**	
		Erasable	TS	28	5	AM2764-3	AMD	
						AM2764-30	AMD	
						MBM2764-30	**Fujitsu (3674)**	
						HN482764	**Hitachi (3789)**	100
						2764-3	**Intel (3820,3822)**	
						2764-30	**Intel (3820,3822)**	
	350 nsF	Erasable	TS	24	5	MCM6874-35	Motorola	
						MCM68766-35	**Motorola (3839)**	
						MCM68L764-35	Motorola	

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† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

MEMORY-PROMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source		Line
PROMs								**(Cont'd)**	
								(Cont'd)	
8192x8	350 nsF	Erasable	TS						
				28	5	**5133-350**	**SEEQ**	**(3891)**	
						TMS2564-35	**TI**	**(442)**	
	450 nsF	Erasable	TS	24	5	**MCM68764**	**Motorola**	**(3839)**	
						MCM68766	**Motorola**	**(3839)**	
				28	5	AM2764-4	AMD		
						AM2764-45	AMD		
						2764-4	**Intel**	**(3820,3822)**	
						2764-45	**Intel**	**(3820,3822)**	
						M2764/S8461†	Intel		
						M2764/S8463†	Intel		10
						M5L2764	Mitsubishi		
						MSM2764A	**OKI**	**(3873)**	
						TMS2564-45	**TI**	**(442)**	
	500 nsF	Erasable	TS	28	5	**TMS2564-50**	**TI**	**(442)**	
16384x8	200 nsF	Erasable	OE	28	5	M27128	† Intel		
	250 nsF	Erasable	OE	28	5	**27128**	**Intel**	**(3821)**	
						27128-2	**Intel**	**(3821)**	
						27128-25	**Intel**	**(3821)**	
			TS	28	5	**MBM27128-25**	**Fujitsu**	**(3674)**	
						5143	**SEEQ**	**(3896)**	20
	300 nsF	Erasable	OE	28	5	**27128-3**	**Intel**	**(3821)**	
						27128-30	**Intel**	**(3821)**	
			TS	28	5	**MBM27128-30**	**Fujitsu**	**(3674)**	
	450 nsF	Erasable	OE	28	5	**27128-4**	**Intel**	**(3821)**	
						27128-45	**Intel**	**(3821)**	
						M27128-45	† Intel		

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature
OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY–RAMs

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	Line
Bubble								
Note: Bubble Memory Support Circuits (controllers, function drivers, coil drivers, sense amplifiers), see Digital-TTL (Volume I)								
1 Megabit (4096x256x1)				20		7110	Intel	
						BPK70	**Intel** (3808)	
74032-Bits Serial	370 ms	NMOS	—	18		**FBM31DB**	**Fujitsu A** (3668)	
83354-Bits Serial	4.5 ms	NMOS	—	18		**FBM32DA**	**Fujitsu A** (3668)	
273745-Bits Serial	6.0 ms		—	20		**FBM43DA**	**Fujitsu A** (3671)	
283026-Bits Serial	8.5 ms	NMOS	—	16		**FBM42DA**	**Fujitsu A** (3671)	
296128-Bits Serial	370 ms					**FBC304M1A**	**Fujitsu A** (3668)	
324024-Bits Serial	4.5 ms	—	—	5		**FBC304D2A**	**Fujitsu A** (3668)	
CCD								
32768-Bits (4096x8x1)			TS	16	±5,12	F232	Fairchild	10
65535-Bits (4096x16x1)			TS	16	±5,12	F264	Fairchild	
Dynamic								
2048x8	50 nsF	NMOS	OC	24	5	μPB409	NEC-Micro	
			TS	24	5	μPB429	NEC-Micro	
4096x1	120 nsF	NMOS	TS	16	±5,12	IM7027-1	Intersil	
						MK4027-1	Mostek	
						MCM4027A-1	Motorola	
	135 nsF	NMOS	TS	22	±5,15	μPD411-4	NEC-Micro	
	150 nsF	NMOS	TS	16	±5,12	MK4027-2	Intersil	
						ITT4027-2	ITT	
						MK4027-2	Mostek	20
						MCM4027A-2	Motorola	
						M4027-2	SGS	
				22	±5,12	μPD411-3	NEC-Micro	
	200 nsF	NMOS	TS	16	±5,12	IM7027-3	Intersil	
						MK4027-3	Intersil	
						ITT4027-3	ITT	
						MK4027-3	Mostek	
						MKB4027-83	Mostek	
						MCM4027A-3	Motorola	
						M4027-3	SGS	30
				18	−5,12	90L50E	AMD	
				22	±5,12	90L60E	AMD	
						MM5280	National	
						μPD411-2	NEC-Micro	
						μPD411A-2	NEC-Micro	
	250 nsF	NMOS	TS	16	±5,12	IM7027-4	Intersil	
						MK4027-4	Intersil	
						ITT4027-4	ITT	
						MK4027-4	Mostek	
						MKB4027-84	Mostek	40
						MCM4027A-4	Motorola	
						M4027-4	SGS	
				18	±5,12	90L50D	AMD	
				22	±5,12	90L60D	AMD	
						μPD411-1	NEC-Micro	
						μPD411A-1	NEC-Micro	
	270 nsF	NMOS	TS	22	±5,12	MM4280	National	
						MM5280-5	National	

(Continued)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	Line
4096x1							(Cont'd)	
	300 nsF	NMOS	TS	18	−5,12	90L50C	AMD	
				22	±5,12	90L60C	AMD	50
						μPD411	NEC-Micro	
						μPD411A	NEC-Micro	
	350 nsF	NMOS	TS	16	±5,12	ITT4027-6	ITT	
8192x1	150 nsF	NMOS	TS	16	±5,12	MM5298-2	National	
	200 nsF	NMOS	TS	16	±5,12	MM5298-3	National	
	250 nsF	NMOS	TS	16	±5,12	MM5298-4	National	
8192x8	100 nsF	CMOS	—	28	5	**MB8464-10**	**Fujitsu** (3672)	
						MB8464-10L	**Fujitsu** (3672)	
	150 nsF	CMOS	—	28	5	**MB8464-15**	**Fujitsu** (3672)	
						MB8464-15L	**Fujitsu** (3672)	60
16384x1	55 nsF	NMOS	TS	20	5	M5M2167-55	Mitsubishi	
	70 nsF	NMOS	TS	20	5	M5M2167-70	Mitsubishi	
	80 nsF	NMOS	TS	16	5	NMC5295-2	National	
	100 nsF	NMOS	TS	16	5	MB8117-10	Fujitsu	
						MB8118-10	Fujitsu	
						HM8416A-3	Hitachi	
						2118-10	Intel	
						MK4516-10	Mostek	
						MCM4517-10	**Motorola** (3839,3844)	
						NMC5295-10	National	70
						μPD2118-3	NEC-Micro	
	120 nsF	NMOS	TS	16	5	MB8117-12	Fujitsu	
						MB8118-12	Fujitsu	
						HM8416A-4	Hitachi	
						2118-4	Intel	
						M2118-4 †	Intel	
						MK4516-12	Mostek	
						MCM4517-12	**Motorola** (3839,3844)	
						NMC5295-4	National	
					±5,12	MB8216E	Fujitsu	80
						HM4716A-1	**Hitachi** (3789)	
						MM5290-1	**National** (3866)	
						NMC5295-12	National	
						μPD-2118-2	NEC-Micro	
						μPD416-5	NEC-Micro	
	150 nsF	NMOS	TS	16	5	**HM4816A-7**	**Hitachi** (3789)	
						2118-15	Intel	
						M2118-7 †	Intel	
						MK4516-15	Mostek	
						MCM4517-15	**Motorola** (3839,3844)	90
					±5,12	F4116-2	Fairchild	
						MB8116H	Fujitsu	
						HM4716A-2	**Hitachi** (3789)	
						ITT4116-2	ITT	
						M5K4116-2	Mitsubishi	
						MK4116-2	Mostek	
						MKB4116-82 †	Mostek	
						MCM4116B-15	**Motorola** (3839)	
						MM5290-2	**National** (3866)	
						NMC5295-15	National	100
						μPD2118	NEC-Micro	
						μPD416-3	NEC-Micro	
						M4116	SGS	
						HYB4116-P2	Siemens	
						TMS4116-15	TI	
						TMM416-2	Toshiba	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

MEMORY–RAMs (Cont'd)

Dynamic (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	Line
16384x1							(Cont'd)	
	200 nsF	NMOS	TS	16	±5	**MCM4517-20**	**Motorola (3839,3844)**	
					±5,12	9016E	AMD	
						F4116-3	Fairchild	
						MB8116E	Fujitsu	
						HM4716A-3	**Hitachi (3789)**	
						ITT4116-3	ITT	
						M5K4116-3	Mitsubishi	
						MK4116-3	Mostek	
						MKB4116-83 †	Mostek	
						MCM4116B-20	**Motorola (3839)**	10
						MM5290-3	**National (3866)**	
						NMC5295-20	National	
						μPD416-2	NEC-Micro	
						MN4116	Panasonic	
						HYB4116-3	Siemens	
						HYB4116-P3	Siemens	
						TMS4116-20	TI	
						TMM416-3	Toshiba	
				18	±5,12	MCM4117-20	Motorola	
	235 nsF	NMOS	TS	16	5	MKB4516-80 †	Mostek	20
	250 nsF	NMOS	TS	16	±5,12	9016D	AMD	
						F4116-4	Fairchild	
						HM4716A-4	**Hitachi (3789)**	
						ITT4116-4	ITT	
						MK4116-4	Mostek	
						MKB4116-84 †	Mostek	
						MCM4116B-25	**Motorola (3839)**	
						MM5290-4	**National (3866)**	
						μPD416-1	NEC-Micro	
						HYB4116-4	Siemens	30
						TMS4116-25	TI	
						TMM416-4	Toshiba	
				18	±5,12	MCM4117-25	Motorola	
	270 nsF	NMOS	TS	16	5	MKB4516-81 †	Mostek	
	300 nsF	NMOS	TS	16	±5,12	9016C	AMD	
						MCM4116B-30	**Motorola (3839)**	
						μPD416	NEC-Micro	
	320 nsF	NMOS	TS	16	5	MKB4516-82 †	Mostek	
16384x4	100 nsF	NMOS	TS	18	5	**MB81416-10**	**Fujitsu (3672)**	
	120 nsF	NMOS	TS	18	5	**MB81416-12**	**Fujitsu (3672)**	40
	150 nsF	NMOS	TS	18	5	**MB81416-15**	**Fujitsu (3672)**	
						TMS4416-15	**TI (442,3959)**	
	200 nsF	NMOS	TS	18	5	**TMS4416-20**	**TI (442,3959)**	
	250 nsF	NMOS	TS	18	5	**TMS4416-25**	**TI (442,3959)**	
32768x1	120 nsF	NMOS	TS	16	5	**HM4864-1**	**Hitachi (3789)**	
						MCM6632A-12	Motorola	
						NMC4132-1	National	
					−2.5,7	MB8132H	Fujitsu	
	150 nsF	NMOS	—	16	−2.5,7	MB8132E	Fujitsu	
			TS	16	5	MCM4132-15	Motorola	50
							(Continued)	

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	Line
32768x1	150 nsF	NMOS	TS	16	5		(Cont'd)	
						MCM6632-15	Motorola	
						MCM6632A-15	Motorola	
						MCM6633-15	Motorola	
						NMC4132-2	National	
	200 nsF	NMOS	TS	16	5	MCM4132-20	Motorola	
						MCM6632-20	Motorola	
						MCM6632A-20	Motorola	
						MCM6633-20	Motorola	
				18	±5,12	MK4332D-3	Mostek	
						MKM4332-83 †	Mostek	60
	250 nsF	NMOS	TS	16	5	MCM4132-25	Motorola	
						MCM6632-25	Motorola	
						MCM6633-25	Motorola	
				18	±5,12	MKM4332-84 †	Mostek	
	300 nsF	NMOS	TS	16	5	MCM4132-30	Motorola	
65536x1	100 nsF	NMOS	TS	16	5	**F4164**	**Fairchild (3666)**	
						MB8264A-10	**Fujitsu (3673)**	
						MB8265A-10	**Fujitsu (3673)**	
						MB8266A-10	**Fujitsu (3673)**	
						IMS2600	**Inmos (3792)**	70
						MCM6664A-12	**Motorola (3839,3842)**	
						μPD4164-2	NEC-Micro	
	120 nsF	NMOS	TS	16	5	**F4164-12**	**Fairchild (3666)**	
						F64K-12	Fairchild	
						MB8264A-12	**Fujitsu (3673)**	
						MB8265A-12	**Fujitsu (3673)**	
						MB8266A-12	**Fujitsu (3673)**	
						MCM6665A-12	**Motorola (3839,3843)**	
						NMC4164-12	National	
						MSM3764-12	**OKI (3873)**	80
						TMS4164-12	**TI (3958)**	
	150 nsF	NMOS	TS	16	5	**F4164-15**	**Fairchild (3666)**	
						F64K-15	Fairchild	
						MB8264-15	**Fujitsu (3673)**	
						MB8265-15	**Fujitsu (3673)**	
						HM4864-2	**Hitachi (3789)**	
						2164-15	Intel	
						2164A-15	Intel	
						M2164 †	Intel	
						M5K4164-15	Mitsubishi	90
						MK4564-15	Mostek	
						MCM6664-15	**Motorola (3839,3842)**	
						MCM6664A-15	**Motorola (3839,3842)**	
							(Continued)	

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature
OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY-RAMs (Cont'd)

Dynamic

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source		Line
65536x1	150 nsF	NMOS	TS	16	5				
						MCM6665-15	**Motorola**	**(3839,3843)**	
						MCM6665A-15	**Motorola**	**(3839,3843)**	
						NMC4164-15	National		
						μPD4164-3	NEC-Micro		
						MSM3764-15	**OKI**	**(3873)**	
						MSM3764-2	**OKI**	**(3873)**	
						TMS4164-15	**TI**	**(3958)**	
						TMM4164-3	Toshiba		
	200 nsF	NMOS	TS	16	5	**F4164-20**	**Fairchild**	**(3666)**	
						F64K-20	Fairchild		10
						MB8264-20	**Fujitsu**	**(3673)**	
						MB8265-20	**Fujitsu**	**(3673)**	
						HM4864-3	**Hitachi**	**(3789)**	
						2164A-20	Intel		
						M5K4164-20	Mitsubishi		
						MK4564-20	Mostek		
						MCM6664-20	**Motorola**	**(3839,3842)**	
						MCM6664A-20	**Motorola**	**(3839,3842)**	
						MCM6665-20	**Motorola**	**(3839,3843)**	
						MCM6665A-20	**Motorola**	**(3839,3843)**	20
						NMC4164-20	National		
						μPD4164-0	NEC-Micro		
						MSM3764-20	**OKI**	**(3873)**	
						MSM3764-3	**OKI**	**(3873)**	
						TMS4164-20	**TI**	**(3958)**	
						TMM4164-4	Toshiba		
	250 nsF	NMOS	TS	16	5	2164-25	Intel		
						MK4564-25	Mostek		
						MCM6664-25	**Motorola**	**(3839,3842)**	
						μPD4164-1	NEC-Micro		30
						TMS4164-25	**TI**	**(3958)**	
65546x1	150 nsF	NMOS	TS	16	5	MKB4564-82	† Mostek		
	200 nsF	NMOS	TS	16	5	MKB4564-83	† Mostek		
	250 nsF	NMOS	TS	16	5	MKB4564-84	† Mostek		
131072x1									
	150 nsF	NMOS	TS	18	5	MK4528-15	Mostek		
	200 nsF	NMOS	TS	18	5	MK4528-20	Mostek		
						MKM4528D-83	† Mostek		
	250 nsF	NMOS	TS	18	5	MK4528-25	Mostek		
						MKM4528D-84	† Mostek		
262144x1									
	100 nsF	NMOS	TS	16	5	**MCM6256-10**	**Motorola**	**(3841)**	40
	120 nsF	NMOS	TS	16	5	**MCM6256-20**	**Motorola**	**(3841)**	

Static

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source		Line
4x4	1 μsR	CMOS	—	24	4.5-15	MC14580BA	† Motorola		
	1.5 μsR	CMOS	—	24	3-15	MC14580BC	Motorola		
	40 nsR	TTL	OC	16	5	54170	† Fairchild		
						54LS170	† Fairchild		
						74170	Fairchild		
						74LS170	Fairchild		
						ZN54170	† Fairchild		
						ZN74170	Ferranti		
						SN54LS170	† Motorola		50
						SN74LS170	Motorola		
						DM54170	† National		
						DM54LS170	† National		
						DM74170	National		
						DM74LS170	National		
						54LS170	† Signetics		
						74LS170	Signetics		
						SN54170	**† TI**	**(893)**	
						SN54LS170	**† TI**	**(893)**	
						SN74170	**TI**	**(893)**	60
						SN74LS170	**TI**	**(893)**	
			TS	16	5	54LS670	† Fairchild		
						74LS670	Fairchild		
						SN54LS670	† Motorola		
						SN74LS670	Motorola		
						DM54LS670	† National		
						DM74LS670	National		
						54LS670	† Signetics		
						74LS670	Signetics		
						SN54LS670	**† TI**	**(990)**	70
						SN74LS670	**TI**	**(990)**	
4x8	1 μsR	CMOS	—	24	3-15	**CD4039A**	**† RCA**	**(3875)**	
						CM4036A	† Solitron		
						CM4039A	† Solitron		
					5	**CD4036A**	**† RCA**	**(3875)**	
8x2	12 nsF	ECL	OE	18	−5.2	10155	Signetics		
	15 nsF	ECL	—	24	−5.2	**MCM10143**	**Motorola**	**(3839)**	
	50 nsR	TTL	TS	24	5	74S172	Signetics		
						SN74172	**TI**	**(894)**	
16x1	20 nsR	TTL	OC	14	5	**SN7481A**	**TI**	**(860)**	80
				16	5	**SN7484A**	**TI**	**(861)**	
	35 nsR	TTL	OC	14	5	MC4004	Motorola		
						MC4005	Motorola		
						MC4304	† Motorola		
						MC4305	† Motorola		
16x12	40 ns *	TTL	OC	20	5	SN54LS313	† TI		
16x4	5 nsF	ECL	OE	16	−4.5	**F100402**	**Fairchild**	**(658)**	
	7 nsF	ECL	OE	24	−4.5	**F100145**	**Fairchild**	**(658)**	
	9 nsF	ECL	OE	16	−5.2	F10145A	Fairchild		
						F10545A	† Fairchild		90
	10 ns *	ECL	OE	16	−5.2	HD10145	Hitachi		
	15 nsF	ECL	OE	16	−5.2	**MCM10145**	**Motorola**	**(3839)**	
	15 nsR	ECL	OE	16	−5.2	10145	Signetics		
	18 nsF	ECL	OE	16	−5.2	MCM10545	† Motorola		
	20 nsF	TTL	TS	18	5	9410C	Fairchild		
	25 nsF	TTL	OC	16	5	AM27S02AC	AMD		
						AM27S06AC	AMD		
						AM27S06C	AMD		
						AM29700C	AMD		
						AM29702C	AMD		100
			TS	16	5	AM27S03AC	AMD		
						AM27S07AC	AMD		
						AM27S07C	AMD		
						AM29701C	AMD		
						AM29703C	AMD		
	30 nsF	TTL	OC	16	5	AM27S02AM	† AMD		

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

MEMORY-RAMs (Cont'd)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	Line
16x4	30 nsF	TTL	OC	16	5		(Cont'd)	
						AM27S06AM	† AMD	
						AM27S06M	† AMD	
						AM29700M	† AMD	
						AM29702M	† AMD	
			TS	16	5	AM27S03AM	† AMD	
						AM27S07AM	† AMD	
						AM27S07M	† AMD	
						AM29701M	† AMD	
						AM29703M	† AMD	
	35 nsF	TTL	OC	16	5	AM27S02C	AMD	10
						AM3101-1C	AMD	
						AM3101AC	AMD	
						AM7489-1	AMD	
						AM74S289	AMD	
						SN74S289	AMD	
						74S289	Fairchild	
						HD74S289	Hitachi	
						DM74S289	National	
						μPB2289	NEC-Micro	
						N3101A	Signetics	20
						SN74S289A	**TI (924)**	
			TS	16	5	AM27S03C	AMD	
						AM74S189	AMD	
						SN74S189	AMD	
						74S189	Fairchild	
						HD74S189	Hitachi	
						DM74S189	National	
						SN74S189A	**TI (900)**	
	40 nsF	TTL	TS	18	5	DM85S68	National	
	45 ns *	TTL	OC	16	5	74LS289	Fairchild	30
						SN74LS289	Motorola	
						SN74LS89	Motorola	
			TS	16	5	74LS189	Fairchild	
						SN74LS189	Motorola	
	45 nsF	TTL	OC	16	5	AM27S02M	† AMD	
			TS	16	5	AM27S03M	† AMD	
	50 nsF	TTL	OC	16	5	AM3101-1M	† AMD	
						AM3101AM	† AMD	
						AM5489-1	† AMD	
						AM54S289	† AMD	40
						AM7489	AMD	
						SN54S289	† AMD	
						54S289	† Fairchild	
						DM54S289	† National	
						N82S25	Signetics	
						S3101A	† Signetics	
						SN54S289A	**† TI (924)**	
				28	5	IDM29705C	National	
			TS	16	5	AM54S189	AMD	
						SN54S189	† AMD	50
						54S189	† Fairchild	
						DM54S189	† National	
						DM8599	National	
						54S189	† Signetics	
						SN54S189A	**† TI (900)**	
				28	5	IDM2970C	National	
	53 nsF	TTL	TS	28	5	**AM29705C**	**AMD (1225)**	
						F29705C	Fairchild	
						F29705M	† National	
						IDM29705	† National	60
	55 ns *	TTL	OC	16	5	54LS289	† Fairchild	
						54LS89	† Fairchild	
						SN54LS289	† Motorola	
						SN54LS89	† Motorola	

(Continued)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	Line
16x4	55 ns *	TTL					(Cont'd)	
			TS	16	5	54LS189	† Fairchild	
						SN54LS189	† Motorola	
	55 nsF	TTL	OC	16	5	AM27LS02AC	AMD	
						AM27LS06C	AMD	
				28	5	IDM29704M	† National	
			TS	16	5	AM27LS03AC	AMD	70
						AM27LS07C	AMD	
	58 nsF	TTL	TS	28	5	**AM29705M**	**† AMD (1225)**	
	60 nsF	TTL	OC	16	5	AM27LS06M	† AMD	
						AM3101	AMD	
						AM5489	† AMD	
						DM8589	National	
						μPB2089	NEC-Electron	
						S82S25	† Signetics	
						SN54LS289A	**† TI (440,924)**	
						SN54LS319A	**† TI (440,929)**	80
						SN74LS289A	**TI (924)**	
						SN74LS319A	**TI (929)**	
				18	5	AM29704C	AMD	
				28	5	F29704C	Fairchild	
						F29704M	† Fairchild	
			TS	16	5	AM27LS07M	† AMD	
						SN54LS189A	**† TI (440,900)**	
						SN54LS219A	**† TI (440,906)**	
						SN74LS189A	**TI (900)**	
						SN74LS219A	**TI (906)**	90
	60 nsR	TTL	OC	16	5	HD7489	Hitachi	
						MC4064	Motorola	
						SN7489	**TI (440,863)**	
	68 nsF	TTL	OC	28	5	AM29704M	† AMD	
	70 nsF	TTL	OC	16	5	AM27LS02C	AMD	
			TS	16	5	AM27LS03C	AMD	
						DM7599	† National	
	75 nsF	TTL	OC	16	5	31013	† AMD	
	80 nsF	TTL	OC	16	5	DM7589	† National	
	85 nsF	TTL	OC	16	5	AM27LS02M	† AMD	100
			TS	16	5	AM27LS03M	† AMD	
	110 nsR	TTL	OC	16	5	31L01C	AMD	
						31L01M	† AMD	
	120 nsR	CMOS	TS	18	4.5-12.5	F4710BC	Fairchild	
						F4710BM	† Fairchild	
	500 nsR	CMOS	TS	18	3-5.5	MM54C989	† National	
						MM74C989	National	
	650 nsR	CMOS	TS	16	5	MM54C89	† National	
						MM74C89	National	
						CD40114B	**† RCA (3874)**	110
						CD4011BE	**RCA (748)**	
16x9	40 ns *	TTL	OC	20	5	SN54LS311	† TI	
						SN54LS312	† TI	
						SN74LS311	TI	
						SN74LS312	TI	
			TS	20	5	SN54LS211	† TI	
						SN54LS212	† TI	
						SN74LS211	TI	
						SN74LS212	TI	
16x12	40 ns *	TTL	TS	20	5	SN54LS213	† TI	120
						SN74LS213	TI	
32x2	50 nsF	TTL	OC	16	5	N82S21	Signetics	
32x8	40 ns *	TTL	OC	20	5	SN54LS318	† TI	
						SN74LS318	TI	
			TS	20	5	SN54LS218	† TI	
						SN74LS218	TI	
	300 ns *	CMOS	TS	18	10	HCMP1824	Hughes	

(Continued)

† Military Temperature Range (−55° to 125°C) · ns*—Nanoseconds Typical · nsF—Nanoseconds over Full Temperature Range · nsR—Nanoseconds at Room Temperature
OC—Open Collector · TS—Three-State · OE—Open Emitter

MEMORY–RAMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	Line
Static							**(Cont'd)**	
32x8	300 ns *	CMOS	TS	18	10		(Cont'd)	
						HMMP1824	† Hughes	
						CDP1824	**† RCA (3874)**	
	600 ns *	CMOS	TS	18	10	HCMP1824C	Hughes	
						HMMP1824C	† Hughes	
						CDP1824C	**† RCA (3874)**	
64x1	1.05 µsR	CMOS	TS	24	5-15	MCM14552A	† Motorola	
	2.1 µsR	CMOS	TS	24	5-15	MCM14552C	Motorola	
	10 nsR	ECL	OE	16	−5.2	SN10142	TI	
	12 nsF	ECL	OE	16	−5.2	µPB10142	NEC-Electron	
	15 nsF	ECL	OE	16	−5.2	**MCM10148**	**Motorola (3839)**	10
						µPB10148	NEC-Electron	
	15 nsR	ECL	OE	16	−5.2	SN10140	TI	
						SN10148	TI	
	270 nsR	CMOS	—	14	3-18	MCM14505A	† Motorola	
	350 nsR	CMOS	—	14	4.5-16	MCM14505C	Motorola	
	500 nsF	CMOS	TS	18	5	MM54C910	† National	
						MM74C910	National	
64x4	6 ns *	ECL	OE	24	−5.2	GXB100473	Siemens	
	40 ns *	TTL	OC	16	5	SN54LS316	† TI	
						SN54LS317	† TI	20
						SN74LS316	TI	
						SN74LS317	TI	
			TS	16	5	SN54LS216	† TI	
						SN54LS217	† TI	
						SN74LS216	TI	
						SN74LS217	TI	
	2000 ns *							
		CMOS	TS	16	5	MN1203	Panasonic	
64x8	1 µsF	CMOS	TS	22	5	CDP1826C	RCA	
64x9	35 nsF	TTL	OC	16	5	N82S09A	Signetics	
				28	5	**93419A**	**Fairchild (3615,3631)**	30
						N82S19	Signetics	
	45 nsF	TTL	OC	28	5	**93419C**	**Fairchild (3615,3631)**	
						MBM93419	Fujitsu	
	60 nsF	TTL	OC	16	5	S82S19	† Signetics	
				28	5	**93419M**	**† Fairchild (3615,3631)**	
	80 nsF	TTL	OC	28	5	S82S09	† Signetics	
64x12	150 nsF	CMOS	TS	18	3-11	IM6512AI	Intersil	
						IM6512AM	† Intersil	
	400 nsF	CMOS	TS	18	3-7	HM6512C-9	Harris	
					5	HM6512-2	† Harris	40
						HM6512-9	Harris	
	460 nsF	CMOS	TS	18	3-7	IM6512I	Intersil	
						IM6512M	† Intersil	
	600 nsF	CMOS	TS	18	3-7	IM6512C	Intersil	
128x1	12 nsR	ECL	OE	16	−5.2	**MCM10147**	**Motorola (3839)**	
						GXB10147A	Siemens	
	15 nsR	ECL	OE	16	−5.2	SN10147	TI	
128x8	—	CMOS	—	8	5	PCD8571	Signetics	
	250 ns *	NMOS	TS	24	5	S68B10	AMI	
						F68B10	Fairchild	50
						MCM68B10	**Motorola (3839)**	
	250 nsF	CMOS	TS	24	10	**CDP1823**	**RCA (3874)**	
	350 nsF	NMOS	TS	24	5	S6810-1	AMI	
	360 nsF	NMOS	TS	24	5	S68A10	AMI	
						F68A10	Fairchild	
						HM468A10	Hitachi	
						MCM68A10	**Motorola (3839)**	

(Continued)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	Line
128x8							(Cont'd)	
	450 nsF	CMOS	TS	24	5	**CDP1823C**	**RCA (3874)**	
		NMOS	TS	24	5	S6810	AMI	
						F6810	**Fairchild (1278)**	60
						HM46810	Hitachi	
						MCM6810	**Motorola (1351,3839)**	
256x1	1 µsR	PMOS	TS	16	−9,5	1101A1	AMD	
	1.4 µsR	CMOS	—	16	3-15	MCM14537A	† Motorola	
	1.5 µsF	PMOS	TS	16	−9,5	1101A	AMD	
						1101AM	† AMD	
	2 µsR	CMOS	—	16	3-15	MCM14537C	† Motorola	
	8 nsF	ECL	OE	16	−5.2	10414-1	Hitachi	
	10 nsF	ECL	OE	16	−5.2	**F100414C**	**Fairchild (3615,3624)**	
						F10414C	**Fairchild (3615)**	70
						10414	Hitachi	
	15 nsF	ECL	OE	16	−5.2	**F10414M**	**† Fairchild (3615)**	
						MCM10152	**Motorola (3839)**	
	25 nsF	ECL	OE	16	−5.2	µPB10144	NEC-Electron	
	26 nsF	ECL	OE	16	−5.2	**MCM10144**	**Motorola (3839)**	
						MCM10544	† Motorola	
						DM10414	National	
	30 nsF	ECL	OE	16	−5.2	**F10410C**	**Fairchild (3615)**	
	35 nsF	TTL	OC	16	5	AM27LS01-1AC	AMD	
						AM27LS01-1AM	† AMD	80
			TS	16	5	AM27LS00-1AC	AMD	
						AM27LS00AC	AMD	
	35 nsR	ECL	OE	16	−5.2	SN10144	TI	
	40 nsF	TTL	OC	16	5	N74LS301	Signetics	
						N82LS17	Signetics	
			TS	16	5	93421AC	Fairchild	
						N82LS16	Signetics	
	45 nsF	TTL	OC	16	5	AM27LS01-1C	AMD	
						AM27LS01AC	AMD	
						AM27LS01AM	† AMD	90
						AM29720C	AMD	
						AM93411AC	AMD	
						93410AC	Fairchild	
						93411AC	Fairchild	
			TS	16	5	AM27LS00-1AM	† AMD	
						AM27LS00-1C	AMD	
						AM27LS00AM	† AMD	
						AM27LS00C	AMD	
						AM29721C	AMD	
						AM93421AC	AMD	100
						93L420C	Fairchild	
	50 nsF	TTL	OC	16	5	µPB2206	NEC-Electron	
						N82S17	Signetics	
			TS	16	5	93421C	Fairchild	
						DM74S200	National	
						µPB2200	NEC-Electron	
						N82S16	Signetics	
	55 nsF	TTL	OC	16	5	AM27LS01-1M	† AMD	
						AM27LS01M	† AMD	
						AM29720M	† AMD	110
						AM93411C	AMD	
						93411C	Fairchild	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

MEMORY-RAMs (Cont'd)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	Line
							(Cont'd)	
256x1	55 nsF	TTL						
			TS	16	5	AM27LS00-1M	† AMD	
						AM27LS00M	† AMD	
						AM29721M	† AMD	
						AM93421C	AMD	
						93L420M	† Fairchild	
	60 nsF	TTL	OC	16	5	93410C	Fairchild	
						DM74S206	National	
						S82LS17	† Signetics	
			TS	16	5	93421M	† Fairchild	
						S82LS16	† Signetics	10
	65 nsF	TTL	OC	16	5	93411M	† Fairchild	
						SN74S301	**† TI (927)**	
			TS	16	5	μPB2202	NEC-Electron	
						SN74S201	**TI (440,905)**	
	70 nsF	TTL	OC	16	5	93410M	† Fairchild	
						54S301	† Signetics	
						S54LS301	† Signetics	
						S82S17	† Signetics	
			TS	16	5	S82S16	† Signetics	
	80 nsF	TTL	OC	16	5	AM27LS01LC	AMD	20
			TS	16	5	AM27LS00LC	AMD	
	90 nsF	TTL	TS	16	5	93L421C	Fairchild	
	95 nsF	TTL	OC	16	5	AM27LS01LM	† AMD	
			TS	16	5	AM27LS00LM	† AMD	
	100 nsF	TTL	TS	16	5	93L421M	† Fairchild	
	150 ns *	CMOS	TS	16	10	**MCM10422**	**Motorola (3839)**	
	200 ns *	CMOS	TS	16	3-15	F4720AC	Fairchild	
					4.5-12.5	F4720C	Fairchild	
						F4720M	† Fairchild	
	345 nsF	CMOS	TS	16	10	**CD40061A**	**† RCA (3874)**	30
	400 nsR	CMOS	TS	16	3-15	MM54C200	† National	
						MM74C200	National	
	850 nsF	CMOS	TS	16	5	CO40061	RCA	
	900 nsF	PMOS	—	16	−12,5	MK4007	Mostek	
						MK4007-4	Mostek	
256x4	1 μsF	NMOS	TS	16	5	AM2101	AMD	
						AM2111	AMD	
						AM2112	AMD	
	3 μsF	CMOS	TS	22	3	ITT5101S	ITT	
	10 nsF	ECL	OE	24	−4.5	**F100422C**	**Fairchild (3615)**	40
						F10422C	**Fairchild (3615,3620)**	
					−5.2	E100422	Fairchild	
						F10422	**Fairchild (3615,3620)**	
						MBM100422	Fujitsu	
						MBM10422H	**Fujitsu (3681)**	
					−7	100422B	Signetics	
						10422B	Signetics	
	12 nsF	ECL	OE	22	−5.2	**MB7072E**	**Fujitsu (3681)**	
						HM100422	**Hitachi (3789)**	
						HM10422	**Hitachi (3789)**	50
				24	−5.2	**MBM10422E**	**Fujitsu (3681)**	
	15 nsF	ECL	OE	22	−5.2	**MB7072N**	**Fujitsu (3681)**	
				24	−5.2	**MBM10422N**	**Fujitsu (3681)**	
						DM100422	National	
						DM10422	**National (3854)**	
					−7	100422A	Signetics	
						10422A	Signetics	
							(Continued)	

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	Line
							(Cont'd)	
256x4	15 nsF	ECL	OE	24	−8	100422	Signetics	
	20 nsF	ECL	OE	24	−7	10422	Signetics	
	25 nsF	NMOS	TS	24	5	AM9122-25	AMD	60
	30 nsF	ECL	OE	24	−7	**93422AM**	**† Fairchild (3615,3634)**	
						93L422AC	**Fairchild (3615,3637)**	
	35 nsF	NMOS	TS	24	5	AM9122-35	AMD	
						AM91L22-35	AMD	
		TTL	OC	22	5	AM93412AC	AMD	
			TS	22	5	AM93422AC	AMD	
	40 nsF	TTL	OC	22	5	AM93412	AMD	
						MCM93412C	Motorola	
			TS	16	5	SN74S207	TI	
				20	5	SN74S208	TI	70
				22	5	AM93422	AMD	
						93422C	**Fairchild (3615,3634)**	
						MCM93422C	**Motorola (3839)**	
	45 nsF	NMOS	TS	24	5	AM91L22-45	AMD	
		TTL	OC	22	5	AM93412AM	† AMD	
						AM93L412AC	AMD	
			TS	22	5	AM93422AM	† AMD	
						AM93L422AC	AMD	
	55 nsF	TTL	OC	22	5	AM93L412AM	† AMD	
			TS	22	5	AM93L422AM	† AMD	80
	60 nsF	NMOS	TS	24	5	AM91L22-60	AMD	
		TTL	OC	22	5	AM93412M	† AMD	
						AM93L412	AMD	
						MCM93412M	† Motorola	
			TS	22	5	AM93422M	† AMD	
						AM93L422	AMD	
						93422M	**† Fairchild (3615,3634)**	
						93L422C	**Fairchild (3615,3637)**	
						MBM100422	**Fujitsu (3681)**	
						MCM93422M	**† Motorola (3839)**	90
	75 nsF	TTL	OC	22	5	AM93L412M	† AMD	
			TS	22	5	AM93L422M	† AMD	
						93L422AM	**Fairchild (3615,3637)**	
						93L422M	**† Fairchild (3615,3637)**	
	150 nsF	CMOS	TS	18	5	NMC6552B-9	National	
				22	5	NMC6551B-9	National	
	175 nsF	NMOS	TS	16	5	SY21H12	Synertek	
				18	5	SY21H11	Synertek	
				22	5	SY21H01	Synertek	
	180 nsF	CMOS	TS	18	5	NMC6552B-2	† National	100
				22	5	NMC6551B-2	† National	
	200 nsF	CMOS	TS	18	5	NMC6552-9	National	
				22	5	NMC6551-9	National	
		NMOS	TS	16	5	SY21H12-2	Synertek	
				18	5	SY21H11-2	Synertek	
				22	5	SY21H01-2	Synertek	
	220 nsF	CMOS	TS	16	5	HM6562B-2	† Harris	
						HM6562B-9	Harris	
				18	5	**HM6561B-2**	**† Harris (669,1333,3760)**	
						HM6561B-9	**Harris (669,1333,3760)**	110
						IM65X61-1	Intel	
						IM65X61-1	Intersil	
						IM65X61-1M	† Intersil	
							(Continued)	

† Military Temperature Range (−55° to 125°C)
OC—Open Collector
ns*—Nanoseconds Typical
nsF—Nanoseconds over Full Temperature Range
TS—Three-State
nsR—Nanoseconds at Room Temperature
OE—Open Emitter

MEMORY–RAMs (Cont'd)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	Line
256x4	220 nsF	CMOS	TS				(Cont'd)	
				22	5	**HM6551B-2**	**† Harris (669,1333,3758)**	
						HM6551B-9	**Harris (669,1333,3758)**	
						IM65X51-1	Intersil	
						IM65X51-1M	† Intersil	
	235 nsF	CMOS	TS	18	10	IM65X61A	Intersil	
						IM65X61AM	† Intersil	
				22	10	IM65X51A	Intersil	
						IM65X51AM	† Intersil	
	240 nsF	CMOS	TS	22	5	HS6551RH	† Harris	
	250 nsF	CMOS	TS	18	5	MM74C921	National	10
						NMC6552-2	† National	
				22	5	MM74C920	National	
						NMC6551-2	† National	
						MWS5101EL2	RCA	
					10	**CDP1822**	**RCA (3874)**	
						TCC-244	RCA	
		NMOS	TS	16	5	AM9101D	AMD	
						AM9111D	AMD	
						AM9112D	AMD	
						SY2112A-2	Synertek	20
				18	5	μPD2111AL-AL-2	NEC-Micro	
						SY2111A-2	Synertek	
				22	5	SY2101A-2	Synertek	
	275 nsF	CMOS	TS	18	5	MM54C921	† National	
				22	5	MM54C920	† National	
	300 nsF	CMOS	TS	16	5	HM6562-2	† Harris	
						HM6562-9	Harris	
				18	5	**HM6561-2**	**† Harris (669,1333,3760)**	
						HM6561-9	**Harris (669,1333,3760)**	
						IM65X61	Intersil	30
						IM65X61M	† Intersil	
						NMC6552-5	National	
				22	5	**HM6551-2**	**† Harris (669,1333,3758)**	
						HM6551-9	**Harris (669,1333,3758)**	
						IM65X51	Intersil	
						IM65X51M	† Intersil	
						NMC6551-5	National	
						LH-5101S	Sharp	
		NMOS	TS	16	5	AM9101C	AMD	
						AM9101CM	† AMD	40
						AM9111C	AMD	
						AM9111CM	† AMD	
						AM9112C	AMD	
						AM9112CM	† AMD	
						AM91L01C	AMD	
						AM91L01CM	† AMD	
						AM91L111C	AMD	
						AM91L11CM	† AMD	
						AM91L12C	AMD	
						AM91L12CM	† AMD	50
	325 nsF	CMOS	TS	18	5	MM74921-3	National	
				22	5	MM74920-3	National	
						MM74C920-3	National	
						MM74C921-3	National	
	350 nsF	CMOS	TS	16	5	HM6562-5	Harris	
				18	5	**HM6561-5**	**Harris (669,1333,3760)**	
						IM65X61C	Intersil	

(Continued)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	Line
256x4	350 nsF	CMOS	TS				(Cont'd)	
				22	5	**HM6551-5**	**Harris (669,1333,3758)**	
						IM65X51C	Intersil	
						MWS5101DL3	† RCA	60
						MWS5101EL3	RCA	
						SCM5101-1A	SSS	
		NMOS	TS	16	5	SY2112A	Synertek	
				18	5	SY2111A	Synertek	
				22	5	SY2101A	Synertek	
	400 nsF	CMOS	TS	22	5	HMMP1822C	† Hughes	
						CDP1822C	**† RCA (3874)**	
		NMOS	TS	16	5	AM9101B	AMD	
						AM9101BM	† AMD	
						AM9111B	AMD	70
						AM9111BM	† AMD	
						AM9112B	AMD	
						AM9112BM	† AMD	
						AM91L01B	AMD	
						AM91L01BM	† AMD	
						AM91L11B	AMD	
						AM91L11BM	† AMD	
						AM91L12B	AMD	
						AM91L12BM	† AMD	
	450 nsF	CMOS	TS	22	5	**S5101L-1**	**AMI (3614)**	80
						S6501L1	AMI	
						HM435101-1	Hitachi	
						M5L5101L-1	Mitsubishi	
						MCM51L01-45	Motorola	
						μPD5101L-1	NEC-Micro	
						SCM5101-1	SSS	
						TC5501	Toshiba	
		NMOS	TS	16	5	SY2112A-4	Synertek	
				18	5	SY2111A-4	Synertek	
				22	5	SY2101A-4	Synertek	90
	500 nsF	NMOS	TS	16	5	AM2112-1	AMD	
						AM9112A	AMD	
						AM9112AM	† AMD	
						AM91L12A	AMD	
						AM91L12AM	† AMD	
						SY2112-1	Synertek	
				18	5	AM2101-1	AMD	
						AM2111-1	AMD	
						AM9101A	AMD	
						AM9101AM	AMD	100
						AM9111A	AMD	
						AM9111AM	AMD	
						AM91L01A	AMD	
						AM91L01AM	AMD	
						AM91L111AM	AMD	
						AM91L11A	AMD	
						SY2111-1	Synertek	
				22	5	SY2101-1	Synertek	
	650 nsF	CMOS	TS	22	5	**S5101L**	**AMI (3614)**	
						S5101L-3	**AMI (3614)**	110
						S6501L	AMI	
						S6501L-3	AMI	
						MCM5101-65	Motorola	
						MCM51L01-65	Motorola	
						μPD5101L	NEC-Micro	
						MSM573A	OKI	
						SCM5101-3	SSS	
						TC5501-1	Toshiba	
		NMOS	TS	16	5	AM2101-2	AMD	
						AM2111-2	AMD	120
						AM2112-2	AMD	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

MEMORY-RAMs (Cont'd)

Static

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	Line
256x4								
	800 nsF	CMOS	TS	22	5	**S5101-8**	**AMI (3614)**	
						S6501-8	AMI	
						S6501L-8	AMI	
						MCM5101-80	Motorola	
						MN5101	Panasonic	
						LH-5101W	Sharp	
						883/5101-4	† SSS	
						SCM5101-8	SSS	
						SCM883/5101-4	† SSS	
	950 nsF	NMOS	TS	18	5	M120	SGS	10
256x8	40 nsF	TTL	TS	22	5	**N8X350**	**Signetics (1501,1509)**	
						S8X350	† Signetics	
256x9	35 nsF	TTL	TS	22	5	N82S212A	Signetics	
	45 nsF	TTL	TS	22	5	**93479DC**	**Fairchild (3615,3649)**	
	60 nsF	TTL	TS	24	5	N82S210	Signetics	
	70 nsF	TTL	TS	22	5	S82S212	† Signetics	
	90 nsF	TTL	TS	24	5	S82S210	† Signetics	
512x4	1.2 µsF	CMOS	TS	24	5	LH-5102	Sharp	
	300 nsF	CMOS	TS	18	5	HM6513-9	Harris	
						NMC6513-9	† National	20
	350 nsF	CMOS	TS	18	5	HM6513-5	Harris	
						NMC6513-5	National	
512x8	300 nsF	NMOS	TS	24	5	ER5304	GI	
1024x1	1 µsF	NMOS	TS	16	5	AM2102	AMD	
	7 nsF	ECL	OE	16	−5.2	**HM2112-1**	**Hitachi (3789)**	
	10 ns*	ECL	OE	16	−5.2	AM100415	AMD	
						AM10415	AMD	
	10 nsF	ECL	OE	16	−5.2	**F10415C**	**Fairchild (3615,3618)**	
						HM2112	**Hitachi (3789)**	
					−7	10041BB	Signetics	30
						10415B	Signetics	
				24	−4.5	**F100415C**	**Fairchild (3615,3625)**	
						MCM10146A	**Motorola (3839)**	
	15 nsF	ECL	OE	16	−5.2	AM100415A	AMD	
						AM10415SA	† AMD	
					−7	100415A	Signetics	
	20 nsF	ECL	OE	16	−5.2	AM100415	AMD	
						AM10415A	† AMD	
						AM10415SA	† AMD	
						F10415AC	**Fairchild (3615,3618)**	40
						MBM10415AH	**Fujitsu (3681)**	
						HM2110-2	**Hitachi (3789)**	
					−7	100415	Signetics	
						10415A	Signetics	
				24	−5.2	DM10415	National	
		NMOS	TS	16	5	2125H-1	Intel	
		TTL	TS	16	5	93F425	Fairchild	
	25 nsF	ECL	OE	16	−5.2	AM10415A	† AMD	
						HM2110-1	**Hitachi (3789)**	
						GXB10415	Siemens	50
		NMOS	OC	16	5	2115H-2	Intel	
			TS	16	5	2125H-2	Intel	
	29 nsF	ECL	OE	16	−5.2	**MCM10146**	**Motorola (3839)**	
	30 nsF	NMOS	OC	16	5	2115H-3	Intel	
			TS	16	5	2125H-3	Intel	
		TTL	OC	16	5	AM93415AC	AMD	

(Continued)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	Line
								(Cont'd)
1024x1	30 nsF	TTL	OC	16	5	AM93425AC	AMD	
						93415AC	**Fairchild (3615)**	
			TS	16	5	**93425AC**	**Fairchild (3615,3640)**	
	35 nsF	ECL	OE	16	−5.2	AM10415	AMD	60
						MBM10415A	**Fujitsu (3681)**	
						HM2110	**Hitachi (3789)**	
						DM10415A	National	
		NMOS	OC	16	5	2115H-4	Intel	
			TS	16	5	2125H-4	Intel	
		TTL	OC	16	5	**HM2510-2**	**Hitachi (3789)**	
	40 nsF	ECL	OE	16	−5.2	AM10415M	† AMD	
						MCM10546	† Motorola	
		TTL	OC	16	5	AM93415AM	† AMD	
			TS	16	5	AM93425AM	† AMD	70
	45 nsF	NMOS	OC	16	5	2115A	Intel	
						2115AL	Intel	
						MCM2115A-45	Motorola	
						MCM21L15A-45	Motorola	
			TS	16	5	2125A	Intel	
						2125AL	Intel	
						MCM2125A-45	Motorola	
						MCM21L25A-45	Motorola	
		TTL	OC	16	5	AM93415C	AMD	
						93415C	**Fairchild (3615)**	80
						HM2510-1	**Hitachi (3789)**	
						MCM93415C	**Motorola (3839)**	
			TS	16	5	AM93425C	AMD	
						93425C	**Fairchild (3615,3640)**	
						HM2511-1	**Hitachi (3789)**	
						MCM93425C	**Motorola (3839)**	
	50 nsF	TTL	OC	16	5	µPB2205	NEC-Electron	
						SN74S314A	TI	
			TS	16	5	SN74S214A	TI	
	55 nsF	NMOS	OC	16	5	MCM2115A-55	Motorola	90
			TS	16	5	MCM2125A-55	Motorola	
	60 nsF	TTL	OC	16	5	AM93L415C	AMD	
						93415M	**† Fairchild (3615)**	
						93L415	Fairchild	
						MCM93415M	**† Motorola (3839)**	
			TS	16	5	**93425M**	**† Fairchild (3615,3640)**	
						93L425C	**Fairchild (3615)**	
						MCM93425M	**† Motorola (3839)**	
	65 nsF	TTL	OC	16	5	AM93415M	† AMD	
			TS	16	5	AM93425M	† AMD	100
	70 ns *	TTL	OC	16	5	SN74LS315	TI	
			TS	16	5	SN74LS215	TI	
	70 nsF	NMOS	OC	16	5	2115A-2	Intel	
						2115AL-2	Intel	
						MCM2115A-70	Motorola	
						MCM21L15A-70	Motorola	
			TS	16	5	2125A-2	Intel	

(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature
OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY-RAMs (Cont'd)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	Line
1024x1	70 nsF	NMOS	TS	16	5			(Cont'd)
						2125AL-2	Intel	
						MCM2125A-70	Motorola	
						MCM21L25A-70	Motorola	
				18	5	HM2148	Hitachi	
		TTL	OC	16	5	AM93L415M	† AMD	
						HM2510	**Hitachi (3789)**	
						SN74S314	TI	
			TS	16	5	AM93L425M	† AMD	
						93L425M	**† Fairchild (3615)**	
						HM2511	**Hitachi (3789)**	10
						SN74S214	TI	
	95 nsF	TTL	OC	16	5	SN74LS314	TI	
			TS	16	5	SN74LS214	TI	
	125 nsF	CMOS	TS	16	4.5-10.5	IM65X08A-1	† Intersil	
						IM65X08A-1I	Intersil	
					5	**CDP1821**	**† RCA (3874)**	
				18	4.5-10.5	IM65X18A-1	Intersil	
						IM65X18A-1M	† Intersil	
	130 nsF	CMOS	TS	16	5	NMC85008B-9	National	
				18	5	NMC6518B-9	National	20
	150 nsF	CMOS	TS	16	5	NMC6508B-2	† National	
				18	5	NMC6518B-2	† National	
	180 nsF	CMOS	TS	16	5	**HM6508B-2**	**† Harris (669,1333,3754)**	
						HM6508B-9	**Harris (669,1333,3754)**	
						IM5X08-1	Intersil	
						IM65X08-1M	† Intersil	
						NMC6508-9	National	
				18	5	**HM6518B-2**	**† Harris (669,1333,3756)**	
						HM6518B-9	**Harris (669,1333,3756)**	
						IM65X18-1	Intersil	30
						IM65X18-1M	† Intersil	
						NMC6518-9	National	
	200 nsF	CMOS	TS	16	4.5-10.5	IM65X08A	Intersil	
						IM65X08AM	† Intersil	
				18	4.5-10.5	IM65X18A	Intersil	
						IM65X18AM	† Intersil	
	220 nsF	CMOS	TS	16	5	NMC6508-2	† National	
				18	5	NMC6518-2	† National	
	240 nsF	CMOS	TS	16	5	MM74C929	National	
				18	5	MM74C930	National	40
	250 nsF	CMOS	TS	16	5	**HM6508-2**	**† Harris (669,1333,3754)**	
						HM6508-9	**Harris (669,1333,3754)**	
						IM65X08	Intersil	
						IM65X08M	† Intersil	
						MCM6508-25	Motorola	
						NMC6508-5	National	
						CDP1821C	**RCA (3874)**	
				18	5	**HM6518-2**	**† Harris (669,1333,3756)**	
								(Continued)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	Line
1024x1	250 nsF	CMOS	TS	18	5			(Cont'd)
						HM6518-9	**Harris (669,1333,3756)**	
						IM65X18C	Intersil	50
						IM65X18M	† Intersil	
						MCM6518-25	Motorola	
						NMC6518-5	National	
		NMOS	TS	16	5	AM9102D	AMD	
						2102H	Fairchild	
						2102HM	† Fairchild	
						2102LH	Fairchild	
						2102LHM	† Fairchild	
						21L02H	Fairchild	
						MM2102A-2	National	60
						MM2102A-2L	National	
						μPD2102AL-AL-2	NEC-Micro	
						M2102A-2	SGS	
						M2102AL-2	SGS	
	260 nsF	CMOS	TS	16	5	HS6508RH	† Harris	
	265 nsF	CMOS	TS	16	5	MM54C929	† National	
				18	5	MM54C930	† National	
	300 nsF	CMOS	TS	16	5	S6508-1	AMI	
						HM6508-5	**Harris (669,1333,3754)**	
						IM65X08C	Intersil	70
						MCM6508-30	Motorola	
				18	5	**HM6518-5**	**Harris (669,1333,3756)**	
						MCM6518-30	Motorola	
		NMOS	TS	16	5	AM9102C	AMD	
						AM9102CM	† AMD	
						AM91L02C	AMD	
						AM91L02CM	† AMD	
	315 nsF	CMOS	TS	16	5	MM74C929-3	National	
				18	5	MM74C930-3	National	
	350 nsF	CMOS	TS	16	4-11	S6508A	AMI	80
					5	SCM21C02-1A	SSS	
		NMOS	TS	16	5	2102F	Fairchild	
						2102FM	† Fairchild	
						2102LF	Fairchild	
						2102LFM	† Fairchild	
						21L02F	Fairchild	
						MM2102A	National	
						MM2102A-L	National	
						M2102A	SGS	
						M2102AL	SGS	90
	370 nsF	CMOS	TS	16	5	TC5508	Toshiba	
	400 nsF	NMOS	TS	16	5	AM9102B	AMD	
						AM9102BM	† AMD	
						AM91L02B	AMD	
						AM91L02BM	† AMD	
						MCM6508-40	Motorola	
	450 nsF	CMOS	TS	16	5	SCM21C02-1	SSS	
						TC5508-4	Toshiba	
		NMOS	TS	16	5	21021	Fairchild	
						21021M	† Fairchild	100
						2102L1	Fairchild	
						2102L1M	† Fairchild	
						21L021	Fairchild	
						MM2102A-4	National	
						MM2102A-4L	National	
						μPD2102AL-AL-4	NEC-Micro	
								(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

MEMORY–RAMs (Cont'd)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	Line
1024x1	450 nsF	NMOS	TS	16	5		(Cont'd)	
						M2102A-4	SGS	
						M2102AL-4	SGS	
	460 nsF	CMOS	TS	16	5	S6508	AMI	
				18	5	MCM6518-46	Motorola	
	500 nsF	NMOS	TS	16	5	AM2102-1	AMD	
						AM9102A	AMD	
						AM9102AM	† AMD	
						AM91L02A	AMD	
						AM91L02AM	† AMD	
	550 nsF	CMOS	TS	16	5	TC5508-1	Toshiba	10
	650 nsF	CMOS	TS	16	5	SCM21C02-3	SSS	
		NMOS	TS	16	5	AM2102-2	AMD	
						AM9102	AMD	
						AM9102M	† AMD	
						AM91L02	AMD	
						AM91L02M	† AMD	
						21022	Fairchild	
						21022M	† Fairchild	
						2102L2	Fairchild	
						2102L2M	† Fairchild	20
						21L022	Fairchild	
						MM2102A-6	National	
						MM2102A-6L	National	
						M2102A-6	SGS	
	800 nsF	CMOS	TS	16	5	SCM21C02-8	SSS	
				22	5	883/21C02	† SSS	
1024x4	15 nsF	ECL	OE	24	5	AM100474A	AMD	
						AM10474AC	AMD	
		TTL	TS	24	5	**MBM100474-15**	**Fujitsu (3681)**	
	20 nsF	ECL	OE	24	5	AM10474AM	† AMD	30
		TTL	TS	24	5	**MBM100474-20**	**Fujitsu (3681)**	
	25 nsF	ECL	—	24	−5.2	**MBM10474**	**Fujitsu (3681)**	
			OE	24	5	AM100474	AMD	
						AM10474C	AMD	
					−5.2	GXB100474	Siemens	
	30 nsF	ECL	OE	24	5	AM10474M	† AMD	
					−4.5	**F100474**	**Fairchild (3615,3629)**	
					−5.2	**F10474C**	**Fairchild (3615,3622)**	
		NMOS	TS	18	5	CM2114	Supertex	
	45 nsF	NMOS	TS	18	5	MBM2148-45	Fujitsu	40
						MBM2149-45	Fujitsu	
						2148H-2	Intel	
						2149H-2	Intel	
						SY2148H-2	**Synertek (3942)**	
						SY2149H-2	**Synertek (3942)**	
		TTL	TS	18	5	**93475**	**Fairchild (3615,3646)**	
	55 nsF	MNOS	TS	18	5	HM2148-3	Hitachi	
		NMOS	TS	18	5	AM9148-55	AMD	
						AM9149-55	AMD	
						MBM2148-55	Fujitsu	50
						MBM2148-55L	Fujitsu	
						MBM2149-55L	Fujitsu	
						MBM2149L-55	Fujitsu	
						2148H-3	Intel	
						2148HL-3	Intel	
						2149H-3	Intel	
						2149HL-3	Intel	

(Continued)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source	Line
1024x4	55 nsF	NMOS	TS	18	5		(Cont'd)	
						MCM2149-55	Motorola	
						NMC2148-3	National	
						μPD2149	NEC-Micro	60
						SY2148H-3	**Synertek (3942)**	
						SY2148HL-3	**Synertek (3942)**	
						SY2149H-3	**Synertek (3942)**	
						SY2149HL-3	**Synertek (3942)**	
						SYM2148H-3	**† Synertek (426)**	
						SYM2149H-3	**† Synertek (426)**	
	70 nsF	CMOS	TS	18	5	**HM6148**	**Hitachi (3789)**	
						HM6148L	**Hitachi (3789)**	
		NMOS	TS	18	5	AM9148-70	AMD	
						AM9149-70	AMD	70
						MBM2149-70	Fujitsu	
						2148H	Intel	
						2148HL	Intel	
						2149H	Intel	
						2149HL	Intel	
						M2148H	† Intel	
						NMC2148	National	
						NMC2148H	National	
						NMC2148L	National	
						SY2148H	**Synertek (3942)**	80
						SY2148HL	**Synertek (3942)**	
						SY2149H	**Synertek (3942)**	
						SY2149HL	**Synertek (3942)**	
						SYM2148H	**† Synertek (426)**	
						SYM2149H	**† Synertek (426)**	
	85 nsF	CMOS	TS	18	5	**HM6148-6**	**Hitachi (3789)**	
						HM6148L-6	**Hitachi (3789)**	
		NMOS	TS	18	5	MCM2149-85	Motorola	
						SYM2148H-6	**† Synertek (426)**	
						SYM2149H-6	**† Synertek (426)**	90
	100 nsF	NMOS	TS	18	5	2114AL-1	Intel	
						NMC2114A-1L	**National (3858)**	
						SY2114AL-1	**Synertek (3941)**	
	120 nsF	NMOS	TS	18	5	2114AL-2	Intel	
						2114L-2	Intel	
						NMC2114A-2	**National (3858)**	
						NMC2114A-2L	**National (3858)**	
						SY2114AL-2	**Synertek (3941)**	
				20	5	**NMC2114A**	**National (3858)**	
	150 nsF	NMOS	TS	18	5	**HM472114A-1**	**Hitachi (3789)**	100
						2114AL-3	Intel	
						M2114AL-3	† Intel	
						MM2114-15	National	
						NMC2114A-3	**National (3858)**	
						NMC2114A-3L	**National (3858)**	
						SY2114AL-3	**Synertek (3941)**	
						SYM2114A-3	**† Synertek (424)**	
						TMS2114-15	TI	
						TMS2114L-15	TI	
	170 nsF	CMOS	TS	18	5	IM6514C	Intersil	110
						IM6514M	† Intersil	

(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature
OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY-RAMs (Cont'd)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage,	Device	Source	Line
1024x4							(Cont'd)	
	200 nsF	CMOS	TS	18	5	**HM6514B-2**	**† Harris (1333,3767)**	
						HM6514B-9	**Harris (1333,3767)**	
						HS6514RH	† Harris	
						μPD444-3	NEC-Micro	
						μPD444/44/6514-3	NEC-Micro	
						MSM5114-2	**OKI (3873)**	
						MSM5115-2	**OKI (3873)**	
						MWS5114-3	**† RCA (3874)**	
						SCM5114-1	SSS	
						SCM6514-1	SSS	10
						TC5514A-2	Toshiba	
						TC5514AL-2	Toshiba	
		NMOS	TS	18	5	AM9114E	AMD	
						AM9124E	AMD	
						AM91L14E	AMD	
						AM91L24E	AMD	
						2114-2	Fairchild	
						2114L-2	Fairchild	
						M2114-2	† GTE Micro	
						HM472114A-2	**Hitachi (3789)**	20
						2114A-4	Intel	
						2114AL-4	Intel	
						M2114A-4	† Intel	
						M2114AL-4	† Intel	
						M5L2114L-2	Mitsubishi	
						MCM2114-20	**Motorola (3839)**	
						MCM21L14-20	**Motorola (3839)**	
						MM2114-2	National	
						MM2114-2L	National	
						NMC2114A-4	**National (3858)**	30
						NMC2114A-4L	**National (3858)**	
						MSM2114-2	**OKI (3873)**	
						MSM2114L-2	**OKI (3873)**	
						SY2114-2	**Synertek (3941)**	
						SY2114A-4	**Synertek (3941)**	
						SY2114AL-4	**Synertek (3941)**	
						SY2114L-2	**Synertek (3941)**	
						SY2114LV-2	**Synertek (3941)**	
						SYM2114A-4	**† Synertek (424)**	
						TMS2114-20	TI	40
						TMS2114L-20	TI	
						TMM314A-1	Toshiba	
						TMM314AL-1	Toshiba	
				20	5	2142-2	Intel	
						2142L-2	Intel	
						SY2142-2	Synertek	
						SY2142L-2	Synertek	
				22	5	AM9130EC	AMD	
	250 nsF	CMOS	TS	18	5	SRM2114	Epson	
						SRM6514	Epson	50
						μPD444/44/6514-2	NEC-Micro	
						MWS5114-2	**† RCA (3874)**	
		NMOS	TS	18	5	2114A-5	Intel	
							(Continued)	

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage,	Device	Source	Line
1024x4	250 nsF	NMOS	TS	18	5		(Cont'd)	
						M2114A-5	† Intel	
						MCM2114-25	**Motorola (3839)**	
						MCM21L14-25	**Motorola (3839)**	
						NMC214A-5	National	
						SY2114A-5	**Synertek (3941)**	
						SYM2114A-5	**† Synertek (424)**	
						TMS2114-25	TI	60
						TMS2114L-25	TI	
				22	5	AM9130DC	AMD	
						AM91L30DC	AMD	
	300 nsF	CMOS	TS	18	5	S6514	AMI	
						MB8414E	Fujitsu	
						HM6514-2	**† Harris (1333,3767)**	
						HM6514-9	**Harris (1333,3767)**	
						HM6514C-9	**Harris (1333,3767)**	
						HM4434-3	Hitachi	
						NMC6514-2	† National	70
						NMC6514-9	National	
						μPD444/44/6514-1	NEC-Micro	
						MSM5514-3	OKI	
						MSM5515-3	OKI	
						MWS5114-1	**† RCA (3874)**	
						SCM5514-3	SSS	
						SCM5514-5	SSS	
						SCM6514-3	SSS	
						TC5514A-3	Toshiba	
						TC5514AL-3	Toshiba	80
		NMOS	TS	18	5	AM9114C	AMD	
						AM9114CM	† AMD	
						AM9124C	AMD	
						AM9124CM	† AMD	
						AM91L14C	AMD	
						AM91L14CM	† AMD	
						AM91L24C	AMD	
						AM91L24CM	† AMD	
						2114-3	Fairchild	
						2114-3M	† Fairchild	90
						2114L-3	Fairchild	
						M2114-3M	† GTE Micro	
						HM472114-3	**Hitachi (3789)**	
						2114A-6	Intel	
						M5L2114L-3	Mitsubishi	
						MCM2114-30	**Motorola (3839)**	
						MCM21L14-30	**Motorola (3839)**	
						MM2114-3	National	
						MM2114-3L	National	
						MSM2114-3	**OKI (3873)**	100
						MSM2114L-3	**OKI (3873)**	
						SY2114-3	**Synertek (3941)**	
						SY2114L-3	**Synertek (3941)**	
						SYM2114-3	**† Synertek (424)**	
				20	5	2142-3	Intel	
						2142L-3	Intel	
						SY2142-3	Synertek	
						SY2142L-3	Synertek	
				22	5	AM9130CC	AMD	
							(Continued)	

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

MEMORY-RAMs (Cont'd)

Static

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage,	Device	Source	Line
							(Cont'd)	
1024x4	300 nsF	NMOS	TS	22	5	AM9130CM	† AMD	
						AM91L30CC	AMD	
						AM91L30CM	† AMD	
	350 nsF	CMOS	TS	18	5	**HM6514-5**	**Harris (1333,3767)**	
						NMC6514-5	National	
						SCM6514-5	SSS	
	400 nsF	NMOS	TS	22	5	AM9130BC	AMD	
						AM9130BM	† AMD	
						AM91L30BC	AMD	
						AM91L30BM	† AMD	10
	450 nsF	CMOS	TS	18	5	**HM4334-4**	**Hitachi (3789)**	
						M58981-45	Mitsubishi	
						µPD444/6514	NEC-Micro	
						MWS5114A	**† RCA (3874)**	
						MWS5114A-5	**† RCA (3874)**	
						SCM5114-8	SSS	
				20	5	µPD445L	NEC-Micro	
						TC5514	Toshiba	
		NMOS	TS	18	5	AM9114B	AMD	
						AM9114BM	† AMD	20
						AM9124B	AMD	
						AM9124BM	† AMD	
						AM91L14B	AMD	
						AM91L14BM	† AMD	
						AM91L24B	AMD	
						AM91L24BM	† AMD	
						2114	Fairchild	
						2114L	Fairchild	
						2114M	† Fairchild	
						L2114UM	† GTE Micro	30
						HM472114-4	**Hitachi (3789)**	
						M5L2114L	Mitsubishi	
						MCM2114-45	**Motorola (3839)**	
						MCM21L14-45	**Motorola (3839)**	
						MM2114	National	
						MM2114L	National	
						EA2114L	NEC-EA	
						µPD2114L	NEC-Micro	
						MSM2114	**OKI (3873)**	
						MSM2114L	**OKI (3873)**	40
						MN2114	Panasonic	
						SY2114	**Synertek (3941)**	
						SY2114L	**Synertek (3941)**	
						SYM2114	**† Synertek (424)**	
						TMS2114-45	TI	
						TMS2114L-45	TI	
						TMM314A	Toshiba	
						TMM314AL	Toshiba	
				20	5	2142	Intel	
						2142L	Intel	50
						SY2142	Synertek	
						SY2142L	Synertek	
	500 nsF	NMOS	TS	22	5	AM9130AC	AMD	
						AM9130AM	† AMD	
						AM91L30AC	AMD	
						AM91L30AM	† AMD	
	550 nsF	CMOS	TS	20	5	TC5047A-1	Toshiba	
	650 nsF	CMOS	TS	18	10	CDP1825	† RCA	
						CDP1825C	† RCA	

(Continued)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage,	Device	Source	Line
							(Cont'd)	
1024x4	650 nsF	CMOS	TS	20	5	µPD445L-1	NEC-Micro	60
						TC5514-1	Toshiba	
	800 nsF	CMOS	TS	20	5	TC5047A-2	Toshiba	
						TC5514-2	Toshiba	
1024x8	55 nsF	NMOS	TS	24	5	MK4801A-55	Mostek	
	70 nsF	NMOS	TS	24	5	MK4801A-70	Mostek	
						MKB4801A-870	† Mostek	
	90 nsF	NMOS	TS	24	5	MK4801A-90	Mostek	
						MKB4801A-890	† Mostek	
						SY2158A-1	**Synertek (3943)**	
						SY2158B-1	**Synertek (3943)**	70
						SY2158L-1	**Synertek (3943)**	
						SY2159A-1	**Synertek (3943)**	
						SY2159B-1	**Synertek (3943)**	
						SY2159L-1	**Synertek (3943)**	
	100 nsF	NMOS	TS	48	5	**SY21D1**	**Synertek (3947)**	
	120 nsF	NMOS	TS	24	5	MK4118A-1	Mostek	
						MKB4801A-81	† Mostek	
						SY2158A-2	**Synertek (3943)**	
						SY2158B-2	**Synertek (3943)**	
						SY2158L-2	**Synertek (3943)**	80
						SY2159A-2	**Synertek (3943)**	
						SY2159B-2	**Synertek (3943)**	
						SY2159L-2	**Synertek (3943)**	
	150 nsF	NMOS	TS	22	5	µPD421-5	NEC-Micro	
				24	5	MK4118A-2	Mostek	
						MKB4118A-82	† Mostek	
						SY2158A-3	**Synertek (3943)**	
						SY2158B-3	**Synertek (3943)**	
						SY2158B-4	**Synertek (3943)**	
						SY2158L-3	**Synertek (3943)**	90
						SY2159A-3	**Synertek (3943)**	
						SY2159B-3	**Synertek (3943)**	
						SY2159L-3	**Synertek (3943)**	
	200 nsF	NMOS	TS	22	5	M8104-2M	† GTE Micro	
						µPD421-3	NEC-Micro	
				24	5	MK4118A-3	Mostek	
						MKB4118A-83	† Mostek	
						SY2158A-4	**Synertek (3943)**	
						SY2158L-4	**Synertek (3943)**	
						SY2159A-4	**Synertek (3943)**	100
						SY2159B-4	**Synertek (3943)**	
						SY2159L-4	**Synertek (3943)**	
	250 nsF	CMOS	TS	24	5	HM6515-9	Harris	
		NMOS	TS	22	5	µPD421-2	NEC-Micro	
				24	5	MK4118A-4	Mostek	
						MKB4118A-84	† Mostek	
	300 nsF	NMOS	TS	22	5	µPD421-1	NEC-Micro	
						R8104-3	Rockwell	
	400 nsF	NMOS	TS	22	5	R8114-3	Rockwell	
	450 nsF	NMOS	TS	22	5	µPD421	NEC-Micro	110
2048x1	300 nsF	CMOS	TS	18	5	HM6503-9	Harris	
						NMC6503-9	† National	
	350 nsF	CMOS	TS	18	5	HM6503-5	Harris	
						NMC6503-5	National	
2048x8	55 nsF	CMOS	TS	24	5	**HM65161B-5**	**Harris (669,1333,3774)**	
	70 nsF	CMOS	TS	24	5	**HM65161-5**	**Harris (669,1333,3774)**	
						IDT6116S70	**IDT (3793)**	

(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature
OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY–RAMs (Cont'd)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage,	Device	Source	Line
2048x8	70 nsF						(Cont'd)	
		NMOS	TS	24	5	AM9218-70	AMD	
	90 nsF	CMOS	TS	24	5	**IDT6116L90**	**† IDT (3793)**	
						IDT6116L90	IDT	
						IDT6116S90	**† IDT (3793)**	
						IDT6116S90	IDT	
		NMOS	TS	24	5	**SY2128-1**	**Synertek (3944)**	
						SY2128L-1	**Synertek (3944)**	
						SY2129-1	**Synertek (3944)**	
						SY2129L-1	**Synertek (3944)**	
	100 nsF	NMOS	TS	24	5	AM9218-10	AMD	10
						F3528-10	**Fairchild (3664)**	
						F3528L-10	**Fairchild (3664)**	
						MB8128-10	Fujitsu	
	120 nsF	CMOS	TS	24	5	**HM6116-2**	**† Harris (669,1333,3777)**	
						HM6116-2	**Hitachi (3789)**	
						HM6116L-2	**Hitachi (3789)**	
						IDT6116L120	**† IDT (3793)**	
						IDT6116L120	IDT	
						IDT6116S120	**† IDT (3793)**	
						IDT6116S120	IDT	20
						M5M5116-12	Mitsubishi	
						M5M5117-12	Mitsubishi	
						M5M5118-12	Mitsubishi	
						SCM6116-2	SSS	
						TMS4016-12	**TI (3968)**	
		NMOS	TS	24	5	**F3528-12**	**Fairchild (3664)**	
						F3528L-12	**Fairchild (3664)**	
						HM6516B-2	**† Harris (669,1333,3772)**	
						HM6516B-9	**Harris (669,1333,3772)**	
						2128-12	Intel	30
						MKB4802-81	† Mostek	
						SY2128-2	**Synertek (3944)**	
						SY2128L-2	**Synertek (3944)**	
						SY2129-2	**Synertek (3944)**	
						SY2129L-2	**Synertek (3944)**	
	150 nsF	CMOS	TS	24	5	S6516	AMI	
						HM6116-3	**Hitachi (3789)**	
						HM6116L-3	**Hitachi (3789)**	
						IDT6116L150	**† IDT (3793)**	
						IDT6116L150	IDT	40
						IDT6116S150	**† IDT (3793)**	
						IDT6116S150	IDT	
						M5M5116-15	Mitsubishi	
						M5M5117-15	Mitsubishi	
						M5M5118-15	Mitsubishi	
						MCM65116-15	**Motorola (3839)**	
						SCM6116-3	SSS	
		NMOS	TS	24	5	AM9218-15	AMD	
						F3528-15	**Fairchild (3664)**	
						F3528L-15	**Fairchild (3664)**	50
						MB8128-15	Fujitsu	
						2128-15	Intel	
						M2128	† Intel	
						M58275-15	Mitsubishi	
						MCM2016-15	**Motorola (3839,3846)**	
						MCM65116-12	**Motorola (3839)**	
						NMC2116-15	**National (3859)**	
						NMC2116-15L	**National (3859)**	

(Continued)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage,	Device	Source	Line
2048x8	150 nsF	NMOS	TS	24	5		(Cont'd)	
						SY2128-3	**Synertek (3944)**	
						SY2128L-3	**Synertek (3944)**	60
						SY2129-3	**Synertek (3944)**	
						SY2129L-3	**Synertek (3944)**	
						SYM2128-3	**† Synertek (427)**	
						SYM2129-3	**† Synertek (427)**	
						TM54016-15	TI	
						TMM2016	Toshiba	
	200 nsF	CMOS	TS	24	5	SRM2016C20	Epson	
						SRM2017C20	Epson	
						SRM2018C20	Epson	
						MB8418	Fujitsu	70
						MB8416	**Fujitsu (3676)**	
						MB8417	**Fujitsu (3676)**	
						MB8418	**Fujitsu (3676)**	
						HM6116-4	**Hitachi (3789)**	
						HM6116L-4	**Hitachi (3789)**	
						MP6116-20	Micro Pwr	
						MP6117-20	Micro Pwr	
						MP6118-20	Micro Pwr	
						MP8416-20	Micro Pwr	
						MP8417-20	Micro Pwr	80
						MP8418-20	Micro Pwr	
						M5M5116	Mitsubishi	
						M5M5117	Mitsubishi	
						M5M5118	Mitsubishi	
						MSM5128	**OKI (3873)**	
						SCM6116-4	SSS	
		NMOS	TS	24	5	AM9218-20	AMD	
						F3528-20	**Fairchild (3664)**	
						F3528L-20	**Fairchild (3664)**	
						2128-20	Intel	90
						M58725	Mitsubishi	
						MCM2016-20	**Motorola (3839,3846)**	
						NMC2116-20L	**National (3859)**	
						NMC2116-25L	**National (3859)**	
						MSM2128	**OKI (3873)**	
						MSM2128-1	**OKI (3873)**	
						SY2128-4	**Synertek (3944)**	
						SY2128L-4	**Synertek (3944)**	
						SY2129-4	**Synertek (3944)**	
						SY2129L-4	**Synertek (3944)**	100
						SYM2128-4	**† Synertek (427)**	
						SYM2129-4	**† Synertek (427)**	
						TMS4016-20	**TI (3968)**	
						TMM2016-2	Toshiba	
	250 nsF	CMOS	TS	24	5	SRM2016C25	Epson	
						SRM2017C25	Epson	
						SRM2018C25	Epson	
						MP6116-25	Micro Pwr	
						MP6117-25	Micro Pwr	
						MP6118-25	Micro Pwr	110
						MP8416-25	Micro Pwr	
						MP8417-25	Micro Pwr	
						MP8418-25	Micro Pwr	
						TC5516	Toshiba	
						TC5516A	Toshiba	
						TC5516A-2	Toshiba	
						TC5516AL	Toshiba	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

MEMORY–RAMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage,	Device	Source	Line
Static							**(Cont'd)**	
							(Cont'd)	
2048x8	250 nsF	CMOS	TS	24	5	TC5516AL-2	Toshiba	
						TC5517A	Toshiba	
						TC5517AL	Toshiba	
						TC5517AL-2	Toshiba	
						TC5518A-2	Toshiba	
						TC5518B	Toshiba	
						TC5518BL	Toshiba	
		NMOS	TS	24	5	**NMC2116-25**	**National (3859)**	
						TMS4016-25	**TI (3968)**	
	300 nsF	NMOS	TS	24	5	MPS2316A	CSG	10
						MPS2316B	CSG	
	350 nsF	NMOS	TS	24	5	**F3528-35**	**Fairchild (3664)**	
4096x1	7 nsF	ECL	OE	18	−5.2	HM2140	Hitachi	
						HM2142	Hitachi	
	15 nsF	ECL	OE	18	−5.2	**HM10470-1**	**Hitachi (3789)**	
						DM10470A	**National (3855)**	
				18	5	AM100470SA	AMD	
						AM10470SAC	AMD	
					−5.2	**MBM10470A-15**	**Fujitsu (3681)**	
	20 nsF	ECL	OE	18	5	AM10470SAM †	AMD	20
						MBM100470	**Fujitsu (3681)**	
					−5.2	**MBM10470A-20**	**Fujitsu (3681)**	
	25 nsF	ECL	OE	18	5	AM100470A	AMD	
						AM10470AC	AMD	
					−4.5	**HM100470**	**Hitachi (3789)**	
						HM10470	**Hitachi (3789)**	
						DM10470	**National (3855)**	
						DM10470L	**National (3855)**	
						100470A	Signetics	
						10470A	Signetics	30
	30 nsF	ECL	OE	18	5	AM10470AM †	AMD	
	35 nsF	CMOS	TS	18	5	MBM2147H-35	Fujitsu	
						HM6147H-35	**Hitachi (3789)**	
						HM6147HL-35	**Hitachi (3789)**	
		ECL	OE	18	5	AM100470	AMD	
						AM10470C	AMD	
					−4.5	100470	Signetics	
						10470	Signetics	
					−5	**F100470**	**Fairchild (3615,3628)**	
						F10470C	**Fairchild (3615,3621)**	40
						MBM10470	**Fujitsu (3681)**	
		NMOS	TS	18	5	AM2147-35	AMD	
						2147H-1	Intel	
	40 nsF	ECL	OE	18	5	AM10470M †	AMD	
		NMOS	TS	18	5	MBM2147H-45	Fujitsu	
	45 nsF	CMOS	TS	18	5	**HM6147HL-45**	**Hitachi (3789)**	
		NMOS	TS	18	5	AM2147-45	AMD	
						AM21L47-45	AMD	
						HM4847-2	Hitachi	
						2147H-2	Intel	50
						MM2148H-2	National	
		TTL	TS	18	5	**93471C**	**Fairchild (3615,3643)**	
	55 nsF	CMOS	TS	18	5	**HM6147-3**	**Hitachi (3789)**	
							(Continued)	

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage,	Device	Source	Line
4096x1	55 nsF	CMOS	TS	18	5		(Cont'd)	
						HM6147L-3	**Hitachi (3789)**	
						MCM65147-55	**Motorola (3839,3845)**	
		NMOS	TS	18	5	9147-55	AMD	
						AM2147-55	AMD	
						AM21L47-55	AMD	
						AM9147-55	AMD	
						MBM2147H	Fujitsu	60
						HM4847-3	Hitachi	
						2147-3	Intel	
						2147A-3	Intel	
						2147AL-3	Intel	
						2147H-3	Intel	
						2147HL-3	Intel	
						M2147H-3 †	Intel	
						ITT2147-55	ITT	
						MCM2147-55	Motorola	
						MM2147-3	National	70
						MM2148H-3	National	
						MM2148H-3L	National	
						NMC2147H-3	National	
						NMC2147H-4	National	
						μPD2147-3	NEC-Micro	
						SY2147-3	**Synertek (3941)**	
						SYM2147-3 †	**Synertek (425)**	
						SYM2147-6 †	**Synertek (425)**	
						TMM315-1	Toshiba	
						UM2147-1	Universal	80
				20	5	**MB8168-55**	**Fujitsu (3675)**	
	60 nsF	TTL	TS	18	5	**93471M** †	**Fairchild (3615,3643)**	
	70 nsF	CMOS	TS	18	5	**HM6147**	**Hitachi (3789)**	
						HM6147L	**Hitachi (3789)**	
						MCM65147-70	**Motorola (3839,3845)**	
						MCM65147-85	**Motorola (3839,3845)**	
		NMOS	TS	18	5	AM2147-70	AMD	
						AM21L47-70	AMD	
						AM9147-70	AMD	
						AM9147-70M †	AMD	90
						AM91L47	AMD	
						MBM2147E	Fujitsu	
						HM4847	Hitachi	
						2147A	Intel	
						2147AL	Intel	
						2147H	Intel	
						2147HL	Intel	
						M2147H †	Intel	
						2147	Intersil	
						ITT2147-70	ITT	100
						MCM2147-70	Motorola	
						MM2147	National	
						MM2147L	National	
						MM2148H	National	
						MM2148H-L	National	
						μPD2147-2	NEC-Micro	
						SY2147	**Synertek (3941)**	
						SY2147L	**Synertek (3941)**	
						SYM2147 †	**Synertek (425)**	
	85 nsF	CMOS	TS	18	5	TMM315	Toshiba	110
		NMOS	TS	18	5	AM9147-85M †	AMD	
						HM6147-6	**Hitachi (3789)**	
						MCM2147-85	Motorola	
						MM2147M †	National	
4096X1	85 nsF	NMOS	TS	18	5	**SY2147-6**	**Synertek (3941)**	

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature
OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY-RAMs (Cont'd)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage,	Device	Source	Line
4096x1	90 nsF	NMOS	TS	18	5	ITT2147-90	ITT	
	100 nsF	NMOS	TS	18	5	MCM2147-100	Motorola	
						μPD2147	NEC-Micro	
	120 nsF	NMOS	TS	18	5	2141-2	Intel	
						NMC2141-2	National	
	150 nsF	NMOS	TS	18	5	AM4044-15	AMD	
						AM4244-15	AMD	
						2141-3	Intel	
						2141L-3	Intel	
						NMC2141-3	National	10
	180 nsF	CMOS	TS	18	5	HS6504RH	† Harris	
	200 nsF	CMOS	TS	18	5	**HM6504B-2**	† **Harris (669,1333,3762)**	
						HM6504B-9	**Harris (669,1333,3762)**	
						HM6505B-2	† Harris	
						HM6505B-9	Harris	
						IM6504C	Intersil	
						IM6504M	† Intersil	
						MSM5104-2	**OKI (3873)**	
						SCM6504-1	SSS	
						TC5504A-2	Toshiba	20
		NMOS	TS	18	5	AM4044-20	AMD	
						AM4244-20	AMD	
						2141-4	Intel	
						2141L-4	Intel	
						IM7141-2	Intersil	
						IM7141-2M	† Intersil	
						IM7141L-2	Intersil	
						M5T4044-20	Mitsubishi	
						MK4104-3	Mostek	
						MK4104-33	Mostek	30
						MCM6641-20	Motorola	
						MCM66L41-20	Motorola	
						μPD4104-2	NEC-Micro	
						TMS4044-20	TI	
						TMS40L44-20	TI	
				22	5	AM9140EC	AMD	
	250 nsF	CMOS	TS	18	5	SRM6504	Epson	
		NMOS	TS	18	5	AM4044-25	AMD	
						AM4244-25	AMD	
						2141-5	Intel	40
						2141L-5	Intel	
						MK4104-34	Mostek	
						MK4104-4	Mostek	
						MKB4104-84	† Mostek	
						MCM6641-25	Motorola	
						MCM66L41-25	Motorola	
						MM5257-25	National	
						MM5257-25L	National	
						μPD4104-1	NEC-Micro	
						TMS4044-25	TI	50
						TMS40L44-25	TI	
				22	5	9140DC	AMD	
						91L40DC	AMD	
	300 nsF	CMOS	TS	18	5	**HM6504-2**	† **Harris (669,1333,3762)**	
						HM6504-9	**Harris (669,1333,3762)**	
						HM6504C-9	**Harris (669,1333,3762)**	
						HM6505-2	† Harris	

(Continued)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage,	Device	Source	Line
4096x1	300 nsF	CMOS	TS	18	5			(Cont'd)
						HM6505-9	Harris	
						NMC6404-9	National	
						NMC6504-2	† National	60
						NMC6504-9	National	
						MSM5104-3	**OKI (3873)**	
						SCM6504-3	SSS	
						TC5504A-3	Toshiba	
		NMOS	TS	18	5	4044-30	AMD	
						4244-30	AMD	
						IM7141-3	Intersil	
						IM7141-3M	† Intersil	
						IM7141L-3	Intersil	
						M5T4044-30	Mitsubishi	70
						MK4104-35	Mostek	
						MK4104-5	Mostek	
						MKB4104-85	† Mostek	
						MCM6641-30	Motorola	
						MCM66L41-30	Motorola	
						MM5257-3	National	
						MM5257-3L	National	
						μPD4104	NEC-Micro	
				22	5	9140CC	AMD	
						9140CM	† AMD	80
						91L40CC	AMD	
						91L40CM	† AMD	
	320 nsF	CMOS	TS	18	5	S6504	AMI	
						MB8404E	Fujitsu	
	350 nsF	CMOS	TS	18	5	**HM6504-5**	**Harris (669,1333,3762)**	
						HM6505-5	Harris	
						NMC6504-5	National	
						SCM6504-5	SSS	
		NMOS	TS	18	5	MK4104-6	Mostek	
						MKB4104-86	† Mostek	90
	400 nsF	NMOS	TS	22	5	9140BC	AMD	
						9140BM	† AMD	
						91L40BC	AMD	
						91L40BM	† AMD	
	450 nsF	CMOS	TS	18	5	**HM4315**	**Hitachi (3789)**	
		NMOS	TS	18	5	4044-45	AMD	
						4244-45	AMD	
						IM7141	Intersil	
						IM7141L	Intersil	
						IM7141M	† Intersil	100
						MCM6641-45	Motorola	
						MCM66L41-45	Motorola	
						MM5257	National	
						MM5257L	National	
						TMS4044-45	TI	
						TMS40L44-45	TI	
	500 nsF	NMOS	TS	22	5	9140AC	AMD	
						9140AM	† AMD	
						91L40AC	AMD	
						91L40AM	† AMD	110
	550 nsF	CMOS	TS	18	5	TC5504-1	Toshiba	
	800 nsF	CMOS	TS	18	5	TC5504-2	Toshiba	
4096x4	30 nsF	MNOS	TS	20	5	**IMS1421**	**Inmos (3790)**	
	45 nsF	CMOS	TS	20	5	**IDT6168L45**	† **IDT (3804)**	
						IDT6168L45	**IDT (3804)**	
						IDT6168S45	† **IDT (3804)**	
						IDT6168S45	**IDT (3804)**	
				24	5	**IDT71681L45**	† **IDT (3805)**	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

MEMORY-RAMs (Cont'd)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source		Line
4096x4	45 nsF	CMOS	TS	24	5			(Cont'd)	
						IDT71681L45	IDT	(3805)	
						IDT71681S45 †	IDT	(3805)	
						IDT71681S45	IDT	(3805)	
		NMOS	TS	20	5	IMS1420	Inmos	(3790)	
	55 nsF	CMOS	TS	20	5	IDT6168L55 †	IDT	(3804)	
						IDT6168L55	IDT	(3804)	
						IDT6168S55 †	IDT	(3804)	
						IDT6168S55	IDT	(3804)	
				24	5	IDT71681L55 †	IDT	(3805)	
						IDT71681L55	IDT	(3805)	10
						IDT71681S55 †	IDT	(3805)	
						IDT71681S55	IDT	(3805)	
	70 nsF	CMOS	TS	20	5	IDT6168L70 †	IDT	(3804)	
						IDT6168L70	IDT	(3804)	
						IDT6168S70 †	IDT	(3804)	
						IDT6168S70	IDT	(3804)	
				24	5	IDT71681L70	IDT	(3805)	
						IDT71681L70	IDT	(3805)	
						IDT71681S70 †	IDT	(3805)	
						IDT71681S70	IDT	(3805)	20
		NMOS	TS	20	5	MB8168-70	Fujitsu	(3675)	
						IMS1420L	Inmos	(3790)	
						SY2169	Synertek	(3946)	
				24	5	SY2168	Synertek	(3946)	
						SYM2168 †	Synertek	(429)	
						SYM2169 †	Synertek	(429)	
	85 nsF	CMOS	TS	20	5	IDT6168L85 †	IDT	(3804)	
						IDT6168L85	IDT	(3804)	
						IDT6168S85 †	IDT	(3804)	
						IDT6168S85	IDT	(3804)	30
				24	5	IDT71681L85 †	IDT	(3805)	
						IDT71681L85	IDT	(3805)	
						IDT71681S85 †	IDT	(3805)	
						IDT71681S85	IDT	(3805)	
	100 nsF	CMOS	TS	20	5	IDT6168L100 †	IDT	(3804)	
						IDT6168L100	IDT	(3804)	
						IDT6168S100	IDT	(3804)	
				24	5	IDT71681L100 †	IDT	(3805)	
						IDT71681L100	IDT	(3805)	
						IDT71681S100 †	IDT	(3805)	40
						IDT71681S100	IDT	(3805)	
4096x8	200 nsF	NMOS	—	28	5	8148	Intel		
8192x8	100 nsF	CMOS	TS	28	5	HM6264-10	Hitachi		
						TC5564	Toshiba		
						TC5564L	Toshiba		
						TC5565	Toshiba		
						TC5565L	Toshiba		
	120 nsF	CMOS	TS	28	5	HM6264-12	Hitachi		
	150 nsF	CMOS	TS	28	5	HM6264-15	Hitachi		
						TC5564-1	Toshiba		50
						TC5564L-1	Toshiba		
						TC5565-1	Toshiba		
		NMOS	TS	28	5	NMC4864	National		
	200 nsF	NMOS	TS	28	5	2186/7	Intel	(3810)	
	250 nsF	NMOS	TS	28	5	2186-25	Intel	(3810)	
	260 nsF*	CMOS	TS	40	5	HS6564RH †	Harris		
	300 nsF	NMOS	TS	28	5	2186-30	Intel	(3810)	
	350 nsF	CMOS	TS	40	5	HM5-6564-2 †	Harris	(3779)	
						HM5-6564-8	Harris	(3779)	
						HM5-6564-9	Harris	(3779)	60
	450 nsF	CMOS	TS	40	5	HM5-6564-5	Harris	(3779)	
16384x1	25 nsF	ECL	OE	20	−4.5	MBM100480	Fujitsu	(3680)	
					−5.2	MBM10480	Fujitsu	(3680)	
	35 nsF	ECL	OE	20	−4.5	F100480	Fairchild	(3630)	
					−5.2	F10480	Fairchild		
	40 nsF	NMOS	TS	20	5	IMS1400	Inmos	(3790)	
	45 nsF	CMOS	TS	20	5	IDT6167L45	IDT	(3799)	
						IDT6167S45	IDT	(3799)	
		NMOS	TS	20	5	MB8167A-45	Fujitsu	(3675)	
						ITT2167-45	ITT		70
	55 nsF	CMOS	TS	20	5	IDT6167L55	IDT	(3799)	
				24	5	IDT6167S55 †	IDT	(3799)	
						IDT6167S55	IDT	(3799)	
		NMOS	TS	20	5	MB8167A-55	Fujitsu	(3675)	
						2167-55	Intel		
						ITT2167-55	ITT		
						μPD2167	NEC-Micro		
	70 nsF	CMOS	TS	20	5	HM6167	Hitachi	(3789)	
						IDT6167L70	IDT	(3799)	
						IDT6167S70	IDT	(3799)	80
		NMOS	TS	20	5	MB8167A-70	Fujitsu	(3675)	
						IMS1400L	Inmos	(3790)	
						2167-70	Intel		
						2167L-70	Intel		
						ITT2167-70	ITT		
						MKB4167-870	† Mostek		
						SY2167	Synertek	(3945)	
				24	5	SYM2167	† Synertek	(428)	
	85 nsF	CMOS	TS	20	5	HM6167-6	Hitachi	(3789)	
						HM6167L-6	Hitachi	(3789)	90
						IDT6167L85 †	IDT	(3799)	
						IDT6167L85	IDT	(3799)	
						IDT6167S85 †	IDT	(3799)	
						IDT6167S85	IDT	(3799)	
						MKB4167-885	† Mostek		
	100 nsF	CMOS	TS	20	5	HM6167-8	Hitachi	(3789)	
						HM6167L-8	Hitachi	(3789)	
						IDT6167S100	IDT	(3799)	
				24	5	IDT6167L100 †	IDT	(3799)	
						IDT6167L100	IDT	(3799)	100
		NMOS	TS	20	5	2167-10	Intel		
						M2167-10 †	Intel		
						MKB4167-80 †	Mostek		
16384x4	350 nsF	CMOS	TS	40	5	HM5-6564-2 †	Harris		
						HM5-6564-8	Harris		
						HM5-6564-9	Harris		
	450 nsF	CMOS	TS	40	5	HM5-6564-5	Harris		
65536x1	150 nsF	NMOS	TS	16	5	ITT4164-15	ITT		
	200 nsF	NMOS	TS	16	5	ITT4164-20	ITT		

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature
OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY–ROMs

Static

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source		Line
32x8	45 nsR	TTL	OC	16	5	**SN7488A**	**TI**	**(863)**	
256x4	1.8 μsR	CMOS	—	16	3-15	**MCM14524A**	**† Motorola**	**(3840)**	
						MCM14524C	**Motorola**	**(3840)**	
	60 nsF	TTL	OC	16	5	**SN74187**	**TI**	**(900)**	
256x8	70 nsF	TTL	OC	20	5	**SN74S271**	**TI**	**(919)**	
			TS	20	5	**SN74S371**	**TI**	**(937)**	
512x4	70 nsF	TTL	OC	16	5	**SN74S270**	**TI**	**(919)**	
			TS	16	5	**SN74S370**	**TI**	**(936)**	
512x8	70 nsF	NMOS	TS	24	5	82HM141C	Intersil		
	90 nsF	NMOS	TS	24	5	82HM141M	† Intersil		10
	500 nsF	CMOS	TS	24	10	HCMP1831	Hughes		
						HCMP1832	Hughes		
						HMMP1831	† Hughes		
						HMMP1832	† Hughes		
						CDP1831	**† RCA**	**(3876)**	
						CDP1832	† RCA		
		NMOS	TS	24	5	9214C	AMD		
						9214M	† AMD		
	700 nsF	PMOS	TS	24	5	3514	AMD		
					−12,5	3514	Fairchild		20
	1000 nsF								
		CMOS	TS	24	5	HCMP1831C	Hughes		
						HCMP1832C	Hughes		
						HMMP1831C	† Hughes		
						HMMP1832C	† Hughes		
						CDP1831C	**† RCA**	**(3876)**	
						CDP1832C	† RCA		
512x10	500 nsF	NMOS	TS	24	5	R03-5120	GI		
1024x4	60 nsF	HMOS	TS	24	5	82HM137C	Intersil		
	80 nsF	HMOS	TS	24	5	82HM137M	† Intersil		
1024x8	45 nsF	TTL	TS	22	5	MB7130E	Fujitsu		30
						MB7130H	Fujitsu		
	55 nsF	TTL	OC	24	5	6280-2	MMI		
			TS	24	5	6281-2	MMI		
	70 nsF	HMOS	TS	24	5	82HM181C	Intersil		
		NMOS	TS	24	5	**SY3308**	**Synertek**	**(3954)**	
	75 nsF	TTL	OC	24	5	5280-2	† MMI		
			TS	24	5	5281-2	† MMI		
	90 nsF	HMOS	TS	24	5	82HM181M	† Intersil		
		TTL	OC	24	5	DM75S29	† National		
			TS	24	5	DM75S28	† National		40
	100 nsF	TTL	OC	24	5	6280-1	MMI		
						6282-1	MMI		
			TS	24	5	6281-1	MMI		
						6283-1	MMI		
	175 nsF	TTL	OC	24	5	AM27S80C	AMD		
						AM29882C	AMD		
						5280-1	† MMI		
						5282-1	† MMI		
			TS	24	5	AM27S81C	AMD		
						AM27S83C	AMD		50
						AM29883C	AMD		
						5281-1	† MMI		
						5283-1	† MMI		
	250 nsF	NMOS	TS	24	5	F68B308	Fairchild		
						MCM68B308	**Motorola**	**(3840)**	
						MCM68B30A	Motorola		
					5,12	9208D	AMD		
	275 nsF	TTL	OC	24	5	AM27S80M	† AMD		
						AM27S82M	† AMD		
						AM29882M	† AMD		60
			TS	24	5	AM27S81M	† AMD		

(Continued)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source		Line
1024x8	275 nsF	TTL	TS	24	5				
						AM27S83M	† AMD		
						AM29883M	† AMD		
	300 nsF	NMOS	TS	24	5,12	9208CC	AMD		
	350 ns *	CMOS	TS	24	10	HCMP1833	Hughes		
						HCMP1834	Hughes		
						HMMP1833	† Hughes		
						HMMP1834	† Hughes		
						CDP1833	**† RCA**	**(3876)**	
						CDP1834	**† RCA**	**(3877)**	70
	350 nsF	NMOS	TS	24	5	MCM68A30A	Motorola		
						μPD8308A-5	NEC-EA		
					±5,12	**MCM68A308**	**Motorola**	**(3840)**	
						MCM68A308P7	Motorola		
	400 nsF	NMOS	TS	24	5,12	9208BC	AMD		
						9208BM	† AMD		
	450 nsF	NMOS	TS	24	5	μPD8308A	NEC-EA		
					±5,12	8308	AMD		
						μPD2308A	NEC-EA		
	500 nsF	NMOS	TS	24	5	HN46830	Hitachi		80
	550 nsF	NMOS	TS	24	5	μPD8308AL	NEC-EA		
	850 ns *	NMOS	TS	24	5	HCMP1833C	Hughes		
						HCMP1834C	Hughes		
						HMMP1833C	† Hughes		
						HMMP1834C	† Hughes		
						CDP1833C	**† RCA**	**(3876)**	
						CDP1834C	**† RCA**	**(3877)**	
1024x9	100 nsF	TTL	OC	24	5	6260-1	MMI		
			TS	24	5	6261-1	MMI		
	150 nsF	TTL	OC	24	5	5260-1	† MMI		90
			TS	24	5	5261-1	† MMI		
1024x10	100 nsF	TTL	OC	24	5	6255-1	MMI		
			TS	24	5	6256-1	MMI		
	150 nsF	TTL	OC	24	5	5255-1	† MMI		
			TS	24	5	5256-1	† MMI		
1024x12	200 nsR	CMOS	TS	18	10	IM6312AI	Intersil		
	220 nsR	CMOS	TS	18	5	IM6312AM	† Intersil		
	350 nsF	CMOS	TS	18	5	HM6322-9	Harris		
	400 nsF	CMOS	TS	18	5	HM6322-2	† Harris		
	500 nsF	CMOS	TS	18	5	HM6322C-9	Harris		100
	510 nsF	CMOS	TS	18	5	IM6312-1I	Intersil		
	560 nsF	CMOS	TS	18	5	IM6312-1M	† Intersil		
	640 nsF	CMOS	TS	18	5	IM6312I	Intersil		
						IM6312M	† Intersil		
2048x4	60 nsF	NMOS	TS	24	5	72HM185C	Intersil		
						82HM185M	† Intersil		
2048x8	—	NMOS	—	16	5	SPR-16	GI		
	45 nsF	TTL	TS	22	5	MB7136H	Fujitsu		
	55 nsF	TTL	TS	22	5	MB7136E	Fujitsu		
				24	5	**MB7138E-W**	**Fujitsu**	**(3679)**	110
	80 nsF	NMOS	TS	24	5	82HM191C	Intersil		
						SY2316A	**Synertek**	**(3949)**	
						SY3316	**Synertek**	**(3954)**	
	100 nsF	NMOS	TS	24	5	82HM191M	† Intersil		
						SYM3316	**† Synertek**	**(432)**	
						SYM3316A	**† Synertek**	**(432)**	
	110 nsF	TTL	OC	24	5	6275-1	MMI		
			TS	24	5	6276-1	MMI		
	120 nsF	TTL	OC	24	5	5275-1	† MMI		
			TS	24	5	5276-1	† MMI		120
	150 ns *	I^2L	OC/TTL						
				24	5	SBP9818C	TI		
						SBP9818M	† TI		

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

MEMORY-ROMs (Cont'd)

Static (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source		Line
2048x8								(Cont'd)	
	150 nsF	CMOS	TS	24	10	**CDP1835**	**†RCA**	**(3876)**	
	200 nsF	NMOS	TS	24	5	**SY2316B-2**	**Synertek**	**(3949)**	
	250 nsF	NMOS	TS	24	5	2616A-25	Signetics		
	300 nsF	CMOS	TS	24	5	G5316	GTE Micro		
						CDP1835C	**†RCA**	**(3876)**	
		HMOS	TS	24	5	IM7332C	Intersil		
		NMOS	TS	24	5	2316-3	GTE Micro		
						2616-30	Signetics		
						SY2316B-3	**Synertek**	**(3949)**	
	350 ns *	CMOS	TS	24	5	IM6316I	Intersil		10
						IM6316M	† Intersil		
		I²L	OC/TTL						
				24	5	SBP8316C	TI		
						SBP8316M	† TI		
	350 nsF	NMOS	TS	24	5	9218C	AMD		
						AM8316EC	AMD		
						MPS23316A	CSG		
						F3516-35	Fairchild		
						F68316	**Fairchild**	**(1281)**	
						R03-9316C	GI		
						MK34000-3	Mostek		20
						MCM68A316A	**Motorola**	**(3840)**	
						MCM68A316E	**Motorola**	**(3840)**	
						MCM68A316EP91	Motorola		
						μPD2316E-5	NEC-EA		
						μPD8316E-5	NEC-EA		
						2616-35	Signetics		
	430 nsF	CMOS	—	18	5	**MCM65516-43**	**Motorola**	**(3840)**	
	450 nsF	CMOS	TS	24	5	CM1600-1	Supertex		
		NMOS	TS	24	5	9217BC	AMD		
						9217BM	† AMD		30
						9218BC	AMD		
						9218BM	† AMD		
						AM8316EB	AMD		
						S6831B	AMI		
						S68A316	**AMI**	**(3611)**	
						S68B316	AMI		
						MPS2316	CSG		
						F3516-45	Fairchild		
						R03-9316B	GI		
						2316-4	GTE Micro		40
						MK34000-84	† Mostek		
						MM52116	National		
						μPD2316E	NEC-EA		
						μPD8316E	NEC-EA		
						MSM2916	**OKI**	**(3873)**	
						R2316B	Rockwell		
						R2316E	Rockwell		
						M2316	SGS		
						2616-45	Signetics		
						SY2316B	**Synertek**	**(3949)**	50
						TMM331A	Toshiba		
						TMM334	Toshiba		
						TSU2316E	Toshiba		
	550 nsF	CMOS	—	18	5	**MCM65516-55**	**Motorola**	**(3840)**	
			TS	24	5	CM1600	Supertex		
		NMOS	TS	24	5	9217AC	AMD		
						9217AM	† AMD		
	600 nsF	CMOS	TS	24	5	SCM23C16	SSS		
						SCM23C17	SSS		
	800 nsF	CMOS	TS	24	5	CM1600-2	Supertex		60
						MM1600	† Supertex		

(Continued)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source		Line
2048x8								(Cont'd)	
	850 nsF	NMOS	TS	24	5	R03-9316A	GI		
	1000 nsF								
		CMOS	TS	24	5	883/23C16	† SSS		
						883/23C17	† SSS		
2048x10	500 nsF	NMOS	TS	40	5	R03-9502	GI		
4096x4	45 nsF	TTL	TS	20	5	**MB7134H**	**Fujitsu**	**(3679)**	
	55 nsF	TTL	TS	20	5	**MB7134E**	**Fujitsu**	**(3679)**	
4096x8	—	NMOS	TS	16	5	SPR-32	GI		
	65 nsF	TTL	TS	24	5	**MB7142E-W**	**† Fujitsu**	**(3679)**	
	200 nsF	NMOS	TS	24	5	R03-9332D	GI		70
						2064-20	Signetics		
						2632A-20	**Signetics**	**(3905)**	
						SY2332-2	**Synertek**	**(3950)**	
						SY2333-2	**Synertek**	**(3950)**	
		TTL	TS	24	5	**2332-20**	**Signetics**	**(3897)**	
	250 nsF	NMOS	TS	24	5	**2632A-25**	**Signetics**	**(3905)**	
						UM2333-25	Universal		
		TTL	TS	24	5	**2332-25**	**Signetics**	**(3897)**	
	300 nsF	CMOS	TS	24	5	SCM23C32	SSS		
						SCM23C33	SSS		80
		NMOS	TS	24	5	9232C	AMD		
						9233C	AMD		
						MP52332A	CSG		
						F3532-30	**Fairchild**	**(1282)**	
						F3533-30	**Fairchild**	**(1282)**	
						IM7332	Intersil		
						R2332-3	Rockwell		
						2632A-30	**Signetics**	**(3905)**	
						2632AE-30	**† Signetics**	**(3905)**	
						SY2332-3	**Synertek**	**(3950)**	90
						SY2333-3	**Synertek**	**(3950)**	
						VT2332A	VTI		
						VT2333A	VTI		
		TTL	TS	24	5	**2332-30**	**Signetics**	**(3897)**	
	350 nsF	NMOS	TS	24	5	**S2333**	**AMI**	**(3608)**	
						S68A332	AMI		
						MPS2332A	CSG		
						F3532-35	**Fairchild**	**(1282)**	
						F3533-35	**Fairchild**	**(1282)**	
						F68A332	Fairchild		100
						R03-9333C	GI		
						2332-3	GTE Micro		
						MCM68A332	**Motorola**	**(3840)**	
						MCM68A332P2	**Motorola**	**(3840)**	
						μPD2332A-1	NEC-EA		
						μPD2332B-1	NEC-EA		
						μPD8332A-1	NEC-EA		
						μPD8332B-1	NEC-EA		
						μPD2332-1	NEC-Micro		
						2632A-35	**Signetics**	**(3905)**	110
						2632AM-35	**† Signetics**	**(3905)**	
						TMM2332	Toshiba		
	450 nsF	CMOS	TS	24	5	TC5332	Toshiba		
						TC5333	Toshiba		
						TC5334	Toshiba		
						TC5335	Toshiba		
		NMOS	TS	24	5	9232BC	AMD		
						9232BM	† AMD		
						9233BC	AMD		
						9233BM	† AMD		120
						S68332	**AMI**	**(3612)**	
						MPS2332	CSG		
						MPS2333	CSG		
						F3532-45	**Fairchild**	**(1282)**	
						F3533-45	**Fairchild**	**(1282)**	
						R03-9332B	GI		
						R03-9333B	GI		

(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature
OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY-ROMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source		Line
Static								**(Cont'd)**	
4096x8	450 nsF	NMOS	TS	24	5			(Cont'd)	
						2332-4	GTE Micro		
						MM52132	National		
						EA8332A	NEC-EA		
						EA8332B	NEC-EA		
						μPD2332	NEC-Micro		
						MN2332	Panasonic		
						R2332	Rockwell		
						2632A-45	**Signetics**	**(3905)**	
						2632AM-45	**†Signetics**	**(3905)**	
						ROM4732	SMC		10
						SY2332	**Synertek**	**(3950)**	
						SY2333	**Synertek**	**(3950)**	
						SYM2332	**†Synertek**	**(430)**	
						SYM2333	† Synertek		
						TMS4732	TI		
						TMM333	Toshiba		
						TSU333-2	Toshiba		
						VT2332	VTI		
						VT2333	VTI		
		TTL	TS	24	5	**2332-45**	**Signetics**	**(3897)**	20
	500 nsF	NMOS	TS	24	5	**F68332**	**Fairchild**	**(1282)**	
	800 nsF	CMOS	TS	24	5	CM3200-2	Supertex		
						MM3200	† Supertex		
	850 nsF	NMOS	TS	24	5	R03-9332A	GI		
	1200 nsF								
		CMOS	TS	24	5	888/23C32	† SSS		
						888/23C34	† SSS		
	1500 nsF								
		CMOS	TS	24	5	CM3200-3	Supertex		
4096x10	300 nsF	NMOS	TS	24	5	R03-9505	GI		
8192x8	200 nsF	—	TS	28	5	**SY23128**	**Synertek**	**(3952)**	
		NMOS	TS	24	5	**MCM68364**	**Motorola**	**(3840)**	30
						μPD2364-20	NEC-EA		
						μPD8364-20	NEC-EA		
						R2364A2	Rockwell		
						2664A-20	**Signetics**	**(3907)**	
						SY2364-2	Synertek		
						SY2364A-2	Synertek		
						SY2365-2	**Synertek**	**(3951)**	
						SY2365A-2	**Synertek**	**(3951)**	
				28	5	μPD2364E	NEC-EA		
						μPD8364E	NEC-EA		40
						R2364B2	Rockwell		
						VT2365B	VTI		
						VT2366B	VTI		
		TTL	TS	28	5	**2364-20**	**Signetics**	**(3899)**	
	250 nsF	NMOS	TS	24	5	AM9264D	AMD		
						S2364	**AMI**	**(3609)**	
						S68B364	AMI		
						F3564-25	**Fairchild**	**(1282)**	
						MK36000-4	Mostek		
						MKB36000-83	† Mostek		50
						MKB37000-84	† Mostek		
						MCM68364-25	**Motorola**	**(3840)**	
						MCM68365-25	**Motorola**	**(3840)**	
						MCM68366-25	**Motorola**	**(3840)**	
						MCM68B364	Motorola		
						R2364A25	Rockwell		
						M36000	SGS		
						2664-25	**Signetics**	**(3907)**	
						2664A-25	**Signetics**	**(3907)**	
								(Continued)	

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source		Line
8192x8	250 nsF	NMOS	TS	24	5			(Cont'd)	
						ROM36000	SMC		60
						SY2364A	Synertek		
				26	5	MK37000-4	Mostek		
						MK37000-5	Mostek		
				28	5	AM9265D	AMD		
						F3565-25	**Fairchild**	**(1282)**	
						R2364B25	Rockwell		
						2364-25	**Signetics**	**(3899)**	
	300 ns *	NMOS	TS	24	5	R03-9365C	GI		
						TMM2364	Toshiba		
				28	5	**2364-30**	**Signetics**	**(3899)**	70
	300 nsF	CMOS	TS	24	5	SCM23C64	SSS		
						SCM23C65	SSS		
				28	5	G5364-3	GTE Micro		
						G5365-3	GTE Micro		
		NMOS	TS	24	5	AM9264C	AMD		
						S4264	AMI		
						MPS2364B	CSG		
						R03-9364C	GI		
						2364-3	GTE Micro		
						MK36000-5	Mostek		80
						MKB36000-84	† Mostek		
						MKB37000-85	† Mostek		
						MCM68364-30	**Motorola**	**(3840)**	
						R2364A3	Rockwell		
						2664A-30	**Signetics**	**(3907)**	
						2664AE-30	**†Signetics**	**(3907)**	
						SY2364-3	Synertek		
						SY2364A-3	Synertek		
						SY2365-3	**Synertek**	**(3951)**	
						SY2365A-3	**Synertek**	**(3951)**	90
				28	5	AM9265C	AMD		
						R2364B3	Rockwell		
						VT2365A	VTI		
						VT2366A	VTI		
	350 nsF	NMOS	TS	24	5	**S68A364**	**AMI**	**(3613)**	
						MPS2364A	CSG		
						F3564-35	**Fairchild**	**(1282)**	
						F3565-35	**Fairchild**	**(1282)**	
						2364-4	GTE Micro		
						IM7364C	Intersil		100
						MCM68365-35	**Motorola**	**(3840)**	
						MCM68366-35	**Motorola**	**(3840)**	
						MCM68A364	Motorola		
						MCM68A364P3	Motorola		
						μPD8364-35	NEC-EA		
				28	5	μPD2364-35	NEC-EA		
						2364-35	Signetics		
						2664AM-35	**†Signetics**	**(3907)**	
	450 nsF	CMOS	TS	24	5	MP2364C	Micro Pwr		
				28	5	G5364-4	GTE Micro		110
						G5365-4	GTE Micro		
		NMOS	TS	24	5	AM9264B	AMD		
						MPS2364	CSG		
						MM52164	National		
						2664A-45	**Signetics**	**(3907)**	
						2664AM-45	**†Signetics**	**(3907)**	
						SY2364	Synertek		
						SYM2364	**†Synertek**	**(431)**	
						SYM2364A	**†Synertek**	**(431)**	
						TMS4764	TI		120
				28	5	AM9265B	AMD		
								(Continued)	

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

MEMORY–ROMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage, V	Device	Source		Line
Static								**(Cont'd)**	
8192x8	450 nsF	NMOS	TS	28	5			(Cont'd)	
						R03-9364B	GI		
						R03-9365B	GI		
						μPD2364-45	NEC-EA		
						μPD8364-45	NEC-EA		
						2364-45	**Signetics**	**(3899)**	
						SY2365	**Synertek**	**(3951)**	
						SY2365A	**Synertek**	**(3951)**	
						SYM2365	**† Synertek**	**(431)**	
						SYM2365A	**† Synertek**	**(431)**	
						VT2365	VTI		10
						VT2366	VTI		
	1500 nsF	CMOS	TS	28	5	CM6400-2	Supertex		
						MM6400	† Supertex		
	2000 nsF	CMOS	TS	28	5	CM6400-3	Supertex		
16384x8	—	NMOS	TS	28	5	SPR-128	GI		
	6 μs	NMOS	TS	24	5	**S3630B**	**AMI**	**(3150)**	
	10 μs	NMOS	TS	24	5	**S3630B-1**	**AMI**	**(3150)**	
	200 nsF	NMOS	TS	5		VT23128A	VTI		
						VT23129A	VTI		
	250 nsF	CMOS	TS	28	5	SCM23C128	SSS		20
		NMOS	TS	5		VT23129	VTI		
				28	5	AM92128D	AMD		
						S23128	**AMI**	**(3610)**	
						μPD23128	NEC-EA		
						23128-25	**Signetics**	**(3901)**	
						VT23128	VTI		
	300 nsF	NMOS	TS	28	5	AM92128C	AMD		
						23128-30	**Signetics**	**(3901)**	
						SYM23128-3	† Synertek		
						SYM23128A-3	† Synertek		30
	350 nsF	NMOS	TS	28	5	**S3630A**	**AMI**	**(3150)**	
						S3630A-1	**AMI**	**(3150)**	
	450 nsF	NMOS	TS	5		VT23128B	VTI		
						VT23129B	VTI		
				28	5	AM92128B	AMD		
						32128-45	Signetics		
						SYM23128	† Synertek		
						SYM23128A	† Synertek		
	1500 nsF	CMOS	TS	28	5	CM1310	Supertex		
	5000 nsF	CMOS	TS	28	5	μPD23C128	NEC-EA		40
				52	5	μPD73128	NEC-EA		
32768x8	150 nsF	CMOS	TS	28	5	TMM23256	Toshiba		
	200 nsF	NMOS	TS	28	5	**23256A**	**Signetics**	**(3903)**	
						SY23256	**Synertek**	**(3953)**	
	250 nsF	CMOS	TS	28	5	SCM23C256	SSS		
		NMOS	TS	5		VT23256	VTI		
						VT23257	VTI		
				28	5	MK38000-25	Mostek		
						MKB38000-84	† Mostek		
						MCM65256	**Motorola**	**(3840)**	50
						μPD23256	NEC-EA		
						μPD83256	NEC-EA		
	300 nsF	NMOS	TS	28	5	MKB38000-85	† Mostek		
	450 nsF	CMOS	TS	28	5	MP2325-45	Micro Pwr		
	850 nsF	CMOS	TS	28	5	MP2325-85	Micro Pwr		
	1500 nsF	CMOS	TS	28	5	CM2560	Supertex		

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature
OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY–Shift Registers

Dynamic

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage, V	Device	Source	Line
100	2	SS	PMOS	2.0 M	±5	1406	† AMD	
						1407	† AMD	
						1506	AMD	
						1507	AMD	
256	4	SS	PMOS	5.0 M	±5	1402AC	AMD	
						1402AM	† AMD	
				10.0 M	±5	AM2802C	AMD	
						AM2802M	† AMD	
455	2	SS	CCD	20.0 M	17	CCD321	Fairchild	
512	1	SS	PMOS	2.0 M	±5	1405A	AMD	10
				3.0 M	±5	AM2805M	† AMD	
						AM2807M	† AMD	
				4.0 M	±5	AM2805C	AMD	
						AM2807C	AMD	
	2	SS	PMOS	5.0 M	±5	1403AC	AMD	
						1403AM	† AMD	
				10.0 M	±5	AM2803C	AMD	
						AM2803M	† AMD	
1024	1	SS	PMOS	3.0 M	±5	AM2806M	† AMD	
						AM2808M	† AMD	20
				4.0 M	±5	AM2806C	AMD	
						AM2808C	AMD	
				5.0 M	±5	1404AC	AMD	
						1404AM	† AMD	
				10.0 M	±5	AM2804C	AMD	
						AM2804M	† AMD	
	2	SS	NMOS	1.0 M	5	AM2401	AMD	
				2.0 M	5	9401C	AMD	
						9401M	† AMD	
			PMOS	2.0 M	−12,5	MM4025	† AMD	30
						MM4026	† AMD	
				5.0 M	−10.5,5	AM2825M	† AMD	
						AM2826M	† AMD	
				6.0 M	−10.5,5	AM2825C	AMD	
						AM2826C	AMD	
2048	1	SS	PMOS	2.0 M	−12,5	MM4027	† AMD	
				4.0 M	−10.5,5	AM2827M	† AMD	
				6.0 M	−10.5,5	AM2827C	AMD	
4096	4	PP	CCD	5.0 M	±5,12	CCD460	Fairchild	
65536	1	SS	CCD	25 M	±5,12	F464	Fairchild	40

Static

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage, V	Device	Source	Line
1-134	4	SS	NMOS	1 M	5	SR5015	SMC	
4	1	PP	Bipolar	3 M	5	SN74L95	TI	
						SN74L99	TI	
					12	375A/C	Teledyne S	
					15	375B/M	Teledyne S	
				6 M	5	DM54L95	† National	
						DM74L95	National	
				15 M	5	93L00C	Fairchild	
						93L00M	† Fairchild	
						MC8300	Motorola	50
						MC9300	† Motorola	
						N8271	Signetics	
						S8270	† Signetics	
						S8271	† Signetics	
				20 M	5	MC7270	Motorola	
						MC7271	Motorola	
						MC8270	Motorola	
						MC8271	Motorola	
						RC8270	Raytheon	
						RC8271	Raytheon	60

(Continued)

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage, V	Device	Source	Line
4	1	PP	Bipolar	20 M	5			(Cont'd)
						RM8270	† Raytheon	
						RM8271	† Raytheon	
				25 M	5	SN74LS194A	AMD	
						54178	† Fairchild	
						54179	† Fairchild	
						54194	† Fairchild	
						5495	† Fairchild	
						74178	Fairchild	
						74179	Fairchild	
						74194	Fairchild	70
						7495	Fairchild	
						ZN5495A	† Ferranti	
						ZN7495A	Ferranti	
						HD74194	Hitachi	
						HD74LS194A	Hitachi	
						MC54194	† Motorola	
						MC74194	Motorola	
						DM54194	† National	
						DM5495	† National	
						DM74194	National	80
						DM7495	National	
						54194	† Signetics	
						5495A	† Signetics	
						74194	Signetics	
						7495A	Signetics	
						74LS95B	Signetics	
						SN54178	**† TI**	**(896)**
						SN54179	**† TI**	**(897)**
						SN54194	**TI**	**(902)**
						SN5495A	**† TI**	**(866)** 90
						SN54L95	**TI**	**(866)**
						SN54L99	**† TI**	**(867)**
						SN54LS194A	**† TI**	**(902)**
						SN54LS95B	**† TI**	**(866)**
						SN74178	**TI**	**(896)**
						SN74179	**TI**	**(897)**
						SN74194	**TI**	**(902)**
						SN7495A	**TI**	**(866)**
						SN74LS194A	**TI**	**(902)**
						SN74LS95B	**TI**	**(866)** 100
				30 M	5	SN54LS195A	† AMD	
						54195	† Fairchild	
						54LS194A	Fairchild	
						54LS195A	† Fairchild	
						54LS295A	† Fairchild	
						54LS395	† Fairchild	
						54LS95B	† Fairchild	
						74195	Fairchild	
						74LS194A	Fairchild	
						74LS195A	Fairchild	110
						74LS295A	Fairchild	
						74LS395	Fairchild	
						74LS95B	Fairchild	
						9300C	Fairchild	
						9300M	† Fairchild	
						9LS194C	Fairchild	
						9LS194M	† Fairchild	
						9LS195C	Fairchild	
						9LS195M	† Fairchild	
						9LS295C	Fairchild	120
						9LS295M	† Fairchild	
						9LS395C	Fairchild	
						9LS395M	† Fairchild	
						9LS95C	Fairchild	
						9LS95M	† Fairchild	
						HD74195	Hitachi	
						HD74LS195A	Hitachi	
						MC54195	† Motorola	
						MC74195	Motorola	
						SN54LS194A	† Motorola	130

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

MEMORY–Shift Registers (Cont'd)

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage, V	Device	Source		Line
Static								**(Cont'd)**	
4	1	PP	Bipolar	30 M	5			(Cont'd)	
						SN54LS195A	† Motorola		
						SN54LS295A	† Motorola		
						SN54LS395	† Motorola		
						SN54LS95B	† Motorola		
						SN74LS194A	Motorola		
						SN74LS195A	Motorola		
						SN74LS295A	Motorola		
						SN74LS395	Motorola		
						SN74LS95B	Motorola		
						DM54195	† National		10
						DM74195	National		
						DM8300	National		
						DM9300	† National		
						T54LS395	† SGS		
						T74LS395	SGS		
						54LS195A	† Signetics		
						74195	Signetics		
						74LS195A	Signetics		
						SN54195	**† TI**	**(903)**	
						SN54LS195A	**† TI**	**(903)**	20
						SN54LS295B	**† TI**	**(925)**	
						SN54LS395A	**† TI**	**(943)**	
						SN74195	**TI**	**(903)**	
						SN74LS195A	**TI**	**(903)**	
						SN74LS295B	**TI**	**(925)**	
						SN74LS395A	**TI**	**(943)**	
				31 M	5	MC5495A	† Motorola		
						MC7495A	Motorola		
				35 M	5	AM25LS194AC	AMD		
						AM25LS194AM	† AMD		30
						MC4012	Motorola		
						MC4312	† Motorola		
				70 M	5	SN54S194	† AMD		
						SN54S195	† AMD		
						SN74S194	AMD		
						SN74S195	AMD		
						54S194	† Fairchild		
						74S194	Fairchild		
						93S00C	Fairchild		
						93S00M	† Fairchild		40
						74S194	Signetics		
						74S195	Signetics		
						SN54S194	**† TI**	**(902)**	
						SN54S195	**† TI**	**(903)**	
						SN74S194	**TI**	**(902)**	
						SN74S195	**TI**	**(903)**	
				140 M	−5.2	95H00C	Fairchild		
				150 M	−5.2	F10000C	Fairchild		
						F95000	Fairchild		
						MC10141	Motorola		50
						MC10541	† Motorola		
						10141	Signetics		
				250 M	−5.2	F10141	Fairchild		
			CMOS	2 M	3-15	F40194BM	† Fairchild		
						F40195BM	† Fairchild		
						F4035BM	† Fairchild		
						HD14035B	Hitachi		
						MC14035BC	Motorola		
						CD4035BC	National		
						MM54C195	† National		60
						CD4035BE	**RCA**	**(748)**	
						883/4035B	† SSS		
						884/4035B	† SSS		
						SCL4035B	SSS		
						CM4035AE	Solitron		
				3 M	3-15	F40194BC	Fairchild		
								(Continued)	

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage, V	Device	Source		Line
4	1	PP	CMOS	3 M	3-15			(Cont'd)	
						F40195BC	Fairchild		
						F4035BC	Fairchild		
						MC14035BA	† Motorola		
						CD4035BM	† National		70
						MM74C195	National		
						CD4035B	**† RCA**	**(748)**	
						CM4035A	† Solitron		
				4.5 M	3-15	MC14194BA	† Motorola		
				6.5 M	3-15	MM54C95	† National		
						MM74C95	National		
		PS	Bipolar	10 M	5	5494	† Fairchild		
						7494	Fairchild		
						ZN5494	† Ferranti		
						ZN7494	Ferranti		80
						MC5494	† Motorola		
						MC7494	Motorola		
						5494	Signetics		
						7494	Signetics		
						SN5494	**† TI**	**(865)**	
						SN7494	**TI**	**(865)**	
		SP		325 M	−5.2	MC1694	† Motorola		
		SS		0.5 M	15	MC686	Motorola		
	2	SP	CMOS	1 M	5	CM4015AE	Solitron		
				1.5 M	5	CM4015A	† Solitron		90
				2.5 M	3-15	F4015BC	Fairchild		
						HD14015B	Hitachi		
						MC14015BC	Motorola		
						CD4015A	National		
						CD4015BE	**RCA**	**(748)**	
				3 M	3-15	F4015BM	† Fairchild		
						CD4015B	**† RCA**	**(748)**	
						883/4015B	† SSS		
						SCL4015B	SSS		
					3-18	MC14015BA	† Motorola		100
5	1	PP	Bipolar	10 M	5	5496	† Fairchild		
						7496	Fairchild		
						ZN5496	† Ferranti		
						ZN7496	Ferranti		
						HD7496	Hitachi		
						MC5496	† Motorola		
						MC7496	Motorola		
						DM5496	† National		
						DM7496	National		
						5496	† Signetics		110
						54LS96	Signetics		
						7496	Signetics		
						74LS96	Signetics		
						SN5496	**† TI**	**(866)**	
						SN7496	**TI**	**(866)**	
				25	5	**SN54LS96**	**† TI**	**(866)**	
						SN74LS96	**TI**	**(866)**	
	4	SS	CMOS	1.5 M	5	CM4006AD	† Solitron		
				2 M	3-15	F4006BC	Fairchild		
						CD4006BE	**RCA**	**(748)**	120
						CM4006A	† Solitron		
						CM4006AE	Solitron		
				2.5 M	3-15	F4006M	† Fairchild		
						CD4006A	National		
				3 M	3-15	883/4006B	† SSS		
						SCL4006B	SSS		
				4 M	5-15	MC14006BC	Motorola		
				7 M	5-15	MC14006BA	† Motorola		
8	1	PP	Bipolar	15 M	5	DM7546	† National		
						DM8546	National		130
				25 M	5	**SN54LS299**	**† AMD**	**(1227)**	
								(Continued)	

† Military Temperature Range (−55° to 125°C)
* Typical Values

SS = Serial In, Serial Out

PP = Parallel In, Parallel Out

MEMORY–Shift Registers (Cont'd)

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage, V	Device	Source		Line
Static						**(Cont'd)**			
8	1	PP	Bipolar	25 M	5			(Cont'd)	
						SN74LS299	**AMD**	**(1227)**	
						54198	† Fairchild		
						54199	† Fairchild		
						74198	Fairchild		
						74199	Fairchild		
						HD74198	Hitachi		
						HD74199	Hitachi		
						DM54198	† National		
						DM54199	† National		
						DM74198	National		10
						DM74199	National		
						74199	Signetics		
						SN54198	**†TI**	**(904)**	
						SN54199	**†TI**	**(905)**	
						SN74198	**TI**	**(904)**	
						SN74199	**†TI**	**(905)**	
				30 M	5	AM24LS299C	AMD		
						AM25LS299M	**†AMD**	**(1227)**	
				35 M	5	AM24LS23M	† AMD		
						AM25LS23C	**AMD**	**(1227)**	20
						SN54LS323	† AMD		
						SN74LS323	AMD		
						54LS299	† Fairchild		
						54LS323	† Fairchild		
						74LS299	Fairchild		
						74LS323	Fairchild		
						SN54LS299	**†TI**	**(927)**	
						SN54LS323	**†TI**	**(930)**	
						SN64LS299	TI		
						SN74LS323	**TI**	**(930)**	30
				50 M	5	**SN54S299**	**†TI**	**(927)**	
						SN74S299	**TI**	**(927)**	
			CMOS	2.5 M	3-15	SCL4034B	SSS		
					3-18	MC14034BC	Motorola		
					5	CM4034AE	Solitron		
				3 M	3-15	CD4034BC	National		
						CD4034BM	National		
						CD4034B	**†RCA**	**(748)**	
						883/4034B	† SSS		
						TC4034	Toshiba		40
					3-18	HD14034B	Hitachi		
						MC14034BA	Motorola		
					5	CM4034A	† Solitron		
		PS	Bipolar	14 M	5	DM7590	† National		
						DM8590	National		
				20 M	5	54165	† Fairchild		
						74165	Fairchild		
						MC54165	† Motorola		
						MC74165	Motorola		
						DM54165	† National		50
						DM74165	National		
						54165	† Signetics		
						74165	Signetics		
						SN54165	**†TI**	**(891)**	
						SN74165	**TI**	**(891)**	
				25 M	5	54166	† Fairchild		
						54LS165	† Fairchild		
						74166	Fairchild		
						74LS165	Fairchild		
						HD74166	Hitachi		60
						SN54LS165	† Motorola		
						SN74LS165	Motorola		
						DM54166	† National		
						DM74166	National		
						54166	† Signetics		
						74166	Signetics		
								(Continued)	
8	1	PS	Bipolar	25 M	5			(Cont'd)	
						SN54166	**†TI**	**(891)**	
						SN54LS165	**†TI**	**(891)**	
						SN54LS166	**†TI**	**(891)**	
						SN74166	**TI**	**(891)**	70
						SN74LS165	**TI**	**(891)**	
						SN74LS166	**TI**	**(891)**	
			CMOS	1 M	3-15	F4014BC	Fairchild		
						F4021BC	Fairchild		
				2.5 M	3-15	HD14021B	Hitachi		
						MC14021BC	Motorola		
						CD4014A	National		
						CD4021A	National		
						CD4014BE	**RCA**	**(748)**	
						CD4021BE	**RCA**	**(748)**	80
						SCL4014B	SSS		
						SCL4021B	SSS		
						CM4018AE	Solitron		
						CM4021AE	Solitron		
				3 M	3-15	F4014BM	† Fairchild		
						F4021BM	† Fairchild		
						MC14014BA	† Motorola		
						MC14021BA	† Motorola		
						CD4014B	**†RCA**	**(748)**	
						CD4021B	**†RCA**	**(748)**	90
						883/4014B	† SSS		
						883/4021B	† SSS		
						CM4014A	† Solitron		
						CM4021A	† Solitron		
				5 M	3-15	MM54C165	† National		
						MM74C165	National		
		SP	Bipolar	6 M	5	DM54L164A	† National		
						DM74L164A	National		
				12 M	5	**SN54L164**	**†TI**	**(891)**	
						SN74L164	TI		100
				25 M	5	SN54LS164	† AMD		
						54164	† Fairchild		
						54LS164	† Fairchild		
						74164	Fairchild		
						74LS164	Fairchild		
						ZN54164	† Ferranti		
						ZN74164	Ferranti		
						HD74164	Hitachi		
						HD74LS164	Hitachi		
						SN54LS164	† Motorola		110
						SN74LS164	Motorola		
						DM54164	† National		
						DM54LS164	† National		
						DM74164	National		
						DM74LS164	National		
						DM7570	† National		
						DM8570	National		
						54164	† Signetics		
						54LS164	† Signetics		
						74164	Signetics		120
						74LS164	Signetics		
						SN54164	**†TI**	**(891)**	
						SN54LS164	**†TI**	**(891)**	
						SN74164	**TI**	**(891)**	
						SN74LS164	**TI**	**(891)**	
						TD3503	Toshiba		
				35 M	5	AM25LS164C	AMD		
						AM25LS164M	† AMD		
				350 M	−5.2	F10041	Fairchild		
			CMOS	5.5 M	3-15	MM54C164	† National		130
						MM74C164	National		
		SS	Bipolar	3 M	5	**SN54L91**	**†TI**	**(864)**	
						SN74L91	TI		
								(Continued)	

† Military Temperature Range (−55° to 125°C)

* Typical Value

Bold face indicates additional data is provided on the page noted.

MEMORY–Shift Registers (Cont'd)

Static (Cont'd)

Bits Per Register	No. of Reg.	Oper-ation	Process	Frequency (Hz - Spec)	Supply Voltage, V	Device	Source		Line
								(Cont'd)	
8	1	SS	Bipolar	4 M	5	DM54L91	† National		
						DM74L91	National		
				10 M	5	5491	† Fairchild		
						7491	Fairchild		
						ZN5491A	† Ferranti		
						ZN7491	Ferranti		
						MC5491A	† Motorola		
						MC7491A	Motorola		
						SN5491A	† National		
						SN7491A	National		10
						5491	† Signetics		
						7491	Signetics		
						SN5491A	**† TI**	**(864)**	
						SN54LS91	**† TI**	**(864)**	
						SN7491A	**TI**	**(864)**	
						SN74LS91	**TI**	**(864)**	
			CMOS	2.5 M	3-15	MC14094BA	† Motorola		
						MC14094BC	Motorola		
						CD4094B	**† RCA**	**(748)**	
						CD4094BE	**RCA**	**(748)**	20
						883/4094B	† SSS		
						SCL4094B	SSS		
						TC4094B	Toshiba		
	2	SS	Bipolar	10 M	5	93L28C	Fairchild		
						93L28M	† Fairchild		
						MC8328	Motorola		
						MC9328	† Motorola		
				15 M	5	RC8277	Raytheon		
						RM8277	† Raytheon		
						N8277	Signetics		30
				20 M	5	9328C	Fairchild		
						9328M	† Fairchild		
10	1	PP	Bipolar	25 M	5	RC8274	Raytheon		
						RM8274	† Raytheon		
						S8274	† Signetics		
		SP	Bipolar	25 M	5	RC8273	Raytheon		
						RM8273	† Raytheon		
						N8273	Signetics		
16	1	SP	NMOS	3.0M	5	**TSC9403**	**Teledyne S**	**(2854)**	
						TSC9404	**Teledyne S**	**(2854)**	40
16-128	1	SS	CMOS	1.5 M	3-15	MC14562BC	Motorola		
				3 M	3-15	MC14562BA	† Motorola		
30	1	SS	CMOS	1 M	3-15	MD4330B	Mitel		
32	6	SS	PMOS	1 M	– 12,5	3348	Fairchild		
						3349	Fairchild		
64	1	SS	CMOS	1 M	3-15	F4031BC	Fairchild		
						CD4031BE	**RCA**	**(748)**	
				2 M	3-15	F4031BM	† Fairchild		
						CD4031B	**† RCA**	**(748)**	
				2.7 M	3-15	F4557BM	† Fairchild		50
					3-16	MC1455BC	Motorola		
				4 M	3-15	CD4031BC	National		
						CD4031BM	† National		
				5 M	3-15	F4557BC	Fairchild		
					3-18	MC14557BA	† Motorola		
				10 M	3-16	MS612	RTC		
	2	SS	CMOS	4 M	3-15	MC14517BC	Motorola		
						CD4517BE	**† RCA**	**(749)**	
						SCL4517B	SSS		
				5 M	3-15	MC14517BA	† Motorola		60
						CD4517BE	† RCA		
						883/4517B	† SSS		
			TTL	30 M	5	**TDC1005**	**† TRW**	**(813)**	
						TDC1005	TRW		

(Continued)

Bits Per Register	No. of Reg.	Oper-ation	Process	Frequency (Hz - Spec)	Supply Voltage, V	Device	Source		Line
								(Cont'd)	
64	4	SS	CMOS	4 M	4.5-12.5	F4731BC	Fairchild		
						F4731BM	† Fairchild		
			PMOS	1.5 M	– 12,5	3342	Fairchild		
80	4	SS	NMOS	1 M	5	SR5015-80	SMC		
				3 M	5	M142	SGS		
						M142A	SGS		70
			PMOS	1.5 M	– 12,5	3347	AMD		
						3347	Fairchild		
				2 M	– 12,5	3357-2	Fairchild		
				2.5 M	– 12,5	AM2847M	† AMD		
						F2847LM	† Fairchild		
						F2847M	† Fairchild		
				3 M	– 12,5	AM2847C	AMD		
						F2847	Fairchild		
						F2847L	Fairchild		
				4 M	– 12,5	3357-1	Fairchild		80
						F3357M	† Fairchild		
81	4	SS	NMOS	1 M	5	SR5015-81	SMC		
						SR5018	SMC		
96	4	SS	PMOS	2.5 M	– 12,5	AM2896M	† AMD		
				3 M	– 12,5	AM2896C	AMD		
128	1	SS	CMOS	5 M	12	MS625	RTC		
	2	SS	PMOS	1 M	– 12,5	MK1002	AMD		
				2 M	– 12,5	AM2809M	† AMD		
						AM2810C	AMD		
						AM2810M	† AMD		90
						TMS3114	AMD		
				2.5 M	– 12,5	AM2809C	AMD		
						AM2814C	AMD		
						AM2814M	† AMD		
	4	SS	PMOS	2.5 M	– 12,5	AM2855	AMD		
						AM4055	† AMD		
						AM5055	AMD		
133	4	SS	NMOS	1 M	5	SR5015-133	SMC		
				1 M	5	SR5017	SMC		
256	1	SS	TTL	30 M	5	**TDC1006**	**† TRW**	**(813)**	100
						TDC1006	TRW		
	2	SS	PMOS	2.5 M	– 12,5	AM2856	AMD		
						AM4056	† AMD		
						AM5056	AMD		
512	1	SS	PMOS	2.5 M	– 12,5	AM2857C	AMD		
						AM4057	† AMD		
						AM5057	AMD		
1024	1	SS	PMOS	1.5 M	– 12,5	AM2533	AMD		
				2 M	– 12,5	AM2833C	AMD		
						AM2833M	† AMD		110
92304	1	SS	Bubble	0.1 M	—	TIB0203S	TI		
290560	1	SS	Bubble		—	H4701B	Hitachi		

† Military Temperature Range (– 55° to 125°C)
* Typical Values

SS = Serial In, Serial Out

PP = Parallel In, Parallel Out

ABBREVIATIONS OF COMPANY NAMES

Action Ins	Action Instruments
AD	Analog Devices
ADT	Advanced Digital Technology
Adapt Sci	Adaptive Science Corp.
Advent	Advent Products, Inc.
Alphatron	Alphatron
AMA	American Automation
AMD	Advanced Micro Devices
AMI	American Microsystems, Inc.
Amperex	Amperex Electronic Corp.
Analogic	Analogic
Analog Sys	Analog Systems
APC	Applied Micro Circuits
Apex	Apex Microtechnology
APM	Applied Microsystems Corp.
Appl Sys	Applied Systems Corp.
APT	Applied Microtechnology
Aptek	Aptek Microsystems
Array Tech	Array Technology
AWI	Analog West
Bedford	Bedford Computer Systems Inc.
Burr-Brown	Burr-Brown Research
CAE	Computer Aided Engineering
Cal Devices	California Devices
Cent Data	Central Data Corp.
Cermetek	Cermetek
CGRS	CGRS Microtech Inc.
Cherry	Cherry Semiconductor
CIC	Custom Integrated Circuits
Citel	Citel, Inc.
Comlinear	Comlinear Corporation
CMA	Custom MOS Arrays
Comark	Comark Corp.
Comdial	Comdial Semiconductor
Comp Auto	Computer Automation
Compas	Compas Microsystems
Cont Logic	Control Logic Inc.
Control Sys	Control Systems Microsystems Div.
CreMicro	Creative Micro Systems
Cromemco	Cromemco, Inc.
CSG	Commodore Semiconductor Group
Cubit	Cubit Inc.
Curtis	Curtis Electro Devices, Inc.
Cybernetic	Cybernetic Micro Systems
Cybersys	Cybersystems
Cybertek	Cybertek Inc.
Data General	Data General
Data I/O	Data I/O
Data Trans	Data Translation
Datel	Datel-Intersil
Datricon	Datricon Corporation
DDC	Data Devices Corporation
DEC	Digital Equipment Corporation
Delco	Delco Electronics
DGM	Digital Microsystems
Digelec	Digelec Corp.
Digitek	Digitek, Inc.
Dionics	Dionics Inc.
Dist Comp	Distributed Computer Systems
Divers Tech	Diversified Technology
E-H	E-H International, Inc.
Elind	Elind Elettronica Industriale
EL Instr	E & L Instruments
EMM	EMM
Emulogic	Emulogic Inc.
Epson	Epson America, Inc.
ETI Micro	ETI Micro
Exar	Exar Integrated Systems
Fairchild	Fairchild
Ferranti	Ferranti Electric
Fujitsu A	Fujitsu America
Fujitsu	Fujitsu Microelectronics, Inc.
GI	General Instrument
GMS	General Microsystems
GTE Micro	GTE Microcircuits
Harris	Harris Semiconductor
Heurikon	Heurikon Corp.
Hilevel	Hilevel Technology, Inc.
Hitachi	Hitachi America, Ltd.
Holt	Holt Inc.
HP	Hewlett-Packard
Hughes	Hughes Aircraft, Solid State Products
Hybrid Sys	Hybrid Systems
Hycom	Hycom Incorporated
IDT	Integrated Device Technology
IMI	International Microcircuits, Inc.
IMP	International Microelectronic Products
IMS	Industrial Micro-systems Inc.
Inconix	Inconix Corporation
Ind Tech	Inductive Technology
Inmos	Inmos
IntCirEng	Integrated Circuit Engineering
IntCirSys	Integrated Circuit Systems
IntCompSys	Integrated Computer Systems
IntCyber	International Cybernetics
Int Micro	International Microsystems
Int Tech	Integrated Technology Corp.
Intech/FMI	Intech/Function Modules Inc.
Intel	Intel
Interdesign	Interdesign
Intersil	Intersil
Intronics	Intronics
IPI	Integrated Photomatrix Inc.
ITT	ITT Semiconductors
Kinetic Sys	Kinetic Systems
Kontron	Kontron Electronics
Lambda	Lambda Semiconductor
Laserdyne	Laserdyne
LSI Comp	LSI Computer Systems
LSI Logic	LSI Logic Corporation
Master Logic	Master Logic Corporation
Matrix	Matrix Corp.
Matrox	Matrox Electronic Systems
MCC	Microcomputer Control
Micrel	Micrel
Micro Eng	Micro Circuit Engineering
Micro Innov	Micro Innovators
Micropac	Micropac Industries
Micro Net	Micro Networks
Micro Pwr	Micro Power Systems
Micro Sci	Micro Sciences Corp.
Micro Tech	Microcircuits Technology
Micro-Link	Micro-Link Corporation
Micron	Micron Technology
MilerTron	MilerTronics
Miller	Miller Technology
Mitel	Mitel Semiconductor
Mitsubishi	Mitsubishi Electronics
MMI	Monolithic Memories, Inc.
Monosil	Monosil
MonSys	Monolithic Systems Corp.
Mostek	Mostek
Motorola	Motorola Semiconductor
MRC	MRC Systems
Murray	Murray Consulting
National	National Semiconductor
NCR	NCR Corp., Microelectronics Division
NEC-EA	NEC/Electronic Arrays Division
NEC Electron	NEC/Electron Division
NEC Micro	NEC/Microcomputer Division
Nitron	Nitron
Nortek	Nortek
OAE	Oliver Advanced Engineering
Octagon	Octagon Systems Corp.
OEI	Optical Electronics Inc.
Ohio Sci	Ohio Scientific
OKI	OKI Semiconductor
Omnibyte	Omnibyte Corp.
Oscar	I. S. Oscar Assoc.
Panasonic	Panasonic
PC/M	Pacific/Cyber Metrix
Percom	Percom Data Co.
Phoenix	Phoenix Digital Corp.
Pico Design	Pico Design
Polycore	Polycore Electronics
Plessey	Plessy Semiconductors
PMI	Precision Monolithics, Inc.
PragDes	Pragmatic Design Inc.
PREMA	PREMA GmbH
Pro-Log	Pro-Log Corp.
Quay	Quay Corp.
Raytheon	Raytheon Semiconductor
RCA	RCA Solid State Division
RCI Data	RCI Data
RELMS	Relational Memory Systems
Reticon	Reticon
RIFA	RFIA
Rockwell	Rockwell, Microelectronic Devices
RTC	Riehl Time Corporation
Sanken	Sanken Electric
Sanyo	Sanyo
SEEQ	SEEQ Technology, Inc.
Semi Proc	Semi Processes
Siemens	Siemens
Signetics	Signetics
SGS	SGS-ATES Semiconductor
Sharp	Sharp
Silicon G	Silicon General
Siliconix	Siliconix
Silicon Sys	Silicon Systems Inc.
Siltronics	Siltronics
SMC	Standard Microsystems Corp.
Solarise	Solarise Enterprises
Solitron	Solitron Devices
Sprague	Sprague Electric Company
SSM	Solid State Micro Technology for Music
SSS	Solid State Scientific
Stag	Stag Microsystems
Struc. Des.	Structured Design inc.
Stynetic	Stynetic Systems
Sunrise	Sunrise Electronics
Sunshine	Sunshine Semiconductor
Supertex	Supertex Inc.
Symtek	Symtek Corp.
Synapse	Synapse Corp.
Synertek	Synertek
Sys Innov	Systems Innovations
Tau Zero	Tau Zero Inc.
Tektronix	Tektronix
Telaris	(See Laserdyne)
Teledyne C	Teledyne Crystalonics
Teledyne P	Teledyne Philbrick
Teledyne S	Teledyne Semiconductor
Telefunken	Telefunken
Telephonics	Telephonics LSI
Telmos	Telmos
Teltone	Teltone Corporation
TI	Texas Instruments
Thomson-CSF	Thompson-CSF Components Corp.
TMX	TMX
Topanga	Topanga Data Systems
Toshiba	Toshiba America
Trans-Data	Trans-Data
TRW	TRW-LSI Products
Unitrode	Unitrode
Universal	Universal Semiconductor, Inc.
Vantage	Vantage Data Products
VTI	VLSI Technology, Inc.
Votrax	Votrax
Weitek	Weitek Corporation
Western	Western Digital
Wintek	Wintek Corp.
Xicor	Xicor, Inc.
Xycom	Xycom
Zendex	Zendex Corp.
Zilog	Zilog
Zymos	Zymos Corporation

Advanced Micro Devices

MOS MEMORY
Am9128

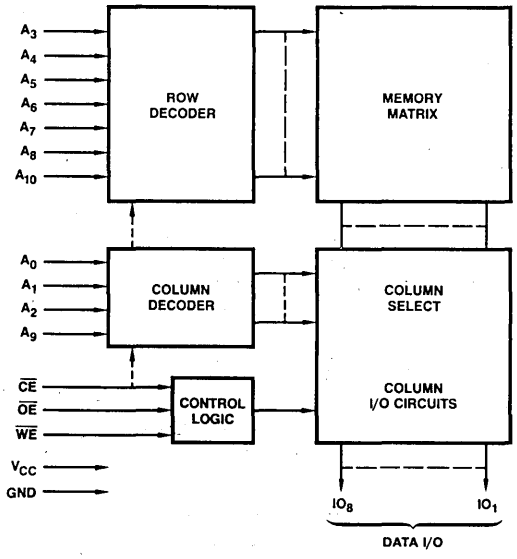
Am9128
2048 x 8 Static R/W Random Access Memory

- 2,048 x 8-bit organization
- Standard 24-pin, 0.6″ wide DIP package
- Logic voltage levels compatible with TTL
- Three-state output buffers-common I/O
- Fully static; no clocks or refresh required
- Single +5V power supply ±10% tolerance
- MIL-STD-883 reliability assurance testing
- I_{CC} max down to 100mA
- T_{AA}/T_{ACS} down to 70ns
- Power down mode (I_{CC} standby max down to 15mA)
- Commercial and full military temperature ranges
- Guaranteed 0.1% AQL

GENERAL DESCRIPTION

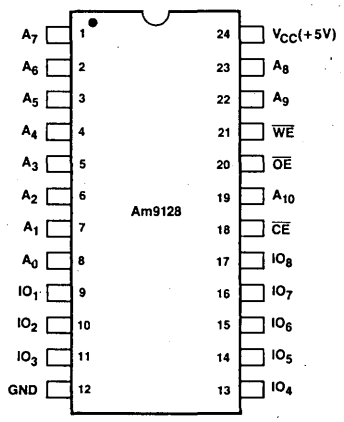
The Am9128 is a 16,384-bit static Random Access Read-write Memory organized as 2048 words of 8 bits. It uses fully static circuitry, requiring no clocks or refresh to operate. Directly TTL-compatible inputs and outputs and operation from a single +5V supply simplify system designs. Common data I/O pins using three-state outputs are provided. The Am9128 is available in an industry-standard 24-pin DIP package with 0.6-inch pin row spacing. The Am9128 uses the JEDEC standard pinout for byte-wide memories (compatible to 16K EPROM's).

BLOCK DIAGRAM



RAM-025

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

RAM-026

PRODUCT SELECTIONS

Part Number		Am9128-70	Am9128-10	Am9128-15	Am9128-20
Maximum Access Time (ns)		70	100	150	200
Maximum Operating Current (mA)	0° to 70°C	140	120	100	140
	−55° to 125°C	N/A	N/A	150	150
Maximum Standby Current (mA)	0° to 70°C	30	15	15	30
	−55° to 125°C	N/A	N/A	30	30

MOS MEMORY
Am9128

MAXIMUM RATINGS beyond which useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
V_{CC} with Respect to V_{SS}	−0.5V to +7.0V
All Signal Voltages with Respect to V_{SS}	−3.0V to +7.0V
Power Dissipation (Package Limitation)	1.0W
DC Output Current	10mA

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Part Number	Ambient Temperature	V_{SS}	V_{CC}
Am9128-10DC/PC Am9128-15DC/PC Am9128-20DC/PC Am9128-70DC/PC	$0°C \leq T_A \leq +70°C$	0V	+5.0V ± 10%
Am9128-15DM Am9128-20DM	$-55°C \leq T_A \leq +125°C$	0V	+5V ± 10%

ELECTRICAL CHARACTERISTICS over operating range (Note 3)

Parameter	Description	Test Conditions		Am9128-10 Min	Am9128-10 Max	Am9128-15 Min	Am9128-15 Max	Am9128-70 Am9128-20 Min	Am9128-70 Am9128-20 Max	Units
I_{OH}	Output HIGH Current	V_{OH} = 2.4V	V_{CC} = 4.5V	−2		−2		−2		mA
I_{OL}	Output LOW Current	V_{OL} = 0.4V		4		4		4		mA
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 1.0	2.0	V_{CC} + 1.0	2.0	V_{CC} + 1.0	Volts
V_{IL}	Input LOW Voltage			−0.5	0.8	−0.5	0.8	−0.5	0.8	Volts
I_{IX}	Input Load Current	$V_{SS} \leq V_I \leq V_{CC}$			10		10		10	μA
I_{OZ}	Output Leakage Current	GND ≤ $V_O \leq V_{CC}$ Output Disabled			10		10		10	μA
C_I	Input Capacitance	Test Frequency = 1.0MHz T_A = 25°C, All pins at 0V	V_{CC} = 5.0V		6		6		6	pF
$C_{I/O}$	Input/Output Capacitance				7		7		7	
I_{CC}	V_{CC} Operating Supply Current	Max V_{CC}, $\overline{CE} \leq V_{IL}$ Outputs Open	T_A = −55°C to +125°C		N/A		150		150 (Note 11)	mA
			T_A = 0°C to +70°C		120		100		140	
I_{SB}	Automatic $\overline{CE}$ Power Down Current	Max V_{CC}, $\overline{CE} \geq V_{IH}$	T_A = −55°C to +125°C		N/A		30		30 (Note 11)	mA
			T_A = 0°C to 70°C		15		15		30	
I_{PO}	Peak Power On Current	V_{CC} = GND to V_{CC} Max $\overline{CE} \geq V_{IH}$ (Note 2)	T_A = −55°C to +125°C		N/A		30		30 (Note 11)	mA
			T_A = 0°C to 70°C		15		15		30	

Notes:
1. The internal write time of the memory is defined by the overlap of $\overline{CE}$ Low and $\overline{WE}$ Low. Both signals must be Low to initiate a write and either signal can terminate a write by going High. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
2. A pull up resistor to V_{CC} on the $\overline{CE}$ input is required during power up to keep the device deselected, otherwise I_{SB} will exceed values given.
3. The operating ambient temperature range is guaranteed with transverse air flow of 400 linear feet per minute.
4. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for all devices.
5. $\overline{WE}$ is High for read cycle.
6. Device is continuously selected, $\overline{CE} = V_{IL}$.
7. Address valid prior to or coincident with $\overline{CE}$ transition Low.
8. $\overline{OE} = V_{IL}$.
9. C_L = 100pF for Am9128-10/-15/-20. C_L = 30pF for Am9128-70.
10. Transition is measured at V_{OH} − 500mV and V_{OL} + 500mV. Levels on the output from 1.5V level on the input with load shown in Figure 1 using C_L = 5pF
11. Am9128-20 only.

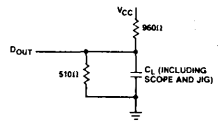
MOS MEMORY
Am9128

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Parameter	Description			Am9128-70 Min	Am9128-70 Max	Am9128-10 Min	Am9128-10 Max	Am9128-15 Min	Am9128-15 Max	Am9128-20 Min	Am9128-20 Max	Units
READ CYCLE												
t_{RC}	Read Cycle Time			70		100		150		200		ns
t_{ACC}	Address Access Time		Note 9		70		100		150		200	ns
t_{ACS}	Chip Select Access Time		Note 9		70		100		150		200	ns
t_{OE}	Output Enable Time	0°C to +70°C	Note 9		40		50		60		70	ns
		−55°C to +125°C			N/A		N/A		70		80	
t_{OH}	Output Hold Time from Address Change			10		10		10		10		ns
t_{CLZ}	Output in LOW-Z from $\overline{CE}$		Notes 4, 10	10		10		10		10		ns
t_{CHZ}	Output in HIGH-Z from $\overline{CE}$		Notes 4, 10		35		40		55		55	ns
t_{OLZ}	Output in LOW-Z from $\overline{OE}$		Notes 4, 10	5		5		5		5		ns
t_{OHZ}	Output in HIGH-Z from $\overline{OE}$		Notes 4, 10		30		35		50		50	ns
t_{PU}	Chip Selection to Power Up Time			0		0		0		0		ns
t_{PD}	Chip Deselection to Power Down Time				40		50		60		60	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time			70		100		150		200		ns
t_{CW}	Chip Selection to End of Write	0°C to +70°C	Note 1	60		90		120		150		ns
		−55°C to +125°C		N/A		N/A		130		160		
t_{AS}	Address Setup Time			5		10		20		20		ns
t_{WP}	Write Pulse Width		Note 1	60		70		100		100		ns
t_{WR}	Write Recovery Time			5		5		5		5		ns
t_{DS}	Data Setup Time			30		40		50		60		ns
t_{DH}	Data Hold Time			5		5		5		5		ns
t_{WLZ}	Output in LOW-Z from $\overline{WE}$		Notes 4, 10	5		5		5		5		ns
t_{WHZ}	Output in HIGH-Z from $\overline{WE}$		Notes 4, 10		30		35		50		50	ns
t_{AW}				65		80		120		120		ns

AC TEST CONDITIONS

Input Pulse Levels	0 to 3.0V
Input Rise and Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V

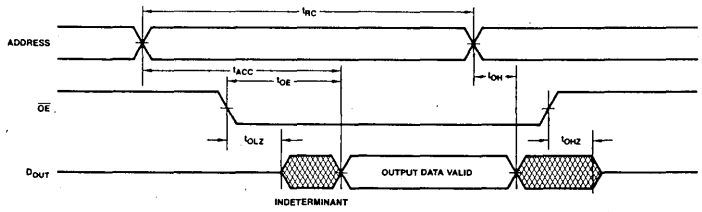


RAM-032

Figure 1. Output Load (Notes 9, 10)

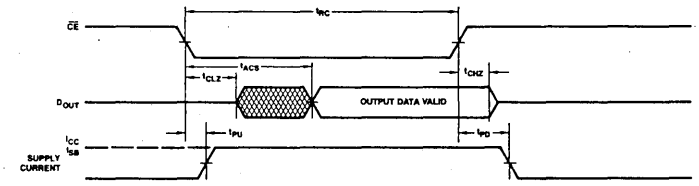
TIMING WAVEFORMS

READ CYCLE 1 (Notes 5, 6)



RAM-027

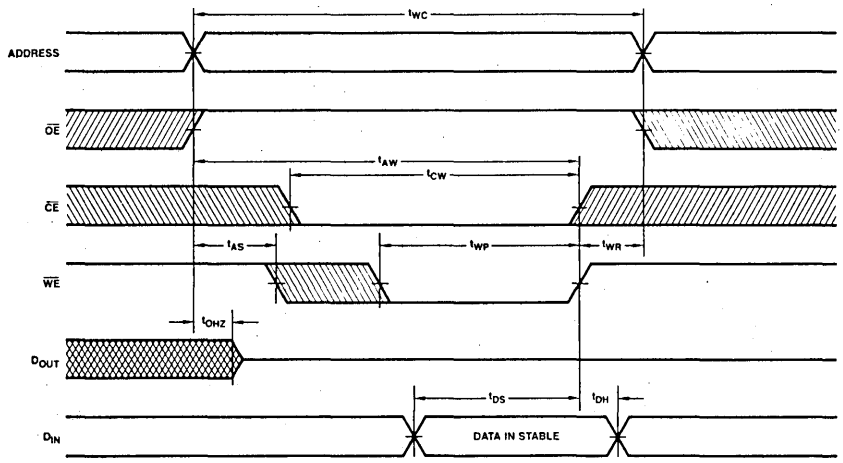
READ CYCLE 2 (Notes 5, 7, 8)



RAM-028

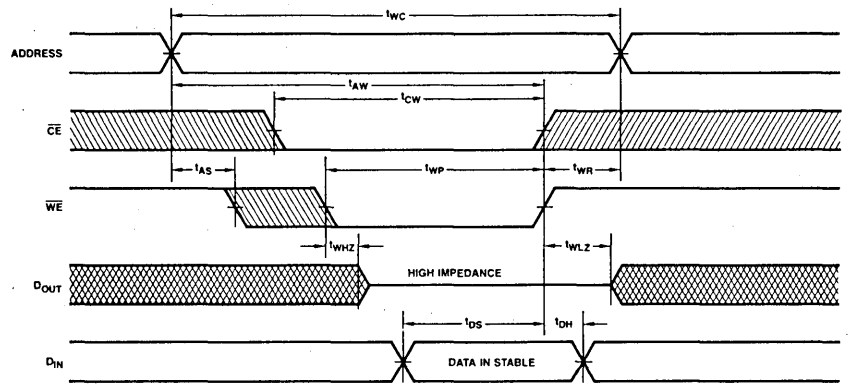
TIMING WAVEFORMS (Cont.)

WRITE CYCLE 1



RAM 029

WRITE CYCLE 2 (Notes 7, 8)



RAM-030

BIT MAP

Address Designators	
External	Internal
A_3	AX_0
A_4	AX_1
A_5	AX_2
A_6	AX_3
A_7	AX_4
A_8	AX_5
A_{10}	AX_6
A_0	AY_0
A_1	AY_1
A_2	AY_2
A_9	AY_3

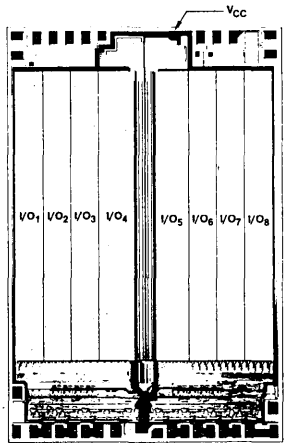
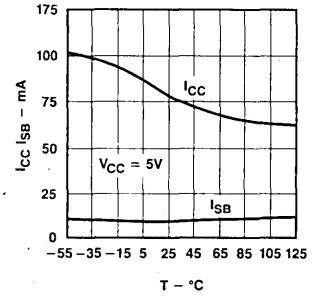


Figure 2. Bit Mapping Information

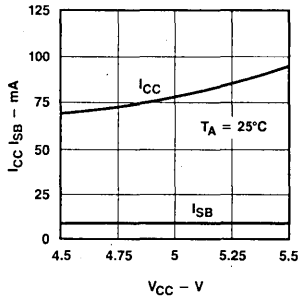
MOS MEMORY
Am9128

TYPICAL DC AND AC CHARACTERISTICS

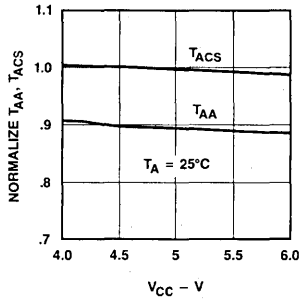
Supply Current Versus Ambient Temperature



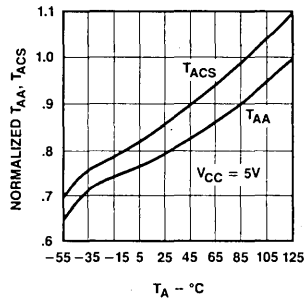
Supply Current Versus Supply Voltage



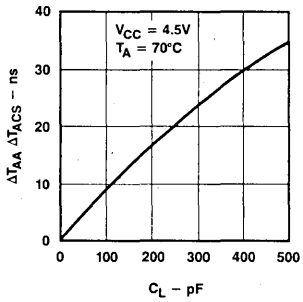
Normalized Access Time Versus Supply Voltage



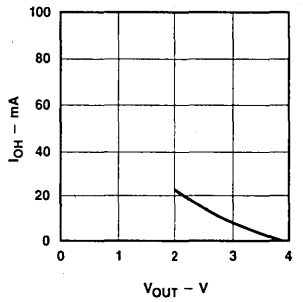
Normalized Access Time Versus Ambient Temperature



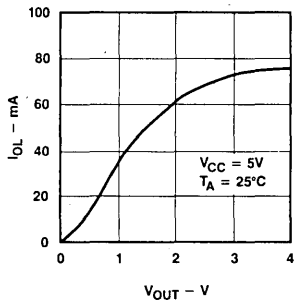
Access Time Change Versus Output Loading



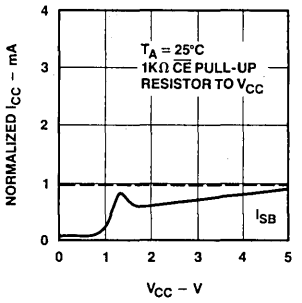
Output Source Current Versus Output Voltage



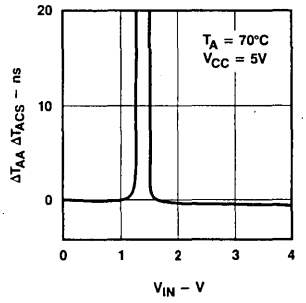
Output Sink Current Versus Output Voltage



Typical Power-On Current Versus Power Supply



Access Time Change Versus Input Voltage



RAM-031

Advanced Micro Devices

MOS MEMORY
Am9128

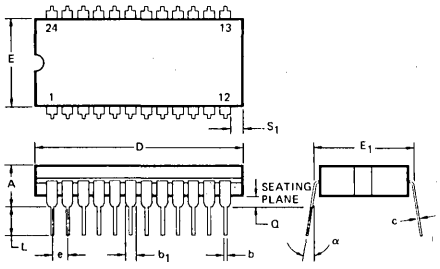
ORDERING INFORMATION

Am9128-70 Order Code	Am9128-10 Order Code	Am9128-15 Order Code	Am9128-20 Order Code	Package Type	Screening Level	Operating Range
AM9128-70PC	AM9128-10PC	AM9128-15PC	AM9128-20PC	P-24-1	C-1	C
AM9128-70DC	AM9128-10DC	AM9128-15DC	AM9128-20DC	D-24-1	C-1	C
		AM9128-15DM	AM9128-20DM	D-24-1	C-3	M
		AM9128-15DMB	AM9128-20DMB	D-24-1	B-3	M

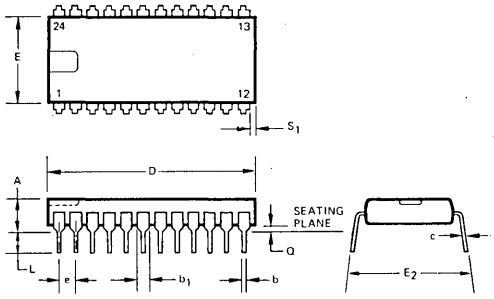
Notes: 1. P = Molded DIP, D = Hermetic DIP. Number following letter is number of leads.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
3. See operating range table.

PHYSICAL DIMENSIONS

Cerdip



Molded



Reference Symbol	Inches			
	Cerdip		Molded	
	Min	Max	Min	Max
A	.150	.225	.170	.215
b	.016	.020	.015	.020
b_1	.045	.065	.055	.065
c	.009	.011	.009	.011
D	1.230	1.285	1.240	1.270
E	.510	.545	.515	.540
E_1 or E_2	.600	.620	.585	.700
e	.090	.110	.090	.110
L	.12	.150	.125	.160
Q	.015	.060	.015	.060
S_1	.010		.035	.065
α	3°	13°		

The following table shows the various programmers and personality cards which may be used with any of Advanced Micro Devices' series of bipolar PROMs.

PROM Programming Equipment Guide

Source and Location	Data I/O 10525 Willows Rd. N.E. Redmond, WA 98052		Pro-Log Corporation 2411 Garden Road Monterey, CA 93940	International Microsystems, Inc. 11554 C. Avenue Auburn, CA 93940	Kontron Electronic, Inc. 630 Price Avenue Redwood City, CA 94063	Digelec, Inc. 7335 E. Acoma Dr. Scottsdale, AZ 85260		Stag Systems, Inc. 528-5 Weddell Dr. Sunnyvale, CA 94086
Programmer Model(s)	Model 5, 7 and 9 Systems 17, 19, 29 and 100		M900, M900B, M910, M920 and M980	IM1010	MPP-80	UPP-801	UPP-803	PPX
AMD Generic Bipolar PROM Personality Module	909-1286-1 919-1286-1 Rev H	Unipak Rev 003 (Family and Pin Code)	PM 9058	IM AMDGEN1	MOD 14	PM 102	FAM-12	PM 2000 Code 90
Socket Adapters and Configurators								
Am27S18/19 Am27LS18/19	715-1407-1	16 02	PA 16-6 and 32 x 8(L)	IM 32 x 8-16-AMD	SA 3-1 B 32 x 8/16	DIS-156 AM	DA 22	AM 110-2
Am27S20/21	715-1408-1	16 01	PA 16-5 and 256 x 4(L)	IM 256 x 4-16-AMD	SA 4-2 B 256 x 4/16	DIS-133 AM	DA 21	AM 130-2
Am27S12/13	715-1408-2	16 03	PA 16-5 and 512 x 4(L)	IM 512 x 4-16-AMD	SA 4-1 B 512 x 4/16	DIS-134 AM	DA 21	AM 130-3
Am27S15	715-1411-1	–	PA 24-14 and 512 x 8(L)	IM 512 x 8-24-27S15-AMD	SA 17-3 B 512 x 8/24	DIS-165 AM	DA 33	–
Am27S25	715-1617	62 65	PA 24-16 and 512 x 8(L)	IM 512 x 8-24-27S25-AMD	SA 31-2 B 512 x 8/24	DIS-213 AM	DA 31	AM 190-2
Am27S27	715-1412-2	–	PA 22-4 and 512 x 8(L)	IM 512 x 8-22-27S27-AMD	SA 18 B 512 x 8/22	DIS-168 AM	DA 28	–
Am27S28/29	715-1413	16 09	PA 20-4 and 512 x 8(L)	IM 512 x 8-20-AMD	SA 6 B 512 x 8/20	DIS-158 AM	DA 34	AM 120-3
Am27S30/31	715-1545	16 36	PA 24-13 and 512 x 8(L)	IM 512 x 8-24-AMD	SA 22-6 B 512 x 8/24	DIS-135 AM	DA 29	–
Am27S32/33	715-1414	16 38	PA 18-6 and 1024 x 4(L)	IM 1024 x 4-18-AMD	SA 24 B 1024 x 4/18	DIS-136 AM	DA 38	AM 170-2
Am27S35 Am27S37	715-1723	62 66	PA 24-18 and 1025 x 8(L)	IM 1024 x 8-27S35/37-AMD	SA 31-1 B 1024 x 8/24	DIS-218 AM	DA 65	AM 190-3
Am27S180/181 Am27PS181	715-1545-2	16 37	PA 24-13 and 1024 x 8(L)	IM 1024 x 8-24-AMD	SA 22-7 B 1024 x 8/24	DIS-137 AM	DA 29	AM 100-6
Am27S280/281 Am27PS281		16 37	–	IM 1024 x 8-24-27S280/281-AMD	–	DIS-214 AM	DA 60	–
Am27S184/185 Am27LS184/185 Am27PS185	715-1616	16 06	PA 18-8 and 2048 x 4(L)	IM 2048 x 4-18-AMD	SA 4-4 B 2048 x 4/18	DIS-211 AM	DA 23	AM 140-3
Am27S190/191 Am27PS191	715-1688-1	16 68	PA 24-17 and 2048 x 8(L)	IM 2048 x 8-24-AMD	SA 22-10 B 2048 x 8/24	DIS-151 AM	DA 61	AM 100-5
Am27S290/291 Am27PS291	715-1688-2	16 68	PA 24-28 and 2048 x 8(L)	IM 2048 x 8-24-27S290/291-AMD	SA 29 B 2048 x 8/24	DIS-215 AM	DA 62	AM 190-7
Am27S40/41 Am27PS41	715-1282	–	PA 20-9 and 4096 x 4(L)	IM 4096 x 4-20-AMD	SA 30 B 4096 x 4/20	DIS-216 AM	DA 63	AM 120-6
Am27S45 Am27S47	715-1660	–	–	IM 2048 x 8-24-27S45/47-AMD	SA 31 B 2048 x 8/24	–	DA 64	AM 170-3
Am27S43	715-1698-002	–	–	IM 4096 x 8-24-AMD	–	–	–	–

AMERICAN MICROSYSTEMS, INC.

S2333

32,768 BIT (4096x8) STATIC NMOS ROM

Features

- ☐ Fast Access Time: 350ns Maximum
- ☐ Fully Static Operation
- ☐ Single +5V ±5% Power Supply
- ☐ Directly TTL Compatible Inputs
- ☐ Three-State TTL Compatible Outputs
- ☐ Two Programmable Chip Selects
- ☐ EPROM Pin Compatible (2732)

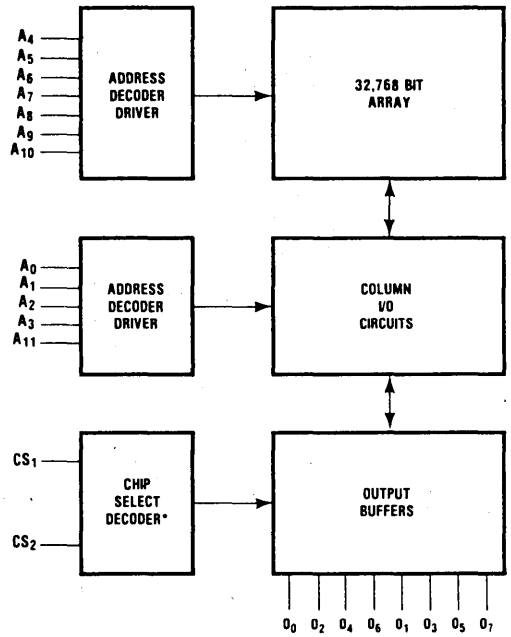
General Description

The AMI S2333 is a 32,768 bit static mask programmable NMOS ROM organized as 4096 words by 8 bits. The device is fully TTL compatible on all inputs and outputs and has a single +5V power supply. The three state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The S2333 is pin compatible with UV EPROMs making system development much easier and more cost effective. It is fully static, requiring no clocks for operation. The two chip selects are mask programmable, the active level for each being specified by the user.

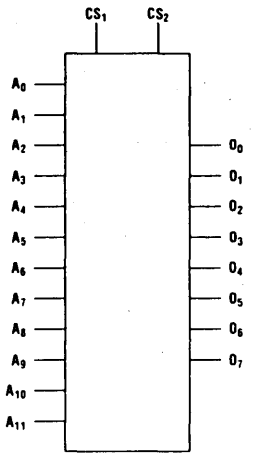
The S2333 is fabricated using AMI's N-Channel MOS technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

Block Diagram

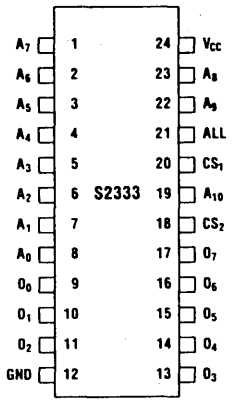


User Defined As Active High (CS), Active Low ($\overline{CS}$) or NC (No Connection)

Logic Symbol



Pin Configuration



Pin Names

$A_0 - A_{11}$	Address Inputs
$O_0 - O_7$	Data Outputs
$CS_1 - CS_2$	Chip Select Inputs
V_{CC}	+5V Power Supply

American Microsystems, Inc.

MEMORY

AMERICAN MICROSYSTEMS, INC.

S2364/S2364A

65,536 BIT (8192x8) STATIC NMOS ROM

Features

- ☐ Fast Access Time: S2364 450ns Maximum
  S2364A 350ns Maximum
- ☐ Low Standby Power
  55mW Maximum
- ☐ Late Mask Programmable
- ☐ Fully Static Operation
- ☐ Single +5V ±10% Power Supply
- ☐ Directly TTL Compatible Inputs
- ☐ Three-State TTL Compatible Outputs
- ☐ Three Programmable Chip Enables
- ☐ EPROM Pin Compatible (2764)

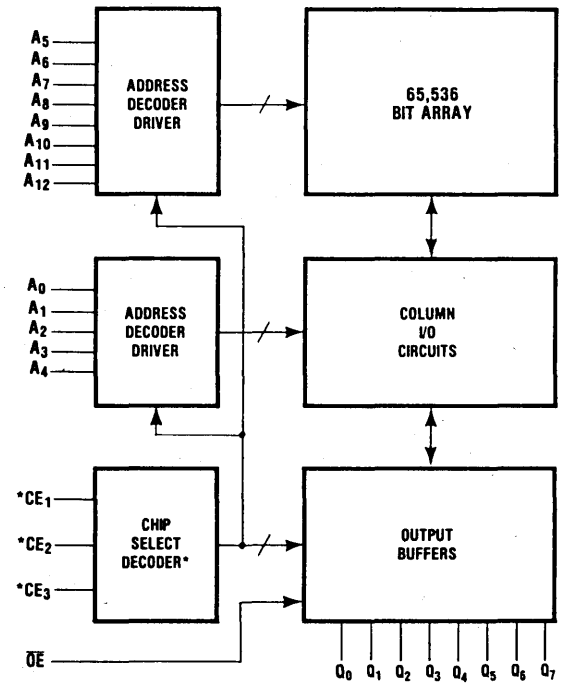
General Description

The AMI S2364 family are 65,536 bit static mask programmable NMOS ROMs organized as 8192 words by 8 bits. The devices are fully TTL compatible on all inputs and outputs and operate from a single +5V power supply. The three state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The S2364/S2364A are pin compatible with the 2764 UV EPROM making system development much easier and more cost effective. They are fully static, requiring no clocks for operation. The three chip enables are mask programmable; the active level for each being specified by the user. When the device is not enabled, the power supply current is reduced to a 10mA maximum.

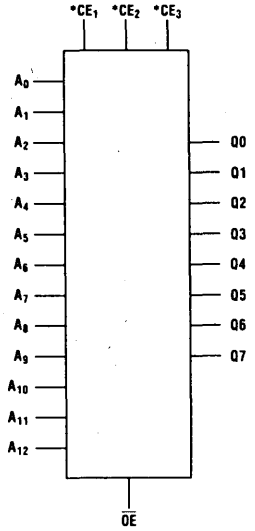
The S2364 family is fabricated using AMI's N-Channel NMOS ROM technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

Block Diagram

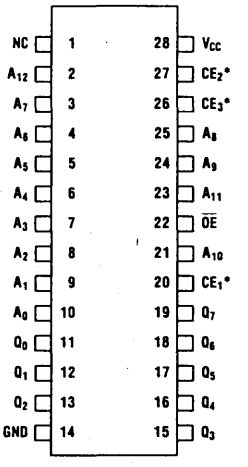


*USER DEFINED MASK PROGRAMMABLE CHIP ENABLE—MAY BE DEFINED AS ACTIVE HIGH, ACTIVE LOW, OR NO CONNECT.

Logic Symbol



Pin Configuration



Pin Names

A_0-A_{12}	Address Inputs
Q_0-Q_7	Data Outputs
CE_1, CE_2, CE_3	Chip Enables (User Defined)
$\overline{OE}$	Output Enable
V_{CC};GND;NC	5V;Ground;No Connect

AMERICAN MICROSYSTEMS, INC.

S23128

131,072 BIT (16384x8) STATIC NMOS ROM

Features

- ☐ Fast Access Time: 250ns Max.
- ☐ Low Standby Power: 66mW Max.
- ☐ Fully Static Operation
- ☐ Single +5V ± 10% Power Supply
- ☐ Directly TTL Compatible Outputs
- ☐ Three-State TTL Compatible Outputs
- ☐ Two Programmable Chip Enables/Selects
- ☐ EPROM Pin Compatible (27128)
- ☐ Late Mask Programmable
- ☐ Programmable Output/Chip Enable

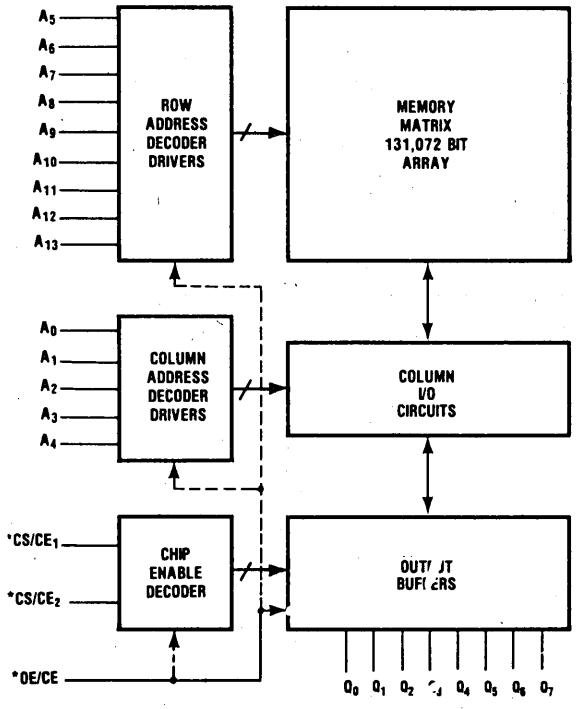
General Description

The AMI S23128 is a 131,072 bit static mask programmable NMOS ROM organized as 16,384 words by 8 bits. The device is fully TTL compatible on all inputs and outputs and has a single +5V power supply. The three state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The S23128 is pin compatible with the 27128 EPROM making system development easier and more cost effective. The fully static S23128 requires no clocks for operation. The three control pins are mask programmable with the active level and function being specified by the user. The pins can also be programmed as no connections. If CE functions are selected, automatic powerdown is available. The power supply current is reduced to 12mA when the chip is disabled.

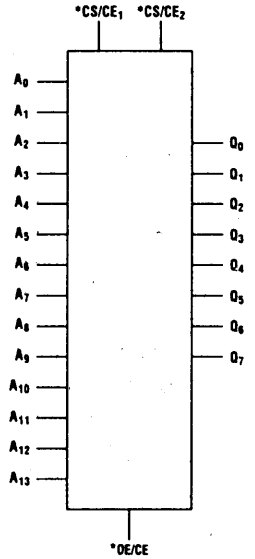
The S23128 is fabricated using AMI's NMOS technology. This permits the manufacture of high density, high performance ROMs.

Block Diagram

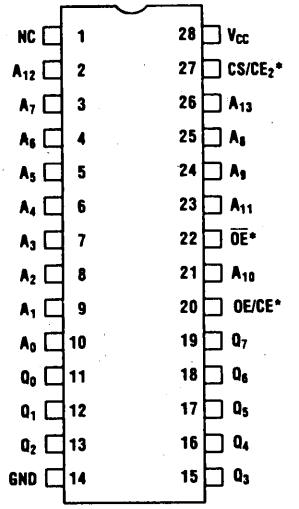


* THE USER DECIDES BETWEEN A CS OR CE FUNCTION AND THEN DEFINES THE ACTIVE LEVEL FOR CS/CE AND OE/CE.

Logic Symbol



Pin Configuration



Pin Names

A_0-A_{13}	Address Inputs
Q_0-Q_7	Data Outputs
CS/CE_1-CS/CE_2	Chip Selects/Enables
OE/CE	Output Enable/Chip Enable
V_{CC};GND;NC	5V;Ground; No Connect

American Microsystems, Inc.

MEMORY

AMERICAN MICROSYSTEMS, INC.

S68A316/S68B316

16,384 BIT (2048x8) STATIC NMOS ROM

Features

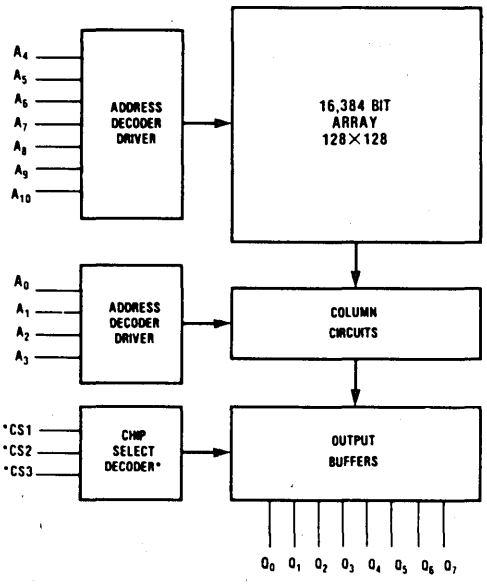
- ☐ Fast Address Access Time:
  S68A316 - 350ns Max.
  S68B316 - 250ns Max.
- ☐ EPROM Pin Compatible
- ☐ Fully Static Operation
- ☐ Three Programmable Chip Selects
- ☐ TTL Compatible Inputs
- ☐ Three-State TTL Compatible Outputs
- ☐ Late Mask Programmable

General Description

The AMI S68316 family of 16,384 bit mask programmable Read-Only-Memories organized as 2048 words by 8 bits offers fully static operation with a single +5V power supply. The device is fully TTL compatible on all inputs and three-state outputs. The three chip selects are mask programmable, the active level is specified by the user. The three-state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

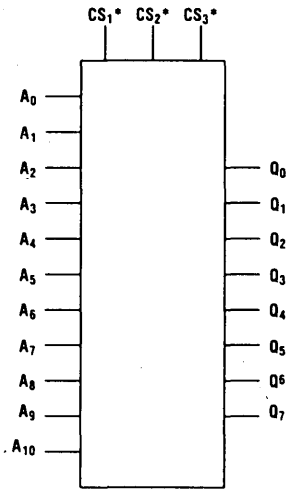
The devices are fabricated using AMI's N-Channel MOS technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

Block Diagram

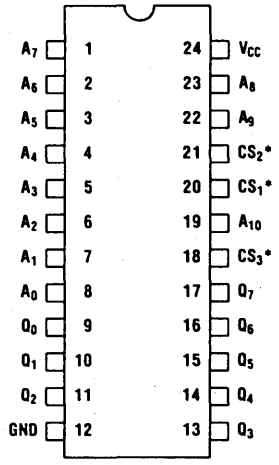


*USER DEFINED CHIP SELECTS
MAY BE DEFINED AS ACTIVE HIGH (CS) OR ACTIVE LOW (CS) OR NO CONNECTION (NC)

Logic Symbol



Pin Configuration



Pin Names

$A_0 - A_{10}$	Address Inputs
$Q_0 - Q_7$	Data Outputs
$CS_1 - CS_3$	Chip Select Inputs
V_{CC}	+5V Power Supply

AMERICAN MICROSYSTEMS, INC.

S68332/S68A332

32,768 BIT (4096x8) STATIC NMOS ROM

Features

- ☐ **Fast Access Time:**
  S68332: 450ns Maximum
  S68A332: 350ns Maximum
- ☐ **Fully Static Operation**
- ☐ **Single +5V ±5% Power Supply**
- ☐ **Directly TTL Compatible Inputs**
- ☐ **Three-State TTL Compatible Outputs**
- ☐ **Two Programmable Chip Selects**
- ☐ **EPROM Pin Compatible**

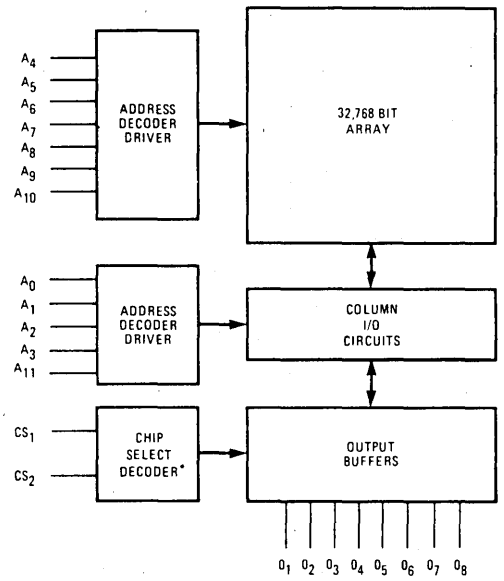
General Description

The AMI S68332 is a 32,768 bit static mask programmable NMOS ROM organized as 4096 words by 8 bits. The device is fully TTL compatible on all inputs and outputs and has a single +5V power supply. The three state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The S68332 is pin compatible with UV EPROMs making system development much easier and more cost effective. It is fully static, requiring no clocks for operation. The two chip selects are mask programmable, the active level for each being specified by the user.

The S68332 is fabricated using AMI's N-Channel MOS technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

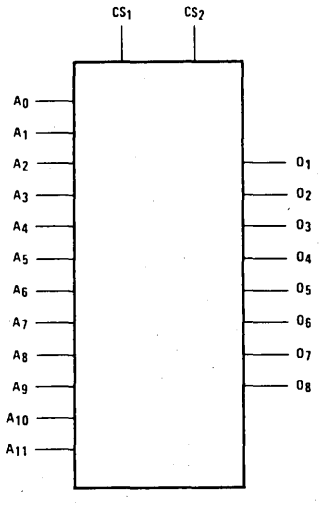
Block Diagram



*PROGRAMMABLE CHIP SELECTS

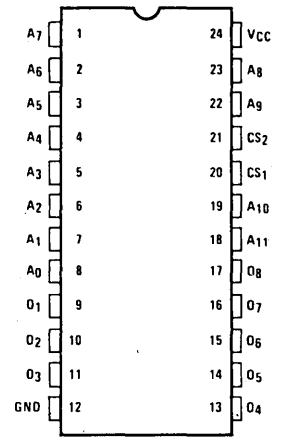
877273

Logic Symbol



877299

Pin Configuration



877300

Pin Names

A_0 - A_{11}	Address Inputs
O_1 - O_8	Data Outputs
CS_1 - CS_2	Chip Select Inputs
V_{CC}	+5V Power Supply

American Microsystems, Inc.

MEMORY

AMERICAN MICROSYSTEMS, INC.

S68A364/S68B364

65,536 BIT (8192x8) STATIC NMOS ROM

Features

- ☐ **Fast Access Time: 350ns Maximum**
- ☐ **Low Standby Power 55mW Maximum**
- ☐ **Fully Static Operation**
- ☐ **Single +5V ±10% Power Supply**
- ☐ **Directly TTL Compatible Inputs**
- ☐ **Three-State TTL Compatible Outputs**
- ☐ **Programmable Chip Enable**

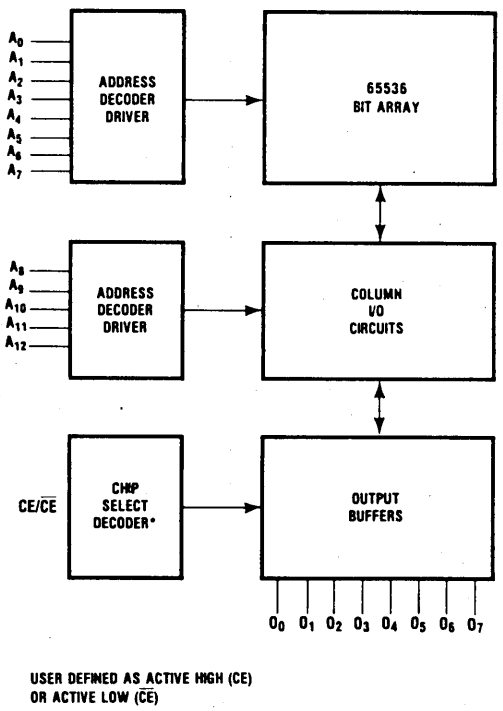
General Description

The AMI S68A364 is a 65,536 bit static mask programmable NMOS ROM organized as 8192 words by 8 bits. The device is fully TTL compatible on all inputs and outputs and has a single +5V power supply. The three state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The S68A364 is fully static, requiring no clocks for operation. The chip enable is mask programmable, the active level being specified by the user. When not enabled, power supply current is reduced to a maximum of 10mA.

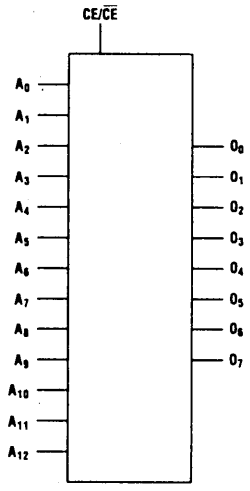
The S68A364 is fabricated using AMI's N-Channel MOS technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

Block Diagram

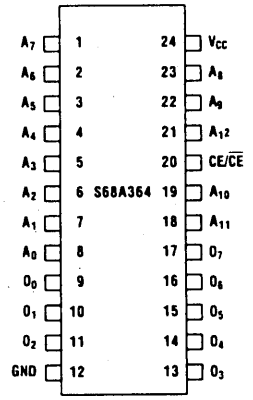


USER DEFINED AS ACTIVE HIGH (CE) OR ACTIVE LOW ($\overline{CE}$)

Logic Symbol



Pin Configuration



Pin Names

A_0-A_{11}	Address Inputs
O_0-O_7	Data Outputs
$CE/\overline{CE}$	Programmable Chip Enable
V_{CC}	+5V Power Supply

AMERICAN MICROSYSTEMS, INC.

S5101

1024 BIT (256×4) STATIC CMOS RAM

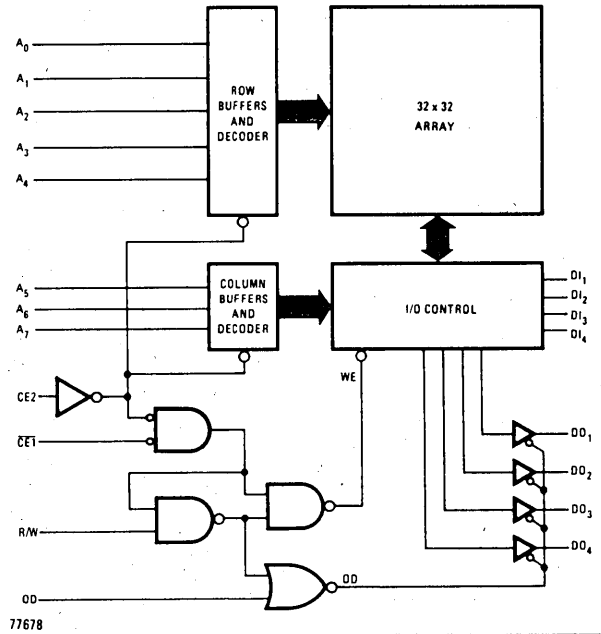
Features

- ☐ Ultra Low Standby Power
- ☐ Data Retention at 2V (L Version)
- ☐ Single +5 Volt Power Supply
- ☐ Completely Static Operation
- ☐ Completely TTL Compatible Inputs
- ☐ Three-State TTL Compatible Outputs

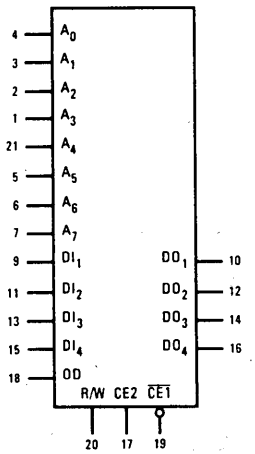
General Description

The AMI S5101 family of 256 x 4-bit ultra low power CMOS RAMs offers fully static operation with a single + 5 volt power supply. All inputs and outputs are directly TTL compatible. With data inputs and outputs on adjacent pins, either separate or common data I/O operations can easily be implemented for maximum design flexibility. The three-state outputs will drive one full TTL load and are disabled (high impedance state) by output disable (OD), either chip enable ($\overline{CE1}$ or CE2), or in a write cycle (R/W = LOW). This facilitates the control of common data I/O systems.

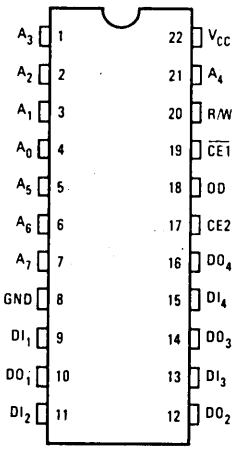
Block Diagram



Logic Symbol



Pin Configuration



Truth Table

$\overline{CE1}$	CE2	OD	R/W	DIN	Output	Mode
H	X	X	X	X	High Z	Not selected
X	L	X	X	X	High Z	Not Selected
X	X	H	H	X	High Z	Output Disabled
L	H	H	L	X	High Z	Write
L	H	L	L	X	High Z	Write
L	H	L	H	X	Dout	Read

Pin Names

A_0 - A_7	Address Inputs	$\overline{CE1}$	Chip Enable
DI_1 - DI_4	Data Inputs	CE2	Chip Enable
DO_1 - DO_4	Data Outputs	R/W	Read/Write Input
OD	Output Disable	V_{CC}	+5 Volt Power Supply

American Microsystems, Inc.

MEMORY

FAIRCHILD
A Schlumberger Company

Bipolar RAM Availability Guide

4th Quarter 1982

	Part No.	Organization	Outputs	Commercial[2] Access Time (Max) ns	Military[2] Access Time (Max) ns	Typical Power Dissipation mW	Available[1] Packages	Available[2] Temperature Ranges	No. of Pins
ECL	F10410	256 X 1	—	30	—	475	D,F,P	C	16
	F10414	256 X 1	—	10	—	520	D,F,P	C	16
	F100414	256 X 1	—	10	—	450	D,F,P	C	16
	F10422	256 X 4	—	10	—	935	D,F	C	24
	F100422	245 X 4	—	10	—	810	D,F	C	24
	F10415	1024 X 1	—	35	—	550	D,F,P	C	16
	F10415A	1024 X 1	—	20	—	550	D,F,P	C	16
	F100415	1024 X 1	—	20	—	475	D,F,P	C	16
	F10470	4096 X 1	—	35	—	830	D,F	C	18
	F10470A	4096 X 1	—	25	—	830	D,F	C	18
	F100470	4096 X 1	—	35	—	720	D,F	C	18
	F100470A	4096 X 1	—	25	—	720	D,F	C	18
	F10474	1024 X 1	—	25	—	830	D,F	C	24
	F100474	1024 X 1	—	25	—	720	D,F	C	24
TTL	93419	64 X 9	OC	45	60	500	D,P	C,M	28
	93419A	64 X 9	OC	35	—	500	D,P	C	28
	93422	256 X 4	3S	45	60	475	D,F,P	C,M	22*
	93422A	256 X 4	3S	35	45	475	D,F,P	C,M	22*
	93L422	256 X 4	3S	60	75	275	D,F,P	C,M	22*
	93L422A	256 X 4	3S	45	55	275	D,F,P	C,M	22*
	93479	256 X 9	3S	45	—	675	D	C	22
	93415	1024 X 1	OC	45	60	475	D,F,P	C,M	16
	93415A	1024 X 1	OC	30	—	475	D,F,P	C	16
	93L415	1024 X 1	OC	60	70	225	D,F,P	C,M	16
	93425	1024 X 1	3S	45	60	475	D,F,P	C,M	16
	93425A	1024 X 1	3S	30	50	475	D,F,P	C,M	16
	93L425	1024 X 1	3S	60	70	225	D,F,P	C,M	16
	93471	4096 X 1	3S	45	60	650	D,F,P	C,M	18
	†93471A	4096 X 1	3S	—	45	650	D,F,P	C,M	18
	†93475	1024 X 4	3S	45	60	700	D,F,P	C,M	18

Note 1. D = Ceramic DIP, F = Flatpak, P = Plastic DIP (commercial only).
Note 2. M = Mil Temp Range −55°C to +125°C, C = Commercial Temp Range 0° to 70°C.

* 24-Pin in Flatpak
† Available Soon

FAIRCHILD
A Schlumberger Company

Bipolar RAM Availability Guide

Cross Reference

	Fairchild Part No.	AMD	Fujitsu	Hitachi	Intel	Motorola	National	Signetics	TI
ECL	F10410			HM2105		MCM10144			
	F10414			HM10414		MCM10152	DM10414A		
	F100414								
	F10422		MBM10422	HM10422			DM10422	10422	
	F100422			HM100422				100422	
	F10415	Am10415	MBM10415	HM2110		MCM10146	DM10415	10415	
	F100415	Am100415		HM100415				100415	
	F10470	Am10470	MBM10470	HM10470		MCM10470	DM10470	10470	
	F100470	Am100470		HM100470				100470	
	F10474		MBM10474	HM10474		MCM10474		10474	
	F100474			HM100474				100474	
TTL	93419		MBM93419					82S19	
	93422	Am93422				MCM93422			
	93L422	Am93L422							
	93479					MCM93479		82S212	
	93415			HM2510	2115H	MCM93415			54/74S314
	93L415				2115				54/74LS314
	93425	Am93425		HM2511-1	2125	MCM93425			54/74S214
	93L425				2125				
	93471								
	93475				2149H-2				2149H

All cross references listed above are for general replacement. Refer to device data sheets for specific parameter equivalence.

FAIRCHILD
A Schlumberger Company

F10414
256 x 1-Bit Static Random Access Memory

F10K ECL Product

Description

The F10414 is a 256-bit read/write Random Access Memory (RAM), organized 256 words by one bit. It is designed for high-speed scratchpad, control and buffer storage applications. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as three active-LOW Chip Select lines.

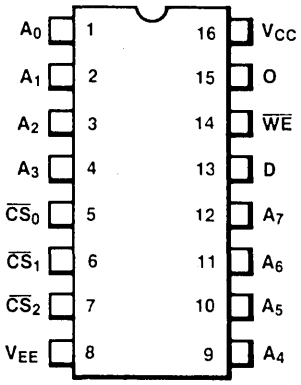
- **Address Access Time–10 ns Max**
- **Chip Select Access Time–6.0 ns Max**
- **Open-emitter Outputs for Easy Memory Expansion**
- **Power Dissipation–1.8 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

Pin Names

$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{CS_0}$–$\overline{CS_2}$	Chip Select Inputs (Active LOW)
A_0–A_7	Address Inputs
D	Data Input
O	Data Output

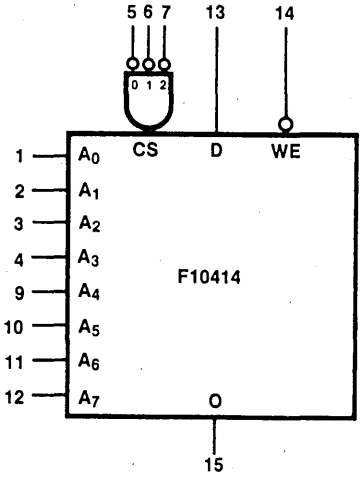
Connection Diagram

16-Pin DIP (Top View)



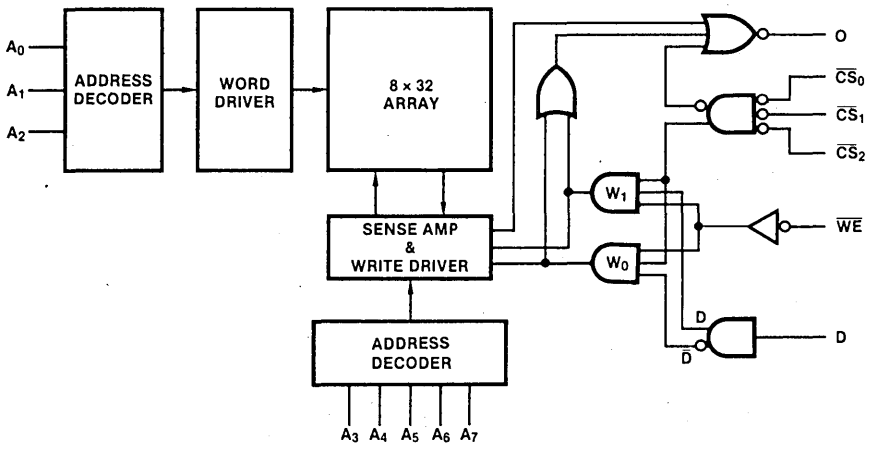
Note
The 16-pin Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

Logic Symbol



V_{CC} = Pin 16
V_{EE} = Pin 8

Logic Diagram



FAIRCHILD
A Schlumberger Company

F10415
1024 x 1-Bit Static Random Access Memory

F10K ECL Product

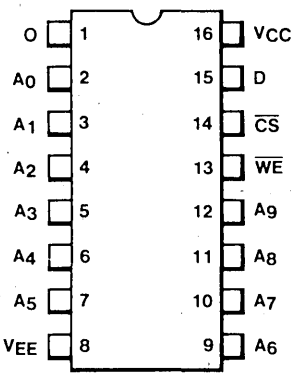
Description

The F10415 is a 1024-bit read/write Random Access Memory (RAM), organized as 1024 words by one bit per word and designed for high-speed scratchpad, control and buffer storage applications. It is available in two speed versions, the F10415 and F10415A. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as an active-LOW Chip Select line.

- **Address Access Time**
  F10415–35 ns Max
  F10415A–20 ns Max
- **Chip Select Access Time**
  F10415–10 ns Max
  F10415A–8.0 ns Max
- **Open-emitter Outputs for Easy Memory Expansion**
- **Power Dissipation–0.5 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

Connection Diagram

16-Pin DIP (Top View)

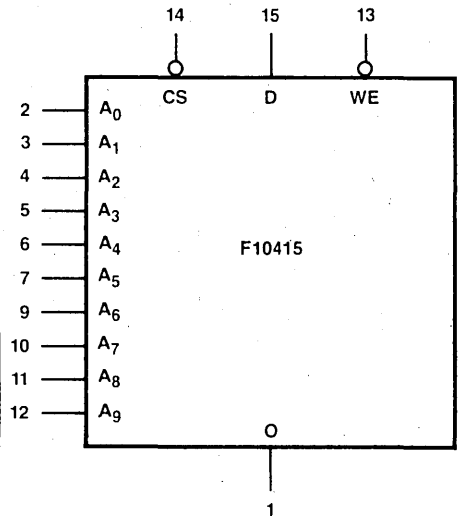


Note
The 16-pin Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

Pin Names

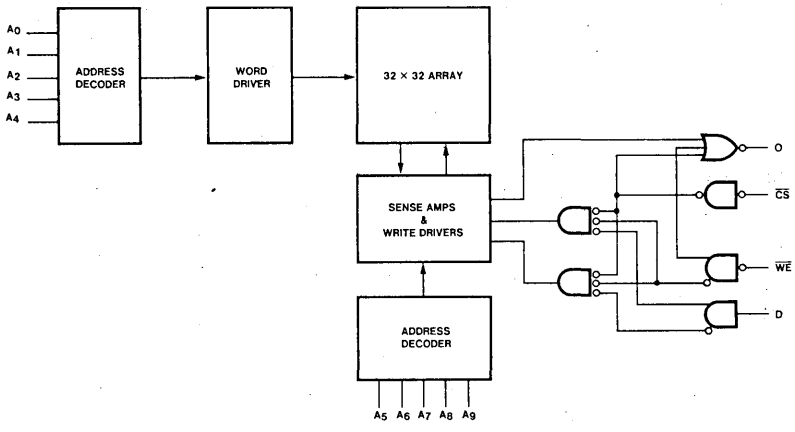
$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{CS}$	Chip Select Input (Active LOW)
A_0–A_9	Address Inputs
D	Data Input
O	Data Output

Logic Symbol



V_{CC} = Pin 16
V_{EE} = Pin 8

Logic Diagram



FAIRCHILD
A Schlumberger Company

F10Z416
256 X 4-Bit Programmable Read Only Memory

F10K Junction Fuse ECL Memory

Description

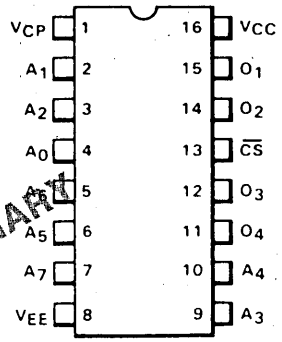
The F10Z416 is a fully decoded 1024-bit Programmable Read Only Memory (PROM), organized 256 words by four bits per word. The F10Z416 is designed for high speed control store, mapping, code conversion and logic replacement. The device is available in two speed versions, standard speed and 'A' grade.

The F10Z416 uses open base transistor (junction) fuse cells. Initially the unprogrammed cell is in the logic '0' state. The cell can be programmed to a logic '1' state by following the specified programming procedure which fuses aluminum through the emitter base junction of the cell transistor.

- **Address Access Time**
  F10Z416 — 15ns Max
  F10Z416A — 10ns Max
- **Highly Reliable Junction Fuses**
- **Power Dissipation — 0.53mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

Connection Diagram

16-Pin DIP (Top View)

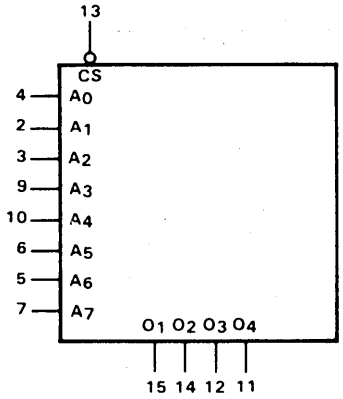


Notes
V_{CP} (Pin 1) is connected to the Programmer (+10.5 V) during programming only; otherwise, it should be grounded.
The Flatpak version has the same pinout (Connection Diagram) as the Dual In-line Package.

Pin Names

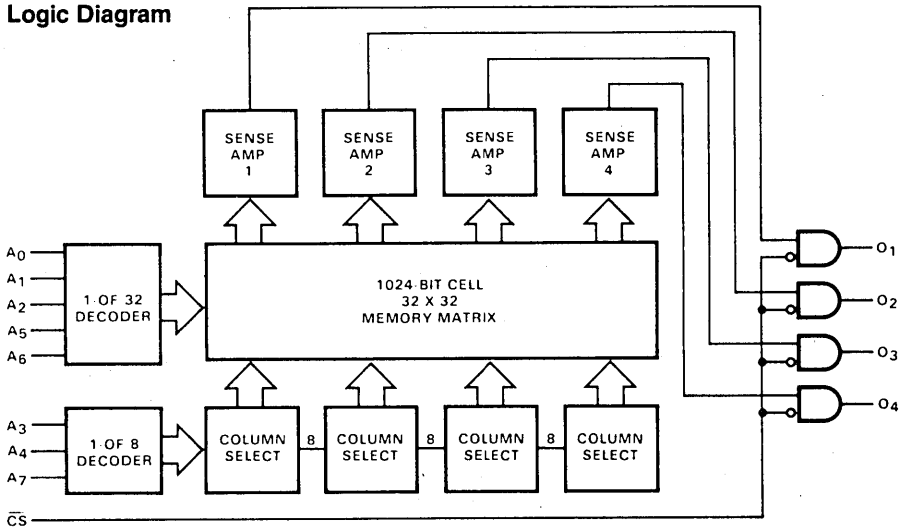
$\overline{CS}$	Chip Select Input (Active LOW)
A_0-A_7	Address Inputs
O_1-O_4	Data Outputs

Logic Symbol



V_{CP} = Pin 1
V_{CC} = Pin 16
V_{EE} = Pin 8

Logic Diagram



FAIRCHILD
A Schlumberger Company

F10422
256 x 4-Bit Static Random Access Memory

F10K ECL Product

Description

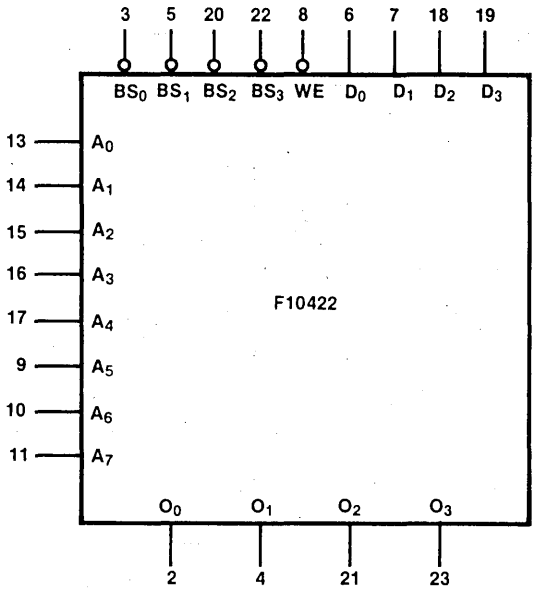
The F10422 is a 1024-bit read/write Random Access Memory (RAM), organized 256 words by four bits per word. It is designed for high-speed scratchpad, control and buffer storage applications. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as four active-LOW Bit Select lines.

- **Address Access Time–10 ns Max**
- **Bit Select Access Time–5.0 ns Max**
- **Four Bits Can be Independently Selected**
- **Open-emitter Outputs for Easy Memory Expansion**
- **Power Dissipation–0.92 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

Pin Names

$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{BS_0}$–$\overline{BS_3}$	Bit Select Inputs (Active LOW)
A_0–A_7	Address Inputs
D_0–D_3	Data Inputs
O_0–O_3	Data Outputs

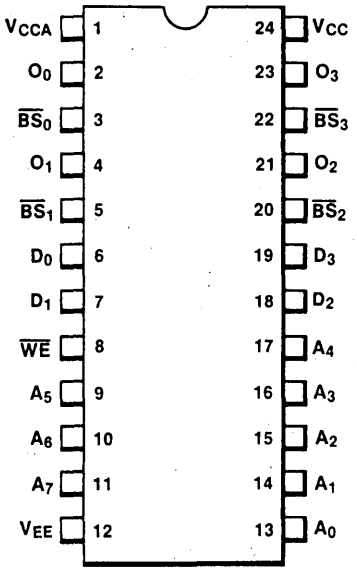
Logic Symbol



V_{CC} = Pin 24
V_{CCA} = Pin 1
V_{EE} = Pin 12

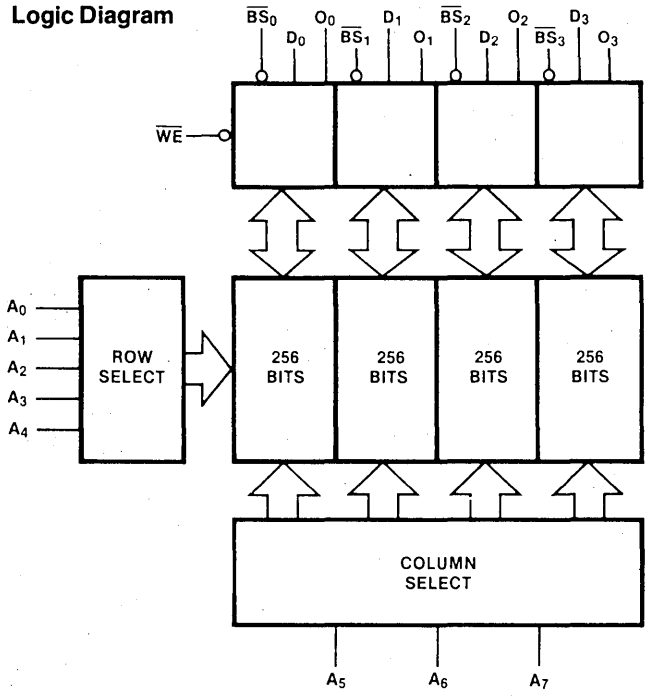
Connection Diagrams

24-Pin DIP (Top View)



Note
The 24-pin flatpak version has the same pinout connections as the Dual In-Line package.

Logic Diagram



Fairchild

MEMORY

FAIRCHILD
A Schlumberger Company

F10470
4096 x 1-Bit Static Random Access Memory

F10K ECL Product

Description

The F10470 is a 4096-bit read/write Random Access Memory (RAM), organized 4096 words by one bit per word and designed for high-speed scratchpad, control and buffer storage applications. It is available in two speed versions, the F10470 and F10470A. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as an active-LOW Chip Select line.

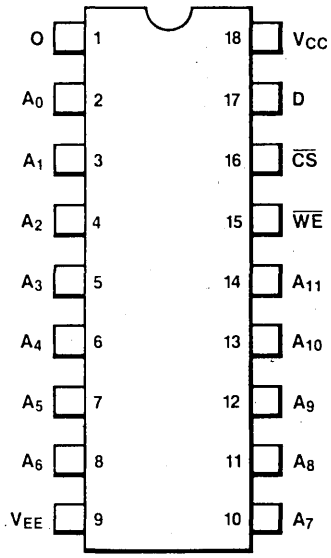
- **Address Access Time**
  F10470-35 ns Max
  F10470A-25 ns Max
- **Chip Select Access Time**
  F10470-15 ns Max
  F10470A-10 ns Max
- **Open-emitter Outputs for Easy Memory Expansion**
- **Power Dissipation-0.20 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

Pin Names

$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{CS}$	Chip Select Input (Active LOW)
A_0-A_{11}	Address Inputs
D	Data Input
O	Data Output

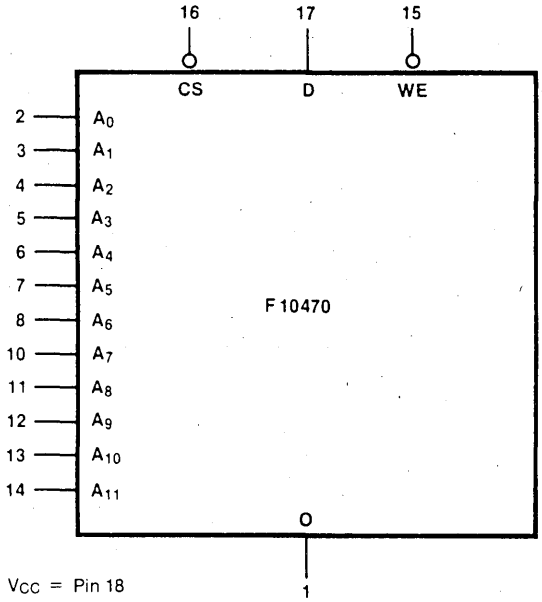
Connection Diagram

18-Pin DIP (Top View)



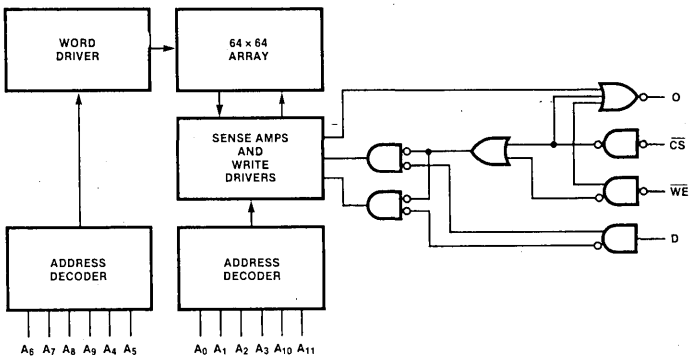
Note
The 18-pin Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

Logic Symbol



V_{CC} = Pin 18
V_{EE} = Pin 9

Logic Diagram



FAIRCHILD
A Schlumberger Company

F10474
1024 x 4-Bit Static Random Access Memory

F10K ECL Product

Description

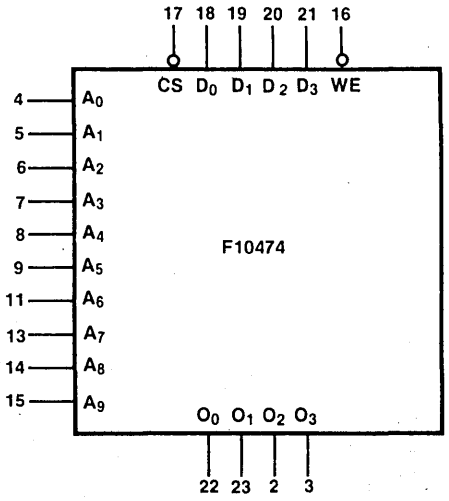
The F10474 is a 4096-bit read/write Random Access Memory (RAM), organized 1024 words by four bits per word. It is designed for high-speed scratchpad, control and buffer storage applications. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as an active-LOW Chip Select line.

- **Address Access Time–25 ns Max**
- **Chip Select Access Time–15 ns Max**
- **Open-emitter Outputs for Easy Memory Expansion**
- **Power Dissipation–0.20 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

Pin Names

$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{CS}$	Chip Select Input (Active LOW)
A_0–A_9	Address Inputs
D_0–D_3	Data Inputs
O_0–O_3	Data Outputs

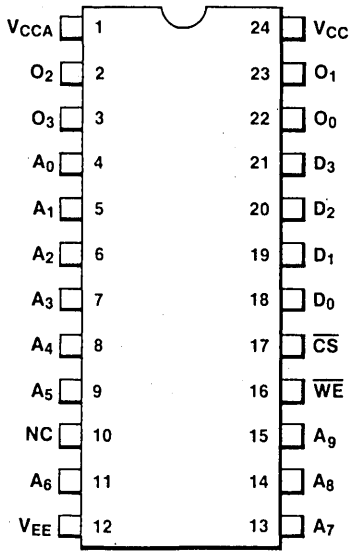
Logic Symbol



V_{CC} = Pin 24
V_{CCA} = Pin 1
V_{EE} = Pin 12
NC = Pin 10

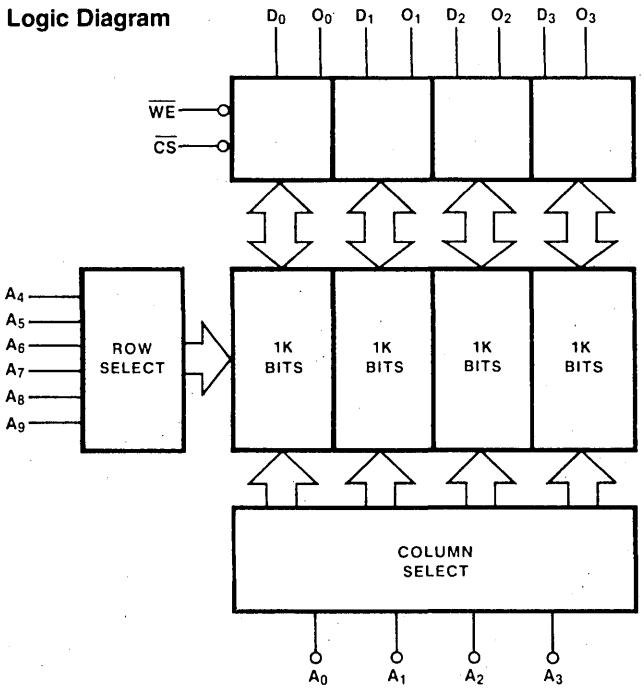
Connection Diagram

24-Pin DIP (Top View)



Note
The 24-pin flatpak version has the same pinout connections as the Dual In-Line package.

Logic Diagram



FAIRCHILD
A Schlumberger Company

F10480
16,364 X 1-Bit Static Random Access Memory

Description

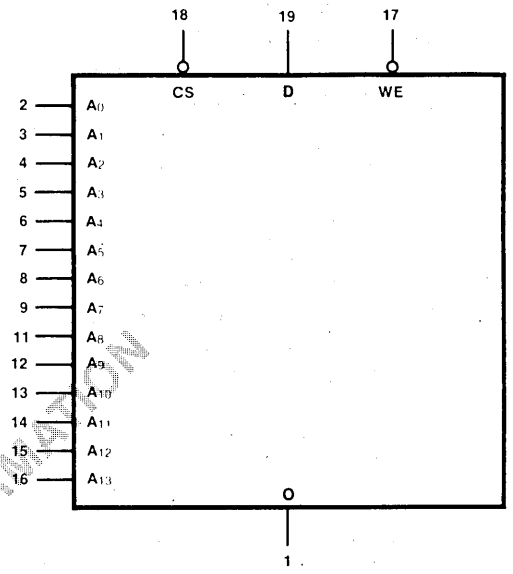
The F10480 is a 16,384-bit read/write Random Access Memory (RAM), organized 16,384 words by one bit per word. It is designed for high-speed scratchpad, control and buffer storage and main memory applications. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as an active LOW Chip Select line.

- **Address Access Time — 25ns Max**
- **Chip Select Access Time — 10ns Max**
- **Open-emitter Outputs for Easy Memory Expansion**
- **Power Dissipation — 0.055mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature.**

Pin Names

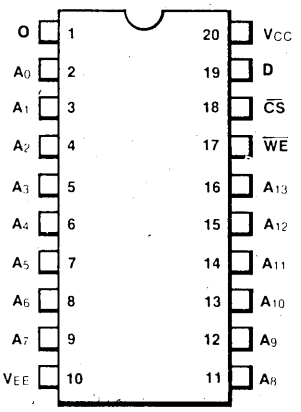
$\overline{WE}$	Write Enable Input (Active-LOW)
$\overline{CS}$	Chip Select Input (Active-LOW)
A_0–A_{13}	Address Inputs
D	Data Input
O	Data Output

Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

Connection Diagram 20-Pin DIP



(Top View)

Note
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

Table 1 Truth Table

Inputs			Output	
$\overline{CS}$	$\overline{WE}$	D_{IN}	Open Emitter	Mode
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{OUT}	Read

L = LOW Voltage Levels = −1.7 V
H = HIGH Voltage Levels = −0.9 V
(Nominal values)
X = Don't Care

FAIRCHILD
A Schlumberger Company

F100414
256 x 1-Bit Static Random Access Memory

F100K ECL Product

Description

The F100414 is a 256-bit read/write Random Access Memory (RAM), organized 256 words by one bit. It is designed for high-speed scratchpad, control and buffer storage applications. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as three active-LOW Chip Select lines.

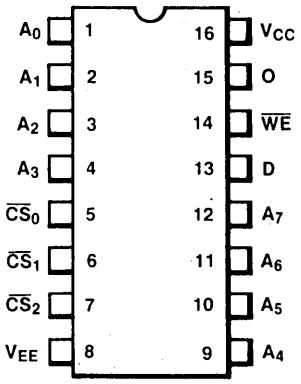
- **Address Access Time–10 ns Max**
- **Chip Select Access Time–6.0 ns Max**
- **Open-emitter Outputs for Easy Memory Expansion**
- **Power Dissipation–1.8 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

Pin Names

$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{CS_0}$–$\overline{CS_2}$	Chip Select Inputs (Active LOW)
A_0–A_7	Address Inputs
D	Data Input
O	Data Output

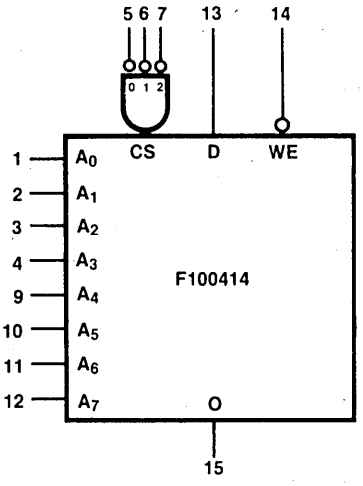
Connection Diagram

16-Pin DIP (Top View)



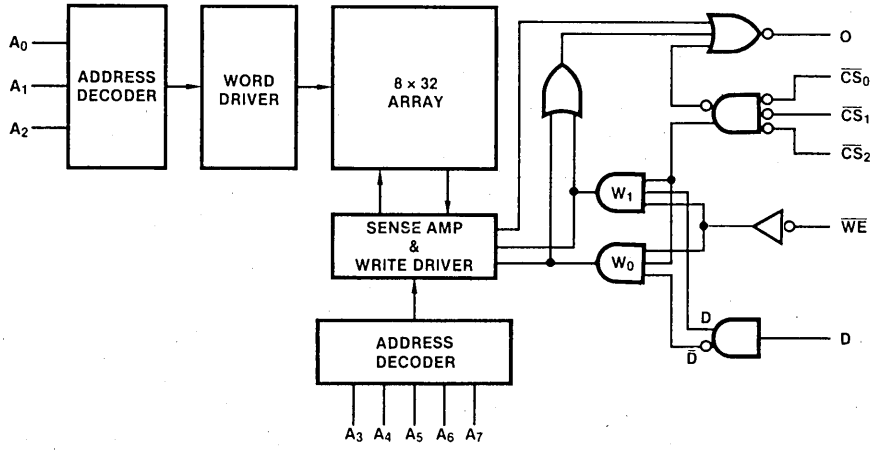
Note
The 16-pin Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

Logic Symbol



VCC = Pin 16
VEE = Pin 8

Logic Diagram



Fairchild

MEMORY

FAIRCHILD
A Schlumberger Company

F100415
1024 x 1-Bit Static Random Access Memory

F100K ECL Product

Description

The F100415 is a 1024-bit read/write Random Access Memory (RAM), organized as 1024 words by one bit per word and designed for high-speed scratchpad, control and buffer storage applications. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as three active-LOW Chip Select line.

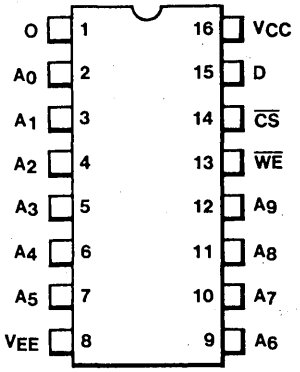
- **Address Access Time — 20 ns Max**
- **Chip Select Access Time — 8.0 ns Max**
- **Open-emitter Outputs for Easy Memory Expansion**
- **Power Dissipation–0.5 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

Pin Names

$\overline{WE}$	Write Enable Inputs (Active LOW)
$\overline{CS}$	Chip Select Input (Active LOW)
A_0–A_9	Address Inputs
D	Data Input
O	Data Output

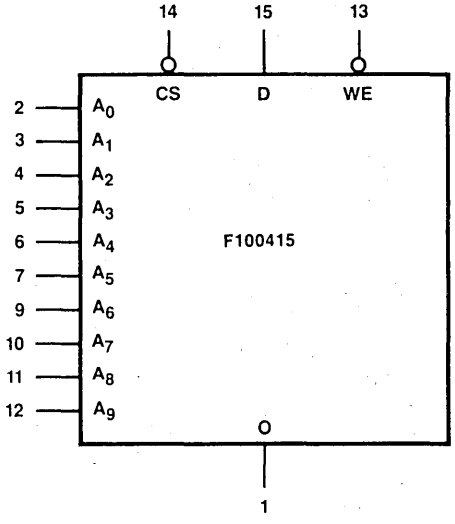
Connection Diagram

16-Pin DIP (Top View)



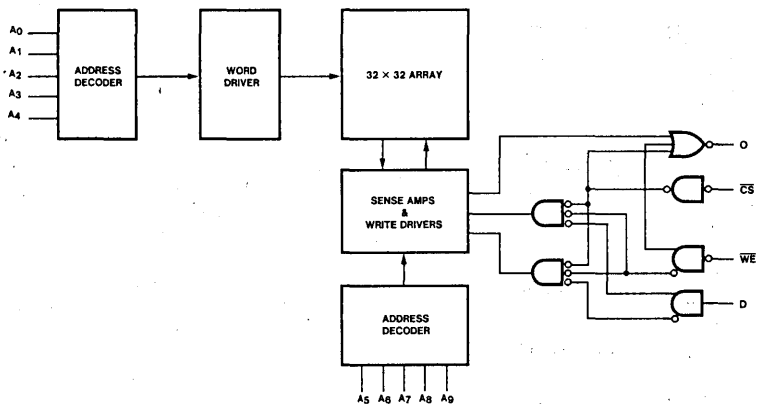
Note
The 16-pin Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

Logic Symbol



V_{CC} = Pin 16
V_{EE} = Pin 8

Logic Diagram



FAIRCHILD
A Schlumberger Company

F100416
256 x 4-Bit Programmable Read Only Memory

F100K ECL Product

Description

The F100416 is a 1024-bit field Programmable Read Only Memory (PROM), organized 256 words by four bits per word. It is designed for high-speed control, mapping, code conversion, and logic replacement. The device includes full on-chip address decoding, non-inverting Data output lines, and an active-LOW Chip Select line for easy memory expansion. The device is manufactured with all bits in the logic-HIGH state. Programmed bits will furnish LOW levels at corresponding outputs.

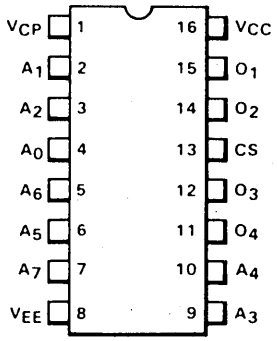
- **Address Access Time – 20 ns Max**
- **Chip Select Access Time – 8.0 ns Max**
- **Chip Select Input and Open-emitter Outputs for Easy Memory Expansion**
- **Power Dissipation – 0.46 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

Pin Names

$\overline{CS}$	Chip Select Input (Active LOW)
A_0–A_7	Address Inputs
O_1–O_4	Data Outputs

Connection Diagram

16-Pin DIP (Top View)

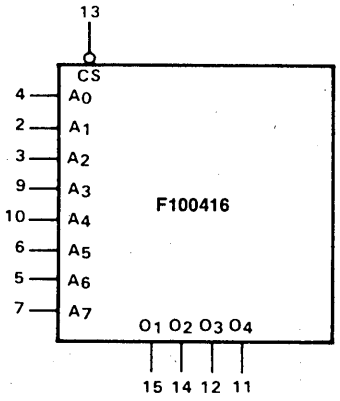


Notes

V_{CP} (Pin 1) is connected to the Programmer (+10.5 V) during programming only; otherwise, it should be grounded.

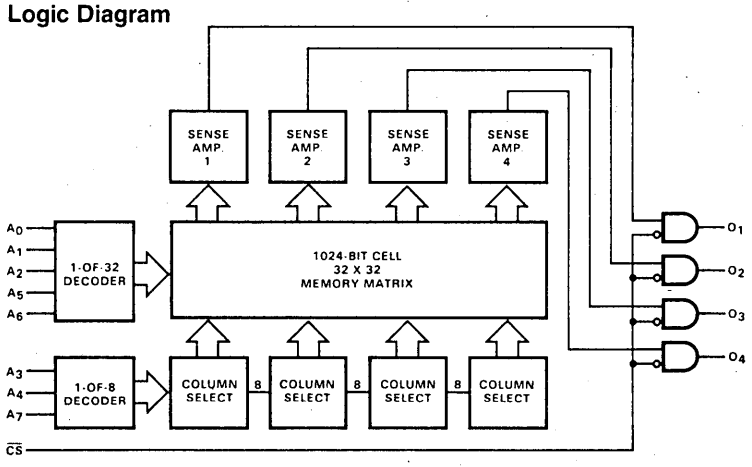
The Flatpak version has the same pinout (Connection Diagram) as the Dual In-line Package.

Logic Symbol



V_{CP} = Pin 1
V_{CC} = Pin 16
V_{EE} = Pin 8

Logic Diagram



FAIRCHILD
A Schlumberger Company

F100Z416
256 X 4-Bit Programmable Read Only Memory

F100K Junction Fuse ECL Memory

Description

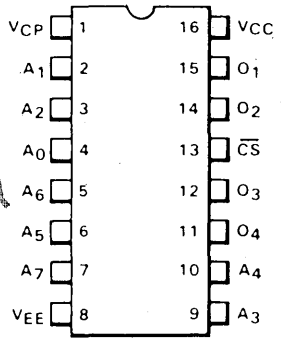
The F100Z416 is a fully decoded 1024-bit Programmable Read Only Memory (PROM), organized 256 words by four bits per word. The F100Z416 is designed for high speed control store, mapping, code conversion and logic replacement. The device is available in two speed versions, standard speed and 'A' grade.

The F100Z416 uses open base transistor (junction) fuse cells. Initially the unprogrammed cell is in the logic '0' state. The cell can be programmed to a logic '1' state by following the specified programming procedure which fuses aluminum through the emitter base junction of the cell transistor.

- **Address Access Time**
  F100Z416 — 15ns Max
  F100Z416A — 10ns Max
- **Highly Reliable Junction Fuses**
- **Power Dissipation — 0.46mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

Connection Diagram

16-Pin DIP (Top View)



Notes

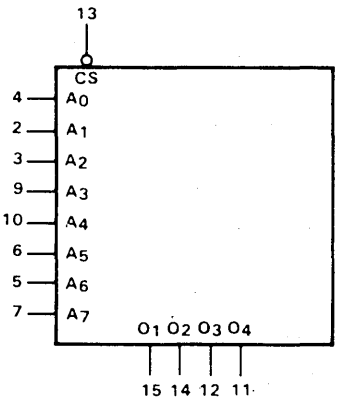
V_{CP} (Pin 1) is connected to the Programmer (+10.5 V) during programming only; otherwise, it should be grounded.

The Flatpak version has the same pinout (Connection Diagram) as the Dual In-line Package.

Pin Names

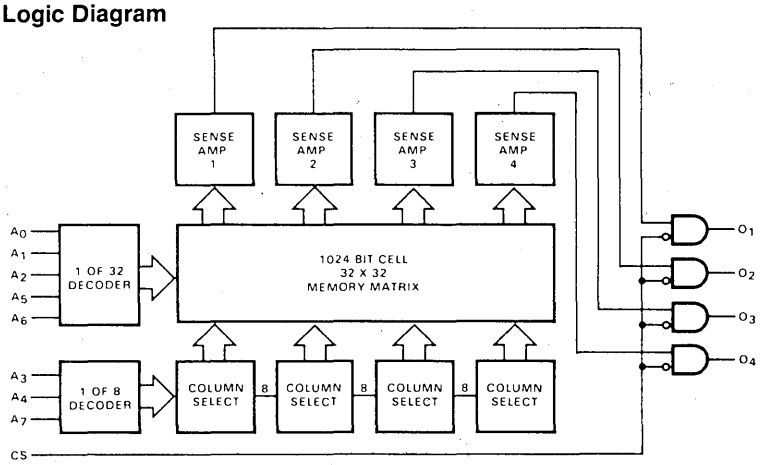
$\overline{CS}$	Chip Select Input (Active LOW)
A_0-A_7	Address Inputs
O_1-O_4	Data Outputs

Logic Symbol



V_{CP} = Pin 1
V_{CC} = Pin 16
V_{EE} = Pin 8

Logic Diagram



FAIRCHILD
A Schlumberger Company

F100470
4096 x 1-Bit Static Random Access Memory

F100K ECL Product

Description

The F100470 is a 4096-bit read/write Random Access Memory (RAM), organized 4096 words by one bit per word and designed for high-speed scratchpad, control and buffer storage applications. It is available in two speed versions, the F100470 and F100470A. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as an active-LOW Chip Select line.

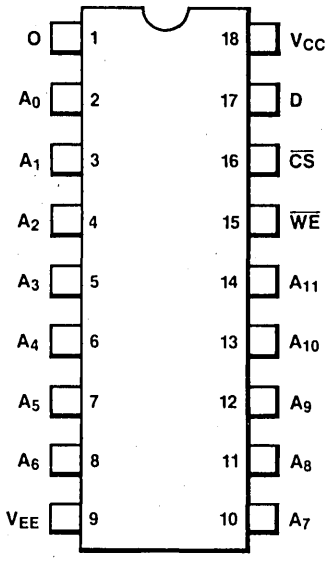
- **Address Access Time**
  F100470-35 ns Max
  F100470A-25 ns Max
- **Chip Select Access Time**
  F100470-15 ns Max
  F100470A-10 ns Max
- **Open-emitter Outputs for Easy Memory Expansion**
- **Power Dissipation-0.70 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

Pin Names

$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{CS}$	Chip Select Input (Active LOW)
A_0-A_{11}	Address Inputs
D	Data Input
O	Data Output

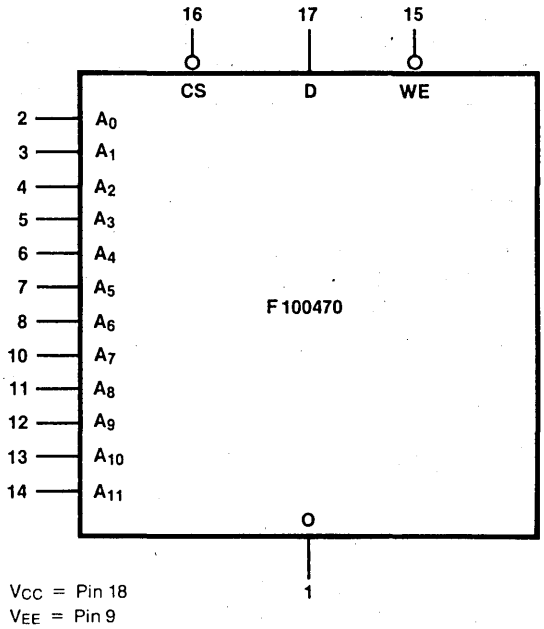
Connection Diagram

18-Pin DIP (Top View)



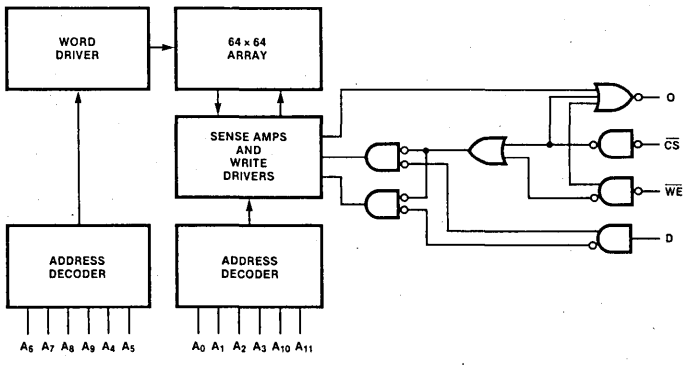
Note
The 18-pin Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

Logic Symbol



VCC = Pin 18
VEE = Pin 9

Logic Diagram



FAIRCHILD
A Schlumberger Company

F100474
1024 x 4-Bit Static Random Access Memory

F100K ECL Product

Description

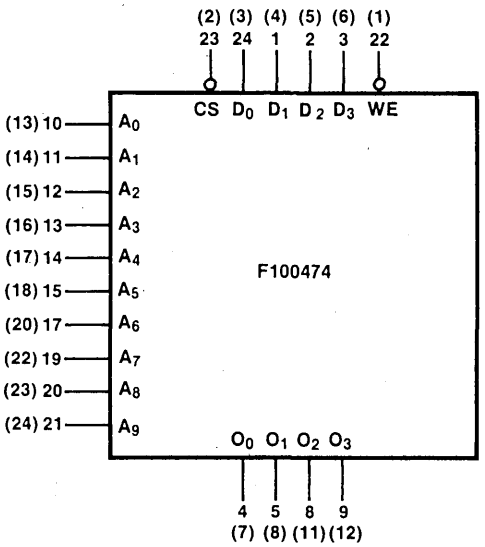
The F100474 is a 4096-bit read/write Random Access Memory (RAM), organized 1024 words by four bits per word. It is designed for high-speed scratchpad, control and buffer storage applications. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as an active-LOW Chip Select line.

- **Address Access Time–25 ns Max**
- **Chip Select Access Time–15 ns Max**
- **Open-emitter Outputs for Easy Memory Expansion**
- **Power Dissipation–0.70 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

Pin Names

$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{CS}$	Chip Select Input (Active LOW)
A_0–A_9	Address Inputs
D_0–D_3	Data Inputs
O_0–O_3	Data Outputs

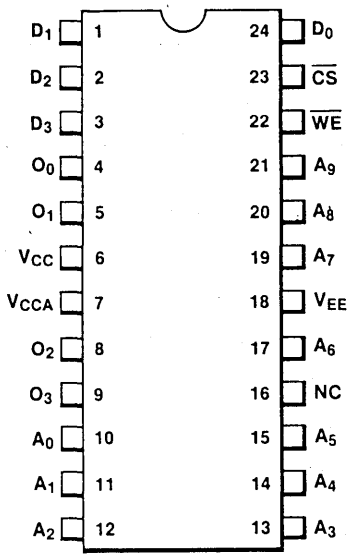
Logic Symbol



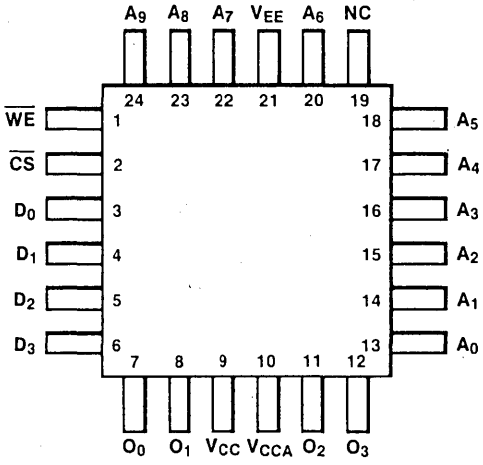
V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Connection Diagrams

24-Pin DIP (Top View)



24-Pin Flatpak (Top View)



Fairchild

MEMORY

FAIRCHILD
A Schlumberger Company

F100480
16,384 x 1-Bit Static Random Access Memory

F100K ECL Memory

Description

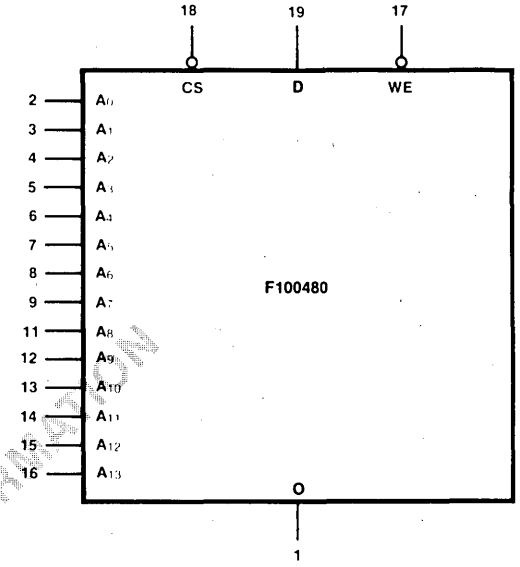
The F100480 is a 16,384-bit read/write Random Access Memory (RAM), organized 16,384 words by one bit per word. It is designed for high-speed scratchpad, control and buffer storage and main memory applications. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as an active LOW Chip Select line.

- **Address Access Time — 25ns Max**
- **Chip Select Access Time — 10ns Max**
- **Open-emitter Outputs for Easy Memory Expansion**
- **Power Dissipation — 0.044mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature.**

Pin Names

$\overline{WE}$	Write Enable Input (Active-LOW)
$\overline{CS}$	Chip Select Input (Active-LOW)
A_0-A_{13}	Address Inputs
D	Data Input
O	Data Output

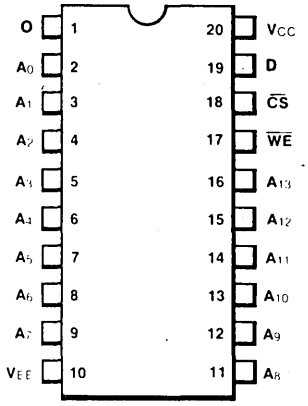
Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

Connection Diagram

20-Pin DIP (Top View)



(Top View)

Note
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

Table 1 Truth Table

Inputs			Output	
$\overline{CS}$	$\overline{WE}$	D_{IN}	Open Emitter	Mode
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{OUT}	Read

L = LOW Voltage Levels = −1.7 V
H = HIGH Voltage Levels = −0.9 V
(Nominal values)
X = Don't Care

Guaranteed Operating Ranges

Supply Voltage (V_{EE})			Ambient Temperature Note 4
Min	Typ	Max	
−5.7 V	−4.5 V	−4.2 V	0°C to 85°C

FAIRCHILD
A Schlumberger Company

93419/93419A
64 x 9-Bit Fully Decoded Random Access Memory

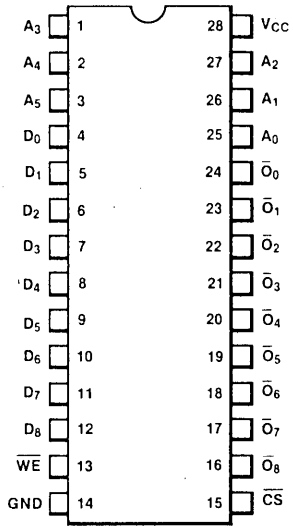
TTL Isoplanar Memory

Description

The 93419/93419A is a 576-Bit Read/Write Random Access Memory organized 64 words by nine bits per word with open collector outputs. It is ideally suited for scratchpad, small buffer and other applications where the number of required words is small and where the number of required bits per word is relatively large. The ninth bit can provide parity for 8-bit word systems.

- **Open Collector Outputs**
- **TTL Inputs and Outputs**
- **Isoplanar Technology**
- **Organization - 64 Words by Nine Bits**
- **Standard 28-Pin Dual in-Line Package**
- **Data Output is the Complement of Data Input**
- **Power Dissipation - 0.9 mW/Bit**
- **Maximum Address Access Time**
  93419 45 ns
  93419A 35 ns
- **Maximum Chip Select Access Time**
  93419 40 ns
  93419A 30 ns

Connection Diagram
28-Pin DIP

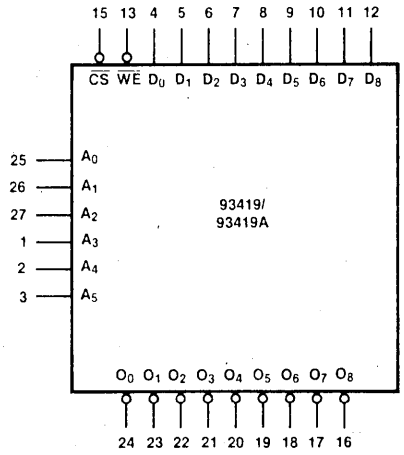


(Top View)

Pin Names

A_0-A_5	Address Inputs
D_0-D_8	Data Inputs
$\overline{O}_0$-$\overline{O}_8$	Outputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input

Logic Symbol



V_{CC} = Pin 28
GND = Pin 14

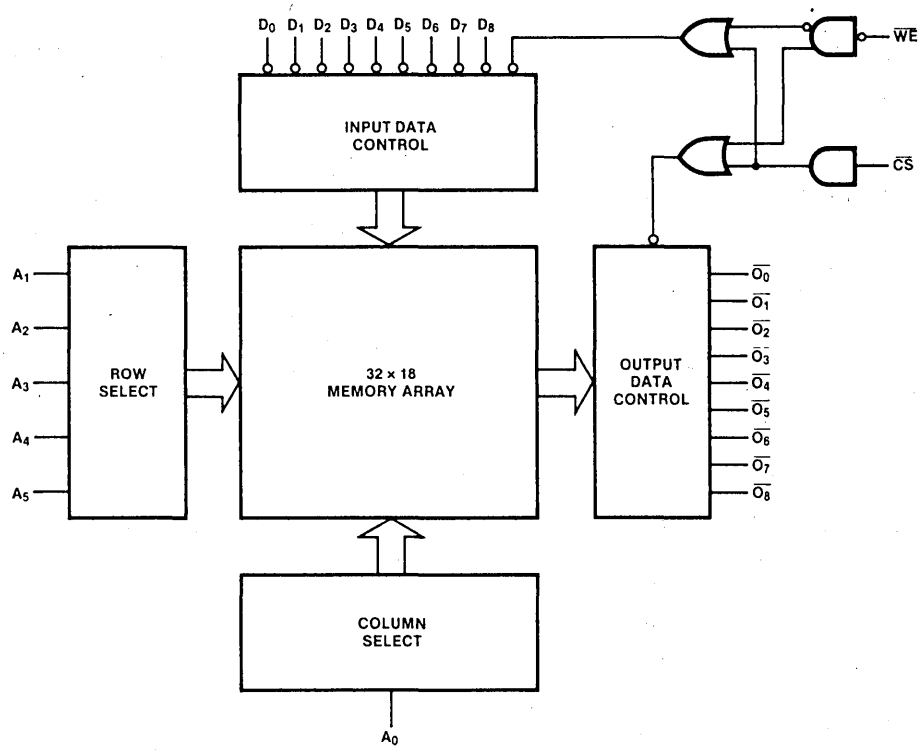
Truth Table

Inputs			Outputs	
$\overline{CS}$	$\overline{WE}$	D_0-D_8	Open Collector	Mode
H	X	X	H	Not Selected
L	L	L	H	Write "0"*
L	L	H	H	Write "1"*
L	H	X	$\overline{D_{OUT}}$*	Read

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Cary (HIGH or LOW)
*Memory inverts from Data In to Data Output

Fairchild Camera and Instrument Corporation
441 Whisman Road, Mountain View, California 94042
TWX 910 379 6435

Logic Diagram



Functional Description

The 93419/93419A is a fully decoded 576-bit Random Access Memory organized 64 words by nine bits. Word selection is achieved by means of a 6-bit address, A_0 to A_5.

The Chip Select input provides for memory array expansion. For large memories, the fast chip select access time permits the decoding of chip select ($\overline{CS}$) from the address without affecting system performance.

The read and write operations are controlled by the state of the active LOW Write Enable ($\overline{WE}$). With $\overline{WE}$ held LOW and the chip selected, the data at D_0-D_8 is written into the addressed location. To read, $\overline{WE}$ is held HIGH and the chip selected. Data in the specified location is presented at $\overline{O}_0$-$\overline{O}_8$ and is inverted from Data In to Data Out.

Open collector outputs are provided to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many 93419s can be tied together. In other applications the wired-OR is not used. In either case an external pull-up resistor of R_L value must be used to provide a HIGH at the output when it is off. Any R_L value within the range specified below may be used.

$$\frac{V_{CC}\,(MAX)}{I_{OL} - FO\,(1.6)} \leq R_L \leq \frac{V_{CC}\,(MIN) - V_{OH}}{n\,(I_{CEX}) + FO\,(0.04)}$$

R_L is in kΩ
n = number of wired-OR outputs tied together
FO = number of TTL Unit Loads (UL) driven
I_{CEX} = Memory Output Leakage Current
V_{OH} = Required Output HIGH Level at Output Node
I_{OL} = Output LOW Current

The minimum R_L value is limited by output current sinking ability. The maximum R_L value is determined by the output and input leakage current which must be supplied to hold the output at V_{OH}. One Unit Load = 40 μA HIGH/1.6 mA LOW. FO_{MAX} = 5 UL.

DC Characteristics Over Operating Temperature Ranges (Notes 1, 2, and 4)

Symbol	Characteristic	Min	Typ (Note 3)	Max	Unit	Conditions
V_{OL}	Output LOW Voltage		0.3	0.50	V	V_{CC} = Min, I_{OL} = 12 mA
V_{IH}	Input HIGH Voltage	2.1	1.6		V	Guaranteed Input HIGH Voltage for all Inputs
V_{IL}	Input LOW Voltage		1.5	0.8	V	Guaranteed Input LOW Voltage for all Inputs
I_{IL}	Input LOW Current		− 200	− 400	μA	V_{CC} = Max, V_{IN} = 0.4 V
I_{IH}	Input HIGH Current		1.0	40 1.0	μA mA	V_{CC} = Max, V_{IN} = 4.5 V V_{CC} = Max, V_{IN} = 5.25 V
I_{CEX}	Output Leakage Current		1.0	100	μA	V_{CC} = Max, V_{OUT} = 4.5 V
V_{CD}	Input Clamp Diode Voltage		− 1.0	− 1.5	V	V_{CC} = Max, I_{IN} = − 10 mA
I_{CC}	Power Supply Current			110	mA	T_A = 125°C; V_{CC} = Max, All Outputs Grounded, Outputs LOW
				120	mA	T_A = 75°C
			100	130	mA	T_A = 0°C
				150	mA	T_A = − 55°C

AC Characteristics Over Guaranteed Operating Ranges (Notes 1, 2, 4, 5, 6)

Symbol	Characteristic	93419AXC Min	93419AXC Max	93419XC Min	93419XC Max	93419XM Min	93419XM Max	Unit	Conditions
Read Mode	**Delay Times**								
t_{ACS}	Chip Select Access Time		30		40		40	ns	See Test Circuit and Waveforms
t_{RCS}	Chip Select Recovery Time		30		40		40	ns	
t_{AA}	Address Access Time		35		45		60	ns	
Write Mode	**Delay Times**								
t_{WS}	Write Disable Time		30		40		45	ns	See Test Circuit and Waveforms
t_{WR}	Write Recovery Time		35		45		55	ns	
	Input Timing Requirements								
t_W	Write Pulse Width (to guarantee write)	25		35		45		ns	
t_{WSD}	Data Setup Time Prior to Write	5		5		5		ns	
t_{WHD}	Data Hold Time After Write	5		5		5		ns	
t_{WSA}	Address Setup Time	5		5		10		ns	
t_{WHA}	Address Hold Time	5		5		5		ns	
t_{WSCS}	Chip Select Setup Time	5		5		5		ns	
t_{WHCS}	Chip Select Hold Time	5		5		5		ns	
C_{IN}	Input Pin Capacitance		5		5		5	pF	
C_{OUT}	Output Pin Capacitance		8		8		8	pF	

Notes

1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameters. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are at V_{CC} = 5.0 V, T_A = + 25°C, and Max loading.
4. The Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a two minute warm-up. Temperature range of operation refers to case temperature for Flatpaks and ambient temperature for all other packages. Typical thermal resistance values of the package at maximum temperature are:

   θ_{JA} (Junction to Ambient) (at 400 fpm air flow) = 30°C/Watt Ceramic DIP, 60°C/Watt Plastic DIP.
   θ_{JA} (Junction to Ambient) (still air) = 75°C/Watt Ceramic DIP, 110°C/Watt Plastic DIP
   θ_{JC} (Junction to Case) = 25°C/Watt Ceramic DIP, 40°C/Watt Plastic Dip

5. The Max address access time is guaranteed to be the "worst case" bit in the memory using a pseudo random testing pattern.
6. T_W measured at t_{WSA} = Min, t_{WSA} measured at t_W = Min.

FAIRCHILD
A Schlumberger Company

93422/93422A
256 x 4-Bit Fully Decoded Random Access Memory

TTL Isoplanar Memory

Description

The 93422/93422A is a 1024-bit Read/Write Access Memory organized 256 words by four bits per word. The 93422/93422A has 3-state outputs, and is designed primarily for buffer control storage and high-performance main memory applications. The device has a typical address access time of 30 ns.

- **Isoplanar Technology**
- **Organization — 256 Words x 4 Bits**
- **3-State Outputs**
- **Available in 22-Pin DIP or 24-Pin Flatpak Packages**
- **Inverting and Non-Inverting Select Inputs Provide Easy Memory Expansion**
- **Power Dissipation — 0.475 mW/Bit Typical**
- **Typical Read Access Time — 30 ns**

Pin Names

A_0-A_7	Address Inputs
D_1-D_4	Data Inputs
CS_1, CS_2	Chip Select Inputs
WE	Write Enable Input
O_1-O_4	Data Outputs
OE	Output Enable

Absolute Maximum Ratings

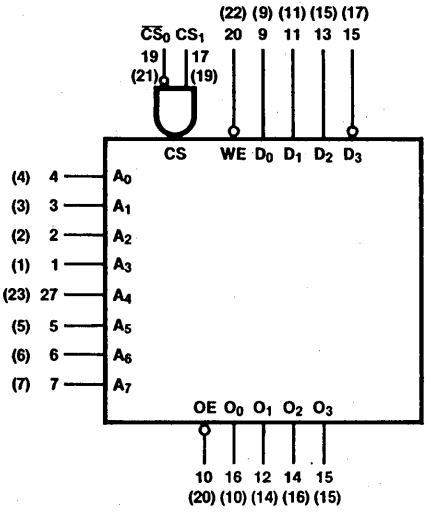
(above which the useful life may be impaired)

Storage Temperature	−65°C,	+150°C
Temperature (Ambient) Under Bias	−55°C,	+125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V,	+7.0 V
*Input Voltage (dc)	−0.5 V,	+5.5 V
*Input Current (dc)	−12 mA,	+5.0 mA
**Voltage Applied to Outputs (output HIGH)	−0.5 V,	+5.50 V
Output Current (dc)		+20 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

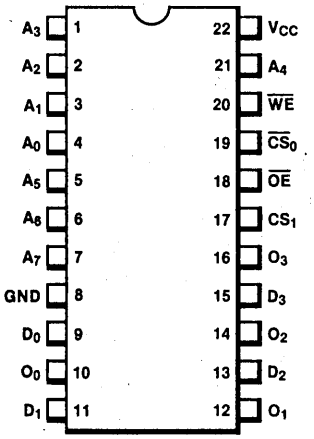
**Output Current Limit Required.

Logic Symbol



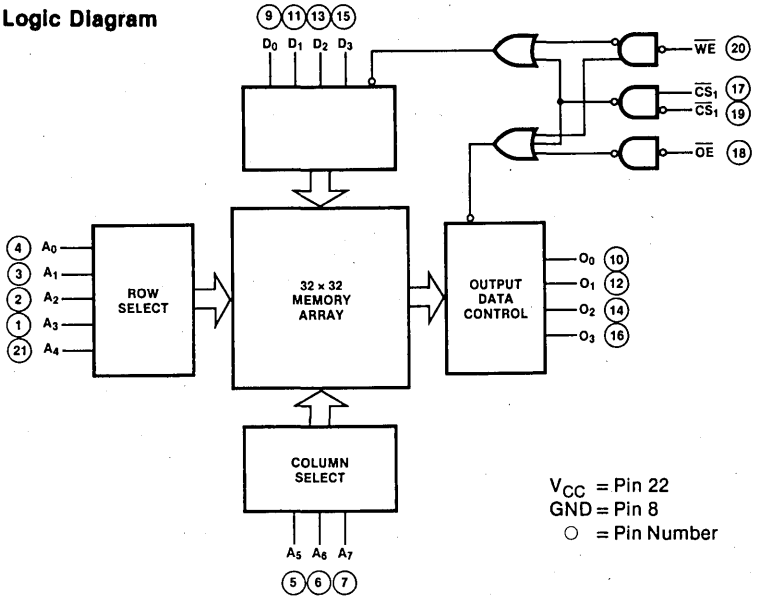
V_{CC} = Pin 20
GND = Pin 10

Connection Diagram
22-Pin DIP



Note
The Flatpak version has the same pinouts (Connection Diagram) as the Dual-in-Line Package.

Logic Diagram



Functional Description

The 93422/92422A is a fully decoded 1024-bit Random Access Memory organized 256 words by four bits. Word selection is achieved by means of an 8-bit address, A_0 through A_7.

Two chip select inputs, inverting and non-inverting, are provided for logic flexibility. For larger memories, the fast chip select access time permits the decoding of chip select, CS, from the address without increasing address access time.

The read and write operations are controlled by the state of the active-LOW write enable, WE (pin 20). With WE held LOW and the chip selected, the data at D_{0-3} is written into the addressed location. To read, WE is held HIGH and the chip selected. Non-inverted data from the specified location is then presented at the output (O_{0-3}).

Truth Table

Inputs					Outputs	
OE Pin 18	CS_0 Pin 19	CS_1 Pin 17	WE Pin 20	D_0-D_3 Pins 9, 11, 13, 15	3-State	Mode
X	H	X	X	X	High Z	Not Selected
X	X	L	X	X	High Z	Not Selected
L	L	H	H	X	O_0-O_3	Read Stored Data
X	L	H	L	L	High Z	Write "0"
X	L	H	L	H	High Z	Write "1"
H	L	H	H	X	High Z	Output Disabled
H	L	H	L	L	High Z	Write "0" (Output Disabled)
H	L	H	L	H	High Z	Write "1" (Output Disabled)

Notes
Pin number specified for DIP only

H = HIGH Voltage
L = LOW Voltage

X = Don't Care (HIGH or LOW)
High Z = High-Impedance.

Guaranteed Operating Ranges

Part Number	Supply Voltage (V_{CC}) Min	Typ	Max	Ambient Temperature Note 4
93422XC, 93422AXC	4.75 V	5.0 V	5.25 V	0°C, +75°C
93422XM	4.50 V	5.0 V	5.50 V	−55°C, +125°C

X = package type; F for Flatpak, D for Ceramic DIP, P for Plastic DIP. See Packaging Information Section for packages available on this product.

DC Characteristics $V_{CC} = 5.0\ V \pm 5\%$, $T_A = 0°C$ to $+75°C$, unless otherwise noted.

Symbol	Characteristic	Min	Typ (Note 3)	Max	Unit	Conditions
V_{OL}	Output LOW Voltage		0.3	0.45	V	V_{CC} = Min, I_{OL} = 8 mA
V_{IH}	Input HIGH Voltage	2.1	1.6		V	Guaranteed Input HIGH Voltage for all Inputs
V_{IL}	Input LOW Voltage		1.5	0.8	V	Guaranteed Input LOW Voltage for all Inputs
I_{IL}	Input LOW Current		−150	−300	μA	V_{CC} = Max, V_{IN} = 0.4 V
I_{IH}	Input HIGH Current		1.0	40 1.0	μA mA	V_{CC} = Max, V_{IN} = 4.5 V V_{CC} = Max, V_{IN} = 5.25 V
V_{CD}	Input Diode Clamp Voltage		−1.0	−1.5	V	V_{CC} = Max, I_{IN} = −10 mA
I_{OFF}	Output Current (High Z)			50 −50	μA	V_{CC} = Max, V_{OUT} = 2.4 V V_{CC} = Max, V_{OUT} = 0.5 V
V_{OH}	Output HIGH Voltage	2.4			V	V_{CC} = Min, I_{OH} = −5.2 mA
I_{OS}	Output Current Short Circuit to Ground			−70	mA	V_{CC} = Max, Note 7
I_{CC}	Power Suply Current 93422XC 93422XC 93422XM 93422XM		95	130 155 120 170	mA	T_A = +75°C T_A = 0°C T_A = +125°C T_A = −55°C V_{CC} = Max, All Inputs and Outputs Open

AC Characteristics Over Guaranteed Operating Ranges (Notes 1, 2, 4, 5, 6)

Symbol	Characteristic	93422AXC Min	93422AXC Max	93422XC Min	93422XC Max	93422AXM Min	93422AXM Max	93422XM Min	93422XM Max	Unit	Conditions
Read Mode	**Delay Times**										
t_{ACS}	Chip Select Time		30		30		35		45	ns	See Test Circuit and Waveforms
t_{ZRCS}	Chip Select to High Z		30		30		35		45	ns	
t_{AOS}	Output Enable Time		30		30		35		45	ns	
t_{ZROS}	Output Enable to High Z		30		30		35		45	ns	
t_{AA}	Address Access Time		35		45		45		60	ns	
Write Mode	**Delay Times**										
t_{ZWS}	Write Disable to High Z		35		35		40		45	ns	See Test Circuit and Waveforms
t_{WR}	Write Recovery Time		35		40		40		50	ns	
Write Mode	**Input Timing Requirements**										
t_W	Write Pulse Width (to guarantee write)	25		30		35		40		ns	
t_{WSD}	Data Set-up Time Prior to Write	5		5		5		5		ns	
t_{WHD}	Data Hold Time After Write	5		5		5		5		ns	
t_{WSA}	Address Set-up Time	5		10		5		10		ns	
t_{WHA}	Address Hold Time	5		5		5		10		ns	
t_{WSCS}	Chip Select Set-up Time	5		5		5		5		ns	
t_{WHCS}	Chip Select Hold Time	5		5		5		10		ns	
C_I	Input Pin Capacitance		5		5		5		5	pF	Measure with Pulse Technique
C_O	Output Pin Capacitance		8		8		8		8	pF	

Notes
1. Conditions for tesing, not shown in the Table, are chosen to guarantee operation under worst case conditions.
2. The specified limits represent the worst case value for the parameters. Since these worst case values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values area at V_{CC} = 5.0 V, T_A = +25°C, and Max loading.
4. The temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute. For military range there is an additional requirement of a two minute warm-up. Temperature range of operation refers to case temperature for flatpaks and ambient temperature for all other packages. Typical thermal resistance values of the package at maximum temperature are:
   θ_{JA} (Junction to Ambient) (at 400 fpm air flow) = 50°C/Watt, Ceramic DIP; 65°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JA} (Junction to Ambient) (still air) = 90°C/Watt, Ceramic DIP; 110°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JC} (Junction to Case) = 25°C/Watt, Ceramic DIP; 25°C/Watt, Plastic DIP; 15°C/Watt, Flatpak.
5. The Max address access time is guaranteed to be the worst case bit in the memory using a pseudo random testing pattern.
6. t_W measured at t_{WSA} = Min, t_{WSA} measured at t_W = Min.
7. Duration of short circuit should not exceed one second.

FAIRCHILD
A Schlumberger Company

93L422/93L422A
256 x 4-Bit Fully Decoded Random Access Memory

TTL Isoplanar Memory

Description

The 93L422/93L422A is a 1024-bit Read/Write Random Access Memory organized 256 words by four bits per word. The 93L422/93L422A has 3-state outputs, and is designed primarily for buffer control storage and high-performance main memory applications. The device has a typical address access time of 45 ns.

- **Isoplanar Technology**
- **Organization — 256 Words x 4 Bits**
- **3-State Outputs**
- **Available in 22-Pin DIP or 24-Pin Flatpak Packages**
- **Inverting and Non-Inverting Chip Select Inputs Provide Easy Memory Expansion**
- **Low Power Dissipation — 0.27 mW/Bit Typical**
- **Typical Read Access Time — 45 ns**

Pin Names

A_0-A_7	Address Inputs
D_0-D_3	Data Inputs
$\overline{CS}_0$, CS_1	Chip Select Inputs
WE	Write Enable Input
O_0-O_3	Data Outputs
OE	Output Enable

Absolute Maximum Ratings

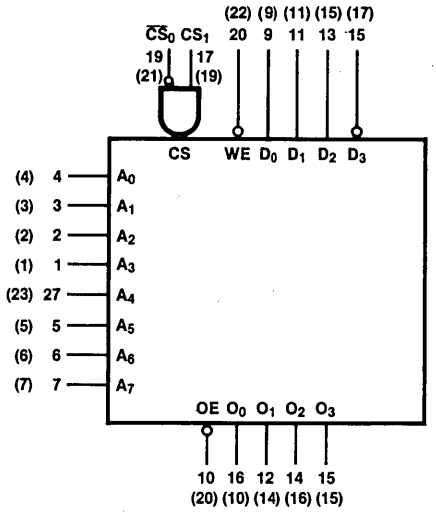
(above which the useful life may be impaired)

Storage Temperature	−65°C, +150°C
Temperature (Ambient) Under Bias	−55°C, +125°C
V_{CC} Lead Potential to Ground Lead	−0.5 V, +7.0 V
Input Voltage (dc)*	−0.5 V, +5.5 V
Input Current (dc)*	−12 mA, +5.0 mA
Voltage Applied to Outputs (output HIGH)**	−0.5 V, +5.50 V
Output Current (dc)	+20 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

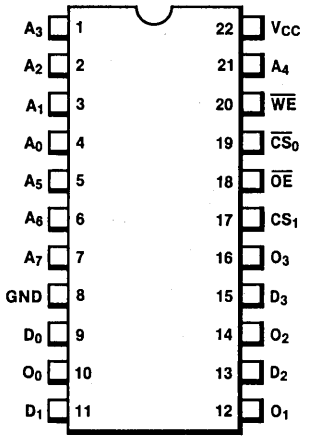
**Output Current Limit Required.

Logic Symbol



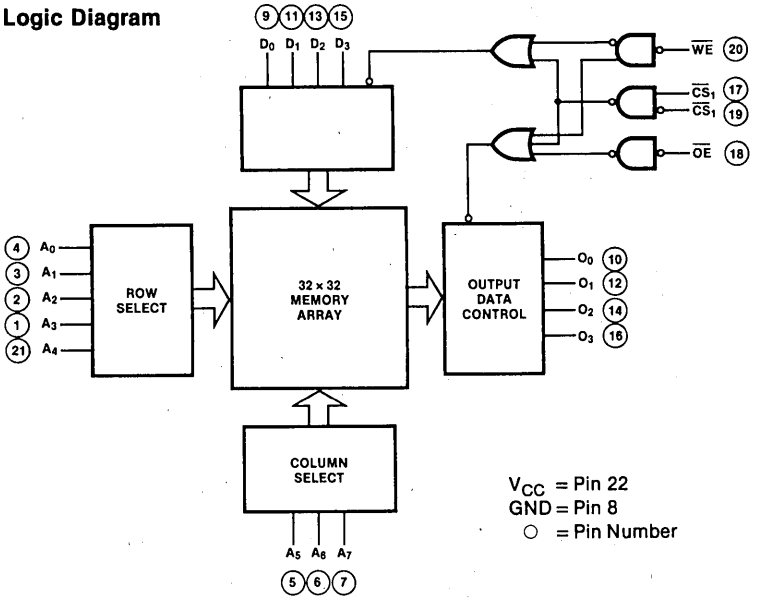
V_{CC} = Pin 20
GND = Pin 10

Connection Diagram
22-Pin DIP



Note
The Flatpak version has the same pinouts (Connection Diagram) as the Dual-in-Line Package.

Logic Diagram



Functional Description

The 93L422/92L422A is a fully decoded 1024-bit Random Access Memory organized 256 words by four bits. Word selection is achieved by means of an 8-bit address, A_0 through A_7.

Two chip select inputs, inverting and non-inverting, are provided for logic flexibility. For larger memories, the fast chip select access time permits the decoding of chip select, CS, from the address without increasing address access time.

The read and write operations are controlled by the state of the active-LOW write enable, WE (pin 20). With WE held LOW and the chip selected, the data at D_{0-3} is written into the addressed location. To read, WE is held HIGH and the chip selected. Non-inverted data from the specified location is then presented at the output (O_{0-3}).

Truth Table

Inputs					Outputs	
OE Pin 18	CS_0 Pin 19	CS_1 Pin 17	WE Pin 20	D_0-D_3 Pins 9, 11, 13, 15	3-State	Mode
X	H	X	X	X	High Z	Not Selected
X	X	L	X	X	High Z	Not Selected
L	L	H	H	X	O_0-O_3	Read Stored Data
X	L	H	L	L	High Z	Write "0"
X	L	H	L	H	High Z	Write "1"
H	L	H	H	X	High Z	Output Disabled
H	L	H	L	L	High Z	Write "0" (Output Disabled)
H	L	H	L	H	High Z	Write "1" (Output Disabled)

Notes
Pin number specified for DIP only

H = HIGH Voltage
L = LOW Voltage

X = Don't Care (HIGH or LOW)
High Z = High-Impedance.

Guaranteed Operating Ranges

Part Number	Supply Voltage (V_{CC})			Ambient Temperature Note 4
	Min	Typ	Max	
93L422XC, 93L422AXC	4.75 V	5.0 V	5.25 V	0°C, +75°C
93L422XM	4.50 V	5.0 V	5.50 V	−55°C, +125°C

X = package type; F for Flatpak, D for Ceramic DIP, P for Plastic DIP.

See Packaging Information Section for packages available on this product.

DC Characteristics $V_{CC} = 5.0\ V \pm 5\%$, $T_A = 0°C$ to $+75°C$, unless otherwise noted.

Symbol	Characteristic	Min	Typ (Note 3)	Max	Unit	Conditions
V_{OL}	Output LOW Voltage		0.3	0.45	V	V_{CC} = Min, I_{OL} = 8 mA
V_{IH}	Input HIGH Voltage	2.1	1.6		V	Guaranteed Input HIGH Voltage for all Inputs
V_{IL}	Input LOW Voltage		1.5	0.8	V	Guaranteed Input LOW Voltage for all Inputs
I_{IL}	Input LOW Current		−150	−300	μA	V_{CC} = Max, V_{IN} = 0.4 V
I_{IH}	Input HIGH Current		1.0	40 1.0	μA mA	V_{CC} = Max, V_{IN} = 4.5 V V_{CC} = Max, V_{IN} = 5.25 V
V_{CD}	Input Diode Clamp Voltage		−1.0	−1.5	V	V_{CC} = Max, I_{IN} = −10 mA
I_{OFF}	Output Current (High Z)			50 −50	μA	V_{CC} = Max, V_{OUT} = 2.4 V V_{CC} = Max, V_{OUT} = 0.5 V
V_{OH}	Output HIGH Voltage	2.4			V	V_{CC} = Min, I_{OH} = 5.2 mA
I_{OS}	Output Current Short Circuit to Ground			−70	mA	V_{CC} = Max, Note 7
I_{CC}	Power Suply Current 93L422XC, 93L422AXC 93L422XC, 93L922AXC 93L422XM 93L422XM		 55 60 50 65	 75 80 70 90	 mA	 T_A = +75°C V_{CC} = Max, T_A = 0°C All Inputs and Outputs Open T_A = +125°C T_A = −55°C

AC Characteristics Over Guaranteed Operating Ranges (Notes 1, 2, 4, 5, 6)

Symbol	Characteristic	93L422AXC Min	93L422AXC Max	93L422XC Min	93L422XC Max	93L422AXM Min	93L422AXM Max	93L422XM Min	93L422XM Max	Unit	Conditions
Read Mode	**Delay Times**										
t_{ACS}	Chip Select Time		30		35		40		45	ns	See Test Circuit and Waveforms
t_{ZRCS}	Chip Select to High Z		30		35		40		45	ns	
t_{AOS}	Output Enable Time		30		35		40		45	ns	
t_{ZROS}	Output Enable to High Z		30		35		40		45	ns	
t_{AA}	Address Access Time		45		60		55		75	ns	
Write Mode	**Delay Times**										
t_{ZWS}	Write Disable to High Z		35		40		45		45	ns	See Test Circuit and Waveforms
t_{WR}	Write Recovery Time		40		45		50		50	ns	
Write Mode	**Input Timing Requirements**										
t_W	Write Pulse Width (to guarantee write)	30		45		40		55		ns	
t_{WSD}	Data Set-up Time Prior to Write	5		5		10		5		ns	
t_{WHD}	Data Hold Time After Write	5		5		5		5		ns	
t_{WSA}	Address Set-up Time	10		10		10		10		ns	
t_{WHA}	Address Hold Time	5		5		5		10		ns	
t_{WSCS}	Chip Select Set-up Time	5		5		10		5		ns	
t_{WHCS}	Chip Select Hold Time	5		5		5		10		ns	
C_I	Input Pin Capacitance		5		5		5		5	pF	Measure with Pulse Technique
C_O	Output Pin Capacitance		8		8		8		8	pF	

Notes:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified Limits represents the "worst case" value for the parameters. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are at V_{CC} = 5.0 V, T_A = 25°C, and Max loading.
4. The Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute. Temperature range of operation refers to case temperature for Flatpaks and ambient temperature for all other packages. Typical thermal resistance values of the package at maximum temperature are:
   θ_{JA} (Junction to Ambient) (at 400 fpm air flow) = 50°C/Watt, Ceramic DIP; 65°C/Watt, Plastic DIP.
   θ_{JA} (Junction to Ambient) (still air) = 90°C/Watt, Ceramic DIP; 110°C/Watt, Plastic DIP.
   θ_{JC} (Junction to Case) = 25°C/Watt, Ceramic DIP; 25°C/Watt, Plastic DIP; 15°C/Watt, Flatpak.
5. The Max address access time is guaranteed to be the "worst case" bit in the memory using a pseudo random testing pattern.
6. tw measured at t_{WSA} = Min, t_{WSA} measured at tw = Min.
7. Duration of short circuit should not exceed one second.

FAIRCHILD
A Schlumberger Company

93415/93425
1024 X 1-Bit Static Random Access Memory

TTL Bipolar Memory

Description

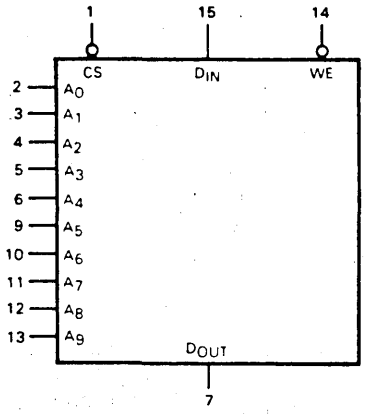
The 93415 and 93425 are 1024-bit read/write Random Access Memories (RAMs), organized 1024 words by one bit. The devices are identical except the 93415 has open collector outputs while the 93425 has three state outputs. They are designed for high speed scratchpad, control and buffer storage applications. Both devices are available in two speed versions, standard speed and 'A' grade. The devices include full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as an Active-LOW Chip Select line.

- **Address Access Time**
  93415/93425 — 45ns Max
  93415A/934245A — 30ns Max
- **Chip Select Access Time**
  93415/93425 — 35ns Max
  93415A/93425A — 20ns Max
- **Fully TTL Compatible**
- **Available with Open Collector (93415) or Three State (93425) Outputs**
- **Power Dissipation — 0.5mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

Pin Names

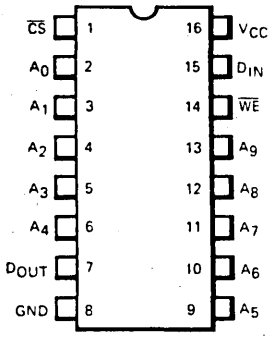
$\overline{CS}$	Active-LOW Chip Select
A_0-A_9	Address Inputs
$\overline{WE}$	Active-LOW Write Enable
D	Data Input
O	Data Output

Logic Symbol



Connection Diagrams

DIP (Top View)



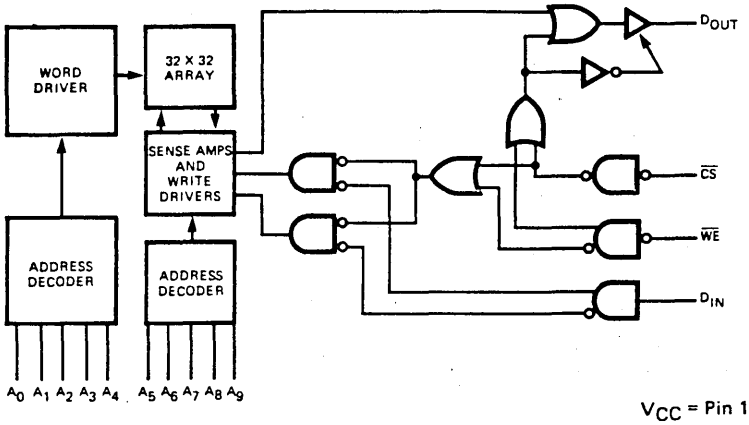
Note:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

Truth Table

Inputs			Outputs		
$\overline{CS}$	$\overline{WE}$	D_{IN}	93415 O.C.	93425 3-State	Mode
H	X	X	H	HIGH Z	Not Selected
L	L	L	H	HIGH Z	Write "0"
L	L	H	H	HIGH Z	Write "1"
L	H	X	D_{OUT}	D_{OUT}	Read

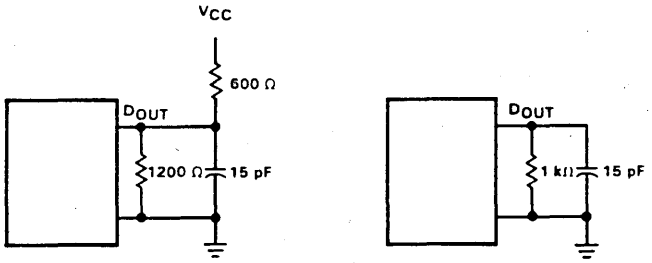
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care (HIGH or LOW)

Logic Diagram



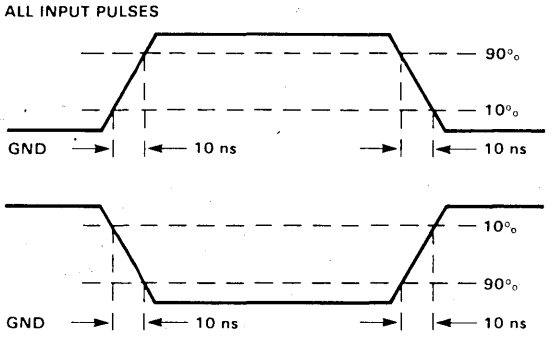
V_{CC} = Pin 16
GND = Pin 8

AC Test Loads and Waveforms



Load A **Load B**

Loading Conditions



Input Pulses

Functional Description

The 93415 and 93425 are fully decoded 1024-bit Random Access Memories organized 1024 words by one bit. Word selection is achieved by means of a 10-bit address, A_0 through A_9.

One Chip Select input is provided for logic flexibility or for memory array expansion up to 2048 words without the need for external decoding. For larger memories, the fast chip select time permits the decoding of Chip Select, ($\overline{CS}$) from the address without affecting system performance.

The read and write operations are controlled by the state of the active-LOW Write Enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW and the chip selected, the data at D is written into the addressed location. Since the write function is level triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the chip selected. Non-inverted data is then presented at the output (O).

The output of the 93415 is an open collector and is designed for use in wired-OR applicatoins. The 93425 has a three state output for use in bus organized systems.

DC Characteristics: Over Operating Temperature Ranges (Notes 1-4)

Symbol	Characteristic	Limits Min	Typ (Note 3)	Max	Units	Conditions
V_{OL}	Output LOW Voltage		0.3	0.45	V	V_{CC} = Min, I_{OL} = 16 mA
V_{IH}	Input HIGH Voltage	2.1	1.6		V	Guaranteed Input HIGH Voltage for all Inputs
V_{IL}	Input LOW Voltage		1.5	0.8	V	Guaranteed Input LOW Voltage for all Inputs
I_{IL}	Input LOW Current		−250	−400	μA	V_{CC} = Max, V_{IN} = 0.4 V
I_{IH}	Input HIGH Current		1.0	40 1.0	μA mA	V_{CC} = Max, V_{in} = 4.5 V V_{CC} = Max, V_{IN} = 5.25 V
I_{OFF}	Output Current (HIGH Z) 93425			50 −50	μA	V_{CC} = Max, V_{OUT} = 2.4 V V_{CC} = Max, V_{OUT} = 0.5 V
I_{OS}	Output Current Short Circuit to Ground 93425			−100	mA	V_{CC} = Max, Note 7
V_{OH}	Output HIGH Voltage 93424XC 93425XM	2.4			V	I_{OH} = −10.3 mA, V_{CC} = 5.0 V ±5% I_{OH} = −5.2 mA
I_{CEX}	Output Leakage Current 93415		1.0	100	μA	V_{CC} = Max, V_{OUT} = 4.5 V
V_{CD}	Input Diode Clamp Voltage		−1.0	−1.5	V	V_{CC} = Max, I_{IN} = −10 mA
I_{CC}	Power Supply Current		95	130 155 170	mA	T_A = 75°C T_A = 0°C T_A = −55°C V_{CC} = Max, All Inputs Grounded

AC Characteristics: Over Guaranteed Operating Ranges (Notes 1, 2, 4, 5, 6)

Symbol	Characteristic	93415/425AXC Min	Typ	Max	93415/425XC Min	Typ	Max	93415/425XM Min	Typ	Max	Units	Conditions
	Read Mode Delay Times											
t_{ACS}	Chip Select Access Time			20			35			45	ns	See Test Circuit and Waveforms
t_{RCS}	Chip Select Recovery Time 93415			20			35			50		
t_{ZRCS}	Chip Select to HIGH Z 93425			20			35			50		
t_{AA}	Address Access Time			30			45			60		
	Write Mode Delay Times											
t_{ZWS}	Write Disable to HIGH Z			20			35			45	ns	See Test Circuit and Waveforms
t_{WR}	Write Recovery Time			25			40			50		
	Write Mode Timing Requirements											
t_W	Write Pulse Width (to guarantee write)	30			35			40			ns	See Test Circuit and Waveforms
t_{WSD}	Data Setup Time Prior to Write	5			5			5				
t_{WHD}	Data Hold Time After Write	5			5			5				
t_{WSA}	Address Setup Time	5			5			15				
t_{WHA}	Address Hold Time	5			5			5				
t_{WSCS}	Chip Select Setup Time	5			5			5				
t_{WHCS}	Chip Select Hold Time	5			5			5				
C_I	Input Pin Capacitance		4	5		4	5		4	5	pF	Measure with Pulse Technique
C_O	Output Pin Capacitance		7	8		7	8		7	8		

Notes:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified Limits represents the "worst case" value for the parameters. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are at V_{CC} = 5.0 V, T_A = 25°C, and Max loading.
4. The Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute. Typical thermal resistance values of the package at maximum temperature are:

   θ_{JA} (Junction to Ambient) (at 400 fpm air flow) = 50°C/Watt, Ceramic DIP; 65°C/Watt, Plastic DIP.
   θ_{JA} (Junction to Ambient) (still air) = 90°C/Watt, Ceramic DIP; 110°C/Watt, Plastic DIP.
   θ_{JC} (Junction to Case) = 25°C/Watt, Ceramic DIP; 25°C/Watt, Plastic DIP; 15°C/Watt, Flatpak.

5. The Max address access time is guaranteed to be the "worst case" bit in the memory using a pseudo random testing pattern.
6. t_W measured at t_{WSA} = Min, t_{WSA} measured at t_W = Min.
7. Duration of short circuit should not exceed one second.

FAIRCHILD
A Schlumberger Company

93471
4096 X 1-Bit Static Random Access Memory

TTL Bipolar Memory

Description

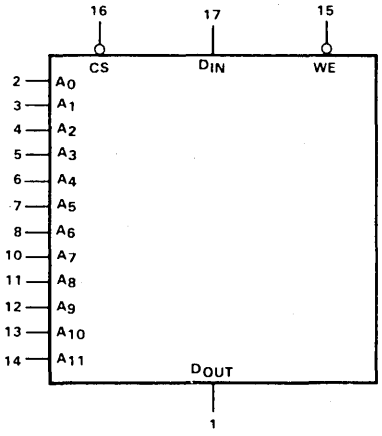
The 93471 is a 4096-bit read/write Random Access Memory (RAM), organized 4096 words by one bit. It is designed for high speed scratchpad, control and buffer storage applications. The 93471 is available in two speed versions, standard speed and 'A' grade. The device includes full on-chip address decoding, separate Data inputs and non-inverting Data outputs, as well as an Active-LOW Chip Select line.

- **Address Access Time — 45ns Max**
- **Chip Select Access Time — 30ns Max**
- **Fully TTL Compatible**
- **Features Three State Outputs**
- **Power Dissipation — 0.15mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

Pin Names

$\overline{CS}$	Chip Select
A_0-A_{11}	Address Inputs
$\overline{WE}$	Write Enable
D	Data Input
O	Data Output

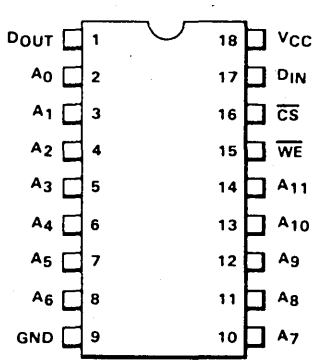
Logic Symbol



V_{CC} = Pin 18
GND = Pin 9

Connection Diagram

DIP (Top View)

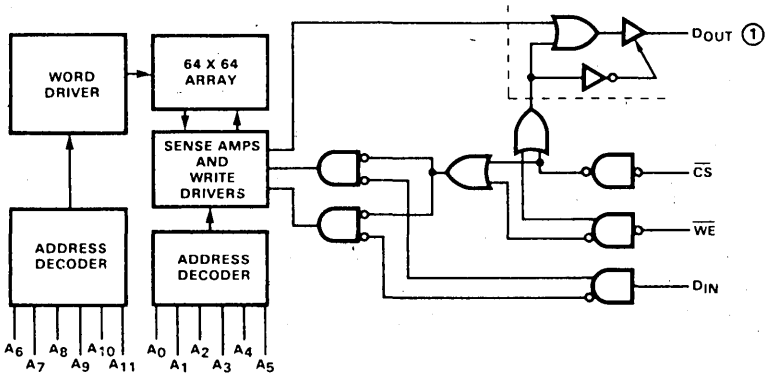


Truth Table

Inputs			Outputs	
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	Mode
H	X	X	HIGH Z	Not Selected
L	L	L	HIGH Z	Write "0"
L	L	H	HIGH Z	Write "1"
L	H	X	D_{OUT}	Read

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care (HIGH or LOW)

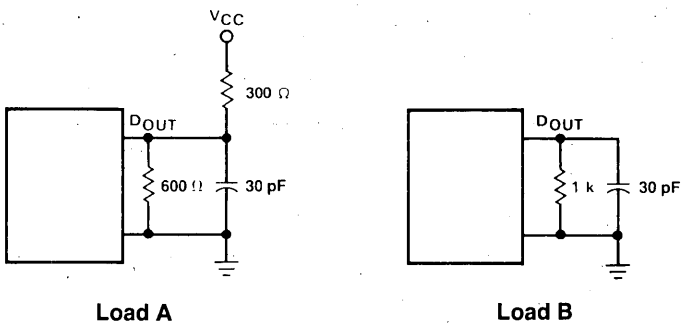
Logic Diagram



V_{CC} = Pin 18
GND = Pin 9

AC Test Loads and Waveforms

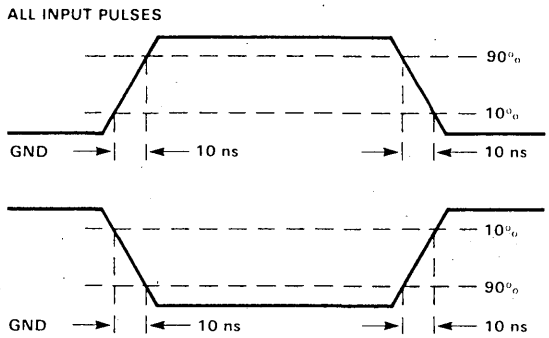
Loading Conditions



Load A

Load B

Input Pulses



Functional Description

The 93471 is a fully decoded 4096-bit Random Access Memory organized 4096 words by one bit. Word selection is achieved by means of a 12-bit address, A_0 through A_{11}.

One Chip Select input is provided for logic flexibility and for memory array expansion up to 8192 bits without the need for external decoding. For larger memories, the fast chip select time permits the decoding of Chip Select, ($\overline{CS}$) from the address without affecting system performance.

The read and write operations are controlled by the state of the active-LOW Write Enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW and the chip selected, the data at D is written into the addressed location. Since the write function is level triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the chip selected. Non-inverted data is then presented at the output (O).

The 93471 has a three state output for use in bus organized systems.

DC Characteristics: Over Operating Temperature Ranges (Notes 1-4)

Symbol	Characteristic	Limits Min	Limits Typ (Note 3)	Limits Max	Units	Conditions	
V_{OL}	Output LOW Voltage		0.3	0.50	V	V_{CC} = Min, I_{OL} = 16 mA	
V_{IH}	Input HIGH Voltage	2.1	1.6		V	Guaranteed Input HIGH Voltage for all Inputs	
V_{IL}	Input LOW Voltage		1.5	0.8	V	Guaranteed Input LOW Voltage for all Inputs	
I_{IL}	Input LOW Current		−250	−400	μA	V_{CC} = Max, V_{IN} = 0.4 V	
I_{IH}	Input HIGH Current		1.0	40 1.0	μA mA	V_{CC} = Max, V_{in} = 4.5 V V_{CC} = Max, V_{IN} = 5.25 V	
V_{CD}	Input Diode Clamp Voltage		−1.0	−1.5	V	V_{CC} = Max, I_{IN} = −10 mA	
I_{OFF}	Output Current (HIGH Z)			50 −50	μA	V_{CC} = Max, V_{OUT} = 2.4 V V_{CC} = Max, V_{OUT} = 0.5 V	
V_{OH}	Output HIGH Voltage	2.4			V	V_{CC} = Min, I_{OH} = −5.2 mA	
I_{OS}	Output Current Short Circuit to Ground			−100	mA	V_{CC} = Max, Note 7	
I_{CC}	Power Supply Current		110 130 100 140	170 180	mA	T_A = 75°C T_A = 0°C T_A = 125°C T_A = −55°C	V_{CC} = Max, All Inputs and Outputs Open

AC Characteristics: Over Guaranteed Operating Ranges (Notes 1-6)

Symbol	Characteristic	93471XC Min	93471XC Typ (Note 3)	93471XC Max	93471XM Min	93471XM Typ (Note 3)	93471XM Max	Units	Conditions
	Read Mode Delay Times								
t_{ACS}	Chip Select Access Time			30			35	ns	See Test Circuit and Waveforms
t_{ZWS}	Write Disable to HIGH Z			35			45		
t_{WR}	Write Recovery Time			35			45		
t_{AA}	Address Access Time			45			60		
	Write Mode Timing Requirements								
t_W	Write Pulse Width (to guarantee write)	30			45			ns	See Test Circuit and Waveforms
t_{WSD}	Data Setup Time Prior to Write	10			15				
t_{WHD}	Data Hold Time After Write	5			10				
t_{WSA}	Address Setup Time	10			15				
t_{WHA}	Address Hold Time	5			10				
t_{WSCS}	Chip Select Setup Time	5			10				
t_{WHCS}	Chip Select Hold Time	5			10				
C_I	Input Pin Capacitance		4	5		4	5	pF	Measure with Pulse Technique
C_O	Output Pin Capacitance		7	8		7	8		

Notes:

1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified Limits represents the "worst case" value for the parameters. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are at V_{CC} = 5.0 V, T_A = 25°C, and Max loading.
4. The Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute. Temperature range of operation refers to case temperature for Flatpaks and ambient temperature for all other packages. Typical thermal resistance values of the package at maximum temperature are:

   θ_{JA} (Junction to Ambient) (at 400 fpm air flow) = 50°C/Watt, Ceramic DIP; 65°C/Watt, Plastic DIP.
   θ_{JA} (Junction to Ambient) (still air) = 90°C/Watt, Ceramic DIP; 110°C/Watt, Plastic DIP.
   θ_{JC} (Junction to Case) = 25°C/Watt, Ceramic DIP; 25°C/Watt, Plastic DIP; 15°C/Watt, Flatpak.

5. The Max address access time is guaranteed to be the "worst case" bit in the memory using a pseudo random testing pattern.
6. t_W measured at t_{WSA} = Min, t_{WSA} measured at t_W = Min.
7. Duration of short circuit should not exceed one second.

FAIRCHILD
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93475
1024 X 4-Bit Static Random Access Memory

TTL Bipolar Memory

Description

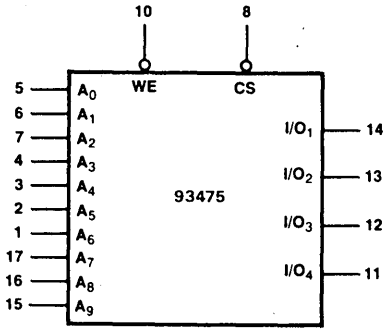
The 93475 is a 4096-bit read/write Random Access Memory (RAM), organized 1024 words by four bits per word. It is designed for high speed scratchpad, control and buffer storage applications. The device includes full on-chip address decoding, common Data input/outputs, as well as an Active-LOW Chip Select line.

- **Address Access Time — 45ns Max**
- **Chip Select Access Time — 35ns Max**
- **Features Three State Outputs**
- **Common Data I/O's**
- **Industry standard 2114 Pinout**
- **Power Dissipation — 0.16mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

Pin Names

A_0–A_9	Address Inputs
$\overline{CS}$	Active-LOW Chip Select
$\overline{WE}$	Active-LOW Write Enable
I/O_1–I/O_4	Data Input/Outputs

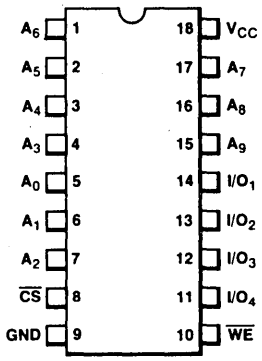
Logic Symbol



V_{CC} = Pin 18
GND = Pin 9

Connection Diagram

DIP (Top View)

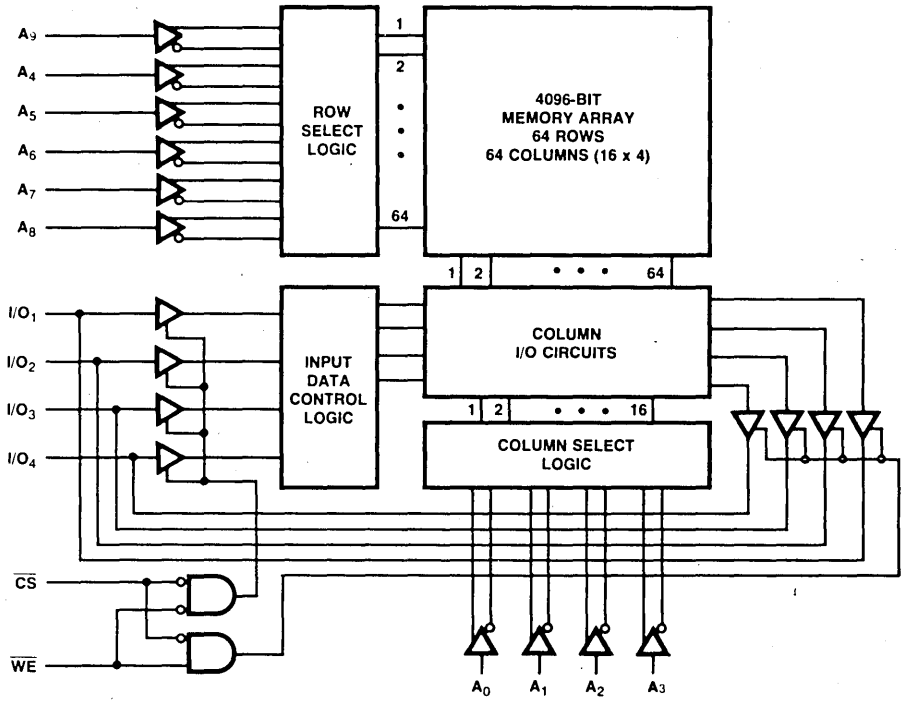


Note
Flatpak version has the same pinouts (Connection Diagram) as the Dual.

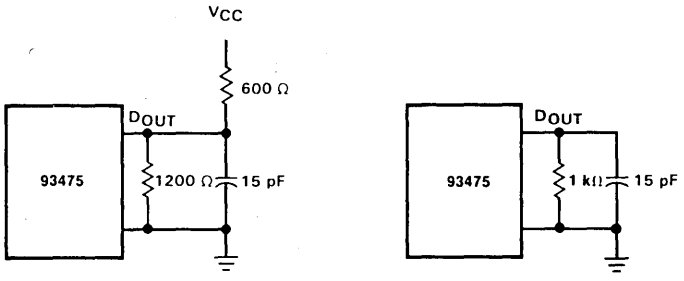
Truth Table

Inputs			
$\overline{CS}$	$\overline{WE}$	I/O_1–I/O_4	Mode
H	X	HIGH Z	Not Selected
L	H	D_{OUT}	Read
L	L	D_{IN} HIGH Z	Write

Block Diagram

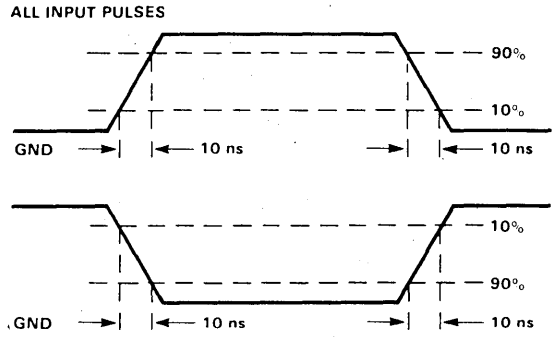


AC Test Loads and Waveforms



Load A Load B

Loading Conditions



Input Pulses

Functional Description

The 93475 is a fully decoded 4096-bit Random Access Memory organized 1024 words by four bits per word. Word selection is achieved by means of a 10-bit address, A_0 through A_9.

One Chip Select input is provided for logic flexibility or for memory array expansion up to 8192 words without the need for external decoding. For larger memories, the fast chip select time permits the decoding of Chip Select, ($\overline{CS}$) from the address without affecting system performance.

The read and write operations are controlled by the state of the active-LOW Write Enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW and the chip selected, the data at I/O_1 through I/O_4 is written into the addressed locations. Since the write function is level triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the chip selected. Non-inverted data is then presented at the outputs (I/O_1 through I/O_4).

The 93475 has three state outputs for use in bus organized systems.

DC Characteristics: Over Operating Temperature Ranges (Notes 1-4)

Symbol	Characteristic	Limits Min	Limits Typ (Note 3)	Limits Max	Units	Conditions	
V_{OL}	Output LOW Voltage		0.35	0.45	V	V_{CC} = Min, I_{OL} = 8 mA	
V_{IH}	Input HIGH Voltage	2.1	1.6		V	Guaranteed Input HIGH Voltage for all Inputs	
V_{IL}	Input LOW Voltage		1.5	0.8	V	Guaranteed Input LOW Voltage for all Inputs	
I_{IL}	Input LOW Current		−250	−400	μA	V_{CC} = Max, V_{IN} = 0.4 V	
I_{IH}	Input HIGH Current		1.0	40 1.0	μA mA	V_{CC} = Max, V_{in} = 4.5 V V_{CC} = Max, V_{IN} = 5.25 V	
V_{CD}	Input Diode Clamp Voltage		−1.0	−1.5	V	V_{CC} = Max, I_{IN} = −10 mA	
I_{OFF}	Output Current (HIGH Z)			50 −400	μA	V_{CC} = Max, V_{OUT} = 2.4 V V_{CC} = Max, V_{OUT} = 0.5 V	
V_{OH}	Output HIGH Voltage	2.4			V	V_{CC} = Min, I_{OH} = −5.2 mA	
I_{OS}	Output Current Short Circuit to Ground			−100	mA	V_{CC} = Max, Note 7	
I_{CC}	Power Supply Current		140 140	170 185	mA	T_A = 0°C T_A = −55°C	V_{CC} = Max, All Inputs and Outputs Open

AC Characteristics: Over Guaranteed Operating Ranges (Notes 1-6)

Symbol	Characteristic	93475XC Min	93475XC Typ (Note 3)	93475XC Max	93475XM Min	93475XM Typ (Note 3)	93475XM Max	Units	Conditions
	Read Mode Delay Times								
t_{ACS}	Chip Select Access Time		20			20			
t_{ZRCS}	Chip Select to HIGH Z		20			20		ns	See Test Circuit
t_{AA}	Address Access Time			45			60		
	Write Mode Delay Times								
t_{SW}	Write Setup Time Prior to Chip Select Write		5			5		ns	See Test Circuit and Waveforms
t_{ZWS}	Write Disable to HIGH Z		20			25			
	Write Mode Timing Requirements								
t_{WH}	Write Enable Hold Time After Chip Deselect		0			0			
t_W	Write Pulse Width (to guarantee write)		20			35			
t_{CSW}	Chip Select Write Pulse Width (Optional Write Mode)		15			25		ns	See Test Circuit and Waveforms
t_{WSD}	Data Setup Time Prior to Write		20			25			
t_{WHD}	Data Hold Time After Write		0			0			
t_{WSA}	Address Setup Time		0			0			
t_{WHA}	Address Hold Time		0			0			
C_I	Input Pin Capacitance		4	5		4	5	pF	Measure with Pulse Technique
C_O	Output Pin Capacitance		7	8		7	8		

Notes:

1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified Limits represents the "worst case" value for the parameters. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are at V_{CC} = 5.0 V, T_A = 25°C, and Max loading.
4. The Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute. Temperature range of operation refers to case temperature for Flatpaks and ambient temperature for all other packages. Typical thermal resistance values of the package at maximum temperature are:

   θ_{JA} (Junction to Ambient) (at 400 fpm air flow) = 50°C/Watt, Ceramic DIP; 65°C/Watt, Plastic DIP.
   θ_{JA} (Junction to Ambient) (still air) = 90°C/Watt, Ceramic DIP; 110°C/Watt, Plastic DIP.
   θ_{JC} (Junction to Case) = 25°C/Watt, Ceramic DIP; 25°C/Watt, Plastic DIP; 15°C/Watt, Flatpak.

5. The Max address access time is guaranteed to be the "worst case" bit in the memory using a pseudo random testing pattern.
6. t_W measured at t_{WSA} = Min, t_{WSA} measured at t_W = Min.
7. Duration of short circuit should not exceed one second.

FAIRCHILD
A Schlumberger Company

93479
256 x 9-Bit Fully Decoded Random Access Memory

TTL Isoplanar Memory

Description

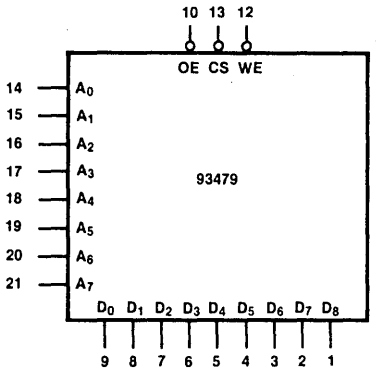
The 93479 is a 2304-Bit Read/Write Random Access Memory organized as 256 words by nine bits per word. It is ideally suited for scratchpad, small buffer and other applications where the number of required words is small and where the number of required bits per word is relatively large. The ninth bit can be used to provide parity for 8-bit word systems.

- **Isoplanar Technology**
- **Organization—256 Words by Nine Bits**
- **3-State Outputs**
- **Standard 22-Pin Dual In-Line Package**
- **TTL Inputs and Outputs**
- **Common Data Input/Output**
- **Power Dissipation—0.29 mW/Bit**
- **Maximum Address Access Time—45 ns**
- **Maximum Chip Select Access Time—25 ns**

Pin Names

A_0-A_7	Address Inputs
D_0-D_8	Data Inputs/Outputs
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input

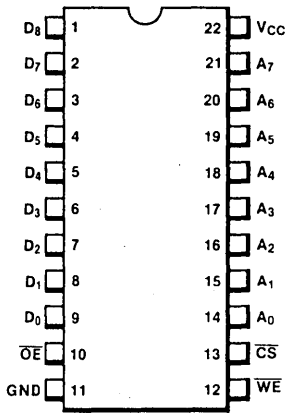
Logic Symbol



V_{CC} = Pin 22
GND = Pin 11

Connection Diagram

22-Pin DIP



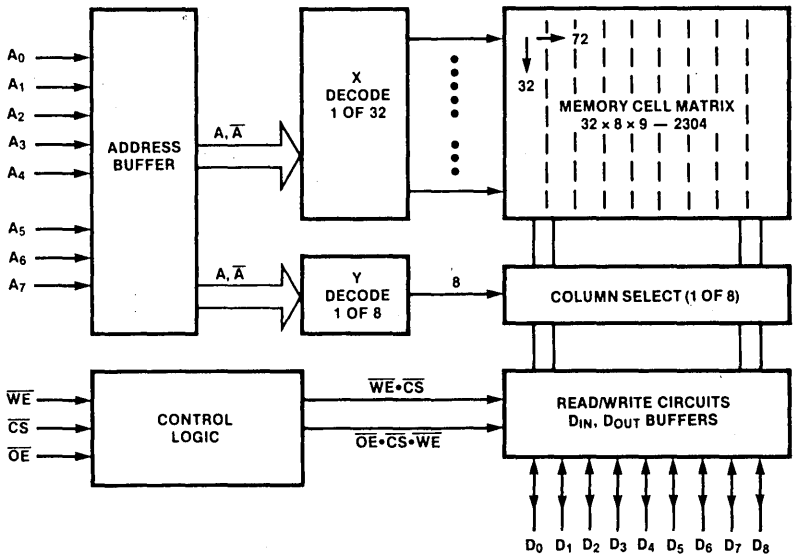
(Top View)

Truth Table

Inputs $\overline{CS}$	Inputs $\overline{OE}$	Inputs $\overline{WE}$	$Data_{In/Out}$ D_0-D_8	Mode
H	X	X	High Z	Not Selected
L	H	H	High Z	Read, o/p Disabled
L	H	L	Data In	Write, o/p Disabled
L	L	H	Data	Read
L	L	L	Data In	Write

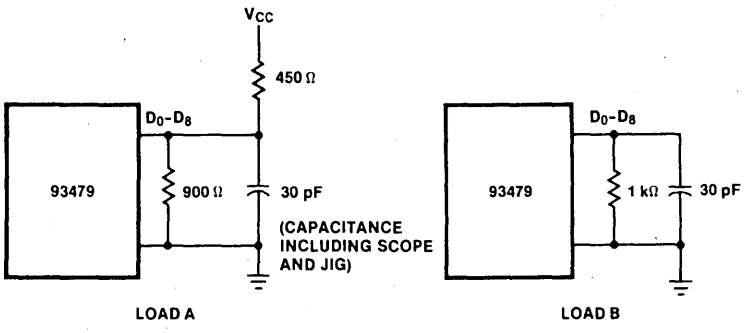
H = HIGH State
L = LOW State
X = Don't Care (HIGH or LOW)
High Z = High-Impedance State
Data = Previously Stored Output Data

Logic Diagram

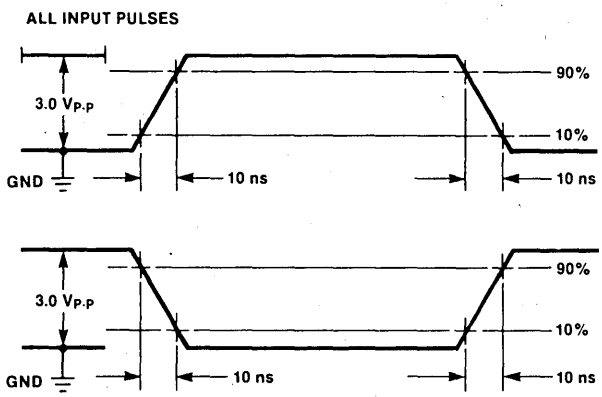


AC Test Loads and Waveforms

Loading Condition



Input Pulses



Functional Description

The 93479 is a fully decoded 2304-bit Random Access Memory organized 256 words by nine bits. Word selection is achieved by means of an 8-bit address, A_0 to A_7.

The chip select input provides for memory array expansion. For large memories, the fast chip select access time permits the decoding of chip select ($\overline{CS}$) from the address without affecting system performance.

The read and write operations are controlled by the state of the active-LOW write enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW, the chip selected, and the output disabled, the data at D_0-D_8 is written into the addressed location.

Since the write function is level-triggered, data must be held stable for at least t_{WSD} (min) plus t_W (min) to insure a valid write. To read, $\overline{WE}$ is held HIGH, the chip selected, and the output enabled. Non-inverted data is then presented at the outputs (D_0-D_8).

The 3-state output provides high-speed drive capability for high capacitive load systems. The third state (high-impedance) allows bus-organized systems where multiple outputs are connected to a common bus.

AC Characteristics Over Guaranteed Operating Ranges (Notes 1, 2, 4, 5, 6)

Symbol	Characteristic	93479XC Min	93479XC Max	Unit	Conditions
Read Mode	**Delay Times**				
t_{ACS}	Chip Select Time		25	ns	See Test Circuit and Waveforms
t_{ZRCS}	Chip Select to High Z		25	ns	
t_{AOS}	Output Enable Time		25	ns	
t_{ZROS}	Output Enable to High Z		25	ns	
t_{AA}	Address Access Time		45	ns	
Write Mode	**Delay Times**				
t_{ZWS}	Write Disable to High Z		25	ns	See Test Circuit and Waveforms
	Input Timing Requirements				
t_W	Write Pulse Width (to guarantee write)	25		ns	
t_{SO}	Output Enable Set-up Time	5		ns	
t_{HO}	Output Enable Hold Time	5		ns	
t_{WSD}	Data Set-up Time Prior to Write	25		ns	
t_{WHD}	Data Hold Time After Write	5		ns	
t_{WSA}	Address Set-up Time	5		ns	
t_{WHA}	Address Hold Time	5		ns	
t_{WSCS}	Chip Select Set-up Time	5		ns	
t_{WHCS}	Chip Select Hold Time	5		ns	
C_{IN}	Input Pin Capacitance		5	pF	
C_{OUT}	Output Pin Capacitance		8	pF	

DC Characteristics Over Guaranteed Operating Ranges (Notes 1, 2, 4)

Symbol	Characteristic	Min	Typ (Note 3)	Max	Unit	Conditions
V_{OL}	Output LOW Voltage		0.3	0.50	V	V_{CC} = Min, I_{OL} = 9.6 mA
V_{OH}	Output HIGH Voltage	2.4			V	V_{CC} = Min, I_{OH} = −5.2mA
V_{IH}	Input HIGH Voltage	2.1	1.6		V	Guaranteed Input HIGH Voltage for all Inputs
V_{IL}	Input LOW Voltage		1.5	0.8	V	Guaranteed Input LOW Voltage for all Inputs
I_{IL}	Input LOW Current		−250	−400	μA	V_{CC} = Max, V_{IN} = 0.4 V
I_{IH}	Input HIGH Current		1.0	40 1.0	μA mA	V_{CC} = Max, V_{IN} = 4.5 V V_{CC} = Max, V_{IN} = 5.25 V
I_{off}	Output Current (High Z)			50 −400	μA	V_{CC} = Max, V_{OUT} = 2.4 V V_{CC} = Max, V_{OUT} = 0.5 V
V_{CD}	Input Diode Clamp Voltage		−1.0	−1.5	V	V_{CC} = Max, I_{IN} = −10 mA
I_{CC}	Power Supply Current			165	mA	$T_A \geq 75°C$; V_{CC} = Max, All Inputs Grounded, Outputs LOW
			135	185	mA	$T_A = 0°C$; V_{CC} = Max, All Inputs Grounded, Outputs LOW
I_{OS}	Output Current Short Circuit to Ground			−70	mA	V_{CC} = Max, Note 7

Notes

1. Conditions for testing not shown in the Table are chosen to guarantee operation under worst case conditions.
2. The specified limits represent the worst case value for the parameters. Since these worst case values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are at V_{CC} = 5.0 V, T_A = +25°C, and Max loading.
4. The temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a two minute warm-up. Temperature range of operation refers to case temperature for flatpaks and ambient temperature for all other packages. Typical thermal resistance values of the package at maximum temperature are:
   θ_{JA} (Junction to Ambient) (at 400 fpm air flow) = 30°C/Watt, Ceramic DIP
   θ_{JA} (Junction to Ambient) (still air) = 60°C/Watt, Ceramic DIP
   θ_{JC} (Junction to Case) = 12°C/Watt, Ceramic DIP
5. The Max address access time is guaranteed to be the worst case bit in the memory using a pseudo random testing pattern.
6. t_W measured at t_{WSA} = Min, t_{WSA} measured at t_W = Min.
7. Duration of short circuit should not exceed one second.

FAIRCHILD
A Schlumberger Company

93Z450/93Z451
1024 X 8-Bit Programmable Read Only Memory

Isoplanar-Z Junction Fuse TTL Memory

Description

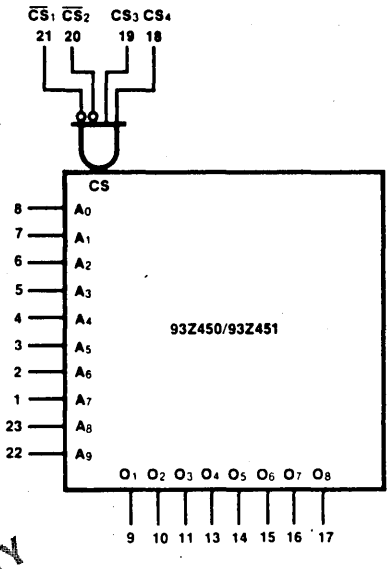
The 93Z450 and 93Z451 are fully decoded 8,192-bit Programmable Read Only Memories (PROMs), organized 1024 words by eight bits per word. The two devices are identical except the 93Z450 has open collector outputs while the 93Z451 has three state outputs. Both devices are available in two speed versions, standard speed and 'A' grade.

The 93Z450 and 93Z451 use open base transistor (junction) fuse cells. Initially the unprogrammed cell is in the logic '0' state. The cell can be programmed to a logic '1' state by following the specified programming procedure which fuses aluminum through the emitter base junction of the cell transistor.

- **Address Access Time**
  93Z450/93Z451 — 45ns Max
  93Z450A/93Z451A — 35ns Max
- **Chip Select Access Time**
  93Z450/93Z451 — 30ns Max
  93Z450A/93Z451A — 25ns Max
- **Fully TTL Compatible**
- **Highly Reliable Vertical Fuses**
- **Available with Open Collector (93Z450) or Three State (93Z451) Outputs**
- **Low Current PNP Inputs**
- **Power Dissipation — 58μW/Bit Typ**

PRELIMINARY

Logic Symbol



V_{CC} = Pin 24
GND = Pin 12

Pin Names

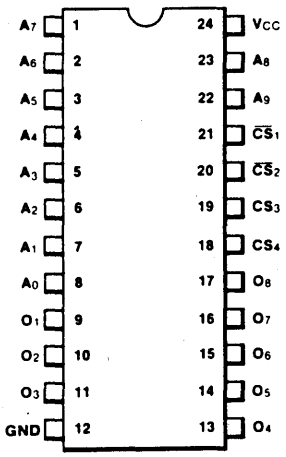
A_0-A_9	Address Inputs
$\overline{CS}_1$, $\overline{CS}_2$, CS_3, CS_4	Chip Select Inputs
O_1-O_8	Data Outputs

Absolute Maximum Ratings

Storage Temperature	-65°C to +150°C
Temperature (Ambient) under Bias	-55°C to +125°C
V_{CC}	-0.5 V to +7.0 V
Input Voltage	-0.5 V to +5.5 V
Current into Output Terminal	100 mA
Output Voltages	-0.5 V to +5.5 V

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

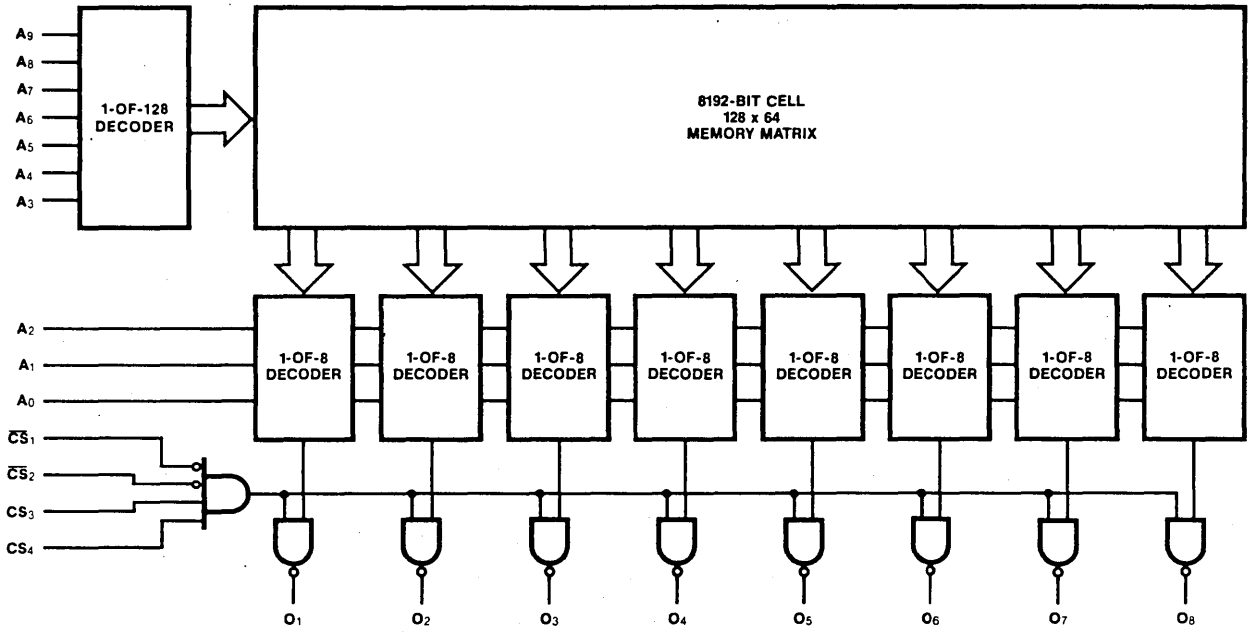
Connection Diagram
24-Pin DIP



(Top View)

Note
The Flatpak version has the same pinouts (Connection Diagram) as Dual In-line Package.

Logic Diagram



Functional Description

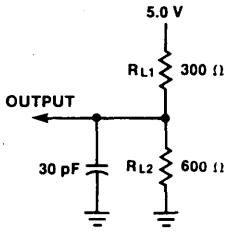
The 93Z450 and 93Z451 are TTL Bipolar field Programmable Read Only Memories (PROMs) organized 1024 words by eight bits per word. Open-collector outputs are provided on the 93Z450 for use in wired-OR systems. The 93Z451 has 3-state outputs which provide active pull ups when enabled and high output impedance when disabled. This allows optimization of word expansion in bus organized systems.

Four chip select inputs are provided to allow memory expansion of up to 128K without the need for external decoding. Either device is enabled only when $\overline{CS}_1$ and $\overline{CS}_2$ are LOW and CS_3 and CS_4 are HIGH.

Programming, which is accomplished by selectively shorting fuse junctions, is outlined in the following section.

The read function is identical to that of a conventional Read Only Memory (ROM). A binary address is applied to the address pins A_0 through A_9, the chip is selected and data is available at the outputs after t_{AA}.

AC Test Output Load



Test Conditions
Input pulse: 0 V to 3.0 V
Input pulse rise and fall times: 5 ns between 1 V and 2 V
Measurements made at 1.5 V level

Guaranteed Operating Ranges

Part Number	Supply Voltage (V_{CC}) Min	Typ	Max	Ambient Temperature
93Z450XC, 93Z451XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93Z450XM, 93Z451XM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

X = Package Type; F for Flatpak, D for Ceramic DIP, P for Plastic DIP, L for Leadless.

DC Characteristics Over guaranteed operating ranges unless otherwise noted

Symbol	Characteristic	Min	Typ[1]	Max	Unit	Condition	
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs	
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IC}	Input Clamp Diode Voltage			−1.2	V	V_{CC} = Min, I_{IN} = −18 mA	
V_{OL}	Output LOW Voltage		0.30	0.45	V	V_{CC} = Min, I_{OL} = 16 mA	
V_{OH}	Output HIGH Voltage (93Z451 only)	2.4			V	V_{CC} = Min, I_{OH} = −2.0 mA Address Any '1'	
I_{IL}	Input LOW Current		−10	−100	μA	V_{CC} = Max, V_{IL} = 0.45 V	
I_{IH}	Input HIGH Current			40	μA	V_{CC} = Max, V_{IH} = 2.4 V	
I_{OHZ}	Output Leakage Current for High Impedance State (93Z451 only)			50 −100	μA μA	V_{OH} = 2.4 V V_{OL} = 0.4 V	0°C to +75°C
I_{OHZ}	Output Leakage Current for High Impedance State (93Z451 only)			100 −100	μA μA	V_{OH} = 2.4 V V_{OL} = 0.4 V	−55°C to +125°C
I_{CEX}	Output Leakage Current (93Z450 only)			50	μA	V_{CC} = 5.25 V, V_{CEX} = 4.95 V, 0°C to +75°C Chip Deselected	
I_{CEX}	Output Leakage Current (93Z450 only)			100	μA	V_{CC} = 5.5 V, V_{CEX} = 5.2 V, −55°C to +125°C Chip Deselected	
I_{OS}	Output Short-Circuit Current (93Z451 only)	−15	−35	−90	mA	V_{CC} = Max, V_O = 0 V, Note 2 Address Any '1'	
I_{CC}	Power Supply Current		95	155	mA	V_{CC} = Max	
C_{IN}	Input Pin Capacitance		4.0		pF	V_{CC} = 5.0 V, V_{IN} = 4.0 V, f = 1.0 MHz	
C_O	Output Pin Capacitance		7.0		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz	

AC Characteristics

Symbol	Characteristic	93Z450AXC 93Z451AXM Min	Max	93Z450XC 93Z451XC Min	Max	93Z450AXM 93Z451AXM Min	Max	93Z450XM 93Z451XM Min	Max	Unit	Condition
t_{AA}	Address to Output Access Time		35		45		45		60	ns	See AC Output Test Loading
t_{ACS}	Chip Select to Output Access Time		25		30		35		35	ns	See AC Output Test Loading

Notes
1. Typical values are at V_{CC} = 5.0 V, T_A = +25°C and maximum loading.
2. Not more than one output to be shorted at a time. Duration of the short circuit should not exceed one second.

FAIRCHILD
A Schlumberger Company

93Z510/93Z511
2048 x 8-Bit PROM

Isoplanar Schottky TTL Memory

Description

The 93Z510 and 93Z511 are fully decoded 16,384-bit field Programmable Read Only Memories (PROMs) organized 2048 words by eight bits per word. The devices are identical except for the output stage. The 93Z510 has open-collector outputs; the 93Z511 has 3-state outputs. Either device is enabled only when $\overline{CS}_1$ is LOW and CS_2 and CS_3 are HIGH. The 93Z510 and 93Z511 are supplied with all bits stored as logic "0s" and can be programmed to logic "1s" by following the programming procedure.

- **FAST ADDRESS ACCESS TIME—35 ns TYP**
- **POWER DISSIPATION—500 mW TYP**
- **FULL MILITARY AND COMMERCIAL RANGES**
- **FIELD PROGRAMMABLE**
- **ORGANIZATION—2048 WORDS x 8 BITS**
- **OPEN-COLLECTOR OUTPUTS—93Z510**
- **3-STATE OUTPUTS—93Z511**
- **LOW CURRENT PNP INPUTS**
- **FULLY DECODED—ON-CHIP ADDRESS DECODER AND BUFFER**
- **CHIP SELECT INPUTS PROVIDE EASY MEMORY EXPANSION**
- **WIRED-OR CAPABILITY—93Z510**
- **STANDARD 24-PIN DUAL IN-LINE PACKAGE**
- **HIGH RELIABILITY VERTICAL FUSES**

Pin Names

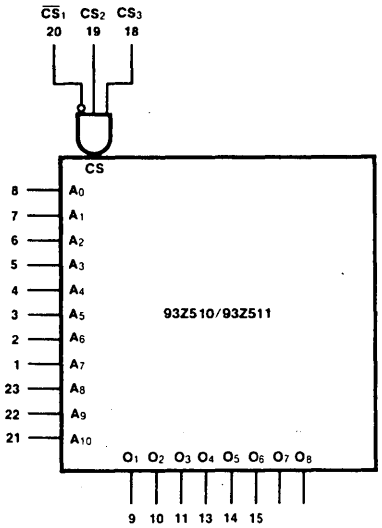
A_0-A_{10}	Address Inputs
$\overline{CS}_1$, CS_2, CS_3	Chip Select Inputs
O_1-O_8	Data Outputs

Absolute Maximum Ratings

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC}	−0.5 V to +7.0 V
Input Voltage	−0.5 V to +5.5 V
Current into Output Terminal	100 mA
Output Voltages	−0.5 V to +5.5 V

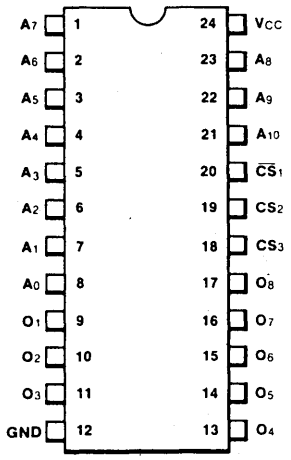
Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Logic Symbol



V_{CC} = Pin 24
GND = Pin 12

Connection Diagram
24-Pin DIP

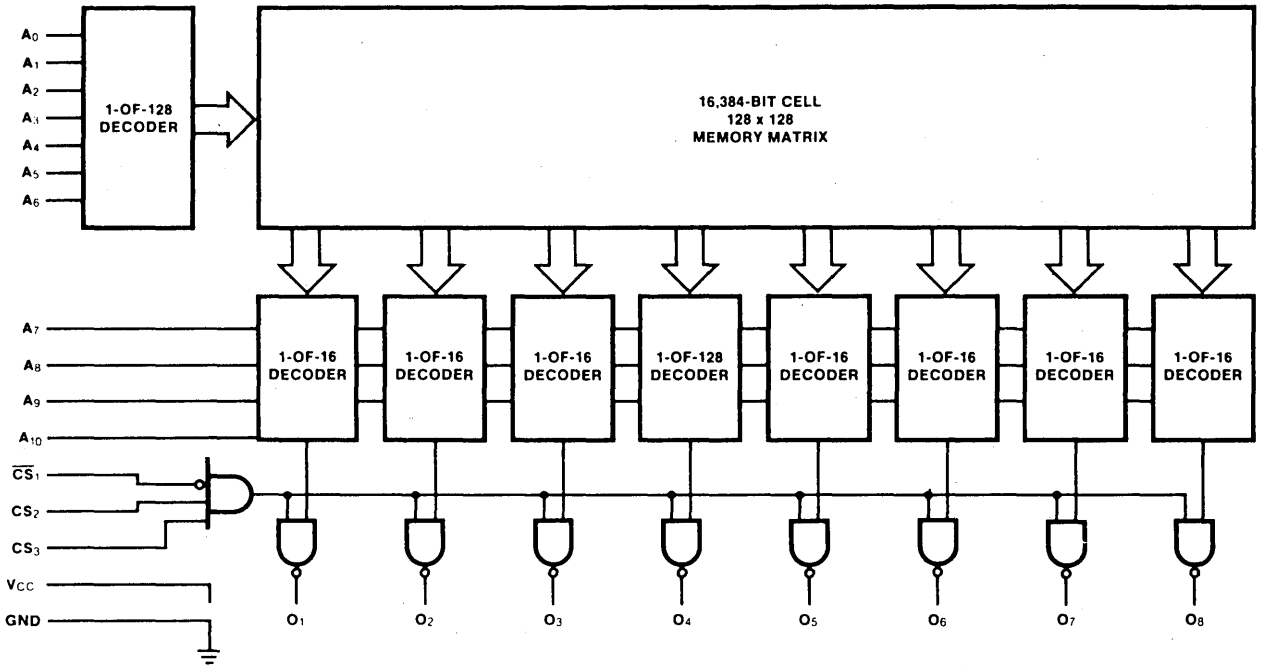


(Top View)

Note
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

Fairchild Camera and Instrument Corporation
464 Ellis Street, Mountain View, California 94042
415/962-5011 TWX 910 379 6435

Logic Diagram



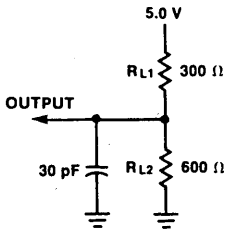
Functional Description

The 93Z510 and 93Z511 are bipolar field Programmable Read Only Memories (PROMs) organized 2048 words by eight bits per word. Open-collector outputs are provided on the 93Z510 for use in wired-OR systems. The 93Z511 has 3-state outputs which provide active pull-ups when enabled and high output impedance when disabled. Either device is enabled only when $\overline{CS}_1$ is LOW and CS_2 and CS_3 are HIGH.

The read function is identical to that of a conventional bipolar ROM. That is, a binary address is applied to the A_0 through A_{10} inputs, the chip is selected, and data is valid at the outputs after t_{AA}.

Programming (shorting selected junctions) is accomplished by following the procedure outlined in the following section.

AC Test Output Load



Test Conditions
Input pulse: 0 V to 3.0 V
Input pulse rise and fall times: 5 ns between 1 V and 2 V
Measurements made at 1.5 V level

Guaranteed Operating Ranges

Part Number	Supply Voltage (V_{CC}) Min	Typ	Max	Ambient Temperature
93Z510XC, 93Z511XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93Z510XM, 93Z511XM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

X = Package Type; F for Flatpak, D for Ceramic DIP, P for Plastic DIP, L for Leadless.

DC Characteristics Over guaranteed operating ranges unless otherwise noted.

Symbol	Characteristic	Min	Typ(1)	Max	Unit	Condition	
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs	
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IC}	Input Clamp Diode Voltage			−1.2	V	V_{CC} = Min, I_{IN} = −18 mA	
V_{OL}	Output LOW Voltage		0.30	0.45	V	V_{CC} = Min, I_{OL} = 16 mA	
V_{OH}	Output HIGH Voltage (93Z511 only)	2.4			V	V_{CC} = Min, I_{OH} = −2.0 mA	
I_{IL}	Input LOW Current		−10	−100	μA	V_{CC} = Max, V_{IL} = 0.45 V	
I_{IH}	Input HIGH Current			40	μA	V_{CC} = Max, V_{IH} = 2.4 V	
I_{OHZ}	Output Leakage Current for High Impedance State (93Z511 only)			50 −100	μA μA	V_{OH} = 2.4 V V_{OL} = 0.4 V	0°C to +75°C
I_{OHZ}	Output Leakage Current for High Impedance State (93Z511 only)			100 −100	μA μA	V_{OH} = 2.4 V V_{OL} = 0.4 V	−55°C to +125°C
I_{CEX}	Output Leakage Current (93Z510 only)			50	μA	V_{CC} = 5.25 V, V_{CEX} = 4.95 V, 0°C to +75°C Chip Deselected	
I_{CEX}	Output Leakage Current (93Z510 only)			100	μA	V_{CC} = 5.5 V, V_{CEX} = 5.2 V, −55°C to +125°C Chip Deselected	
I_{OS}	Output Short-Circuit Current (93Z511 only)	−15	−35	−90	mA	V_{CC} = Max, V_O = 0 V, Note 2	
I_{CC}	Power Supply Current		120	175	mA	V_{CC} = Max	
C_{IN}	Input Capacitance		4.0		pF	V_{CC} = 5.0 V, V_{IN} = 4.0 V, f = 1.0 MHz	
C_O	Output Capacitance		7.0		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz	

AC Characteristics

Symbol	Characteristic	V_{CC} = 5 V ± 5%, T_A = 0°C to +75°C Min	Typ(1)	Max	V_{CC} = 5 V ± 10%, T_A = −55°C to +125°C Min	Typ(1)	Max	Unit	Condition
t_{AA}	Address to Output Access Time		35	45		35	55	ns	See AC Test Output Load
t_{ACS}	Chip Select Access Time		15	25		15	25	ns	See AC Test Output Load

Notes
1. Typical values are at V_{CC} = 5.0 V, T_A = +25°C and maximum loading.
2. Not more than one output to be shorted at a time. Duration of the short circuit should not exceed one second.

FAIRCHILD
A Schlumberger Company

93Z564/93Z565
8192 x 8-Bit PROM

Isoplanar-Z Vertical Fuse TTL Memory

Description

The 93Z564 and 93Z565 are fully decoded 65,536-bit field Programmable Read Only Memories (PROMs) organized 8192 words by eight bits per word. The two devices are identical except the 93Z564 has open collector outputs while the 93Z565 has 3-state outputs.

The 93Z564 and 93Z565 use open base vertical fuse (transistor) cells. Initially the unprogrammed cell is in the logic '0' state. The cell can be programmed to a logic '1' state by following the specified programming procedure which fuses aluminum through the emitter base junction of the cell transistor.

- **Fully TTL Compatible**
- **Maximum Address Access Time — 45ns**
- **Maximum Chip Select Access Time — 25ns**
- **Available in Full Military and Commercial Temp. Ranges**
- **Fully Field Programmable**
- **Organized 8192 Words x 8 Bits**
- **Open-Collector Outputs on 93Z564**
- **3-State Outputs on 93Z565**
- **Low Current PNP Inputs**
- **High Reliability Vertical Fuses**
- **Chip Select for Easy Memory Expansion**

Pin Names

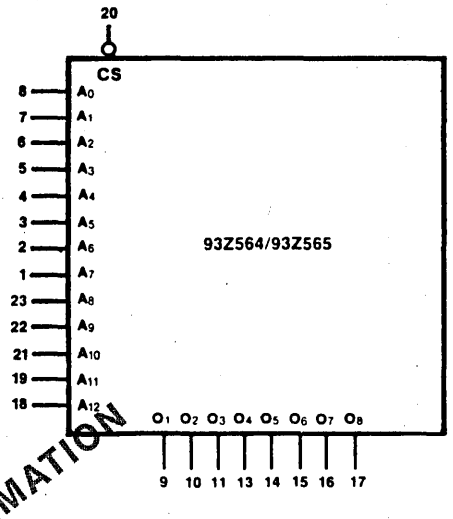
A_0–A_{12}	Address Inputs
$\overline{CS}$	Chip Select Input
O_1–O_8	Data Outputs

Absolute Maximum Ratings

Storage Temperature	-65°C to +150°C
Temperature (Ambient) under Bias	-55°C to +125°C
V_{CC}	-0.5 V to +7.0 V
Input Voltage	-0.5 V to +5.5 V
Current into Output Terminal	100 mA
Output Voltages	-0.5 V to +5.5 V

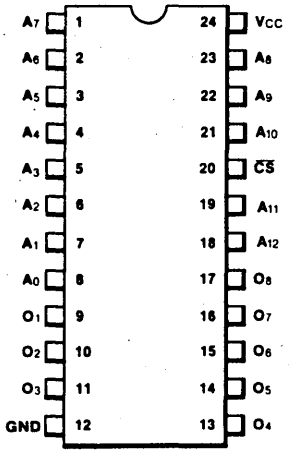
Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Logic Symbol



V_{CC} = Pin 24
GND = Pin 12

Connection Diagram
24-Pin DIP

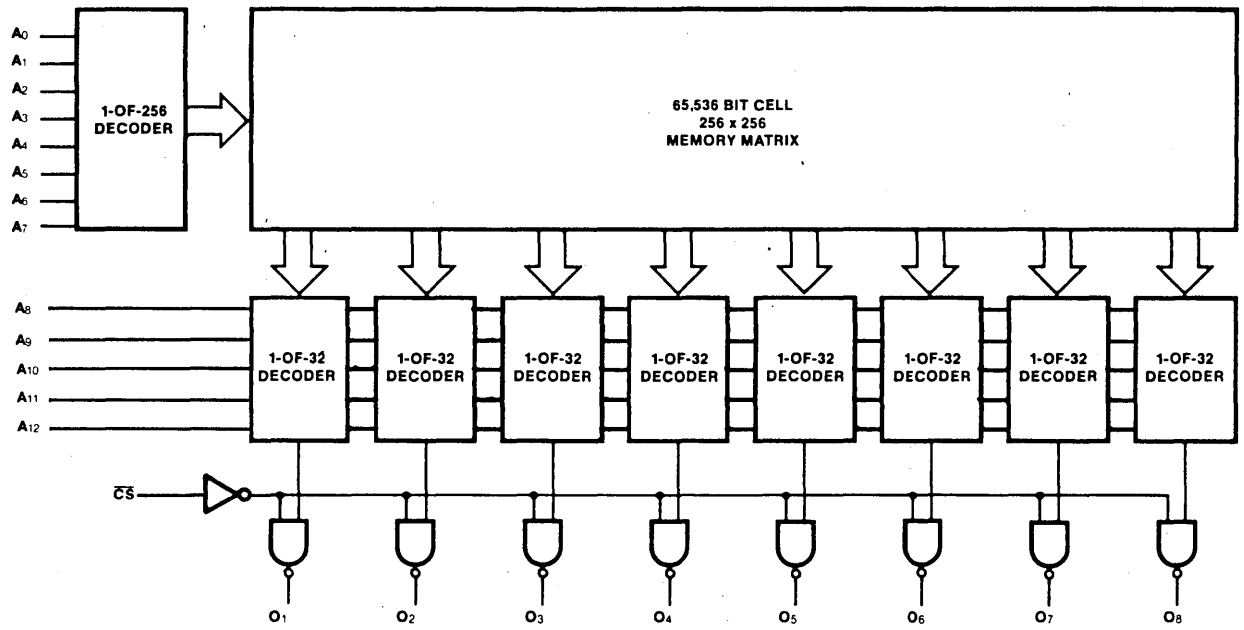


(Top View)

Note
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

Fairchild Camera and Instrument Corporation, Advanced Bipolar Division
464 Ellis Street, Mountain View, California 94042

Logic Diagram



Functional Description

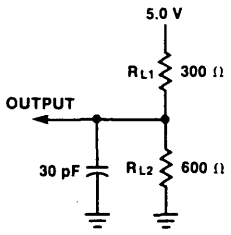
The 93Z564 and 93Z565 are TTL Bipolar field Programmable Read Only Memories (PROMs) organized 8192 words by eight bits per word. Open-collector outputs are provided on the 93Z564 for use in wired-OR systems. The 93Z565 has 3-state outputs which provide active pull ups when enabled and high output impedance when disabled. This allows optimization of word expansion in bus organized systems.

One chip select input is provided to allow memory expansion of up to 128K without the need for external decoding. Either device is enabled only when $\overline{CS}$ is LOW.

Programming, which is accomplished by selectively shorting fuse junctions, is outlined in the following section.

The read function is identical to that of a conventional Read Only Memory (ROM). A binary address is applied to the address pins A_0 through A_{12}, the chip is selected and data is available at the outputs after t_{AA}.

AC Test Output Load



Test Conditions

Input pulse: 0 V to 3.0 V
Input pulse rise and fall times: 5 ns between 1 V and 2 V
Measurements made at 1.5 V level

Guaranteed Operating Ranges

Part Number	Supply Voltage (V_{CC}) Min	Typ	Max	Ambient Temperature
93Z564XC, 93Z565XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93Z564XM, 93Z565XM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

X = Package Type; F for Flatpak, D for Ceramic DIP, P for Plastic DIP, L for Leadless.

DC Characteristics Over guaranteed operating ranges unless otherwise noted

Symbol	Characteristic	Min	Typ[1]	Max	Unit	Condition	
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs	
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IC}	Input Clamp Diode Voltage			−1.2	V	V_{CC} = Min, I_{IN} = −18 mA	
V_{OL}	Output LOW Voltage		0.30	0.45	V	V_{CC} = Min, I_{OL} = 16 mA	
V_{OH}	Output HIGH Voltage (93Z565 only)	2.4			V	V_{CC} = Min, I_{OH} = −2.0 mA Address Any '1'	
I_{IL}	Input LOW Current		-10	-100	μA	V_{CC} = Max, V_{IL} = 0.45 V	
I_{IH}	Input HIGH Current			40	μA	V_{CC} = Max, V_{IH} = 2.4 V	
I_{OHZ}	Output Leakage Current for High Impedance State (93Z565 only)			50 -100	μA μA	V_{OH} = 2.4 V V_{OL} = 0.4 V	0°C to +75°C
I_{OHZ}	Output Leakage Current for High Impedance State (93Z565 only)			100 -100	μA μA	V_{OH} = 2.4 V V_{OL} = 0.4 V	−55°C to +125°C
I_{CEX}	Output Leakage Current (93Z564 only)			50	μA	V_{CC} = 5.25 V, V_{CEX} = 4.95 V, 0°C to +75°C Chip Deselected	
I_{CEX}	Output Leakage Current (93Z564 only)			100	μA	V_{CC} = 5.5 V, V_{CEX} = 5.2 V, −55°C to +125°C Chip Deselected	
I_{OS}	Output Short-Circuit Current (93Z565 only)	−15	−35	−90	mA	V_{CC} = Max, V_O = 0 V, Note 2 Address Any '1'	
I_{CC}	Power Supply Current		120	175	mA	V_{CC} = Max	
C_{IN}	Input Capacitance		4.0		pF	V_{CC} = 5.0 V, V_{IN} = 4.0 V, f = 1.0 MHz	
C_O	Output Capacitance		7.0		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz	

AC Characteristics

Symbol	Characteristic	V_{CC} = 5 V ± 5%, T_A = 0°C to +75°C Min	Typ[1]	Max	V_{CC} = 5 V ± 10%, T_A = −55°C to +125°C Min	Typ[1]	Max	Unit	Condition
t_{AA}	Address to Output Access Time		35	45		35	55	ns	See AC Test Output Load
t_{ACS}	Chip Select Access Time		15	25		15	25	ns	See AC Test Output Load

Notes

1. Typical values are at V_{CC} = 5.0 V, T_A = +25°C and maximum loading.
2. Not more than one output to be shorted at a time. Duration of the short circuit should not exceed one second.

FAIRCHILD
A Schlumberger Company

93458/93459
16 x 48 x 8 FPLA

Isoplanar Schottky TTL Logic Array

Description

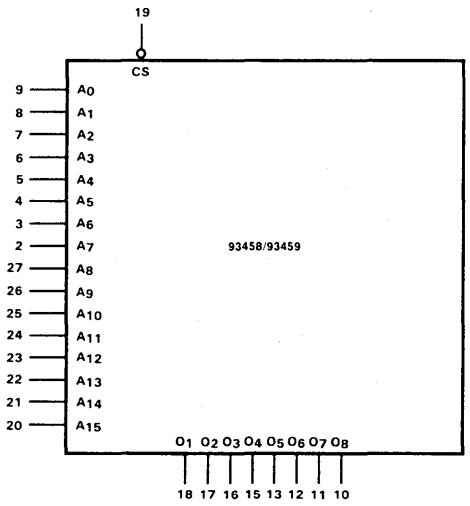
The 93458 and 93459 are bipolar Field Programmable Logic Arrays (FPLA) organized with 16 inputs, 48 product terms and eight outputs. The 16 inputs and their complements are fuse linked to the inputs of 48 AND gates (48 product terms). Each of the 48 AND gates are fuse linked to eight 48-input OR gates (eight summing terms). Each output may be programmed active HIGH or active LOW. The devices are identical except for the output stage. The 93458 has open-collector outputs; the 93459 has 3-state outputs. In either case, the outputs are enabled when $\overline{CS}$ is LOW.

- **FAST CYCLE TIME—25 ns TYP**
- **FULL MILITARY AND COMMERCIAL RANGES**
- **FIELD PROGRAMMABLE**
- **ORGANIZATION—16 INPUTS x 48 PRODUCT TERMS x 8 OUTPUTS**
- **OPEN-COLLECTOR OUTPUTS—93458**
- **3-STATE OUTPUTS—93459**
- **CHIP SELECT INPUT PROVIDES EASY FUNCTIONAL EXPANSION**
- **STANDARD 28-PIN PACKAGE**
- **NICHROME FUSE LINKS FOR HIGH RELIABILITY**

Pin Names

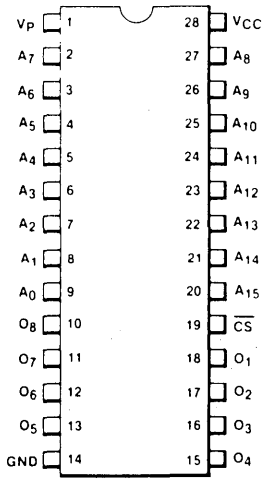
$\underline{A_0}$-A_{15}	Address inputs
$\overline{CS}$	Chip Select Input
O_1-O_8	Data Outputs
V_P	Programming Pin

Logic Symbol



V_{CC} = Pin 28
GND = Pin 14
V_P = Pin 1

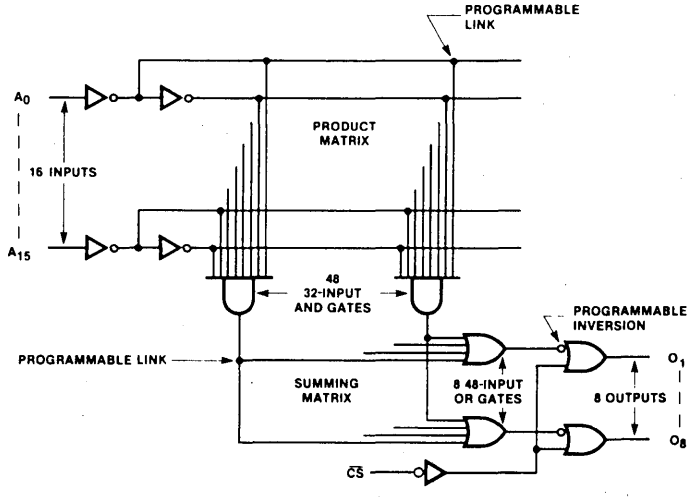
Connection Diagram
28-Pin DIP



(Top View)

Note
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

Logic Diagram



MEMORY

Fairchild

Functional Description

The 93458 and 93459 are bipolar Field Programmable Logic Arrays (FPLA) organized 16 inputs by 48 product terms by eight outputs. Open-collector outputs are provided on the 93458 for use in wired-OR systems. The 93459 has 3-state outputs which provide active pull-ups when enabled and high output impedance when disabled. Chip Select for both devices is active LOW; i.e., a HIGH (logic "1") on the $\overline{CS}$ pin will disable all outputs.

The read function is identical to that of a conventional bipolar ROM. That is, a binary address is applied to the A_0 through A_{15} inputs, the chip is selected, and data is valid at the outputs after t_{AA}.

Programming (selectively opening nichrome fuse links) is accomplished by following the sequence outlined in the *Programming Specifications* table.

By programming, the eight outputs of an FPLA can be made to relate to the 16 inputs as given by the following example:

8 outputs total

$$O_1 = A_0\,\overline{A_6}\,A_{14} + \overline{A_2}\,\overline{A_{15}} + \underbrace{\overline{A_0}\,A_1 \ldots A_{15}}_{\text{16 input terms max}} + \overline{A_8}\,A_{10}\,\overline{A_{13}}$$

48 product terms max

$$O_2 = A_0\,\overline{A_6}\,A_{14} + \overline{A_2}\,\overline{A_{15}}$$

(Output polarity programmed, active HIGH.)

$$O_8 = \overline{(\overline{A_8}\,A_{10}\,\overline{A_{13}} + A_4\,\overline{A_7}\,\overline{A_9}\,A_{11}\,\overline{A_{12}})}$$

(Output polarity not programmed, active LOW.)

Logic Relationships

Input Term

A_n — n = 0, . . ., 15, one of 16 inputs

Product Term

$P_m = \pi_0^{15} (i_n A_n + j_n \overline{A_n})$ — m = 0, . . ., 47, one of 48 product terms.

where:

a) $i_n = j_n = 0$ for unprogrammed input

b) $i_n = j_n$ for programmed input

c) $i_n = j_n = 1$ for immaterial input

$F_r = \Sigma_0^{47} P_m$ — r = 1, . . ., 8, the OR function of the 48 product terms

Summing Term

$S_r = \Sigma_0^{47} k_m P_m$ — where $k_m = 0$ for product term inactive (programmed)

$k_m = 1$ for product term active (unprogrammed)

				Output	
Mode	$\overline{CS}$	F_r	S_r	Active HIGH	Active LOW
Read	L	H	L	L	H
	L	H	H	H	L
	L	L	X	L	H
Disable	H	X	X	H (93458) High-Z (93459)	H (93458) High-Z (93459)
	H	X	X		

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Guaranteed Operating Ranges

Part Number	Supply Voltage (V_{CC}) Min	Typ	Max	Ambient Temperature
93458XC, 93459XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93458XM, 93459XM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

X = Package Type; F for Flatpak, D for Ceramic DIP, P for Plastic DIP, L for Leadless.

DC Characteristics Over guaranteed operating ranges unless otherwise noted

Symbol	Characteristic	Min	Typ(1)	Max	Unit	Condition	
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs	
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IC}	Input Clamp Diode Voltage			−1.2	V	V_{CC} = Min, I_{IN} = −18 mA	
V_{OL}	Output LOW Voltage		0.30	0.45	V	V_{CC} = Min, I_{OL} = 16 mA	
V_{OH}	Output HIGH Voltage (93459 only)	2.4			V	V_{CC} = Min, I_{OH} = −2.0 mA	
I_{IL}	Input LOW Current		−160	−250	μA	V_{CC} = Max, V_{IL} = 0.45 V	
I_{IH}	Input HIGH Current			40	μA	V_{CC} = Max, V_{IH} = 2.4 V	
I_{OHZ}	Output Leakage Current for High Impedance State (93459 only)			50 −50	μA μA	V_{OH} = 2.4 V V_{OL} = 0.4 V	0°C to +75°C
I_{OHZ}	Output Leakage Current for High Impedance State (93459 only)			100 −100	μA	V_{OH} = 2.4 V V_{OL} = 0.4 V	−55°C to +125°C
I_{CEX}	Output Leakage Current (93458 only)			50	μA	V_{CC} = 5.25 V, V_{CEX} = 4.95 V, −0°C to +75°C Chip Deselected	
I_{CEX}	Output Leakage Current (93458 only)			100	μA	V_{CC} = 5.5 V, V_{CEX} = 5.2 V, −55°C to +125°C Chip Deselected	
I_{OS}	Output Short-Circuit Current (93459 only)	−15	−35	−90	mA	V_{CC} = Max, V_O = 0 V, Note 2	
I_{CC}	Power Supply Current		105	170	mA	V_{CC} = Max, Chip Selected, Note 3	
C_{IN}	Input Pin Capacitance		4.0		pF	V_{CC} = 5.0 V, V_{IN} = 4.0 V, f = 1.0 MHz	
C_O	Output Pin Capacitance		7.0		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz	

AC Characteristics

Symbol	Characteristic	V_{CC} = 5 V ± 5%, T_A = 0°C to +75°C Min	Typ(1)	Max	V_{CC} = 5 V ± 10%, T_A = −55°C to +125°C Min	Typ(1)	Max	Unit	Condition
t_{AA}	Address to Output Access Time		25	45		25	65	ns	See AC Test Output Load
t_{ACS}	Chip Select Access Time		15	25		15	30	ns	See AC Test Output Load

Notes

1. Typical values are at V_{CC} = 5.0 V, T_A = +25°C and maximum loading.
2. Not more than one output to be shorted at a time. Duration of the short circuit should not exceed one second.
3. For programmed part, add 0.45 mA typical, 0.60 mA maximum per selected programmed product terms and add 2.9 mA typical, 3.9 mA maximum per enabled low output or 33 mA typical, 44 mA maximum for disabled states.

FAIRCHILD
A Schlumberger Company

F3528
2048 x 8 Static RAM

Preliminary Data Sheet

MOS Memory Products

Description

The F3528 is a 16,384-bit static Random Access Memory (RAM) organized as 2048 words of eight bits each. Since the operation of the F3528 is entirely static, no clocks or refresh are required. This device operates from a single +5V supply and is directly TTL compatible at all inputs and outputs, including the eight bidirectional data DQ pins. The F3528 has an automatic power down feature controlled by the Chip Enable function ($\overline{E}$ = active LOW). When not enabled, the F3528 is in standby mode; this reduces power dissipation by as much as 75% with no degradation of access time.

The F3528 is designed for memory applications where static operation, low cost, large bit-capacity and simple interfacing are important design considerations. It is manufactured using Fairchild's high performance, scaled NMOS technology, Isoplanar-H™. State-of-the-art design and process techniques ensure high density, lower power dissipation and excellent speed performance.

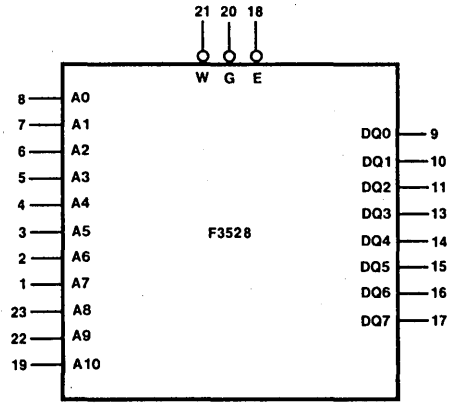
The F3528 is available in a standard 24-pin dual in-line package in a configuration that is pin and function compatible with industry standard EPROMS.

- **2048 x 8-BIT ORGANIZATION**
- **COMPLETELY STATIC—NO CLOCKS OR REFRESH**
- **SINGLE +5V SUPPLY**
- **AUTOMATIC POWER DOWN WHEN CHIP NOT ENABLED ($\overline{E}$)**
- **ACCESS TIME—100ns, 120ns, 150ns, 200ns**
- **LOW POWER DISSIPATION 550 mW ACTIVE (MAX) 82.5 mW STANDBY (MAX)**
- **TOTALLY TTL COMPATIBLE WITH SIMPLE BUS CONTROL**
- **COMMON DATA I/O BUS WITH 3-STATE CAPABILITY**
- **JEDEC STANDARD PINOUT**
- **STANDARD 24-PIN DIP**
- **EPROM COMPATIBLE PINOUT**

Pin Names

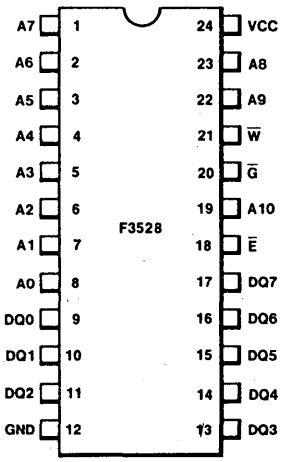
AO-A10	Address Inputs
$\overline{W}$	Write Enable Input
$\overline{G}$	Output Enable Input
$\overline{E}$	Chip Enable Input
DQO-DQ7	Data Inputs/Outputs
VCC	Power (+5V)
GND	Ground (OV)

Logic Symbol



VCC = Pin 24
GND = Pin 12

Connection Diagram
24-Pin DIP



(Top View)

Package	Outline	Order Code
Ceramic DIP	IT	D
Plastic DIP	IU	P

Fairchild Camera and Instrument Corporation
101 Bernal Road, San Jose, California 95119-1399
(408)224-7000 TWX 910 379 6435

FAIRCHILD
A Schlumberger Company

F3528L
2048 x 8 Static RAM

Preliminary Data Sheet

MOS Memory Products

Description

The F3528L is a 16,384-bit static Random Access Memory (RAM) organized as 2048 words of eight bits each. Since the operation of the F3528L is entirely static, no clocks or refresh are required. This device operates from a single +5V supply and is directly TTL compatible at all inputs and outputs, including the eight bidirectional data DQ pins. The F3528L has an automatic power down feature controlled by the Chip Enable function ($\overline{E}$ = active LOW). When not enabled, the F3528L is in standby mode; this reduces power dissipation by as much as 75% with no degradation of access time.

The F3528L is designed for memory applications where static operation, low cost, large bit-capacity and simple interfacing are important design considerations. It is manufactured using Fairchild's high performance, scaled NMOS technology, Isoplanar-H™. State-of-the-art design and process techniques ensure high density, lower power dissipation and excellent speed performance.

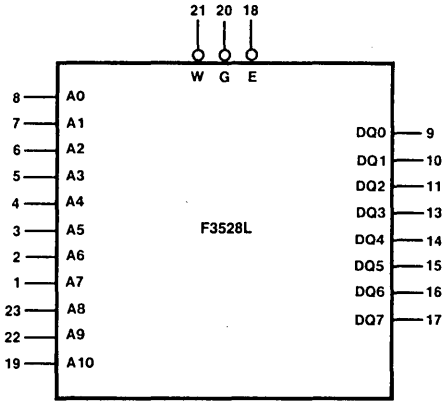
The F3528L is available in a standard 24-pin dual in-line package in a configuration that is pin and function compatible with industry standard EPROMS.

- **2048 x 8-BIT ORGANIZATION**
- **COMPLETELY STATIC—NO CLOCKS OR REFRESH**
- **SINGLE +5V SUPPLY**
- **AUTOMATIC POWER DOWN WHEN CHIP NOT ENABLED ($\overline{E}$)**
- **ACCESS TIME—100ns, 120ns, 150ns, 200ns**
- **LOW POWER DISSIPATION 330 mW ACTIVE (MAX) 66 mW STANDBY (MAX)**
- **TOTALLY TTL COMPATIBLE WITH SIMPLE BUS CONTROL**
- **COMMON DATA I/O BUS WITH 3-STATE CAPABILITY**
- **JEDEC STANDARD PINOUT**
- **STANDARD 24-PIN DIP**
- **EPROM COMPATIBLE PINOUT**

Pin Names

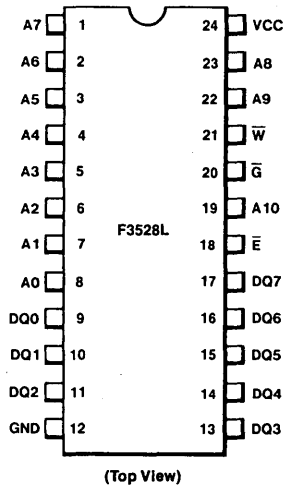
AO-A10	Address Inputs
$\overline{W}$	Write Enable Input
$\overline{G}$	Output Enable Input
$\overline{E}$	Chip Enable Input
DQO-DQ7	Data Inputs/Outputs
VCC	Power (+5V)
GND	Ground (OV)

Logic Symbol



VCC = Pin 24
GND = Pin 12

Connection Diagram
24-Pin DIP



(Top View)

Package	Outline	Order Code
Ceramic DIP	IT	D
Plastic DIP	IU	P

Fairchild Camera and Instrument Corporation
101 Bernal Road, San Jose, California 95119-1399
(408)224-7000 TWX 910 379 6435

FAIRCHILD
A Schlumberger Company

F4164
65,536 x 1 Dynamic RAM

Preliminary Data Sheet | MOS Memory Products

Description

The F4164 is a dynamic Random Access Memory (RAM) circuit organized as 65,536 single-bit words. This memory uses the Fairchild advanced double poly NMOS, Isoplanar-H™ process which allows volume manufacture of reliable, high density memory products.

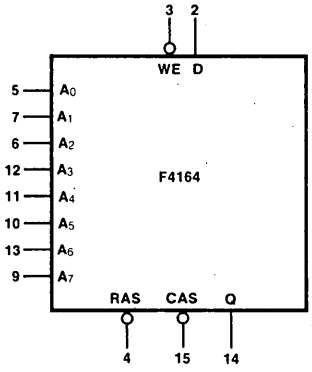
Innovative architecture and circuit design provide significant user benefits including wide operating margins, low power dissipation and excellent noise characteristics. Double cruciform architecture minimizes signal path lengths to improve noise margin and reduce propagation delays. A multiplexed sense amplifier scheme halves the number of sense amplifiers and the bit-line to cell capacitance ratio; this simultaneously reduces power consumption and improves signal sensing margins. Full-sized reference cells provide good margins and control. Low capacitance TTL-compatible inputs with overshoot and anti-static protection insure data and address input integrity.

- **INDUSTRY STANDARD 16-PIN DIP WITH PIN 1 NOT CONNECTED (NC)**
- **LOW CAPACITANCE TTL-COMPATIBLE INPUTS WITH OVERSHOOT AND ANTI-STATIC PROTECTION**
- **COMMON I/O CAPABILITY**
- **STANDARD 5 V ± 10% SINGLE POWER SUPPLY REQUIREMENT**
- **LOW POWER**
  209 mW ACTIVE (MAX)
  19.3 mW STANDBY (MAX)
- **FAST ACCESS TIME—$\overline{120}$ ns, 150 ns or 200 ns**
- **READ-MODIFY-WRITE, $\overline{RAS}$-ONLY REFRESH AND PAGE MODE CAPABILITY**
- **OUTPUT UNLATCHED AT CYCLE END ALLOWS FOR PAGE BOUNDARY EXTENSION AND TWO-DIMENSIONAL CHIP SELECTION**

Pin Names

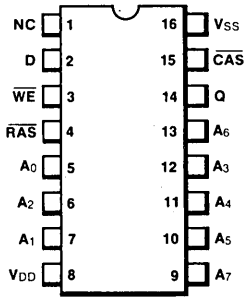
A_0-A_7	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
D	Data Input
Q	Data Output

Logic Symbol



V_{SS} = Pin 16
V_{DD} = Pin 8

Connection Diagram
16-Pin DIP



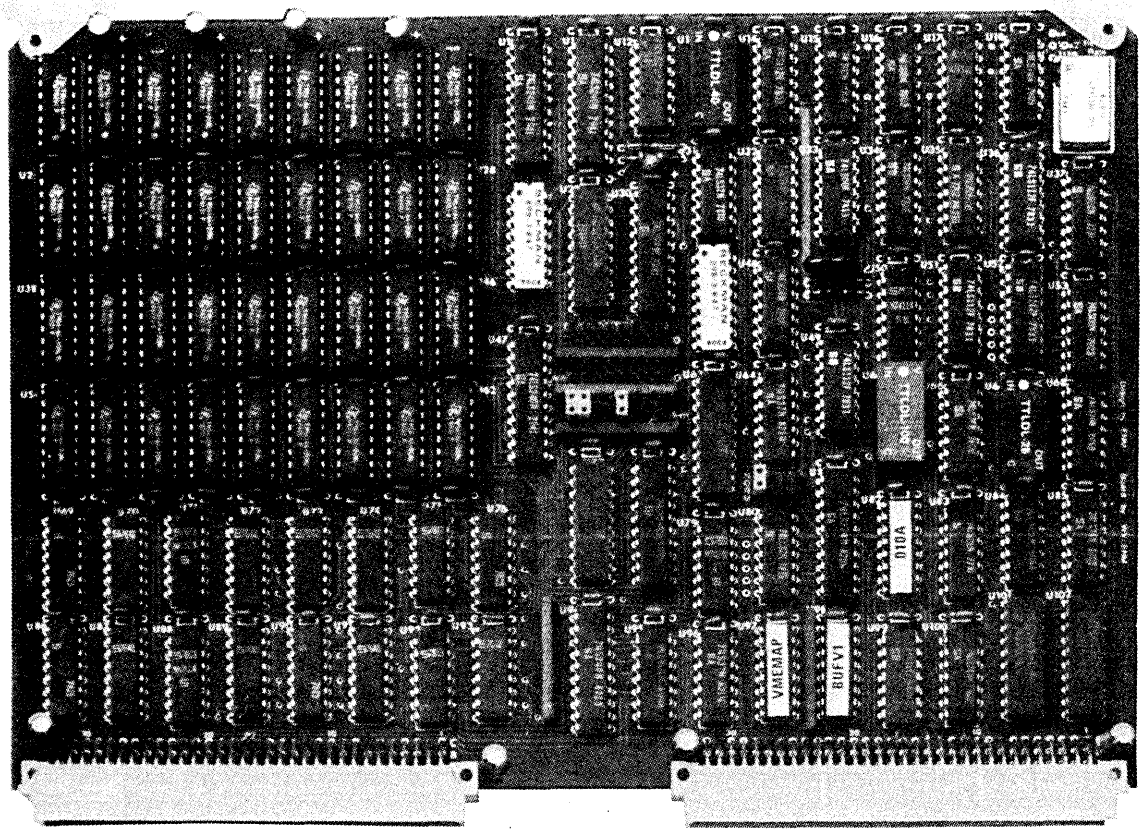
(Top View)

Fairchild

MEMORY

Fairchild Camera and Instrument Corporation
464 Ellis Street, Mountain View, California 94042
415/962-5011 TWX 910 379 6435

For Key Data On Every IC On This Board, The Place To Look Is...



This Signetics Memory Module provides 256K bytes of dynamic random access memory, plus parity protection.

Equipment and system design often require the use of a wide variety of integrated circuits in order to obtain optimum performance. One way for an engineer to be certain that he hasn't overlooked the best device for his application is to refer to the pages of IC MASTER.

Surveys conducted by IC MASTER, integrated circuit manufacturers, and independent research agencies confirm that four out of five IC MASTER users have specified one or more products as the result of using IC MASTER.

Device No.	Description
74LS00	Quadruple 2-Input NAND Gate
74LS08	Quadruple 2-Input AND Gate
74LS04	Hex Inverter
74LS20	Dual 4-Input NAND Gate
74LS32	Quadruple 2-Input OR Gate
74LS37	Quadruple 2-Input NAND Buffer
74LS24	Schmitt Trigger
74LS74	Dual D-Type Edge-Triggered Flip-Flop
74LS132	Quadruple 2-Input Schmitt Trigger
74LS112	Dual J-K Edge-Triggered Flip-Flop
74LS10	Triple-3-Input NAND Gate
74LS244	Octal Buffer/Line Driver
74LS645	Octal Bus Transceiver
AM25LS2521	8-Bit Equal-to Comparator
74S38	AND/NAND Gate
N7411	Triple-3-Input AND Gate
N74S40	Dual 4-Input NAND Buffer
TMS4164	64K Dynamic RAM
7641	512 x 8 PROM
7642	1K x 4 PROM

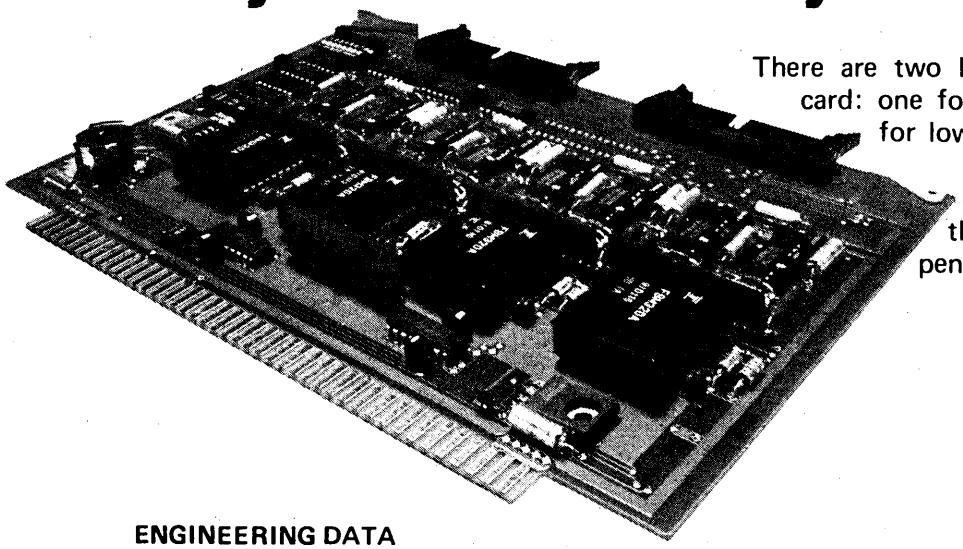
Representative list of ICs on Signetics SMVME3100 Memory Card. Key specifications for all of these ICs can be found in IC MASTER.

IC MASTER

BE SURE. BEGIN WITH THE IC MASTER

32K byte Bubble Memory Card

FUJITSU



There are two kinds of Fujitsu bubble memory card: one for high-speed file memory and one for low-speed file memory.

Both can be connected to the 8-bit micro-processor buss and the capacity is easily increased depending on a system.

ENGINEERING DATA

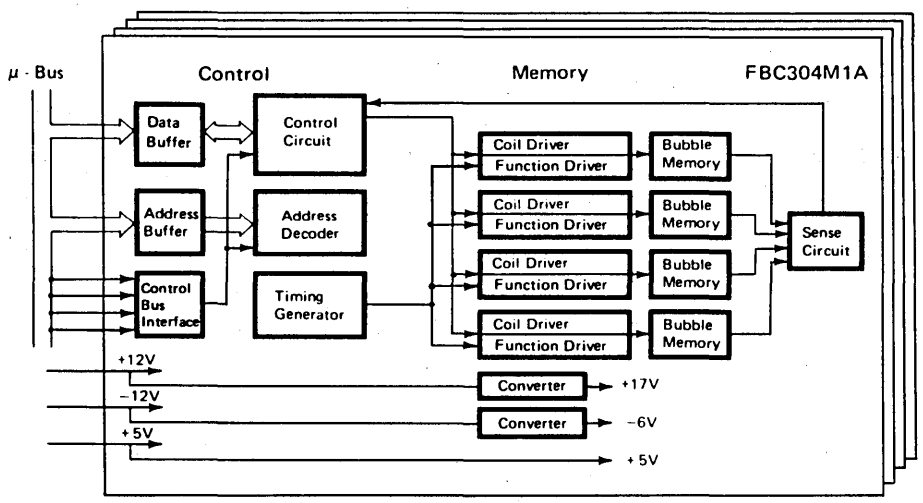
	FBC304M1A	FBC304D2A
Devices	FBM31DB	FBM32DA
Number of Devices	4	4
Organization	Serial loop	Major/Minor loop
Capacity	296,128 bits	324,024 bits
Average Access Time	370 ms	4.5 ms
Drive Frequency	100KHz	100KHz
Data Rate	100K bits/sec.	200K bits/sec.
Interface	TTL Compatible	TTL Compatible
Power Consumption Operating Stand-by	 9 W 6 W	 11 W 2.5 W
Power Requirement *	+12 V (± 5 %) 0.3A Max. −12 V (± 5 %) 0.2A Max. + 5 V (± 5 %) 1.6A Max.	+12 V (± 5 %) 1.0A Max. −12 V (± 5 %) 0.2A Max. + 5 V (± 5 %) 0.7A Max.
Temperature Range Operating Non-volatile Storage	 0°C to +50°C −40°C to +85°C	 0°C to +50°C −40°C to +85°C
Card Dimension	230 x 160 mm²	230 x 160 mm²

* Sequencial power-on and power-off are unnecessary.

Fijutsu 32K byte Bubble Memory Card

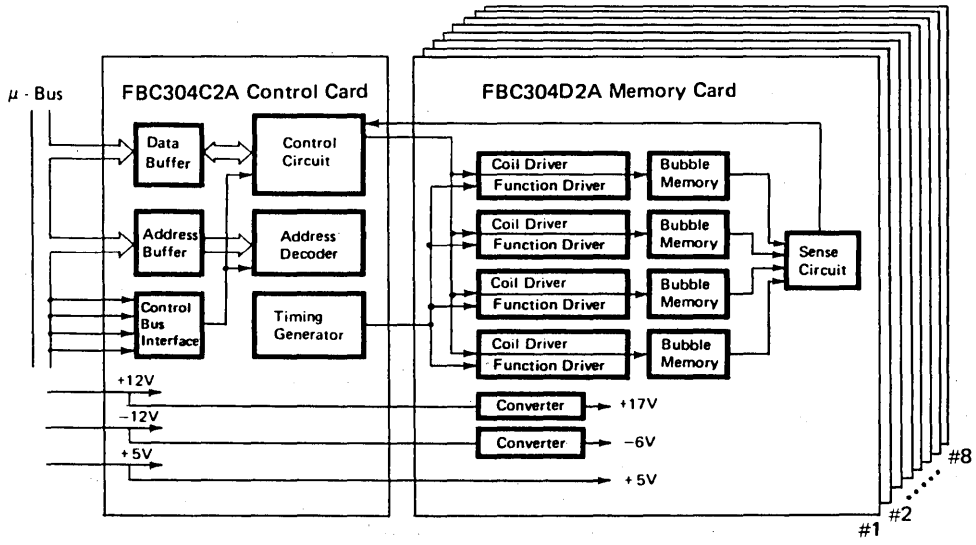
FBC304M1A is a 32K byte bubble memory card containing four 74K bit serial loop organized Bubble Memory Devices FBM31DB.

The timing and control circuits, in addition to coil drivers, function drivers, sense amplifier, etc., are also mounted on the same card, which can be directly connected to the 8-bit micro-processor as a low-speed data file and program memory.



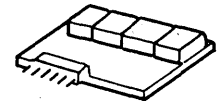
Fujitsu America, Inc., 918 Sherwood Drive, Lake Bluff, Illinois 60044

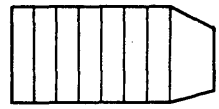
FBC304D2A is a 32K byte high-speed bubble memory card with a TTL interface, containing four 83K bit major/minor loop organized Bubble Memory Devices FBM32DA with peripheral circuits. As a high-speed random access file memory this card can be connected to the 8 bit microprocessor buss via a control card FBC304C2A and the number of cards can be increased up to 256K bytes (8 cards), according to a system scale.

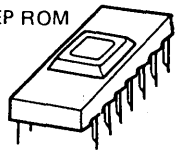


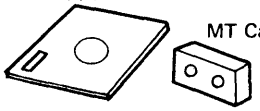
EXPECTED BUBBLE MEMORY APPLICATIONS

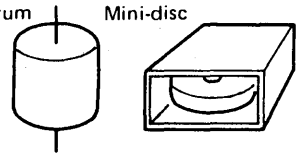
System Memory Capacity (Byte)	10K	100K	1M	10M
Chip Capacity (bit)	64K ~ 100K	256K ~ 1M	> 1 M	
Bubble Memory Products	Program Memory: Micro-processor + Bubble Memory	Mini-File Memory	File Memory	
Competing Technology (Application Area)	EP ROM	Floppy Disc, MT Cassette	Drum, Mini-disc	







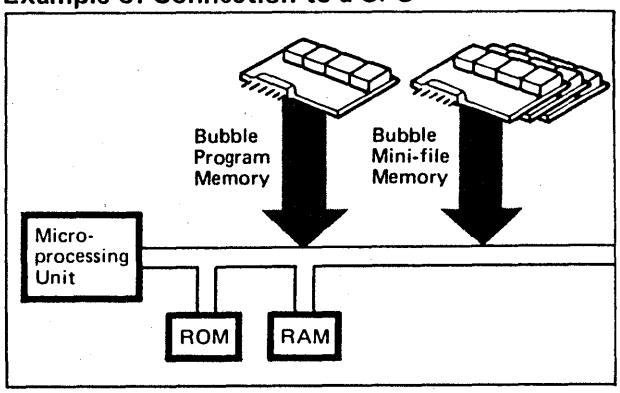




Applications

- File memory for micro-computer and mini-computer
- Replacement for disc, drum and tape devices
- Program loaders for testing equipment and numerical control systems

Example of Connection to a CPU



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64K bit Bubble Memory Device

FUJITSU

FBM31DB and FBM32DA are 18-pin DIP packages that contain a 64K bit serial loop chip and a 64K bit major/minor loop chip, respectively, orthogonal coils for rotating magnetic field, and a magnet for biasing which makes the bubbles stable to keep data.

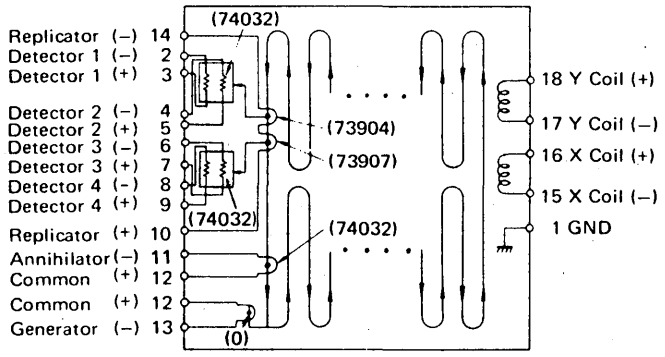
These bubble memory devices serve as the heart of the Fujitsu bubble memory card mounted on a printed circuit board.

ENGINEERING DATA

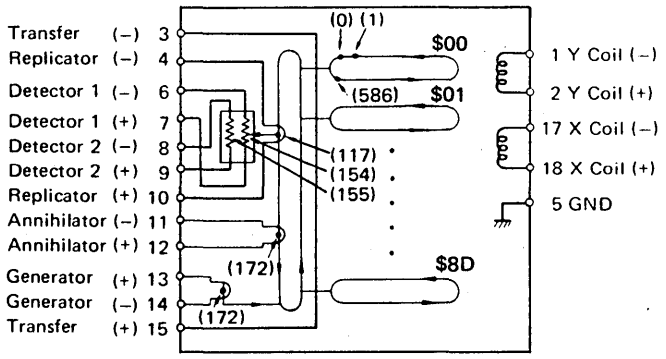
	FBM31DB	FBM32DA
Capacity:	74,032 bits	83,354 bits (total) 81,006 bits (effective)
Organization:	Serial loop	Major/Minor loop
Drive Frequency:	100KHz	100KHz
Transfer Rate:	100K bits/sec.	50K bits/sec.
Average Access Time:	370 ms	4.5 ms
Power Consumption:	500 mW	500 mW
Temperature Range Operating: Non-volatile Storage:	 0°C to + 55°C −40°C to + 85°C	 0°C to + 55°C −40°C to + 85°C
External Magnetic Field Operating: Non-Volatile Storage:	 50 Oe Max. 100 Oe Max.	 50 Oe Max. 100 Oe Max.
Physical Structure:	18 pin DIP	18 pin DIP
Dimensions:	27.94 x 31 x 10 mm^3	27.94 x 31 x 10 mm^3
Weight	30 g	30 g

CIRCUIT DIAGRAM

- FBM31DB (Serial loop)



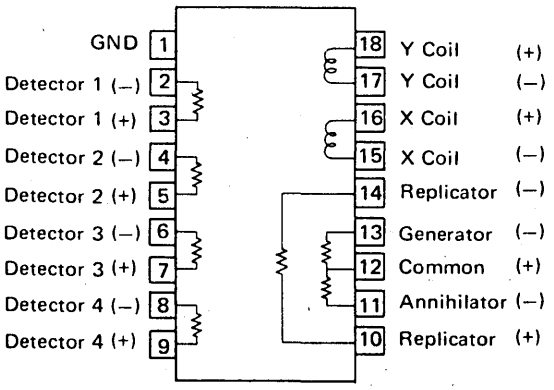
- FBM32DA (Major/Minor loop)



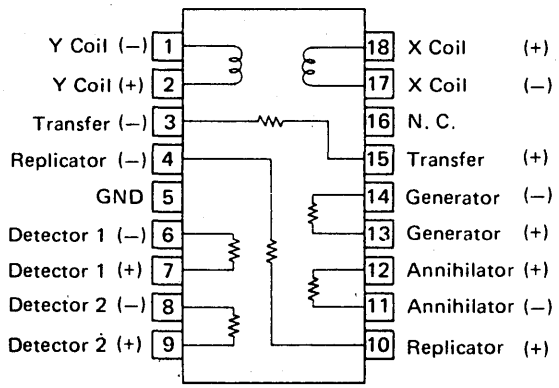
* Loop numbers (00 through 8D) are designated by hexadecimal code.

PIN ASSIGNMENT

- FBM31DB (Serial loop)



- FBM32DA (Major/Minor loop)



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256K bit Bubble Memory Device

FUJITSU

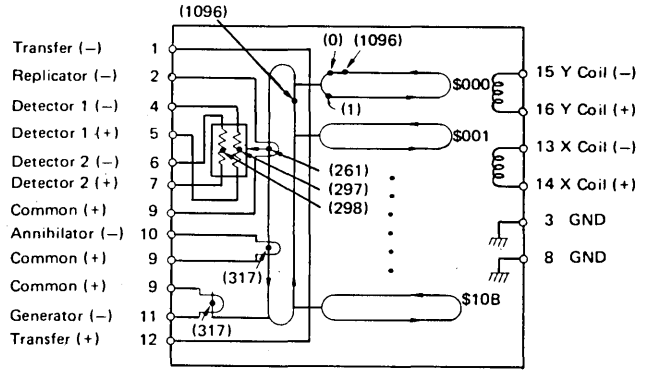
The FBM42DA is a major/minor bubble memory device in a 16 DIP package containing a 256K bit chip; the FBM43DA is a block replicator transfer bubble memory device in a 20 pin DIP package containing a 256K bit chip. Both devices are mountable on a printed circuit board and have orthogonal coils for rotating magnetic field. They also incorporate magnets for biasing, thereby providing the bubbles with stability to retain data.

ENGINEERING DATA

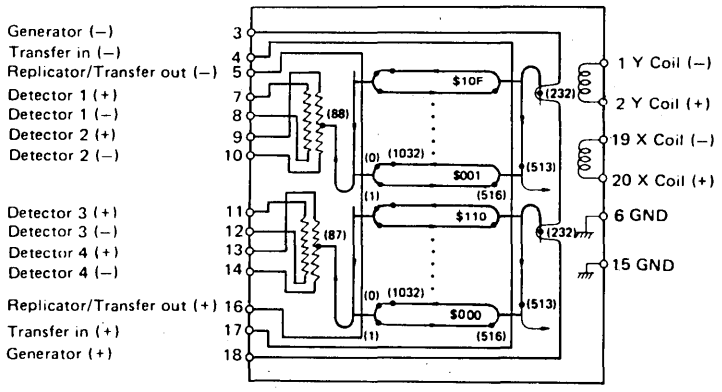
	FBM42DA	FBM43DA
Capacity	283,026 bits (effective) 1,097 bits X 258 loops	273,745 bits (effective) 1,033 bits X 265 loops
Organization	Major/minor loop	Major/minor loop (Block replicator transfer system)
Drive Frequency	100KHz	100KHz
Transfer Rate	50K bits/sec	100K bits/sec
Average Access Time	8.5 ms	6.0 ms
Power Consumption	670 mW	670 mW
Temperature Range Operating Non-volatile Storage	 0°C to +55°C −40°C to +85°C	 0°C to +55°C −40°C to +85°C
External Magnetic field	50 Oe Max.	50 Oe Max.
Physical Structure	16 pin DIP	20 pin DIP
Dimensions	27.94 x 31 x 11 mm^3	27.94 x 31 x 11 mm^3
Weight	30 g	30 g

CIRCUIT DIAGRAM

- FBM42DA (Major/minor loop)

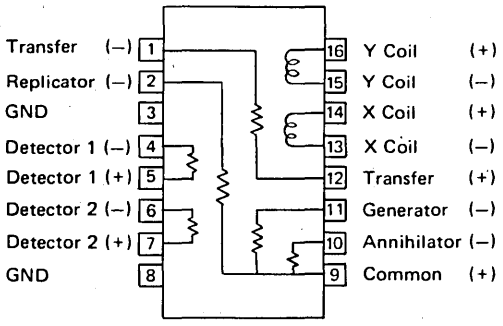


- FBM43DA (Block replicator transfer)

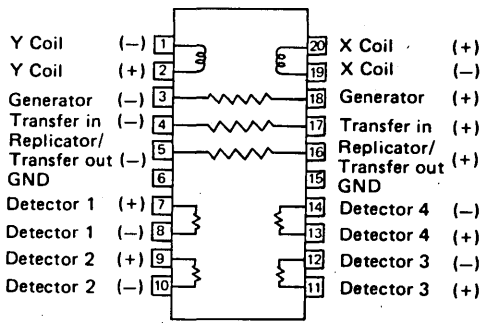


PIN ASSIGNMENT

- FBM420A (Major/minor loop)



- FBM43DA (Block replicator transfer)



* The $ mark prefixed hexadecimal codes in the circuit diagrams indicate minor loop numbers.

Fujitsu America, Inc., 918 Sherwood Drive, Lake Bluff, Illinois 60044

FUJITSU
MICROELECTRONICS

MB8464
MB81416

NEW PRODUCTS FOR 1983

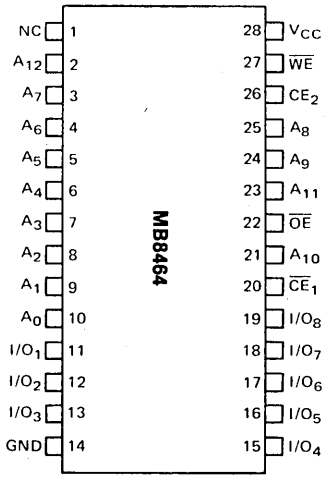
MB8464 64K CMOS STATIC RAM

Organized as 8192 words by 8-bits

- Static operation: no clocks or refresh required
- Fast Access Times:
  - MB8464-10 100 ns max.
  - MB8464-10L 100 ns max.
  - MB8464-15 150 ns max.
  - MB8464-15L 150 ns max.
- Low Power Consumption:
  - MB8464-10/-15
    - 11 mW max. (Standby)
    - 500 mW max. (Op. Power)
  - MB8464-10L/-15L
    - 1.1 mW max. (Standby)
    - 330 mW max. (Op. Power)
- Single +5V supply voltage (±10% tolerance)
- Common data inputs and output
- TTL compatible inputs and output
- Low data retention voltage: 2.0V min.
- Standard 28-pin DIP

MB8464-10
MB8464-10L
MB8464-15
MB8464-15L

PIN ASSIGNMENT

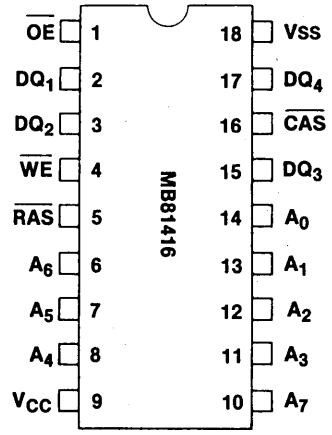


MB81416 64K (16K x 4) DYNAMIC RAM

- Organized as 16,384 words by 4-bits
- Fast Access Times:
  - MB81416-10 100 ns max.
  - MB81416-12 120 ns max.
  - MB81416-15 150 ns max.
- Cycle Times:
  - MB81416-10 200 ns min.
  - MB81416-12 230 ns min.
  - MB81416-15 270 ns min.
- Low Power Consumption:
  - MB81416-10:
    - 330 mW (Active)
  - MB81416-12:
    - 303 mW (Active)
  - MB81416-15:
    - 275 mW (Active)
  - All devices:
    - 25 mW max. (Standby)
- Single +5V supply voltage (±10% tolerance)
- On-chip substrate bias generator for high performance
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- 128 refresh cycles ($A_0 \sim A_6$), 2 ms
- Output unlatched at cycle end
- Early Write or $\overline{OE}$ to Control Output buffer impedance
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- Read-Modify-Write, page-mode operation and $\overline{RAS}$-only refresh capability
- On-chip latches for addresses and data-in
- Standard 18-pin DIP

MB81416-10
MB81416-12
MB81416-15

PIN ASSIGNMENT



A_0-A_7	Address Inputs
$\overline{CAS}$	Column Address Strobe
DQ_1-DQ_4	Data
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Write Enable
V_{CC}	+5 V Supply
V_{SS}	Ground

For complete data sheets contact: Fujitsu Microelectronics • 2985 Kifer Road • Santa Clara, CA 95051 • (408) 727-1700 • Telex I/II: 910-338-0190

FUJITSU
MICROELECTRONICS

MB8264
MB8265
MB8264A
MB8265A
MB8266A

NMOS 65,536-BIT DYMAMIC RANDOM ACCESS MEMORIES

MB8264/MB8265 GENERAL DESCRIPTION

- Organized as 65,536 x 1
- Address Access Times:
  MB8264-15/MB8265-15 150 ns max.
  MB8264-20/MB8265-20 200 ns max.
- Cycle Times:
  MB8264-15/MB8265-15 270 ns min.
  MB8264-20/MB8265-20 270 ns min.
  Low Power Dissipation:
  MB8264-15: 303 mW Max. (Active)
  MB8264-20: 248 mW Max. (Active)
  Both: 28 mW Max. (Standby)
  MB8265: 253 mW (REFRESH cycling, $\overline{RAS}$, $\overline{CAS}$ high)
- ±5V supply voltage, ±10% tolerance
- 128 refresh cycles (2 ms interval)
- On-chip substrate bias generator
- TTL compatible inputs, low capacitive load
- Three-state compatible output
- Common I/O capability using "Early Write" operation
- Output unlatched at cycle end allows extended page boundary and two-dimensional chip select
- Read-Modify-Write, $\overline{RAS}$-only Refresh and Page-mode capability
- On-chip latches for Addresses and Data-in
- Industry standard 16-pin package

MB8264 SPECIAL FEATURES

- Hidden Refresh capability
- "Gated" $\overline{CAS}$ feature
- Available tested to Fujitsu Mil-Std 883 Class B in extended temp. range of −55°C to 110°C as part numbers MB8264-15-SB/MB8264-20-SB

MB8265 SPECIAL FEATURES

- Pin 1 controls Refresh Function
- Refresh eliminates need to generate refresh addresses externally
- Hidden $\overline{RFSH}$ Refresh Cycle
- Output Data can be held indefinitely by $\overline{CAS}$
- On-chip refresh control generator and refresh address counter

MB8264A/MB8265A/MB8266A GENERAL DESCRIPTION

- Organized as 65,536 x 1
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row Access Time:
  MB8264A-10/65A-10/66A-10: 100 ns max.
  MB8264A-12/65A-12/66A-12: 120 ns max.
- Cycle Time:
  MB8264A-10/65A-10/66A-10: 200 ns min.
  MB8264A-12/65A-12/66A-12: 230 ns min.
- Single +5V supply voltage, ±10% tolerance
- On-chip substrate bias generator
- All inputs TTL compatible, low capacitive load
- Three-state compatible output
- Common I/O capability using "Early Write" operation
- Output unlatched at cycle end allows extended page boundary and two-dimensional chip select
- On-chip latches for Addresses and Data-in
- 128 refresh cycles

MB8264A SPECIAL FEATURES

- Low power:
  275 mW active (MB8264A-10)
  250 mW active (MB8264A-12)
  22 mW Standby (max.)
- "Gated" $\overline{CAS}$
- Read-Modify-Write, $\overline{RAS}$-only refresh, Hidden refresh and Page-mode capability
- Available tested to Fujitsu Mil-Std 883 Class B in extended temp. range of −55°C to 110°C as part numbers MB8264A-15-SB/MB8264A-20-SB

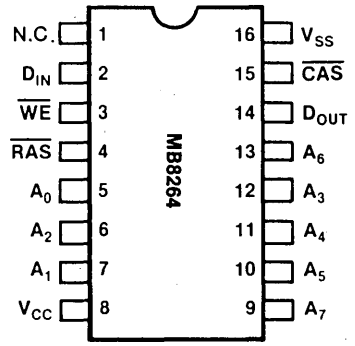
MB8266A SPECIAL FEATURES

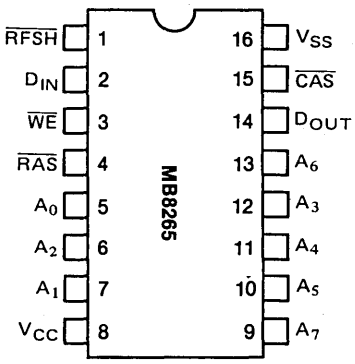
- Nibble Mode capability (A_3 & A_6)
- Low power:
  275 mW active (MB8266A-10)
  250 mW active (MB8266A-12)
  25 mW Standby (max.)
- Nibble Access Time:
  MB8266A-10 25 ns max.
  MB8266A-12 30 ns max.
- Nibble Cycle Time:
  MB8266A-10 60 ns min.
  MB8266A-12 70 ns min.
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- Read-Modify-Write and $\overline{RAS}$-only refresh capability

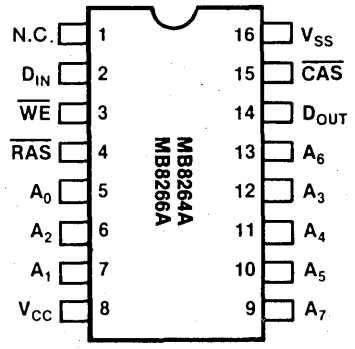
MB8265A SPECIAL FEATURES

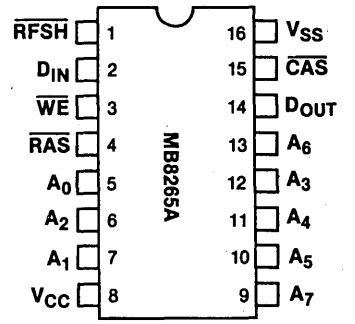
- Low power:
  330 mW active (MB8265A-10)
  300 mW active (MB8265A-12)
  25 mW Standby (max.)
- Pin 1 Refresh capability
- Offers two variations of hidden refresh
- Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-mode capability

PIN ASSIGNMENTS









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FUJITSU
MICROELECTRONICS

MBM2764
MBM27C64
MBM27128

64K AND 128K UV EPROMS

MBM2764 FEATURES

- Organized as 8192 x 8
- Address Access Times:
  - MBM2764-20 200 ns max.
  - MBM2764-25 250 ns max.
  - MBM2764-30 300 ns max.
  - MBM2764-30X 300 ns max.
- Low Power Dissipation:
  - I_{CC} (Active) = 150 mA max.
  - I_{CC} (Standby) = 35 mA max.
- Available in extended temp. ranges, −40°C to +85°C and −55°C to +125°C
- Single +5V supply voltage
- Static operation, no clocks required
- TTL compatible inputs and outputs
- Two level chip control
  - Output Enable ($\overline{OE}$) controls output buffers and eliminates bus contention problems
  - Chip Enable ($\overline{CE}$) controls standby operation
- Compatible with high speed 8 MHz 8086-2 MPU; zero wait state
- Three-state output with OR-tie capability
- Single location programming
- Programs with one 50 ms pulse

MBM27C64 FEATURES

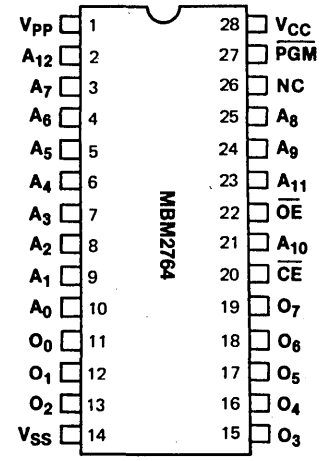
- CMOS Power Consumption:
  - 500μW max. (Standby)
  - 5μW typ. (Standby)
  - 40mW/MHz (Active)
- Organized as 8192 x 8
- Utilizes same simple programming requirements as NMOS MBM2764
- Single location programming
- Programming pulse may be reduced to 25 ns to cut programming time in half
- No clock required, fully static operation
- TTL compatible inputs/outputs
- Three-state output with OR-tie capability
- Available in extended temp. ranges, −40°C to +85°C and −55°C to +125°C
- Fast Access Time:
  - MBM27C64-25 250 ns max.
  - MBM27C64-30 300 ns max.
- Single +5V operation
- Pin and function compatible with 2764-type devices

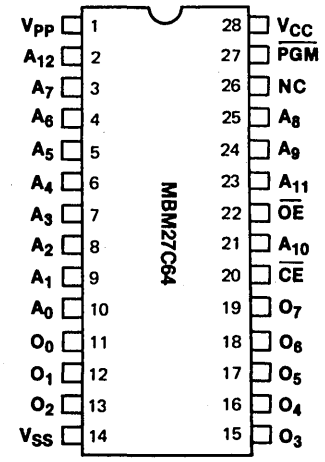
MBM27128 FEATURES (PRELIMINARY)

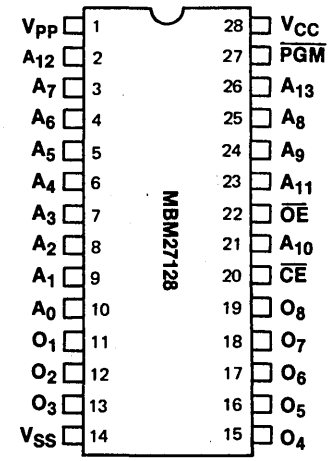
- Organized as 16,384 x 8
- Fast Access Times:
  - MBM27128-25 250 ns max.
  - MBM27128-30 300 ns max.
- Simple programming requirements
- Single location programming
- Programs with one 50 ms pulse
- Low power requirements:
  - 525 mW (Active)
  - 184 mW (Standby)
- No clocks required, fully static operation
- TTL compatible inputs and outputs
- Three-state output with OR-tie capability
- Output Enable ($\overline{OE}$) pin for easy memory expansion
- Single +5V supply voltage
- Pin compatible with Intel 27128

PIN ASSIGNMENTS

All packages meet Jedec standards







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FUJITSU
MICROELECTRONICS

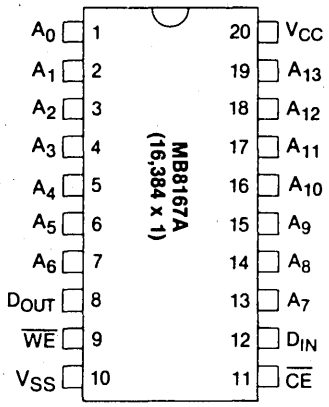
MB8167A
MB8168

NMOS 16,384-BIT STATIC RANDOM ACCESS MEMORIES

MB8167A FEATURES

- Organized as 16,384 words by 1-bit
- Static operation: no clocks or refresh required
- Fast Access Times:
  MB8167A-45 45 ns max.
  MB8167A-55 55 ns max.
  MB8167A-70 70 ns max.
- Separate data input and output
- TTL compatible inputs and output
- Single +5V supply voltage
- Three-state output with OR-tie capability
- Chip enable for easy memory expansion and automatic power down
- All inputs and output have protection against static charge
- Available in extended temperature range from −55°C to +125°C as part numbers MB8167A-70-W and MB8167A-85-W (Standard manufacturing and testing flow)
- Available in extended temperature range from −55°C to +125°C as part numbers MB8167A-70-SB and MB8167A-85-SB (Fujitsu's Mil-Std 883 Class B manufacturing and testing flow)
- Standard 20-pin DIP

MB8167A-45
MB8167A-55
MB8167A-7O
PIN ASSIGNMENT

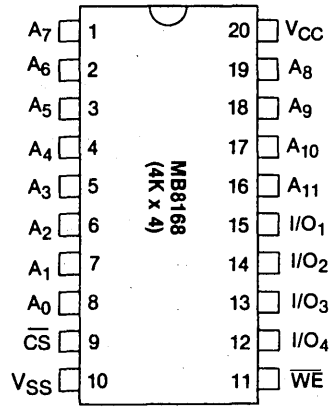


- Pin compatible with Inmos IMS1400

MB8168 FEATURES

- Organized as 4096 words by 4-bits
- Static operation: no clock or refresh required
- Fast Access Times:
  MB8168-55 55 ns max.
  MB8168-70 70 ns max.
- Common data input and output
- TTL compatible inputs and output
- Single +5V supply voltage
- Three-state output with OR-tie capability
- Chip select for easy memory expansion and automatic power down
- All inputs and output have protection against static charge
- Available in extended temperature range from −55°C to +125°C as part numbers MB8168-70-W and MB8168-85-W (Standard manufacturing and testing flow)
- Available in extended temperature range from −55°C to +125°C as part numbers MB8168-70-SB and MB8168-85-SB (Fujitsu Mil-Std 883 Class B manufacturing and testing flow)
- Standard 20-pin DIP

MB8168-55
MB8168-7O
PIN ASSIGNMENT



- Pin compatible with Inmos IMS1420

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FUJITSU
MICROELECTRONICS

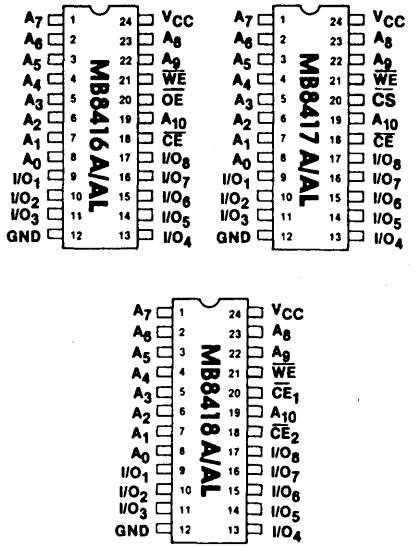
CMOS 16384-BIT STATIC RAMS

MB8416A/AL
MB8417A/AL
MB8418A/AL

GENERAL DESCRIPTION

- Organized as 2048 x 8
- Address Access Times:
  MB8416A/8417A/8418A-12(-12L) 120 ns max.
  MB8416A/8417A/8418A-15(15-L) 150 ns max.
- Low Power Dissipation:
  I_{CC} (Active) = 60 mA max.
  I_{SB} (Standby) = I_{CCDR} (Data Retention)
  MB8416A/17A/18A-12L & MB8416A/17A/18A-15L = 50μA
  MB8416A/17A/18A-12 & MB8416A/17A/18A-15 = 2 mA
- Data Retention 2.0V min.
- Single +5V supply voltage, ± 10% tolerance
- Completely static operation, no clocks required
- Equal Access and Cycle Times
- Two Level chip control
  - Chip Select
  - Output Enable
- Fast $\overline{OE}$ Access Times:
  MB8416A/17A/18A-12(-12L) = 50 ns
  MB8416A/17A/18A-15(-15L) = 60 ns
- Output timing reference levels: 0.8V-2.2V
- TTL compatible inputs and outputs
- Plug-in compatible with 16K EPROMS
- Industry standard 24-pin DIP package

PIN ASSIGNMENTS



SPECIAL FEATURES

MB8416 A/AL
- $\overline{CE}$ (Pin 18) control for simple memory expansion, standby power and data retention
- $\overline{OE}$ (Pin 20) control for fast memory access, output buffer control and elimination of bus contention problems
- $\overline{OE}$ Access Time - 100 ns Max.
- Pin and function compatible with 2716 EPROM
- Pin compatible with HM6116, TC5517, μPD446

MB8417 A/AL
- $\overline{CE}$ (Pin 18) control for simple memory expansion, standby power and data retention
- $\overline{CS}$ (Pin 20) control for simple memory expansion
- $\overline{CS}$ Access Time - 100 ns Max.
- Pin compatible with TC5516, μPD447

MB8418 A/AL
- Both $\overline{CE}_2$ (Pin 18) and $\overline{CE}_1$ (Pin 20) provide power down capability
- $\overline{CE}_2$ and $\overline{CE}_1$ provide simple memory expansion
- $\overline{CE}_2$ and $\overline{CE}_1$ Access Time - 200 ns Max.
- Pin compatible with TC5518

DEVICE NUMBER	MB8416A/AL					MB8417A/AL					MB8418A/AL				
PIN NUMBER	18	20	21	24	9-11 13-17	18	20	21	24	9-11 13-17	18	20	21	24	9-11 13-17
PIN NAME / MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	SUPPLY CURRENT	I/O	$\overline{CE}$	$\overline{CS}$	$\overline{WE}$	SUPPLY CURRENT	I/O	$\overline{CE}_2$	$\overline{CE}_1$	$\overline{WE}$	SUPPLY CURRENT	I/O
WRITE	L	X	L	I_{CC}	D_{IN}	L	L	L	I_{CC}	D_{IN}	L	L	L	I_{CC}	D_{IN}
READ	L	L	H	I_{CC}	D_{OUT}	L	L	H	I_{CC}	D_{OUT}	L	L	H	I	D_{OUT}
OUTPUT DISABLE	L	H	H	I_{CC}	HIGH Z	—	—	—	—	—	—	—		—	—
CHIP DESELECT	—	—	—	—	—	L	H	X	I_{CC}	HIGH Z	—	—	—	—	—
STANDBY 1	—	—	—	—	—	—	—	—	—	—	X	H	X	I_{SB1}	HIGH Z
STANDBY 2	H	X	X	I_{SB}	HIGH Z	H	X	X	I_{SB}	HIGH Z	H	X	X	I_{SB2}	HIGH Z

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FUJITSU
MICROELECTRONICS

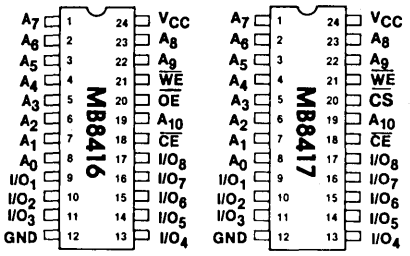
MB8416
MB8417
MB8418

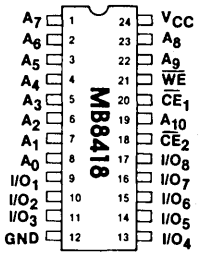
CMOS 16384-BIT STATIC RAMS

GENERAL DESCRIPTION

- Organized as 2048 x 8
- Address Access Time - 200 ns Max.
- Low Power Dissipation - I_{CC} (Active) = 60 mA Max.
  I_{SB} (Standby) = 10μA Max. at 85°C
  I_{CCDR} (Data Retention) = 10 μA Max. at 85°C
- Operating Temperature Range: −40°C to +85°C
- Available in extended temperature range (Standard manufacturing and testing flow) of −55°C to +125°C as part numbers MB8416-25-W, MB8417-25-W and MB8418-25-W
- Available in extended temperature range (MIL-Std 883 Class B manufacturing and testing flow) of −55°C to +125°C as part numbers MB8416-25-SB, MB8417-25-SB and MB8418-25-SB
- Data Retention 2.0V Min.
- Single +5V DC supply, ±10% tolerance
- Completely static operation, no clocks required
- Equal Access and Cycle Times
- Two Level chip control • Chip Select • Output Enable
- Fast $\overline{OE}$ Access Time: 100 ns Max.
- Output timing reference levels - 0.8V - 2.2V
- TTL compatible inputs and outputs
- Plug-in compatible with 16K EPROMS
- Industry standard 24-pin DIP package

PIN ASSIGNMENTS





SPECIAL FEATURES

MB8416
- $\overline{CE}$ (Pin 18) control for simple memory expansion, standby power and data retention
- $\overline{OE}$ (Pin 20) control for fast memory access, output buffer control and elimination of bus contention problems
- $\overline{OE}$ Access Time - 100 ns Max.
- Pin and function compatible with 2716 EPROM
- Pin compatible with HM6116, TC5517, μPD446

MB8417
- $\overline{CE}$ (Pin 18) control for simple memory expansion, standby power and data retention
- $\overline{CS}$ (Pin 20) control for simple memory expansion
- $\overline{CS}$ Access Time - 100 ns Max.
- Pin compatible with TC5516, μPD447

MB8418
- Both $\overline{CE}_2$ (Pin 18) and $\overline{CE}_1$ (Pin 20) provide power down capability
- $\overline{CE}_2$ and $\overline{CE}_1$ provide simple memory expansion
- $\overline{CE}_2$ and $\overline{CE}_1$ Access Time - 200 ns Max.
- Pin compatible with TC5518

TRUTH TABLE

DEVICE NUMBER	MB8416					MB8417					MB8418				
PIN NUMBER	18	20	21	24	9-11 13-17	18	20	21	24	9-11 13-17	18	20	21	24	9-11 13-17
PIN NAME / MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	SUPPLY CURRENT	I/O	$\overline{CE}$	$\overline{CS}$	$\overline{WE}$	SUPPLY CURRENT	I/O	$\overline{CE_2}$	$\overline{CE_1}$	$\overline{WE}$	SUPPLY CURRENT	I/O
WRITE	L	X	L	I_{CC}	D_{IN}	L	L	L	I_{CC}	D_{IN}	L	L	L	I_{CC}	D_{IN}
READ	L	L	H	I_{CC}	D_{OUT}	L	L	H	I_{CC}	D_{OUT}	L	L	H	I	D_{OUT}
OUTPUT DISABLE	L	H	H	I_{CC}	HIGH Z	—	—	—	—	—	—	—		—	—
CHIP DESELECT	—	—	—	—	—	L	H	X	I_{CC}	HIGH Z	—	—	—	—	—
STANDBY 1	—	—	—	—	—	—	—	—	—	—	X	H	X	I_{SB1}	HIGH Z
STANDBY 2	H	X	X	I_{SB}	HIGH Z	H	X	X	I_{SB}	HIGH Z	H	X	X	I_{SB2}	HIGH Z

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FUJITSU
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MB7143E
MB7144E

HIGH SPEED SCHOTTKY TTL 64K PROMS

NEW PRODUCT FOR 1983

GENERAL DESCRIPTION

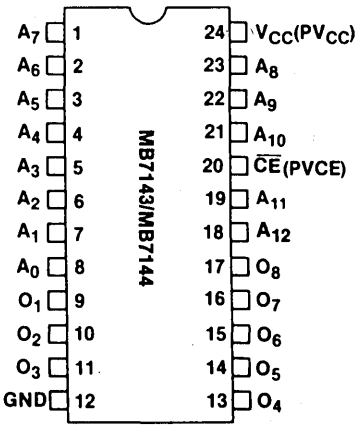
The Fujitsu MB7143 and MB7144 are high speed Schottky TTL electrically field programmable read only memories. With uncommitted collector outputs on the MB7143 and three-state outputs on the MB7144, memory expansion is simple.

The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be programmed by the highly reliable DEAP™ (Diffused Eutectic Aluminum Process) according to simple programming procedures.

The sophisticated passive isolation, termed IOP (Isolation by Oxide and Polysilicon), with thin epitaxial layer and Schottky TTL process permits minimal chip size and fast access time.

The extra test cells and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform AC, DC and programming test prior to shipment. This results in extremely high programmability.

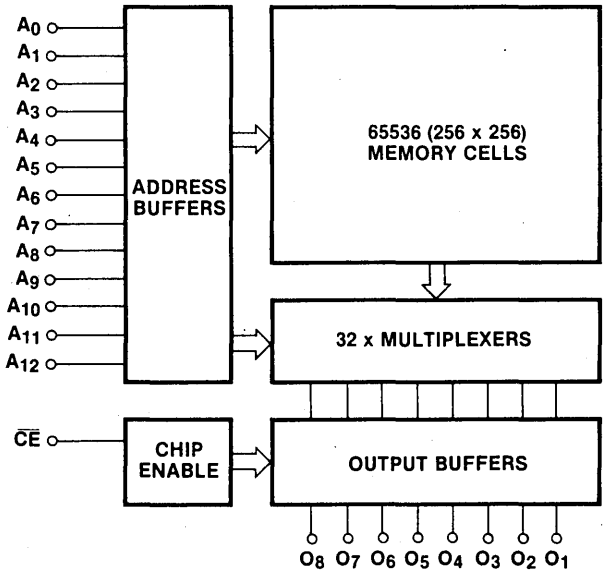
PIN ASSIGNMENT



FEATURES

- **Organized as 8192 x 8**
- **Fast Access Times:**
  40 ns Typ.
  MB7143E/MB7144E:
  65 ns max.
  MB7143H/MB7144H:
  55 ns max.
- **Single +5V supply voltage**
- **Simplified and lower power programming**
- **Low current PNP inputs**
- **AC characteristics guaranteed over full operating voltage and temperature range via unique testing techniques**
- **TTL compatible inputs and outputs**
- **Proven high programmability and reliability**
- **Standard 24-pin DIP package**
- **Jedec approved pin-out**

MB7143/MB7144 BLOCK DIAGRAM



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HIGH SPEED SCHOTTKY TTL PROMS

FEATURES

- Many organizations in 4K to 64K densities
- Choice of three-state or open collector output on all devices
- Proven high programmability and reliability of DEAP™ (Diffused Eutectic Aluminum Process) PROMS
- Single +5V supply voltage
- TTL compatible input/output
- Simplified and lower power programming
- Commercial and Extended Temperature Ranges (−55°C to +125°C) available
- Low current PNP inputs
- Chip enable leads for easy memory expansion
- Most PROMS are multiply sourced
- Industry standard pin assignments and packages

COMMERCIAL TEMPERATURE RANGE PROMS

Device Number	Density	Organization	Max. Access Time (ns)	Typ. Access Time (ns)	Power Max. (mW)	Output Type	Package
MB7121E	4K	1024 x 4	45	25	787	0C	18-pin DIP
MB7121H	4K	1024 x 4	35	25	787	0C	
MB7122E	4K	1024 x 4	45	25	787	3S	
MB7122H	4K	1024 x 4	35	25	787	3S	
MB7123E	4K	512 x 8	45	25	850	0C	300 mil wide 20-pin DIP
MB7123H	4K	512 x 8	35	25	850	0C	
MB7124E	4K	512 x 8	45	25	850	3S	
MB7124H	4K	512 x 8	35	25	850	3S	
MB7127E	8K	2048 x 4	55	30	820	0C	18-pin DIP
MB7127H	8K	2048 x 4	45	30	820	0C	
MB7127Y	8K	2048 x 4	35	25	820	0C	
MB7128E	8K	2048 x 4	55	30	820	3S	
MB7128H	8K	2048 x 4	45	30	820	3S	
MB7128Y	8K	2048 x 4	35	25	820	3S	
MB7131E	8K	1024 x 8	55	35	920	0C	24-pin DIP
MB7131H	8K	1024 x 8	45	35	920	0C	
MB7131Y	8K	1024 x 8	35	25	920	0C	
MB7132E	8K	1024 x 8	55	35	920	3S	
MB7132H	8K	1024 x 8	45	35	920	3S	
MB7132Y	8K	1024 x 8	35	25	920	3S	
MB7134E	16K	4096 x 4	55	35	850	3S	400 mil wide 20-pin DIP
MB7134H	16K	4096 x 4	45	35	850	3S	
MB7137E	16K	2048 x 8	55	30	950	0C	24-pin DIP
MB7137H	16K	2048 x 8	45	30	950	0C	
MB7138E	16K	2048 x 8	55	30	950	3S	
MB7138H	16K	2048 x 8	45	30	950	3S	
MB7141E	32K	4096 x 8	65	45	975	0C	
MB7141H	32K	4096 x 8	55	45	975	0C	
MB7142E	32K	4096 x 8	65	45	975	3S	
MB7142H	32K	4096 x 8	55	45	975	3S	
MB7143H	64K	8192 x 8	55	45	975	0C	
MB7144H	64K	8192 x 8	55	45	975	3S	

EXTENDED TEMPERATURE RANGE PROMS (−55°C to +125°C)

MB7128-W*	8K	2048 x 8	55	30	820	3S	18-pin DIP 18-pin FLATPACK 28-pad LCC
MB7132E-W*	8K	1024 x 8	55	35	920	3S	24-pin DIP 24-pin FLATPACK 28-pad LCC
MB7138E-W*	16K	2048 x 8	55	30	950	3S	
MB7142E-W*	32K	4096 x 8	65	45	975	3S	

*Also available with open collector output

FUJITSU
MICROELECTRONICS

MBM10480
MBM100480

10K/100K ECL RANDOM ACCESS MEMORIES

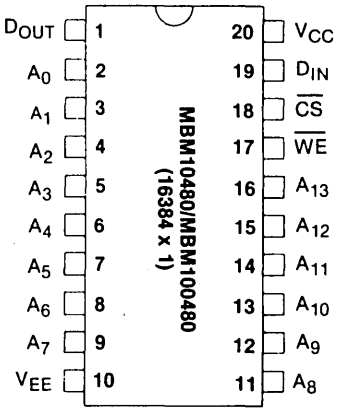
GENERAL DESCRIPTION

The Fujitsu MBM10480 and MBM100480 are fully decoded 16,384-bit ECL read/write random access memories designed for high speed scratch pad, microprocessor and buffer storage applications. These devices are organized as 16,384 words by one-bit and they feature on-chip voltage compensation for improved noise margin.

The MBM10480 and MBM100480 offer extremely small cell and chip sizes, achieved through the use of Fujitsu's patented DOPOS (Doped Polysilicon) as well as IOP (Isolation by Oxide and Polysilicon) processing. As a result, very fast access times with high yields and outstanding device reliability are achieved in volume production.

Operation for the MBM10480 and MBM100480 is specified over a temperature range from 0°C to 75°C (ambient). They are packaged in industry standard 20-pin DIP packages and are fully compatible with industry standard 10K and 100K ECL families.

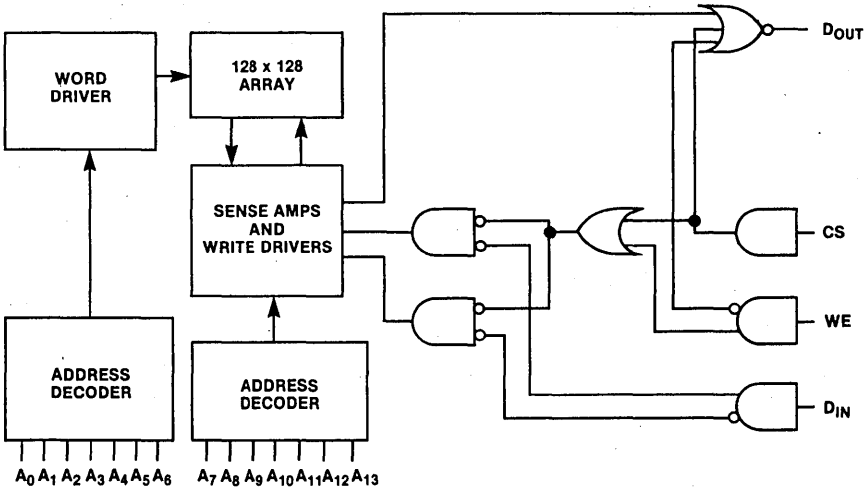
PIN ASSIGNMENT



FEATURES

- **Organized as 16,384 words by one-bit**
- **On-chip voltage compensation for improved noise margin**
- **Address Access Time:**
  25 ns max.
- **Chip Select Access Time:**
  15 ns max.
- **Open emitter output for easy memory expansion**
- **Supply Voltage**
  MBM10480: −5.2V
  MBM100480: −4.5V
- **Low Power Dissipation:**
  MBM10480: 0.05 mW/bit
  MBM100480: 0.04 mW/bit
- **DOPOS and IOP processing**
- **Fully compatible with industry standard 10K and 100K ECL families**
- **Pin compatible with F10480 and F100480**

MBM10480/MBM100480 BLOCK DIAGRAM



TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{OUT}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't Care

For complete data sheets contact: Fujitsu Microelectronics • 2985 Kifer Road • Santa Clara, CA 95051 • (408) 727-1700 • Telex I/II: 910-338-0190

FUJITSU
MICROELECTRONICS

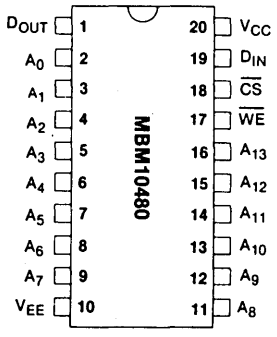
10K/100K ECL RAM SERIES

FEATURES

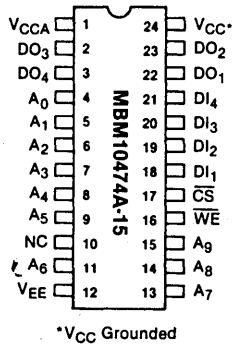
- On-chip voltage compensation for improved noise margin
- Fully compatible with industry standard 10K and 100K ECL families
- Open emitter output for easy memory expansion
- Low power dissipation (see chart below)
- DOPOS (Doped Polysilicon) and IOP (Isolation by Oxide and Polysilicon) processing

Device Number	Density	Organization	Access Time Max. (ns)	Access Time Typ. (ns)	Power (mW)	Package
MB7072E	1K	256 x 4	12	9	1040	22-pin DIP
MBM10415AH	1K	1K x 1	20	13	780	16-pin DIP
MBM10422	1K	256 x 4	10	8	1040	24-pin DIP
MBM10422A-7	1K	256 x 4	7	5.5	1040	24-pin DIP
MBM10470A-20	4K	4K x 1	20	13	900	18-pin DIP
MBM10470A-10	4K	4K x 1	10	8	1040	18-pin DIP
MBM10474A-15	4K	1K x 4	15	12	700	24-pin DIP
MBM10480	16K	16K x 1	25	20	900	20-pin DIP
MBM100422A-7	1K	256 x 4	7	5.5	900	24-pin DIP
MBM100470A-10	4K	4K x 1	10	8	900	18-pin DIP
MBM100474A-15	4K	1K x 4	15	12	900	24-pin DIP
MBM100480	16K	16K x 1	25	20	700	20-pin DIP

16K x 1 (25 ns)

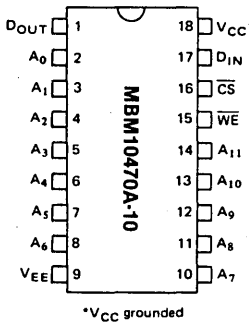


1K x 4 (15 ns)



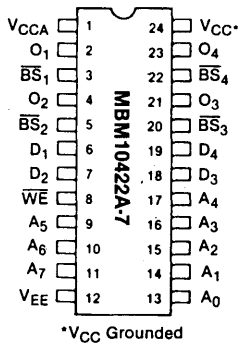
*V_{CC} Grounded

4K x 1 (10 ns)



*V_{CC} grounded

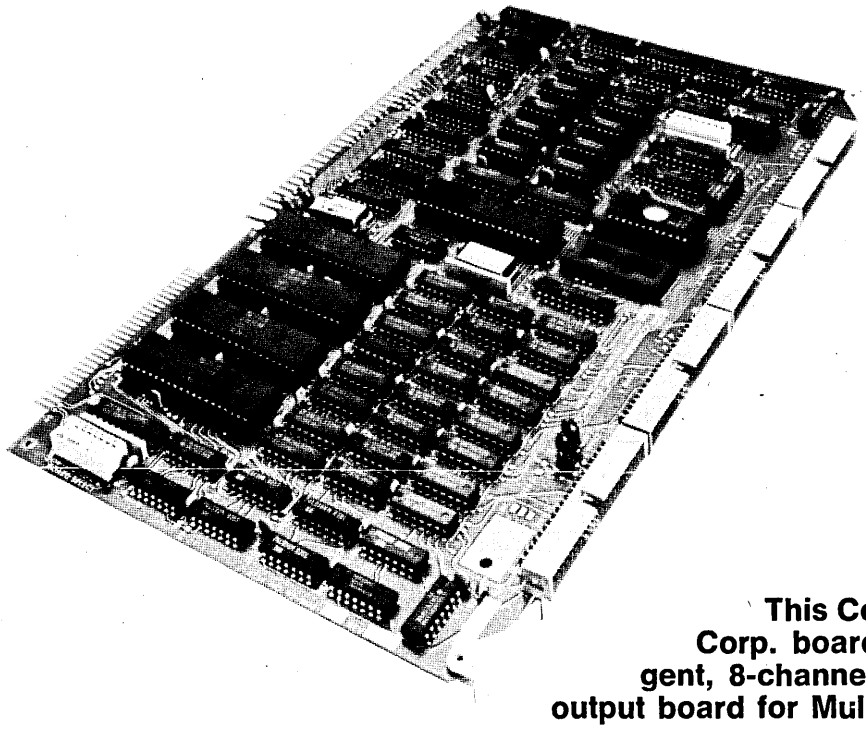
256 x 4 (7 ns)



*V_{CC} Grounded

For complete data sheets contact: Fujitsu Microelectronics • 2985 Kifer Road • Santa Clara, CA 95051 • (408) 727-1700 • Telex I/II: 910-338-0190

For Key Data On Every IC On This Board, The Place To Look Is...



This Codata Systems Corp. board is an intelligent, 8-channel serial input/output board for Multibus systems.

Equipment and system design often require the use of a wide variety of integrated circuits in order to obtain optimum performance. One way for an engineer to be certain that he hasn't overlooked the best device for his application is to refer to the pages of IC MASTER.

Surveys conducted by IC MASTER, integrated circuit manufacturers, and independent research agencies confirm that four out of five IC MASTER users have specified one or more products as the result of using IC MASTER.

Device No.	Description
AM25LS2521	8-Bit, Equal-to Comparator
AM26LS29	Line Driver, Single-Ended
AM26LS32	Line Receiver, Differential
74LS02	Quad 2-Input NOR Gate
74LS08	Quad 2-Input AND Gate
74LS32	Quad 2-Input OR Gate
74LS74	Dual D-Type Positive Edge Triggered Flip-Flop with Preset and Clear
74LS138	3 Line to 8 Line Decoder/Demultiplexer
74LS164	8-Bit Gated Serial-In, Parallel-Out Shift Register
74LS244	Octal Bus Driver (Schmitt trigger) Non-Inverting, 3-State, Complementary Control
74LS273	Octal D-Type Edge-Triggered Flip-Flop
MBM2716	Fujitsu 248 by 8 PROM
SN74LS04	Hex Inverter
SN74LS133	13-Input NAND Gate
SN74S240	Octal Buffer/Line.Driver/Line Receiver Inverted 3-State Outputs
Z80A	Zilog 8-Bit Microprocessor
Z8530	Zilog Serial Communications Controller

Representative list of ICs on Codata Systems Corp. board for data communications equipment.

IC MASTER

BE SURE. BEGIN WITH THE IC MASTER

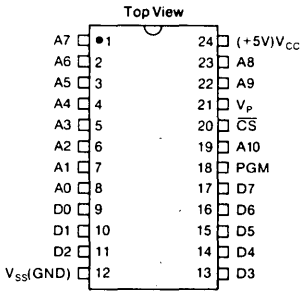
16K N-Channel Electrically Erasable and Programable ROM

FEATURES

- 2048 Word x 8 Bit Organization, Fully Decoded
- Electrically Block Erasable with 1sec, +25V Pulse
- Electrically Programable — 1ms per Byte
- Single +5V Power Supply in Read Mode
- 300ns Access Time
- 10 year Non-Volatile Data Retention
- Static Operation — No Clocks
- N-Channel, Silicon Gate SNOS Technology
- Low Active Power Dissipation: 300mW max
- Pin for Pin Compatible with Hitachi HN48016
- Interchangeable with Intel 2716 EPROM

PIN CONFIGURATION

24 pin dual in line



DESCRIPTION

The ER5716 is an Electrically Erasable and Programable Read Only Memory fabricated in N-Channel, Silicon Gate SNOS technology. Address decoding circuitry is provided on the chip and its operation is fully static, requiring no clocks. +5 volts only is required to perform a Read operation. An additional +25V supply is necessary in the Erase and Write modes.

This device is pin for pin compatible with the Hitachi HN48016 and is also interchangeable with the 2716 family of ultraviolet erasable EPROMs.

Being electrically erasable and programable, the ER5716 need never be removed from the system for reprograming since it may be performed, in the circuit, under system or end-user control. Also eliminated is the danger of accidental erasure of data by ultraviolet irradiation.

ER5716 VERSUS 2716

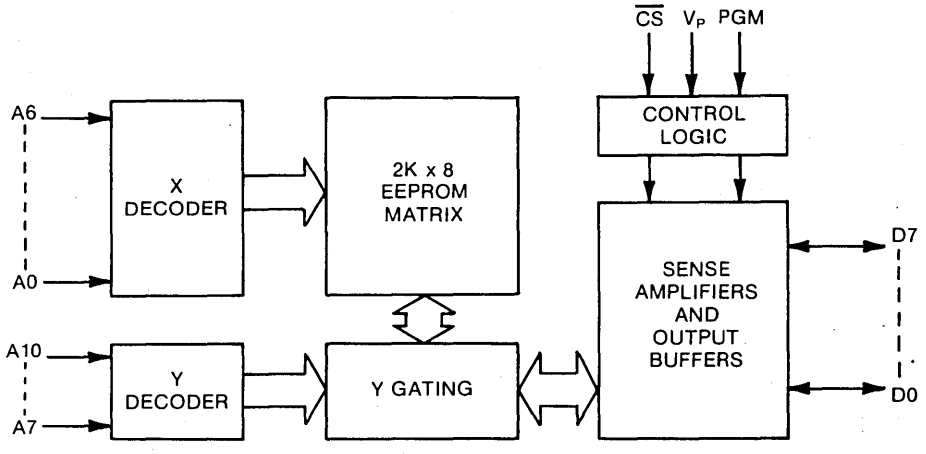
All pins of the two devices are functionally identical with the exception of pins 18 and 20. In order to make the ER5716 electrically alterable, the independent functions of Chip Enable and Output Enable for the 2716 have been combined in the Chip Select ($\overline{CS}$) function of the ER5716, pin 20. Pin 18 retains the Program or Write function, but no longer serves as Chip Enable.

DEVICE OPERATION

V_P (pin 21) requires a d.c. supply of +25V in the Erase and Write modes, but remains at +5V for all other operations. Reading may occur with V_P at either level, however continuous operation of the device with V_P at 25V is not recommended.

Writing of data into the memory need not be sequential, it may be performed at any randomly selected byte location. However, writing is possible only after an Erase operation which removes all previously programed data from the entire memory: individual word erasures are not possible.

BLOCK DIAGRAM



MODES OF OPERATION

PGM	$\overline{CS}$	V_P	OPERATING MODE
0	0	+5	READ—Data presented at the output pins a time, t_A after an address change.
Don't care	1	+5	STANDBY—Chip deselected, data outputs in the high impedance state.
Pulsed 0 to 1	1	+25	SINGLE WORD WRITE—Data at the data inputs is written to the selected address location. NOTE that correct writing can occur only if the chip has been previously erased.
0	0	+25	PROGRAM VERIFY—Same as Read mode.
Pulsed 0 to 1	0	+25	ERASE—All 16,384 bits simultaneously erased to a logic '1' state.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs except V_P (with respect to V_{SS}) .... −0.3V to +7V
V_P (with respect to V_{SS}) ..... −0.3V to +28V
Storage temperature (with Data Retention) ..... −40°C to +85°C
Storage temperature (without Data Retention) ..... −65°C to +150°C
Soldering temperature of leads (10 seconds) ..... +300°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise noted):

V_{SS} = GND
V_{CC} = +5 ± 5% volts
Programming Voltage, V_P = +25V ± 1V
Operating Temperature range (T_A) = 0°C to +70°C
−40°C to +85°C
−55°C to +125°C

DC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Unit	Conditions
Input Logic "1"	V_{IH}	2	—	V_{CC}+0.3	V	
Input Logic "0"	V_{IL}	−0.3	—	0.8	V	
Input Logic "1" (V_P only)	V_{PH}	V_{CC}−0.6	—	V_{CC}+0.6	V	See Note 1
Output Logic "1"	V_{OH}	2.4	—	V_{CC}	V	I_{OH} = 100μA
Output Logic "0"	V_{OL}	V_{SS}	—	0.4	V	I_{OL} = 1.6mA
Input Leakage (Except Data)	I_L	—	—	2	μA	V_{IN} = 5.8V
Input Leakage (Data Pins)	I_{LD}	—	—	10	μA	V_{IN} = 5.8V
Output Leakage (Data Pins)	I_{OD}	—	—	10	μA	V_{OUT} = V_{CC} max
Power Supply Current						
V_P Supply:						
Read Mode	I_P	—	4	7	mA	V_P = 6.1V
Write Mode	I_P	—	5	10	mA	V_P = 26V
Erase Mode	I_P	—	5	10	mA	V_P = 26V
V_{CC} Supply:						
Read Mode	I_{CC}	—	32	50	mA	$\overline{CS}$ = V_{IH} or V_{IL}
Write Mode	I_{CC}	—	32	50	mA	$\overline{CS}$ = V_{IH} or V_{IL}
Erase Mode	I_{CC}	—	32	50	mA	$\overline{CS}$ = V_{IH} or V_{IL}
Power Dissipation						
Read Mode	P_{RD}	—	200	318	mW	V_{CC} = 5.5V, V_P = 6.1V
Write Mode	P_{WR}	—	306	535	mW	V_{CC} = 5.5V, V_P = 26V
Erase Mode	P_{ER}	—	306	535	mW	V_{CC} = 5.5V, V_P = 26V

NOTE: Characteristic data for ER5716IR/HR not available for inclusion at this time. Data available from General Instrument Distributors upon request.

AC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Unit	Conditions
Input Capacitance — Control Inputs	C_I	—	—	7.5	pf	f = 1MHz
Input Capacitance — Data Inputs	C_D	—	—	15	pf	f = 1MHz
Read Mode Characteristics						
Read Access Time	t_A	—	—	300	ns	
Chip Select to Data Out Delay	t_{D1}	—	—	120	ns	Output load: 1TTL gate + C_L = 100pf
Data Hold Time	t_{D2}	—	—	100	ns	
Address to Output Float Time	t_{D3}	10	—	—	ns	
Write Mode Characteristics						
Chip Deselect to Start of Write	t_{D11}	200	—	—	ns	
Address and Data Setup Time	t_{D12}	2	—	—	μs	
Data and $\overline{CS}$ Hold Time	t_{D13}	2	—	—	μs	
Chip Select to Output Delay	t_{D14}	—	—	120	ns	See Note 2
Address Hold Time	t_{D15}	2	—	—	μs	
PGM Pulse Width	t_{PW}	800	—	—	μs	
PGM Pulse Rise and Fall Times	t_r, t_f	5	—	—	ns	
Written State (data I/O)	V_W	—	V_{IL}, V_{OL}	—	V	
Erase Mode Characteristics						
$\overline{CS}$ Setup Time	t_{D21}	2	—	—	μs	
PGM to Output Delay	t_{D22}	2	—	—	μs	
PGM Pulse Width	t_{PE}	1	—	—	sec	
PGM Pulse Rise and Fall Times	t_r, t_f	5	—	—	ns	
Erased State (data I/O)	V_E	—	V_{IH} V_{OH}	—	V	

NOTES:
1. The wide tolerance of this parameter allows the use of a driver circuit for switching V_P between +5V for reading and +25V in the Erase and Write modes. Although all operations may be performed with +25V applied to the chip, continuous operation is not recommended under these conditions.
2. A Read immediately following a Write is not a required operation.

NOTE: Characteristic data for ER5716IR/HR not available for inclusion at this time. Data available from General Instrument Distributors upon request.

TIMING DIAGRAM

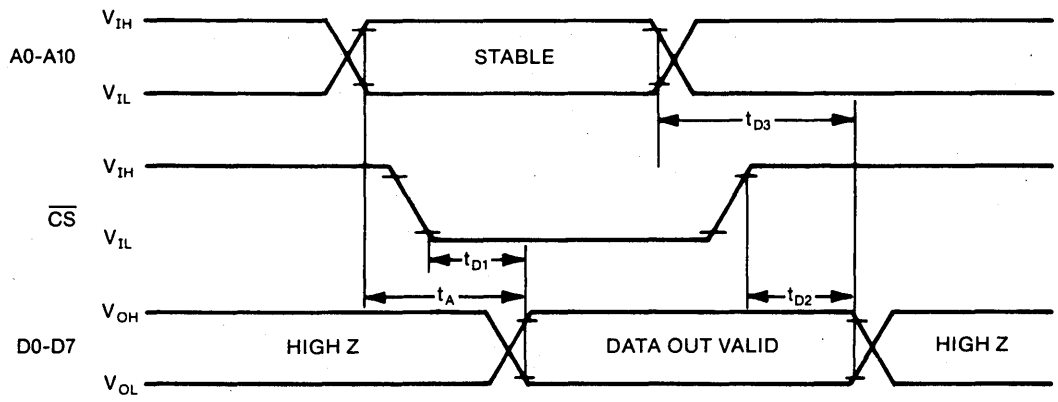


Fig. 1 READ MODE TIMING

TIMING DIAGRAMS

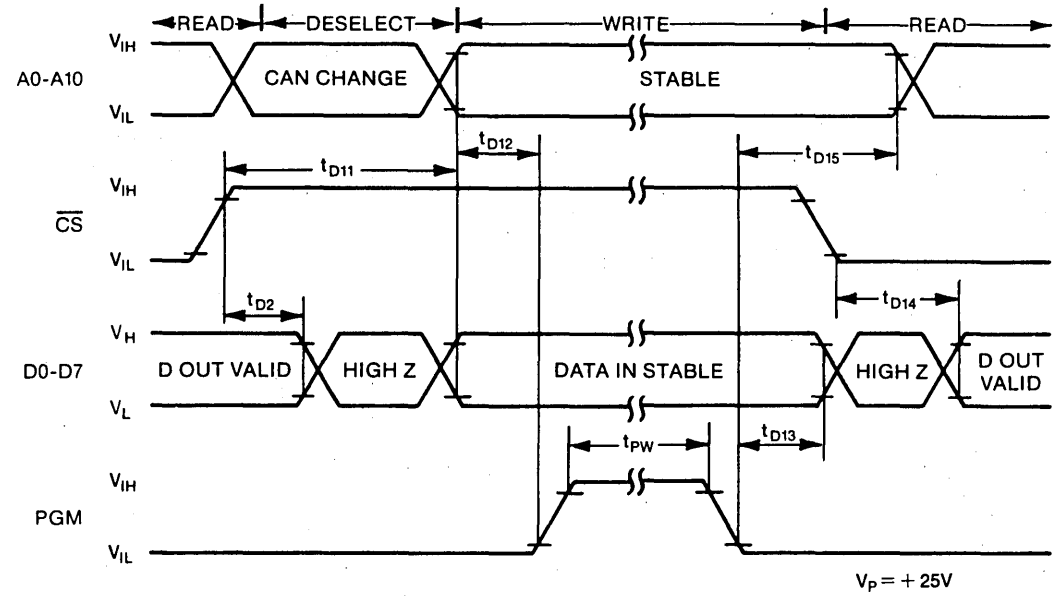


Fig. 2 WRITE MODE TIMING

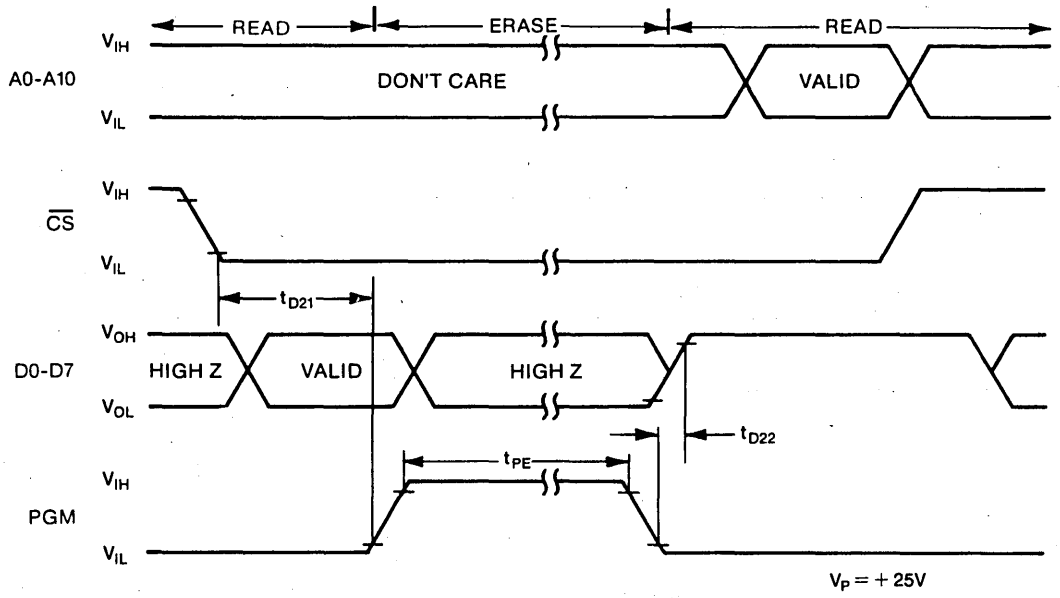


Fig. 3 ERASE MODE TIMING

Word Alterable 1K Bit Electrically Erasable and Programable ROM

FEATURES

- 1024 Bits, Organized 128 x 8
- N-Channel Si-Gate SNOS Technology
- +5V Operation in All Modes; No High Voltages
- Fully TTL Compatible Inputs and Outputs
- On-Chip Latching of Addresses and Data
- Self-Timing, Processor Transparent Programing Mode with RDY/$\overline{\text{BUSY}}$ Signal
- Address and Data Buses may be used Separately or Multiplexed
- $\overline{\text{CE}}$ and $\overline{\text{OE}}$ Inputs to Avoid Bus Contention
- Word Alterable
- Read Access time of Less Than 200ns
- 10 Years' Data Retention over Temperature Range of −40° to +85°C
- Unlimited Read Accesses

DESCRIPTION

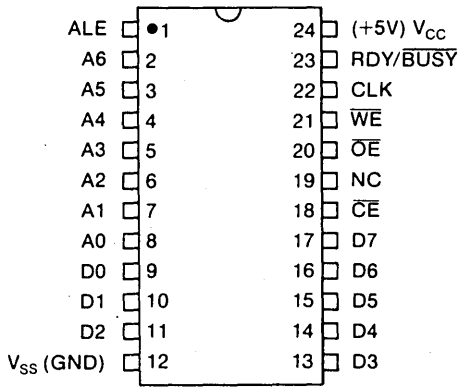
The ER5901 is a high speed electrically word erasable memory manufactured in the General Instrument proven SNOS technology. The key features of this device are its +5V only operation and microprocessor compatible architecture which allows the ER5901 to be accessed from the system bus in the same way as a static RAM.

Internal memory management has been incorporated in this device. On-board latching of address and data lines in the reprograming mode, and busy signal (RDY/$\overline{\text{BUSY}}$) output make this mode transparent to the host processor.

PIN CONFIGURATION

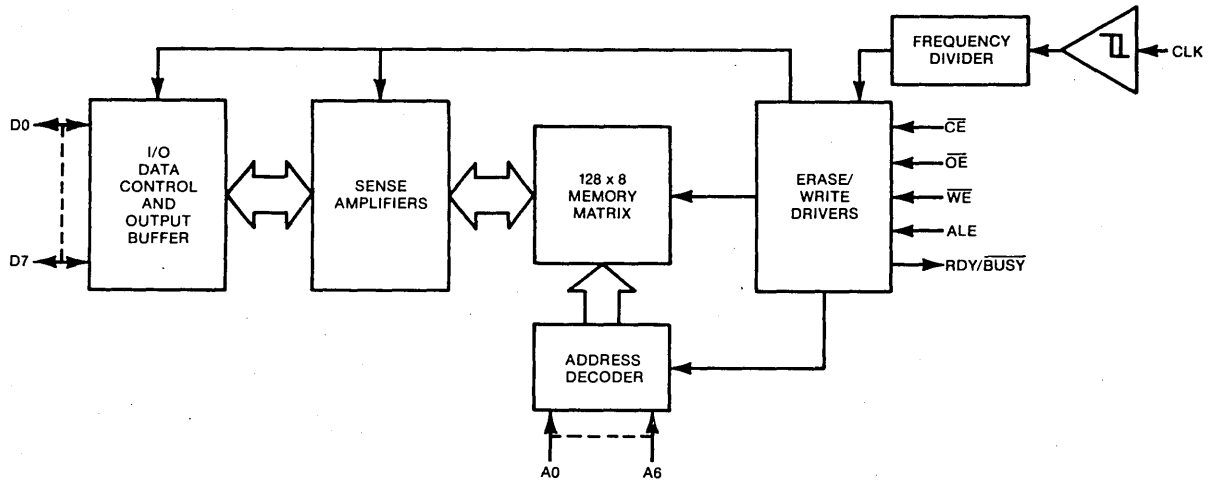
24 LEAD DUAL IN LINE

Top View



NC = No Internal Connection

BLOCK DIAGRAM



An ADDRESS LATCH ENABLE (ALE) input is provided so that memory may be used with a multiplexed address and data bus. When this feature is not required, ALE may be tied to $\overline{WE}$.

Bus contention problems are minimized by twin line control provided by CHIP ENABLE ($\overline{CE}$) and OUTPUT ENABLE ($\overline{OE}$).

By virtue of the on-chip reprograming control and timing of the ER5901, a minimum amount of servicing is required from a host microprocessor or microcomputer.

The user may select one of five operating modes:

1. READ with separate address and data lines.
2. READ with multiplexed address and data lines.
3. PROGRAM with separate address and data lines.
4. PROGRAM with multiplexed address and data lines.
5. STANDBY — power consumption is reduced by 66%.

PIN FUNCTIONS

Symbol	Function	Comments
ALE	Address Latch Enable	Address inputs latched on negative edge. May be tied to $\overline{WE}$ when separate address and data lines are used.
A0-A6	7 bit address	
D0-D7	8 bit data I/O	
V_{SS}	Chip Ground connection	
$\overline{CE}$	Chip Enable input	Used for chip selection.
$\overline{OE}$	Output Enable input	Gates data to output pins during read cycle.
$\overline{WE}$	Write Enable input	Enables reprograming cycle; input data latched on positive edge.
CLK	Timing inputs	Defines clock frequency for reprograming. May be RC or external clock.
RDY/BUSY	Status output	Low when chip is in reprograming mode and cannot be accessed. High when in read mode.
V_{CC}	+5 Volt power connection	

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

All inputs and outputs with respect to Ground ..... +6V to −0.3V
Storage temperature (unpowered and without data retention) ..... −65°C to +150°C
Soldering temperature of leads (10 secs.) ..... +300°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise noted)

V_{SS} = GND
V_{CC} = +5V ±10% Volts
Operating Temperature Ranges T_A: 0°C to +70°C (Commercial)
−40°C to +85°C (Industrial)
−55°C to +125°C (Military)

DC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Input Logic "1"	V_{IH}	2	—	V_{CC}+0.3	V	
Input Logic "0"	V_{IL}	−0.1	—	+0.8	V	
Output Logic "1"	V_{OH}	2.4	—	V_{CC}	V	I_{OH} = 400μA
Output Logic "0"	V_{OL}	—	—	0.4	V	I_{OL} = 1.6mA
Input Leakage Current	I_{IL}	—	—	10	μA	V_{IN} = 5.25V
Output Leakage Current	I_{OL}	—	—	10	μA	V_{OUT} = 5.25V
Power Supply Requirements						
V_{CC} Supply:						
Chip Selected	I_{CC}	—	35	80	mA	V_{CC} = +5.5V
Chip Deselected (Standby Mode)	I_{CC}	—	12	35	mA	V_{CC} = +5.5V
Power Dissipation:						
Chip Selected	P_D	—	195	300	mW	V_{CC} = +5.5V
Chip Deselected (Standby Mode)	P_D	—	66	100	mW	V_{CC} = +5.5V

AC CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Input Capacitance	C_I	—	—	6	pf	V_{IN} = 0V
Output Capacitance	C_O	—	—	10	pf	V_{OUT} = 0V

MEMORY CHARACTERISTICS

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Erased State	V_E	—	V_{IH}, V_{OH}	—	V	
Written State	V_W	—	V_{IL}, V_{OL}	—	V	
Data Retention Time (Powered or Unpowered)	t_S	10	—	—	Years	
Number of Reprograming Cycles per Byte	N_P	10^4	—	—	—	See Note
Number of Read Accesses Between Refresh	N_{RA}	Unlimited				

NOTE:
There is a tradeoff to be made between the data retention time (t_S) and the number of reprograming cycles (N_P) performed per address. A gradual logarithmic reduction in retention time is experienced as the number of reprograming cycles increases. The specified limit is merely one point on this curve and does not imply a sudden cutoff or end of life. After 10^4 cycles a typical retention time is 10 years.

MODE SELECTION: Multiplexed Address and Data Lines

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$(1)	ALE(2)	RDY/$\overline{BUSY}$
Standby	V_{IH}	Don't Care	Don't Care	Don't Care	V_{OH}
Read	V_{IL}	V_{IL}(3)	V_{IH}	⎍	V_{OH}
Program	V_{IL}	V_{IH}	⎍	⎍	V_{OL}

MODE SELECTION: Separate Address and Data Lines

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$/ALE(1, 2, 4)	RDY/$\overline{BUSY}$
Standby	V_{IH}	Don't Care	Don't Care	V_{OH}
Read	V_{IL}	V_{IL}	V_{IH}	V_{OH}
Program	V_{IL}	V_{IH}	⎍	V_{OL}

NOTES:
1. Data inputs latched on rising edge of $\overline{WE}$.
2. Address inputs latched on falling edge of ALE.
3. To avoid bus contention $\overline{OE}$ must be strobed when the device is used in the multiplexed mode.
4. $\overline{WE}$ and ALE inputs may be tied together when the device is used in the non-multiplexed mode.

READ OPERATION (With Separate Address and Data Lines)

To initiate a read cycle a valid address must appear on the A_0 to A_6 inputs and remain there for the duration of the cycle because the address is not latched in this mode. $\overline{CE}$ may then be brought low to select the device. The desired memory byte will be in internal registers a short time later and will appear on data lines D_0 to D_7 after a time delay (t_{OE}) measured from the falling edge of OE. Alternatively, if bus contention is not a problem, $\overline{OE}$ may be tied low. The maximum read access time (t_A) is 200ns, and data will remain valid until a logic level change occurs on $\overline{CE}$, $\overline{OE}$, or an address line. In this mode of operation ALE and $\overline{WE}$ are held high and may be tied together. (See Figure 1.)

READ MODE (Separate Address and Data Lines)

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Access Time — Address to Output Delay	t_A	—	—	200	ns	Load = 1 TTL gate + C_L = 100pf $\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}	—	—	200	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	t_{OE}	10	—	150	ns	$\overline{CE}$ = V_{IL}
Address — $\overline{CE}$ or $\overline{OE}$ to Output Tri-State	t_{TS}	10	—	75	ns	

READ OPERATION (With Multiplexed Address and Data Lines)

The ALE line is pulsed high, while a valid address is presented to the A_0 to A_6 inputs of a selected device. The address is latched into the ER5901 on the falling edge of ALE and, in order to avoid bus contention, these lines should be tri-stated prior to pulsing $\overline{OE}$ low. After a delay (t_{OE}), the selected byte will appear on lines D_0 to D_7 until either $\overline{OE}$ or $\overline{CE}$ goes high. (See Figure 2.)

READ MODE (Multiplexed Address and Data Lines)

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Address Setup Time	t_{AS}	10	—	—	ns	
Chip Enable to Address Latch Enable	t_{CA}	100	—	—	ns	
ALE Pulse Width	t_{ALE}	100	—	—	ns	
Address Hold Time	t_{AH}	40	—	—	ns	
Address Float to Output Enable	t_{AO}	20	—	—	ns	
$\overline{OE}$ to Output Delay	t_{OE}	10	—	150	ns	$\overline{CE} = V_{IL}$
Address — $\overline{CE}$ or $\overline{OE}$ to Output Tri-State	t_{TS}	10	—	75	ns	

PROGRAM MODE (With Separate Address and Data Lines)

In this mode the ALE and $\overline{WE}$ inputs may be tied together. With a stable address and data word presented to the respective inputs of a selected device, the $\overline{WE}$/ALE line is pulsed low to initiate a program cycle. The falling edge of $\overline{WE}$/ALE latches the address inputs and the rising edge latches the data inputs. After a delay (t_{DB}), the RDY/$\overline{BUSY}$ output will go low and remain low for the duration of the programing cycle. All inputs to the ER5901 are disabled during a programing cycle. (See Figure 3.)

PROGRAM MODE (Separate Address and Data Lines)

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Address Setup Time	t_{AS}	50	—	—	ns	
Chip Enable to Write Enable Delay	t_{CW}	100	—	—	ns	
Data Setup Time	t_{DS}	0	—	—	ns	
Address Hold Time	t_{AH}	40	—	—	ns	
Write Enable Pulse Width	t_{WE}	0.1	—	10	μs	
Data Hold Time	t_{DH}	40	—	—	ns	
$\overline{WE}$ to $\overline{CE}$ Delay	t_{CH}	0	—	—	ns	
Status Delay	t_{DB}	10	—	150	ns	
Status Low Time (Programing Time)	t_{PR}	20	—	100	ms	With min clock freq as defined by TI input
Program Clock Frequency	F_{PR}	10	—	50	KHz	

PROGRAM MODE (With Multiplexed Address and Data Lines)

The ALE line is pulsed high while the address to be altered is presented to lines A_0 to A_6 of the selected device. The fall of ALE latches the address into the ER5901, and the information on the bus line is then changed to the data to be written into the EEPROM. $\overline{WE}$ is pulsed low and the data is latched on its rising edge. After a delay (t_{DB}), the RDY/$\overline{BUSY}$ output will go low for the duration of the programing cycle. (See Figure 4.)

PROGRAM MODE (Multiplexed Address and Data Lines)

Characteristics	Sym	Min	Typ	Max	Units	Conditions
Address Setup Time	t_{AS}	10	—	—	ns	
Chip Enable to Address Latch Enable	t_{CA}	100	—	—	ns	
ALE Pulse Width	t_{ALE}	100	—	—	ns	
Address Hold Time	t_{AH}	40	—	—	ns	
Data Setup Time	t_{DS}	10	—	—	ns	
$\overline{WE}$ Pulse Width	t_{WE}	0.1	—	10	μs	
Data Hold Time	t_{DH}	40	—	—	ns	
$\overline{WE}$ to $\overline{CE}$ Delay	t_{CH}	0	—	—	ns	
Status Delay	t_{STA}	10	—	150	ns	
Status Low Time (Programing Time)	t_{PR}	20	—	100	ms	With min clock freq as defined by TI input
Program Clock Frequency	F_{PR}	10	—	50	KHz	

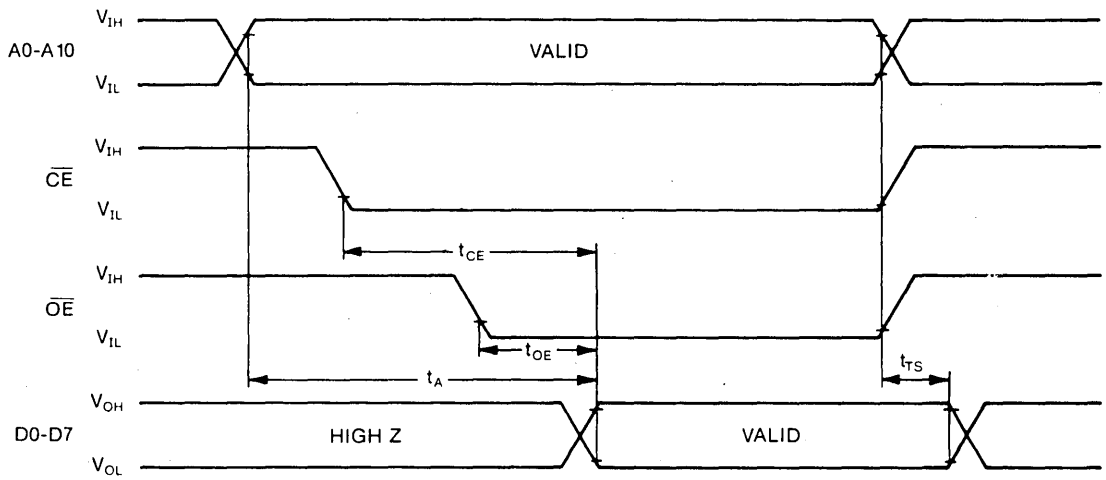


Fig. 1 READ MODE WITH SEPARATE ADDRESS AND DATA LINES

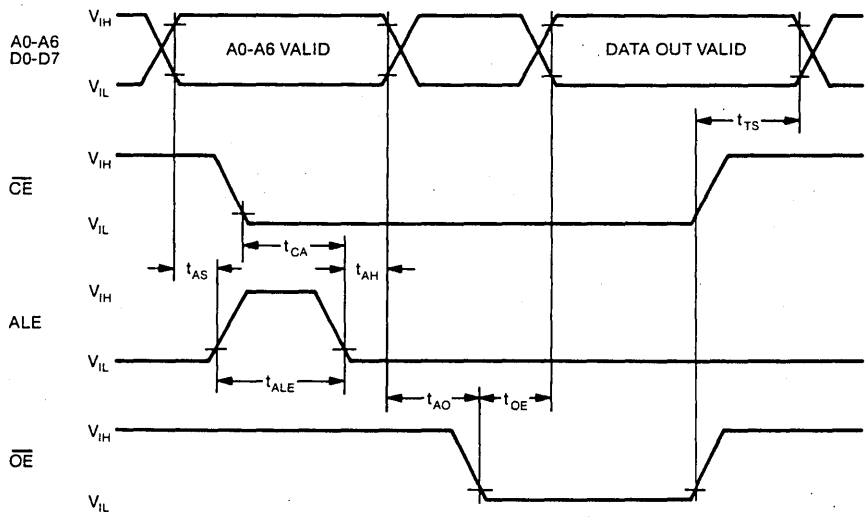


Fig. 2 READ MODE WITH MULTIPLEXED ADDRESS AND DATA LINES

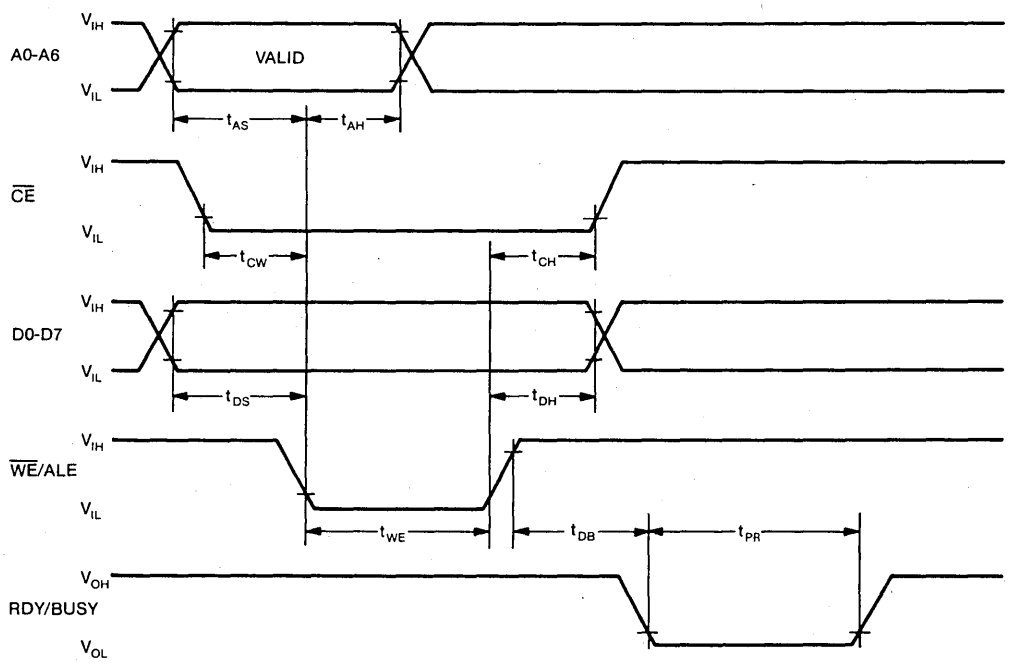


Fig. 3 PROGRAM MODE WITH SEPARATE ADDRESS AND DATA LINES

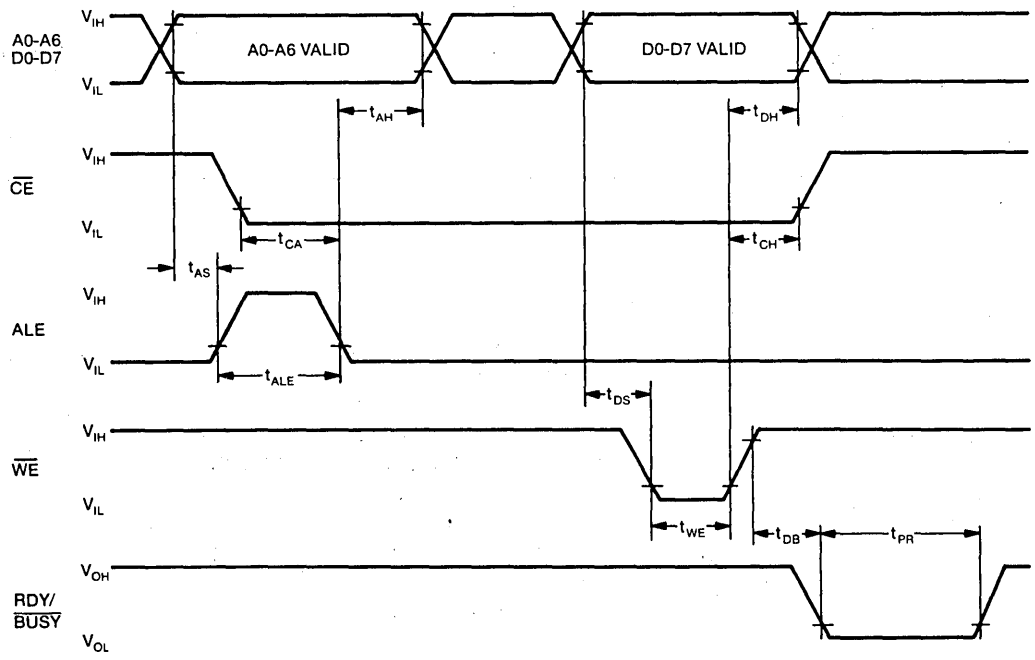


Fig. 4 PROGRAM MODE WITH MULTIPLEXED ADDRESS AND DATA LINE

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GENERAL INSTRUMENT

HARRIS

SEMICONDUCTOR DIGITAL PRODUCTS DIVISION

HM-7602/03

32 x 8 PROM

HM-7602 — Open Collector Outputs

HM-7603 — "Three State" Outputs

Features

- 50ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD

Description

The HM-7602/03 is a fully decoded high speed Schottky TTL 256/Bit Field Programmable ROM in a 32 word by 8 bit/word format with open collector (HM-7602) or "Three State" (HM-7603) outputs. These PROMs are available in a 16 pin D.I.P. (ceramic or epoxy) and a 16 pin flatpack.

All bits are manufactured storing a logical "1" (Positive Logic) and can be selectively programmed for a logical "0" in any one bit position.

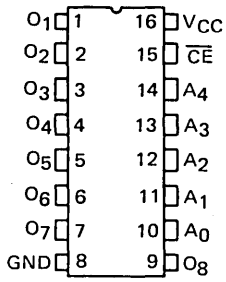
Nickel-chromium fuse technology is used on this and all other Harris Bipolar PROMs.

The HM-7602/03 contains test rows which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows are blown prior to shipment.

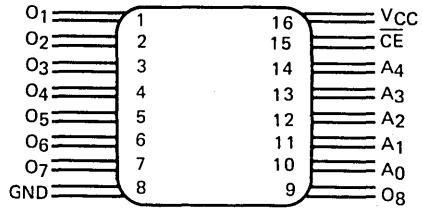
There is one chip enable input on the HM-7602/03. $\overline{CE}$ low enables the chip.

Pinouts

TOP VIEW – DIP



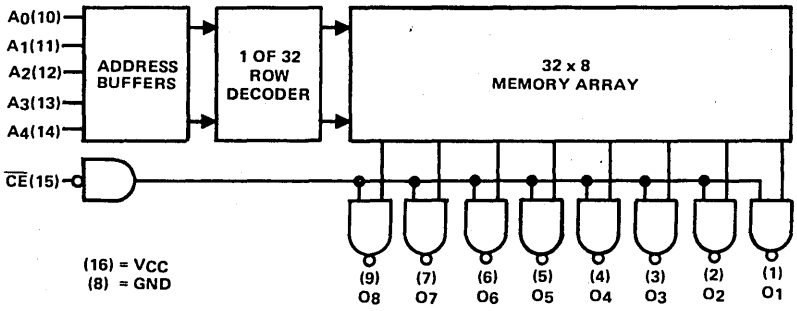
TOP VIEW – FLATPACK



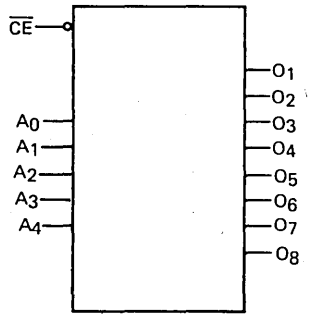
PIN NAMES

$A_0 - A_4$	Address Inputs
$O_1 - O_8$	Data Outputs
$\overline{CE}$	Chip Enable Inputs

Functional Diagram



Logic Symbol



Harris Semiconductor

MEMORY

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7602/03-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7602/03-2 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/Enable "1"	–	–	+40	µA	V_{IH} = V_{CC} Max.
I_{IL}	Input Current "0"	–	-50.0	-250	µA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0	1.5	–	V	V_{CC} = V_{CC} Min
V_{IL}	Voltage "0"	–	1.5	0.8	V	V_{CC} = V_{CC} Max.
V_{OH}	Output Voltage "1"	2.4*	3.2*	–	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	"0"	–	0.35	0.45	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}	Output Disable "1"	–	–	+100	µA	V_{OH}, V_{CC} = V_{CC} Max.
I_{OLE}	Current "0"	–	–	-100	µA	V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	–	-100*	mA	V_{CC} = V_{CC} Max., V_{OUT} = 0.0V One Output Only for a Max. of 1 Second.
I_{CC}	Power Supply Current	–	90	130	mA	V_{CC} = V_{CC} Max. All Inputs Grounded

NOTE: Positive current defined as into device terminals
* "Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

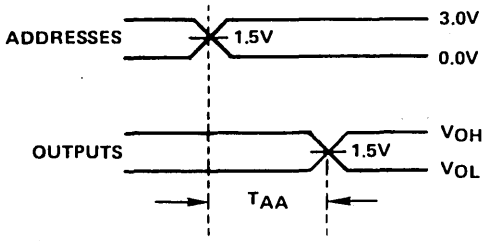
		HM-7602/03-5 5V ±5% 0°C to +75°C			HM-7602/03-2 5V ±10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX*	MIN	TYP	MAX*	UNITS
T_{AA}	Address Access Time	–	30	50	–	–	60	ns
T_{EA}	Chip Enable Access Time	–	20	35	–	–	50	ns

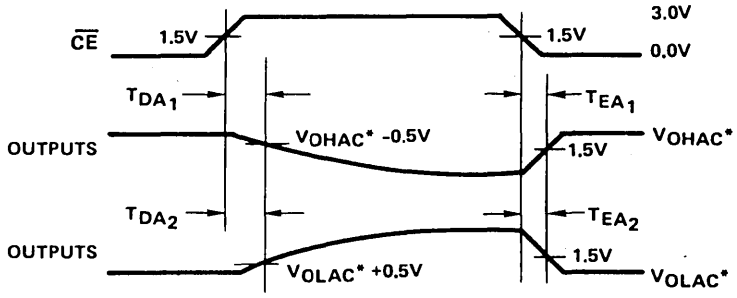
*A.C. limits guaranteed for worst case N2 sequencing with maximum test frequency of 5MHz.

CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	12	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	12	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS

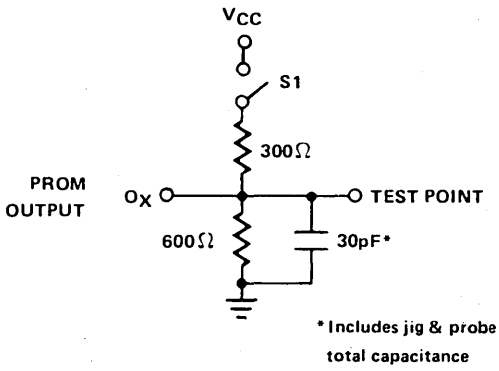




tr, tf < 5ns

*VOLAC AND VOHAC ARE THE MEASURED OUTPUT VOLTAGE LEVELS WHILE ENABLED.

A.C. TEST LOAD



*Includes jig & probe total capacitance

SYMBOL	PARAMETER	S1
T_{AA}	Address Access Time	Closed
T_{EA_1}	Chip Enable Access Time from "Three State" to V_{OH}	Open
T_{EA_2}	Chip Enable Access Time from "Three State" to V_{OL}	Closed
T_{DA_1}	Chip Disable Access Time from V_{OH} to "Three State"	Open
T_{DA_2}	Chip Disable Access Time from V_{OL} to "Three State"	Closed

HM-7610/11

HIGH SPEED 256 x 4 PROM

HM-7610 - Open Collector Outputs
HM-7611 - "Three State" Outputs

Features

- FAST ADDRESS ACCESS TIME
  - HM-7610/11 . . . . . 60 ns MAXIMUM
  - HM-7610A/11A . . . . . 45 ns MAXIMUM
  - HM-7610B/11B . . . . . 35 ns MAXIMUM
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND TWO CHIP ENABLE INPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE ONE PULSE/BIT ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- INPUTS AND OUTPUTS TTL COMPATIBLE
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- PIN COMPATIBLE WITH INDUSTRY STANDARD 1K PROMs.

Description

The HM-7610/11 are fully decoded high speed Schottky TTL 1024 bit Field Programmable ROM's in a 256 word by 4 bit/word format with open collector (HM-7610) or "three state" (HM-7611) outputs. The PROMs are available in 16 pin D.I.P. (ceramic or power plastic).

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

The HM-7610/11 contain test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

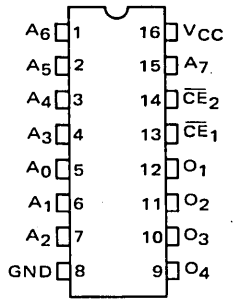
This PROM is intended for use in state of the art high speed logic systems.

Nickel-chromium fuse technology is used on these and all other Harris Bipolar PROMs.

There are two chip enable inputs on the HM-7610/11 where $\overline{CE}_1$ and $\overline{CE}_2$ low enables the chip.

Pinouts

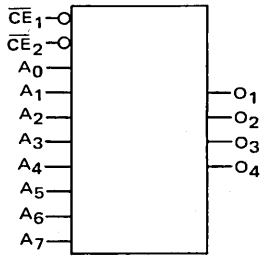
TOP VIEW–DIP



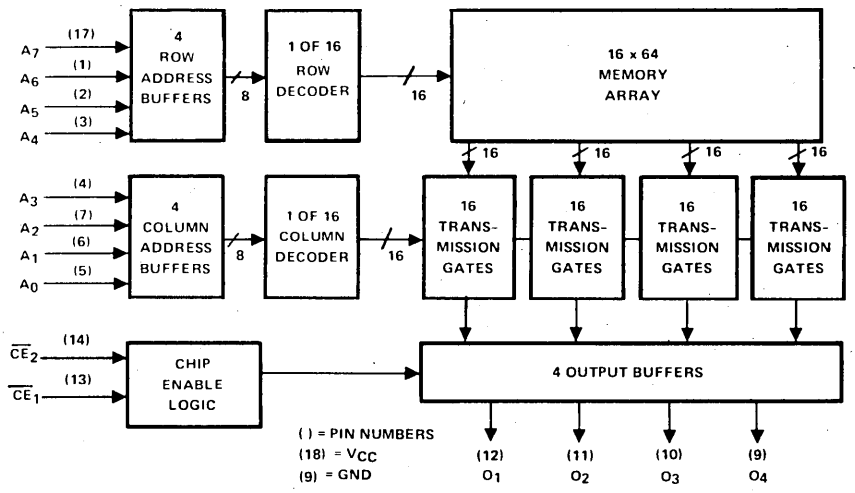
PIN NAMES

$A_0 - A_7$ Address Inputs
$O_1 - O_4$ Data Outputs
$\overline{CE}_1, \overline{CE}_2$ Chip Enable Inputs

Logic Symbol



Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7610/11-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7610/11-2/-8 (V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– –	+40 –250	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4* –	3.2* 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+100 –100*	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current *	-15*	–	-100*	mA	V_{OUT} = 0.0V One Output Only for a Max. of 1 Second
I_{CC}	Power Supply Current	–	90	130	mA	V_{CC} = V_{CC} Max. All Inputs Grounded

NOTE: Positive current defined as into device terminals.
* " Three State" Only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

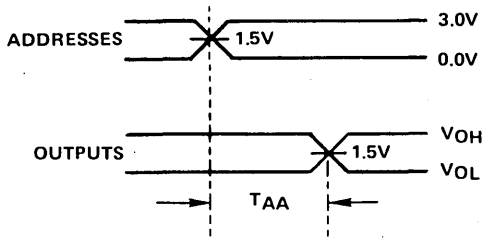
		HM-7610/11-5 5V ±5% 0°C to +75°C						HM-7610/11-2 5V ±10% −55°C to +125°C						
		"B"		"A"		STD		"B"		"A"		STD		
SYMBOL	PARAMETER	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	UNITS
T_{AA}	Address Access Time	25	35	35	45	40	60	–	50	–	65	–	75	ns
T_{EA}	Chip Enable Access Time	–	25	–	25	–	25	–	30	–	30	–	30	ns
T_{DA}	Chip Disable Access Time	–	25	–	25	–	25	–	30	–	30	–	30	

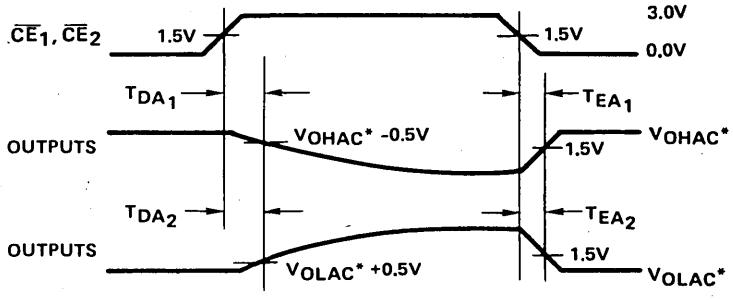
A.C. limits guaranteed for worst case N2 sequencing with maximum test frequency of 5MHz.

CAPACITANCE: T_A = 25°C (NOTE: Sampled and guaranteed – but not 100% tested.)

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS

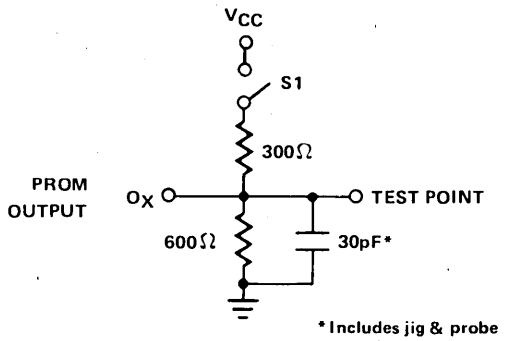




tr, tf < 5ns

*VOLAC AND VOHAC ARE THE MEASURED OUTPUT VOLTAGE LEVELS WHILE ENABLED.

A.C. TEST LOAD



*Includes jig & probe total capacitance

SYMBOL	PARAMETER	S1
T_{AA}	Address Access Time	Closed
T_{EA_1}	Chip Enable Access Time from "Three State" to V_{OH}	Open
T_{EA_2}	Chip Enable Access Time from "Three State" to V_{OL}	Closed
T_{DA_1}	Chip Disable Access Time from V_{OH} to "Three State"	Open
T_{DA_2}	Chip Disable Access Time from V_{OL} to "Three State"	Closed

HM-7620/21

HIGH SPEED 512 x 4 PROM

HM-7620 - Open Collector Outputs
HM-7621 - "Three State" Outputs

Features

- FAST ADDRESS ACCESS TIME
  - HM-7620/21 . . . . . 70 ns MAXIMUM
  - HM-7620A/21A . . . . . 50 ns MAXIMUM
  - HM-7620B/21B . . . . . 40 ns MAXIMUM
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND A SINGLE CHIP ENABLE INPUT
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE ONE PULSE/BIT ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- INPUTS AND OUTPUTS TTL COMPATIBLE
- FAST ACCESS TIME–GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- PIN COMPATIBLE WITH INDUSTRY STANDARD 2K PROMs.

Description

The HM-7620/21 are fully decoded high speed Schottky TTL 2048 bit Field Programmable ROM's in a 512 word by 4 bit/word format with open collector (HM-7620) or "three state" (HM-7621) outputs. These PROMs are available in 16 pin D.I.P. (ceramic or power plastic).

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

The HM-7620/21 contain test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A. C. performance. The fuses in these test rows and columns are blown prior to shipment.

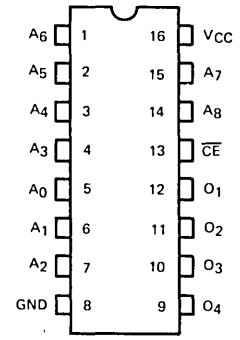
This PROM is intended for use in state of the art high speed logic systems.

Nickel-chromium fuse technology is used on these and all other Harris Bipolar PROMs.

There is a single chip enable input on the HM-7620/21 where $\overline{CE}$ low enables the chip.

Pinout

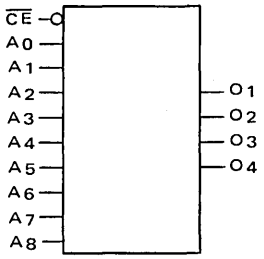
TOP VIEW - DIP



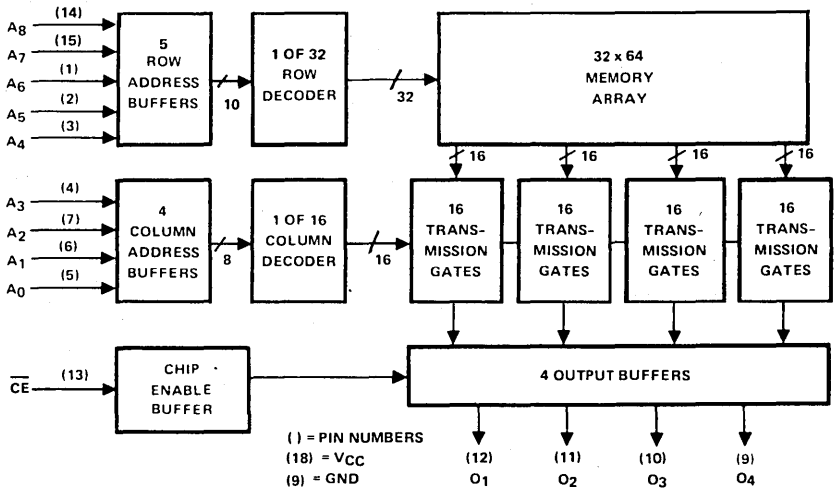
PIN NAMES

A0 – A8	Address Inputs
$\overline{CE}$	Chip Enable Input
O1 – O4	Data Outputs

Logic Symbol



Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7620/21-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7620/21-2/-8 (V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/enable "1" Input Current "0"	– –	– –	+40 −250	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	– –	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4 * –	3.2 * 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+100 −100*	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15 *	–	-100 *	mA	V_{OUT} = 0.0V One Output Only for a Max. of 1 Second
I_{CC}	Power Supply Current	–	90	130	mA	V_{CC} = V_{CC} Max. All Inputs Grounded

*"Three State" only
NOTE: Positive current defined as into device terminals.

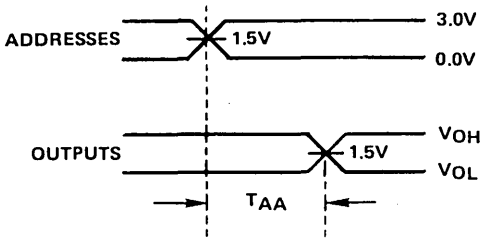
A.C. ELECTRICAL CHARACTERISTICS (Operating)

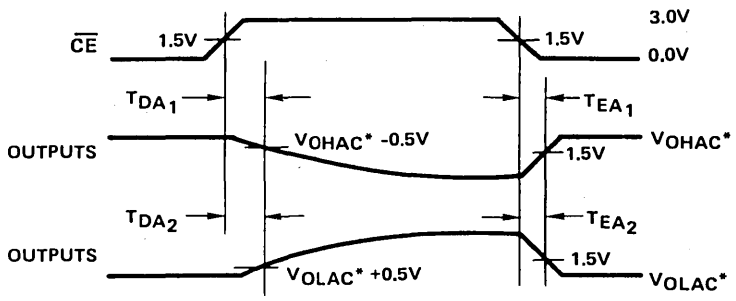
		HM-7620/21 - 5 5V ±5% 0°C to +75°C						HM-7620/21-2/8 5V ±10% −55°C to +125°C						
		"B"		"A"		STD		"B"		"A"		STD		
SYMBOL	PARAMETER	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	UNITS
T_{AA}	Address Access Time	30	40	40	50	50	70	–	55	–	70	–	85	ns
T_{EA}	Chip Enable Access Time	–	25	–	25	–	25	–	30	–	30	–	30	ns
T_{DA}	Chip Disable Access Time	–	25	–	25	–	25	–	30	–	30	–	30	ns

A.C. limits guaranteed for worst case N2 sequencing with maximum test frequency of 5MHz.

CAPACITANCE: T_A = 25°C (NOTE: Sampled and guaranteed – but not 100% tested.)

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

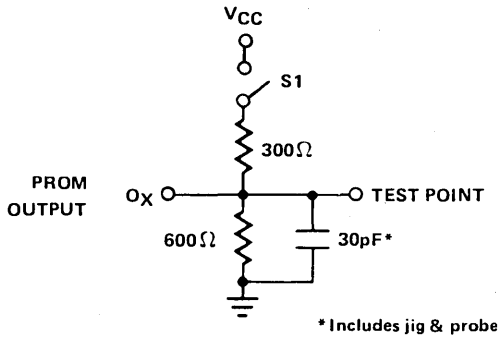




tr, tf < 5ns

*VOLAC AND VOHAC ARE THE MEASURED OUTPUT VOLTAGE LEVELS WHILE ENABLED.

A.C. TEST LOAD



*Includes jig & probe total capacitance

SYMBOL	PARAMETER	S1
T_{AA}	Address Access Time	Closed
T_{EA_1}	Chip Enable Access Time from "Three State" to V_{OH}	Open
T_{EA_2}	Chip Enable Access Time from "Three State" to V_{OL}	Closed
T_{DA_1}	Chip Disable Access Time from V_{OH} to "Three State"	Open
T_{DA_2}	Chip Disable Access Time from V_{OL} to "Three State"	Closed

HM-7640/41

HIGH SPEED 512 x 8 PROM

HM-7640 - Open Collector Outputs
HM-7641 - "Three State" Outputs

Features

- FAST ADDRESS ACCESS TIME
  - HM-7640/41 . . . . . 70 ns MAXIMUM
  - HM-7640A/41A . . . . . 45 ns MAXIMUM
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND FOUR CHIP ENABLE INPUTS.
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE — ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- PIN COMPATIBLE WITH INDUSTRY STANDARD 4K PROMs.

Description

The HM-7640/41 are fully decoded high speed Schottky TTL 4096 bit Field Programmable ROMs in a 512 word by 8 bit/word format and are available in a 24 pin DIP (ceramic or power plastic).

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

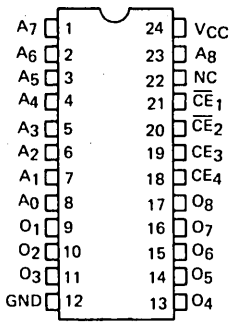
Nickel-chromium fuse technology is used on this and all other Harris Bipolar PROMs.

The HM-7640/41 contain test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

There are four chip enable inputs on the HM-7640/41 where $\overline{CE}_1$ and $\overline{CE}_2$ low and CE_3 and CE_4 high enables the chip.

Pinouts

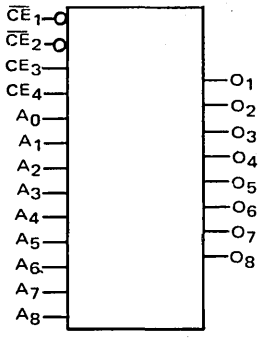
TOP VIEW – DIP



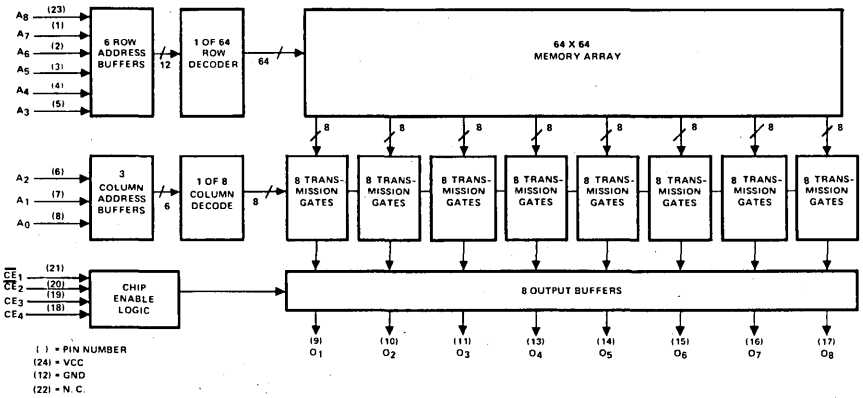
PIN NAMES

$A_0 - A_8$	Address Inputs
$O_1 - O_8$	Data Outputs
$\overline{CE}_1, \overline{CE}_2, CE_3, CE_4$	Chip Enable Inputs

Logic Symbol



Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7640/41-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7640/41-2/-8 (V_{CC} - 5.0V ±10%, T_A = −55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– –	+40 -250	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	– –	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4* –	3.2* 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+100 −100*	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	–	-100*	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	125	170	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
*"Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

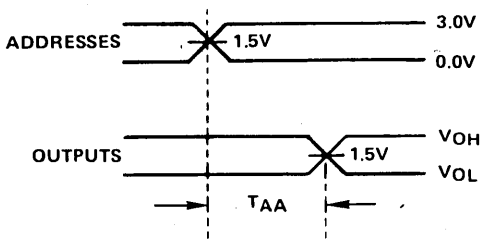
		HM-7640/41-5 5V ±5% 0°C to +75°C				HM-7640/41-2/-8 5V ±10% −55°C to +125°C				
		"A"		STD		"A"		STD		
SYMBOL	PARAMETER	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	UNITS
T_{AA}	Address Access Time	35	45	50	70	–	60	–	85	ns
T_{EA}	Chip Enable Access Time	–	35	–	40	–	45	–	50	ns
T_{DA}	Chip Disable Access Time	–	35	–	40	–	45	–	50	ns

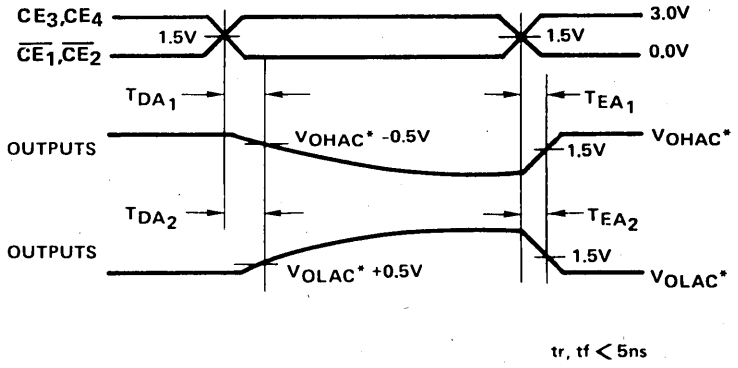
A.C. limits guaranteed for worst case N2 sequencing with maximum test frequency of 5MHz.

CAPACITANCE: T_A = 25°C (NOTE: Sampled and guaranteed — but not 100% tested.)

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS

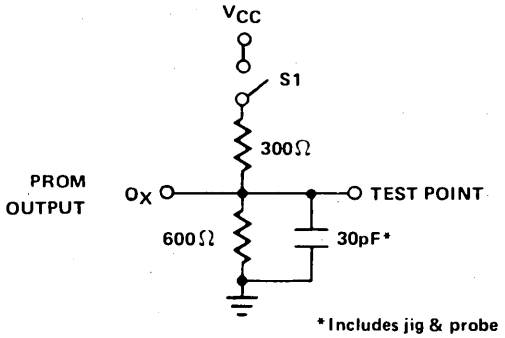




tr, tf < 5ns

*VOLAC AND VOHAC ARE THE MEASURED OUTPUT VOLTAGE LEVELS WHILE ENABLED.

A.C. TEST LOAD



*Includes jig & probe total capacitance

SYMBOL	PARAMETER	S1
T_{AA}	Address Access Time	Closed
T_{EA_1}	Chip Enable Access Time from "Three State" to V_{OH}	Open
T_{EA_2}	Chip Enable Access Time from "Three State" to V_{OL}	Closed
T_{DA_1}	Chip Disable Access Time from V_{OH} to "Three State"	Open
T_{DA_2}	Chip Disable Access Time from V_{OL} to "Three State"	Closed

HM-7642/43

HIGH SPEED 1K x 4 PROM

HM-7642 - Open Collector Outputs
HM-7643 - "Three State" Outputs

Features

- FAST ADDRESS ACCESS TIME
  - HM-7642/43 . . . . . 60 ns MAXIMUM
  - HM-7642A/43A . . . . . 50 ns MAXIMUM
  - HM-7642B/43B . . . . . 45 ns MAXIMUM
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND TWO CHIP ENABLE INPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- PIN COMPATIBLE WITH INDUSTRY STANDARD 4K PROM'S.

Description

The HM-7642/43 are fully decoded high speed Schottky TTL 4096 bit Field Programmable ROMs in a 1K word by 4 bit/word format with open collector (HM-7642) or "three state" (HM-7643) outputs. These PROM's are available in an 18 pin DIP (ceramic or power plastic).

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

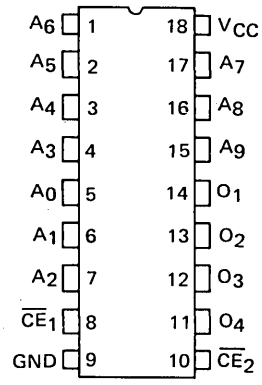
Nickel-chromium fuse technology is used on these and all other Harris Bipolar PROMs.

The HM-7642/43 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

There are two chip enable inputs on the HM-7642/43. $\overline{CE}_1$ and $\overline{CE}_2$ low enables the chip.

Pinout

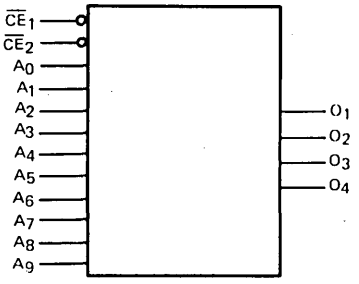
TOP VIEW—DIP

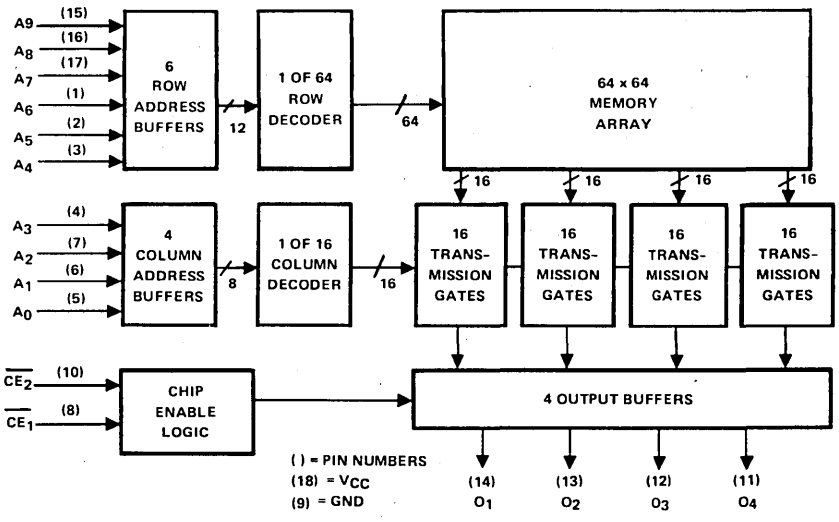


PIN NAMES

$A_0 - A_9$	ADDRESS INPUTS
$O_1 - O_4$	DATA OUTPUTS
$\overline{CE}_1, \overline{CE}_2$	CHIP ENABLE INPUTS

Logic Symbol





ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7642/43-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7642/43-2 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical Measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/Enable "1"	–	–	+40	μA	V_{IH} = V_{CC} Max.
I_{IL}	Input Current "0"	–	–	-250	μA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0	–	–	V	V_{CC} = V_{CC} Min.
V_{IL}	Voltage "0"	–	–	0.8	V	V_{CC} = V_{CC} Max.
V_{OH}	Output "1"	2.4*	3.2*	–	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	Voltage "0"	–	0.35	0.50	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}	Output Disable "1"	–	–	+100	μA	V_{OH}, V_{CC} = V_{CC} Max.
I_{OLE}	Current "0"	–	–	–100*	μA	V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	–	-100*	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	100	140	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
*"Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

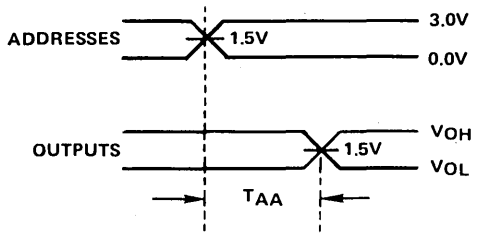
		HM-7642/43-5 5V ±5% 0°C to +75°C						HM-7642/43-2/-8 5V ±10% –55°C to +125°C						
		"B"		"A"		STD		"B"		"A"		STD		
SYMBOL	PARAMETER	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	UNITS
T_{AA}	Address Access Time	35	45	40	50	45	60	–	55	–	70	–	85	ns
T_{EA}	Chip Enable Access Time	–	25	–	25	–	25	–	30	–	30	–	30	ns
T_{DA}	Chip Disable Access Time	–	25	–	25	–	25	–	30	–	30	–	30	ns

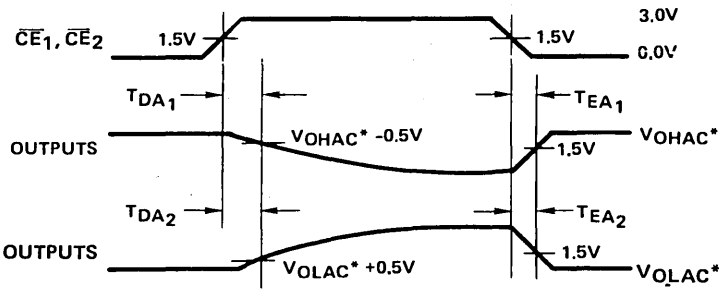
A.C. limits guaranteed for worst case N2 sequencing with maximum test frequency of 5MHz.

CAPACITANCE: T_A = 25°C (NOTE: Sampled and guaranteed – but not 100% tested.)

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
CINA, CINCE	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
COUT	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS

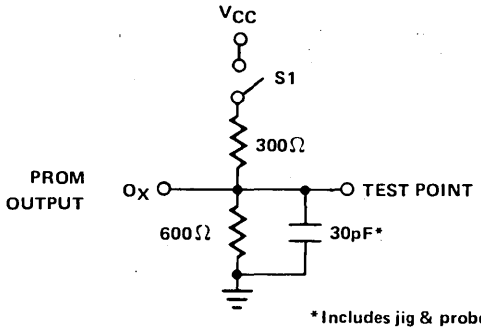




tr, tf < 5ns

*VOLAC AND VOHAC ARE THE MEASURED OUTPUT VOLTAGE LEVELS WHILE ENABLED.

A.C. TEST LOAD



*Includes jig & probe total capacitance

SYMBOL	PARAMETER	S1
T_{AA}	Address Access Time	Closed
T_{EA_1}	Chip Enable Access Time from "Three State" to V_{OH}	Open
T_{EA_2}	Chip Enable Access Time from "Three State" to V_{OL}	Closed
T_{DA_1}	Chip Disable Access Time from V_{OH} to "Three State"	Open
T_{DA_2}	Chip Disable Access Time from V_{OL} to "Three State"	Closed

HARRIS

HM-7649

HIGH SPEED 512 x 8 PROM

Features

- FAST ADDRESS ACCESS TIME
  - HM-7649 . . . . . 60 ns MAXIMUM
  - HM-7649A . . . . . .45 ns MAXIMUM
- "THREE STATE" OUTPUTS AND A SINGLE CHIP ENABLE INPUT
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- PIN COMPATIBLE WITH THE 74S473
- LOW INPUT LOADING

Description

The HM-7649 is a fully decoded high speed Schottky TTL 4096 bit Field Programmable ROM in a 512 word by 8 bit/word format with "Three State" outputs. This PROM is available in a 20 pin D.I.P. (ceramic or power plastic).

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

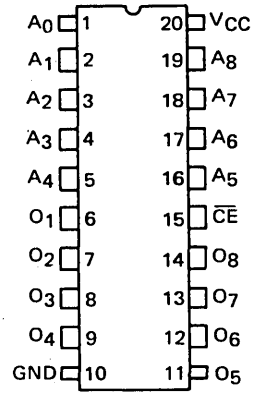
Nickel Chromium fuse technology is used on this and all other Harris Bipolar PROMs.

The pinout is identical to the 74S473 PROM.

The HM-7649 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametic and A. C. performance. The fuses in these test rows and columns are blown prior to shipment.

There is a chip enable input on the HM-7649 where $\overline{CE}$ low enables the device.

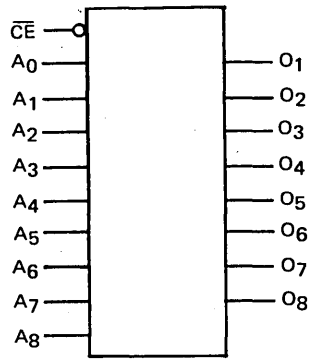
Pinout

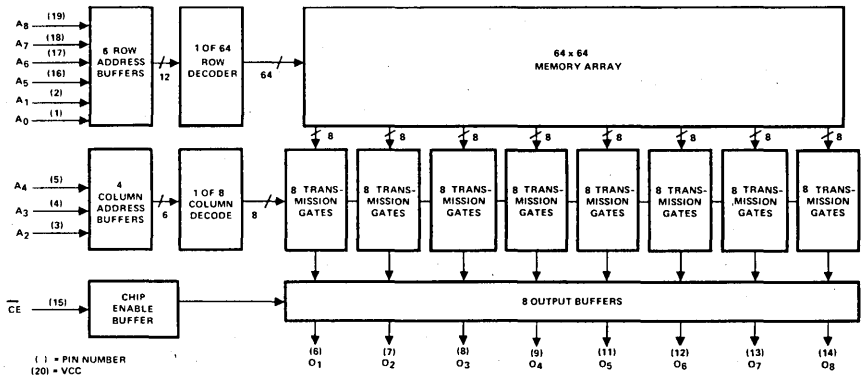


TOP VIEW - D.I.P.

PIN NAMES	
A_0-A_8	Address Inputs
O_1-O_8	Data Outputs
CE	Chip Enable Input

Logic Symbol





ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7649-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7649-2/8 (V_{CC} - 5.0V ±10%, T_A = −55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– –	+25 -250	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	– –	– 0.80	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4 –	3.2 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-20	–	-100	mA	V_{OUT} = 0.0V One Output Only for a Max. of 1 Second
I_{CC}	Power Supply Current	–	120	170	mA	V_{CC} = V_{CC} Max. All Inputs Grounded

NOTE: Positive current defined as into device terminals.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

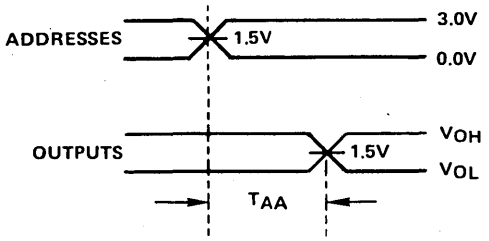
		HM-7649-5 5V ±5% 0°C to +75°C				HM-7649-2/-8 5V ±10% −55°C to +125°C				
		"A"		STD		"A"		STD		
SYMBOL	PARAMETER	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	UNITS
T_{AA}	Address Access Time	35	45	40	60	–	60	–	80	ns
T_{EA}	Chip Enable Access Time	–	35	–	40	–	45	–	50	ns
T_{DA}	Chip Disable Access Time	–	35	–	40	–	45	–	50	ns

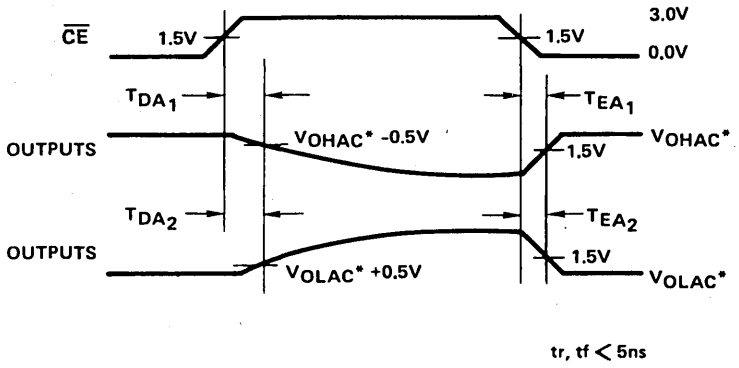
A.C. limits guaranteed for worst case N2 sequencing with maximum test frequency of 5MHz.

CAPACITANCE: T_A = 25°C (NOTE: Sampled and guaranteed – but not 100% tested.)

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

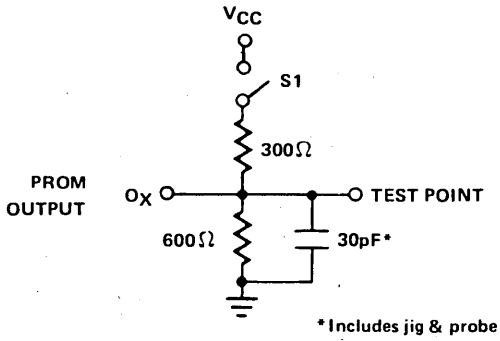
SWITCHING TIME DEFINITIONS





*VOLAC AND VOHAC ARE THE MEASURED OUTPUT VOLTAGE LEVELS WHILE ENABLED.

A.C. TEST LOAD



*Includes jig & probe total capacitance

SYMBOL	PARAMETER	S1
T_{AA}	Address Access Time	Closed
T_{EA_1}	Chip Enable Access Time from "Three State" to V_{OH}	Open
T_{EA_2}	Chip Enable Access Time from "Three State" to V_{OL}	Closed
T_{DA_1}	Chip Disable Access Time from V_{OH} to "Three State"	Open
T_{DA_2}	Chip Disable Access Time from V_{OL} to "Three State"	Closed

HM-7681

HIGH SPEED 1K x 8 PROM

Features

- FAST ADDRESS ACCESS TIME
  - HM-7681 . . . . . 70 ns MAXIMUM
  - HM-7681A . . . . . 50 ns MAXIMUM
- "THREE STATE" OUTPUTS AND FOUR CHIP ENABLE INPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE ONE PULSE/BIT ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES
- PIN COMPATIBLE WITH INDUSTRY STANDARD 8K PROMs

Description

The HM-7681 is a fully decoded high speed Schottky TTL 8192 bit Field Programmable ROM in a 1K word by 8 bit/word format with "Three State" outputs. This PROM is available in a 24 pin D.I.P. (ceramic or power plastic).

All bits are manufactured storing a logic "1" (Positive Logic) and can be selectively programmed for a logical "0" in any one bit position.

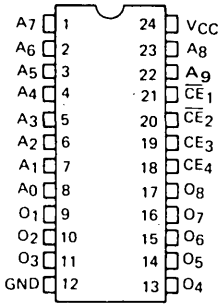
Nickel-chromium fuse technology is used on this and all other HARRIS Bipolar PROMs.

The HM-7681 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

There are four chip enable inputs on the HM-7681. $\overline{CE}_1$, $\overline{CE}_2$ low, and CE_3, CE_4 high enables the chip.

Pinouts

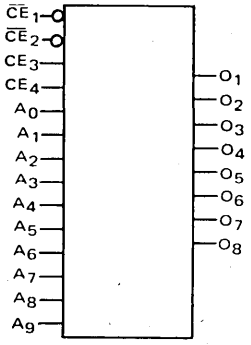
TOP VIEW – DIP



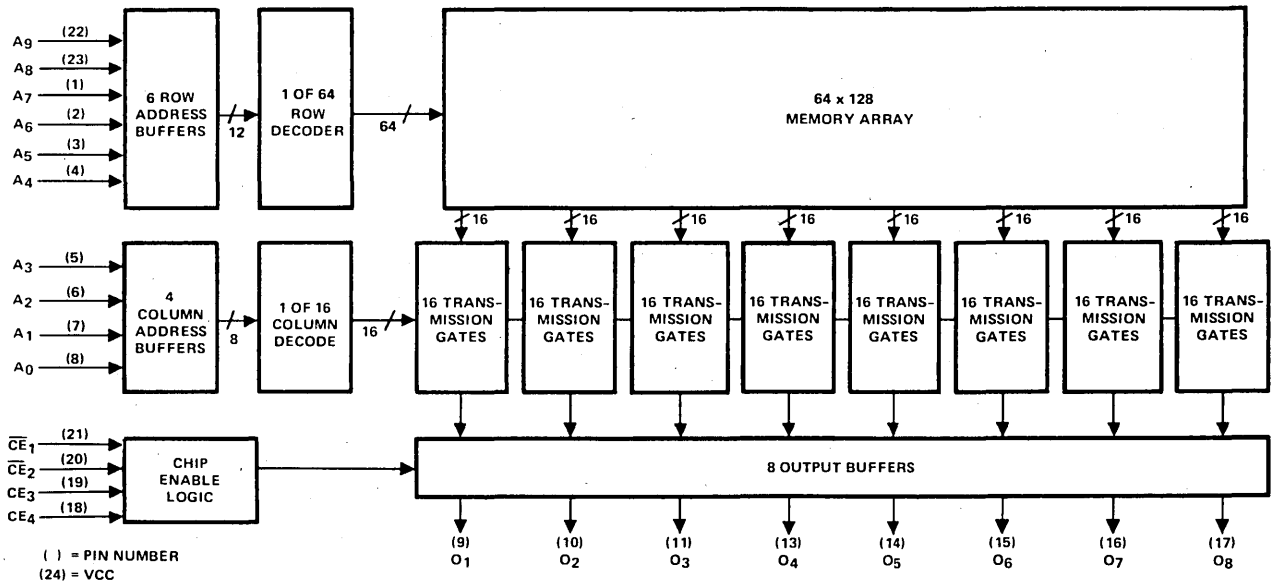
PIN NAMES

A_0 - A_9	Address Inputs
O_1 - O_8	Data Outputs
$\overline{CE}_1$, $\overline{CE}_2$, CE_3, CE_4	Chip Enable Inputs

Logic Symbol



Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	0°C to + 75°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7681-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7681-2/8 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/enable "1" Input Current "0"	– –	– –	+40 -250	µA µA	V_{IH} = VCC Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	– –	– 0.8	V V	VCC = VCC Min. VCC = VCC Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4 –	3.2 0.35	– 0.50	V V	I_{OH} = -2.0mA, VCC = VCC Min. I_{OL} = +16mA, VCC = VCC Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40	µA µA	V_{OH}, VCC = VCC Max. V_{OL} = 0.3V, VCC = VCC Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15	–	-100	mA	VCC = VCC Max., V_{OUT} = 0.0V One Output Only for a Max. of 1 Second
I_{CC}	Power Supply Current	–	130	170	mA	VCC = VCC Max. All Inputs Grounded

NOTE: Positive current defined as into device terminals.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

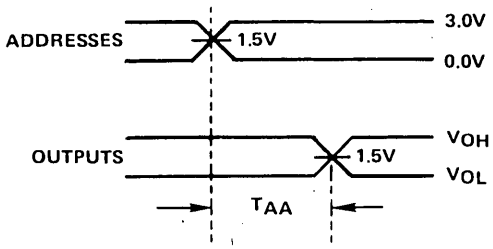
		HM-7681-5 5V ±5% 0°C to +75°C				HM-7681-2/8 5V ±10% –55°C to +125°C				
		"A"		STD		"A"		STD		
SYMBOL	PARAMETER	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	UNITS
T_{AA}	Address Access Time	40	50	50	70	–	60	–	90	ns
T_{EA}	Chip Enable Access Time	–	35	–	40	–	40	–	50	ns
T_{DA}	Chip Disable Access Time	–	35	–	40	–	40	–	50	ns

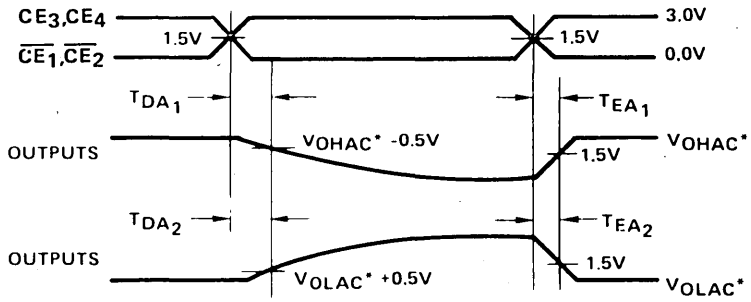
A.C. Limits guaranteed for worst case N^2 sequencing with maximum test frequency of 5MHz.

CAPACITANCE : T_A = 25°C (NOTE: Sampled and guaranteed – but not 100% tested.)

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	VCC = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	VCC = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS

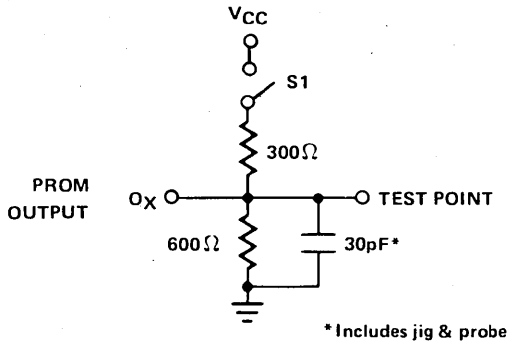




tr, tf < 5ns

*VOLAC AND VOHAC ARE THE MEASURED OUTPUT VOLTAGE LEVELS WHILE ENABLED.

A.C. TEST LOAD



*Includes jig & probe total capacitance

SYMBOL	PARAMETER	S1
T_{AA}	Address Access Time	Closed
T_{EA_1}	Chip Enable Access Time from "Three State" to V_{OH}	Open
T_{EA_2}	Chip Enable Access Time from "Three State" to V_{OL}	Closed
T_{DA_1}	Chip Disable Access Time from V_{OH} to "Three State"	Open
T_{DA_2}	Chip Disable Access Time from V_{OL} to "Three State"	Closed

HARRIS

HM-7685

HIGH SPEED 2K x 4 PROM

Features

- FAST ADDRESS ACCESS TIME
  - HM-7685 . . . . . 70 ns MAXIMUM
  - HM-7685A . . . . . 50 ns MAXIMUM
- "THREE STATE" OUTPUTS AND A SINGLE CHIP ENABLE INPUT
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES
- PIN COMPATIBLE WITH INDUSTRY STANDARD 8K PROMS

Description

The HM-7685 is a fully decoded high speed Schottky TTL 8192- bit Field Programmable ROM in a 2K word by a 4 bit/word format with "Three State" outputs. This PROM is available in an 18 pin DIP (ceramic or power plastic).

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

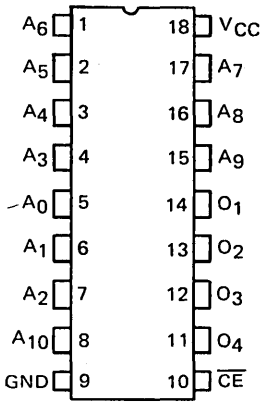
Nickel-chromium fuse technology is used on this and all other Harris Bipolar PROMs.

The HM-7685 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A. C. performance. The fuses in these test rows and columns are blown prior to shipment.

There is a chip enable on the HM-7685. $\overline{CE}$ low enables the chip.

Pinouts

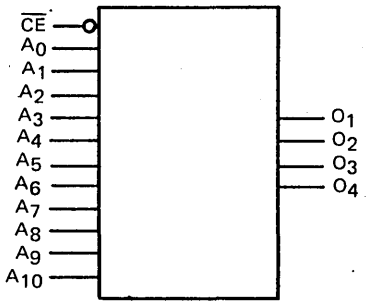
TOP VIEW - DIP

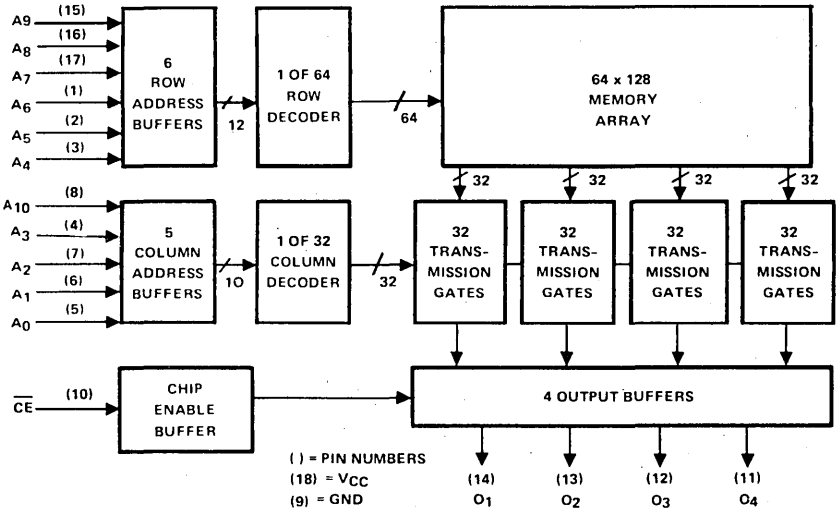


PIN NAMES

$A_0 - A_{10}$	Address Inputs
$O_1 - O_4$	Data Outputs
$\overline{CE}$	Chip Enable Input

Logic Symbol





ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7685-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-7685-2/-8 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– –	+40 -250	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	– –	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4 –	3.2 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15	–	-100	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	120	170	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

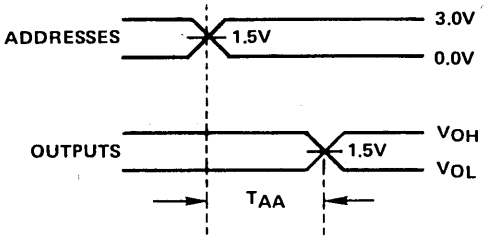
		HM-7685-5 5V ±5% 0°C to +75°C				HM-7685-2/-8 5V ±10% –55°C to +125°C				
		"A"		STD		"A"		STD		
SYMBOL	PARAMETER	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	UNITS
T_{AA}	Address Access Time	40	50	50	70	–	60	–	90	ns
T_{EA}	Chip Enable Access Time	–	30	–	40	–	35	–	50	ns
T_{DA}	Chip Disable Access Time	–	30	–	40	–	35	–	50	ns

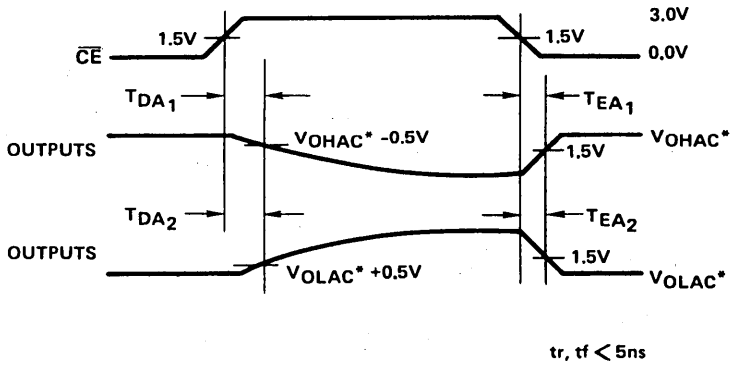
A.C. limits guaranteed for worst case N2 sequencing with maximum test frequency of 5MHz.

CAPACITANCE: T_A = 25°C (NOTE: Sampled and guaranteed – but not 100% tested.)

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS

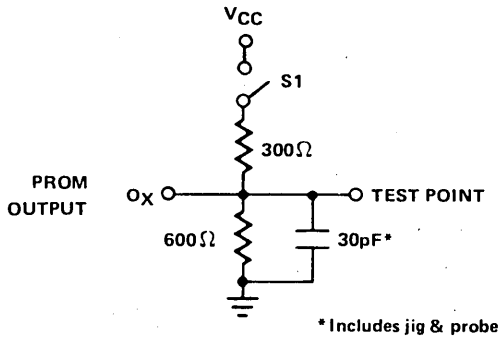




tr, tf < 5ns

*VOLAC AND VOHAC ARE THE MEASURED OUTPUT VOLTAGE LEVELS WHILE ENABLED.

A.C. TEST LOAD



*Includes jig & probe total capacitance

SYMBOL	PARAMETER	S1
T_{AA}	Address Access Time	Closed
T_{EA_1}	Chip Enable Access Time from "Three State" to V_{OH}	Open
T_{EA_2}	Chip Enable Access Time from "Three State" to V_{OL}	Closed
T_{DA_1}	Chip Disable Access Time from V_{OH} to "Three State"	Open
T_{DA_2}	Chip Disable Access Time from V_{OL} to "Three State"	Closed

HARRIS

HM-76161

HIGH SPEED 2K x 8 PROM

Features

- FAST ADDRESS ACCESS TIME
  - HM-76161 . . . . . 60 ns MAXIMUM
  - HM-76161A . . . . . 50 ns MAXIMUM
- "THREE STATE" OUTPUTS AND THREE CHIP ENABLE INPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE – ONE PULSE/BIT ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES
- PIN COMPATIBLE WITH INDUSTRY STANDARD 16K PROMs

Description

The HM-76161 is a fully decoded high speed Schottky TTL 16,384 bit Field Programmable ROM in a 2K word by 8 bit/word format with "Three State" outputs. This PROM is available in a 24 pin DIP (ceramic or power plastic).

All bits are manufactured storing a logical "1" (Positive Logic) and can be selectively programmed for a logical "0" in any bit position.

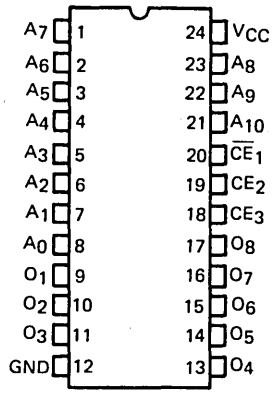
The nickel-chromium fuse technology used is the same as all other Harris Bipolar PROMs and the JAN approved MIL-M-38510 PROMs.

The HM-76161 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

There are three chip enable inputs on the HM-76161. $\overline{CE}_1$ low, CE_2 high, and CE_3 high enables the device.

Pinout

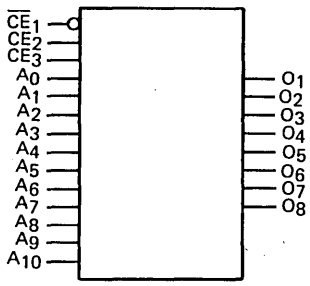
TOP VIEW - D I P



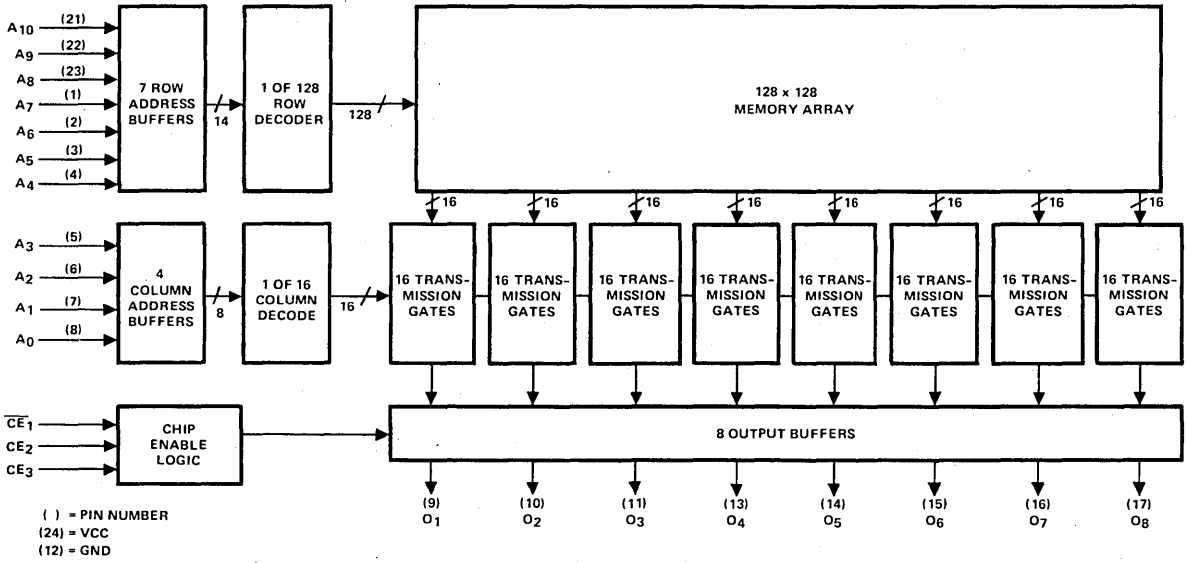
PIN NAMES

$A_0 - A_{10}$	Address Inputs
$O_1 - O_8$	Data Outputs
$\overline{CE}_1, CE_2, CE_3$	Chip Enable Inputs

Logic Symbol



Functional Diagram



( ) = PIN NUMBER
(24) = VCC
(12) = GND

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-76161-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-76161-2/-8 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical Measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/Enable "1"	–	–	+40	µA	V_{IH} = V_{CC} Max.
I_{IL}	Input Current "0"	–	–	-100	µA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0	–	–	V	V_{CC} = V_{CC} Min.
V_{IL}	Voltage "0"	–	–	0.8	V	V_{CC} = V_{CC} Max.
V_{OH}	Output "1"	2.4	3.2	–	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	Voltage "0"	–	0.35	0.50	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}	Output Disable "1"	–	–	+40	µA	V_{OH}, V_{CC} = V_{CC} Max.
I_{OLE}	Current "0"	–	–	-40	µA	V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15	–	-100	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	130	180	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

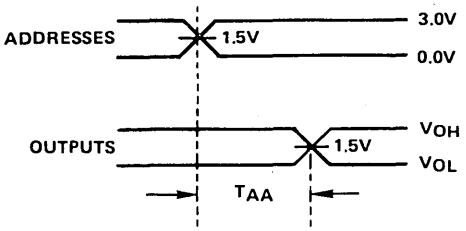
		HM-76161-5 5V ±5% 0°C to +75°C				HM-76161-2/-8 5V ±10% -55°C to +125°C		
		"A"		STD		STD		
SYMBOL	PARAMETER	TYP	MAX	TYP	MAX	TYP	MAX	UNITS
T_{AA}	Address Access Time	40	50	45	60	–	80	ns
T_{EA}	Chip Enable Access Time	–	40	–	40	–	50	ns
T_{DA}	Chip Disable Access Time	–	40	–	40	–	50	ns

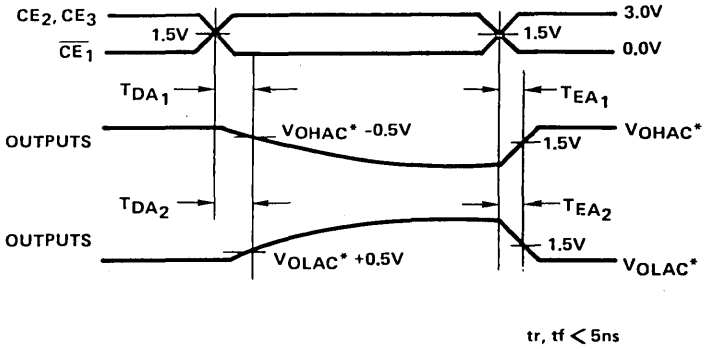
A.C. limits guaranteed for worst case N² sequencing with maximum test frequency of 5MHz

CAPACITANCE: T_A = 25°C (NOTE: Sampled and guaranteed – but not 100% tested.)

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS

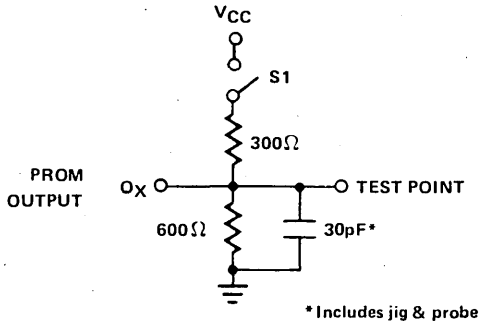




tr, tf < 5ns

*VOLAC AND VOHAC ARE THE MEASURED OUTPUT VOLTAGE LEVELS WHILE ENABLED.

A.C. TEST LOAD



*Includes jig & probe total capacitance

SYMBOL	PARAMETER	S1
T_{AA}	Address Access Time	Closed
T_{EA_1}	Chip Enable Access Time from "Three State" to V_{OH}	Open
T_{EA_2}	Chip Enable Access Time from "Three State" to V_{OL}	Closed
T_{DA_1}	Chip Disable Access Time from V_{OH} to "Three State"	Open
T_{DA_2}	Chip Disable Access Time from V_{OL} to "Three State"	Closed

HARRIS

HM-7616

2K x 8 PROM

Features

- FAST ADDRESS ACCESS TIME
  - HM-7616 . . . . . 60 ns MAXIMUM
  - HM-7616A . . . . . 50 ns MAXIMUM
- "THREE STATE" OUTPUTS AND A SINGLE CHIP ENABLE INPUT
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE – ONE PULSE/BIT ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES
- PIN COMPATIBLE WITH THE 2716

Description

HM-7616 is a fully decoded high speed Schottky TTL, 16,384 bit Field Programmable ROM in a 2K word by 8 bit/word format with "Three State" outputs. This PROM is available in a 24 pin DIP (ceramic or power plastic).

All bits are manufactured storing a logical "1" (Positive Logic) and can be selectively programmed for a logical "0" in any bit position.

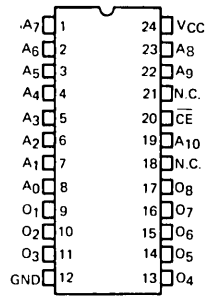
The Nickel-chromium fuse technology used is the same as all other Harris Bipolar PROMs and the JAN approved MIL-M-38510 PROMs.

The HM-7616 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

There is a chip enable input on the HM-7616. $\overline{CE}$ low enables the device.

Pinout

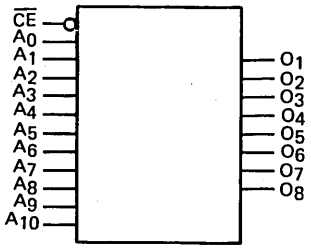
TOP VIEW - D.I.P.



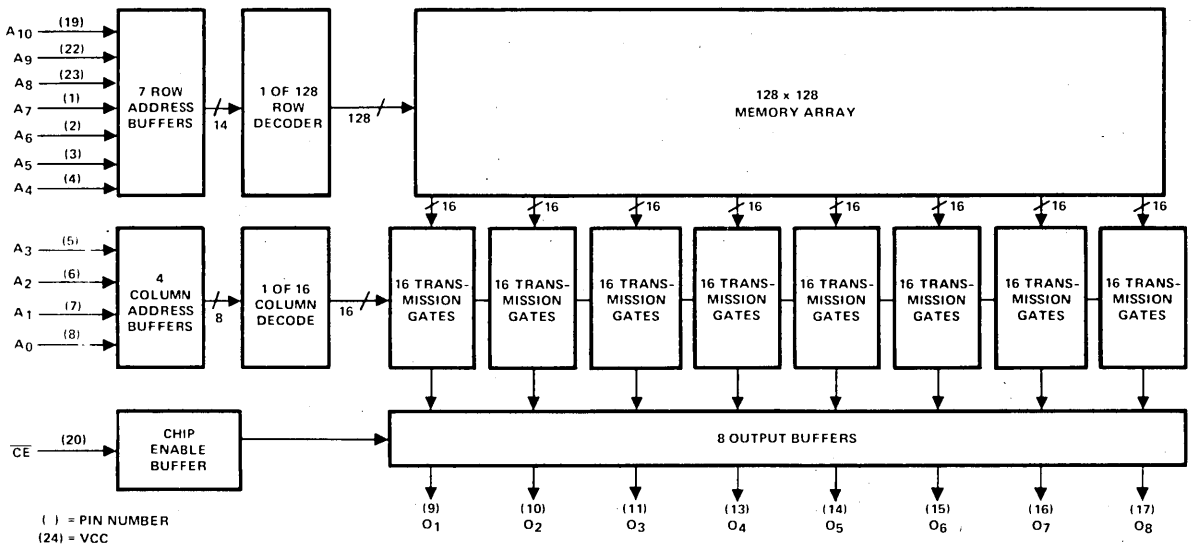
PIN NAMES

$A_0 - A_{10}$	Address Inputs
$O_1 - O_8$	Data Outputs
$\overline{CE}$	Chip Enable Input
N.C.	No Connection

Logic Symbol



Functional Diagram



( ) = PIN NUMBER
(24) = VCC
(12) = GND
(21) = N.C.
(18) = N.C.

Harris Semiconductor

MEMORY

ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7616-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7616-2/-8 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical Measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– –	+40 -100	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	– –	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4 –	3.2 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15	–	-100	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	130	180	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

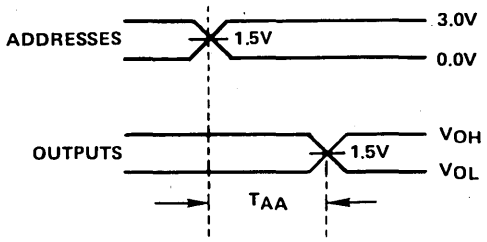
		HM-7616-5 5V ±5% 0°C to +75°C				HM-7616-2/-8 5V ±10% –55°C to +125°C		
		"A"		STD		STD		
SYMBOL	PARAMETER	TYP	MAX	TYP	MAX	TYP	MAX	UNITS
T_{AA}	Address Access Time	40	50	45	60	–	80	ns
T_{EA}	Chip Enable Access Time	–	40	–	40	–	50	ns
T_{DA}	Chip Disable Access Time	–	40	–	40	–	50	ns

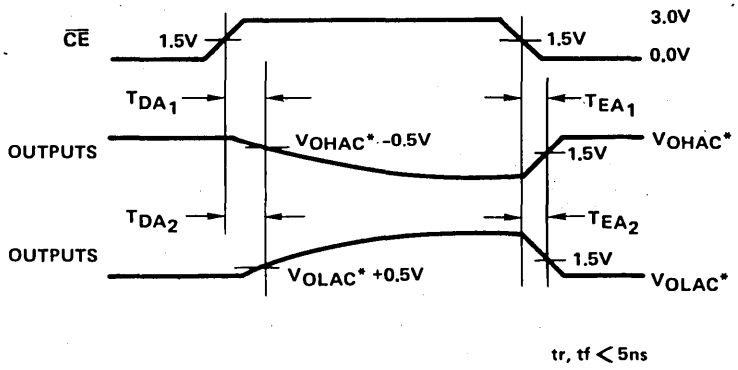
A.C. limits guaranteed for worst case N^2 sequencing with maximum test frequency of 5MHz.

CAPACITANCE: T_A = 25°C (NOTE: Sampled and guaranteed – but not 100% tested.)

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS

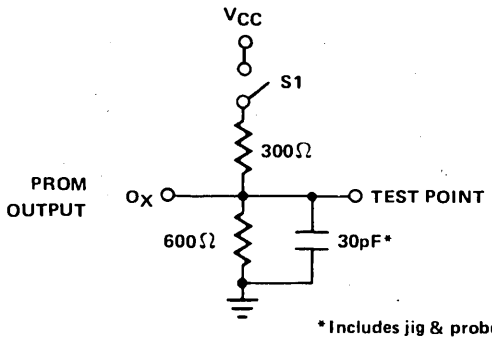




tr, tf < 5ns

*V_{OLAC} AND V_{OHAC} ARE THE MEASURED OUTPUT VOLTAGE LEVELS WHILE ENABLED.

A.C. TEST LOAD



*Includes jig & probe total capacitance

SYMBOL	PARAMETER	S1
T_{AA}	Address Access Time	Closed
T_{EA_1}	Chip Enable Access Time from "Three State" to V_{OH}	Open
T_{EA_2}	Chip Enable Access Time from "Three State" to V_{OL}	Closed
T_{DA_1}	Chip Disable Access Time from V_{OH} to "Three State"	Open
T_{DA_2}	Chip Disable Access Time from V_{OL} to "Three State"	Closed

HARRIS

HM-76165

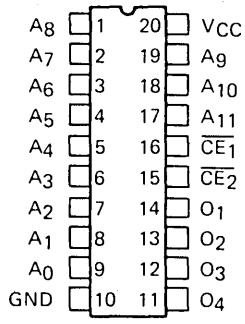
4K x 4 PROM

Features

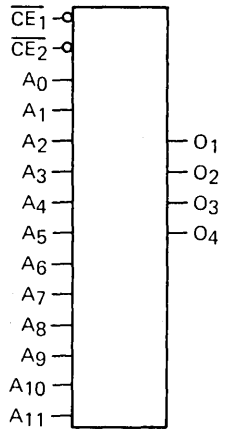
- 60ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OUTPUTS WITH TWO ACTIVE LOW CHIP ENABLES
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES
- INDUSTRY STANDARD 0.300 INCH 20 PIN PACKAGE
- PRODUCED ON MIL-M-38510 QUALIFIED WAFER FAB LINE
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT TYPICALLY ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY

Pinout

TOP VIEW



Logic Symbol



Description

The HM-76165 PROM is a fully decoded Schottky TTL 16,384 bit field programmable ROM in a 4K word by 4 bit/word format with "Three State" outputs. This PROM is available in a 20 pin 0.300 inch wide DIP.

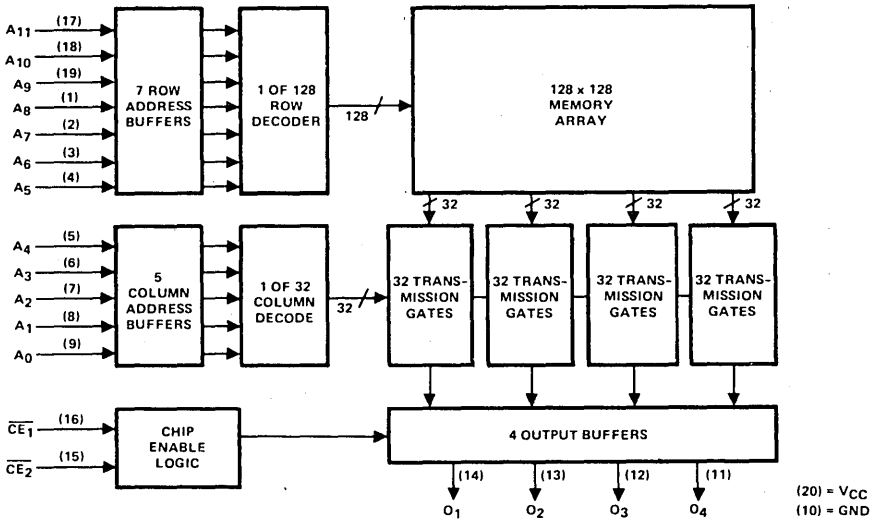
All bits are manufactured storing a logical "1" and can be selectively programmed for a logical "0" in any bit position.

MIL-M-38510 qualified NiCr technology is used on the HM-76165 and all other HARRIS bipolar PROMs.

The HM-76165 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

The HM-76165 utilizes two chip enables where $\overline{CE_1}$ low and $\overline{CE_2}$ low enables the device.

Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-76165-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-76165-2/-8 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical Measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– -50.0	+40 -100	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.80	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4 –	3.2 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}(1) I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15	–	-100	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	120	170	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
(1) I_{OHE} = +60µA for -2 and -8.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

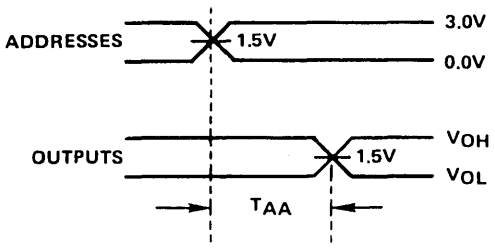
		HM-76165-5 5V ±5% 0°C to +75°C			HM-76165-2/-8 5V ±10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	–	45	60	–	50	80	ns
T_{EA}	Chip Enable Access Time	–	25	35	–	30	40	ns
T_{DA}	Chip Disable Access Time	–	25	35	–	30	40	ns

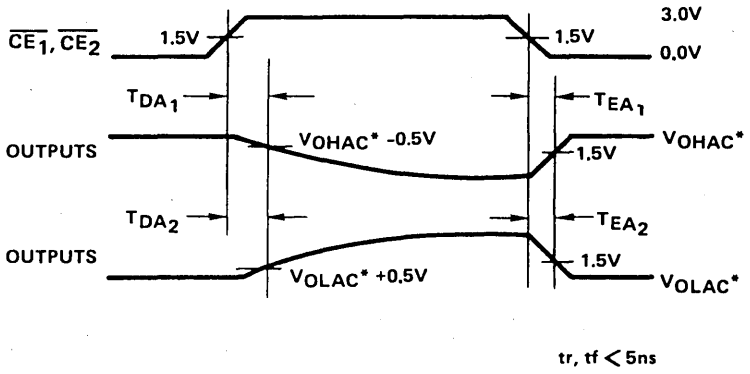
A.C. limits guaranteed for worst case N^2 sequencing with maximum test frequency of 5MHz.

CAPACITANCE: T_A = 25°C (NOTE: Sampled and guaranteed – but not 100% tested.)

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS

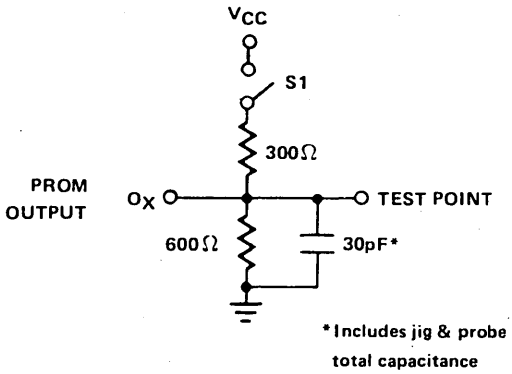




tr, tf < 5ns

*VOLAC AND VOHAC ARE THE MEASURED OUTPUT VOLTAGE LEVELS WHILE ENABLED.

A.C. TEST LOAD



*Includes jig & probe total capacitance

SYMBOL	PARAMETER	S1
T_{AA}	Address Access Time	Closed
T_{EA_1}	Chip Enable Access Time from "Three State" to V_{OH}	Open
T_{EA_2}	Chip Enable Access Time from "Three State" to V_{OL}	Closed
T_{DA_1}	Chip Disable Access Time from V_{OH} to "Three State"	Open
T_{DA_2}	Chip Disable Access Time from V_{OL} to "Three State"	Closed

HARRIS

HM-76321

4K x 8 PROM

Features

- 65ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OUTPUTS AND TWO CHIP ENABLE CONTROLS
- SIMPLE HIGH SPEED PROGRAMMING - ONE PULSE/BIT TYPICAL
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE
- PRODUCED ON MIL-M-38510 QUALIFIED WAFER FAB LINE
- INDUSTRY STANDARD 24 PIN PACKAGE

Description

The HM-76321 is a fully decoded Schottky TTL 32,768 bit field programmable ROM in a 4K word by 8 bit/word format with "Three State" outputs. This PROM is available in a 24 pin DIP.

All bits are manufactured storing a logical "1" (Positive Logic) and can be selectively programmed for a logical "0" in any bit position.

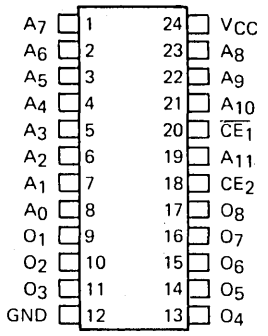
MIL-M-38510 qualified NiCr technology is used on the HM-76321 and all other HARRIS Bipolar PROMs.

The HM-76321 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

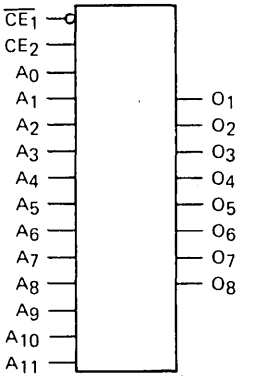
The HM-76321 utilizes two chip enable controls, where $\overline{CE_1}$ low and CE_2 high enables the device.

Pinout

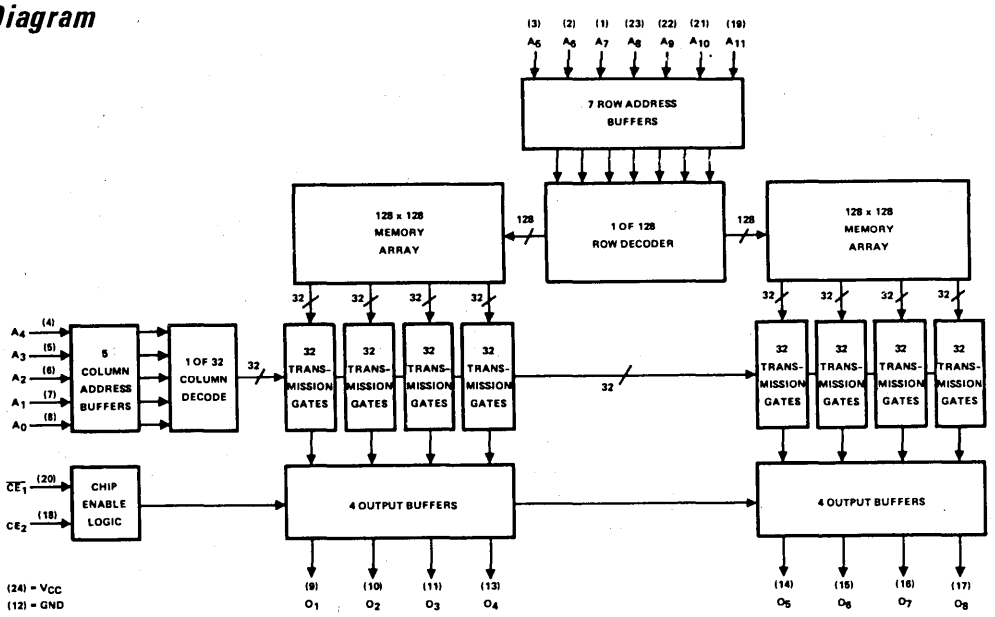
TOP VIEW



Logic Symbol



Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-76321-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-76321-2/-8 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical Measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– -50.0	+40 -100	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4 –	3.2 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}(1) I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15	–	-100	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	–	190	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
(1) I_{OHE} = +100µA for -2 and -8.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

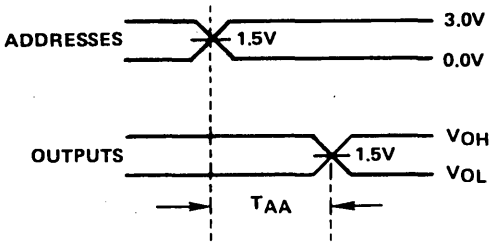
		HM-76321-5 5V ±5% 0°C to +75°C			HM-76321-2/-8 5V ±10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	–	45	65	–	–	85	ns
T_{EA}	Chip Enable Access Time	–	25	35	–	–	40	ns
T_{DA}	Chip Disable Access Time	–	25	35	–	–	40	ns

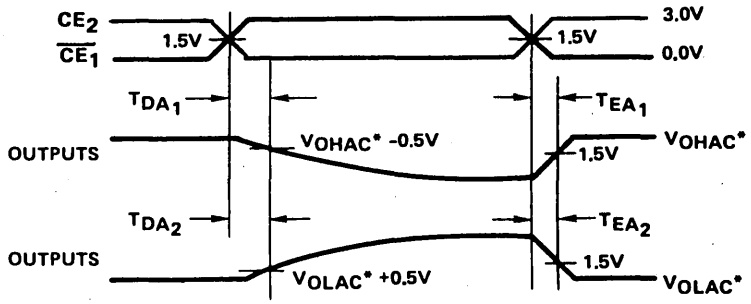
A.C. limits guaranteed for worst case N^2 sequencing with maximum test frequency of 5MHz.

CAPACITANCE: T_A = 25°C (NOTE: Sampled and guaranteed – but not 100% tested.)

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS

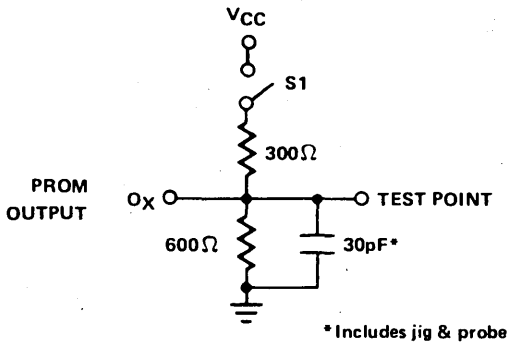




tr, tf < 5ns

*VOLAC AND VOHAC ARE THE MEASURED OUTPUT VOLTAGE LEVELS WHILE ENABLED.

A.C. TEST LOAD



*Includes jig & probe total capacitance

SYMBOL	PARAMETER	S1
T_{AA}	Address Access Time	Closed
T_{EA_1}	Chip Enable Access Time from "Three State" to V_{OH}	Open
T_{EA_2}	Chip Enable Access Time from "Three State" to V_{OL}	Closed
T_{DA_1}	Chip Disable Access Time from V_{OH} to "Three State"	Open
T_{DA_2}	Chip Disable Access Time from V_{OL} to "Three State"	Closed

HARRIS

HM-76641

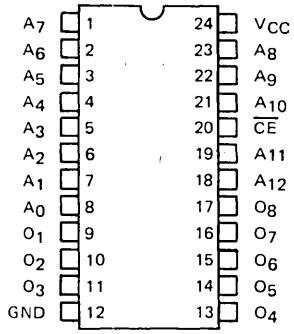
8K x 8 PROM

Features

- 85ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OUTPUTS
- ACTIVE LOW CHIP ENABLE CONTROL
- HIGHEST DENSITY AVAILABLE IN THE INDUSTRY
- FOUR FOLD INCREASE IN DENSITY OVER CURRENTLY AVAILABLE 16K PROMs WITH 1/4 POWER DISSIPATION PER BIT
- INDUSTRY STANDARD 24 PIN PACKAGE
- SIMPLE HIGH SPEED PROGRAMMING - ONE PULSE/BIT TYPICAL
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE
- PRODUCED ON MIL-M-38510 QUALIFIED WAFER FAB LINE

Pinout

TOP VIEW



Description

The HM-76641 is a fully decoded Schottky TTL 65,536 bit field programmable ROM in an 8K word by 8 bit/word format with "Three State" outputs. This PROM is available in a 24 pin DIP.

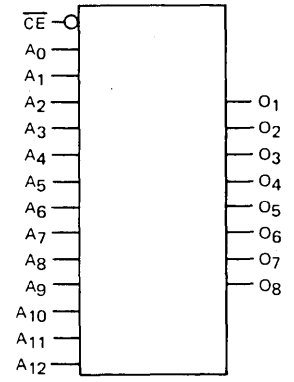
All bits are manufactured storing a logical "1" (Positive Logic) and can be selectively programmed for a logical "0" in any bit position.

MIL-M-38510 qualified NiCr technology is used on the HM-76641 and all other HARRIS bipolar PROMs.

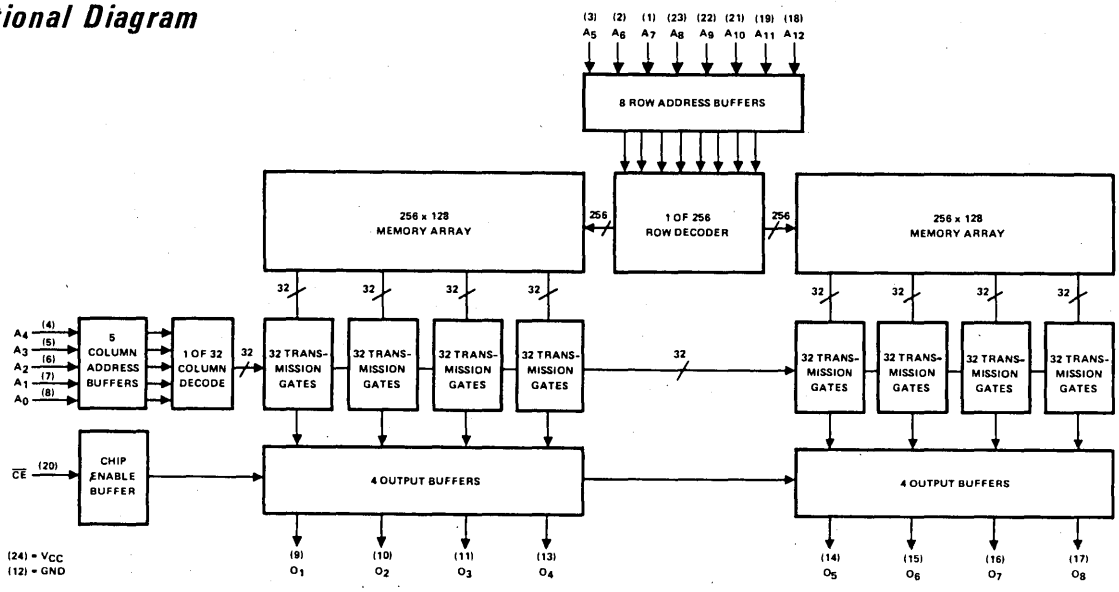
The HM-76641 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

The HM-76641 utilizes a single chip enable, $\overline{CE}$, which when low enables the device.

Logic Symbol



Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-76641-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-76641-2/-8 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical Measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– -50.0	+40 -100	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4 –	3.2 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}(1) I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15	–	-100	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	–	190	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
(1) I_{OHE} = +100µA for -2 and -8.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

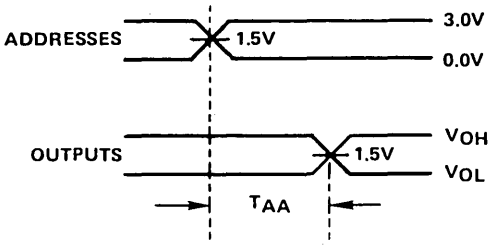
		HM-76641-5 5V ±5% 0°C to +75°C			HM-76641-2/-8 5V ±10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	–	50	85	–	–	100	ns
T_{EA}	Chip Enable Access Time	–	30	40	–	–	45	ns
T_{DA}	Chip Disable Access Time		30	40			45	ns

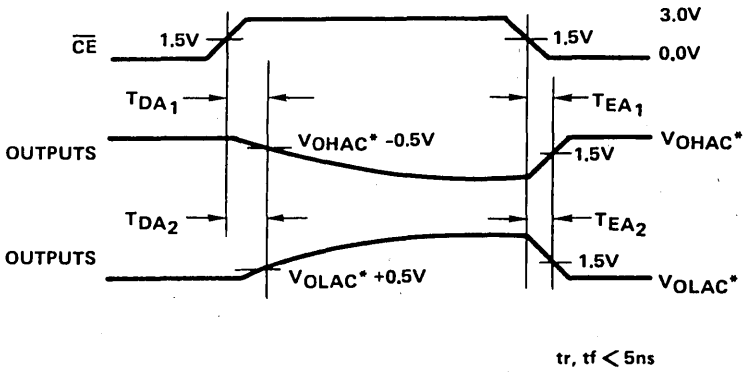
A.C. limits guaranteed for worst case N^2 sequencing with a maximum test frequency of 5MHz.

CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS

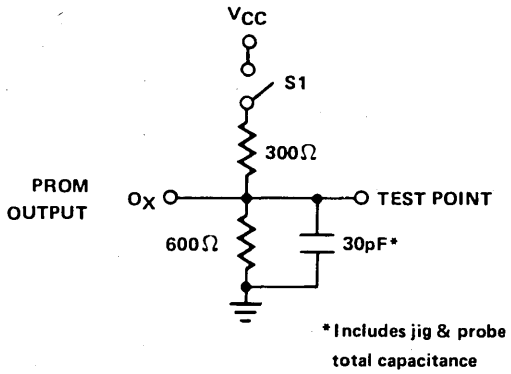




tr, tf < 5ns

*VOLAC AND VOHAC ARE THE MEASURED OUTPUT VOLTAGE LEVELS WHILE ENABLED.

A.C. TEST LOAD



*Includes jig & probe total capacitance

SYMBOL	PARAMETER	S1
T_{AA}	Address Access Time	Closed
T_{EA_1}	Chip Enable Access Time from "Three State" to V_{OH}	Open
T_{EA_2}	Chip Enable Access Time from "Three State" to V_{OL}	Closed
T_{DA_1}	Chip Disable Access Time from V_{OH} to "Three State"	Open
T_{DA_2}	Chip Disable Access Time from V_{OL} to "Three State"	Closed

All 76xxx series devices utilize the same programming method which is one of the characteristics that lends to the term "Generic" PROM.

Harris Generic PROMs have the industry's highest programming yield and exhibit an extremely high level of reliability in the field, however, this level of device quality can only be obtained if the PROM has been properly programmed to the data sheet specifications. Outlined below are the key points which deserve attention to assure that programming has been optimumly performed.

- Be certain that you are following the latest revision status of programming specifications.
- If you are utilizing a commercial programmer, be sure that the card set for Harris Generic PROMs is certified for the most recent revision level.
- Have the Programmer calibrated at routine intervals to assure that the electrical and mechanical characteristics are acceptable. This would include such things as:
  - ▸ Making certain that the socket which the device is placed into is clean, free of corrosion and is mechanically sound.
  - ▸ Check ribbon cable connectors for good continuity.
  - ▸ Making sure that all voltage levels conform to the programming specifications.
  - ▸ Assuring that all pulses are clean of distortion and exhibit the correct timing characteristics.

If there is any problem in determining how to follow any of these guidelines, contact a local Harris office for assistance.

PROGRAMMING PROCEDURE

The following is the generic programming procedure which is used for all Harris Generic 76xxx PROMs. Please note that the PD input(s) on power down devices can be considered equivalent to chip enable input(s) during the programming procedure in that they both disable the device. Also, the logic levels required to place the strobe input into the "transparent read" mode (essential during programming) will vary among the various device types.

The HM-76xxx PROMs are manufactured with all bits storing a logical "1" (output high). Any desired bit can be programmed to a logical "0" (output low) by following the simple procedure shown below. One may build their own programmer to satisfy the specifications described in the table, or use any of the commercially available programmers which meet these specifications. This PROM can be programmed automatically or by the manual procedure shown on the next page.

The HM-76XXX PROMs are manufactured with all bits storing a logical "1" (output high). Any desired bit can be programmed to a logical "0" (output low) by following the simple procedure shown below. One may build his own programmer to satisfy the specifications described in the table, or use any of the commercially available programmers which can meet these specifications.

PROGRAMMING SPECIFICATIONS

SYMBOL	PARAMETER	MINIMUM	RECOMMENDED OR TYPICAL	MAXIMUM	UNITS
V_{IH} V_{IL}	Address Input Voltage (1)	2.4 0.0	5.0 0.4	5.0 0.5	V V
V_{PH} (2) V_{PL} (3)	Programming/Verify Voltage to V_{CC}	12.0 4.5	12.0 4.5	12.5 5.5	V V
I_{ILP}	Programming Input Low Current at V_{PH}	–	-300	-600	μA
tr tf	Programming (V_{CC}) Voltage Rise and Fall Time	1.0 1.0	1.0 1.0	10.0 10.0	μs μs
td	Programming Delay	10	10	100	μs
tp	Programming Pulse Width (4)	90	100	110	us
P.D.C.	Programming Duty Cycle	–	50	90	%
V_{OPE} V_{OPD}	Output Voltage Enable (5) Disable	10.5 4.5	10.5 5.0	11.0 5.5	V V
I_{OPE}	Output Voltage Enable Current	–	–	10.0	mA
Ta	Ambient Temperature	–	25	75	°C

During programming the chip must be disabled for proper operation.

NOTES:
1. No inputs should be left open for V_{IH}.
2. V_{PH} source must be capable of supplying one ampere.
3. It is recommended that dual verification be made at V_{PL} min and V_{PL} max.
4. Note step 10 in programming procedure.
5. Disable condition will be met with output open circuited.

PROGRAMMING PROCEDURE

1. Address the PROM with the binary address of the word to be programmed. Address inputs are TTL compatible. An open circuit should not be used to address the PROM.
2. Bring the $\overline{CE}_X$ input(s) high and the $\overline{CE}_X$ input(s) low to disable the device. The disabling of the device during programming is an essential step in correctly programming all Harris PROMs. The chip enables are TTL compatible. An open circuit should not be used to disable the device.
3. Disable the programming circuitry by applying a voltage of V_{OPD} to the outputs of the PROM. Any output may be left open to achieve the disable.
4. Raise V_{CC} to V_{PH} with rise time less than or equal to t_r.
5. After a delay equal to or greater than t_d, apply a pulse with amplitude of V_{OPE} and duration of t_p to the output selected for programming. Note that the PROM is supplied with fuses intact, which generates an output high. Programming a fuse will cause the output to go low.
6. Other bits in the same word may be programmed while the V_{CC} input is raised to V_{PH} by applying output enable pulses to each output which is to be programmed. The output enable pulses must be separated by a minimum interval of t_d.
7. Lower V_{CC} to 4.5 volts following a delay of t_d from last programming enable pulse applied to an output.
8. Enable the PROM for verification by applying V_{IL} to $\overline{CE}_X$ and V_{IH} to CE_X.
9. Repeat verification (step 8) at V_{CC} = 5.5 volts.
10. If any bit does not verify as programmed, repeat steps 2 through 9 until the bit has received a total of 1ms of programming time. Bits which do not program within 1ms are programming rejects. No further attempt to program these parts should be made.
11. Repeat steps 1 through 10 for all other bits to be programmed in the PROM.
12. Programming rejects returned to the factory must be accompanied by data giving address, desired data, and actual output data of the location in which a programming failure has occurred.

TYPICAL PROGRAMMING CIRCUIT

The circuit and timing diagrams shown in Figures 1 and 2 will establish the proper programming conditions for the output enable pulses. This allows the use of standard TTL parts for all logic inputs to the PROM. Note the gate which senses the output must withstand inputs up to 11.0 volts during programming.

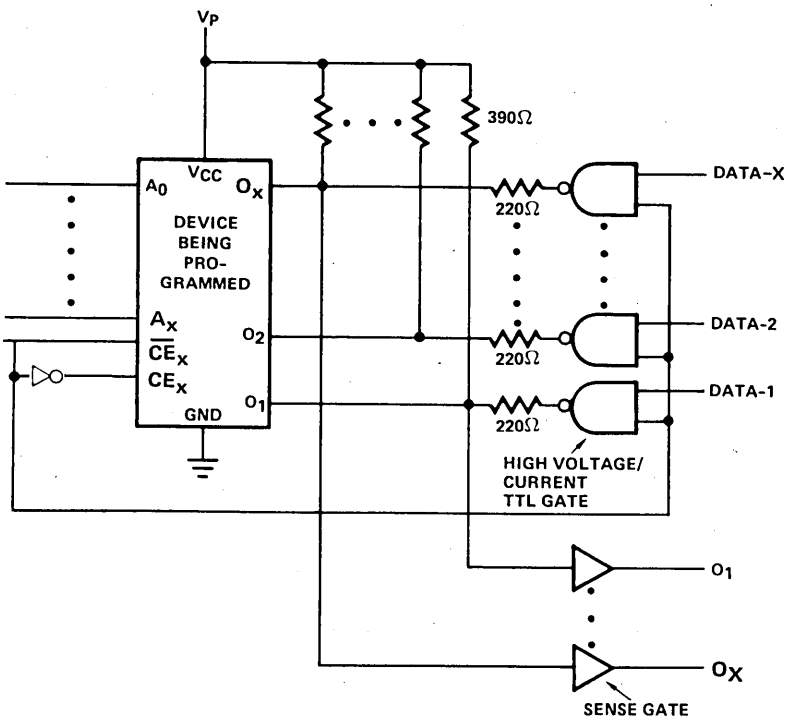


FIGURE 1

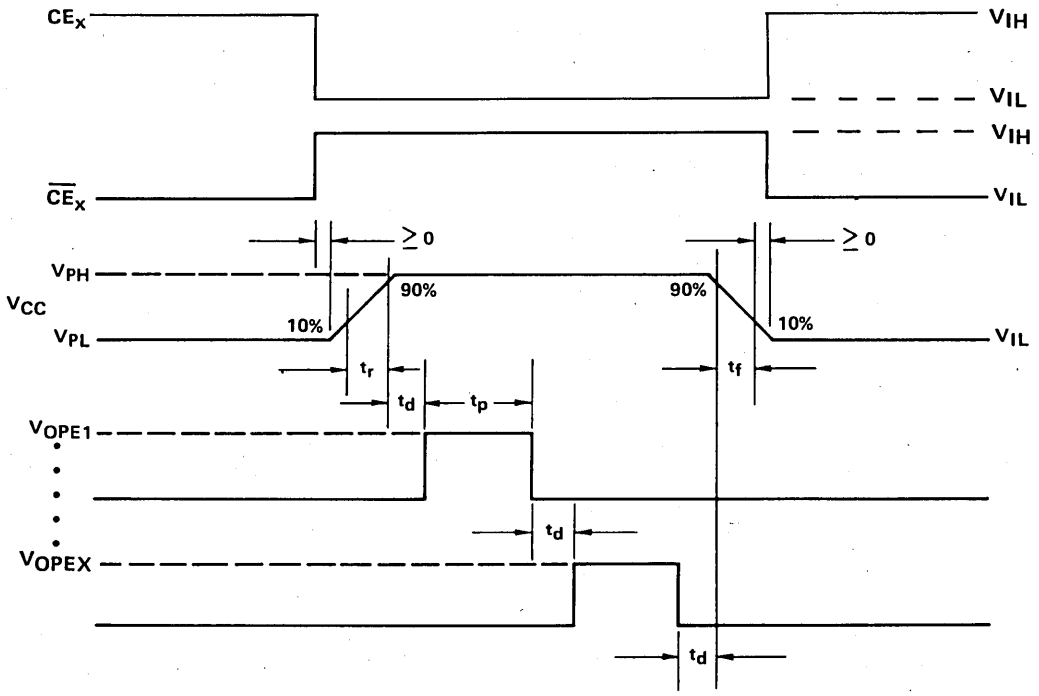


FIGURE 2

Waveforms Applied to the Device Pins During Programming

HARRIS

SEMICONDUCTOR DIGITAL PRODUCTS DIVISION

JAN-0512

512 BIT, BIPOLAR PROM

MIL/M38510/20101

Features

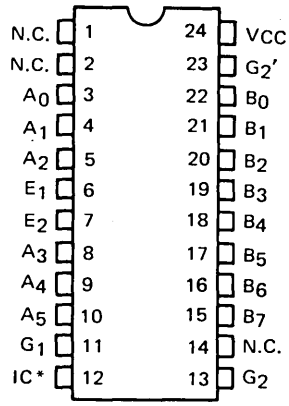
- FIELD PROGRAMMABLE
- 64 WORDS/8 BITS PER WORD
- FULLY DECODED
- DTL/TTL COMPATIBLE
- 55ns ACCESS TIME

Description

The JAN-0512 is a field programmable 64 word by 8 bit PROM. In an unprogrammed memory, all "Memory Elements" are short circuits so that logical "zeros" appear at each output bit position for any address input. "Electronic Programming" involves the alteration of specific "Memory Elements" to create logical "ones" in selected bit positions. This alteration is irreversible and cannot be accomplished under normal operating conditions.

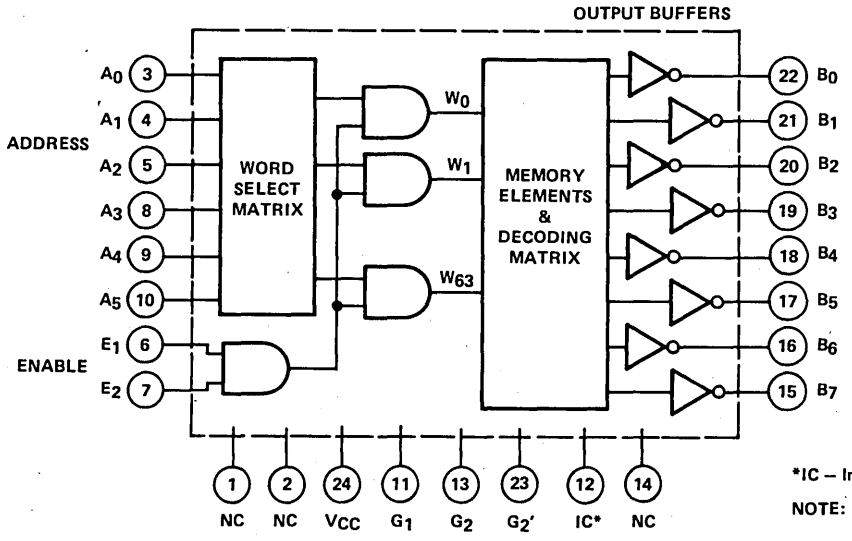
Pinout

TOP VIEW – D.I.P.



*Must be left open circuit

Block Diagram



*IC – Internal Connection must be left open

NOTE: For operational condition, return pins 11, 13, and 23 to system ground.

Harris Semiconductor

MEMORY

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range	-0.5 V_{DC} to 7.0 V_{DC}
Input Voltage Range	-1.5 V_{DC} at -12mA to 5.5V_{DC}
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 10 Seconds)	300°C
Thermal Resistance, Junction-to-Case	JC' Case J = 30°C/w
Output Supply Voltage	-0.5V_{DC} to 7.0V_{DC}
Output Sink Current	+30mA
Maximum Power Dissipation, P_D	575mWdc
Maximum Junction Temperature, T_J	175°C

RECOMMENDED OPERATING CONDITIONS

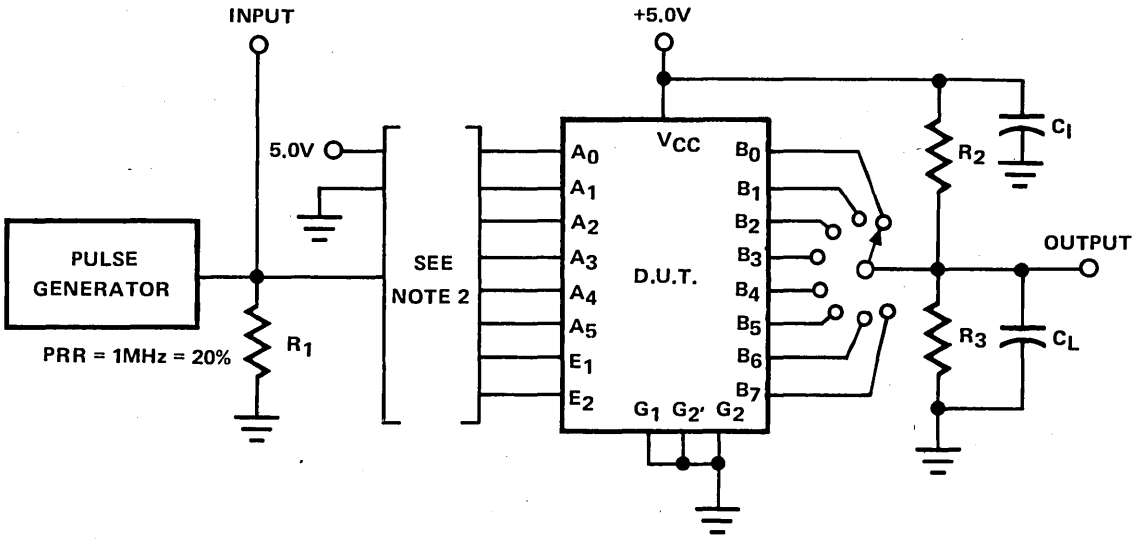
Supply Voltage	4.75 V_{DC} Min. to 5.25V_{DC} Maximum
Minimum High Level Input Voltage	2.0V_{DC}
Maximum Low Level Input Voltage	0.8V_{DC}
Normalized Fanout (Each Output)	6 Maximum (10mA)
Ambient Operating Temperature Range	-55°C to +125°C

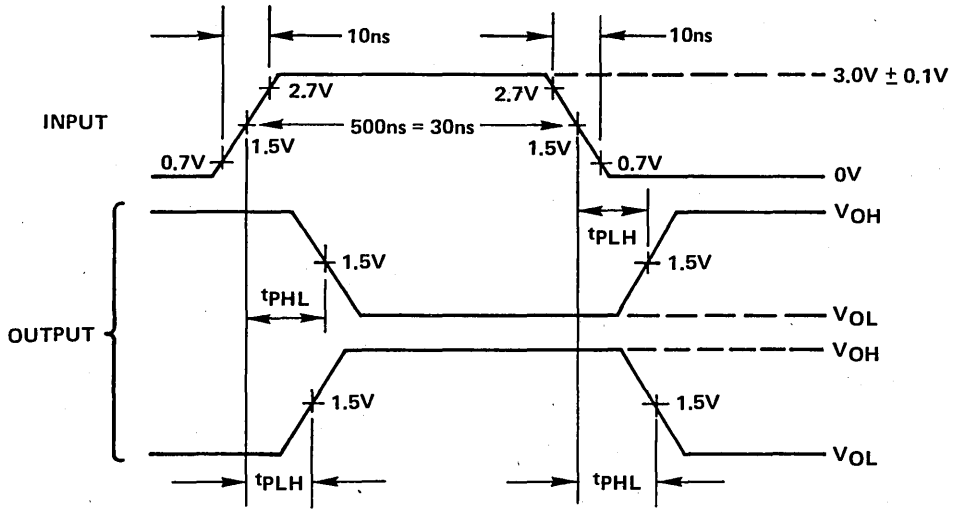
ELECTRICAL CHARACTERISTICS

The electrical characteristics are as specified in the table and apply over the full recommended ambient operating temperature range, unless otherwise specified.

SYMBOL	TEST	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
V_{OL}	Low Level Output Voltage		0.45	Volts	V_{CC} = 4.75V V_{IN} = 2.0V I_{OL} = 10mA
V_{IC}	Input Clamp Voltage		-1.5	Volts	V_{CC} = 4.75V I_{IN} = -12mA T_A = 25°C
I_{CEX1}	Maximum Collector Cut-Off Current		100	μA	V_{CC} = 5.25V V_{OH} = 2.8V V_{IN} = 0.8V
I_{CEX2}			200	μA	V_{CC} = 5.25V V_{OH} = 5.25V V_{IN} = 0.8V
I_{IH1}	High Level Input Current		60	μA	V_{CC} = 5.25V V_{IN} = 2.4V;
I_{IH2}			100	μA	V_{CC} = 5.25V V_{IN} = 5.25; (1)
I_{IL}	Low Level Input Current	-0.2	-1.6	mA	V_{CC} = 5.25V V_{IN} = 0.4V; (2)
I_{CC}	Supply Current		100	mA	V_{CC} = 5.25V V_{IN} = 0
t_{PHL}	Propagation Delay Time High-to-Low Level Logic	25	140	ns	V_{CC} = 5.0V C_L = 30pF Min. R_1 = 470Ω ±5%
t_{PLH}	Propagation Delay Time Low-to-High Level Logic	25	140	ns	

NOTES: 1. When testing one E input, apply 5.25V to the other.
2. When testing one E input, apply GND to the other.

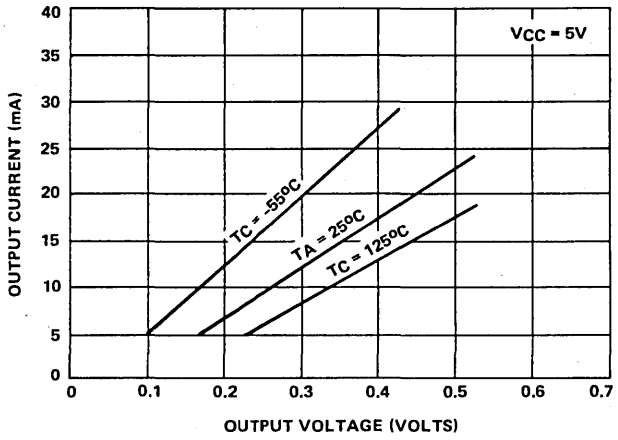




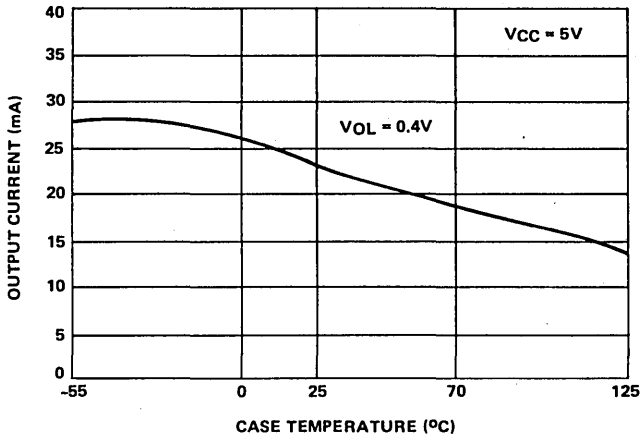
NOTES:

1. Pins 12 and 14 shall be left open.
2. The applicable test table should be selected from the altered item drawing.
3. $C_1 = 0.5\mu F \pm 10\%$; $R_1 = 50\Omega \pm 5\%$; $R_2 = 470\Omega \pm 5\%$; $R_3 = 1k\Omega \pm 5\%$; C_L = 30pF including jig and probe capacitance.

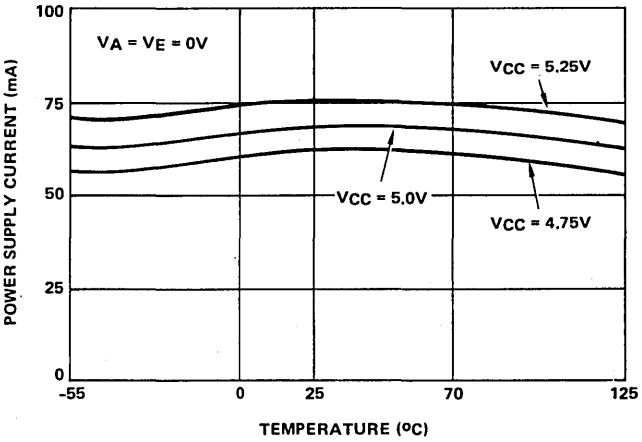
OUTPUT CHARACTERISTICS



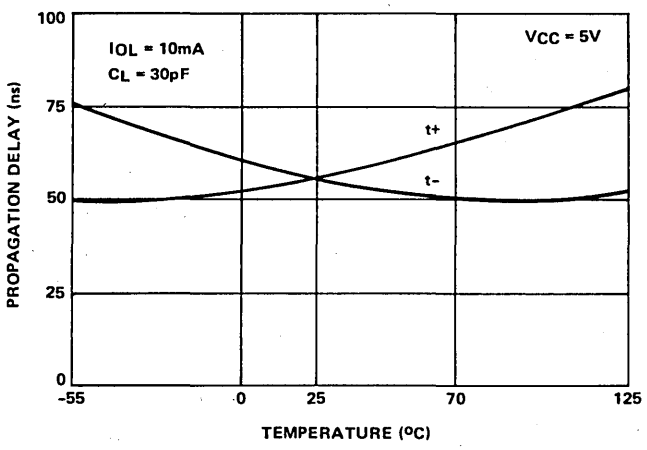
OUTPUT CURRENT vs. TEMPERATURE



POWER SUPPLY CURRENT vs. TEMPERATURE



PROPAGATION DELAY vs. TEMPERATURE



PROGRAMMING SPECIFICATIONS

PARAMETER	VALUE
Address Input Voltage High Logic Level Low Logic Level	 Open Circuit (1) -5.0V
Power Supply Voltage	+5.0V +5%, -0%
G_1 Voltage (2)	-5.0V
G_2 Voltage	0V
G_2' Voltage For Device Type 01 Circuit A	 Open
Maximum Programming Voltage	-7.0V
Maximum Programming Current	100mA
Maximum Number or Attempts to Program a Given Bit	2
Maximum Case Temperature During Programming	75°C

1. Open collector TTL gates meet this requirement.
2. G_1 must be connected to -5.0V prior to applying V_{CC} or programming voltage.

PROGRAMMING PROCEDURES

Using the test conditions of the table, the following procedures shall be used for programming the device:

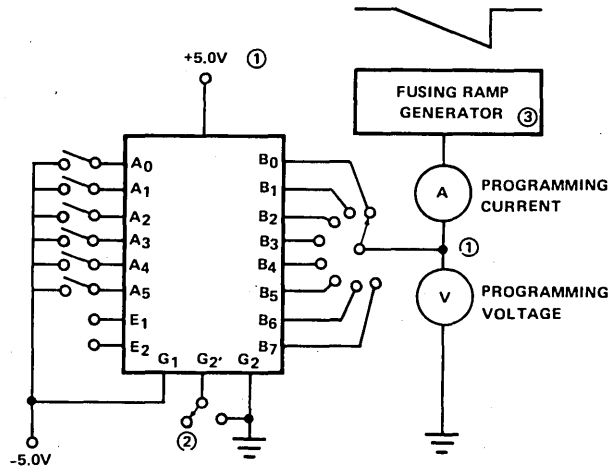
(a) Connect the device as shown in Figure 1, using the fusing generator of Figure 1 or the alternate circuit of Figure 2. The circuit shown in Figure 2 can be used in more automated programming systems. This circuit generates a current pulse which is at the proper voltage and current levels for fast reliable programming. The input programming pulse width shall be 750ms ±50ms. The number of attempts to program a given bit shall be as specified in the table.

(b) To address a particular word in the memory, set the input switches to the binary equivalent of that word, where a logical low level is -5.0V and a logical high level is an open circuit. (Do not return to supply). All output bits (B_0, B_1, . . . B_7) of this word are now available for programming.

(c) With the output current limited (as specified in the table), apply a negative going current pulse to the pin associated with the first bit to be changed from a logical low level to a logical high level. This is most easily accomplished by connecting the negative terminal of a variable power supply to the proper output pin and manually increasing the voltage to approximately 6.0V.

(d) Skipping any bit which is to remain a logical low level, repeat step (c) for each logical low level in the word being addressed. Not more than one bit shall be programmed at a time.

(e) Set the next input address and repeat steps (c) and (d). This procedure is repeated for each input address for which a specific output word pattern is desired. Note that all addresses do not have to be programmed at the same time, nor do all output bits for a given address. A logical low level can always be changed to a logical high level, simply by repeating steps (b) and (c). A logical low level, once programmed to a logical high level, cannot be reprogrammed.



NOTES:
1. Connect -5.0V to G_1 before applying V_{CC} or programming voltage.
2. For device type 01, G_2' shall be open.
3. Generator characterisitics are defined in Programming Procedures.

FIGURE 1
PROGRAMMING CONNECTIONS

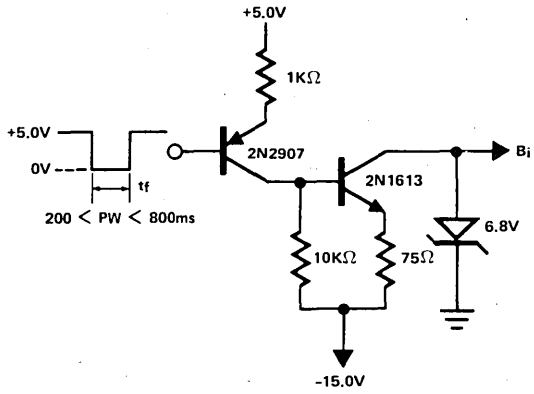


FIGURE 2
PROGRAMMING CIRCUIT

38510/	PRODUCT	NUMBER OF BITS	ORGANIZATION	OUTPUTS	NUMBER OF PINS	QPL STATUS
20101BJB	HPROM-0512	512	64X8	Open Collector	24	Approved QPL 1
20701BEB	HMI-7602	256	32X8	Open Collector	16	Approved QPL 1
20702BEB	HMI-7603	256	32X8	Three State	16	Approved QPL 1
20301BEB	HMI-7610	1024	256X4	Open Collector	16	Approved QPL 1
20302BEB	HMI-7611	1024	256X4	Three State	16	Approved QPL 1
20401BEB	HMI-7620	2048	512X4	Open Collector	16	Approved QPL 1
20402BEB	HMI-7621	2048	512X4	Three State	16	Approved QPL 1
20801BJB	HMI-7640	4096	512X8	Open Collector	24	Approved QPL 1
20802BJB	HMI-7641	4096	512X8	Three State	24	Approved QPL 1
20601BVB	HMI-7642	4096	1024X4	Open Collector	18	Approved QPL 1
20602BVB	HMI-7643	4096	1024X4	Three State	18	Approved QPL 1
20904BJB	HMI-7681	8192	1024X8	Three State	24	QPL 1 Projected 1st Qtr. 1983
20902BVB	HMI-7685	8192	2048X4	Three State	18	QPL 1 Projected 1st Qtr. 1983
21002BJB	HMI-76161	16384	2048X8	Three State	24	QPL 1 Projected 1st Qtr. 1983
21004BRB	HMI-76165	16384	4096X4	Three State	20	*
21101BJB	HMI-76321	32768	4096X8	Three State	24	*
21201BJB	HMI-76641	65536	8192X8	Three State	24	*

* Qualification will be scheduled when the finalized issue of the applicable 38510 slash sheet is released.

HARRIS

SEMICONDUCTOR DIGITAL PRODUCTS DIVISION

MONOLITHIC DIODE MATRICES

Features

- FIELD PROGRAMMABLE
- CMOS COMPATIBLE
- ZERO POWER DISSIPATION
- FAST SWITCHING
- FIVE POPULAR ORGANIZATIONS

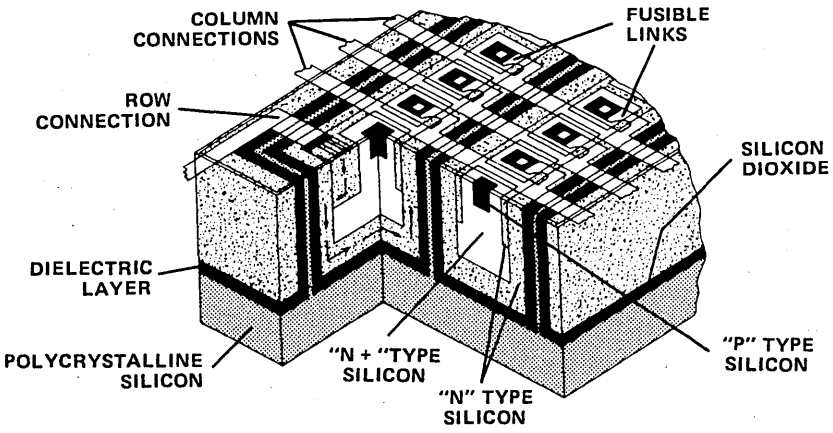
Description

Designed with the CMOS circuit engineer in mind, these versatile diode matrices allow the application of logically powerful programmable solutions to low power CMOS system applications.

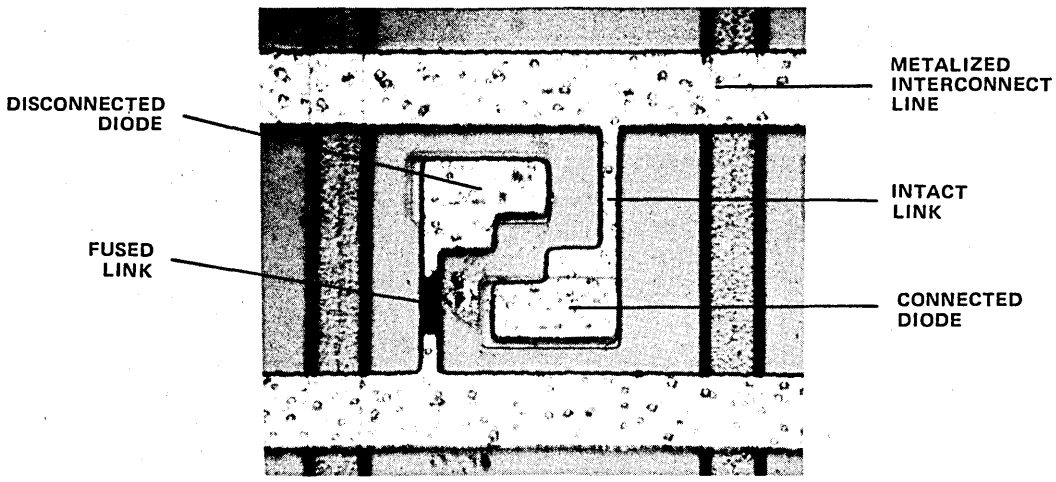
These devices incorporate an advanced dielectric isolation process to eliminate the need for power supply pins and allow parasitic free operation.

Programming is accomplished by cleanly vaporizing a fusible link by application of a brief high voltage pulse to a selected array element. This operation open circuits a row to column orring diode eliminating their former interaction.

Monolithic Structure



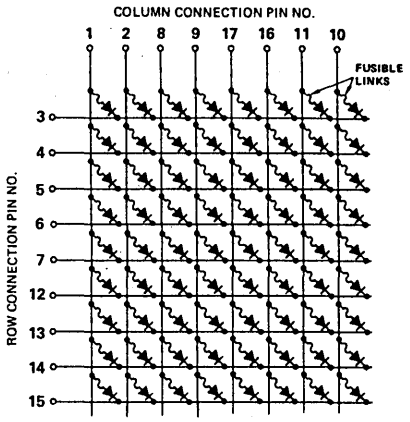
Fusible Link System



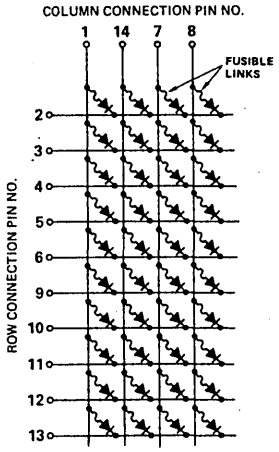
Monolithic Diode Matrices

HM-0168 6 x 8 DIODE MATRICES
HM-0186 8 x 6 DIODE MATRICES
HM-0410 4 x 10 DIODE MATRICES
HM-0104 10 x 4 DIODE MATRICES
HM-0198 9 x 8 DIODE MATRICES

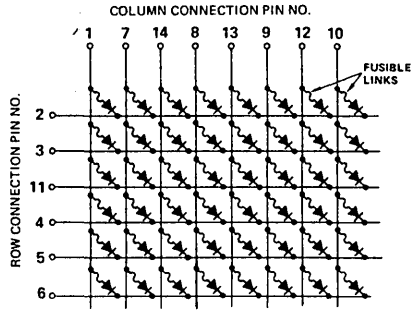
HM-0198



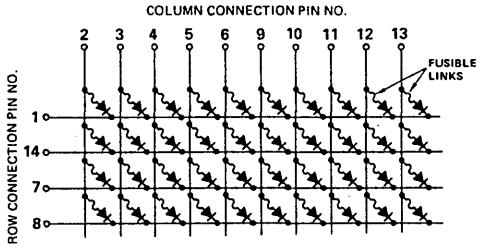
HM-0104



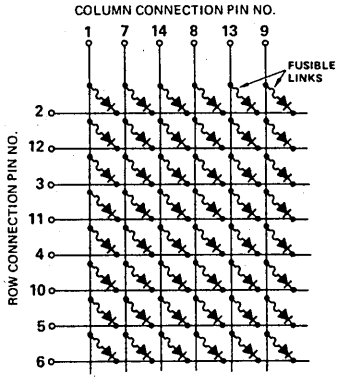
HM-0168



HM-0410



HM-0186



CUSTOM PATTERNS

When ordering a matrix with a custom pattern: Send a paper tape, or copy a matrix pattern and circle out those diodes to be removed from the matrix. Another method to clearly identify a pattern is to call out respective anode and cathode for each diode to be removed, by package pin number.

ABSOLUTE MAXIMUM RATINGS

Forward Current	100mA
Surge Current (100 μs Max.)	200mA
Total Ckt. Dissipation (Still Air)	450mW
Storage Temperature (Ambient)	-65°C to +150°C

Maximum Ratings are limiting values above which permanent damage may occur.

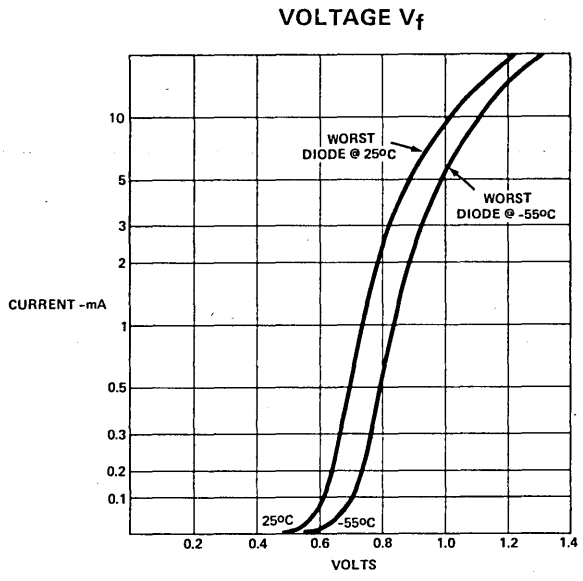
ELECTRICAL CHARACTERISTICS

		HM-0XXX-5		HM-0XXX-2 HM-0XXX-8			
	T_A	0°C to +75°C		-55°C to +125°C			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS	CONDITIONS
V_F	Forward Voltage		1.5 0.9		1.5 .9	V V	I_F = 20mA I_F = 1mA
BV_R	Reverse Breakdown Voltage	20		30		V	I_{BV} = 100μA
		25°C		25°C			
t_{rr}	Reverse Recovery Time		50		100	ns	I_F = 10mA to I_R = 10mA Recovery to 1mA
C_C	Crosspoint Capacitance (1)				8	pF	V_R = 5V; f = 1MHz (2)

(1) Guaranteed but not 100% tested.

(2) $C_C \propto \frac{1}{V_{BIAS}}$

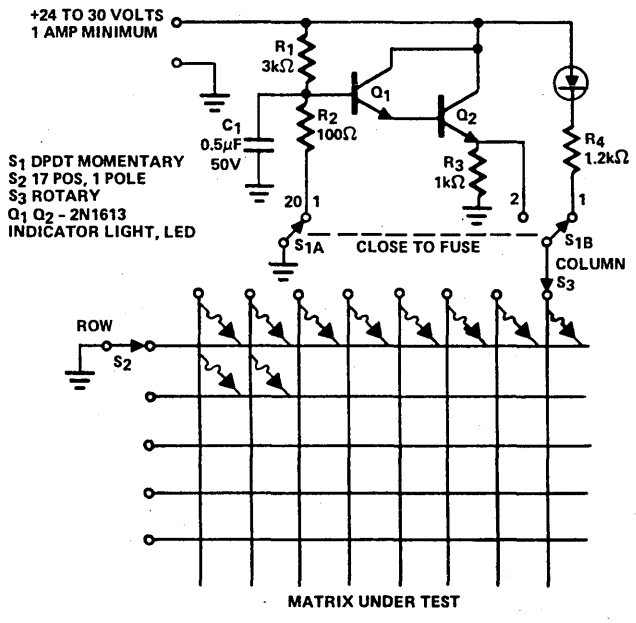
TYPICAL PERFORMANCE CURVES



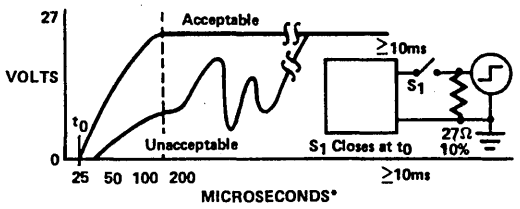
Use a simple supply capable of driving a 27 ohm resistor (carbon) with a clean transition from 0 to 24-30 volts in less than 500μs, for at least 10ms. The diode to be disconnected is selected by setting the row and column switches S2 and S3 respectively as required. When switch S1 is depressed, programming current is provided to column contacts in the matrix. This current opens the fusible link, in series with the selected diode. The peak fusing current required to open a fusible link is approximately 750 milliamperes. As the temperature of the fuse is raised, the aluminum begins to melt. This melting continues until the fuse link separates. The cohesive forces of the melting aluminum retracts the remaining portions of the metal, thereby preventing formation of loose aluminum residues. The melting temperature of aluminum (approximately 650°C) will not affect the passivating layer of silicon dioxide, whose melting temperature is about 1350°C. Test verification is obtained by an indicator lamp or LED placed in series with the column and row switches through the verify contacts of S1 to give electrical indication of the condition of each diode in the matrix before and after fusing.

Caution: Programming is limited to one fuse at a time.

SIMPLE PROGRAMMER



PROGRAMMER TEST CONFIGURATION



* Max T_{RISE} = 500 μsec
Typ T_{RISE} = 200 μsec to 10V Reference

NOTE: The 27 ohm resistor is only used for oscilloscope measurements of the Power Supply Characteristics becaues it represents a typical unprogrammed fuse/diode.

HARRIS

SEMICONDUCTOR DIGITAL PRODUCTS DIVISION

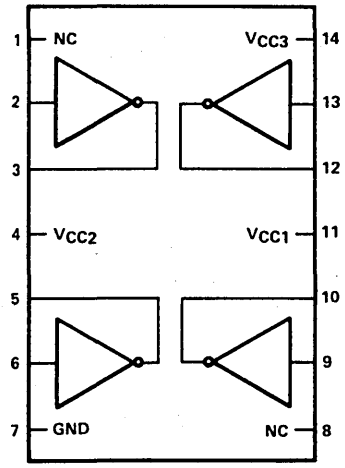
HD-6600

QUAD POWER STROBE

Features

- HIGH DRIVE CURRENT—200mA
- HIGH SPEED 50ns TYPICAL
- TTL COMPATIBLE INPUTS
- DIELECTRIC ISOLATION
- QUAD MONOLITHIC CONSTRUCTION
- POWER SUPPLY FLEXIBILITY
- LOW POWER:
  STANDBY—30mW/CIRCUIT
  ACTIVE—95mW/CIRCUIT

Logic Diagram

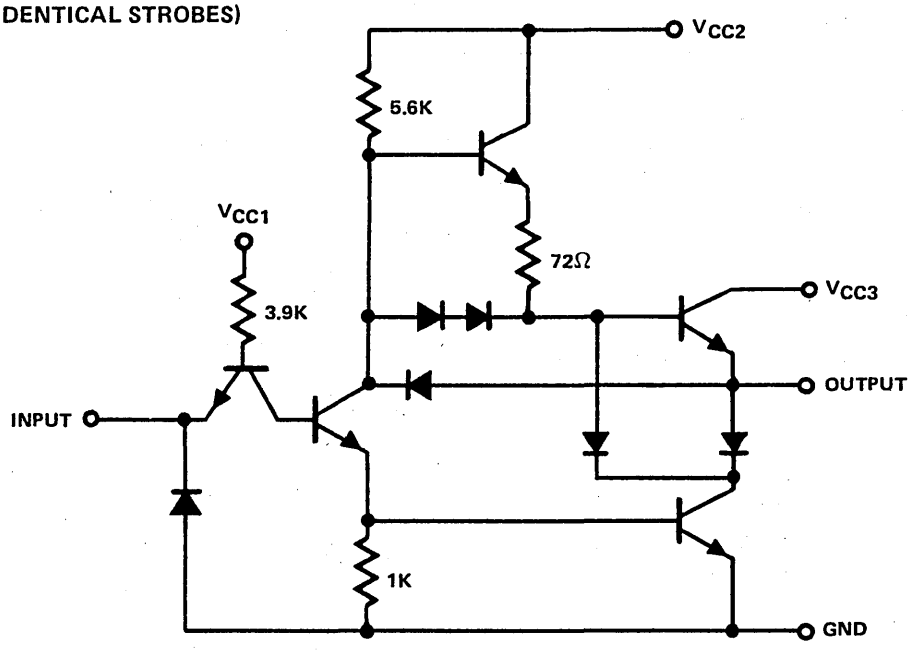


Description

The HD-6600 Quad Power Strobe is constructed with Harris Dielectric Isolation Bipolar Monolithic Process. The design incorporates power supply flexibility with TTL compatible inputs and high current outputs. This circuit is intended for use in power switched PROM arrays.

Circuit Diagram

(ONE OF FOUR IDENTICAL STROBES)



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	V_{CC1}	+8 VDC
	V_{CC2}	+18 VDC
	V_{CC3}	+18 VDC
Input Voltage V_{IN}		-0.5 VDC to +5.5 VDC
Storage Temperature T_{STG}		-65°C to +150°C
Output Current I_L		-200mA
Power Dissipation at 25°C		1000mW
		(Derate 9mW/°C Above 60°C)

RECOMMENDED OPERATING CONDITIONS

Power Supplies:	V_{CC1}	5 VDC ± 10%
	V_{CC2}	12 VDC ± 15%
	V_{CC3}	5 VDC ± 20%

ELECTRICAL CHARACTERISTICS

T_A = -55°C to +125°C HD1-6600-2 V_{CC2} = 12.0 VDC
T_A = 0°C to +75°C HD1-6600-5 V_{CC3} = 5.0 VDC

D.C.

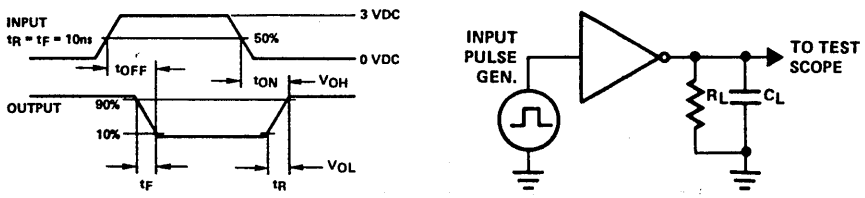
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
I_{IR} I_{IF}	Input Current			60 -1.6	μA mA	V_{IN} = 2.4 VDC V_{IN} = 0.4 VDC V_{CC1} = 5.5 VDC
V_{IH} V_{IL}	Input Threshold Voltage	2.0		 0.8	V V	V_{CC1} = 4.5 VDC
V_{OH}	Output Voltage (Note 1)	4.75	4.85		V	V_{CC1} = 5.0 VDC V_{IN} = 0.4 VDC I_L = -150mA DC
V_{OL}				1.0	V	V_{CC1} = 5.0 VDC I_L = 500μA DC
I_{CC1}	Supply Current (Note 2)		4	6.0	mA	V_{CC1} = 5.5 VDC V_{IN} = 2.4 VDC
I_{CC2}			40	70	mA	V_{CC1} = 5.5 VDC V_{IN} = 0.4 VDC I_L = -150mA DC
I_{CC2}			8	15	mA	V_{CC1} = 5.5 VDC V_{IN} = 2.4 VDC I_L = 0

A.C.

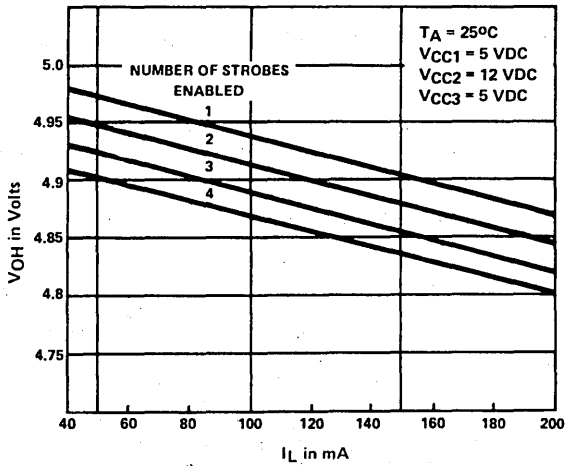
SYMBOL	PARAMETER	TYP.	MAX.	UNITS	CONDITIONS T_A = 25°C
tON	Turn On Delay	50	75	ns	V_{CC1} = 5.0 VDC
tOFF	Turn Off Delay	50	75	ns	V_{CC2} = 12 VDC
					V_{CC3} = 5.0 VDC
tR	Rise Time	40	65	ns	R_L = 33Ω
tF	Fall Time	40	65	ns	C_L = 620 pF

NOTES (1) One strobe enabled. (2) All strobes enabled.

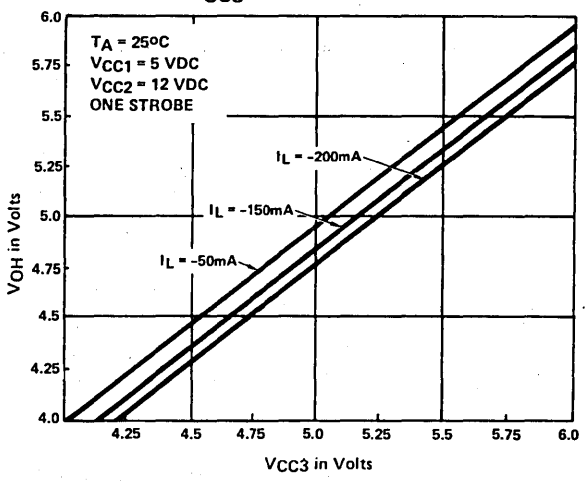
Switching Time Definitions



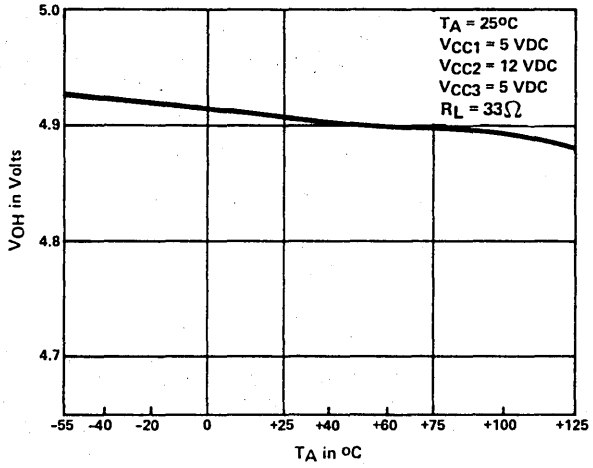
TYPICAL OUTPUT VOLTAGE vs.
LOAD CURRENT AND NUMBER OF STROBES ENABLED



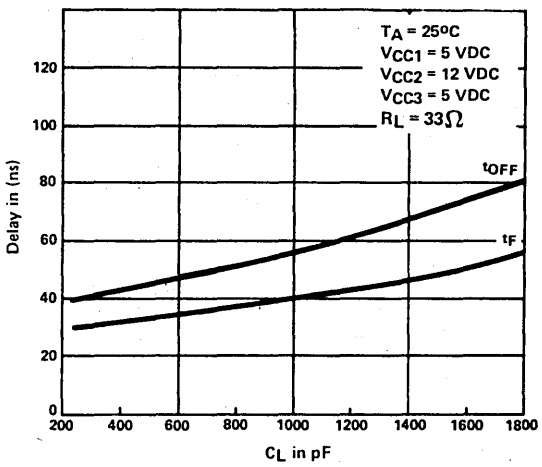
TYPICAL OUTPUT VOLTAGE vs.
V_{CC3} SUPPLY VOLTAGE



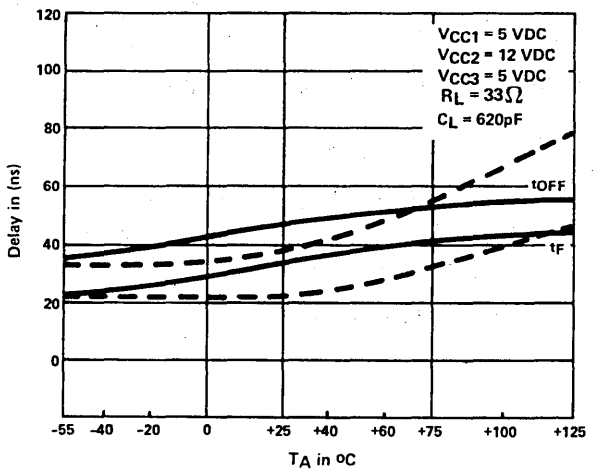
TYPICAL OUTPUT VOLTAGE vs.
AMBIENT TEMPERATURE



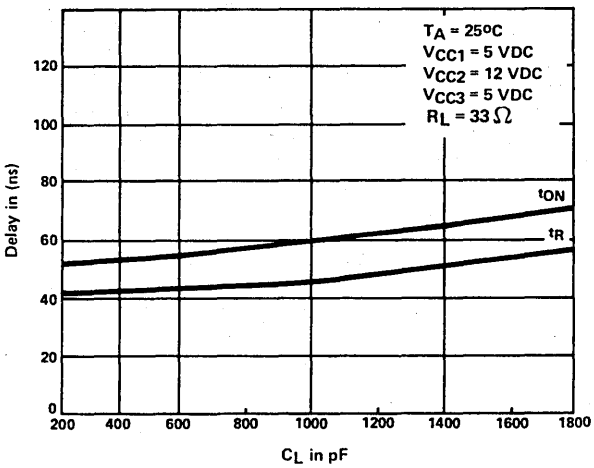
TYPICAL DELAY t_{OFF} AND t_F vs.
LOAD CAPACITANCE



TYPICAL DELAY vs.
AMBIENT TEMPERATURE



TYPICAL DELAY t_{ON} AND t_R vs.
LOAD CAPACITANCE



HARRIS

HPL

THE LOGICAL SOLUTION

INTRODUCTION TO HARRIS PROGRAMMABLE LOGIC.

Introduction

Harris Programmable Logic (HPL) is a family of user configurable logic elements designed to be space and power saving replacements for random logic designs implemented in TTL or LSTTL. HPL products are a natural progression for Harris Semiconductor, already a major PROM supplier with over ten years experience in the field of nichrome fuse programmable devices. The HPL family contains devices which are functional and pinout replacements for existing industry standard devices, and also includes new devices with enhanced architectural features designed for applications which are not served by existing devices.

Family

The HPL family is divided into three architecturally distinct groups, each with its own advantages and areas of application. The three HPL groups are: IFL™, PAL™ and PROM, and are all similar in that they contain two logic arrays. The first array is an AND array which is used to form PRODUCT terms from combinations of feedback and/or input variables. The second array is an OR array which is used to form SUM terms from combinations of product terms generated by the first array. The difference between the three architectural groups results from various combinations of user configurable and fixed arrays.

The PAL type devices have a programmable first array (AND) and a fixed second array (OR). The PROM type devices have this configuration reversed; they have a fixed first array (AND) and a programmable second array (OR).

The IFL architectural group is different again, with both its first (AND) and second (OR) logic arrays being programmable. The various combinations of fixed and programmable arrays are shown graphically in FIG 2 on the following page. No one architectural group is the optimum solution for all designs, and for this reason Harris offers a wide range of devices to suit almost any design requirement.

Programming

All HPL devices, with the exception of the high speed PROM group, program generically on any conventional programmer fitted with the appropriate adaptor. The HPL generic programming method employs a simple programming algorithm which does not require stress-inducing high voltages for individual fuse addressing; instead, program mode fuse addressing is done using TTL logic level signals. By using low voltages during programming, functional yield and in-circuit device reliability are maximized. Another advantage of family wide generic programming is a reduction in the number of programmer adaptors required to program a wide range of devices, and therefore a reduction in the time required for familiarization by the operator. The HPL generic programming philosophy will be used on all future products, helping to ensure non-obsolescence of programming equipment.

Quality

One of the fundamental requirements for high quality is the ability to perform testing on unprogrammed devices as they are manufactured. It was only after the appearance on the market of early Programmable Array Logic devices that both manufacturers and users became aware of the inherent non-testability of those devices. The reasons for this difficulty in testing blank devices stemmed from architectural differences between programmable logic and programmable memory.

In a programmable memory device, such as a PROM, the same circuitry that is used at manufacture to verify the existence of fuses is used during the normal operation of the device. Therefore, if a PROM passes a fuse array verification test, then the logic paths from input to output are automatically tested for functionality. This simplicity of testing is not, however, present in programmable logic devices because the fuse array is verified using totally separate circuitry to that which is used to carry logic signals during normal device operation. Consequently, verification of the fuse array at manufacture does not guarantee correct operation of the logic paths, and because of this, fuse pattern verification by the user does not guarantee correct device functionality. It is apparent that, unlike a PROM, there are two components of FUNCTIONAL YIELD in a Programmable Logic device: FUSING YIELD and LOGIC PATH YIELD. The FUSING YIELD of a programmable logic device is similar to a PROM and is close to 100%. However, the LOGIC PATH YIELD is an unknown quantity and varies from device to device. The components of FUNCTIONAL YIELD for a programmable logic and programmable memory device are shown in FIG 1.

FUNCTIONAL YIELD (PROM) = FUSING YIELD

FUNCTIONAL YIELD (PROGRAMMABLE LOGIC) = FUSING YIELD × LOGIC PATH YIELD

FIG. 1

Responding to customer requirements for high quality devices, Harris developed unique on-chip test circuitry, which is enabled at the time of manufacture to allow complete testing of all logic paths, eliminating the uncertain factor of LOGIC PATH YIELD. One of the benefits of this test circuitry is that the user receives a completely tested device which, providing the fuse array programs correctly, is guaranteed to be functional, eliminating the problem of devices that verify on the programmer but fail in the circuit board. A second benefit of on-chip test circuitry is the ability to perform AC/DC parametric testing at the time of manufacture. This allows Harris to ship devices which are TESTED AND GUARANTEED, and not simply GUARANTEED.

Family Features and Characteristics

- Broad range of device types
- Generic "Low Voltage" programming
- Industry standard and proprietary devices
- Quality "TESTED AND GUARANTEED" devices
- MIL-M-38510 approved NiCr fuse technology
- Slimline packages including "Power Plastic" and LCC

IFL is a trade mark of Signetics Corporation.

PAL is a trade mark of MMI.

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HPL THE LOGICAL SOLUTION

HPL PRODUCT LINE

The HPL product range includes devices from all three of the possible programmable logic architectures, in recognition of the fact that no one architecture is the optimum solution for all designs.

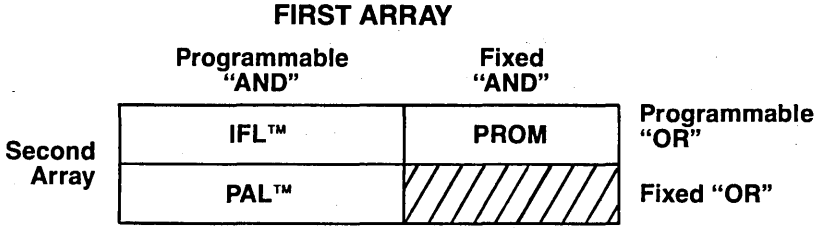


FIG 2

PART NUMBER	GENRE	PINS	FUNCTIONALITY
HPL-77153/82S153	IFL	20	Asynchronous Field Programmable Logic Array with Programmable Output Polarity
*HPL-77161	IFL	24	Asynchronous Field Programmable Gate Array with Programmable Output Polarity
*HPL-77171	IFL	20	Asynchronous Field Programmable Gate Array with Programmable Output Polarity
HPL-77209/16L8	PAL	20	Asynchronous Programmable Array Logic with Active Low Outputs
*HPL-77210/16R4	PAL	20	Sync/Asynchronous Programmable Array Logic with Active Low Outputs
*HPL-77211/16R6	PAL	20	Sync/Asynchronous Programmable Array Logic with Active Low Outputs
*HPL-77212/16R8	PAL	20	Synchronous Programmable Array Logic with Active Low Outputs
HPL-77215/16H8	PAL	20	Asynchronous Programmable Array Logic with Active High Outputs
HPL-77216/16P8	PAL	20	Asynchronous Programmable Array Logic with Programmable Output Polarity
HPL-77317/16LD8	PAL	20	8 Product Terms per Output Version of HPL-77209/16L8
HPL-77318/16HD8	PAL	20	8 Product Terms per Output Version of HPL-77215/16H8
*HPL-77800	PAL	24	8192 Product Terms Per Output PLA with Active High Outputs
*HPL-77801	PAL	24	4096 Product Terms Per Output PLA with Active High Outputs
*HPL-77903	PROM	16	High Speed 32 × 8 PROM designed for Logic Replacement

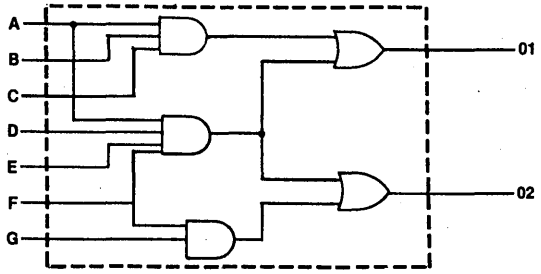
* CONTACT FACTORY OR SALES OFFICE FOR AVAILABILITY.

IFL is a trademark of Signetics
PAL is a trademark of MMI

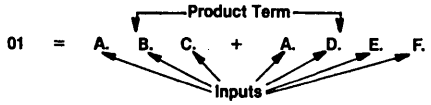
CHOOSING AND USING PROGRAMMABLE LOGIC

Because of the wide range of HPL products available, some method of selecting the right device for a given application is necessary. The method offered below is one way of selecting a device based on input, output and product term usage. This is only one method; other selection criteria, such as speed or power, may require a different selection procedure and will be different from user to user. However, the method shown is a good first approach. Decisions based on other criteria can be made after a device is initially selected.

FOUR CRITERIA ARE IMPORTANT

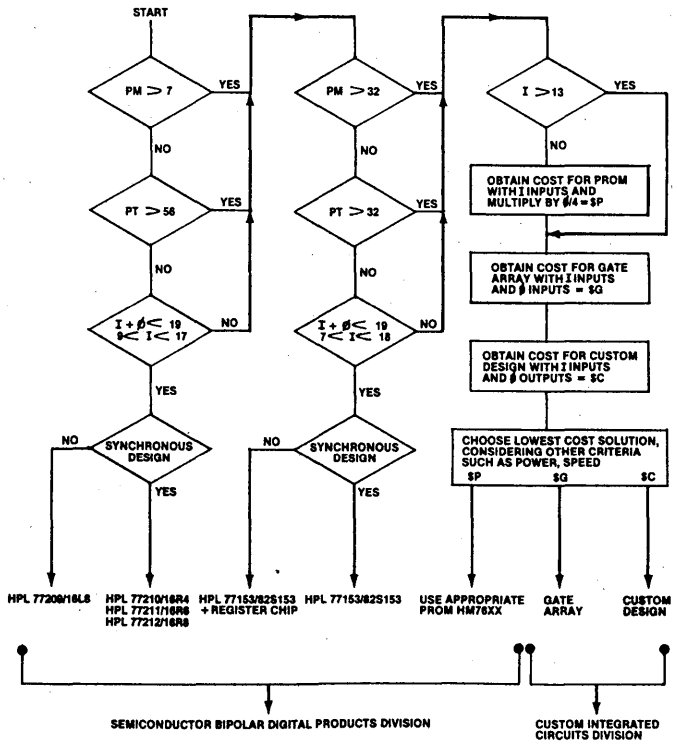


1. DRAW BOX AROUND SECTION OF CIRCUIT TO BE REPLACED, COUNT NUMBER OF INPUTS = I
2. COUNT NUMBER OF OUTPUTS = Ø
3. DERIVE LOGIC EQUATIONS FOR EACH OUTPUT e.g.:



COUNT NUMBER OF PRODUCT TERMS FOR ALL OUTPUTS = PT

4. HOW MANY PRODUCT TERMS ARE USED ON THE OUTPUT WITH MOST PRODUCT TERMS = PM



H.E.L.P. SUPPORT SOFTWARE

No microprocessor, regardless of how fast or powerful, would be very useful without a complete package of support software to assist the designer during program development. For the same reason, Harris recognized that a complete software package would be an essential aid to a designer using programmable logic. The *H*arris *E*nhanced *L*anguage for *P*rogrammable Logic (HELP) is a large and sophisticated software package, running on a mainframe at the Harris computer facility in Melbourne, FL. The HELP software package has many unique and useful features, and is often updated to include new features as they become available. Access to HELP is via the public telephone network and requires that the user has only a simple terminal (glass or paper) and a suitable modem. HELP allows a user to enter logic expressions for his design (initially, only Boolean expressions will be supported, but later truth table and net-list entry formats will be added). HELP also allows a user to edit those expressions, store away expressions using file management utilities, recover expressions, manipulate expressions using a logic minimizer ("single pass" or "run to minimum form"), generate a fuse table from the reduced expressions and generate test vectors for final device testing. In addition, a logic emulator is available for exercising the final equations before programming the actual devices. A flow chart showing a typical sequence of events during the development of an HPL program is shown in FIG 3.

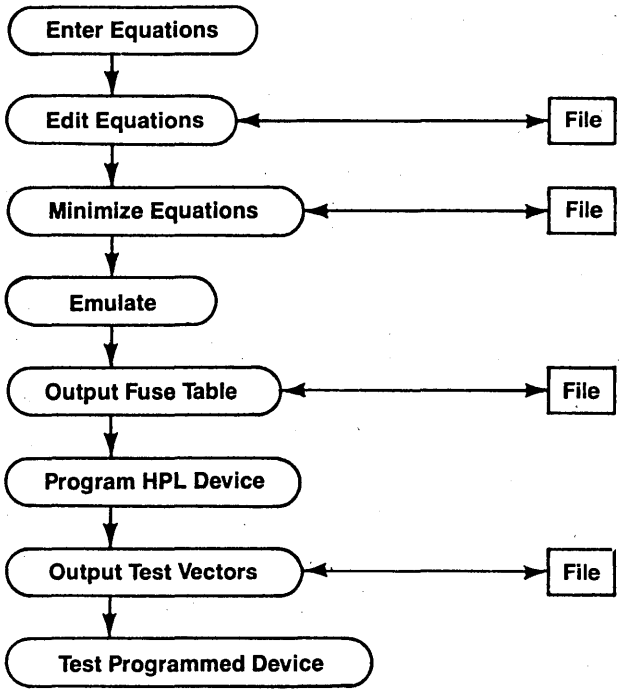


FIG 3

HELP FEATURES

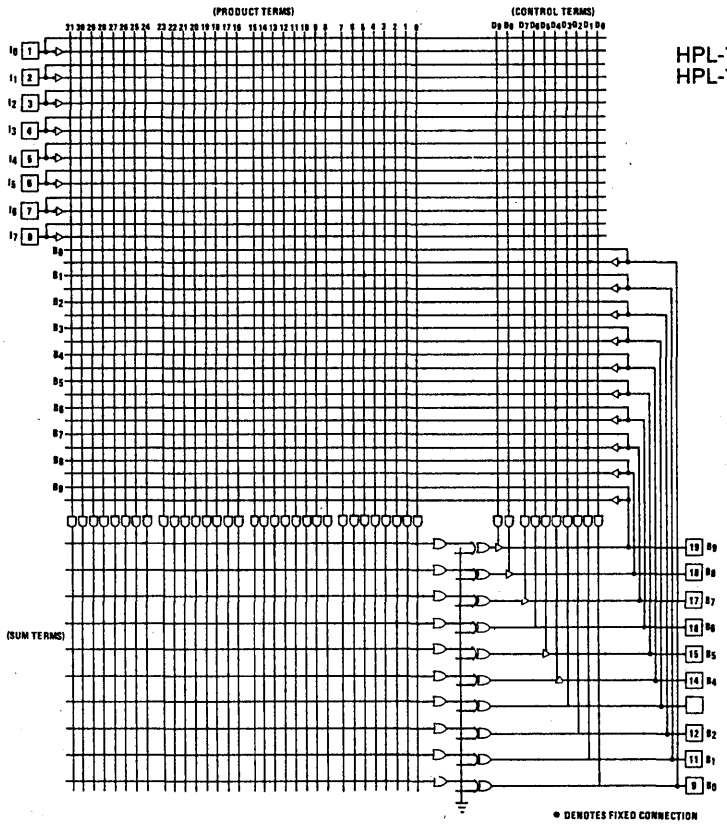
- HELP RUNS ON A HARRIS MAINFRAME IN MELBOURNE.
- ACCESS VIA PUBLIC TELEPHONE NETWORK.
- CUSTOMER NEEDS ONLY LOW COST TERMINAL PLUS MODEM (APPROX. $500).
- COMPUTER "PROMPTING" GIVES FRIENDLY SERVICE.
- MENU DRIVEN TO MINIMIZE FAMILIARIZATION TIME.
- COMPUTER SELECTS "BEST FIT" HPL DEVICE IF NOT SPECIFIED.
- TEST VECTOR GENERATION.
- OUTPUT TO MASK GENERATOR FOR "HARD" PRODUCTS.
- DIRECT INTERFACE WITH PROGRAMMING EQUIPMENT OR VIA FIRM MEDIA.

HARRIS

HPL THE LOGICAL SOLUTION

Functional Diagram

HPL-77153/82S153



D.C. ELECTRICAL CHARACTERISTICS (Operating)

HPL-77215/216/209 −5 (V_{CC} = 5.0V±5%, T_A = 0°C to +75°C)
HPL-77215/216/209 −2/−8 (V_{CC} = 5.0V±10%, T_A = −55°C to +125°C)

SYMBOL	PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS	
I_{IH}	Input Current	"1"	–	+40	A	$V_{IH} = V_{CC}$ MAX	
I_{IL}	Dedicated Input	"0"	–	-100	A	V_{IL} = 0.4V	$V_{CC} = V_{CC}$ MAX
I_{BZH}	Input Current Bidirectional Pin Current	"1"	–	+40	A	$V_{BH} = V_{CC}$ MAX	
I_{BZL}	Hi-Z State	"0"	–	-100	A	V_{BL} = 0.4V	$V_{CC} = V_{CC}$ MAX
V_{IH}	Input Threshold Voltage	"1"	2.0	–	V	$V_{CC} = V_{CC}$ MAX	
V_{IL}		"0"	–	0.8	V	$V_{CC} = V_{CC}$ MIN	
V_{OH}	High-Level Output Voltage		2.4	–	V	$V_{CC} = V_{CC}$ MIN	I_{OH} = -2.0mA
V_{OL}	Low-Level Output Voltage		–	0.5	V	V_{IL} = 0.8V, V_{IH} = 2.0V	I_{OL} = +16mA
V_{CL}	Input Clamp Voltage		–	-1.2	V	I_{IN} = -18mA, V_{CC} = 0V	
I_{OS}	Output Short Circuit Current*	C	-20	-70	mA	V_{CC} = 5.0V, V_{OUT} = 0V	
		M	-15	-85	mA	One output for MAX of One Sec.	
I_{CC}	Power Supply Current	C	–	155	mA	$V_{CC} = V_{CC}$ MAX	
		M	–	165	mA		

C = Commercial (-5) M = Military (-2/-8)

A. C. SWITCHING CHARACTERISTICS (Operating)

SYMBOL			HPL-77153/82S153-5 5V ± 5% 0°C to +75°C		HPL-77153/82S153-2/-8 5V ± 10% -55°C to +125°C		
JEDEC STANDARD	OLD SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
TDVQH1	T_{PD}	Propagation Delay-Input or I/O to Active High Output	–	40	–	55	ns
TDVQL1	T_{PD}	Propagation Delay-Input or I/O to Active Low Output	–	40	–	55	ns
TDVQH2	T_{OE}	Enable Access Time to Active High Output	–	35	–	45	ns
TDVQL2	T_{OE}	Enable Access Time to Active Low Output	–	35	–	45	ns
TDVQZ1	T_{OD}	Disable Access Time from Active High,Output	–	30	–	45	ns
TDVQZ2	T_{OD}	Disable Access Time from Active Low Output	–	30	–	45	ns

NOTE: Maximum test frequency is 5MHz with a 50% duty cycle.

Description

The HPL-77153/82S153 is a programmable logic device designed to be cost effective and space saving replacement for discrete logic designs. This device is a two-level logic element, consisting of 32 product terms (AND) and 10 sum terms (OR) with fusible links for programming I/O polarity and direction.

All product terms can be linked to 8 inputs (I) and 10 bidirectional I/O lines (B) allowing variable I/O configurations using the 10 direction control gates (C), ranging from 17 inputs and 1 output to 8 inputs and 10 outputs.

On chip T/C buffers allow either True (I, B) and/or Complement (I, B) signals to be linked to any of the product terms, the outputs of which may be used as inputs to any or all of the sum terms. The output polarity of the sum terms is individually programmable by means of a fuse-link controlled EX-OR gate to allow implementation of Sum Of Products (SOP) or inverted Sum Of Products (ISOP) expressions.

The HPL-77153/82S153 is field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

Nickel-chromium fuse technology is used on these and all other HARRIS HPL-77XXX programmable logic devices. The HPL-77153/82S153 is available in a 20 pin slimline ceramic DIP with a pinout identical to the 82S153. NOTE: The HPL-77152/82S152 (open collector outputs) can also be made available.

The HPL-77153/82S153 contains unique test circuitry developed by HARRIS which is enabled at the time of manufacture to allow complete AC and DC testing.

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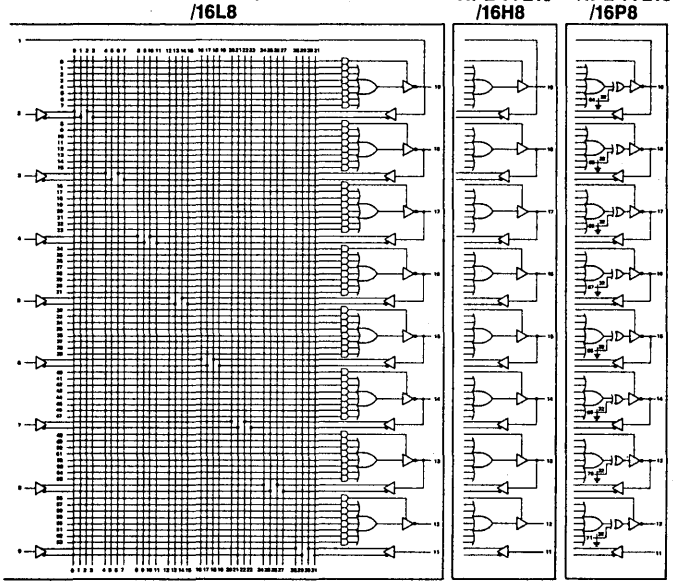
Functional Diagrams

HPL-77209 /16L8 | HPL-77215 /16H8 | HPL-77216 /16P8



D.C. ELECTRICAL CHARACTERISTICS (Operating)

HPL-77215/216/209 -5 (V_{CC} = 5.0V±5%, T_A = 0°C to +75°C)
HPL-77215/216/209 -2/-8 (V_{CC} = 5.0V±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS
I_{IH}	Input Current	"1"	—	+25	µA	V_{IH} Vcc MAX
I_{IL}	Dedicated Input	"0"	—	-100	µA	V_{IL} 0.4 V Vcc Vcc MAX
I_{IZH}	Output Current	"1"	—	+40	µA	V_{IH} Vcc MAX
I_{IZL}	Hi-Z State	"0"	—	-40	µA	V_{IL} 0.4V Vcc Vcc MAX
I_{BZH}	Bidirectional Pin Current	"1"	—	+40	µA	V_{IH} Vcc MAX
I_{BZL}	Hi-Z State	"0"	—	-100	µA	V_{IL} 0.4V Vcc Vcc MAX
V_{IH}	Input Threshold (1)	"1"	2.0	—	V	Vcc Vcc MAX
V_{IL}	Voltage	"0"	—	0.8	V	Vcc Vcc MIN
V_{OH}	High-Level Output Voltage (2)		2.4	—	V	Vcc Vcc MIN; I_{OH} -2.0mA (M), -3.2mA (C)
V_{OL}	Low-Level Output Voltage (2)		—	0.5	V	V_{IL} 0.8V, V_{IH} 2.0V; I_{OL} +16mA (M), +24mA (C) (3)
V_{CL}	Input Clamp Voltage (1)		—	-1.2	V	I_{IN} -18mA, Vcc 0V
I_{OS}	Output Short Circuit Current (2)		-30	-130	mA	Vcc 5.0V, V_{OUT} 0V; One Output for MAX of One Sec.
I_{CC}	Power Supply Current		—	155 (C)	mA	Vcc = Vcc MAX
			—	165 (M)	mA	

C Commercial (-5) M Military (-2, -8)
(1) These specifications apply to both Input (I) and Bidirectional (B) pins
(2) These specifications apply to both Output (F) and Bidirectional (B) pins
(3) One output at a time, otherwise 15mA

A. C. SWITCHING CHARACTERISTICS (Operating)

			HPL-77215-5 HPL-77216-5 HPL-77209-5 5V±5% 0°C to +75°C		HPL-77215-2/-8 HPL-77216-2/-8 HPL-77209-2/-8 5V±10% -55°C to +125°C		
SYMBOL JEDEC STANDARD	SYMBOL OLD SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
TDVOH1	T_{PD}	Propagation Delay - Input or I/O to Active High Output	—	35	—	45	ns
TDVOL1	T_{PD}	Propagation Delay - Input or I/O to Active Low Output	—	35	—	45	ns
TDVOH2	T_{PZX}	Enable Access Time to Active High Output (1)	TDVQZ1	35	TDVQZ1	45	ns
TDVOL2	T_{PZX}	Enable Access Time to Active Low Output (1)	TDVQZ2	35	TDVQZ2	45	ns
TDVQZ1	T_{PXZ}	Disable Access Time from Active High Output	—	30	—	35	ns
TDVQZ2	T_{PXZ}	Disable Access Time from Active Low Output	—	30	—	35	ns

(1) Enable Access Time is guaranteed greater than Disable Access Time to avoid device contention.
NOTE Maximum test frequency is 5MHz with a 50% duty cycle.

Description

The HPL-77215/216/209 are programmable logic devices designed to be cost effective and space saving replacements for discrete logic designs. These devices are two-level logic elements consisting of 7 product terms (AND) summed (OR) together to generate each of the 8 outputs. An eighth product term associated with each output can drive it to a high impedance state allowing 6 (B0-B5) of the 8 outputs to be used as inputs, either permanently or dynamically.

The HPL-77209 is functionally identical to the industry standard 16L8, and implements logic expressions of the Inverted Sum Of Products (ISOP) form.

The HPL-77215 is a similar device to the 16L8 but does not include the associated output inversion, it implements logic expressions of the Sum Of Products (SOP) form.

The HPL-77216 is a more flexible device, it includes 8 EX-OR gates in each output path, controlled by 8 extra fuses, allowing the polarity of each output to be user configured. This device can implement a combination of SOP and ISOP expressions.

The HPL-77215/216/209 are field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

Nickel-chromium fuse technology is used on these and all other HARRIS HPL-77XXX programmable logic devices. The HPL-77215/216/209 are available in 20 pin slimline DIP packages with pinouts identical to the 16L8.

The HPL-77215/216/209 contain unique test circuitry developed by HARRIS which is enabled at the time of manufacture to allow complete AC and DC testing.

HARRIS

SEMICONDUCTOR DIGITAL PRODUCTS DIVISION

HM-6508

1024 x 1 CMOS RAM

Features

- LOW STANDBY POWER — 50 μW MAX
- LOW OPERATING POWER — 20mW/MHz MAX
- FAST ACCESS TIME — 180nsec MAX
- DATA RETENTION VOLTAGE — 2.0 VOLTS MIN
- TTL COMPATIBLE IN/OUT
- HIGH OUTPUT DRIVE – 2 TTL LOADS
- HIGH NOISE IMMUNITY
- ON CHIP ADDRESS REGISTER
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE
- THREE-STATE OUTPUTS
- 16 PIN PACKAGE FOR HIGH DENSITY

Description

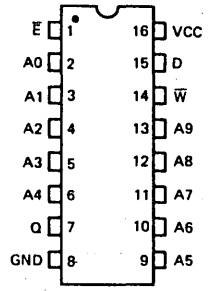
The HM-6508 is a 1024 by 1 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for address allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HM-6508 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

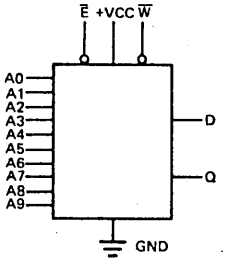
Pinout

TOP VIEW

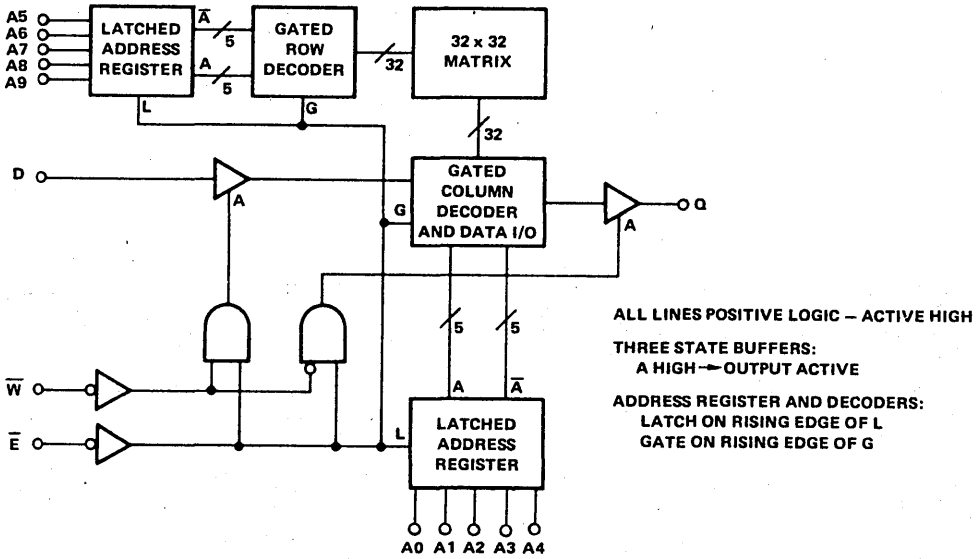


A – Address Input
$\overline{E}$ – Chip Enable
$\overline{W}$ – Write Enable
D – Data Input
Q – Data Output

Logic Symbol



Functional Diagram



ALL LINES POSITIVE LOGIC – ACTIVE HIGH

THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE

ADDRESS REGISTER AND DECODERS:
LATCH ON RISING EDGE OF L
GATE ON RISING EDGE OF G

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage - (VCC -GND)	-0.3V to +8.0V	Operating Supply Voltage -VCC	
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Military (-2)	4.5V to 5.5V
		Industrial (-9)	4.5V to 5.5V
Storage Temperature	-65°C to +150°C	Operating Temperature	
		Military (-2)	-55°C to +125°C
		Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10	0.1	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4	1.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		5	0.01	μA	VCC = 2.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.2	V	IO = 3.2mA
	VOH	Output High Voltage	2.4		4.5	V	IO = -0.4mA
	CI	Input Capacitance ③		6	4	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10	6	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		180	100	ns	④
	TAVQV	Address Access Time		180	90	ns	④
	TELQX	Chip Enable Output Enable Time	20	120	40	ns	④
	TWLQZ	Write Enable Output Disable Time		120	40	ns	④
	TEHQZ	Chip Enable Output Disable Time		120	40	ns	④
	TELEH	Chip Enable Pulse Negative Width	180		100	ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		50	ns	④
	TAVEL	Address Setup Time	0		-10	ns	④
	TELAX	Address Hold Time	40		20	ns	④
	TDVWH	Data Setup Time	80		40	ns	④
	TWHDX	Data Hold Time	0		0	ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	100		50	ns	④
	TELWH	Chip Enable Write Pulse Hold Time	100		50	ns	④
	TWLWH	Write Enable Pulse Width	100		50	ns	④
	TELEL	Read or Write Cycle Time	280		150	ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — CLOAD = 50pF. All timing measurements at 1.5V reference level.

HARRIS

SEMICONDUCTOR DIGITAL PRODUCTS DIVISION

HM-6518

1024 x 1 CMOS RAM

Features

- HM-6100 COMPATIBLE
- LOW STANDBY POWER — 50μW MAX
- LOW OPERATING POWER — 20mW/MHz MAX
- FAST ACCESS TIME — 180nsec MAX
- DATA RETENTION VOLTAGE — 2.0 VOLTS MIN
- TTL COMPATIBLE IN/OUT
- HIGH OUTPUT DRIVE - 2 TTL LOADS
- HIGH NOISE IMMUNITY
- ON CHIP ADDRESS REGISTER
- TWO CHIP SELECTS FOR EASY ARRAY EXPANSION
- THREE STATE OUTPUTS
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE

Description

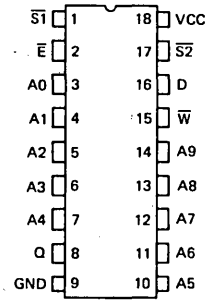
The HM-6518 is a 1024 by 1 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HM-6518 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

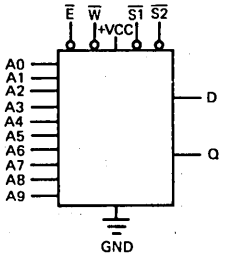
Pinout

TOP VIEW

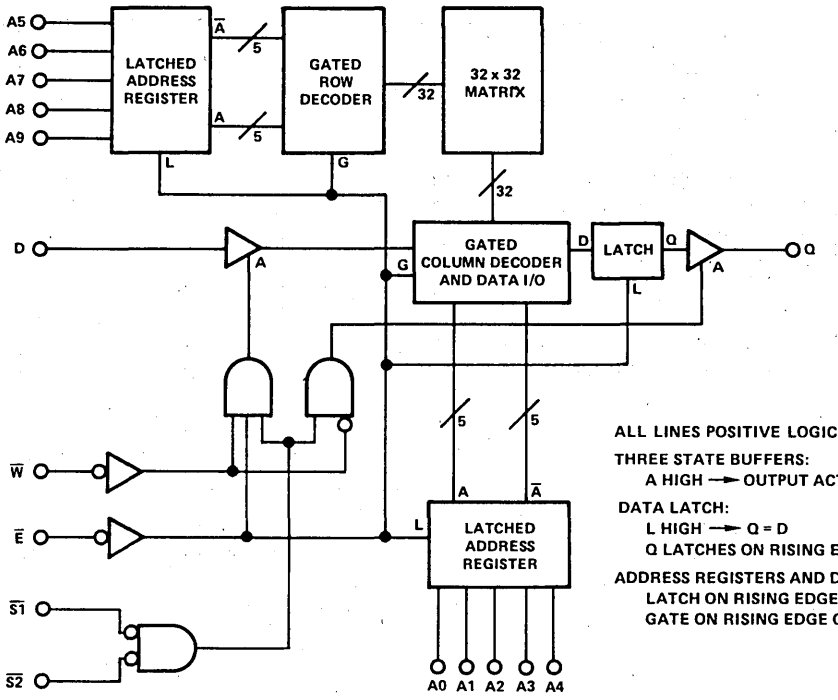


A - ADDRESS INPUT
E - CHIP ENABLE
S - CHIP SELECT
W - WRITE ENABLE
D - DATA INPUT
Q - DATA OUTPUT

Logic Symbol



Functional Diagram



CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage - (VCC -GND)	-0.3V to +8.0V	Operating Supply Voltage -VCC	
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Military (-2)	4.5V to 5.5V
		Industrial (-9)	4.5V to 5.5V
Storage Temperature	-65°C to +150°C	Operating Temperature	
		Military (-2)	-55°C to +125°C
		Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	TEMP. = 25°C ① VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10	0.1	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4	1.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		5	0.01	μA	VCC = 2.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.2	V	IO = 3.2mA
	VOH	Output High Voltage	2.4		4.5	V	IO = -0.4mA
	CI	Input Capacitance ③		6	4	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10	6	pF	VO= VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		180	100	ns	④
	TAVQV	Address Access Time		180	90	ns	④
	TSLQX	Chip Select Output Enable Time	20	120	40	ns	④
	TWLQX	Write Enable Output Disable Time		120	40	ns	④
	TSHQX	Chip Select Output Disable Time		120	40	ns	④
	TELEH	Chip Enable Pulse Negative Width	180		100	ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		50	ns	④
	TAVEL	Address Setup Time	0		-10	ns	④
	TELAX	Address Hold Time	40		20	ns	④
	TDVWH	Data Setup Time	80		30	ns	④
	TWHDX	Data Hold Time	0		0	ns	④
	TWLSH	Chip Select Write Pulse Setup Time	100		50	ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	100		50	ns	④
	TSLWH	Chip Select Write Pulse Hold Time	100		50	ns	④
	TELWH	Chip Enable Write Pulse Hold Time	100		50	ns	④
	TWLWH	Write Enable Pulse Width	100		50	ns	④
	TELEL	Read or Write Cycle Time	280		150	ns	④

NOTES
① All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
② Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
③ Capacitance sampled and guaranteed — not 100% tested.
④ AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — CLOAD = 50pF. All timing measurements at 1.5V reference level.

HARRIS

SEMICONDUCTOR DIGITAL PRODUCTS DIVISION

HM-6551

256 x 4 CMOS RAM

Features

- LOW STANDBY POWER — 50 μW MAX
- LOW OPERATING POWER — 20mW/MHz MAX
- FAST ACCESS TIME — 220nsec MAX
- DATA RETENTION VOLTAGE — 2.0 VOLTS MIN
- TTL COMPATIBLE IN/OUT
- HIGH OUTPUT DRVIE – 1 TTL LOAD
- INTERNAL LATCHED CHIP SELECT
- HIGH NOISE IMMUNITY
- ON CHIP ADDRESS REGISTERS
- LATCHED OUTPUTS
- THREE STATE OUTPUTS
- MILITARY AND INDUSTRIAL TEMPERATURE RANGES

Description

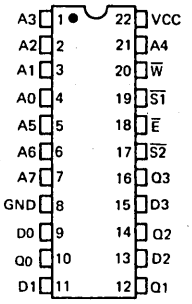
The HM-6551 is a 256 by 4 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for addresses and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HM-6551 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

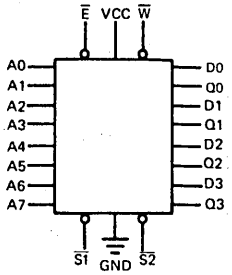
Pinout

TOP VIEW

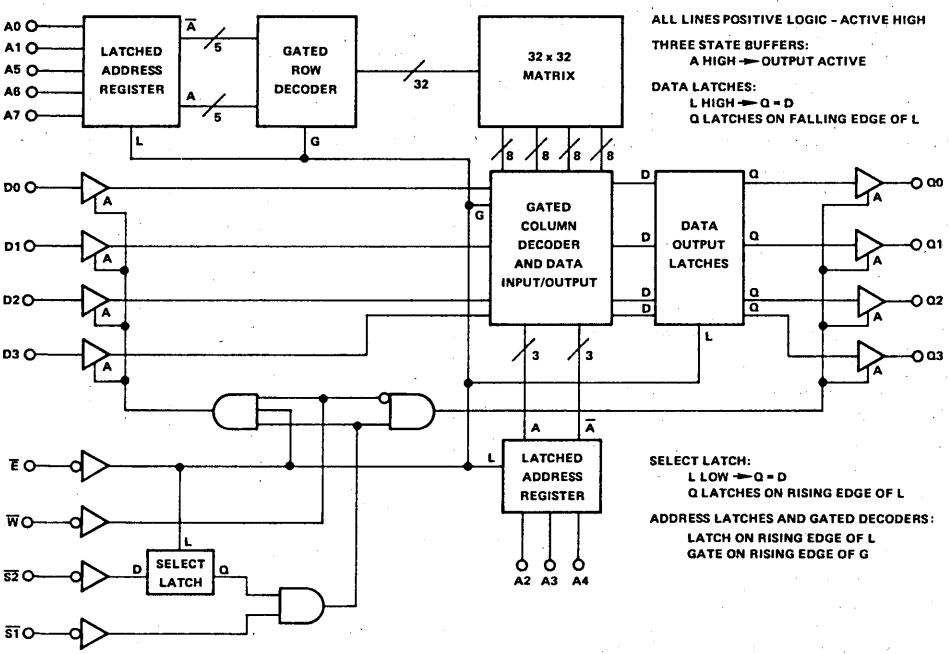


A – Address Input
E – Chip Enable
S – Chip Select
W – Write Enable
D – Data Input
Q – Data Output

Logic Symbol



Functional Diagram



CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage -(VCC -GND)	-0.3V to +8.0V	Operating Supply Voltage -VCC	
		Military (-2)	4.5V to 5.5V
Applied Input or Output Voltage	(GND -0.3V) to (GND +0.3V)	Industrial (-9)	4.5V to 5.5V
		Operating Temperature	
Storage Temperature	-65°C to +150°C	Military (-2)	-55°C to +125°C
		Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	TEMP. = 25°C ① VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10	0.1	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4	1.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10	0.01	μA	VCC = 2.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.2	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		4.5	V	IO = -0.4mA
	CI	Input Capacitance ③		6	4	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10	6	pF	VO= VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		220	120	ns	④
	TAVQV	Address Access Time		220	110	ns	④
	TS1LQX	Chip Select 1 Output Enable Time	20	130	50	ns	④
	TWLQZ	Write Enable Output Disable Time		130	50	ns	④
	TS1HQZ	Chip Select 1 Output Disable Time		130	50	ns	④
	TELEH	Chip Enable Pulse Negative Width	220		120	ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		50	ns	④
	TAVEL	Address Setup Time	0		-10	ns	④
	TS2LEL	Chip Select 2 Setup Time	0		-10	ns	④
	TELAX	Address Hold Time	40		20	ns	④
	TELS2X	Chip Select 2 Hold Time	40		20	ns	④
	TDVWH	Data Setup Time	100		50	ns	④
	TWHDX	Data Hold Time	0		0	ns	④
	TWLS1H	Chip Select 1 Write Pulse Setup Time	120		60	ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	120		60	ns	④
	TS1LWH	Chip Select 1 Write Pulse Hold Time	120		60	ns	④
	TELWH	Chip Enable Write Pulse Hold Time	120		60	ns	④
	TWLWH	Write Enable Pulse Width	120		60	ns	④
	TELEL	Read or Write Cycle Time	320		170	ns	④

NOTES:
① All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
② Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
③ Capacitance sampled and guaranteed — not 100% tested.
④ AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — CLOAD = 50pF. All timing measurements at 1.5V reference level.

HARRIS

SEMICONDUCTOR DIGITAL PRODUCTS DIVISION

HM-6561

256 x 4 CMOS RAM

Features

- HM-6100 COMPATIBLE
- LOW STANDBY POWER — 50μW MAX
- LOW OPERATING POWER — 20 mW/MHz MAX
- FAST ACCESS TIME — 220nsec MAX
- DATA RETENTION VOLTAGE — 2.0 VOLTS MIN
- TTL COMPATIBLE IN/OUT
- HIGH OUTPUT DRIVE – 1 TTL LOAD
- ON CHIP ADDRESS REGISTERS
- COMMON DATA IN/OUT
- THREE STATE OUTPUTS
- EASY MICROPROCESSOR INTERFACING
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE

Description

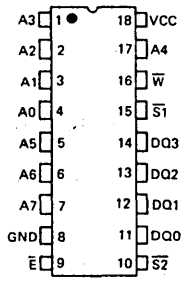
The HM-6561 is a 256 by 4 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays. The data inputs and outputs are multiplexed internally for common I/O bus compatibility.

The HM-6561 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

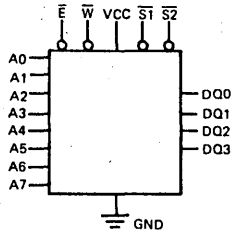
Pinout

TOP VIEW

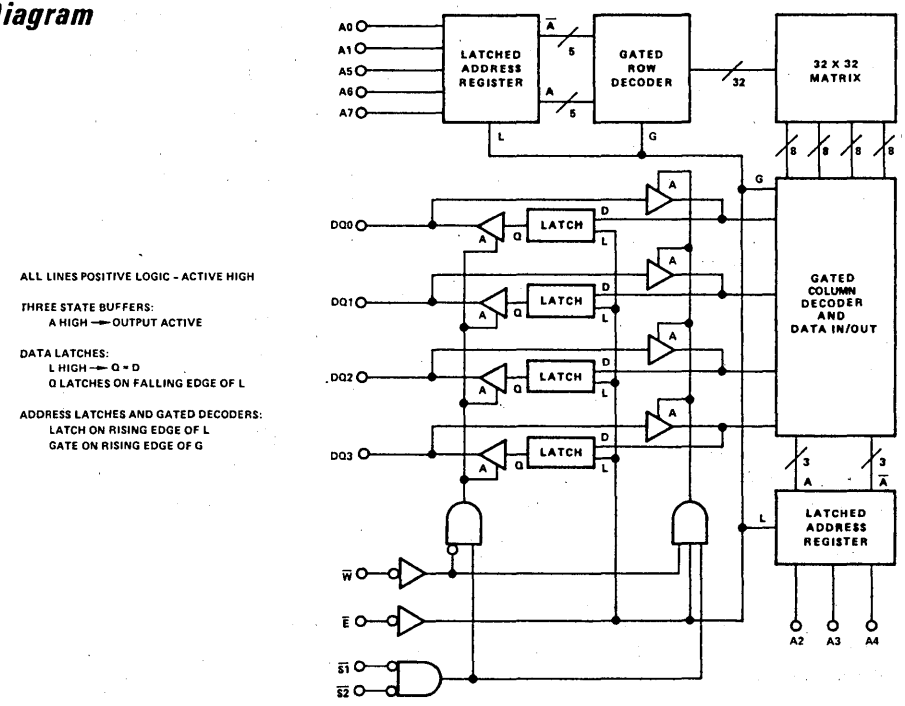


A – Address Input
E – Chip Enable
S – Chip Select
W – Write Enable
DQ – Data In/Out

Logic Symbol



Functional Diagram



CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage - (VCC - GND)	-0.3V to +8.0V	Operating Supply Voltage -VCC	
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Military (-2)	4.5V to 5.5V
		Industrial (-9)	4.5V to 5.5V
Storage Temperature	-65°C to +150°C	Operating Temperature	
		Military (-2)	-55°C to +125°C
		Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	TEMP. = 25°C ① VCC = 5.0V TYPICAL	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10	0.1	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4	1.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10	0.01	μA	VCC = 2.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		1.4	V	
	II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	0.0	μA	GND ≤VIO≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	2.0	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.0	V	
	VOL	Output Low Voltage		0.4	0.2	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		4.5	V	IO = -0.4mA
	CI	Input Capacitance ③		6	4	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance ③		10	6	pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		220	120	ns	④
	TAVQV	Address Access Time		220	110	ns	④
	TSLQX	Chip Select Output Enable Time	20	120	50	ns	④
	TWLQZ	Write Enable Output Disable Time		120	50	ns	④
	TSHQZ	Chip Select Output Disable Time		120	50	ns	④
	TELEH	Chip Enable Pulse Negative Width	220		120	ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		50	ns	④
	TAVEL	Address Setup Time	0		-10	ns	④
	TELAX	Address Hold Time	40		20	ns	④
	TDVWH	Data Setup Time	100		50	ns	④
	TWHDX	Data Hold Time	0		0	ns	④
	TWLDV	Write Data Delay Time	120		50	ns	④
	TWLSH	Chip Select Write Pulse Setup Time	120		60	ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	120		60	ns	④
	TSLWH	Chip Select Write Pulse Hold Time	120		60	ns	④
	TELWH	Chip Enable Write Pulse Hold Time	120		60	ns	④
	TWLWH	Write Enable Pulse Width	120		60	ns	④
	TWLSL	Early Output High Z Time	0		-10	ns	④
	TSHWH	Late Output High Z Time	0		-10	ns	④
	TELEL	Read or Write Cycle Time	320		170	ns	④

NOTES:
① All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
② Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
③ Capacitance sampled and guaranteed — not 100% tested.
④ AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — CLOAD = 50pF. All timing measurements at 1.5V reference level.

HARRIS

HM-6504

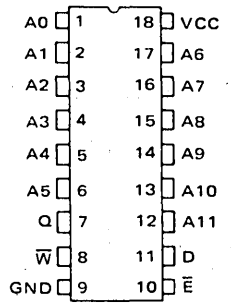
4096 x 1 CMOS RAM

Features

- LOW POWER STANDBY
- LOW POWER OPERATION — 125μW MAX.
- EXTREMELY LOW SPEED POWER PRODUCT — 35mW/MHz MAX.
- DATA RETENTION
- TTL COMPATIBLE INPUT/OUTPUT — @ 2.0V MIN.
- THREE-STATE OUTPUT
- STANDARD JEDC PINOUT
- FAST ACCESS TIME
- MILITARY TEMPERATURE RANGE — 120/200nsec MAX.
- INDUSTRIAL TEMPERATURE RANGE
- 18 PIN PACKAGE FOR HIGH DENSITY
- ON CHIP ADDRESS REGISTER
- GATE INPUTS-NO PULL UP OR PULL DOWN RESISTORS REQUIRED

Pinout

TOP VIEW



Description

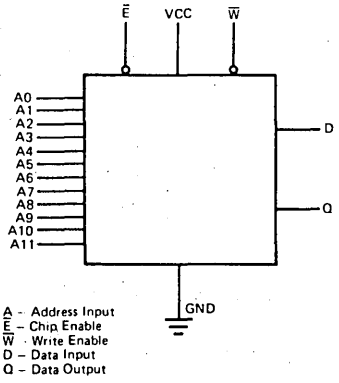
The HM-6504 is a 4096 x 1 static CMOS RAM fabricated using self aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

On chip latches are provided for addresses, data input and data output allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance for use in expanded memory arrays.

The HM-6504 is a fully static RAM and may be maintained in any state for an indefinite period of time.

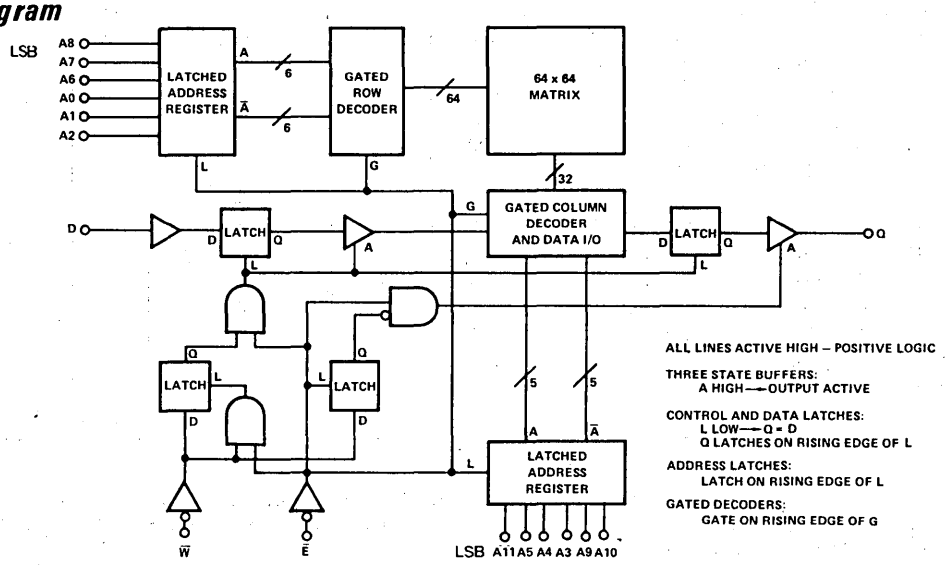
Data retention supply voltage and supply current are guaranteed over temperature.

Logic Symbol



A - Address Input
Ē - Chip Enable
W̄ - Write Enable
D - Data Input
Q - Data Output

Functional Diagram



CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

ABSOLUTE MAXIMUM RATINGS *		OPERATING RANGE	
Supply Voltage – (VCC -GND)	-0.3V to +8.0V	Operating Supply Voltage Military (-2)	4.5V to 5.5V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Operating Temperature Military (-2)	-55°C to +125°C
Storage Temperature	-65°C to +150°C		

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS PRELIMINARY

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP = 25°C (1) VCC = 5.0V TYP	TEMP = 25°C (1) VCC = 5.0V MAX (5)	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		25		3.0	µA	IO = 0 $\overline{E}$ = VCC –0.3V
	ICCOP	Operating Supply Current (2)		7	5		mA	$\overline{E}$ = 1MHz, IO = 0 VI = GND
	ICCDR	Data Retention Supply Current		15		2.0	µA	VCC = 2.0V, IO = 0 $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		1.4		V	
	II	Input Leakage Current	-1.0	+1.0	0.0		µA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0		µA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	1.8		V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.2		V	
	VOL	Output Low Voltage		0.4	0.25		V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0		V	IO = -1.0mA
	CI	Input Capacitance (3)		8.0	5.0		pF	f = 1MHz VI = VCC or GND
	CO	Output Capacitance (3)		10.0	6.0		pF	f = 1MHz VO = VCC or GND
A.C.	TELQV	Chip Enable Access Time		120			ns	(4)
	TAVQV	Address Access Time		120			ns	(4)
	TELQX	Chip Enable Output Enable Time	10				ns	(4)
	TEHQZ	Chip Enable Output Disable Time		50			ns	(4)
	TELEH	Chip Enable Pulse Negative Width	120				ns	(4)
	TEHEL	Chip Enable Pulse Positive Width	50				ns	(4)
	TAVEL	Address Setup Time	0				ns	(4)
	TELAX	Address Hold Time	40				ns	(4)
	TWLWH	Write Enable Pulse Width	20				ns	(4)
	TWLEH	Write Enable Pulse Setup Time	70				ns	(4)
	TWLEL	Early Write Pulse Setup Time	0				ns	(4)
	TWHEL	Write Enable Read Mode Setup Time	0				ns	(4)
	TELWH	Early Write Pulse Hold Time	40				ns	(4)
	TDVWL	Data Setup Time	0				ns	(4)
	TDVEL	Early Write Data Setup Time	0				ns	(4)
	TWLDX	Data Hold Time	25				ns	(4)
	TELDX	Early Write Data Hold Time	25				ns	(4)
	TQVWL	Data Valid to Write Time	0				ns	(4)
	TELEL	Read or Write Cycle Time	170				ns	(4)

NOTES:
(1) All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed unless specified.
(2) Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
(3) Capacitance sampled and guaranteed – not 100% tested.
(4) AC Test Conditions: Inputs – TRISE = TFALL = 5 nsec; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.
(5) This value is guaranteed and tested at 25°C.

ABSOLUTE MAXIMUM RATINGS *		OPERATING RANGE	
Supply Voltage – (VCC -GND)	-0.3V to +8.0V	Operating Supply Voltage Military (-2)	4.5V to 5.5V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Operating Temperature Military (-2)	-55°C to +125°C
Storage Temperature	-65°C to +150°C		

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP = 25°C (1) VCC = 5.0V TYP	TEMP = 25°C (1) VCC = 5.0V MAX (5)	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		50		5.0	μA	IO = 0 $\overline{E}$ = VCC –0.3V
	ICCOP	Operating Supply Current (2)		7	5		mA	$\overline{E}$ = 1MHz, IO = 0 VI = GND
	ICCDR	Data Retention Supply Current		25		3.0	μA	VCC = 2.0V, IO = 0 $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		1.4		V	
	II	Input Leakage Current	-1.0	+1.0	0.0		μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0		μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	1.8		V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.2		V	
	VOL	Output Low Voltage		0.4	0.25		V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0		V	IO = -1.0mA
	CI	Input Capacitance (3)		8.0	5.0		pF	f = 1MHz VI = VCC or GND
	CO	Output Capacitance (3)		10.0	6.0		pF	f = 1MHz VO = VCC or GND
A.C.	TELQV	Chip Enable Access Time		200			ns	(4)
	TAVQV	Address Access Time		220			ns	(4)
	TELQX	Chip Enable Output Enable Time	20				ns	(4)
	TEHQZ	Chip Enable Output Disable Time		80			ns	(4)
	TELEH	Chip Enable Pulse Negative Width	200				ns	(4)
	TEHEL	Chip Enable Pulse Positive Width	90				ns	(4)
	TAVEL	Address Setup Time	20				ns	(4)
	TELAX	Address Hold Time	50				ns	(4)
	TWLWH	Write Enable Pulse Width	60				ns	(4)
	TWLEH	Write Enable Pulse Setup Time	150				ns	(4)
	TWLEL	Early Write Pulse Setup Time	0				ns	(4)
	TWHEL	Write Enable Read Mode Setup Time	0				ns	(4)
	TELWH	Early Write Pulse Hold Time	60				ns	(4)
	TDVWL	Data Setup Time	0				ns	(4)
	TDVEL	Early Write Data Setup Time	0				ns	(4)
	TWLDX	Data Hold Time	60				ns	(4)
	TELDX	Early Write Data Hold Time	60				ns	(4)
	TQVWL	Data Valid to Write Time	0				ns	(4)
	TELEL	Read or Write Cycle Time	290				ns	(4)

NOTES:
(1) All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed unless specified.
(2) Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
(3) Capacitance sampled and guaranteed – not 100% tested.
(4) AC Test Conditions: Inputs – TRISE = TFALL = 10ns; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.
(5) This value is guaranteed and tested at 25°C.

ABSOLUTE MAXIMUM RATINGS *

Supply Voltage – (VCC -GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage	
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Industrial (-9)	-40°C to +85°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS PRELIMINARY

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP = 25°C (1) VCC = 5.0V TYP	TEMP = 25°C (1) VCC = 5.0V MAX (5)	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		25		3.0	μA	$\overline{IO} = 0$ $\overline{E} = VCC - 0.3V$
	ICCOP	Operating Supply Current (2)		7	5		mA	$\overline{E}$ = 1MHz, IO = 0 VI = GND
	ICCDR	Data Retention Supply Current		15		2.0	μA	VCC = 2.0V, IO = 0 $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		1.4		V	
	II	Input Leakage Current	-1.0	+1.0	0.0		μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0		μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	1.8		V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.2		V	
	VOL	Output Low Voltage		0.4	0.25		V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0		V	IO = -1.0mA
	CI	Input Capacitance (3)		8.0	5.0		pF	f = 1MHz VI = VCC or GND
	CO	Output Capacitance (3)		10.0	6.0		pF	f = 1MHz VO = VCC or GND
A.C.	TELQV	Chip Enable Access Time		120			ns	(4)
	TAVQV	Address Access Time		120			ns	(4)
	TELQX	Chip Enable Output Enable Time	10				ns	(4)
	TEHQZ	Chip Enable Output Disable Time		50			ns	(4)
	TELEH	Chip Enable Pulse Negative Width	120				ns	(4)
	TEHEL	Chip Enable Pulse Positive Width	50				ns	(4)
	TAVEL	Address Setup Time	0				ns	(4)
	TELAX	Address Hold Time	40				ns	(4)
	TWLWH	Write Enable Pulse Width	20				ns	(4)
	TWLEH	Write Enable Pulse Setup Time	70				ns	(4)
	TWLEL	Early Write Pulse Setup Time	0				ns	(4)
	TWHEL	Write Enable Read Mode Setup Time	0				ns	(4)
	TELWH	Early Write Pulse Hold Time	40				ns	(4)
	TDVWL	Data Setup Time	0				ns	(4)
	TDVEL	Early Write Data Setup Time	0				ns	(4)
	TWLDX	Data Hold Time	25				ns	(4)
	TELDX	Early Write Data Hold Time	25				ns	(4)
	TQVWL	Data Valid to Write Time	0				ns	(4)
	TELEL	Read or Write Cycle Time	170				ns	(4)

NOTES:
(1) All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed unless specified.
(2) Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
(3) Capacitance sampled and guaranteed – not 100% tested.
(4) AC Test Conditions: Inputs – TRISE = TFALL = 5 nsec; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.
(5) This value is guaranteed and tested at 25°C.

ABSOLUTE MAXIMUM RATINGS *		OPERATING RANGE	
Supply Voltage – (VCC -GND)	-0.3V to +8.0V	Operating Supply Voltage Industrial (-9)	4.5V to 5.5V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)	Operating Temperature Industrial (-9)	-40°C to +85°C
Storage Temperature	-65°C to +150°C		

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP = 25°C ① VCC = 5.0V TYP	TEMP = 25°C ① VCC = 5.0V MAX ⑤	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		25		3.0	µA	IO = 0 $\overline{E}$ = VCC –0.3V
	ICCOP	Operating Supply Current ②		7	5		mA	$\overline{E}$ = 1MHz, IO = 0 VI = GND
	ICCDR	Data Retention Supply Current		15		2.0	µA	VCC = 2.0V, IO = 0 $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		1.4		V	
	II	Input Leakage Current	-1.0	+1.0	0.0		µA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	0.0		µA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	1.8		V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.2		V	
	VOL	Output Low Voltage		0.4	0.25		V	IO = 1.6mA
	VOH	Output High Voltage	2.4		4.0		V	IO = -0.4mA
	CI	Input Capacitance ③		8.0	5.0		pF	f = 1MHz VI = VCC or GND
	CO	Output Capacitance ③		10.0	6.0		pF	f = 1MHz VO = VCC or GND
A.C.	TELQV	Chip Enable Access Time		200			ns	④
	TAVQV	Address Access Time		220			ns	④
	TELQX	Chip Enable Output Enable Time	20				ns	④
	TEHQZ	Chip Enable Output Disable Time		80			ns	④
	TELEH	Chip Enable Pulse Negative Width	200				ns	④
	TEHEL	Chip Enable Pulse Positive Width	90				ns	④
	TAVEL	Address Setup Time	20				ns	④
	TELAX	Address Hold Time	50				ns	④
	TWLWH	Write Enable Pulse Width	60				ns	④
	TWLEH	Write Enable Pulse Setup Time	150				ns	④
	TWLEL	Early Write Pulse Setup Time	0				ns	④
	TWHEL	Write Enable Read Setup Time	0				ns	④
	TELWH	Early Write Pulse Hold Time	60				ns	④
	TDVWL	Data Setup Time	0				ns	④
	TDVEL	Early Write Data Setup Time	0				ns	④
	TWLDX	Data Hold Time	60				ns	④
	TELDX	Early Write Data Hold Time	60				ns	④
	TQVWL	Data Valid to Write Time	0				ns	④
	TELEL	Read or Write Cycle Time	290				ns	④

NOTES:
① All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed unless specified.
② Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
③ Capacitance sampled and guaranteed – not 100% tested.
④ AC Test Conditions: Inputs – TRISE = TFALL = 10nsec; Outputs – CLOAD = 50pF. All timing measurements at 1.5V reference level.
⑤ This value is guaranteed and tested at 25°C.

HARRIS

HM-6514

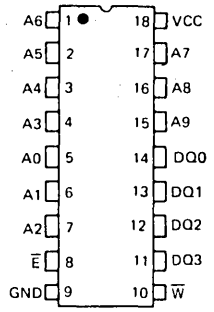
1024 x 4 CMOS RAM

Features

- LOW POWER STANDBY — 125µW MAX.
- LOW POWER OPERATION — 35mW/MHz MAX.
- DATA RETENTION — @ 2.0V MIN.
- TTL COMPATIBLE INPUT/OUTPUT
- COMMON DATA IN/OUT
- THREE-STATE OUTPUTS
- STANDARD JEDEC PINOUT
- FAST ACCESS TIME — 120 /200nsec MAX.
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE
- 18 PIN PACKAGE FOR HIGH DENSITY
- ON-CHIP ADDRESS REGISTER
- GATED INPUTS—NO PULL UP OR PULL DOWN RESISTORS REQUIRED

Pinout

TOP VIEW



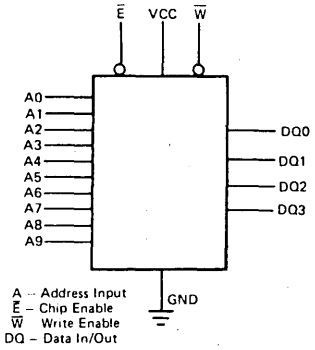
Description

The HM-6514 is a 1024 x 4 static CMOS RAM fabricated using self aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

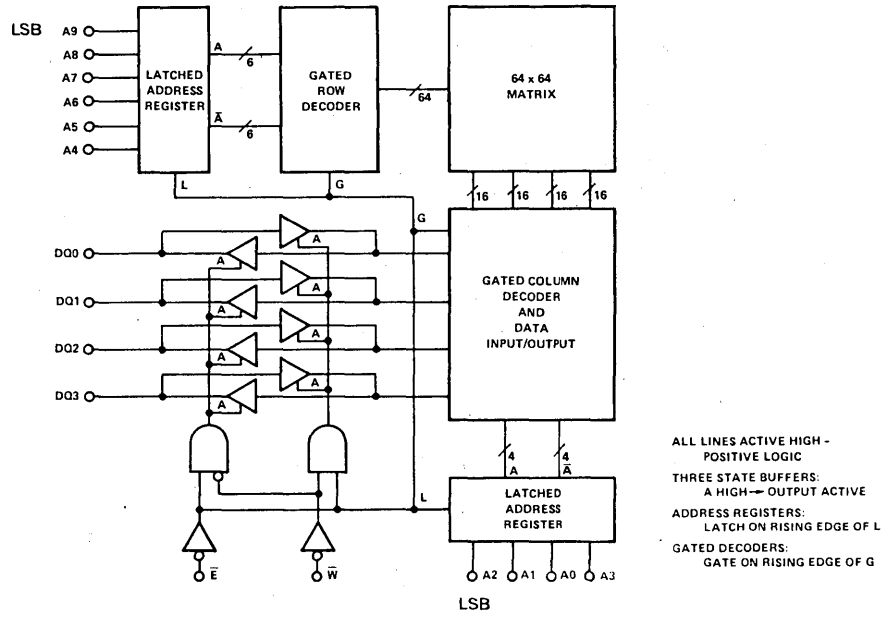
On-chip latches are provided for the addresses allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance state for use in expanded memory systems.

The HM-6514 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

Logic Symbol



Functional Diagram



ABSOLUTE MAXIMUM RATINGS *

Supply Voltage - (VCC - GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage Military (-2)	4.5V to 5.5V
Operating Temperature Military (-2)	-55°C to +125°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS — PRELIMINARY

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP = 25°C (1) VCC = 5.0V TYP	TEMP = 25°C (1) VCC = 5.0V MAX (5)	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		50		5.0	µA	IO = 0 $\overline{E}$ = VCC –0.3V
	ICCOP	Operating Supply Current (2)		7	5		mA	$\overline{E}$ = 1MHz, IO = 0 VI = GND
	ICCDR	Data Retention Supply Current		25		3.0	µA	VCC = 2.0V, IO = 0 $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		1.4		V	
	II	Input Leakage Current	-1.0	+1.0	0.0		µA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	0.0		µA	GND ≤ VIO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	1.8		V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.2		V	
	VOL	Output Low Voltage		0.4	0.25		V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0		V	IO = -1.0mA
	CI	Input Capacitance (3)		8.0	5.0		pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance (3)		10.0	6.0		pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		120			ns	(4)
	TAVQV	Address Access Time		120			ns	(4)
	TELQX	Chip Enable Output Enable Time	10				ns	(4)
	TWLQZ	Write Enable Output Disable Time		50			ns	(4)
	TEHQZ	Chip Enable Output Disable Time		50			ns	(4)
	TELEH	Chip Enable Pulse Negative Width	120				ns	(4)
	TEHEL	Chip Enable Pulse Positive Width	50				ns	(4)
	TAVEL	Address Setup Time	0				ns	(4)
	TELAX	Address Hold Time	40				ns	(4)
	TWLWH	Write Enable Pulse Width	120				ns	(4)
	TWLEH	Write Enable Pulse Setup Time	120				ns	(4)
	TELWH	Write Enable Pulse Hold Time	120				ns	(4)
	TDVWH	Data Setup Time	50				ns	(4)
	TWHDZ	Data Hold Time	0				ns	(4)
	TWLDV	Write Data Delay Time	70				ns	(4)
	TWLEL	Early Output High-Z Time	0				ns	(4)
	TEHWH	Late Output High-Z Time	0				ns	(4)
	TELEL	Read or Write Cycle Time	170				ns	(4)

NOTES:
(1) All devices tested at worst case limits. Room Temp., 5V data provided for information — not guaranteed unless specified.
(2) Operating Supply Current (ICCOP) is proportional to Operating Frequency. Ex: Typical ICCOP = 5mA/MHz.
(3) Capacitance sampled and guaranteed — not 100% tested.
(4) AC test conditions: Inputs — TRISE = TFALL = 5ns; Output — CLOAD = 50pF. All timing measured at 1.5V reference level.
(5) This typical value is guaranteed and tested at 25°C.

ABSOLUTE MAXIMUM RATINGS *		OPERATING RANGE	
Supply Voltage - (VCC - GND)	-0.3V to +8.0V	Operating Supply Voltage Industrial (-9)	4.5V to 5.5V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)		
Storage Temperature	-65°C to +150°C	Operating Temperature Industrial (-9)	-40°C to +85°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS — PRELIMINARY

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP = 25°C (1) VCC = 5.0V TYP	TEMP = 25°C (1) VCC = 5.0V MAX (5)	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		25		3.0	µA	IO = 0 $\overline{E}$ = VCC –0.3V
	ICCOP	Operating Supply Current (2)		7	5		mA	$\overline{E}$ = 1MHz, IO = 0 VI = GND
	ICCDR	Data Retention Supply Current		15		2.0	µA	VCC = 2.0V, IO = 0 $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		1.4		V	
	II	Input Leakage Current	-1.0	+1.0	0.0		µA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	0.0		µA	GND ≤ VIO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	1.8		V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.2		V	
	VOL	Output Low Voltage		0.4	0.25		V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0		V	IO = -1.0mA
	CI	Input Capacitance (3)		8.0	5.0		pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance (3)		10.0	6.0		pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		120			ns	(4)
	TAVQV	Address Access Time		120			ns	(4)
	TELQX	Chip Enable Output Enable Time	10				ns	(4)
	TWLQZ	Write Enable Output Disable Time		50			ns	(4)
	TEHQZ	Chip Enable Output Disable Time		50			ns	(4)
	TELEH	Chip Enable Pulse Negative Width	120				ns	(4)
	TEHEL	Chip Enable Pulse Positive Width	50				ns	(4)
	TAVEL	Address Setup Time	0				ns	(4)
	TELAX	Address Hold Time	40				ns	(4)
	TWLWH	Write Enable Pulse Width	120				ns	(4)
	TWLEH	Write Enable Pulse Setup Time	120				ns	(4)
	TELWH	Write Enable Pulse Hold Time	120				ns	(4)
	TDVWH	Data Setup Time	50				ns	(4)
	TWHDZ	Data Hold Time	0				ns	(4)
	TWLDV	Write Data Delay Time	70				ns	(4)
	TWLEL	Early Output High-Z Time	0				ns	(4)
	TEHWH	Late Output High-Z Time	0				ns	(4)
	TELEL	Read or Write Cycle Time	170				ns	(4)

NOTES:
(1) All devices tested at worst case limits. Room Temp., 5V data provided for information – not guaranteed unless specified.
(2) Operating Supply Current (ICCOP) is proportional to Operating Frequency. Ex: Typical ICCOP = 5mA/MHz.
(3) Capacitance sampled and guaranteed – not 100% tested.
(4) AC test conditions: Inputs – TRISE = TFALL = 5ns; Output – CLOAD = 50pF. All timing measured at 1.5V reference level.
(5) This value is guaranteed and tested at 25°C.

ABSOLUTE MAXIMUM RATINGS *		OPERATING RANGE	
Supply Voltage – (VCC -GND)	-0.3V to +8.0V	Operating Supply Voltage Military (-2)	4.5V to 5.5V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)		
Storage Temperature	-65°C to +150°C	Operating Temperature Military (-2)	-55°C to +125°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP = 25°C (1) VCC = 5.0V TYP	TEMP = 25°C (1) VCC = 5.0V MAX (5)	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		50		5.0	μA	IO = 0 $\overline{E}$ = VCC –0.3V
	ICCOP	Operating Supply Current (2)		7	5		mA	$\overline{E}$ = 1MHz, IO = 0 VI = GND
	ICCDR	Data Retention Supply Current		25		3.0	μA	VCC = 2.0V, IO = 0 $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		1.4		V	
	II	Input Leakage Current	-1.0	+1.0	0.0		μA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	0.0		μA	GND ≤ VIO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	1.8		V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.2		V	
	VOL	Output Low Voltage		0.4	0.25		V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0		V	IO = -1.0mA
	CI	Input Capacitance (3)		8.0	5.0		pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance (3)		10.0	6.0		pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		200			ns	(4)
	TAVQV	Address Access Time		220			ns	(4)
	TELQX	Chip Enable Output Enable Time	20				ns	(4)
	TWLQZ	Write Enable Output Disable Time		80			ns	(4)
	TEHQZ	Chip Enable Output Disable Time		80			ns	(4)
	TELEH	Chip Enable Pulse Negative Width	200				ns	(4)
	TEHEL	Chip Enable Pulse Positive Width	90				ns	(4)
	TAVEL	Address Setup Time	20				ns	(4)
	TELAX	Address Hold Time	50				ns	(4)
	TWLWH	Write Enable Pulse Width	200				ns	(4)
	TWLEH	Write Enable Pulse Setup Time	200				ns	(4)
	TELWH	Write Enable Pulse Hold Time	200				ns	(4)
	TDVWH	Data Setup Time	120				ns	(4)
	TWHDZ	Data Hold Time	0				ns	(4)
	TWLDV	Write Data Delay Time	80				ns	(4)
	TWLEL	Early Output High-Z Time	0				ns	(4)
	TEHWH	Late Output High-Z Time	0				ns	(4)
	TELEL	Read or Write Cycle Time	290				ns	(4)

NOTES:
(1) All devices tested at worst case limits. Room Temp., 5V data provided for information – not guaranteed unless specified.
(2) Operating Supply Current (ICCOP) is proportional to Operating Frequency. Ex: Typical ICCOP = 5mA/MHz.
(3) Capacitance sampled and guaranteed – not 100% tested.
(4) AC test conditions: Inputs – TRISE = TFALL = 10ns; Output – CLOAD = 50pF. All timing measured at 1.5V reference level.
(5) This value is guaranteed and tested at 25°C.

ABSOLUTE MAXIMUM RATINGS *

Supply Voltage – (VCC -GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage	
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Industrial (-9)	-40°C to +85°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP = 25°C (1) VCC = 5.0V TYP	TEMP = 25°C (1) VCC = 5.0V MAX (5)	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		25		3.0	µA	IO = 0 $\overline{E}$ = VCC –0.3V
	ICCOP	Operating Supply Current (2)		7	5		mA	$\overline{E}$ = 1MHz, IO = 0 VI = GND
	ICCDR	Data Retention Supply Current		15		2.0	µA	VCC = 2.0V IO = 0 $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		1.4		V	
	II	Input Leakage Current	-1.0	+1.0	0.0		µA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	0.0		µA	GND ≤ VIO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	1.8		V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.2		V	
	VOL	Output Low Voltage		0.4	0.25		V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.0		V	IO = -1.0mA
	CI	Input Capacitance (3)		8.0	5.0		pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance (3)		10.0	6.0		pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		200			ns	(4)
	TAVQV	Address Access Time		220			ns	(4)
	TELQX	Chip Enable Output Enable Time	20				ns	(4)
	TWLQZ	Write Enable Output Disable Time		80			ns	(4)
	TEHQZ	Chip Enable Output Disable Time		80			ns	(4)
	TELEH	Chip Enable Pulse Negative Width	200				ns	(4)
	TEHEL	Chip Enable Pulse Positive Width	90				ns	(4)
	TAVEL	Address Setup Time	20				ns	(4)
	TELAX	Address Hold Time	50				ns	(4)
	TWLWH	Write Enable Pulse Width	200				ns	(4)
	TWLEH	Write Enable Pulse Setup Time	200				ns	(4)
	TELWH	Write Enable Pulse Hold Time	200				ns	(4)
	TDVWH	Data Setup Time	120				ns	(4)
	TWHDZ	Data Hold Time	0				ns	(4)
	TWLDV	Write Data Delay Time	80				ns	(4)
	TWLEL	Early Output High-Z Time	0				ns	(4)
	TEHWH	Late Output High-Z Time	0				ns	(4)
	TELEL	Read or Write Cycle Time	290				ns	(4)

NOTES:
(1) All devices tested at worst case limits. Room Temp., 5V data provided for information – not guaranteed unless specified.
(2) Operating Supply Current (ICCOP) is proportional to Operating Frequency. Ex: Typical ICCOP = 5mA/MHz.
(3) Capacitance sampled and guaranteed – not 100% tested.
(4) AC test conditions: Inputs – TRISE TFALL = 10ns; Output – CLOAD = 50pF. All timing measured at 1.5V reference level.
(5) This value is guaranteed and tested at 25°C.

HARRIS

HM-6516

Advance Information

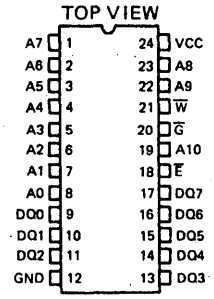
2K x 8 CMOS RAM

Features

- LOW POWER STANDBY — 275 μW MAX
- LOW POWER OPERATION — 55mW/MHz MAX
- FAST ACCESS — 120/200 ns MAX
- INDUSTRY STANDARD PINOUT
- SINGLE SUPPLY — 5 VOLT VCC
- TTL COMPATIBLE
- STATIC MEMORY CELLS
- HIGH OUTPUT DRIVE
- ON CHIP ADDRESS LATCHES
- EASY MICROPROCESSOR INTERFACING
- WIDE TEMPERATURE RANGE

Pinout

TOP VIEW



PIN NAMES

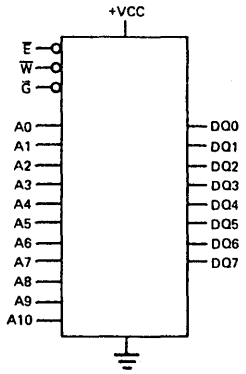
A	Address Input
DQ	Data Input/Output
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable

Description

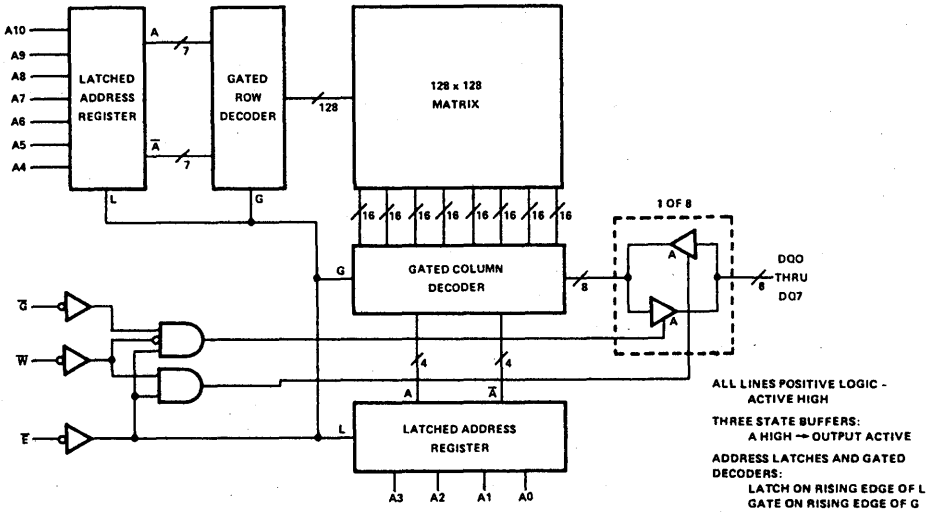
The HM-6516 is a CMOS 2048 x 8 Static Random Access Memory. Extremely low power operation is achieved by the use of complementary MOS design techniques. This low power is further enhanced by the use of synchronous circuit techniques that keep the active (operating) power low, and also give fast access times. The pinout of the HM-6516 is the popular 24 pin, 8 bit wide JEDEC standard which allows easy memory board layouts, flexible enough to accomodate a variety of PROMs, RAMs, EPROMs, and ROMs.

The HM-6516 is ideally suited for use in microprocessor based systems. The byte wide organization simplifies the memory array design,and keeps operating power down to a minimum because only one device is enabled at a time. The address latches allow very simple interfacing to recent generation microprocessors which employ a multiplexed address/data bus. The convenient output enable control also simplifies multiplexed bus interfacing by allowing the data outputs to be controlled independent of the chip enable.

Logic Symbol



Functional Diagram



CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage (VCC – GND)	–0.3 to 8.0V	Operating Supply Voltage	
Input or Output Voltage Applied	(GND –0.3V) to (VCC +0.3V)	Military (–2)	4.5V to 5.5V
		Industrial (–9)	4.5V to 5.5V
Storage Temperature	–65°C to 150°C	Operating Temperature	
		Military (–2)	–55°C to +125°C
		Industrial (–9)	–40°C to +85°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP.& VCC = OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		50	µA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		10	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		25	µA	IO = 0, VCC = 2.0, VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	–1.0	+1.0	µA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	–1.0	+1.0	µA	GND ≤ VIO ≤ VCC
	VIL	Input Low Voltage	–0.3	0.8	V	
	VIH	Input High Voltage	2.4	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 3.2mA
	VOH	Output High Voltage	2.4		V	IO = –1.0mA
	CI	Input Capacitance ③		8.0	pF	VI = VCC or GND, f = 1MHz
	CIO	Input/Output Capacitance ③		10.0	pF	VIO = VCC or GND, f = 1MHz
A.C.	TELQV	Chip Enable Access Time		120	ns	④
	TAVQV	Address Access Time		120	ns	④
	TELQX	Chip Enable Output Enable Time	10		ns	④
	TWLQZ	Write Enable Output Disable Time		50	ns	④
	TEHQZ	Chip Enable Output Disable Time		50	ns	④
	TGLQX	Output Enable Output Enable Time	10		ns	④
	TGHQZ	Output Enable Output Disable Time		50	ns	④
	TELEH	Chip Enable Pulse Negative Width	120		ns	④
	TEHEL	Chip Enable Pulse Positive Width	50		ns	④
	TAVEL	Address Setup Time	0		ns	④
	TELAX	Address Hold Time	30		ns	④
	TWLWH	Write Enable Pulse Width	120		ns	④
	TWLEH	Write Enable Pulse Setup Time	120		ns	④
	TELWH	Write Enable Pulse Hold Time	120		ns	④
	TDVWH	Data Setup Time	50		ns	④
	TWHDX	Data Hold Time	0		ns	④
	TWLDV	Write Data Delay Time	50		ns	④
	TELEL	Read or Write Cycle Time	170		ns	④

NOTES:

① All devices tested at worst case limits. Room temp., 5 volt data provided for information - not guaranteed.

② Operating Supply Current (ICCOP) is proportional to Operating Frequency.
Example: Typical ICCOP = 5mA/MHz.

③ Capacitance sampled and guaranteed - not 100% tested.

④ AC test conditions: Inputs – TRISE = TFALL = 5ns; Output – CLOAD = 50pF. All timing measured at 1.5V reference level.

HARRIS

HM-65161

2048 × 8 Asynchronous CMOS Static RAM

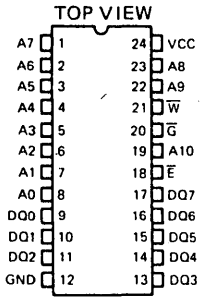
Advance Information

Features

- FAST ACCESS TIME — 55/70 ns MAX
- LOW STANDBY CURRENT — 100μA MAX
- LOW OPERATING CURRENT — 60mA MAX
- DATA RETENTION @2.0VOLTS — 40μA MAX
- TTL COMPATIBLE INPUTS AND OUTPUTS
- JEDEC APPROVED PINOUT (2716, 6116 TYPE)
- NO CLOCKS OR STROBES REQUIRED
- WIDE TEMPERATURE RANGE — -55°C to +125°C
- EQUAL CYCLE AND ACCESS TIME
- SINGLE 5 VOLT SUPPLY

Pinout

TOP VIEW



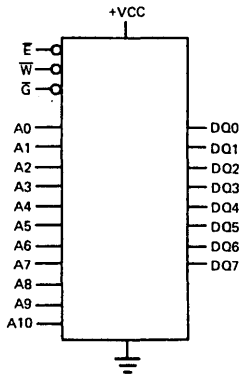
PIN NAMES

A	Address Input
DQ	Data Input/Output
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable

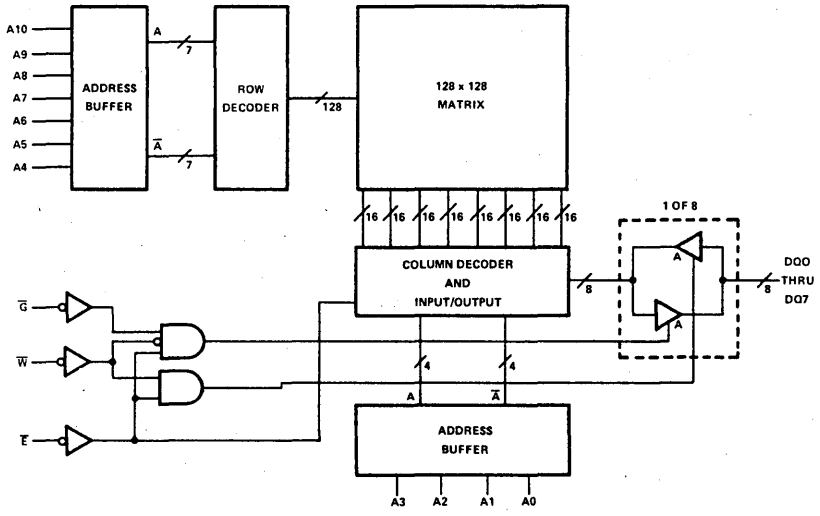
Description

The HM-65161 is a CMOS 2048 x 8 Static Random Access Memory. It is manufactured using the HARRIS' advanced SAJI IV process. The device utilizes asynchronous circuit design for fast cycle time and ease of use. The pinout is the JEDEC 24 pin, 8 bit wide standard which allows easy memory board layouts flexible to accomodate a variety of industry standard PROM's, RAM's, ROM's and EPROM's. The HM-65161 is ideally suited for use in microprocessor based systems with its 8 bit word length organization. The convenient output enable also simplifies the bus interface by allowing the data outputs to be controlled independent of the chip enable.

Logic Symbol



Functional Diagram



CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

ABSOLUTE MAXIMUM RATINGS*		OPERATING RANGE	
Supply Voltage (VCC - GND)	−0.3 to 8.0V	Operating Supply Voltage	
Input or Output Voltage Applied	(GND −0.3V) to (VCC +0.3V)	Commercial (−5)	4.5V to 5.5V
		Operating Temperature	
Storage Temperature	−65°C to 150°C	Commercial (−5)	0°C to +75°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. &VCC= OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB1	Standby Supply Current		500	μA	IO = 0, $\overline{E}$ = VCC-0.3V
	ICCSB	Standby Supply Current		15	mA	$\overline{E}$ = VIH, IO =O
	ICC	Enabled Supply Current		70	mA	$\overline{E}$ = OV
	ICCOP	Operating Supply Current ②		70	mA	$\overline{E}$ = OV
	ICCDR	Data Retention Supply Current		200	μA	IO = 0, VCC = 2.0 $\overline{E}$ = VCC-0.3V
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	−1.0	+1.0	μA	GND≤ VI≤ VCC
	IIOZ	Input/Output Leakage Current	−1.0	+1.0	μA	GND≤VIO≤VCC
	VIL	Input Low Voltage	−0.3	0.8	V	
	VIH	Input High Voltage	2.4	VCC +0.3V	V	
	VOL	Output Low Voltage		0.4	V	IO = 4.0mA
	VOH	Output High Voltage	2.4		V	IO = −1.0mA
	CI	Input Capacitance ③		8	pF	VI = VCC or GND, f = 1MHz
	CIO	Input/Output Capacitance ③		10	pF	VIO = VCC or GND, f = 1MHz
READ CYCLE	TAVAV	Read Cycle Time	55		ns	④
	TAVQV	Address Access Time		55	ns	④
	TELQV	Chip Enable Access Time		55	ns	④
	TELQX	Chip Enable Output Enable Time	10		ns	④
	TGLQV	Output Enable Output Enable Time		35	ns	④
	TGLQX	Output Enable Output Enable Time	0		ns	④
	TEHQZ	Chip Enable Output Disable Time		25	ns	④
	TGHQZ	Output Enable Output Disable Time		25	ns	④
	TAVQX	Output Hold from Address Change	10		ns	④
A.C. WRITE CYCLE	TAVAV	Write Cycle Time	55		ns	④
	TELWH	Chip Selection to End of Write	50		ns	④
	TAVWL	Address Setup Time	0		ns	④
	TWLWH	Write Enable Pulse Width	50		ns	④
	TWHAV	Write Enable Read Setup Time	5		ns	④
	TGHQZ	Output Enable Output Disable Time		25	ns	④
	TWLQZ	Write Enable Output Disable Time		25	ns	④
	TDVWH	Data Setup Time	25		ns	④
	TWHDX	Data Hold Time	5		ns	④
	TWHQX	Write Enable Output Enable Time	5		ns	④
	TWLEH	Write Enable Pulse Setup Time	50		ns	④
	TDVEH	Chip Enable Data Setup Time	25		ns	④

NOTES:
① All devices tested at worst case limits.
② Typical derating = 5mA/MHz increase in ICCOP; VI = VCC or GND.
③ Capacitance sampled and guaranteed - not 100% tested.
④ AC test conditions: Inputs — TRISE = TFALL = 5ns; Output — CLOAD = 30pF. All timing measured at 1.5V reference level.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (VCC - GND)	−0.3 to 8.0V
Input or Output Voltage Applied	(GND −0.3V) to (VCC +0.3V)
Storage Temperature	−65°C to 150°C

OPERATING RANGE

Operating Supply Voltage	
Commercial (−5)	4.5V to 5.5V
Operating Temperature	
Commercial (−5)	0°C to +75°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. &VCC= OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB1	Standby Supply Current		100	µA	IO = 0, $\overline{E}$ = VCC-0.3V
	ICCSB	Standby Supply Current		10	mA	$\overline{E}$ = VIH, IO =O
	ICC	Enabled Supply Current		60	mA	$\overline{E}$ = OV
	ICCOP	Operating Supply Current ②		60	mA	$\overline{E}$ = OV
	ICCDR	Data Retention Supply Current		40	µA	IO = 0, VCC = 2.0 $\overline{E}$ = VCC−0.3V
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	−1.0	+1.0	µA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	−1.0	+1.0	µA	GND ≤ VIO ≤ VCC
	VIL	Input Low Voltage	−0.3	0.8	V	
	VIH	Input High Voltage	2.4	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 4.0mA
	VOH	Output High Voltage	2.4		V	IO = −1.0mA
	CI	Input Capacitance ③		8	pF	VI = VCC or GND, f = 1MHz
	CIO	Input/Output Capacitance ③		10	pF	VIO = VCC or GND, f = 1MHz
READ CYCLE	TAVAV	Read Cycle Time	70		ns	④
	TAVQV	Address Access Time		70	ns	④
	TELQV	Chip Enable Access Time		70	ns	④
	TELQX	Chip Enable Output Enable Time	10		ns	④
	TGLQV	Output Enable Output Enable Time		40	ns	④
	TGLQX	Output Enable Output Enable Time	0		ns	④
	TEHQZ	Chip Enable Output Disable Time		35	ns	④
	TGHQZ	Output Enable Output Disable Time		35	ns	④
	TAVQX	Output Hold from Address Change	10		ns	④
A.C. WRITE CYCLE	TAVAV	Write Cycle Time	70		ns	④
	TELWH	Chip Selection to End of Write	65		ns	④
	TAVWL	Address Setup Time	0		ns	④
	TWLWH	Write Enable Pulse Width	65		ns	④
	TWHAV	Write Enable Read Setup Time	5		ns	④
	TGHQZ	Output Enable Output Disable Time		35	ns	④
	TWLQZ	Write Enable Output Disable Time		35	ns	④
	TDVWH	Data Setup Time	30		ns	④
	TWHDX	Data Hold Time	5		ns	④
	TWHQX	Write Enable Output Enable Time	5		ns	④
	TWLEH	Write Enable Pulse Setup Time	65		ns	④
	TDVEH	Chip Enable Data Setup Time	30		ns	④

NOTES:
① All devices tested at worst case limits.
② Typical derating = 5 mA/MHz increase in ICCOP; VI = VCC or GND.
③ Capacitance sampled and guaranteed - not 100% tested.
④ AC test conditions: Inputs – TRISE = TFALL = 5ns; Output – CLOAD = 30pF. All timing measured at 1.5V reference level.

HARRIS

HM-6116

2048 × 8 Asynchronous CMOS Static RAM

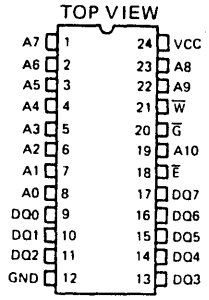
Advance Information

Features

- FAST ACCESS TIME — 120 ns MAX
- LOW STANDBY CURRENT — 100μA MAX
- LOW OPERATING CURRENT — 70mA MAX
- DATA RETENTION @2.0VOLTS — 50μA MAX
- TTL COMPATIBLE INPUTS AND OUTPUTS
- JEDEC APPROVED PINOUT (2716, 6116 TYPE)
- NO CLOCKS OR STROBES REQUIRED
- WIDE TEMPERATURE RANGE — -55°C to +125°C
- EQUAL CYCLE AND ACCESS TIME
- SINGLE 5 VOLT SUPPLY

Pinout

TOP VIEW



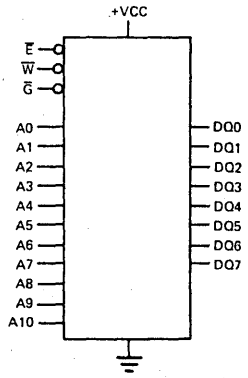
PIN NAMES

A	Address Input
DQ	Data Input/Output
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable

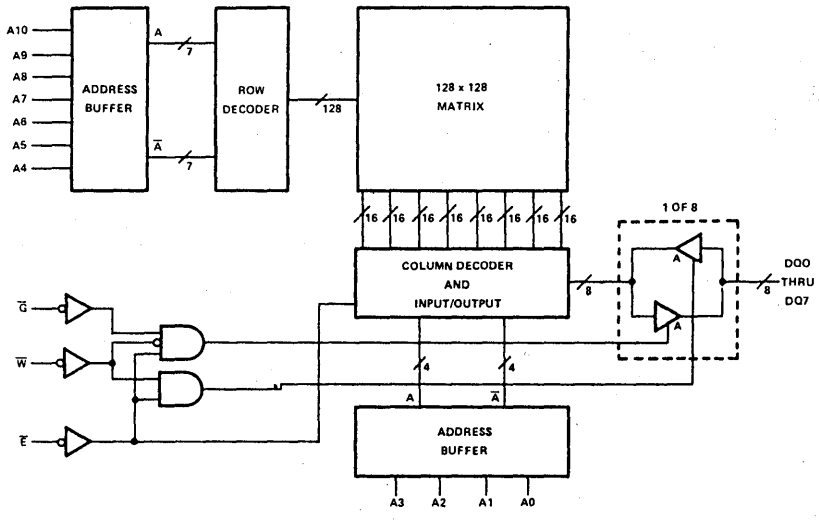
Description

The HM-6116 is a CMOS 2048 x 8 Static Random Access Memory. It is manufactured using the HARRIS' advanced SAJI IV process. The device utilizes asynchronous circuit design for fast cycle time and ease of use. The pinout is the JEDEC 24 pin, 8 bit wide standard which allows easy memory board layouts flexible to accomodate a variety of industry standard PROM's, RAM's, ROM's and EPROM's. The HM-6116 is ideally suited for use in microprocessor based systems with its 8 bit word length organization. The convenient output enable also simplifies the bus interface by allowing the data outputs to be controlled independent of the chip enable.

Logic Symbol



Functional Diagram



CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (VCC - GND)	−0.3 to 8.0V
Input or Output Voltage Applied	(GND −0.3V) to (VCC +0.3V)
Storage Temperature	−65°C to 150°C

OPERATING RANGE

Operating Supply Voltage	
Military (−2)	4.5V to 5.5V
Operating Temperature	
Military (−2)	−55°C to +125°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. &VCC= OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB1	Standby Supply Current		3	mA	IO = 0, $\overline{E}$ = VCC-0.3V
	ICCSB	Standby Supply Current		20	mA	$\overline{E}$ = VIH, IO =O
	ICC	Enabled Supply Current		85	mA	$\overline{E}$ = OV
	ICCOP	Operating Supply Current ②		85	mA	$\overline{E}$ = OV
	ICCDR	Data Retention Supply Current		1.2	mA	IO = 0, VCC = 2.0 $\overline{E}$ = VCC-0.3V
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	−10.0	+10.0	μA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	−10.0	+10.0	μA	GND ≤ VIO ≤ VCC
	VIL	Input Low Voltage	−0.3	0.8	V	
	VIH	Input High Voltage	VCC −2.0	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 4.0mA
	VOH	Output High Voltage	2.4		V	IO = −1.0mA
	CI	Input Capacitance ③		8	pF	VI = VCC or GND, f = 1MHz
	CIO	Input/Output Capacitance ③		10	pF	VIO = VCC or GND, f = 1MHz
READ CYCLE	TAVAV	Read Cycle Time	120		ns	④
	TAVQV	Address Access Time		120	ns	④
	TELQV	Chip Enable Access Time		120	ns	④
	TELQX	Chip Enable Output Enable Time	10		ns	④
	TGLQV	Output Enable Output Enable Time		80	ns	④
	TGLQX	Output Enable Output Enable Time	10		ns	④
	TEHQZ	Chip Enable Output Disable Time		40	ns	④
	TGHQZ	Output Enable Output Disable Time		40	ns	④
	TAVQX	Output Hold from Address Change	10		ns	④
A.C. WRITE CYCLE	TAVAV	Write Cycle Time	120		ns	④
	TELWH	Chip Selection to End of Write	70		ns	④
	TAVWH	Address Valid to End of Write	105		ns	④
	TAVWL	Address Setup Time	20		ns	④
	TWLWH	Write Enable Pulse Width	70		ns	④
	TWHAV	Write Enable Read Setup Time	5		ns	④
	TGHQZ	Output Enable Output Disable Time		40	ns	④
	TWLQZ	Write Enable Output Disable Time		50	ns	④
	TDVWH	Data Setup Time	35		ns	④
	TWHDX	Data Hold Time	5		ns	④
	TWHQX	Write Enable Output Enable Time	5		ns	④
	TWLEH	Write Enable Pulse Setup Time	70		ns	④
	TDVEH	Chip Enable Data Setup Time	35		ns	④

NOTES:
① All devices tested at worst case limits.
② Typical derating = 5mA/MHz increase in ICCOP; VI = VCC or GND.
③ Capacitance sampled and guaranteed - not 100% tested.
④ AC test conditions: Inputs — TRISE = TFALL = 5ns; Output — CLOAD = 100pF (including scope and jig) All timing measured at 1.5V reference level.

HARRIS

SEMICONDUCTOR CMOS DIGITAL PRODUCTS DIVISION

HM5-6564

8K x 8, 16K x 4 CMOS RAM

Features

- LOW POWER STANDBY — 4mW MAX
- LOW POWER OPERATION — 280mW/MHz MAX
- DATA RETENTION — 2.0V MIN
- TTL COMPATIBLE IN/OUT
- THREE STATE OUTPUTS
- FAST ACCESS TIME — 350ns MAX
- FULL MILITARY TEMPERATURE AVAILABLE — -55°C to 125°C
- INDUSTRIAL TEMPERATURE STANDARD — -40°C to 85°C
- COMMERCIAL TEMPERATURE AVAILABLE — 0°C to 75°C
- ON CHIP ADDRESS REGISTERS
- ORGANIZABLE 8K x 8 or 16K x 4
- 40 PIN DIP PINOUT - 2.000" x 0.900"

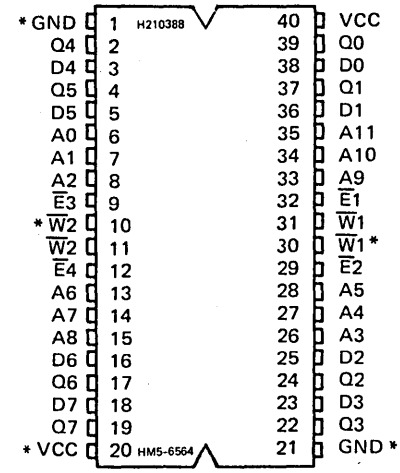
Description

The HM-6564 is a 64K bit CMOS RAM. It consists of 16 HM4-6504 4K x 1 CMOS RAMs, in leadless carriers, mounted on a ceramic substrate. The HM-6564 is configured as an extra wide, standard length 40 pin DIP. The memory appears to the system as an array of 16 4K x 1 static RAMs. The array is organized as two 8K by 4 blocks of RAM sharing only the address bus. The data inputs, data outputs, chip enables and write enables are separate for each block of RAM. This allows the user to organize the HM-6564 RAM as either an 8K by 8 or a 16K by 4 array. The HM-6564 also contains decoupling capacitors to reduce noise and to minimize the need for additional external decoupling.

This 64K memory provides a unique blend of low power CMOS semiconductor technology and advanced packaging techniques. The HM-6564 is intended for use in any application where a large amount of RAM is needed, and where power consumption and board space are prime concerns. The guaranteed low voltage data retention characteristics allow easy implementation of non-volatile read/write memory by using very small batteries mounted directly on the memory circuit board. Example applications include digital avionic instrumentation, remote data acquisition, and portable or hand held digital communications devices.

Pinout

TOP VIEW

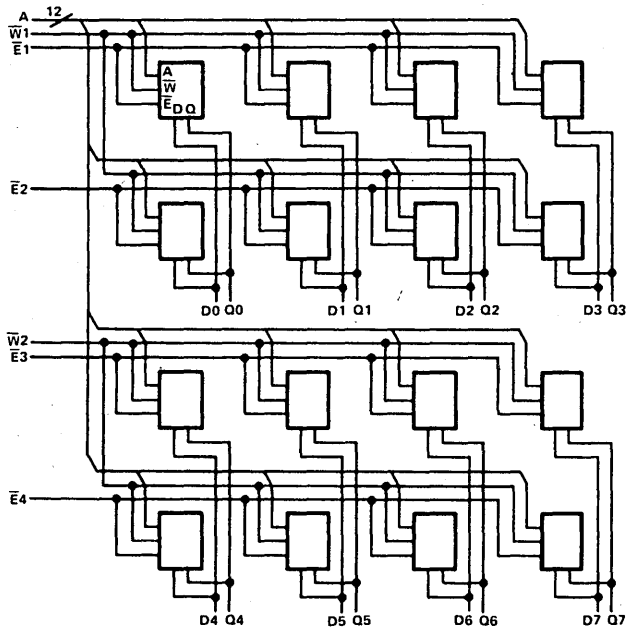


***NOTES:**

Pins 20 and 40 (VCC) are internally connected. Similarly pins 1 and 21 (Ground) are connected. The user is advised to connect all four VCC pins and Ground pins to his board busses. This will improve power distribution across the array and will enhance decoupling.

Pin 10 is internally connected to pin 11, and pin 30 is connected to pin 31. For those users wishing to preserve board compatibility with possible future RAM arrays, we recommend connections to the write lines be made at pins 11 and 31, leaving pins 10 and 30 free for future expansion.

Functional Diagram



CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage - (VCC - GND)	-0.3V to +8.0V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage	
Military (-2)/Industrial (-9)	+4.5V to +5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS

D.C.

SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX ④	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current		800		150/48	μA	IO = 0 VI = VCC or GND
ICCOP1	Operating Supply Current (8K x 8) ②		56	40		mA	f = 1MHz, IO = 0 VI = VCC or GND
ICCOP2	Operating Supply Current (16K x 4) ②		28	20		mA	f = 1MHz, IO = 0 VI = VCC or GND
ICCDR	Data Retention Supply Current		400		48/32	μA	IO = 0, VCC = 2.0, VI = VCC or GND
VCCDR	Data Retention Supply Voltage	2.0		1.4		V	
IIA	Address Input Leakage	-20	+20	1		μA	GND≤VI≤VCC
IID1	Data Input Leakage (8K x 8)	-3	+3	0.1		μA	GND≤VI≤VCC
IID2	Data Input Leakage (16K x 4)	-5	+5	0.5		μA	GND≤VI≤VCC
IIE1	Enable Input Leakage (8K x 8)	-10	+10	0.2		μA	GND≤VI≤VCC
IIE2	Enable Input Leakage (16K x 4)	-5	+5	0.2		μA	GND≤VI≤VCC
IIW	Write Enable Input Leakage (Each)	-10	+10	0.5		μA	GND≤VI≤VCC
IOZ1	Output Leakage (8K x 8)	-5	+5	0.4		μA	GND≤VO≤VCC
IOZ2	Output Leakage (16K x 4)	-10	+10	1		μA	GND≤VO≤VCC
VIL	Input Low Voltage	-0.3	0.8	2.0		V	
VIH	Input High Voltage	VCC-2.0	VCC+0.3	2.0		V	
VOL	Output Low Voltage		0.4	0.25		V	IO = 2.0mA
VOH	Output High Voltage	2.4		4.0		V	IO = -1.0mA
CIA	Address Input Capacitance ③		200	170		pF	f = 1MHz, VI = VCC or GND
CID1	Data Input Capacitance (8K x 8) ③		50	30		pF	f = 1MHz, VI = VCC or GND
CID2	Data Input Capacitance (16K x 4) ③		100	60		pF	f = 1MHz, VI = VCC or GND
CIE1	Enable Input Capacitance (8K x 8) ③		160	100		pF	f = 1MHz, VI = VCC or GND
CIE2	Enable Input Capacitance (16K x 4) ③		80	50		pF	f = 1MHz, VI = VCC or GND
CIW	Write Enable Input Capacitance (Each) ③		100	80		pF	f = 1MHz, VI = VCC or GND
CO1	Output Capacitance (8K x 8) ③		50	30		pF	f = 1MHz, VO = VCC or GND
CO2	Output Capacitance (16K x 4) ③		100	60		pF	f = 1MHz, VO = VCC or GND
CVCC	Decoupling Capacitance	.25		0.33		μF	f = 1MHz

NOTES:

① Each individual RAM in the leadless carrier is fully tested at worst case limits of temperature and voltage. The complete assembled HM-6564 array is tested at room temperature only. The worst case parameters are guaranteed over the specified temperature and voltage ranges. Room temperature, 5 volt data is provided for information purposes and is not guaranteed.

② Operating supply current is proportional to operating frequency. ICCOP is specified at an operating frequency of 1MHz, indicating repetive accessing at a 1μs rate. Operation at slower rates will decrease ICCOP proportionally.

③ Capacitance sampled and guaranteed - not 100% tested.

④ This value is guaranteed and tested at 25°C.

ELECTRICAL CHARACTERISTICS

A.C.

SYMBOL	PARAMETER	TEMP & VCC = OPERATING RANGE		TEMP = 25°C ① VCC = 5.0V			UNITS	TEST CONDITIONS
		MIN	MAX	MIN	TYP	MAX		
TELQV	Chip Enable Access		350		250	300	ns	⑤
TAVQV	Address Access (TAVQV=TELQV+TAVEL)		400		270	350	ns	⑤
TELQX	Output Enable	20	120		50	100	ns	⑤
TEHQZ	Output Disable		120		50	100	ns	⑤
TELEL	Read or Write Cycle	480		410	320		ns	⑤
TELEH	Chip Enable Low	350		300	250		ns	⑤
TEHEL	Chip Enable High	130		110	70		ns	⑤
TAVEL	Address Setup	50		50	20		ns	⑤
TELAX	Address Hold	50		50	20		ns	⑤
TWLWH	Write Enable Low	150		130	100		ns	⑤
TWLEH	Write Enable Setup	250		220	170		ns	⑤
TWLEL	Early Write Setup (Write Mode)	10		10	0		ns	⑤
TWHEL	Write Enable Read Setup	10		10	0		ns	⑤
TELWX	Early Write Hold (Write Mode)	100		100	70		ns	⑤
TDVWL	Data Setup	10		10	0		ns	⑤
TDVEL	Early Write Data Setup	10		10	0		ns	⑤
TWLDX	Data Hold	100		100	70		ns	⑤
TELDX	Early Write Data Hold	100		100	70		ns	⑤
TQVWL	Data Valid to Write (Read-Modify-Write)	0		0	0		ns	⑤

NOTES:

⑤ AC Test Conditions:

Inputs - Trise = Tfall $\leq$ 20ns.
Outputs - CLOAD = 100pF.
Timing measured at 1.5V reference level.

HARRIS

HM-92560

256K SYNCHRONOUS CMOS RAM MODULE

PREVIEW

Features

- LOW STANDBY CURRENT — 1mA/8 mA
- FAST ACCESS TIME — 250 ns
- DATA RETENTION — 2.0V min VCC
- THREE STATE OUTPUTS
- ORGANIZABLE AS 32K×8 or 16K×16 ARRAY
- ON CHIP ADDRESS REGISTERS
- 48 PIN DIP PINOUT – 2.53″ × 1.30″ × 0.25″
- SYNCHRONOUS OPERATION YIELDS LOW OPERATING POWER — 30mA/MHz
- WIDE TEMPERATURE RANGE — −55°C to +125°C

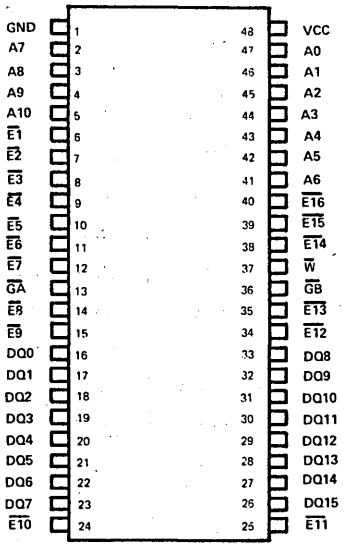
Description

The HM-92560 is a high density 256K bit CMOS RAM module. Sixteen synchronous HM-6516 2K × 8 CMOS RAMs in leadless chip carriers are mounted on a multilayer ceramic substrate. The HM-92560 RAM module is organized as two 16K by 8 CMOS RAM arrays sharing a common address bus. Separate data input/output buses and chip enables allow the user to format the HM-92560 as either a 16K×16 or 32K×8 array. Ceramic capacitors are included on the substrate to reduce noise and to minimize the need for additional external decoupling.

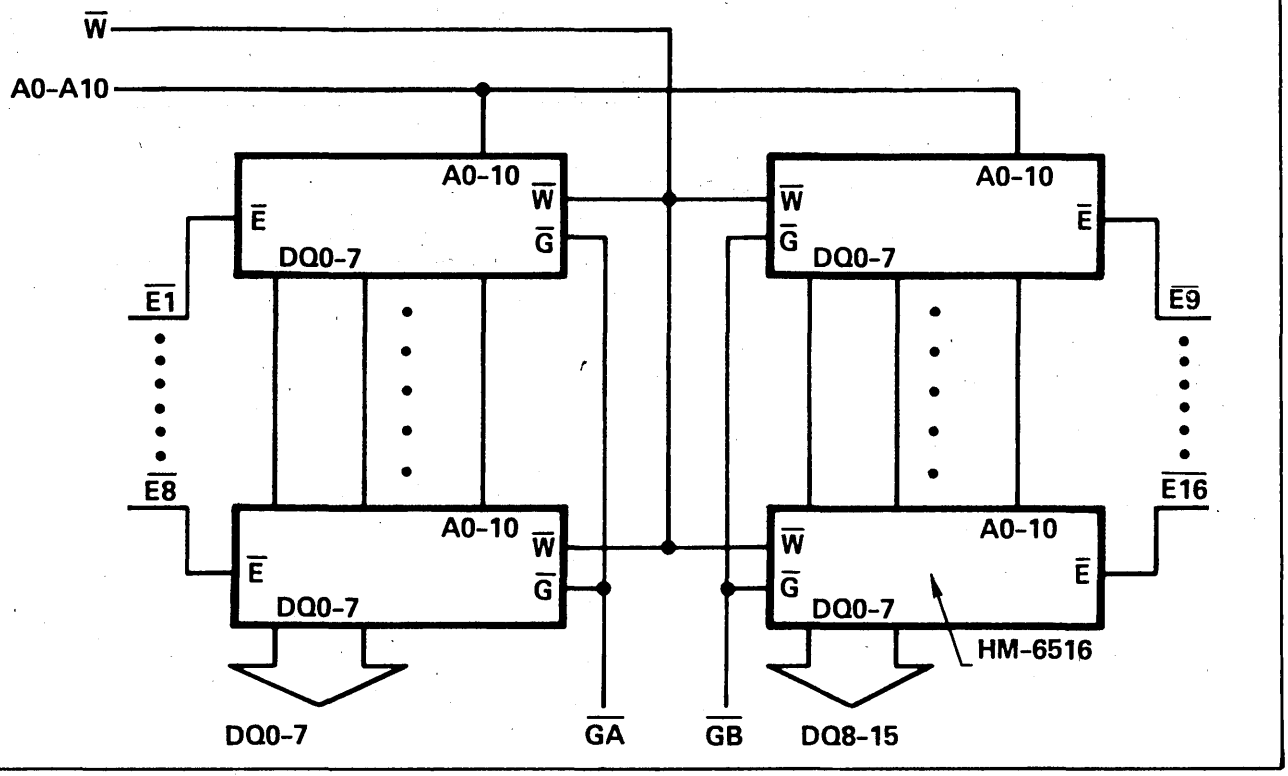
The synchronous design of the HM-92560 provides low operating power along with address latches for ease of interface to multiplexed address/data bus microprocessors.

The HM-92560 is physically constructed as an extra wide 48 pin dual-in-line package with standard 0.1″ centers between pins. This packaging technique combines the high packing density of CMOS and leadless chip carriers with the ease of use of DIP packaging.

Pinout



Functional Diagram



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

HARRIS

HM-6641

Preliminary 512 x 8 CMOS PROM

Features

- LOW POWER STANDBY — 500μW MAX.
- LOW POWER OPERATION — 50mW/MHz MAX.
- FAST ACCESS TIME — 250ns MAX.
- FIELD PROGRAMMABLE
- POLYSILICON FUSE LINKS
- TTL COMPATIBLE IN/OUT
- POPULAR PINOUT LIKE BIPOLAR 7641
- THREE STATE OUTPUTS
- ADDRESS LATCHES INCLUDED ON CHIP
- EASY MICROPROCESSOR INTERFACING
- WIDE TEMPERATURE RANGES

Description

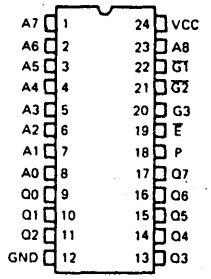
The HM-6641 is a 512 x 8 CMOS polysilicon fuse link Programmable Read Only Memory in the popular 24 pin, byte wide pinout. Synchronous circuit design techniques combine with CMOS processing to give this device high speed performance with very low power dissipation.

On chip address latches are provided, allowing easy interfacing with recent generation microprocessors that use multiplexed address/data bus structures, such as the 8085. The output enable controls, both active low and active high, further simplify microprocessor system interfacing by allowing output data bus control independent of the chip enable control. The data output latches allow the use of the HM-6641 in high speed pipelined architecture systems, and also in synchronous logic replacemant functions.

Applications for the HM-6641 CMOS PROM include low power handheld microprocessor based instrumentation and communications systems, remote data acquisition and processing systems, processor control store, and synchronous logic replacement.

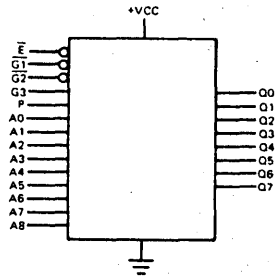
Pinout

TOP VIEW

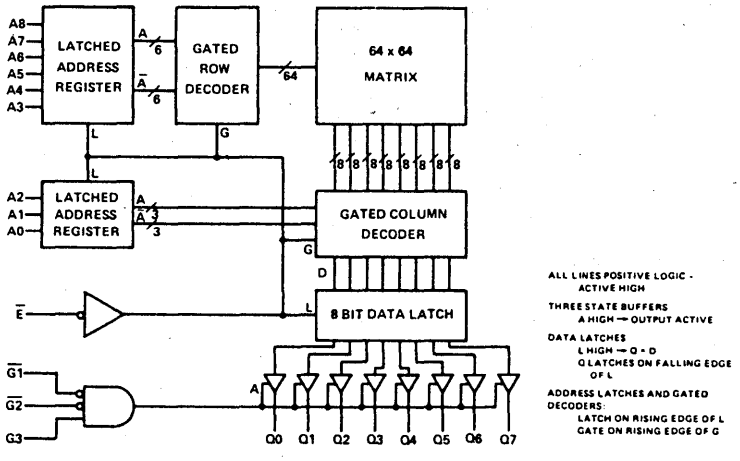


A Address Input
Q Data Output
$\overline{E}$ Chip Enable
$\overline{G}$ Output Enable
P Program Enable
(P = Gnd. except when programming)

Logic Symbol



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge.

ABSOLUTE MAXIMUM RATINGS *		OPERATING RANGE	
Supply Voltage -VCC	+8.0V	Operating Supply	
		Military (-2)	4.5V to 5.5V
Input or Output Voltage Applied	GND -0.3Vto VCC +0.3V	Industrial (-9)	4.5V to 5.5V
		Operating Temperature	
Storage Temperature	-65°C to +150°C	Military (-2)	-55°C to +125°C
		Industrial (-9)	-40°C to +85°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

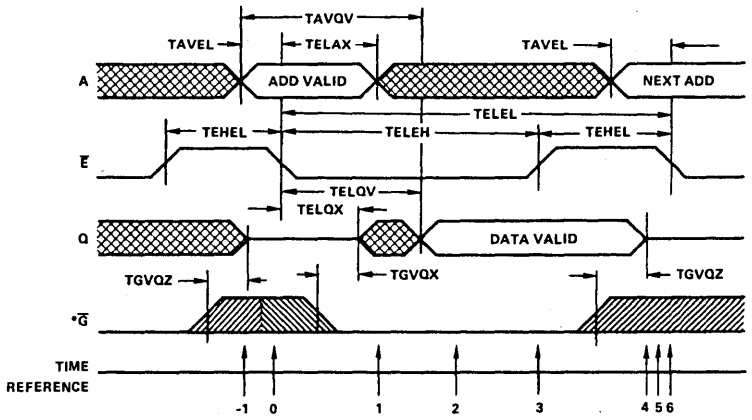
ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEMP & VCC = OPERATING RANGE MIN	TEMP & VCC = OPERATING RANGE MAX	TEMP=25°C VCC=5.0 (1) TYPICAL	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current		100	10	μA	IO = 0 VI = GND OR VCC
ICCOP	Operating Supply Current (2)		10	5	mA	f = 1MHz, IO = 0 VI = VCC or GND
II	Input Leakage Current	-1.0	+1.0	0.0	μA	GND≤VI≤VCC
IOZ	Output Leakage Current	-1.0	+1.0	±0.5	μA	GND≤VO≤VCC
VIL	Input Low Voltage	-0.3	0.8	2.0	V	
VIH	Input High Voltage	VCC-2.0	VCC+0.3	2.0	V	
VOL	Output Low Voltage		0.4	0.1	V	IOL = 3.2mA
VOH	Output High Voltage	2.4		4.25	V	IOH = -1.0mA
CI	Input Capacitance (3)		8.0	5.0	pF	VI = VCC or GND f = 1MHz
CO	Output Capacitance (3)		10.0	8.0	pF	VO = VCC OR GND f = 1MHz
TELQV	Chip Enable Access Time		250	150	ns	(4)
TAVQV	(TAVQV = TELQV + TAVEL) Address Access Time		270	150	ns	(4)
TELQX	Chip Enable Output Enable Time	20	150	70	ns	(4)
TGVQX	Output Enable Output Enable Time	20	150	70	ns	(4)
TGXQZ	Output Enable Output Disable Time	20	150	70	ns	(4)
TELEH	Chip Enable Pulse Negative Width	250		150	ns	(4)
TELEL	Read Cycle Time	400		230	ns	(4)
TEHEL	Chip Enable Pulse Positive Width	150		80	ns	(4)
TAVEL	Address Set-up Time	20		0	ns	(4)
TELAX	Address Hold Time	60		40	ns	(4)

NOTES:

(1) All devices tested at worst case limits. Room temp., 5 volt data provided for information - not guaranteed.
(2) Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
(3) Capacitance sampled and guaranteed - not 100% tested.
(4) AC Test Conditions: Inputs-TRISE = TFALL = 20nsec; Outputs -CLOAD = 50pF. All timing measurements at 1.5V.

Read Cycle



*G HAS SAME TIMING AS $\overline{G}$ EXCEPT SIGNAL IS INVERTED

TRUTH TABLE

TIME REFERENCE	INPUTS			OUTPUTS	FUNCTION
	E	G	A	O	
-1	H	H	X	Z	MEMORY DISABLED
0	↘	H	V	Z	CYCLE BEGINS-ADDRESSES ARE LATCHED
1	L	L	X	X	OUTPUT ENABLED
2	L	L	X	V	OUTPUT VALID
3	↗	L	X	V	OUTPUT LATCHED
4	H	H	X	Z	READ ACCOMPLISHED AND OUTPUT DISABLED
5	H	H	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
6	↘	H	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

In the HM-6641 read cycle, the address information is latched into the on chip registers on the falling edge of $\overline{E}$(T = 0). Minimum address setup and hold time requirements must be met. After the required hold time,the addresses may change state without affecting device operation. To read data $\overline{G1}$ and $\overline{G2}$ must be low, and G3 must be high. After access time, $\overline{E}$ may be taken high to latch the data outputs and begin TEHEL. Taking either or both $\overline{G1}$ or $\overline{G2}$ high or G3 low will force the output buffers to a high impedance state. The output data may be re-enabled at any time taking $\overline{G1}$ and $\overline{G2}$ low and G3 high. On the falling edge of $\overline{E}$ the data will be unlatched. P should be grounded except when in the programming mode.

HARRIS

HM-6616

PRELIMINARY

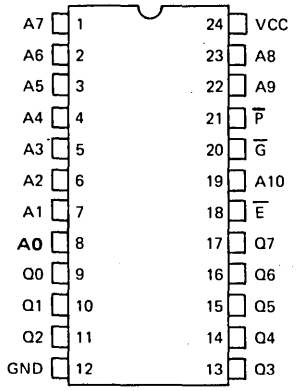
2K x 8 CMOS PROM

Features

- LOW STANDBY AND OPERATING POWER
  - ICCSB – 100μA
  - ICCOP – 13mA/MHz
- FAST ACCESS TIME 175ns
- INDUSTRY STANDARD PINOUT
- SINGLE 5.0 VOLT SUPPLY
- TTL COMPATIBLE INPUTS
- HIGH OUTPUT DRIVE 12 LSTTL LOADS
- SYNCHRONOUS OPERATION
- ON-CHIP ADDRESS LATCHES
- SEPARATE OUTPUT ENABLE
- FULL INDUSTRIAL AND MILITARY TEMPERATURE RANGES

Pinout

TOP VIEW



PIN NAMES

A Address Input
Q Data Output
Ē Chip Enable
Ḡ Output Enable
P̄ Program Enable

Description

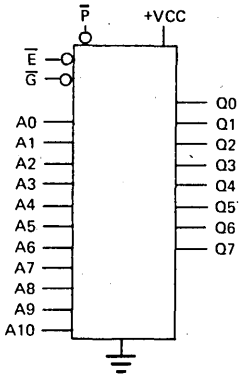
The HM-6616 is a 16,384 bit fuse link CMOS PROM in a 2K word by 8 bit/word format with "Three State" outputs. This PROM is available in the standard 0.600 inch wide DIP.

The HM-6616 utilizes a synchronous design technique. This includes on-chip address latches and a separate output enable control which makes this device ideal for applications utilizing recent generation microprocessors. This design technique, combined with the Harris advanced self-aligned silicon gate CMOS process technology offers ultra-low standby current. Low ICCSB is ideal for battery applications or other systems with low power requirements.

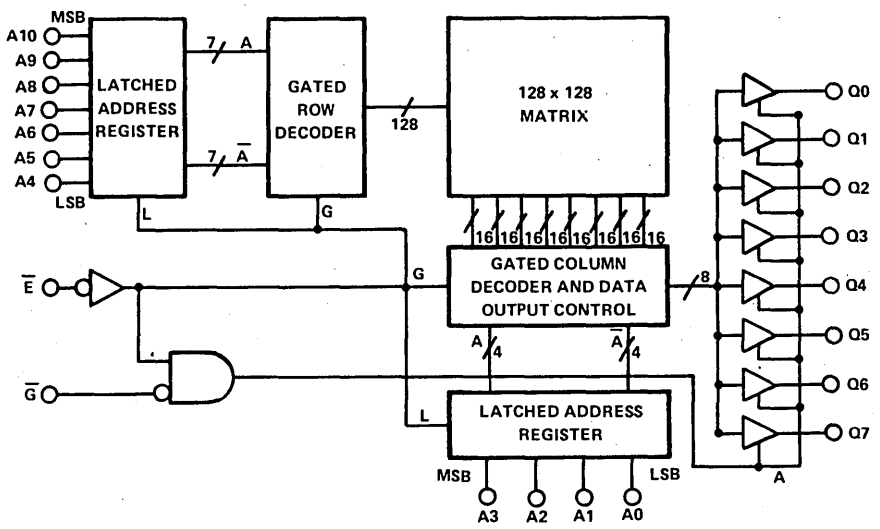
The Harris polysilicon fuse link technology is utilized on this and all other Harris CMOS PROMS. This gives the user a PROM with permanent, stable storage characteristics over the full industrial and military temperature and voltage ranges. Polysilicon fuse technology combined with the low power characteristics of CMOS provides an excellent alternative to standard Bipolar PROMS or NMOS EPROMS.

All bits are manufactured storing a logical "0" and can be selectively programmed for a logical "1" at any bit location.

Logic Symbol



Functional Diagram



ALL LINES POSITIVE LOGIC:
ACTIVE HIGH

THREE STATE BUFFERS:
A HIGH ⟶ OUTPUT ACTIVE

ADDRESS LATCHES AND GATED DECODERS:
LATCH ON RISING EDGE OF L
GATE ON RISING EDGE OF G

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

ABSOLUTE MAXIMUM RATINGS *

Supply Voltage	+8.0 VOLTS
Input/Output Voltage Applied	GND−0.3V to VCC+0.3V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
Military−HM-6616-2/-8	−55°C to +125°C
Industrial−HM-6616-9	−40°C to +85°C
Operating Voltage Range	+4V to +7V

** CAUTION: Stresses above those listed under the "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

D.C. ELECTRICAL CHARACTERISTICS

VCC = 5.0V ± 10%; T_A = Industrial −40°C to +85°C (HM-6616-9)
= Military −55°C to +125°C (HM-6616-2/-8)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	LOGICAL ONE INPUT VOLTAGE	2.4		V	
VIL	LOGICAL ZERO INPUT VOLTAGE		0.8	V	
VOH	LOGICAL ONE OUTPUT VOLTAGE	2.4		V	IOH = − 2.0 mA
VOL	LOGICAL ZERO OUTPUT VOLTAGE		0.4	V	IOL = +4.8 mA
II	INPUT LEAKAGE	−1.0	1.0	μA	OV≤VIN≤VCC
IOZ	OUTPUT LEAKAGE	−1.0	1.0	μA	OV≤VO≤VCC $\overline{G}$ = HIGH
ICCSB	STANDBY POWER SUPPLY CURRENT		100	μA	VIN=VCC or GND VCC = 5.5 V IO = 0
ICCOP	OPERATING POWER SUPPLY CURRENT		13	mA	f = 1 MHz VCC = 5.5 V IO = 0 VIN=VCC or GND
CIN	INPUT CAPACITANCE*		6	pf	f = 1 MHz VIN=VCC or GND
COUT	OUTPUT CAPACITANCE*		10	pf	f = 1 MHz VIN=VCC or GND

*Guaranteed and sampled, but not 100% tested.

A.C. ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%; T_A = Industrial −40°C to +85°C (HM-6616-9)
= Military −55°C to +125°C (HM-6616-2/-8)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
TAVQV	ADDRESS ACCESS TIME		175	ns	see notes 1, 2
TELQV	CHIP ENABLE ACCESS TIME		150	ns	
TELQX	CHIP ENABLE TIME	5		ns	
TAVEL	ADDRESS SETUP TIME	25		ns	
TELAX	ADDRESS HOLD TIME	30		ns	
TELEH	CHIP ENABLE LOW WIDTH	150		ns	
TEHEL	CHIP ENABLE HIGH WIDTH	50		ns	
TELEL	CYCLE TIME	200		ns	
TGLQV	OUTPUT ACCESS TIME		75	ns	
TGLQX	OUTPUT ENABLE TIME	5		ns	
TGHQZ	OUTPUT DISABLE TIME		75	ns	
TEHQZ	CHIP ENABLE DISABLE TIME		75	ns	

NOTE 1: All A.C. parameters tested at worst case limits and per test circuits and definitions in Figures 1 and 2.
NOTE 2: Input test signals must switch between OV and 3.0V. Input rise and fall times must be ≤20 ns.

Switching Waveforms

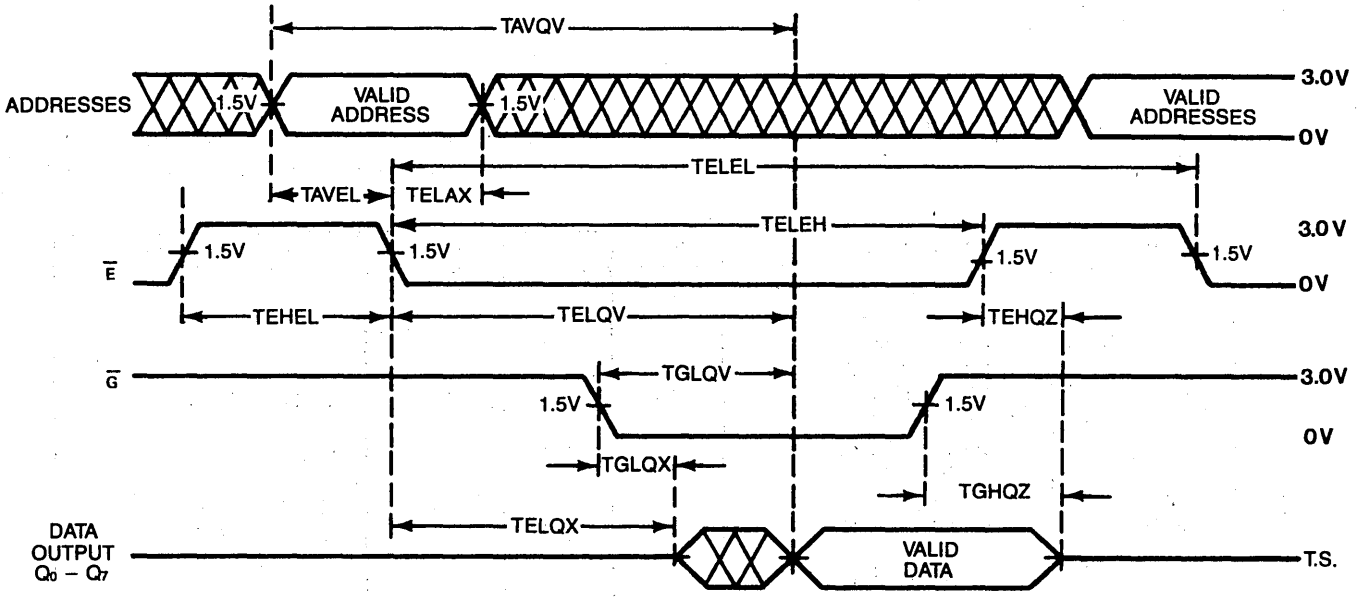


FIGURE 1
READ CYCLE

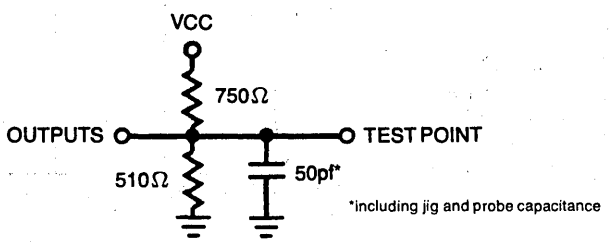


FIGURE 2
OUTPUT TEST CIRCUIT

HITACHI Memory Products Quick Reference Chart

TYPICAL CHARACTERISTICS

MOS RAM									Package *				
Type No.	Process	Number of bits	Organization	Mode	Access Time (ns) max.	Cycle Time (ns) min.	Supply Voltage (V)	Typ. Power Dissipation (mW)	Pin No.	C	G	P	Replacement
HM472114A-1	NMOS	4K	1024 × 4	Static	150	150	+5	200	18		o	o	Intel 2114
HM472114A-2					200	200					o	o	Intel 2114
HM472114-3					300	300	+5	200	18		o	o	Intel 2114
HM472114-4					450	450					o	o	Intel 2114
HM4334-3	CMOS				300	460	+5	20	18			o	Harris HM-6514
HM4334-4					450	640						o	
HM6148					70	70	+5	200	18			o	Intel 2148
HM6148-6					85	85						o	Intel 2148
HM6148L					70	70	+5	200	18			o	Intel 2148
HM6148L-6					85	85						o	Intel 2148
HM4315			4096 × 1		450	640	+5	20	18			o	
HM6147					70	70	+5	75	18		o	o	Intel 2147
HM6147-3					55	55					o	o	Intel 2147
HM6147H-45					45	45					o	o	Intel 2147
HM6147H-35					35	35					o	o	Intel 2147
HM6147L					70	70					o	o	Intel 2147
HM6147L-3					55	55					o	o	Intel 2147
HM6147HL-35					45	45					o	o	Intel 2147
HM6147HL-45					35	35					o	o	Intel 2147
HM6167-8		16K	16384 × 1		100	100	+5	150	20		o	o	Intel 2167
HM6167-6					85	85					o	o	Intel 2167
HM6167					70	70					o	o	Intel 2167
HM6167L-8					100	100					o	o	Intel 2167
HM6167L-6					85	85					o	o	Intel 2167
HM6167L					70	70					o	o	Intel 2167
HM6116-4			2048 × 8		200	200	+5	160	24		o	o	
HM6116-3					150	150					o	o	
HM6116-2					120	120					o	o	
HM6116L-2					120	120					o	o	
HM6116L-3					150	150					o	o	
HM6116L-2					200	200					o	o	
HM4716A-1	NMOS	16K	16384 × 1	Dynamic	120	320	+12, +5, −5	350	16		o	o	
HM4716A-2					150	320					o	o	Mostek MK4116-2
HM4716A-3					200	375					o	o	Mostek MK4116-3
HM4716A-4					250	410					o	o	Mostek MK4116-4
HM4816					100	200	+5	250	16	o			Industry Std. Jedec Pinout
HM4864-2		64K	65536 × 1		150	270	+5	170	16	o			
HM4864-3					200	335				o			

Bipolar RAM								Package *				
Type No.	Process	Number of bits	Organization	Output	Access Time (ns) max.	Supply Voltage (V)	Typ. Power Dissipation (mW/bit)	Pin No.	C	G	P	Replacement
HM10414†	ECL	256	256 × 1	Open Emitter	10	−5.2	2.8	16		o		Fairchild F10414
HM10414-1†					8		2.8	16		o		
HM10422†		1K	256 × 4		10		0.8	24		o		Fairchild F10422
HM100422†					10	−4.5	0.8	24		o		Fairchild F100422
HM2110			1024 × 1		35	−5.2	0.5	16		o		Fairchild F10415A
HM2110-1					25		0.5	16		o		
HM2110-2					20		0.5	16		o		
HM2112					10		0.8	16		o		
HM2112-1					8		0.8	16		o		
HM10470†		4K	4096 × 1		25		0.2	18		o		Fairchild F10470
HM10470-1†					15		0.2	18		o		
HM100470					25		0.2	18		o		100470
HM100470-1					15		0.2	18		o		100470A
HM10474			1024 × 4		25		0.2	18		o		10474
HM10474-1					15		0.2	18		o		10474A
HM100474					25		0.2	18		o		100474
HM100474-1					15		0.2	18		o		100474A
HM2510	TTL	1K	1024 × 1	Open Collector	70	+5.0	0.5	16		o		
HM2510-1					45		0.5	16		o		Fairchild 93415
HM2510-2					35		0.5	16		o		Fairchild 93415A
HM2511				3-state	70		0.5	16		o		
HM2511-1					45		0.5	16		o		Fairchild 93425

MOS ROM	TYPICAL CHARACTERISTICS OF READ ONLY MEMORIES				Access Time (ns) max.	Supply Voltage (V)	Typ. Power Dissipation (mW)	Package				
Type No.	Program	Number of bits	Organization	Process				Pin No.	C	G	P	Replacement
HN462716	UV Erasable and Electrically Programmable	16K	2048 × 8	NMOS	450	+5	310	24	o	o		Intel 2716
HN462532		32K	4096 × 8		450		450	24	o	o		TI TMS2532
HN462732								24	o	o		Intel 2732
HN482764-4	UV Erasable and Elect. Programmable	64K	8182 × 8		450		500	28	o			Intel 2764
HN48016	Electrically Erasable and Programmable	16K	2048 × 8		350		160	24			o	

*The package codes of C,G, and P are applied to the package materials as follows: C-Ceramic with Lid, G-Glass-Sealed Ceramic, P-Plastic. †-Preliminary.

HITACHI
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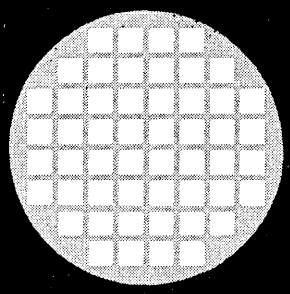
1800 Bering Drive, San Jose, CA 95112 (408) 292-6404



inmos

High Performance 16K Static RAM

IMS1400
IMS1400L 16Kx1

IMS1420
IMS1420L
IMS1421 4Kx4

Features
- Single 5V ±10% supply
- $\overline{E}$(CE) power down function
- TTL compatible inputs and output
- Fully static—no clocks for timing
- Three-state output
- 20-pin, 300 mil DIP, and 20-pin chip carrier (high system packing densities)

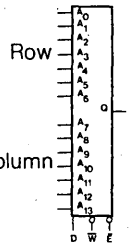
IMS1400
- 45 and 55ns Chip Enable access
- Maximum active power 660mW
- Low power standby mode 110mW Max

IMS1400L
- 70 and 100ns Chip Enable access
- Maximum active power 495mW
- Maximum standby power 83mW

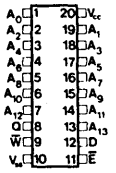
Pin Names

A_0-A_{13}	Address Inputs	V_{CC}	Power (+5V)
$\overline{W}$	Write Enable	V_{SS}	Ground
$\overline{E}$	Chip Enable		
D	Data Input		
Q	Data Output		

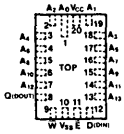
Logic Symbol



Pin Configuration

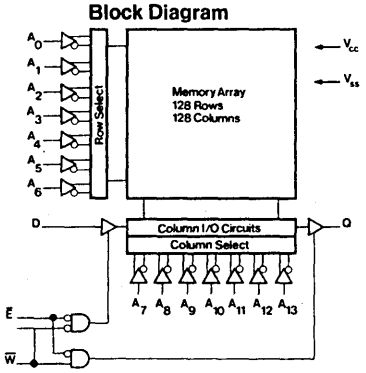


DIP



Chip Carrier

Block Diagram



Features
- 4K x 4 bit Organization
- Fully TTL compatible
- Common data inputs and outputs
- Single +5V ±10% Operation

IMS1420
- 45 and 55ns Chip Enable access
- Power down function
- 40 and 50ns address access
- 605mW Maximum active power
- 165mW Maximum standby power

IMS1420L
- 70 and 100ns Chip Enable access
- Maximum active power 495mW
- Maximum standby power 83mW

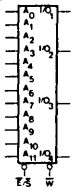
IMS1421
- High speed Chip Select function
- 30 and 40ns Chip Select access
- 40 and 50ns address access
- 605mW Maximum active power

- Three-state outputs
- Fully static, no clocks for timing
- 20-pin 300-mil DIP, and 20-pin chip carrier (high system packing densities)

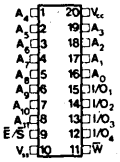
Pin Names

A_0-A_{11}	Address Inputs	V_{CC}	Power (+5V)
$\overline{W}$	Write Enable	V_{SS}	Ground
$\overline{E}$	Chip Enable		
$\overline{S}$	Chip Select		
I/O	Date In/Out		

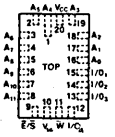
Logic Symbol



Pin Configuration

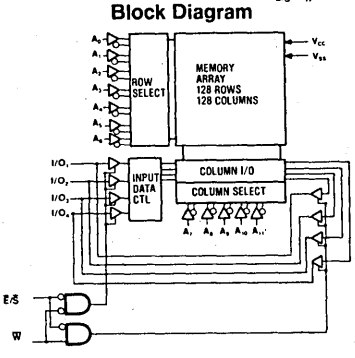


DIP



Chip Carrier

Block Diagram



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High Performance 16K Static RAM (MIL-STD 883B)

IMS1400M 16Kx1

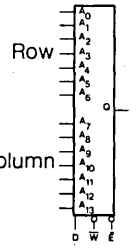
Features

- Specifications guaranteed over full military temperature range (−55°C to 125°C)
- MIL-STD 883B Processing
- 55 and 70ns Chip Enable Access
- Maximum Active Power 660mW
- Maximum Standby Power 165mW
- Single +5V ± 10% Supply
- $\overline{E}$ Power Down Function
- TTL Compatible Inputs and Output
- Fully Static—No Clocks for Timing
- Three-State Output

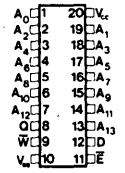
Pin Names

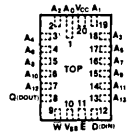
A_0-A_{13}	Address Inputs	V_{CC}	Power (+5V)
$\overline{W}$	Write Enable	V_{SS}	Ground
$\overline{E}$	Chip Enable		
D	Data Input		
Q	Data Output		

Logic Symbol



Pin Configuration





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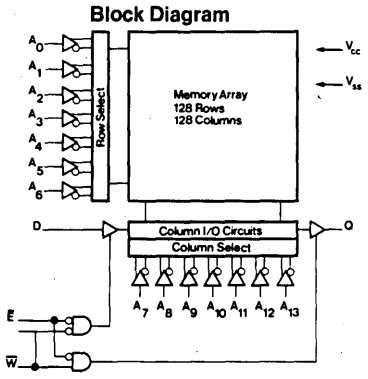


IMS1420M 4Kx4

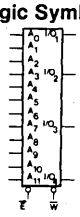
Features

- Specifications guaranteed over full military temperature range (−55°C to 125°C)
- MIL-STD 883B Processing
- 4K x 4 Bit Organization
- 55 and 70ns Address Access
- 660mW Maximum Power Dissipation
- Fully TTL Compatible
- Common Data Inputs & Outputs
- Single +5V ± 10% Operation
- 55 and 70ns Chip Enable Access
- Power Down Function
- 165mW Maximum Standby Power

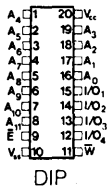
Pin Names

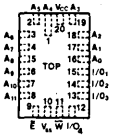
A_0-A_{11}	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{W}$	WRITE ENABLE	V_{SS}	GROUND
$\overline{E}$	CHIP ENABLE		
I/O	DATA IN/OUT		

Logic Symbol

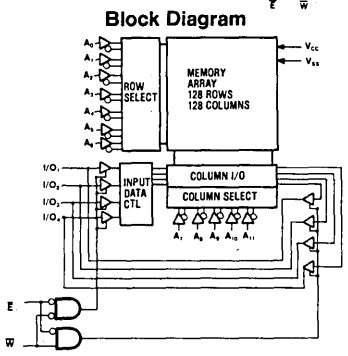


Pin Configuration





Block Diagram



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High Performance 64K Dynamic RAM

inmos

IMS2600 64Kx1

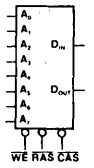
Features

- High Speed, $\overline{RAS}$ Access of 100 and 120ns
- Cycle Times of 160 and 190ns
- Low Power:
  22mW Standby
  303mW Active (350ns Cycle Time)
  413mW Active (190ns Cycle Time)
- Single +5V ± 10% Power Supply
- On-Chip refresh using $\overline{CAS}$-before-$\overline{RAS}$, Pin 1 left as N/C for 256K expansion
- Indefinite D_{OUT} Hold Under $\overline{CAS}$ Control
- Industry Standard 16 Pin Configuration
- Nibble-Mode Capability (High Speed 4 Bit Serial Mode)
- 4ms/256 Cycle Refresh
- All Inputs and Output TTL Compatible
- Read, Write and Read-Modify-Write Capability on Single Bit and in Nibble Mode
- $\overline{RAS}$-Only Refresh Capability
- Common I/O Capability using "Early-Write"

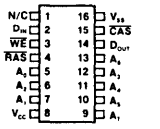
Pin Names

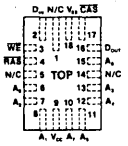
A_0-A_7	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{RAS}$	ROW ADDRESS STROBE
D_{IN}	DATA IN
D_{OUT}	DATA OUT
$\overline{WE}$	WRITE ENABLE
V_{CC}	+5 VOLT SUPPLY INPUT
V_{SS}	GROUND

Logic Symbol

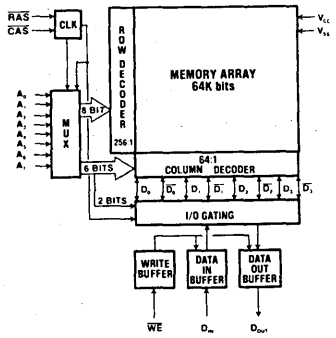


Pin Configuration





Block Diagram



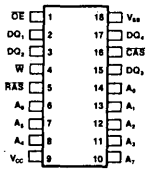
IMS2620* 16Kx4

*No Page Mode Operation

Features

- 16K x 4 Organization
- High Speed, $\overline{RAS}$ Access of 100, 120 and 150ns
- Cycle Times of 160, 190 and 230ns
- Low Power
  22mW Standby
  303mW Active (350ns Cycle Time)
  413mW Active (190ns Cycle Time)
- Common I/O
- Single +5V ± 10% Power Supply
- On-Chip Refresh Assist using $\overline{CAS}$-before-$\overline{RAS}$
- Multiplexed Addresses 8 Row, 6 Column
- 18 Pin Package—JEDEC Std. Pinout
- All Inputs and Outputs TTL Compatible
- Output Enable ($\overline{OE}$) Control for Greater Timing Flexibility
- 4ms/256 Cycle Refresh
- Read, Write and Read-Modify-Write Capability
- 25 MBit Data Rate

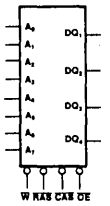
Pin Configuration



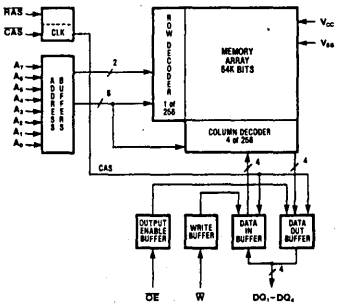
Pin Names

A_0 - A_7	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{RAS}$	ROW ADDRESS STROBE
DQ_1 - DQ_4	DATA IN/DATA OUT
$\overline{OE}$	OUTPUT ENABLE
$\overline{W}$	WRITE ENABLE
V_{CC}	+5V SUPPLY
V_{SS}	GROUND

Logic Symbol



Block Diagram



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Integrated Device Technology, Inc.

CMOS STATIC RAMS 16K (2K x 8 BIT)

IDT6116S
IDT6116L

MILITARY / INDUSTRIAL / COMMERCIAL TEMPERATURE RANGES

FEATURES:

- High-speed (equal access and cycle time)
  - —MILITARY/INDUSTRIAL
    - IDT6116S 90/120/150 ns (max.)
    - IDT6116L 90/120/150 ns (max.)
  - —COMMERCIAL
    - IDT6116S 70/90/120 ns (max.)
    - IDT6116L 90/120/150 ns (max.)
- Low power consumption

IDT6116S	IDT6116L
Active: 180 mW (Typ.)	Active: 160 mW (Typ.)
Standby: 100 μW (Typ.)	Standby: 20 μW (Typ.)

- Battery backup operation — 2V data retention voltage
- Produced with advanced CEMOS™ I high-performance technology
- CEMOS™ I process virtually eliminates alpha particle soft-error rates (with no organic die coatings)
- Single 5V (±10%) power supply
- Input and output directly TTL compatible
- Three-state output
- Static operation: no clocks or refresh required
- Standard 24-pin dual-in-line ceramic sidebrazed package or 28-pin and 32-pin LCC
- Pin compatible with standard 16K static RAM and EPROM
- Standard product 100% screened to MIL-STD-883, Class C
- Military product available 100% screened to Class B

DESCRIPTION:

The IDT6116 is a 16,384-bit high-speed static RAM organized as 2K x 8. It is fabricated using IDT's high-performance, high-reliability technology—CEMOS™ I. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective alternative to bipolar and fast NMOS memories.

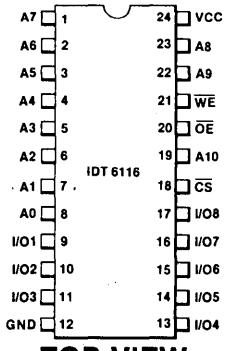
Access times as fast as 70ns are available with maximum power consumption of only 550mW. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a standby power mode as long as $\overline{CS}$ remains high. In the standby mode, the low power device consumes less than 20μW typically. This capability provides significant system level power and cooling savings. Both versions also offer a battery backup data retention capability where the circuit typically consumes only 1 μW to 4 μW operating off of a 2V battery.

All inputs and outputs of the IDT6116 are TTL compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation, providing equal access and cycle times for ease of use.

The IDT6116 is packaged in either a 24-pin, 600 mil-DIP or 32-pin and 28-pin leadless chip carriers, providing high board-level packing densities.

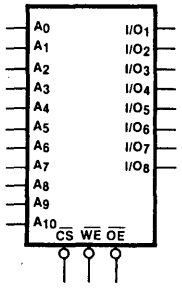
The IDT6116 Military RAM is 100% processed in compliance to the test methods of MIL-STD-883, Method 5004, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATION

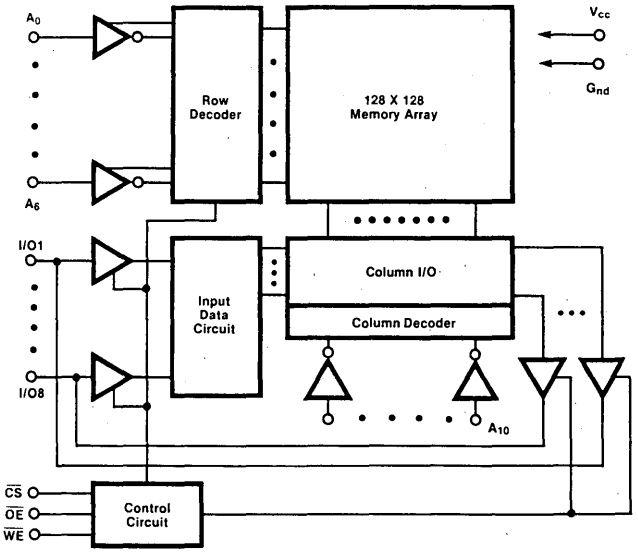


TOP VIEW

LOGIC SYMBOL



FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_0-A_{10}	ADDRESS	$\overline{WE}$	WRITE ENABLE
I/O1-I/O8	DATA INPUT/OUTPUT	$\overline{OE}$	OUTPUT ENABLE
$\overline{CS}$	CHIP SELECT	GND	GROUND
V_{CC}	POWER		

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ABSOLUTE MAXIMUM RATINGS[1]

TEMPERATURE RANGE		−55°C to +125°C	−40°C to +85°	0°C to +70°C	
SYMBOL	PARAMETER	RATING			UNIT
V_{TERM}	Voltage on any Pin with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	−0.5 to +7.0	V
T_A	Operating Temperature	−55 to +125	−40 to +85	0 to +70	°C
T_{BIAS}	Temperature Under Bias	−65 to +135	−55 to +125	−55 to +125	°C
T_{STG}	Storage Temperature	−65 to +150	−65 to +150	−10 to +85	°C
P_T	Power Dissipation	1.0	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	50	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.5	6.0	V
V_{IL}	Input Low Voltage	−1.0*	—	+0.8	V
C_L	Output Load	—	—	100	pF
TTL	Output Load	—	—	1	—

*Pulse Width: 50ns, DC: V_{IL} min. = −0.3V.

MILITARY (T_A = −55°C to +125°C)
INDUSTRIAL (T_A = −40°C to +85°C)
COMMERCIAL (T_A = 0°C to +70°C)

IDT6116S DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V ±10%, T_A= −55°C to +125°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT6116S90/120			IDT6116S150			UNIT
			MIN.	TYP.[1]	MAX.	MIN.	TYP.[1]	MAX.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = GND to V_{CC}	—	—	10	—	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = GND to V_{CC}	—	—	10	—	—	10	µA
I_{CC}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA	—	40	100	—	35	90	mA
I_{CC1}		V_{IH} = 3.5V, V_{IL} = 0.6V $I_{I/O}$ = 0mA	—	35	—	—	30	—	mA
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle = 100%	—	40	100	—	35	90	mA
I_{SB}	Standby Power Current	$\overline{CS}$ = V_{IH}	—	5	25	—	5	25	mA
I_{SB1}		$\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V	—	0.02	10	—	0.02	10	mA
V_{OL}	Output Low Voltage	I_{OL} = 3.5mA[2]	—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = −1.0mA	2.4	—	—	2.4	—	—	V

1. V_{CC} = 5V, T_A = 25°C
2. I_{OL} = 2.1mA for IDT6116S150

IDT6116L DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V ±10%, T_A= −55°C to +125°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT6116L90/120			IDT6116L150			UNIT
			MIN.	TYP.[1]	MAX.	MIN.	TYP.[1]	MAX.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = GND to V_{CC}	—	—	5	—	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = GND to V_{CC}	—	—	5	—	—	5	µA
I_{CC}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA	—	40/35	100/90	—	30	80	mA
I_{CC1}		V_{IH} = 3.5V, V_{IL} = 0.6V $I_{I/O}$ = 0mA	—	35/30	—	—	30	—	mA
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle = 100%	—	40/35	100/90	—	30	80	mA
I_{SB}	Standby Power Current	$\overline{CS}$ = V_{IH}	—	5	20	—	5	15	mA
I_{SB1}		$\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V	—	4	900	—	4	900	µA
V_{OL}	Output Low Voltage	I_{OL} = 3.5mA[2]	—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = −1.0mA	2.4	—	—	2.4	—	—	V

1. V_{CC} = 5V, T_A = 25°C
2. I_{OL} = 2.1mA for IDT6116L150

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IDT6116S DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, T_A = −40°C to +85°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT6116S90/120 MIN.	IDT6116S90/120 TYP.(1)	IDT6116S90/120 MAX.	IDT6116S150 MIN.	IDT6116S150 TYP.(1)	IDT6116S150 MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = GND to V_{CC}	—	—	10	—	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = GND to V_{CC}	—	—	10	—	—	10	µA
I_{CC}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA	—	40	90	—	35	80	mA
I_{CC1}		V_{IH} = 3.5V, V_{IL} = 0.6V $I_{I/O}$ = 0mA	—	35	—	—	30	—	mA
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle = 100%	—	40	90	—	35	80	mA
I_{SB}	Standby Power Current	$\overline{CS}$ = V_{IH}	—	5	20	—	5	20	mA
I_{SB1}		$\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V	—	20	2000	—	20	2000	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA(2)	—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = −1.0mA	2.4	—	—	2.4	—	—	V

1. V_{CC} = 5V, T_A = 25°C
2. I_{OL} = 2.1mA for IDT6116S150

IDT6116L DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, T_A = −40°C to +85°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT6116L90/120 MIN.	IDT6116L90/120 TYP.(1)	IDT6116L90/120 MAX.	IDT6116L150 MIN.	IDT6116L150 TYP.(1)	IDT6116L150 MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = GND to V_{CC}	—	—	2	—	—	2	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = GND to V_{CC}	—	—	2	—	—	2	µA
I_{CC}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA	—	40/35	90/80	—	30	70	mA
I_{CC1}		V_{IH} = 3.5V, V_{IL} = 0.6V $I_{I/O}$ = 0mA	—	35/30	—	—	30	—	mA
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle = 100%	—	40/35	90/80	—	30	70	mA
I_{SB}	Standby Power Current	$\overline{CS}$ = V_{IH}	—	5	20/15	—	4	12	mA
I_{SB1}		$\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V	—	4	200	—	4	200	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA(2)	—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = −1.0mA	2.4	—	—	2.4	—	—	V

1. V_{CC} = 5V, T_A = 25°C
2. I_{OL} = 2.1mA for IDT6116L150

IDT6116S DC CHARACTERISTICS (Vcc = 5V ±10%, Gnd = 0V, T^A = 0°C to +70°C)

SYMBOL	ITEM	TEST CONDITIONS	IDT6116S 70 MIN.	IDT6116S 70 TYP.(1)	IDT6116S 70 MAX.	IDT6116S 90/120 MIN.	IDT6116S 90/120 TYP.*	IDT6116S 90/120 MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = GND to V_{CC}	—	—	10	—	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = GND to V_{CC}	—	—	10	—	—	10	µA
I_{CC}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA	—	50	100	—	40	80	mA
I_{CC1}		V_{IH} = 3.5V, V_{IL} = 0.6V $I_{I/O}$ = 0mA	—	40	—	—	35	—	mA
I_{CC2}	Average Operating Current	Min. Cycle Duty = 100%	—	50	100	—	40	80	mA
I_{SB}	Standby Power Current	$\overline{CS}$ = V_{IH}	—	5	15	—	5	15	mA
I_{SB1}		$\overline{CS}$ ≥ V_{CC} −0.2V, V_{IN} ≥ V_{CC} −0.2V or V_{IN} ≤ 0.2V	—	20	2000	—	20	2000	µA
V_{OL}	Output Voltage	I_{OL} = 4mA	—	—	0.4	—	—	0.4	V
V_{OH}		I_{OH} = −1.0mA	2.4	—	—	2.4	—	—	V

1. V_{CC} = 5V, T_A = 25°C

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IDT6116L DC CHARACTERISTICS (V_{CC} = 5V ±10%, GND = 0V, T_A = 0°C to +70°C)

SYMBOL	ITEM	TEST CONDITIONS	IDT6116L 90 MIN.	IDT6116L 90 TYP.[1]	IDT6116L 90 MAX.	IDT6116L 120/150 MIN.	IDT6116L 120/150 TYP.[1]	IDT6116L 120/150 MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = GND to V_{CC}	—	—	2	—	—	2	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = GND to V_{CC}	—	—	2	—	—	2	µA
I_{CC}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA	—	40	80	—	35/30	70/60	mA
I_{CC1}		V_{IH} = 3.5V, V_{IL} = 0.6V $I_{I/O}$ = 0mA	—	35	—	—	30	—	mA
I_{CC2}	Average Operating Current	Min. Cycle Duty = 100%	—	40	80	—	35/30	70/60	mA
I_{SB}	Standby Power Current	$\overline{CS}$ = V_{IH}	—	5	15	—	4	12	mA
I_{SB1}		$\overline{CS} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	—	4	100	—	4	100	µA
V_{OL}	Output Voltage	I_{OL} = 4mA[2]	—	—	0.4	—	—	0.4	V
V_{OH}		I_{OH} = −1.0mA	2.4	—	—	2.4	—	—	V

1. V_{CC} = 5V, T_A = 25°C 2. I_{OL} = 2.1mA for IDT6116L 150

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = −55°C to +125°C/−40°C to +85°C/0°C to +70°C)[1]

SYMBOL	PARAMETER	[2] IDT616S70 MIN.	IDT616S70 MAX.	IDT6116S90 IDT6116L90 MIN.	IDT6116S90 IDT6116L90 MAX.	IDT6116S120 IDT6116L120 MIN.	IDT6116S120 IDT6116L120 MAX.	IDT6116S150 IDS6116L150 MIN.	IDT6116S150 IDS6116L150 MAX.	UNIT
READ CYCLE										
t_{RC}	Read Access Time	70	—	90	—	120	—	150	—	ns
t_{AA}	Address Access Time	—	70	—	90	—	120	—	150	ns
t_{ACS}	Chip Select Access Time	—	70	—	90	—	120	—	150	ns
t_{CLZ}	Chip Selection to Output in Low Z	5	—	0/0/5	—	5/5/10	—	10/15[3]	—	ns
t_{OE}	Output Enable to Output Valid	—	50	—	65	—	80	—	100	ns
t_{OLZ}	Output Enable to Output in Low Z	5	—	0/0/5	—	5/5/10	—	10/15[3]	—	ns
t_{CHZ}	Chip Deselection to Output in High Z	0	35	0	40	0	40	0	50	ns
t_{OHZ}	Output Disable to Output in High Z	0	35	0	40	0	40	0	50	ns
t_{OH}	Output Hold from Address Change	5	—	0/0/5	—	5/5/10	—	10/15[3]	—	na
WRITE CYCLE										
t_{WC}	Write Cycle Time	70	—	90	—	120	—	150	—	ns
t_{CW}	Chip Selection to End of Write	40	—	55	—	70	—	90	—	ns
t_{AW}	Address Valid to End of Write	65	—	80	—	105	—	120	—	ns
t_{AS}	Address Setup Time	15	—	15	—	20	—	20	—	ns
t_{WP}	Write Pulse Width	40	—	55	—	70	—	90	—	ns
t_{WR}	Write Recovery Time	5	—	10/5/5	—	10/5/5	—	10	—	ns
t_{OHZ}	Output Disable to Output in High Z	0	35	0	40	0	40	0	50	ns
t_{WHZ}	Write to Output in High Z	0	40	0	50	0	50	0	60	ns
t_{DW}	Data to Write Time Overlap	30	—	30	—	35	—	40	—	ns
t_{DH}	Data Hold from Write Time	5	—	10/10/5	—	10/10/5	—	10	—	ns
t_{OW}	Output Active from End of Write	0	—	0	—	0/5/5	—	5/10[4]	—	ns

1. Parameters listing three limits apply in this Temp. Range order: Military/Industrial/Commercial. All other limits apply to all three Temp. Ranges.
2. IDT6116S70 available in Commercial 0°C to 70°C only.
3. 10ns applies over −55°C to +125°C and −40°C to +85°C; 15ns applies over 0°C to +70°C.
4. t_{OW} = 5ns over −55°C to +125°C; t_{OW} = 10ns over −40°C to +85°C and 0°C to +70°C.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	1 TTL Gate and C_L=100pF (including scope and jig)

***Including scope and jig.**

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TRUTH TABLE

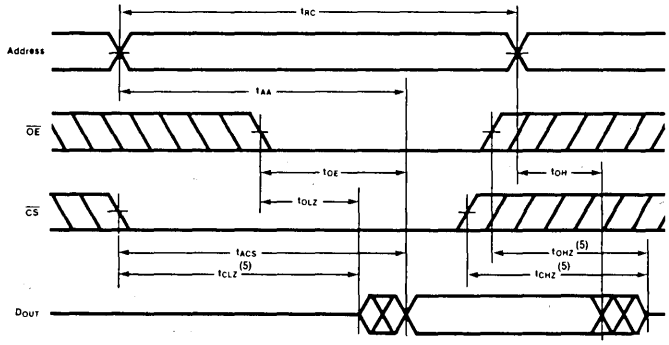
MODE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O OPERATION
Standby	H	X	X	High Z
Read	L	L	H	D_{OUT}
Read	L	H	H	High Z
Write	L	X	L	D_{IN}

CAPACITANCE[1] ($T_A = 25°C$, f = 1.0MHz)

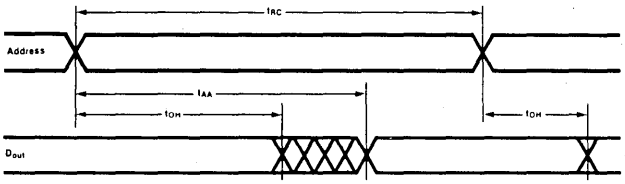
SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O} = 0V$	8	pF

1. This parameter is sampled and not 100% tested.

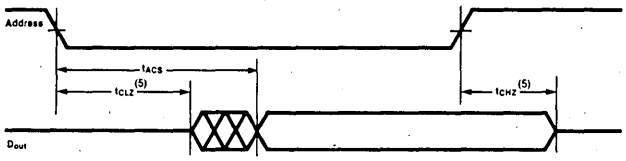
TIMING WAVEFORMS OF READ CYCLE NO. 1[1]



READ CYCLE 2[1,2,4]

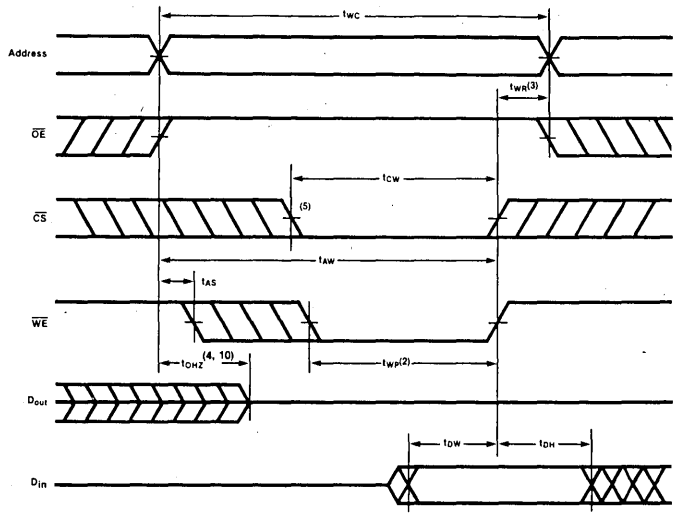


READ CYCLE 3[1,3,4]



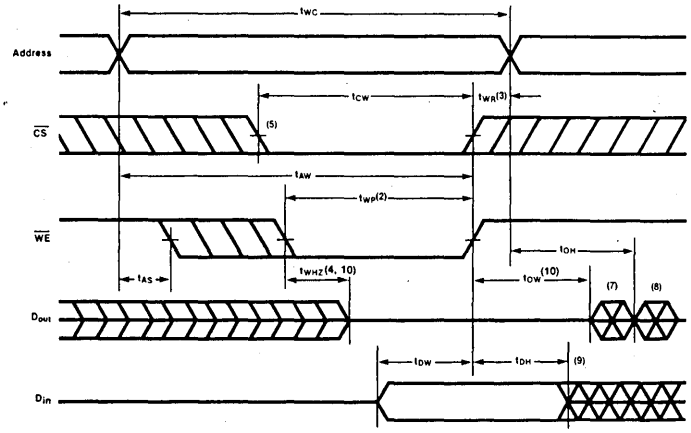
NOTES: 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

TIMING WAVEFORMS OF WRITE CYCLE 1[1]



NOTE: See footnotes on next page.

TIMING WAVEFORM OF WRITE CYCLE 2[1,6]



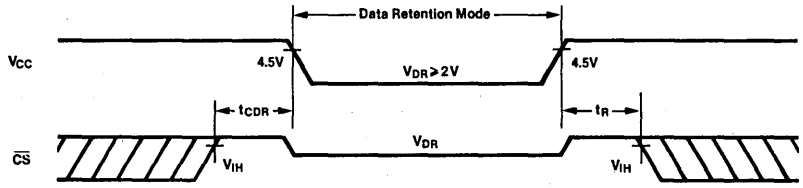
NOTES:
1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{CE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

DATA RETENTION CHARACTERISTICS
(T_A = −55°C to +125°C/−40°C to +85°C/0°C to 70°C)

SYMBOL	PARAMETER	TEST CONDITIONS		IDT6116L MIN.	IDT6116L TYP.[1]	IDT6116L MAX.	IDT6116S MIN.	IDT6116S TYP.[1]	IDT6116S MAX.	UNIT
V_{DR}	V_{CC} for Retention Data	V_{CC} = 2.0V, $\overline{CS} \geqslant V_{CC}-0.2V$ $V_{IN} \geqslant V_{CC}-0.2V$ or $V_{IN} \leqslant 0.2V$		2.0	—	—	2.0	—	—	V
I_{CCDR}	Data Retention Current		COM'L	—	0.5	20	—	2	400	µA
			IND	—	0.5	40	—	2	600	µA
			MIL	—	0.5	300	—	2	1000	µA
t_{CDR}	Chip Deselect to Data Retention Time			0	—	—	0	—	—	ns
t_R	Operation Recovery Time			t_{RC}[2]	—	—	t_{RC}[2]	—	—	ns

1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time

LOW V_{CC} DATA RETENTION WAVEFORM



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Integrated Device Technology, Inc.

CMOS STATIC RAMS 16K (16K x 1 BIT)

IDT6167S
IDT6167L

MILITARY / COMMERCIAL TEMPERATURE RANGES

FEATURES:

- High-speed (equal access and cycle time)
  - —MILITARY
    - IDT6167S 55/70/85/100ns (max.)
    - IDT6167L 55/70/85/100ns (max.)
  - —COMMERCIAL
    - IDT6167S 45/55/70/85ns (max.)
    - IDT6167L 45/55/70/85ns (max.)
- Low power consumption

IDT6167S	IDT6167L
Active: 150mW (typ.)	Active: 125mW (typ.)
Standby: 100μW (typ.)	Standby: 10μW (typ.)

- Battery backup operation — 2V data retention voltage (IDT6167L only)
- High-density 20-pin dual-in-line package and 20-pin leadless chip carriers
- Produced with advanced CEMOS™ I high-performance technology
- CEMOS™ I process virtually eliminates alpha particle soft-error rates (with no organic die coatings)
- Separate data input and output
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Pin-compatible with standard 16K x 1 static RAMs
- Standard product 100% screened to MIL-STD-883 Class C
- Military product available 100% screened to Class B

DESCRIPTION:

The IDT6167 is a 16,384-bit high-speed static RAM organized as 16K x 1. It is fabricated using IDT's high-performance, high-reliability technology — CEMOS™ I. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective alternative to bipolar and fast NMOS memories.

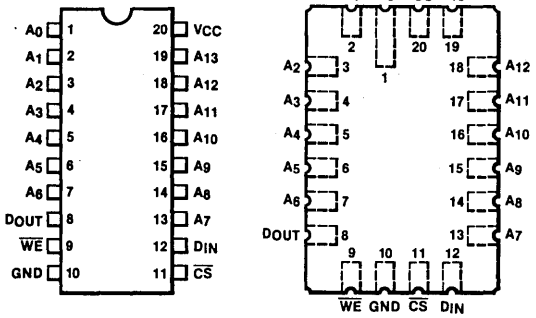
Access times as fast as 45ns are available with maximum power consumption of only 330mW. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a standby mode as long as $\overline{CS}$ remains high. In the standby mode, the device consumes less than 100μW, typically. This capability provides significant system-level power and cooling savings. The low power, (L), version also offers a battery backup data retention capability where the circuit typically consumes only 1μW operating off of a 2V battery.

All inputs and the output of the IDT6167 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Fully static asynchronous circuitry is used, which requires no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

The IDT6167 is packaged in either a space-saving 20-pin, 300 mil DIP or 20-pin leadless chip carrier, providing high board-level packing densities.

The IDT6117 Military RAM is 100% processed in compliance to the test methods of MIL-STD-883, Method 5004, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATIONS



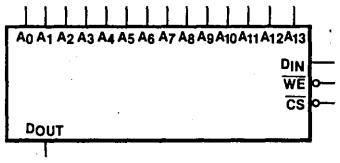
LCC
Top View

PIN NAMES

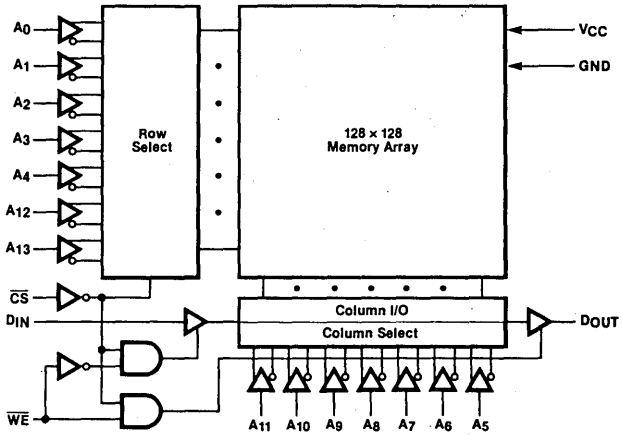
A_0-A_{13}	ADDRESS INPUTS	D_{IN}	DATA IN
$\overline{CS}$	CHIP SELECT	D_{OUT}	DATA OUT
$\overline{WE}$	WRITE ENABLE	GND	GROUND
V_{CC}	POWER		

CEMOS is a trademark of Integrated Device Technology, Inc.

LOGIC SYMBOL



FUNCTIONAL BLOCK DIAGRAM



IDT6167S/IDT6167L CMOS STATIC RAMS 16K (16K x 1 BIT)

Integrated Device Technology

MEMORY

ABSOLUTE MAXIMUM RATINGS[1]

TEMPERATURE RANGE		−55°C to +125°C	0°C to +70°C	
SYMBOL	RATING	VALUE		UNIT
V_{TERM}	Terminal Voltage with Respect to GND	−0.5 to +7.0	−0.5 to +7.0	V
T_A	Operating Temperature	−55 to +125	0 to +70	°C
T_{BIAS}	Temperature Under Bias	−65 to +135	−55 to +125	°C
T_{STG}	Storage Temperature	−65 to +150	−65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	20	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = −55°C to +125°C/0°C to +70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	−0.5	—	0.8	V

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = −55°C to +125°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT6167S			IDT6167L			UNIT
			MIN.	TYP.[1]	MAX.	MIN.	TYP.[1]	MAX.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	—	10	—	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	—	10	—	—	5	µA
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, Output Open	—	30	60	—	25	50	mA
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle = 100%	—	30	60	—	25	50	mA
I_{SB}	Standby Power Supply Current	$\overline{CS} \geq V_{IH}$	—	5	20	—	5	20	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS} \geq V_{CC}$ −0.2V $V_{IN} \geq V_{CC}$ −0.2V or ≤ 0.2V	—	0.02	10	—	0.002	0.9	mA
V_{OL}	Output Low Voltage	I_{OL} = 8mA	—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4mA	2.4	—	—	2.4	—	—	V

1. V_{CC} = 5V, T_A = 25°C

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0 to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT6167S			IDT6167L			UNIT
			MIN.	TYP.[1]	MAX.	MIN.	TYP.[1]	MAX.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	—	2	—	—	2	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	—	2	—	—	2	µA
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, Output Open	—	30	60	—	25	50	mA
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle = 100%	—	30	60	—	25	50	mA
I_{SB}	Standby Power Supply Current	$\overline{CS} \geq V_{IH}$	—	5	20	—	5	20	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS} \geq V_{CC}$ −0.2V $V_{IN} \geq V_{CC}$ −0.2V or ≤ 0.2V	—	20	2000	—	2	50	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA	—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4mA	2.4	—	—	2.4	—	—	V

1. V_{CC} = 5V, T_A = 25°C

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	D Out	Active
Write	L	L	High Z	Active

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

SYMBOL	ITEM	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	6	pF

NOTE: This parameter is sampled and not 100% tested.

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AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = −55°C to +125°C unless otherwise noted.)

SYMBOL		PARAMETER	IDT6167S55 IDT6167L55 MIN.	MAX.	IDT6167S70 IDT6167L70 MIN.	MAX.	IDT6167S85 IDT6167L85 MIN.	MAX.	IDT6167S100 IDT6167L100 MIN.	MAX.	UNIT
READ CYCLE											
t_{RC}	(TAVAV)	Read Cycle Time	55	—	70	—	85	—	100	—	ns
t_{AA}	(TAVQV)	Address Access Time	—	55	—	70	—	85	—	100	ns
t_{ACS}	(TELQV)	Chip Select Access Time	—	55	—	70	—	85	—	100	ns
t_{OH}	(TAXQX)	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
t_{LZ}	(TELQX)	Chip Selection to Output in Low Z	5	—	5	—	5	—	5	—	ns
t_{HZ}	(TEHQZ)	Chip Deselection to Output in High Z	0	40	0	40	0	50	0	50	ns
t_{PU}	(TELICCH)	Chip Selection to Power Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}	(TEHICCL)	Chip Deselection to Power Down Time	—	55	—	70	—	85	—	100	ns
WRITE CYCLE											
t_{WC}	(TAVAV)	Write Cycle Time	55	—	70	—	85	—	100	—	ns
t_{CW}	(TELWH)	Chip Selection to End of Write	45	—	55	—	65	—	80	—	ns
t_{AW}	(TAVWH)	Address Valid to End of Write	45	—	55	—	65	—	80	—	ns
t_{AS}	(TAVWL)	Address Setup Time	0	—	0	—	0	—	0	—	ns
t_{WP}	(TWLWH)	Write Pulse Width	35	—	40	—	45	—	55	—	ns
t_{WR}	(TWHAX)	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	(TDVWH)	Data Valid to End of Write	25	—	30	—	35	—	40	—	ns
t_{DH}	(TWHDX)	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{WZ}	(TWLQZ)	Write Enable to Output in High Z	0	40	0	40	0	50	0	50	ns
t_{OW}	(TWHQX)	Output Active from End of Write	0	—	0	—	0	—	0	—	ns

AC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0 to +70°C) unless otherwise noted.)

SYMBOL		PARAMETER	IDT6167S45 IDT6167L45 MIN.	MAX.	IDT6167S55 IDT6167L55 MIN.	MAX.	IDT6167S70 IDT6167L70 MIN.	MAX.	IDT6167S85 IDT6167L85 MIN.	MAX.	UNIT
READ CYCLE											
t_{RC}	(TAVAV)	Read Cycle Time	45	—	55	—	70	—	85	—	ns
t_{AA}	(TAVQV)	Address Access Time	—	45	—	55	—	70	—	85	ns
t_{ACS}	(TELQV)	Chip Select Access Time	—	45	—	55	—	70	—	85	ns
t_{OH}	(TAXQX)	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
t_{LZ}	(TELQX)	Chip Selection to Output in Low Z	5	—	5	—	5	—	5	—	ns
t_{HZ}	(TEHQZ)	Chip Deselection to Output in High Z	0	30	0	30	0	30	0	40	ns
t_{PU}	(TELICCH)	Chip Selection to Power Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}	(TEHICCL)	Chip Deselection to Power Down Time	—	35	—	35	—	35	—	40	ns
WRITE CYCLE											
t_{WC}	(TAVAV)	Write Cycle Time	45	—	55	—	70	—	85	—	ns
t_{CW}	(TELWH)	Chip Selection to End of Write	40	—	45	—	55	—	65	—	ns
t_{AW}	(TAVWH)	Address Valid to End of Write	40	—	45	—	55	—	65	—	ns
t_{AS}	(TAVWL)	Address Setup Time	0	—	0	—	0	—	0	—	ns
t_{WP}	(TWLWH)	Write Pulse Width	30	—	35	—	40	—	45	—	ns
t_{WR}	(TWHAX)	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	(TDVWH)	Data Valid to End of Write	25	—	25	—	30	—	35	—	ns
t_{DH}	(TWHDX)	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{WZ}	(TWLQZ)	Write Enable to Output in High Z	0	30	0	30	0	30	0	40	ns
t_{OW}	(TWHQX)	Output Active from End of Write	0	—	0	—	0	—	0	—	ns

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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

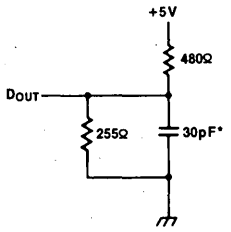


Figure 1. Output Load

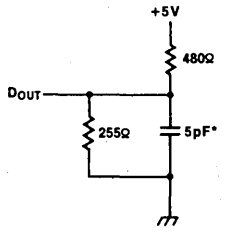
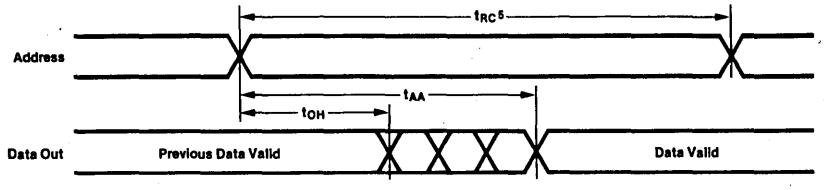


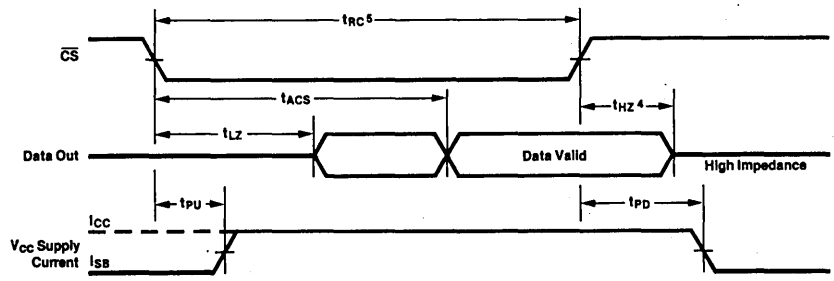
Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

*Including scope and jig.

TIMING WAVEFORM OF READ CYCLE NO. 1[1,2]

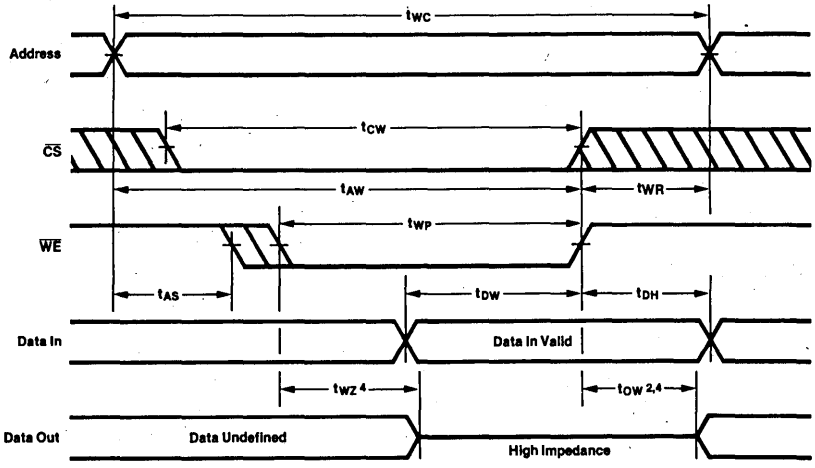


TIMING WAVEFORM OF READ CYCLE NO. 2[1,3]



NOTES:
1. $\overline{WE}$ is high for READ cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2. This parameter is sampled, not 100% tested.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)[1]



NOTES:
1. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
2. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2. This parameter is sampled and not 100% tested.

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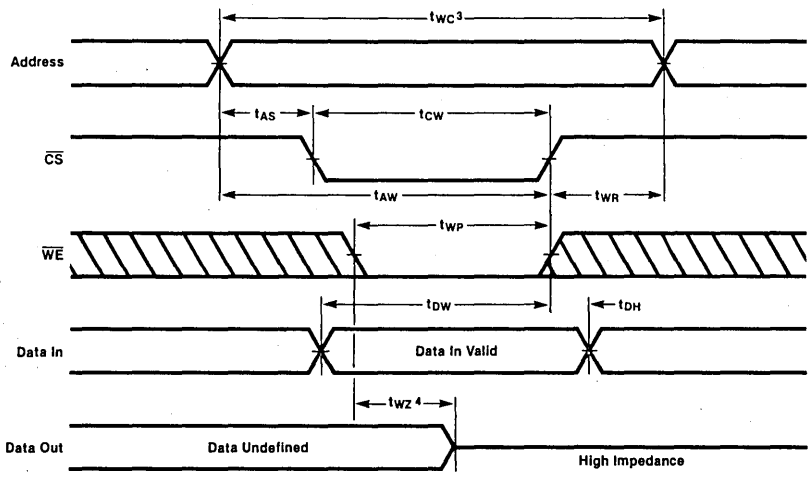
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)[1]



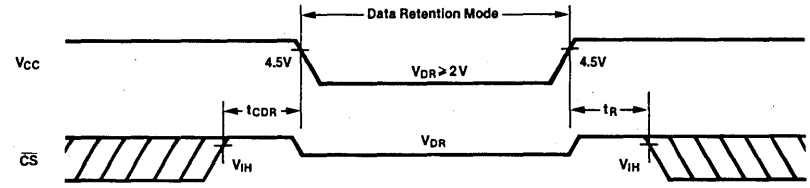
NOTES: 1. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
2. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2. This parameter is sampled and not 100% tested.

LOW V_{CC} DATA RETENTION CHARACTERISTICS FOR L VERSION ONLY (T_A = −55°C to +125°C/0°C to 70°C)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.[1]	MAX.	UNIT
V_{DR}	V_{CC} for Data Retention		2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{CC} - 0.2V$	— —	0.5[2] 1.0[3]	300/20[2] 450/30[3]	µA
t_{CDR}	Chip Deselect to Data Retention Time	$V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$	0	—	—	ns
t_R	Operation Recovery Time		t_{RC}[4]	—	—	ns

NOTES: 1. T_A = 25°C
2. at V_{CC} = 2V
3. at V_{CC} = 3V
4. t_{RC} = Read Cycle Time

LOW V_{CC} DATA RETENTION WAVEFORM



Integrated Device Technology, Inc.

CMOS STATIC RAMS 16K (4K x 4 BIT)

IDT71681S
IDT71681L

SEPARATE DATA INPUTS AND OUTPUTS

FEATURES:

- Separate data inputs and outputs
- High-speed (equal access and cycle time)
  IDT71681S 45/55/70/85ns (max.)
  IDT71681L 45/55/70/85ns (max.)
- Low power consumption
  —IDT71681S
  Active: 225mW (typ.)
  Standby: 100μW (typ.)
  —IDT71681L
  Active: 225mW (typ.)
  Standby: 10μW (typ.)
- Battery backup operation — 2V data retention voltage (IDT71681L only)
- 24-pin 300-mil dual-in-line package
- Produced with advanced CEMOS™ I high-performance technology
- CEMOS™ I process virtually eliminates alpha particle soft-error rates (with no organic die coatings)
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- 100% screened to MIL-STD-883 Class C

DESCRIPTION:

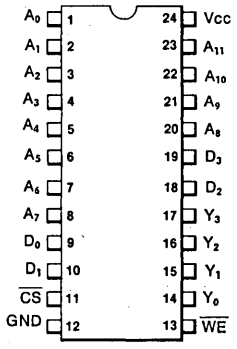
The IDT71681 is a 16,384-bit high-speed static RAM organized as 4K x 4 with separate data inputs and outputs. The separate input and output feature allows for improved system architectures. The external latches of a bidirectional bus system are not needed, improving both board density and system power levels. The absence of bus contention allows a streamlined approach enhancing system speeds. Also, the IDT71681 fits readily into a pipeline structure. It is fabricated using IDT's high-performance, high-reliability technology — CEMOS™ I. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective alternative to bipolar and fast NMOS memories.

Access times as fast as 45ns are available with maximum power consumption of only 495mW. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a standby mode as long as $\overline{CS}$ remains high. In the standby mode, the device consumes less than 100μW, typically. This capability provides significant system-level power and cooling savings. The low power, (L), version also offers a battery backup data retention capability where the circuit typically consumes only 1μW operating off of a 2V battery.

All inputs and outputs of the IDT71681 are TTL- compatible and operate from a single 5V supply, thus simplifying system designs. Fully static asynchronous circuitry is used, which requires no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

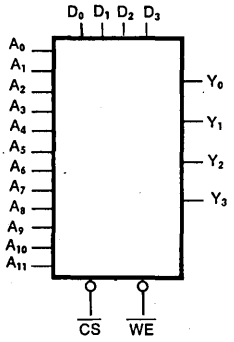
The IDT71681 is packaged in a space-saving 24-pin, 300 mil DIP providing high board-level packing densities.

PIN CONFIGURATION

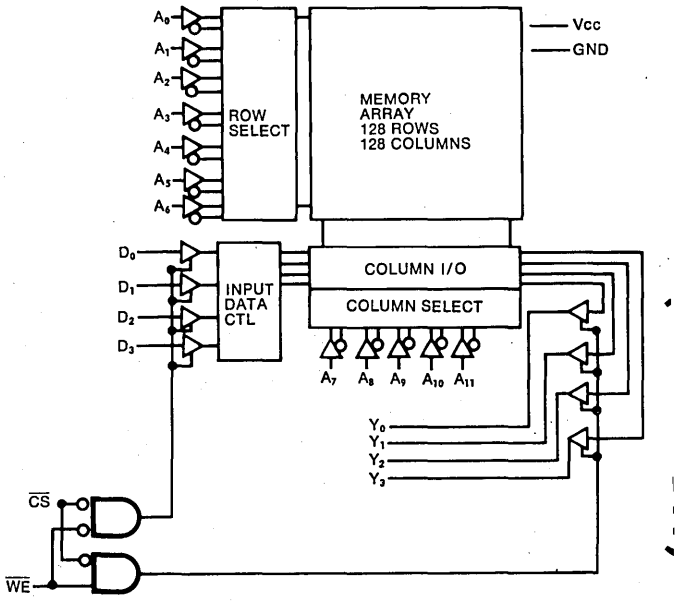


DIP
TOP VIEW

LOGIC SYMBOL



FUNCTIONAL BLOCK DIAGRAM



A_0-A_{11}	ADDRESS INPUTS	Di	DATA IN
$\overline{CS}$	CHIP SELECT	Yi	DATA OUT
$\overline{WE}$	WRITE ENABLE	GND	GROUND
Vcc	POWER		

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COMMERCIAL TEMPERATURE RANGE **DECEMBER 1982**

Planned availability — samples Q1 1983, production Q2 1983

Integrated Device Technology

MEMORY

Integrated Device Technology, Inc.

CMOS STATIC RAMS 16K (4K x 4 BIT)

IDT6168S IDT6168L

FEATURES:

- High-speed (equal access and cycle time)
  IDT6168S 45/55/70/85ns (max.)
  IDT6168L 45/55/70/85ns (max.)
- Low power consumption
  —IDT6168S
  Active: 225mW (typ.)
  Standby: 100μW (typ.)
  —IDT6168L
  Active: 225mW (typ.)
  Standby: 10μW (typ.)
- Battery backup operation—2V data retention voltage (IDT6168L only)
- High-density 20-pin dual-in-line package and 20-pin leadless chip carriers
- Produced with advanced CEMOS™ I high-performance technology
- CEMOS™ I process virtually eliminates alpha particle soft-error rates (with no organic die coatings)
- Bidirectional data input and output
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Pin-compatible with standard 4K x 4 static RAMs
- 100% screened to MIL-STD-883 Class C

DESCRIPTION:

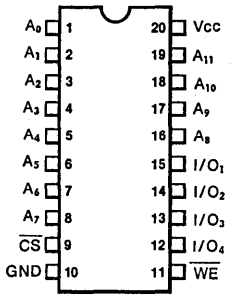
The IDT6168 is a 16,384-bit high-speed static RAM organized as 4K x 4. It is fabricated using IDT's high-performance, high-reliability technology—CEMOS™ I. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective alternative to bipolar and fast NMOS memories.

Access times as fast as 45ns are available with maximum power consumption of only 495mW. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a standby mode as long as $\overline{CS}$ remains high. In the standby mode, the device consumes less than 100μW, typically. This capability provides significant system-level power and cooling savings. The low power, (L), version also offers a battery backup data retention capability where the circuit typically consumes only 1μW operating off of a 2V battery.

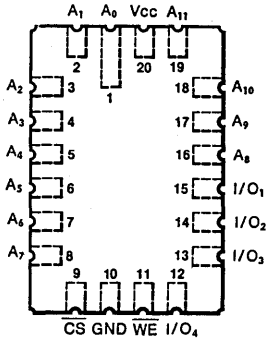
All inputs and outputs of the IDT6168 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Fully static asynchronous circuitry is used, which requires no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

The IDT6168 is packaged in either a space-saving 20-pin, 300 mil DIP or 20-pin leadless chip carrier, providing high board-level packing densities.

PIN CONFIGURATIONS

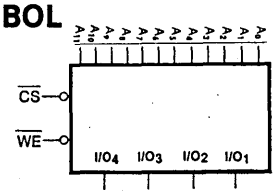


DIP
Top View

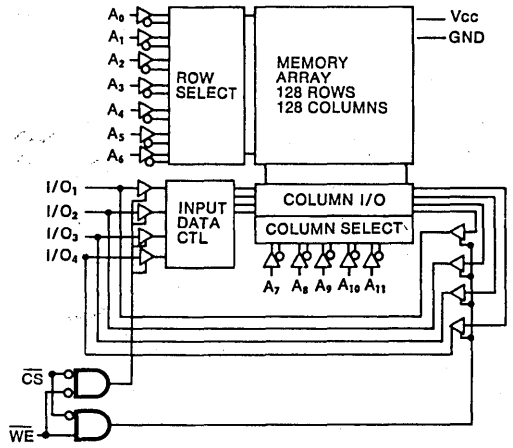


LCC
Top View

LOGIC SYMBOL



FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

A_0-A_{11}	ADDRESS INPUTS	I/O_1-I/O_4	DATA INPUT/OUTPUT
$\overline{CS}$	CHIP SELECT	Vcc	POWER
$\overline{WE}$	WRITE ENABLE	GND	GROUND

CEMOS is a trademark of Integrated Device Technology, Inc.

COMMERCIAL TEMPERATURE RANGE **DECEMBER 1982**

Planned availability — samples Q1 1983, production Q2 1983

IDT6116S/IDT6116L—IDT6167S/IDT6167L CMOS STATIC RAMS SCREENED TO MIL-STD-883 CRITERIA

IDT MILITARY PROCESSING TO MIL-STD-883

Maintaining the highest standards of quality in our memory products is the basis of IDT's standard manufacturing systems and procedures. IDT products begin with stringent design rules derived for use in high reliability programs. This is followed by a dedicated commitment to reliable workmanship as well as rigid controls throughout wafer fab, device assembly and electrical test, all of which are designed to produce products that are inherently reliable.

All products, including commercial, are manufactured and screened to the criteria of MIL-STD-883. Documentation, design, processing and assembly workmanship guidelines are patterned after MIL-M-38510 specifications.

For customer applications requiring higher levels of reliability screening, we supply full military range products completely screened to the Class B criteria of Method 5004 with Inspection lots tested to the Quality Conformance Requirements of Method 5005 as shown in the next column. This includes 100% 160-hour burn-in at $T_A = +125°C$ (or equivalent) per Method 1015 Cond D followed by 100% temperature testing of all DC, AC, and functional characteristics over the full −55°C to +125°C temperature range.

Samples of product which have been processed to Method 5004 100% screening requirements are submitted to the Quality Conformance inspection requirements of MIL-STD-883. These Quality Conformance inspections are performed to the criteria of Method 5005 Group A (electrical), Group B (mechanical), Group C (chip integrity), and Group D (package environmental integrity).

Specification of our IDT6116 Class B screened product will ensure the user not only of a high performance memory, but also a component tested to meet stringent reliability requirements.

SCREENING PROCEDURES
PER MIL-STD-883, METHOD 5004, CLASS B

SCREEN	TEST METHOD	LEVEL
Visual and Mechanical		
Internal Visual	2010, Condition B	100%
High-Temperature Storage	1008, Condition C	100%
Temperature Cycle	1010, Condition C	100%
Constant Acceleration	2001	100%
Hermeticity, Fine and Gross	1014	100%
Burn-In		
Pre-Burn-In Electrical	Per Applicable Device Specification	100%
Burn-In	1015, 160 Hrs. @ +125°C or Equivalent	100%
Final Electrical Tests		
Static (DC)	a. At 25°C and Power Supply Extremes	100%
	b. At Temperature and Power Supply Extremes	100%
Functional	a. At 25°C and Power Supply Extremes	100%
	b. At Temperature and Power Supply Extremes	100%
Switching (AC) or Dynamic	At 25°C, Nominal Power Supply	100%
External Visual	2009	100%

QUALITY CONFORMANCE TESTING
PER MIL-STD-883, METHOD 5005, CLASS B

SCREEN	TEST METHOD	LEVEL
Quality Conformance Sample Tests	Group A (Electrical Tests)	Sample
	Group B (Mechanical Tests)	Sample
	Group C (Chip Integrity Tests)	Sample
	Group D (Package Integrity Tests)	Sample

For special customer specifications or quality requirements beyond Class B levels of MIL-STD-883, such as SEM analysis, X-ray, or other screening flows to meet specific needs, contact your local IDT sales office.

Individual die, which have been manufactured to the same rigid controls in wafer fabrication and visually inspected to MIL-STD-883 Method 2010 Condition B, are available for shipment.

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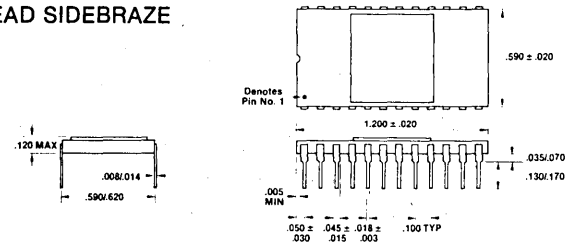
Integrated Device Technology, Inc.

CMOS STATIC RAMS
PACKAGE DIAGRAMS

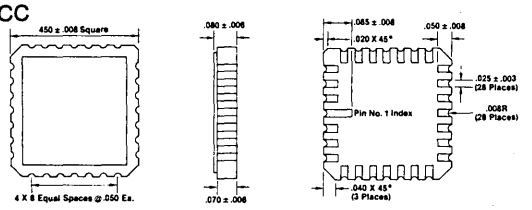
IDT6116S/L
IDT6167S/L
IDT6168S/L
IDT71681S/L

IDT6116S/IDT6116L

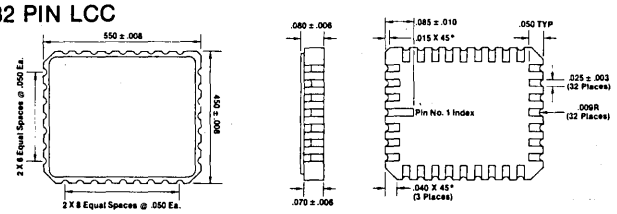
24-LEAD SIDEBRAZE



28 PIN LCC



32 PIN LCC



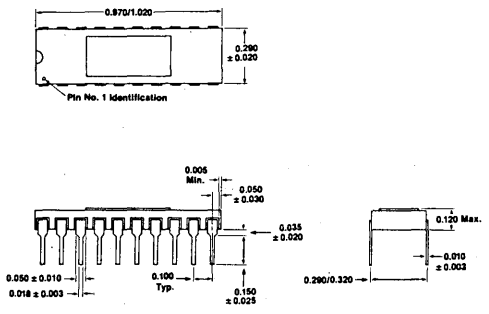
PINOUT CONFIGURATION

16K CMOS SRAM IDT6116 (2K × 8)

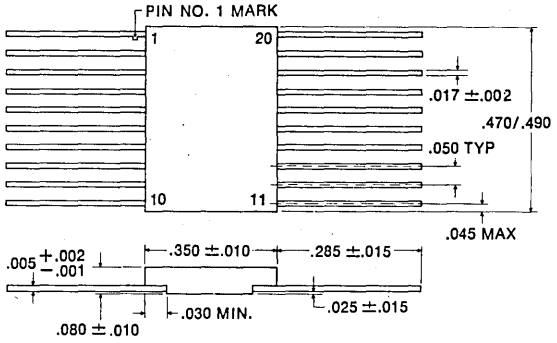
FUNCTION	LOGIC SYMBOL	PIN NUMBER 24 DIP	28 LCC	32 LCC
Address Line	A_7	1	1	4
Address Line	A_6	2	2	5
Address Line	A_5	3	3	6
Address Line	A_4	4	4	7
Address Line	A_3	5	5	8
Address Line	A_2	6	6	9
Address Line	A_1	7	9	10
Address Line	A_0	8	10	11
Input/Output	I/O 1	9	11	13
Input/Output	I/O 2	10	12	14
Input/Output	I/O 3	11	13	15
Power Ground	GND	12	14	16
Input/Output	I/O 4	13	15	18
Input/Output	I/O 5	14	16	19
Input/Output	I/O 6	15	17	20
Input/Output	I/O 7	16	18	21
Input/Output	I/O 8	17	19	22
Chip Select/ Data Retention	$\overline{CS}$	18	20	23
Address Line	A_{10}	19	23	24
Output Enable	$\overline{OE}$	20	24	25
Write Enable	$\overline{WE}$	21	25	26
Address Line	A_9	22	26	28
Address Line	A_8	23	27	29
Power Supply	V_{CC}	24	28	32

IDT6167S/IDT6167L/IDT6168S/IDT6168L

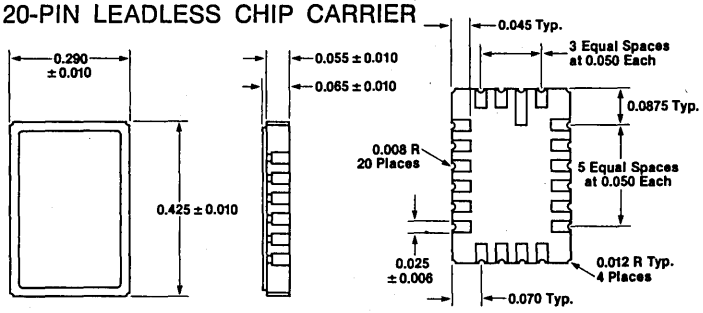
20-LEAD SIDEBRAZE



20-LEAD FLATPACK (IDT6167S/L ONLY)

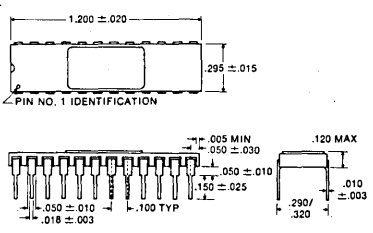


20-PIN LEADLESS CHIP CARRIER



IDT71681

24-LEAD THINDIP SIDEBRAZE



Integrated Device Technology

MEMORY

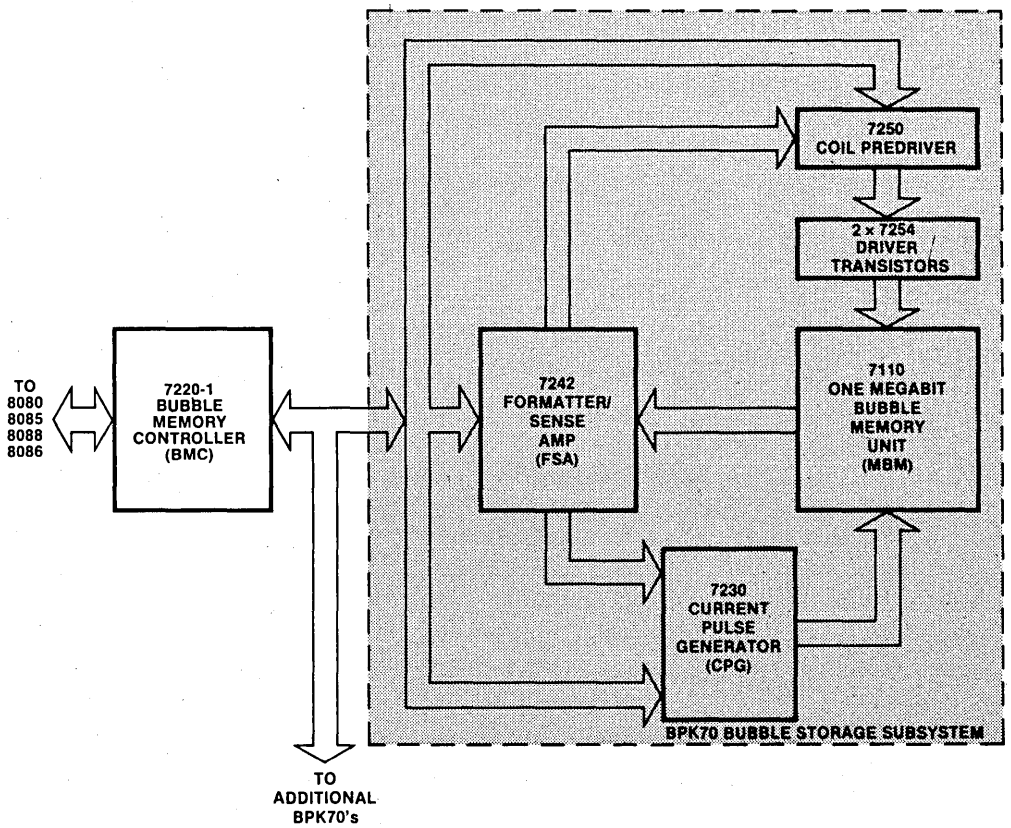
BPK 70
1 MBIT BUBBLE MEMORY SUBSYSTEMS

BPK 70-1	0–75°C
BPK 70-4	10–55°C
BPK 70-5	−20–85°C

- **1 MBit, Non-Volatile, Read-Write, High-Density Bubble Memory Subsystems**
- **Average Access Time of 48 ms**
- **Operates from +5V and +12V Power Supplies**
- **Maximum Data Rate of 100 KBit/Sec**

A Bubble Storage Subsystem contains components for production of 1 MBit Bubble Storage System. The kit consists of one 1 MBit Magnetic Bubble Memory and five support circuits (shown in the figure below). The BPK 70 Subsystem is controlled by an additional 7220 Bubble Memory Controller. One 7220-1 is capable of controlling up to eight BPK 70-1s or BPK 70-4s and one 7220-5 is capable of controlling up to four BPK 70-5s. Larger systems may be built using multiple 7220's with additional Bubble Storage Subsystems. The user interface of the 7220 is compatible with microprocessor bus systems for 8080, 8085, 8086 and 8088 and other standard microprocessors.

For applications in 0–75°C and 10–55°C temperature range, the Bubble Memory (7110-1/7110-4) and the other support circuits (7230, 7242, 7250, 7254) are available as separate, interchangeable components. Each of the components in the Subsystem are described in detail on the respective component data sheets.



CONFIGURATION OF ONE BPK 70 BUBBLE STORAGE SUBSYSTEM WITH THE 7220 CONTROLLER

ORDER NUMBER: 210356-001

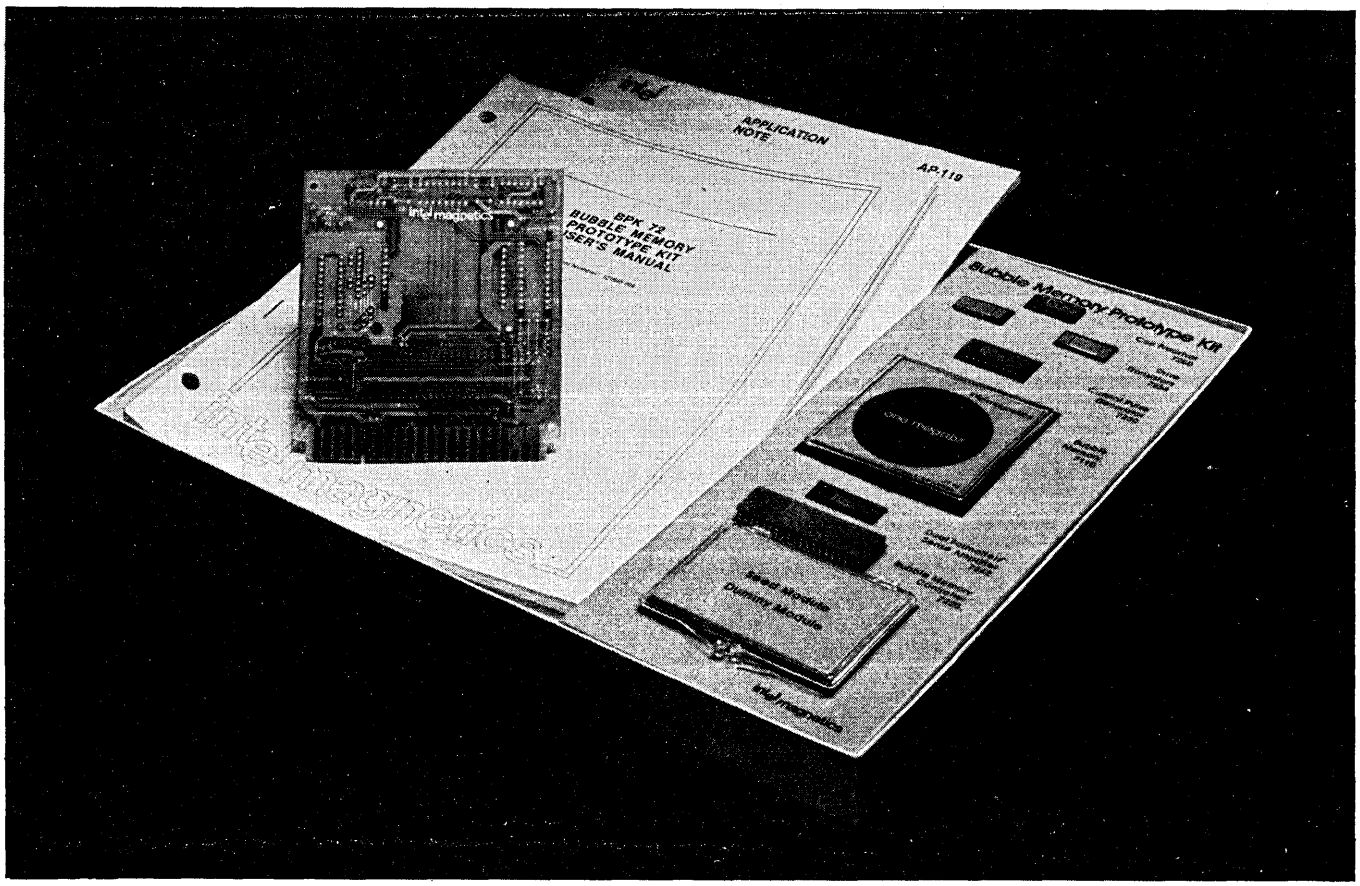
BPK 72
1 MBIT BUBBLE MEMORY PROTOTYPE KIT

BPK 72-1	0–75°C
BPK 72-4	10–55°C
BPK 72-5	−20–85°C

- **1 Mbit, Non-Volatile, Read-Write, High-Density, Bubble Storage Units**
- **Operates from +5V and +12V Power Supplies**
- **Average Access Time of 48 ms**
- **Built-in Error Correction/Detection**
- **Complete with Components, Blank Board, Accessories and Documentation for Prototyping**
- **Powerfail Data Protection**
- **Maximum Data Rate of 100K bit/sec**
- **Compatible with 8080/85/86/88 and other Standard Microprocessors**

The BPK 72 prototype kit contains all the necessary items and documentation required to build a 1 Megabit bubble storage prototype system with a minimum of design effort. Thus this unit gives the design engineer the opportunity to learn the characteristics of a Bubble Memory System and to actually test the bubble in a prototype product. Application information on microprocessor interfacing is included in the kit.

Each of the components in the kit, i.e., 7110, 7220, 7230, 7242, 7250, 7254 are described in detail on the respective component data sheet.



PRELIMINARY

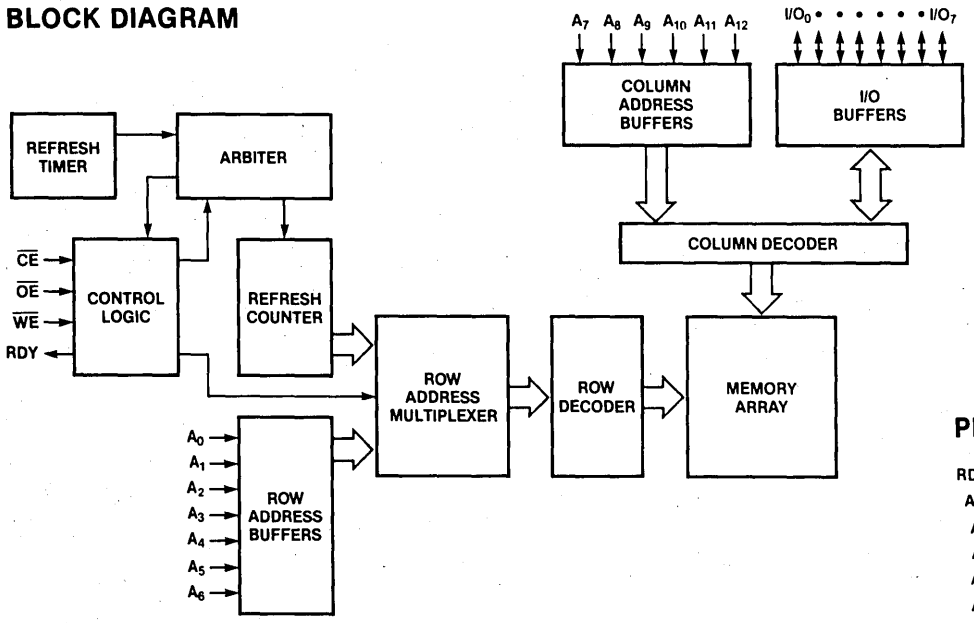
2186
8192 × 8 BIT INTEGRATED RAM

- Low-cost, high-volume HMOS technology
- High density one transistor cell
- Single +5V ± 10% supply
- Proven HMOS reliability
- Low active current (70 mA)
- Simple asynchronous refresh operation/ static RAM compatible
- 2764 EPROM compatible pin-out
- Two-line bus control
- JEDEC standard 28-pin site
- Low standby current (20 mA)

The Intel 2186 is a 8192 word by 8-bit integrated random access memory (iRAM) fabricated on Intel's proven HMOS dynamic RAM technology. Integrated refresh control provides static RAM characteristics at a significantly lower cost. Packaged in the industry standard 28-pin DIP, the 2186 conforms to the industry standard JEDEC 28-pin site. Designs based on 2186 timings can be made fully compatible with EPROMs and static RAMs.

The 2186 is particularly suited for microprocessor applications and incorporates many requisite system features including low power dissipation, automatic initialization, extended cycle operation and two-line bus control to eliminate bus contention.

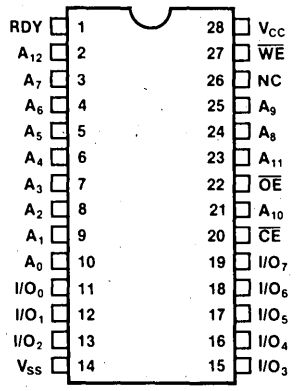
BLOCK DIAGRAM



PIN NAMES

A_0-A_{12}	ADDRESS INPUTS
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O_0-I/O_7	DATA INPUT/OUTPUT
RDY	READY
V_{CC}	+5V POWER
V_{SS}	GROUND

PIN CONFIGURATION



28-LEAD

B1164

September 1982
Order Number: 210460-001

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −10°C to +80°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin with
Respect to Ground ..... −1.0V to +7V
D.C. Continuous Current per Output ..... 10 mA
D.C. Maximum Data Out Current ..... 50 mA
D.C. Power Dissipation 1.0W

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. AND OPERATING CHARACTERISTICS[1]

TA = 0°C to +70°C, VCC = +5V ± 10% unless otherwise noted.

Symbol	Parameter	Limits		Unit	Test Conditions	Notes
		Min.	Max.			
ILI	Input Load Current (All Input Pins)		10	μA	VIH = VSS to VCC	
|ILO|	Output Leakage Current		10	μA	$\overline{OE}$ = VIH	
ICC	Operating Current		70	mA	Minimum Cycle Time	2
ISB	Standby Current		20	mA	$\overline{CE}$ = VIH	
VIL	Input Low Voltage	−1.0	0.8	V		3
VIH	Input High Voltage	2.4	7.0	V		
VOL	Output Low Voltage		0.45	V	IOL = 2.1 mA	4
VOH	Output High Voltage	2.4		V	IOH = −1.0 mA	

NOTES:
1. Typical limits are VCC = +5V, TA = 25°C.
2. ICC is dependent on output loading when the device output is selected. Specified ICC max. is measured with the output open.
3. Specified VIL min. is for steady state operation. During transitions the inputs may overshoot to −2.0V for periods not to exceed 20 nsec.
4. IOL for RDY is 10 mA.

A.C. TEST CONDITIONS

Input Pulse and Timing
Reference Levels ..... 0.8V to 2.4V
Input Rise and Fall Times ..... 10 nsec
Output Timing Reference Levels .. 0.45V and 2.4V
Output Load ..... See Figure 1

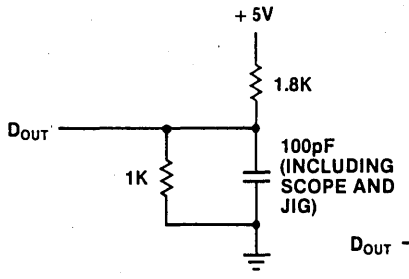


Figure 1.

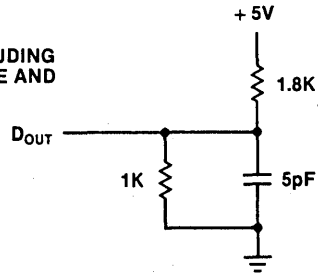


Figure 2.
(FOR HIGH IMPEDANCE MEASUREMENTS ONLY)

CAPACITANCE[5]

TA = 25°C, f = 1.0 MHz

Symbol	Parameter	Max.	Unit	Conditions
C_{ADD}	Address Capacitance	8	pF	V_{ADD} = 0V
$C_{I/O}$	I/O Capacitance	14	pF	$V_{I/O}$ = 0V
C_{IN}	Control Capacitance	14	pF	V_{IN} = 0V

NOTE: 5. This parameter is characterized and not 100% tested.

A.C. CHARACTERISTICS

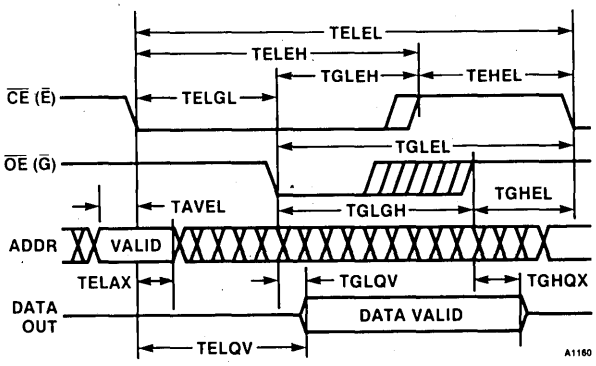
TA = 0°C to +70°C, VCC = +5V ± 10% unless otherwise noted.

READ CYCLE ($\overline{WE}$ = VIH)

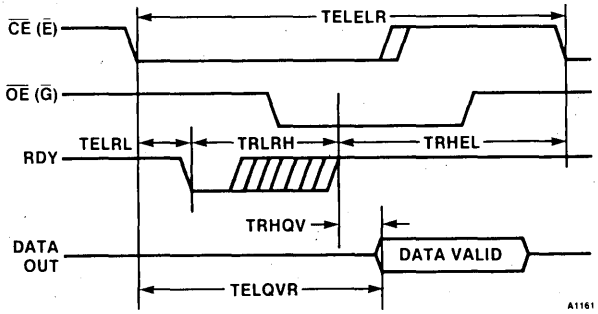
Symbol	Parameter	2186-25		2186-30		2186-35		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
TELEL	Cycle Time	425		500		600		ns	1
TELQV	Access Time from $\overline{CE}$		250		300		350	ns	1
TELELR	Cycle Time with Refresh	850		1000		1200		ns	2
TELQVR	Access Time from $\overline{CE}$ w/Refresh		675		800		950	ns	2
TGLQV	Access Time from $\overline{OE}$		65		70		75	ns	
TELEH	$\overline{CE}$ Pulse Width	40		40		40		ns	
TEHEL	$\overline{CE}$ High Time	40		40		40		ns	
TAVEL	Address Set-Up Time	0		0		0		ns	
TELAX	Address Hold Time	30		30		30		ns	
TGLEL	$\overline{OE}$ low to next $\overline{CE}$ low	250		275		300		ns	
TGLGH	$\overline{OE}$ Pulse Width	65		70		75		ns	
TGHEL	$\overline{OE}$ high to next $\overline{CE}$ low	40		40		40		ns	
TGHQX	$\overline{OE}$ high to Data Float	10	60	10	60	10	60	ns	3
TELGL	$\overline{CE}$ low to $\overline{OE}$ low — Pulse Mode	0	90	0	90	0	90	ns	4,5
TGLEH	$\overline{OE}$ low to $\overline{CE}$ high — Long Mode	40		40		40		ns	4
TELRL	$\overline{CE}$ low to RDY low		50		60		70	ns	6
TRLRH	RDY Pulse Width	100		100		100		ns	6
TRHQV	RDY high to Data Valid		60		70		95	ns	
TRHEL	RDY high to next $\overline{CE}$ low	250		275		350		ns	

WAVEFORMS

READ CYCLE



READ CYCLE WITH REFRESH



A.C. CHARACTERISTICS

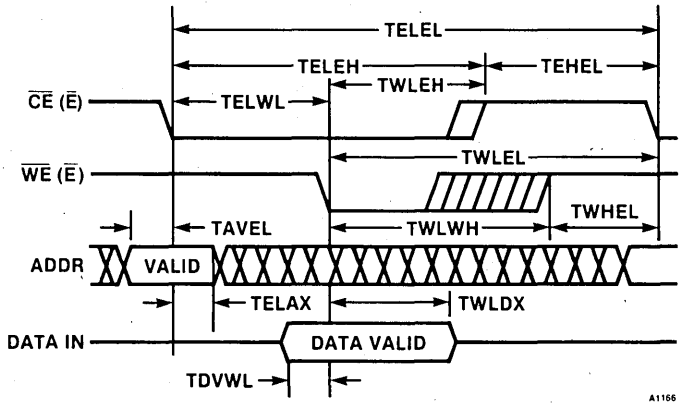
TA = 0°C to +70°C, VCC = +5V ± 10% unless otherwise noted.

WRITE CYCLE ($\overline{OE}$ = VIH)

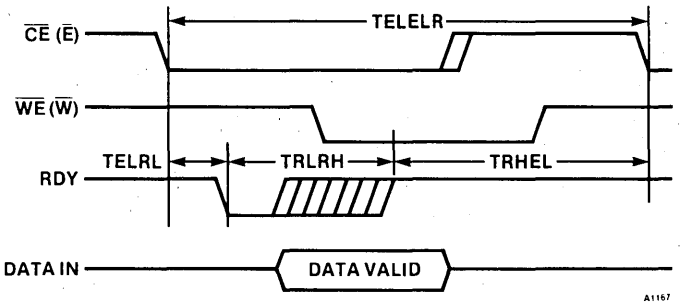
Symbol	Parameter	2186-25		2186-30		2186-35		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
TELEL	Cycle Time	425		500		600		ns	1
TELELR	Cycle Time with Refresh	850		1000		1200		ns	2
TELEH	$\overline{CE}$ Pulse Width	40		40		40		ns	
TEHEL	$\overline{CE}$ High Time	40		40		40		ns	
TAVEL	Address Set-Up Time	0		0		0		ns	
TELAX	Address Hold Time	30		30		30		ns	
TWLEL	$\overline{WE}$ low to next $\overline{CE}$ low	250		300		350		ns	
TWLWH	$\overline{WE}$ Pulse Width	40		40		40		ns	
TWHEL	$\overline{WE}$ high to next $\overline{CE}$ low	40		40		40		ns	
TDVWL	Data Set-Up to $\overline{WE}$ low	0		0		0		ns	
TWLDX	Data Hold from $\overline{WE}$ low	40		45		50		ns	
TELWL	$\overline{CE}$ low to $\overline{WE}$ low — Pulse Mode	0	90	0	90	0	90	ns	4,5
TWLEH	$\overline{WE}$ low to $\overline{CE}$ high — Long Mode	40		40		40		ns	4
TELRL	$\overline{CE}$ low to RDY low		50		60		70	ns	6
TRLRH	RDY Pulse Width	100		100		100		ns	6
TRHEL	RDY high to next $\overline{CE}$ low	250		275		350		ns	

WAVEFORMS

WRITE CYCLE



WRITE CYCLE WITH REFRESH



A.C. CHARACTERISTICS

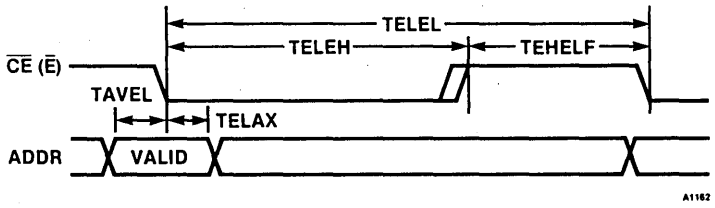
TA = 0°C to +70°C, VCC = +5V ± 10% unless otherwise noted.

FALSE MEMORY CYCLE ($\overline{OE}$ and $\overline{WE}$ = VIH)

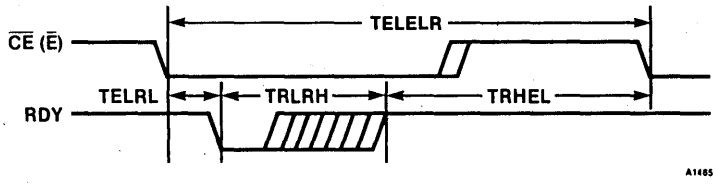
Symbol	Parameter	2186-25		2186-30		2186-35		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
TELEL	Cycle Time	425		500		600		ns	1
TELELR	Cycle Time with Refresh	850		1000		1200		ns	2
TELEH	$\overline{CE}$ Pulse Width	40	10000	40	10000	40	10000	ns	7
TEHELF	$\overline{CE}$ High Time for F.M.C.	200		250		275		ns	8
TAVEL	Address Set-Up Time	0		0		0		ns	
TELAX	Address Hold Time	30		30		30		ns	
TELRL	$\overline{CE}$ low to RDY low		50		60		70	ns	6
TRLRH	RDY Pulse Width	100		100		100		ns	6
TRHEL	RDY high to next $\overline{CE}$ low	250		275		350		ns	

WAVEFORMS

FALSE MEMORY CYCLE



FALSE MEMORY CYCLE WITH REFRESH



NOTES:

1. TELEL < TELELR and TELQV < TELQVR.
2. For reference only.
3. Transition is measured ±500 mV from steady state logic level with specified loading in Figure 2.
4. For Pulse Mode TELEH ≤ $TELGL_{max}$ + $TGLEH_{min}$ or TELEH ≤ $TELWL_{max}$ + $TWLEH_{min}$. For Long Mode TELEH > $TELGL_{max}$ + $TGLEH_{min}$ or TELEH > $TELWL_{max}$ + $TWLEH_{min}$.
5. For Long Mode $TELGL_{max}$ and $TELWL_{max}$ = 10 μsec.
6. C_{RDY} < 100 pF and R_{EXT} = 510Ω.
7. False Memory Cycles Only.
8. Note TEHELF > TEHEL.

FUNCTIONAL DESCRIPTION

The 2186 has three control pins: $\overline{CE}$ (Chip Enable), $\overline{OE}$ (Output Enable), and $\overline{WE}$ (Write Enable). An open-drain output pin called RDY indicates if refresh is occurring during an access request. *RDY will only respond when the 2186 has been selected by $\overline{CE}$ going active low during a refresh cycle.*

Cycles are initiated by latching addresses into the 2186 with the leading (falling) edge of $\overline{CE}$. When $\overline{CE}$ goes active during internal refresh, the RDY pin is pulled low signaling a delay. RDY remains low until shortly before both refresh and access (Read/-Write) cycles are complete.

On-chip control circuitry tracks all operations for nearly transparent refresh. A high-speed on-chip arbitration circuit prevents conflicts from occurring between refresh and access cycles.

Access Cycles

READ CYCLE

A read cycle is initiated by $\overline{CE}$ and $\overline{OE}$ both going active low during the same cycle. $\overline{CE}$ may be either pulsed to initiate a cycle or held active low throughout the cycle. $\overline{OE}$ is a logic level; $\overline{OE}$ controls the 2186 data output bus. Access times are specified from both $\overline{OE}$ and $\overline{CE}$. Data remains on the data bus until $\overline{OE}$ returns inactive (high) *independent of $\overline{CE}$.* $\overline{WE}$ may not go active during a Read cycle.

WRITE CYCLE

A Write cycle is initiated by $\overline{CE}$ and $\overline{WE}$ going active low during the same cycle. $\overline{CE}$ may be a pulse or a logic level. *$\overline{WE}$ leading edge* latches data from the data bus into the 2186. $\overline{OE}$ may not go active during a Write cycle.

FALSE MEMORY CYCLE (FMC)

A False Memory cycle is initiated by $\overline{CE}$ going active *without* either $\overline{OE}$ or $\overline{WE}$ going active. No memory cycle will be performed. Note that address set-up and hold times must be observed for False Memory cycle operation.

Operating Modes

REFRESH OPERATION

Refresh is totally automatic and requires no external stimulas. All refresh functions are controlled internally.

A high-speed arbitration circuit will resolve any potential conflict arising between simultaneous external access and internal refresh cycle requests. The internal timer period is specified as 24 μsec. ± 50%.

The 2186 may also be refreshed by performing Read, Write, or False Memory cycles on all 128 rows (A0 through A6) within a two millisecond period.

EXTENDED CYCLE OPERATION

Extended cycle operation is defined as holding $\overline{OE}$ or $\overline{WE}$ valid (low) for indefinite periods. ($\overline{CE}$ is allowed to return high.) Data will remain valid on the bus as long as $\overline{OE}$ is valid. $\overline{WE}$ latches data on the leading (falling) edge. Automatic refreshes will continue to be performed as needed, even while $\overline{OE}$ or $\overline{WE}$ is held low; RDY will *not* respond during these extended cycle refreshes.

INITIALIZATION

To guarantee initialization, all control inputs must be inactive (high) for a 100 microsecond period after V_{CC} is within specification. No extra cycles are required before normal operation may begin.

Interfacing Considerations

The 2186 is an edge enabled RAM. Below is an illustration of a simple interface for connecting microprocessors with edge enable memories. *A stable $\overline{CE}$ clock is necessary to avoid accidentally selecting the RAM.* Generally, stable select signals are desirable in all types of microsystem applications. Most common decoding circuits allow addresses to flow directly through the decoder (i.e. decoder permanently "enabled"). This technique may allow false decoder outputs to occur when addresses are in transition. This may result in false $\overline{CE}$ signals and potentially, invalid memory requests. A simple gating circuit will inhibit enabling the decoder until addresses are valid at the decoder inputs.

Another interfacing consideration is the relationship between $\overline{WE}$ and valid data. The 2186 performs a write operation on the leading edge of $\overline{WE}$. In a minimum mode 8088 or 8086 system, $\overline{WE}$ occurs before data is valid. The cross-coupled NAND gate configuration shown below on the $\overline{WR}$ signal will prevent this from occurring. This implementation also guarantees valid data on the rising (trailing) edge of $\overline{WE}$ to maintain compatibility with fully static RAMs. (For maximum mode 8088 or 8086 operation, the control signal $\overline{MWTC}$ directly from the 8288 bus controller serves the same function.) For a more detailed description of designing iRAM

systems, refer to Intel App. Note #132 on *"Designing Memory Systems with the 8K × 8 iRAM"*.

Layout Considerations

To ensure compatibility with other 28-pin memory devices such as EPROMs, several pins require close examination; specifically, pins number 1, 26 and 27. Following is a discussion of the system level operation and the design considerations for these pins.

PIN #1

Pin 1 on all EPROMs is reserved for the high voltage programming bias, V_{PP}. EPROMs are usually programmed external to the system. Therefore, in normal system operation, pin 1 is connected to V_{CC}.

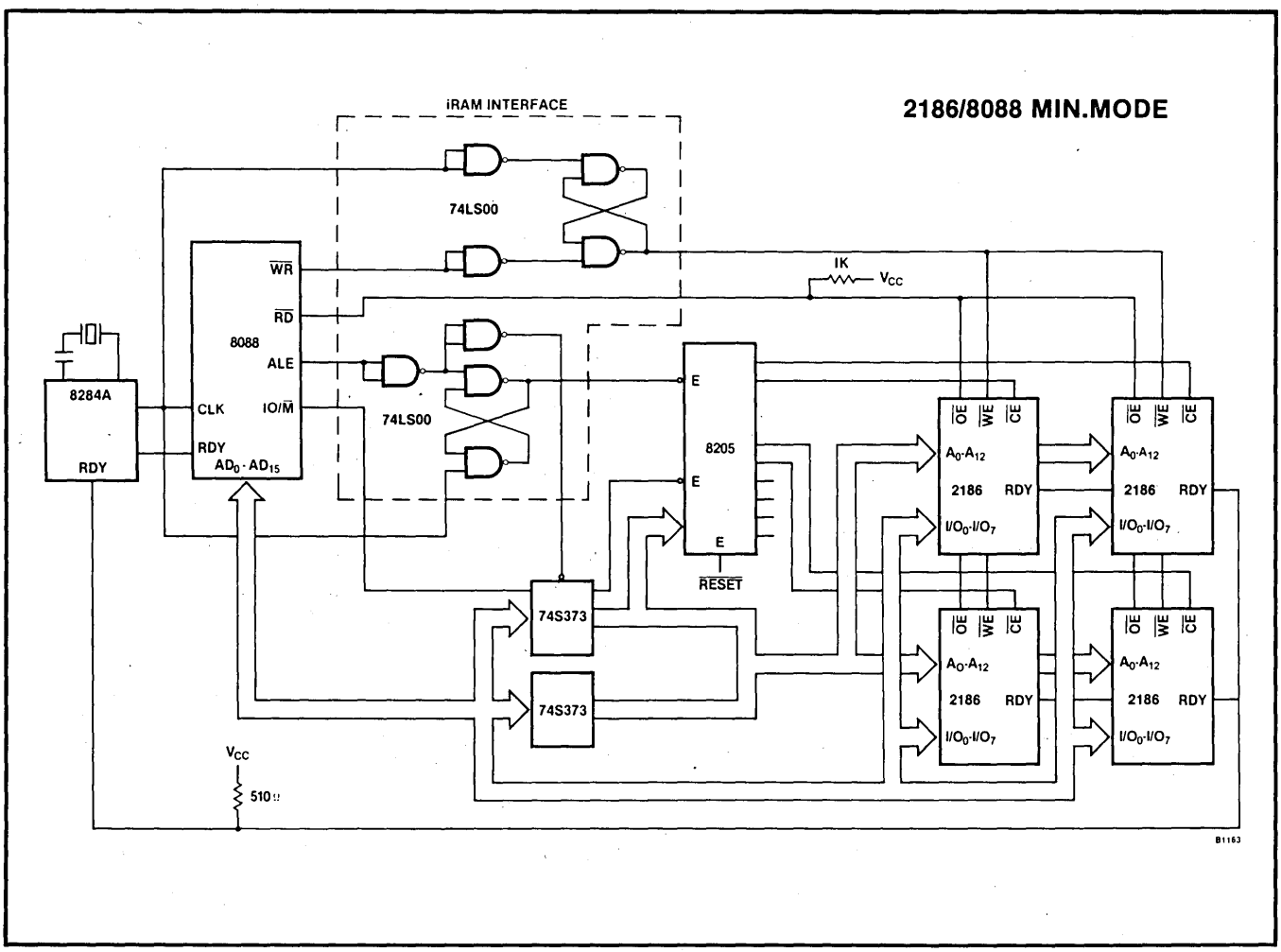
Pin 1 on the 2186 is the microprocessor handshake signal, RDY. The RDY signal may be bussed to the RDY input of either the microprocessor or clock generator. Because RDY is an open drain output, all 2186 RDY signals may be "wire OR'd" with any other RDY signals in the system. A 510 ohm pull-up resistor is required between RDY and V_{CC}. For the 2186 application, a trace should be run from pin 1 of each socket location to the RDY input of either the microprocessor or clock generator. Also, a provision for a pull-up resistor to V_{CC} is needed.

PIN #26

While pin 26 is a No Connect for both the 2186 or the 2764 EPROM, a trace to pin 26 from V_{CC} will guarantee compatibility between 24 pin and 28 pin EPROMs. Pin 26 will carry the additional address bit required to future higher density memories. For flexibility, provide a jumper for an address bit and/or V_{CC} on pin 26.

PIN #27

Pin 27 is labelled $\overline{WE}$ on the RAM and $\overline{PGM}$ on the EPROM. While $\overline{WE}$ is a system level control signal, $\overline{PGM}$ is only used when programming the EPROM (V_{PP} at +21V). $\overline{PGM}$ may be allowed to toggle during normal EPROM operation (V_{PP} at +5V). Therefore, $\overline{WE}$ may be bussed to every socket location with no jeopardy of illegal operation.



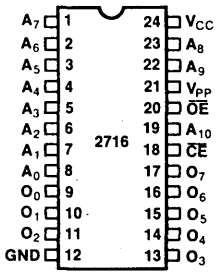
2716
16K (2K x 8) UV ERASABLE PROM

- **Fast Access Time**
  - **— 2716-1: 350 ns Max.**
  - **— 2716-2: 390 ns Max.**
  - **— 2716: 450 ns Max.**
  - **— 2716-5: 490 ns Max.**
  - **— 2716-6: 650 ns Max.**
- **Single +5V Power Supply**
- **Low Power Dissipation**
  - **— Active Power: 525 mW Max.**
  - **— Standby Power: 132 mW Max.**
- **Pin Compatible to Intel 2732A EPROM**
- **Simple Programming Requirements**
  - **— Single Location Programming**
  - **— Programs with One 50 ms Pulse**
- **Inputs and Outputs TTL Compatible During Read and Program**
- **Completely Static**

The Intel 2716 is a 16,384-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2716 operates from a single 5-volt power supply, has a static standby mode, and features fast single-address programming. It makes designing with EPROMs fast, easy and economical.

The 2716, with its single 5-volt supply and with an access time up to 350 ns, is ideal for use the high-performance +5V microprocessors such as Intel's 8085 and 8086. Selected 2716-5s and a 2716-6s are also available for slower speed applications. The 2716 also has a static standby mode which reduces power consumption without increasing access time. The maximum active power dissipation is 525 mW while the maximum standby power dissipation is only 132 mW, a 75% savings.

The 2716 uses a simple and fast method for programming a single TTL-level pulse. No need for high voltage pulsing because all programming controls are handled by TTL signals. Program any location at any time—either individually, sequentially or at random with the 2716's single-address programming. Total programming time for all 16,384 bits is only 100 seconds.



PIN NAMES

A_0-A_{10}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS

Figure 1. Pin Configuration

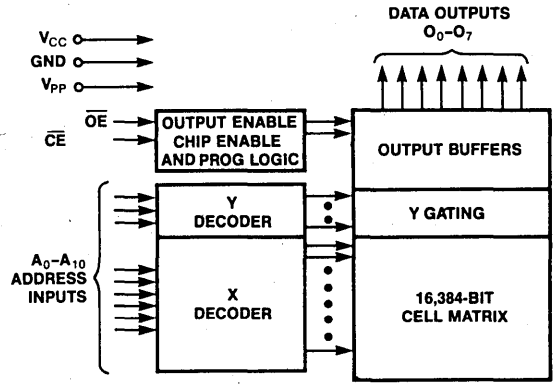


Figure 2. Block Diagram

OCTOBER 1982
ORDER NUMBER: 210310-002

2732A
32K (4K x 8) UV ERASABLE PROM

- 200 ns (2732A-2) Maximum Access Time . . . HMOS*-E Technology
- Compatible with High-Speed 8mHz iAPX 186...Zero WAIT State
- Two Line Control
- Pin Compatible to 2764 EPROM
- Industry Standard Pinout . . . JEDEC Approved
- Low Standby Current . . . 35 mA Maximum
- ±10% V_{CC} Tolerance Available
- int$_e$ligent Identifier™ Mode

The Intel 2732A is a 5V only, 32,768 bit ultraviolet erasable and electrically programmable read-only-memory (EPROM). The standard 2732A access time is 250 ns with speed selection (2732A-2) available at 200 ns. The access time is compatible with high performance microprocessors such as the 8 MHz iAPX 186. In these systems, the 2732A allows the microprocessor to operate without the addition of WAIT states.

An important 2732A feature is the separate output control, Output Enable ($\overline{OE}$), from the Chip Enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in microprocessor systems. Intel's Application Note AP-72 describes the microprocessor system implementation of the $\overline{OE}$ and $\overline{CE}$ controls on Intel's EPROMs. AP-72 is available from Intel's Literature Department.

The 2732A has a standby mode which reduces power consumption without increasing access time. The maximum active current is 125 mA, while the maximum standby current is only 35 mA, a 70% saving. The standby mode is selected by applying the TTL-high signal to the CE input.

The 2732A is fabricated with HMOS*-E technology, Intel's high-speed N-channel MOS Silicon Gate Technology.

*HMOS is a patented process of Intel Corporation.

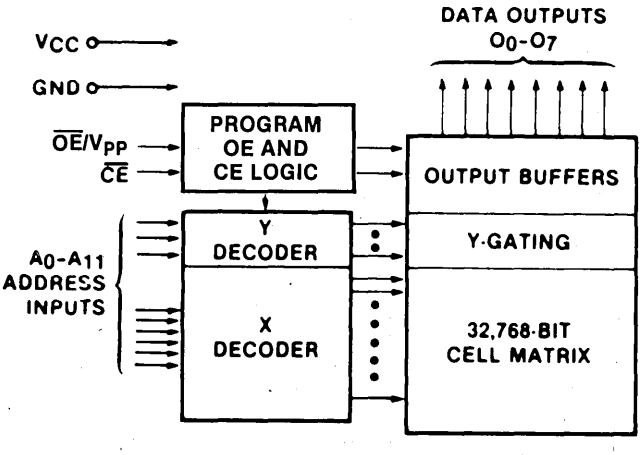


Figure 1. Block Diagram

PIN NAMES

A_0-A_{11}	ADDRESSES	
$\overline{CE}$	CHIP ENABLE	
$\overline{OE}/V_{PP}$	OUTPUT ENABLE/	V_{PP}
O_0-O_7	OUTPUTS	

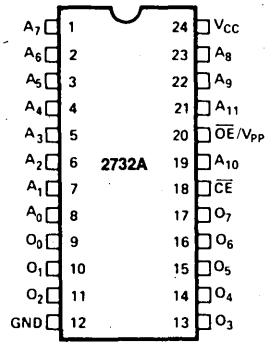


Figure 2. Pin Configurations

OCTOBER 1982
AFN-01545B

2764
64K (8K x 8) UV ERASABLE PROM

- **200 ns (2764-2) Maximum Access Time . . . HMOS*-E Technology**
- **Compatible with High-Speed 8mHz iAPX 186...Zero WAIT State**
- **Two Line Control**
- **Pin Compatible to 27128 EPROM**
- **inteligent Programming™ Algorithm**
- **Industry Standard Pinout . . . JEDEC Approved**
- **Low Active Current...100mA Max.**
- **±10% V_{CC} Tolerance Available**

The Intel 2764 is a 5V only, 65,536-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The standard 2764 access time is 250 ns with speed selection available at 200 ns. The access time is compatible with high-performance microprocessors such as Intel's 8 mHz iAPX 186. In these systems, the 2764 allows the microprocessor to operate without the addition of WAIT states.

An important 2764 feature is the separate output control, Output Enable ($\overline{OE}$) from the Chip Enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in microprocessor systems. Intel's Application Note AP-72 describes the microprocessor system implementation of the $\overline{OE}$ and $\overline{CE}$ controls on Intel's EPROMs. AP-72 is available from Intel's Literature Department.

The 2764 has a standby mode which reduces power consumption without increasing access time. The maximum active current is 100 mA, while the maximum standby current is only 40 mA. The standby mode is selected by applying a TTL-high signal to the $\overline{CE}$ input.

±10% V_{CC} tolerance is available as an alternative to the standard ±5% V_{CC} tolerance for the 2764. This can allow the system designer more leeway with regard to his power supply requirements and other system parameters.

The 2764 is fabricated with HMOS*-E technology, Intel's high-speed N-channel MOS Silicon Gate Technology.

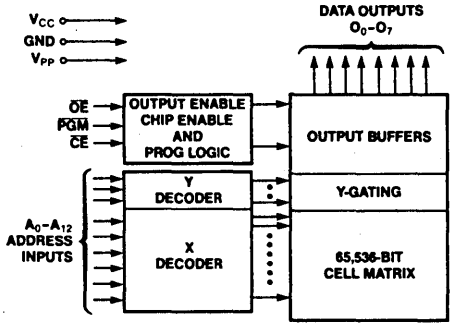
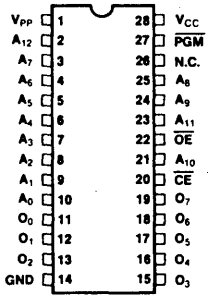


Figure 1. Block Diagram

27256	27128	2732A	2716
VPP	-VPP		
A12	A12		
A7	A7	A7	A7
A6	A6	A6	A6
A5	A5	A5	A5
A4	A4	A4	A4
A3	A3	A3	A3
A2	A2	A2	A2
A1	A1	A1	A1
A0	A0	A0	A0
O0	O0	O0	O0
O1	O1	O1	O1
O2	O2	O2	O2
Gnd	Gnd	Gnd	Gnd

2764



2716	2732A	27128	27256
		VCC	VCC
		PGM	A14
VCC	VCC	A13	A13
A8	A8	A8	A8
A9	A9	A9	A9
VPP	A11	A11	A11
OE	OE/VPP	OE	OE
A10	A10	A10	A10
CE	CE	CE	CE
O7	O7	O7	O7
O6	O6	O6	O6
O5	O5	O5	O5
O4	O4	O4	O4
O3	O3	O3	O3

NOTE: INTEL "UNIVERSAL SITE"-COMPATIBLE EPROM PIN CONFIGURATIONS ARE SHOWN IN THE BLOCKS ADJACENT TO THE 2764 PINS

Figure 2. Pin Configurations

MODE SELECTION

MODE \ PINS	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	A_9 (24)	V_{PP} (1)	V_{CC} (28)	Outputs (11-13, 15-19)
Read	V_{IL}	V_{IL}	V_{IH}	X	V_{CC}	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{IL}	X	V_{PP}	V_{CC}	D_{IN}
Verify	V_{IL}	V_{IL}	V_{IH}	X	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	X	X	X	V_{PP}	V_{CC}	High Z
inteligent Identifier	V_{IL}	V_{IL}	V_{IH}	V_H	V_{CC}	V_{CC}	Code
inteligent Programming	V_{IL}	V_{IH}	V_{IL}	X	V_{PP}	V_{CC}	D_{IN}

1. X can be V_{IH} or V_{IL}
2. V_H = 12.0V ±0.5V

PIN NAMES

A_0-A_{12}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS
$\overline{PGM}$	PROGRAM
N.C.	NO CONNECT

*HMOS is a patented process of Intel Corporation

OCTOBER 1982
ORDER NUMBER: 210570-002

27128
128K (16K x 8) UV ERASABLE PROM

- 250 ns Maximum Access Time . . . HMOS*-E Technology
- Compatible with High-Speed 8 MHz iAPX 186...Zero WAIT State
- Two-Line Control
- Pin Compatible to 2764 EPROM
- Industry Standard Pinout . . . JEDEC Approved
- ±10% V_{CC} Tolerance Available
- Low Active Current . . . 100 mA Max.
- int$_e$ligent Programming™ Algorithm

The Intel 27128 is a 5V only, 131,072-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The standard 27128 access time is 250 ns which is compatible with high-performance microprocessors such as Intel's 8 MHz iAPX 186. In these systems the 27128 allows the microprocessor to operate without the addition of WAIT states.

An important 27128 feature is the separate output control, Output Enable ($\overline{OE}$) from the Chip Enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in microprocessor systems. Intel's Application Note AP-72 describes the microprocessor system implementation of the $\overline{OE}$ and $\overline{CE}$ controls on Intel's EPROMs. AP-72 is available from Intel's Literature Department.

The 27128 has standby mode which reduces the power consumption without increasing access time. The maximum active current is 100 mA, while the maximum standby current is only 40 mA. The standby mode is selected by applying a TTL-high signal to the $\overline{CE}$ input.

±10% V_{CC} tolerance is available as an alternative to the standard ±5% V_{CC} tolerance for the 27128. This can allow the system designer more leeway with regard to his power supply requirements and other system parameters.

The 27128 is fabricated with HMOS*-E technology, Intel's high-speed N-channel MOS Silicon Gate Technology.

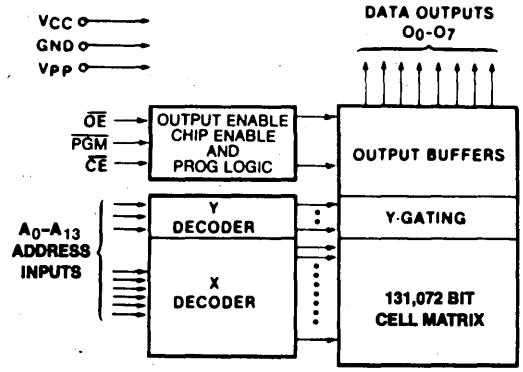
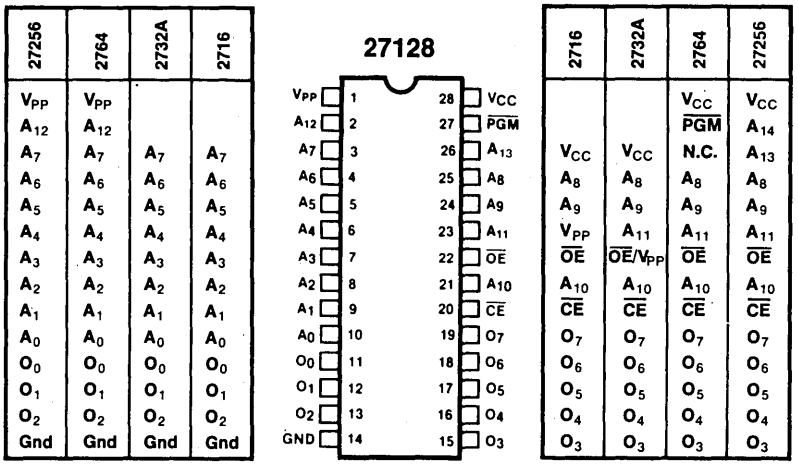


Figure 1. Block Diagram

MODE SELECTION

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	A_9 (24)	V_{PP} (1)	V_{CC} (28)	Outputs (11-13,15-19)
Read	V_{IL}	V_{IL}	V_{IH}	X	V_{CC}	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	V_{CC}	V_{PP}	High Z
Standby	V_{IH}	X	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{IL}	X	V_{PP}	V_{CC}	D_{IN}
Verify	V_{IL}	V_{IL}	V_{IH}	X	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	X	X	X	V_{PP}	V_{CC}	High Z
int$_e$ligent Identifier	V_{IL}	V_{IL}	V_{IH}	V_H	V_{CC}	V_{CC}	Code
int$_e$ligent Programming	V_{IL}	V_{IH}	V_{IL}	X	V_{PP}	V_{CC}	D_{IN}

NOTES:
1. X can be V_{IH} or V_{IL}
2. V_H = 12.0V ±0.5V



NOTE: INTEL "UNIVERSAL SITE" COMPATIBLE EPROM PIN CONFIGURATIONS ARE SHOWN IN THE BLOCKS ADJACENT TO THE 27128 PINS

Figure 2. Pin Configurations

PIN NAMES

A_0-A_{13}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS
$\overline{PGM}$	PROGRAM
N.C.	NO CONNECT

*HMOS is a patented process of Intel Corporation.

SEPTEMBER 1982
ORDER NUMBER: 210224-003

UV ERASABLE PROM FAMILY

EXPRESS

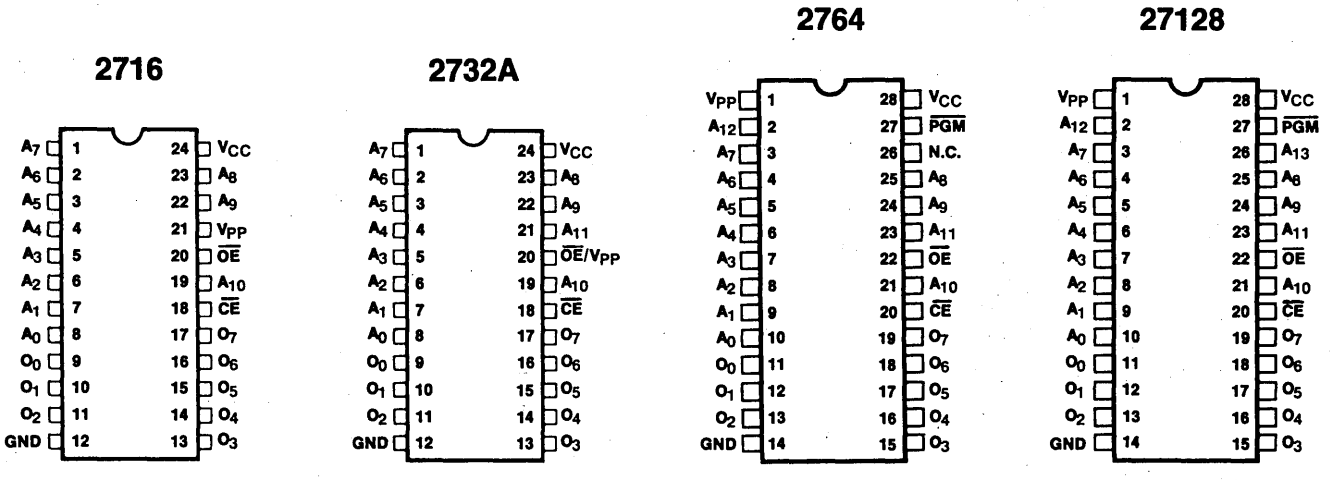
- **0–70°C Temperature Range Standard**
- **Extended Temperature Range −40°C – +85°C Available**
- **Two Line Control**
- **168±8 Hour Burn-in Available**
- **Industry Standard Pinout . . . JEDEC Approved**
- **Inspected To 0.1% AQL**

The Intel EXPRESS EPROM family is a series of ultraviolet erasable and electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications. Intel's JEDEC approved 28 pin Universal Memory Socket provides the industry standard upgrade path to higher density EPROMs.

EXPRESS EPROM products are available with 168±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration (equivalent to MIL-STD-883B). This process exceeds or meets most industry specifications of burn-in.

The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to 85°C) EXPRESS products are available. EXPRESS products plus military grade EPROMs (−55°C to 125°C) provide the most complete choice of standard and extended temperature range EPROMs available.

Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.



PIN CONFIGURATION

FEBRUARY 1982
ORDER NUMBER: 210322-001

EXPRESS
EPROM Product Family

Type	Organization	Maximum Access (ns)	Power Supply	Operating Temperature (°C)	Burn-in 125°C (hr)
QD2716-1	2048x8	350	5V ± 10%	0 to 70	168±8
QD2716-2	2048x8	390	5V ± 5%	0 to 70	168±8
QD2716	2048x8	450	5V ± 5%	0 to 70	168±8
LD2716	2048x8	450	5V ± 5%	−40 to 85	168±8
TD2716	2048x8	450	5V ± 5%	−40 to 85	NONE
QD2732A-2	4096x8	200	5V ± 5%	0 to 70	168±8
QD2732A	4096x8	250	5V ± 5%	0 to 70	168±8
QD2732A-3	4096x8	300	5V ± 5%	0 to 70	168±8
QD2732A-4	4096x8	450	5V ± 5%	0 to 70	168±8
QD2732A-20	4096x8	200	5V ± 10%	0 to 70	168±8
QD2732A-25	4096x8	250	5V ± 10%	0 to 70	168±8
QD2732A-30	4096x8	300	5V ± 10%	0 to 70	168±8
LD2732A	4096x8	250	5V ± 5%	−40 to 85	168±8
LD2732A-4	4096x8	450	5V ± 5%	−40 to 85	168±8
LD2732A-25	4096x8	250	5V ± 10%	−40 to 85	168±8
LD2732A-45	4096x8	450	5V ± 10%	−40 to 85	168±8
TD2732A	4096x8	250	5V ± 5%	−40 to 85	NONE
TD2732A-4	4096x8	450	5V ± 5%	−40 to 85	NONE
TD2732A-25	4096x8	250	5V ± 10%	−40 to 85	NONE
TD2732A-45	4096x8	450	5V ± 10%	−40 to 85	NONE
QD2764-2	8192x8	200	5V ± 5%	0 to 70	168±8
QD2764	8192x8	250	5V ± 5%	0 to 70	168±8
QD2764-3	8192x8	300	5V ± 5%	0 to 70	168±8
QD2764-4	8192x8	450	5V ± 5%	0 to 70	168±8
QD2764-25	8192x8	250	5V ± 10%	0 to 70	168±8
QD2764-30	8192x8	300	5V ± 10%	0 to 70	168±8
QD2764-45	8192x8	450	5V ± 10%	0 to 70	168±8
LD2764*	8192x8	250	5V ± 5%	−40 to 85	168±8
LD2764-4*	8192x8	450	5V ± 5%	−40 to 85	168±8
LD2764-25*	8192x8	250	5V ± 10%	−40 to 85	168±8
LD2764-45*	8192x8	450	5V ± 10%	−40 to 85	168±8
TD2764*	8192x8	250	5V ± 5%	−40 to 85	NONE
TD2764-4*	8192x8	450	5V ± 5%	−40 to 85	NONE
TD2764-25*	8192x8	250	5V ± 10%	−40 to 85	NONE
TD2764-45*	8192x8	450	5V ± 10%	−40 to 85	NONE
QD27128*	16384x8	250	5V ± 5%	0 to 70	168±8
QD27128-4*	16384x8	450	5V ± 5%	0 to 70	168±8

AFN-02139A

*Preliminary

2816
16K (2K x 8) ELECTRICALLY ERASABLE PROM

- **HMOS*-E FLOTOX Cell Design**
- **Reliable Floating Gate Technology**
- **Very Fast Access Time:**
  —2816, 250 ns Max.
  —2816-3, 350 ns Max.
  —2816-4, 450 ns Max.
- **Single Byte Erase/Write Capability**
- **10 ms Byte Erase/Write Time**
- **Chip Erase Time of 10 ms**
- **Conforms to JEDEC Byte-Wide Family Standard**
- **Microprocessor Compatible Architecture**
- **Low Power Dissipation:**
  —Active Current, 110 mA Max.
  —Standby Current, 50 mA Max.
- **Erase/Write Specifications Guaranteed 0-70°C**

The Intel 2816 is a 16,384 bit electrically erasable programmable read-only memory (E^2PROM). The 2816 can be easily erased and reprogrammed on a byte basis. A chip erase function is also provided. The device operates from a 5-volt power supply in the read mode; writing and erasing are accomplished by providing a single 21-volt pulse.

The 2816, with its very fast read access speed, is compatible with high performance microprocessors such as the 8086-2. Using the fast access speed allows zero wait operation in large system configurations.

The electrical erase/write capability of the 2816 makes it ideal for a wide variety of applications requiring in-system, non-volatile erase and write. Never before has in-system alterability been possible with this combination of density, performance and flexibility. Any byte can be erased or written in 10 ms without affecting the data in any other byte. Alternatively, the entire memory can be erased in 10 ms allowing the total time to rewrite all 2K bytes to be cut by 50%. The 2816 provides a significant increase in flexibility allowing new applications (dynamic reconfiguration, continuous calibration) never before possible.

The 2816 E^2PROM possesses Intel's 2-line control architecture to eliminate bus contention in a system environment. A power down mode is also featured; in the standby mode power consumption is reduced by over 55% without increasing access time. The standby mode is achieved by applying a TTL-high signal to the CE input.

Byte erase and write are controlled entirely by TTL signal levels, yet require no control signals beyond $\overline{CE}$ and $\overline{OE}$. For byte write a selected chip ($\overline{CE}$ = TTL low) senses the 21V V_{PP} pulse and automatically goes into write mode. Byte erase mode is identical to byte write except that data-in must be all logic ones (TTL-high). Never before has an in-system alteration of non-volatile information been implemented with such simple control.

*HMOS-E is a patented process of Intel Corporation.

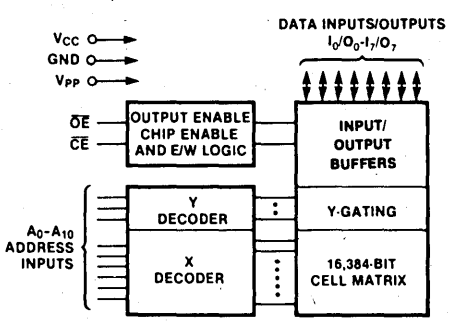


Figure 1. 2816 Functional Block Diagram

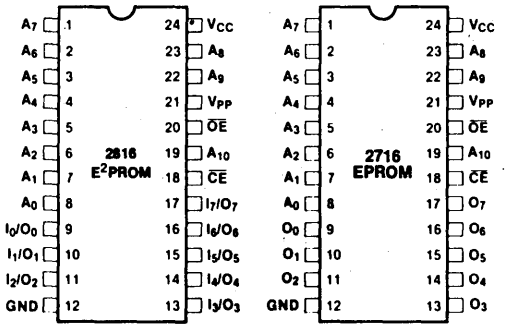


Figure 2. Pin Configuration

PIN NAMES

A_0-A_{10}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	DATA OUTPUTS
I_0-I_7	DATA INPUTS
V_{PP}	PROGRAM VOLTAGE

OCTOBER 1982

PRELIMINARY

2817

16K (2K X 8) ELECTRICALLY ERASABLE PROM

- **Self Timed Byte Write with Automatic Erase**
- **Direct Microprocessor Interface Capability**
- **Static 21 Volt V_{PP}**
- **Reduces Support Component Requirement by 70% to 90% Over 2816 and 2815**
- **Fast Byte Write Time:**
  —Write Typical, 5 mS
  —Cycle Typical, 10 mS
- **Very Fast Read Access Time:**
  —2817, 250 nS
  —2817-3, 350 nS
  —2817-4, 450 nS
- **Reliable Intel FLOTOX E^2PROM Technology**

The Intel 2817 is a 16,384 bit Electrically Erasable Programmable Read Only Memory. Like the Intel 2816 and 2815, it has completely Non-Volatile Data Storage. However, in addition, it offers a high degree of integrated functionality which enables in-circuit byte writes to be performed with minimal hardware and software overhead. The Intel 2817 is a product of Intel's advanced E^2PROM technology and uses the powerful HMOS*-E process for reliable, *non-volatile,* data storage.

The Intel 2817 eliminates all the interfacing hardware logic and firmware required to perform data writes. The device has complete self-timing which leaves the processor free to perform other tasks until the 2817 signals 'Ready.' With a transparent erase before write, the user benefits by saving an erase command contributing to efficient usage of system processing time. On chip latching further enhances system performance.

The Intel 2817's very fast read access time makes it compatible with high performance microprocessor applications. It uses Intel's proven 2-line control architecture which eliminates bus contention in a system environment. Combining these features with the 2817's 'Ready' signal makes the device an extremely powerful, yet simple to use, E^2 memory—available to the designer today.

The density, and level of integrated control, makes the Intel 2817 suitable for users requiring low hardware overhead, high system performance, minimal board space and design ease. Designing with, and using the 2817, is extremely cost effective as 70% of the required voltage and interfacing hardware required for other E^2PROM devices has been eliminated. See Figures 1, 2, and 3 for the Intel 2817's block diagram, pinout, and simple interface requirements.

*HMOS-E is a patented process of Intel Corporation.

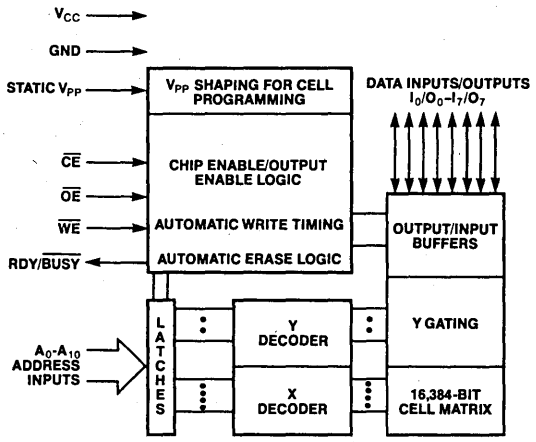


Figure 1. 2817 Functional Block Diagram

PIN NAMES

A_0-A_{10}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	DATA OUTPUTS
I_0-I_7	DATA INPUTS
V_{PP}	STATIC PROGRAMMING VOLTAGE
RDY/$\overline{BUSY}$	DEVICE READY/BUSY
TC	TIMING CAPACITOR
N.C.	NO CONNECT

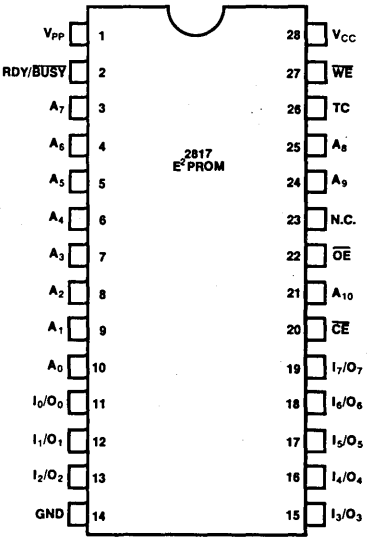


Figure 2. 2817 Pin Configuration

OCTOBER 1982
ORDER NO. 210255-003

3826
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Monolithic Memories MMI

Monolithic Memories MMI

Bipolar PROM Cross-Reference Guide

Memory Description				MMI	AMD	Fair-child	Fujitsu	Harris	Intel	Motorola	National	Raytheon	Signetics	TI
Size	Organization	Pins	Output											
256	32 x 8	16	OC	6330-1 63S080	27S18	—	—	7602	—	—	74S188	—	82S23	18SA030
			TS	6331-1 63S081	27S19	—	—	7603	—	—	74S288	—	82S123	18S030
1024	256 x 4	16	OC	6300-1 63S140 63LS140	27S20	—	—	7610	—	—	74S387	—	82S126	24SA10
			TS	6301-1 63S141 63LS141	27S21	—	—	7611	—	—	74S287	—	82S129	24S10
2048	256 x 8	20	IC	6308-1	—	—	—	—	—	—	—	—	—	18SA22
			TS	6309-1	—	—	—	—	—	—	—	—	—	18S22
		24	OC	6335-1	—	—	—	—	—	—	—	—	—	—
			TS	6336-1	—	—	—	—	—	—	—	—	—	—
2048	512 x 4	16	OC	6305-1 63S240 63LS240	27S12	—	—	7620	—	—	74S570	—	82S130	—
			TS	6306-1 63S241 63LS241	27S13	—	—	7621	—	—	74S571	29613	82S131	—
4096	512 x 8	20	OC	6348-1, -2	27S28	—	7120	7648	—	—	74S473	—	—	28SA42
			TS	6349-1, -2	27S29	—	7124	7649	—	—	74S472	29623	82S147	28S42
4096	512 x 8	24	OC	6340-1, -2	27S30	93438	—	7640	—	7640	74S475	—	—	28SA46
			TS	6341-1, -2	27S31	93448	—	7641	—	7641	74S474	—	82S141	28S46
4096	1024 x 4	18	OC	6352-1	27S32	93452	—	7642	—	7642	74S572	29640	—	24SA41
			TS	6353-1 63S441 63S441A	27S33	93453	7122	7643	—	7643	74S573	29641	82S137	24S41
			TS	63RA441	—	—	—	—	—	—	—	—	—	—
8192	1024 x 8	24	OC	6380-1, -2	27S180	93450	—	7680	—	7680	87S180	—	82S180	28SA86
			TS	6381-1, -2	27S181	93451	7132	7681	3628	7681	87S181	29631	82S181	28S86
8192	2048 x 4	18	OC	6388-1	27S184	93514	7127	7684	—	7684	87S184	—	82S184	24SA81
			TS	6389-1, -2 63S841 63S841A	27S185	93515	7128	7685	—	7685	87S185	29653	82S185	24S81
16384	4096 x 4	20	TS	63S1641 63S1641A	27S41	93513	7134	76165	—	—	—	29653	82S195	—

NOTE: Only Commercial Specification part numbers are listed.

High Performance 32x8 Ti-W PROM 53/63S080 53/63S081

Features/Benefits

- 9ns typical access time
- Reliable Titanium-Tungsten fuses (Ti-W)
- Low voltage generic programming
- Pin compatible with standard Schottky PROMs
- PNP inputs for low input current

Applications

- Programmable logic element
- Address decoder
- Priority encoder
- Random logic replacement

Description

The 53/63S080 and 53/63S081 features low input current PNP inputs, full Schottky clamping and three-state and open collector outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on chip circuitry and extra fuses provide preprogramming testing which assure high programming yields and high reliablity.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

Programming

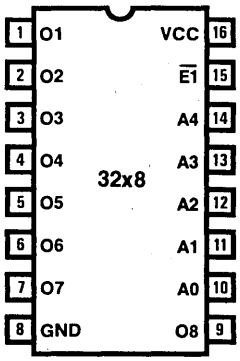
The 53/63S080 and 53/63S081 are programmed with the same programming algorithm as all other Monolithic Memories' generic Ti-W PROMs. For details refer to Monolithic Memories' LSI Data Book.

Selection Guide

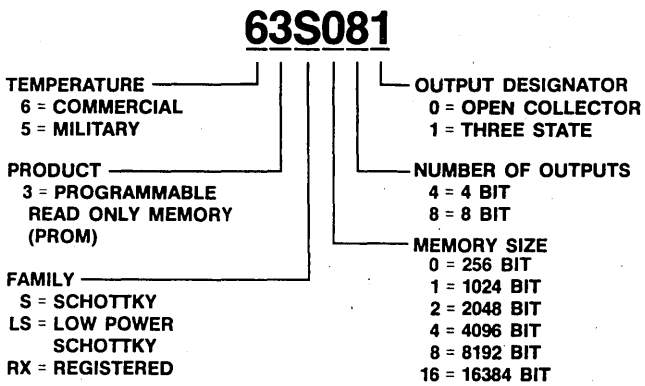
MEMORY			PACKAGE		DEVICE TYPE	
SIZE	ORGANIZATION		PINS	TYPE	0°C to +75°C	-55°C to +125°C
1/4 K	32x8	O.C.	16	N, J	63S080	53S080
		T.S.			63S081	53S081

Pin Configuration

53/63S080
53/63S081



Part Numbering System



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Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 7V
Off-state output voltage 5.5V
Storage temperature ..... –65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = –18mA				–1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V				–0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 16mA	MIL			0.5	V
				COM			0.45	
V_{OH}	High-level output voltage*	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL I_{OH} = –2mA		2.4			V
			COM I_{OH} = –3.2mA					
I_{OZL}	Off-state output current *	V_{CC} = MAX	V_O = 0.4V				–40	μA
I_{OZH}			V_O = 2.4V				40	μA
I_{CEX}	Open collector output current	V_{CC} = MAX	V_O = 2.4V				40	μA
			V_O = 5.5V				100	
I_{OS}	Output short-circuit current*,**	V_{CC} = 5V	V_O = 0V		–20		–90	mA
I_{CC}	Supply current	V_{CC} = MAX	All inputs grounded. All outputs open.			90	125	mA

* Three-state only

** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

†Typicals at 5.0V V_{CC} and 25°C TAA

Switching Characteristics

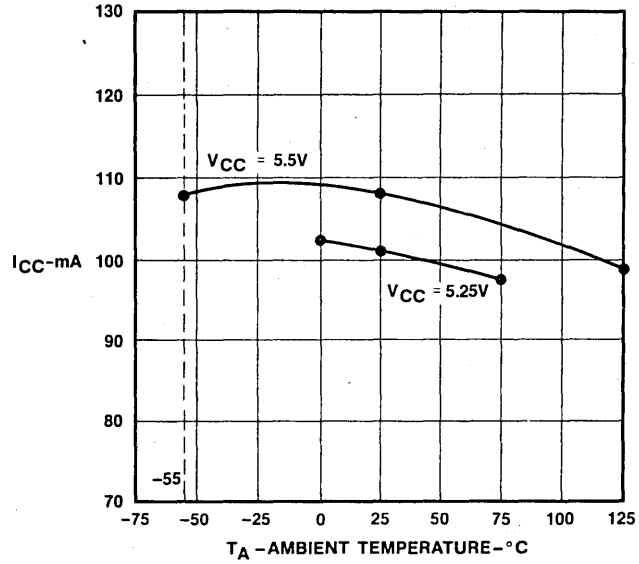
Over Operating Conditions

DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME TYP†	t_{AA} (ns) ADDRESS ACCESS TIME MAX	t_{EA} AND t_{ER} (ns) ENABLE ACCESS AND RECOVERY TIME TYP†	t_{EA} AND t_{ER} (ns) ENABLE ACCESS AND RECOVERY TIME MAX	CONDITIONS (See standard test load) R1(Ω)	CONDITIONS (See standard test load) R2(Ω)
63S080/1	9	25	9	20	300	600
53S080/1	9	35	9	30		

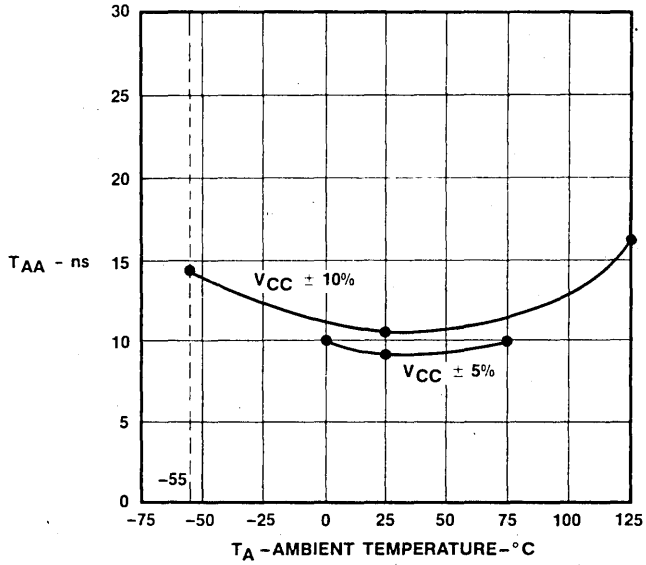
†Typicals at 5.0 V_{CC} and 25°C TA.

53/63S081

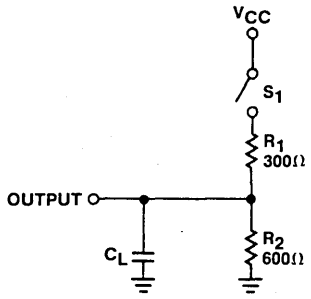
Typical I_{CC} vs Temperature



Typical T_{AA} vs Temperature



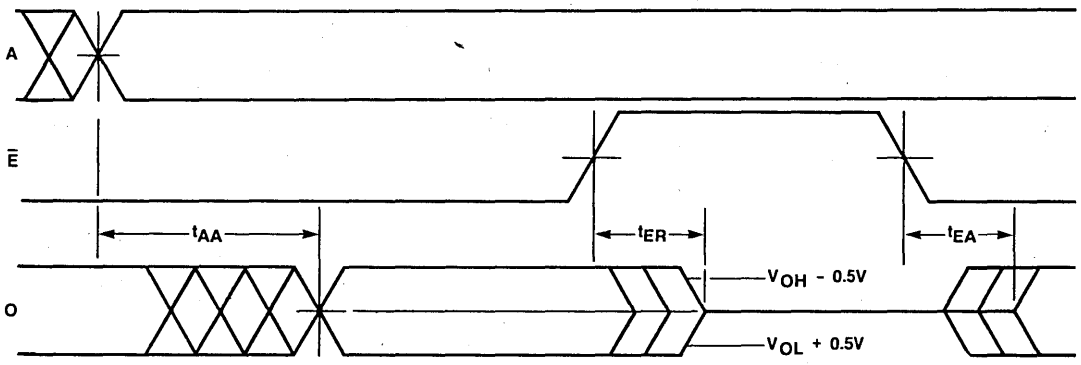
Switching Test Load



Definition of Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

Definition of Waveforms



NOTES: 1. Input pulse amplitude 0V to 3.0V.

2. Input rise and fall times 5ns from 1.0V to 2.0V.
3. Input access measured at the 1.5V level.
4. t_{AA} is tested with switch S_1 closed, C_L = 30pF and measured at 1.5V output level.
5. For open collector devices. TEA and TER are measured at the 1.5V output level with S_1 closed and C_L = 30pF.
6. For three-state devices, TEA is measured at the 1.5V output level with C_L = 30pF. S_1 is open for high impedance to "1" test and closed for high impedance to "0" test.

   TER is tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH} - 0.5 output level; S_1 is closed for "0" to high impedance test measured at V_{OL} + 0.5V output level.

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High Performance 1024x4 PROM Ti-W PROM Family

53/63S441
53/63S441A

Features/Benefits

- 23ns typical access time
- Reliable Titanium-Tungsten fuses (Ti-W)
- Low voltage generic programming
- Pin compatible with standard Schottky PROMs
- PNP inputs for low input current
- Three state outputs

Applications

- Microprogram control stores
- Microprocessor program store
- Look up table
- Character generator
- Code converter

Description

The 5/63S441 features low input current PNP inputs, full Schottky clamping and three-state outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on chip circuitry and extra fuses provide pre-programming testing which assure high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

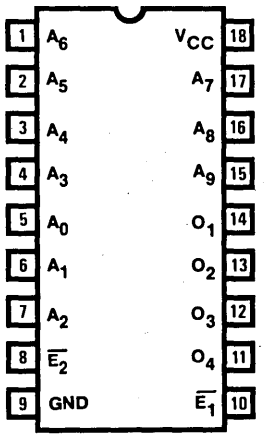
Programming

The 5/63S441 PROM is programmed with the same programming alogrithm as all other Monolithic Memories' generic Ti-W PROMs. For details refer to Monolithic Memories' LSI Data Book.

Selection Guide

MEMORY			PACKAGE	PERFORMANCE	PART NUMBER	
SIZE	ORGANIZATION	OUTPUT			0°C to +75°C	-55°C to +125°C
4K	1Kx4	TS	J	STANDARD	63S441	53S441
				ENHANCED	63S441A	53S441A

Pin Configuration



Part Numbering System

63S441A

TEMPERATURE
6 = COMMERCIAL
5 = MILITARY

PRODUCT
3 = PROGRAMMABLE READ ONLY MEMORY (PROM)

FAMILY
S = SCHOTTKY
LS = LOW POWER SCHOTTKY
RX = REGISTERED

MEMORY SIZE
0 = 256 BIT
1 = 1024 BIT
2 = 2048 BIT
4 = 4096 BIT
8 = 8192 BIT
16 = 16384 BIT

NUMBER OF OUTPUTS
4 = 4 BIT
8 = 8 BIT

OUTPUT DESIGNATOR
0 = OPEN COLLECTOR
1 = THREE STATE

PERFORMANCE
NONE = STANDARD
A = ENHANCED

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Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 7V
Off-state output voltage 5.5V
Storage temperature ..... –65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	–55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = –18mA				–1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V				–0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 16mA	MIL			0.5	V
				COM			0.45	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL I_{OH} = –2mA		2.4			V
			COM I_{OH} = –3.2mA					
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4V				–40	μA
I_{OZH}			V_O = 2.4V				40	
I_{OS}	Output short-circuit current *	V_{CC} = 5V	V_O = 0V		–20		–90	mA
I_{CC}	Supply current	V_{CC} = MAX All inputs grounded. All outputs open.				95	140	mA

*Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
†Typicals at 5.0V V_{CC} and 25°C T_A.

Switching Characteristics Over Operating Conditions

DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME TYP†	t_{AA} (ns) ADDRESS ACCESS TIME MAX	t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME TYP†	t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME MAX	CONDITIONS (See standard test load) R1(Ω)	CONDITIONS (See standard test load) R2(Ω)
63S441	23	45	12	25	300	600
53S441	23	55	12	30		
63S441A	23	35	12	25		
53S441A	23	50	12	30		

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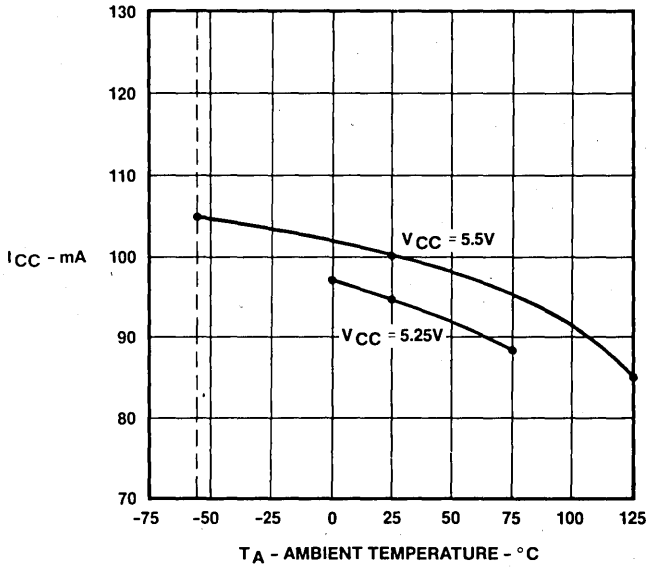
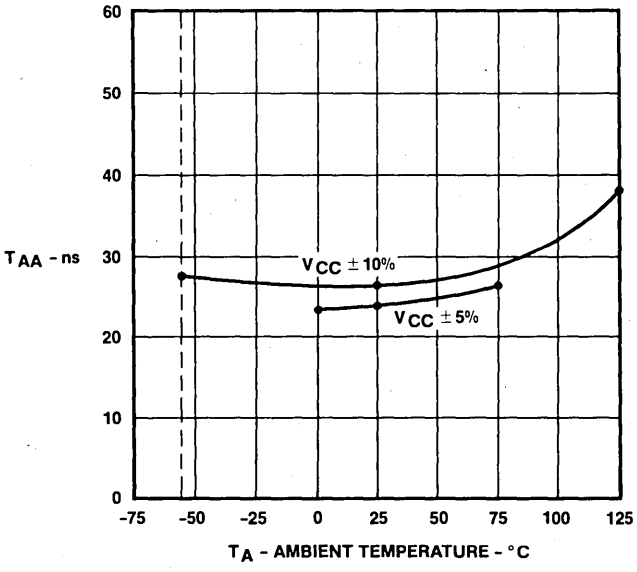
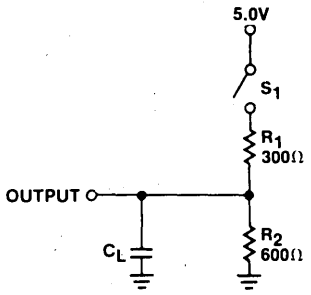
Typical I_{CC} vs Temperature



Typical T_{AA} vs Temperature



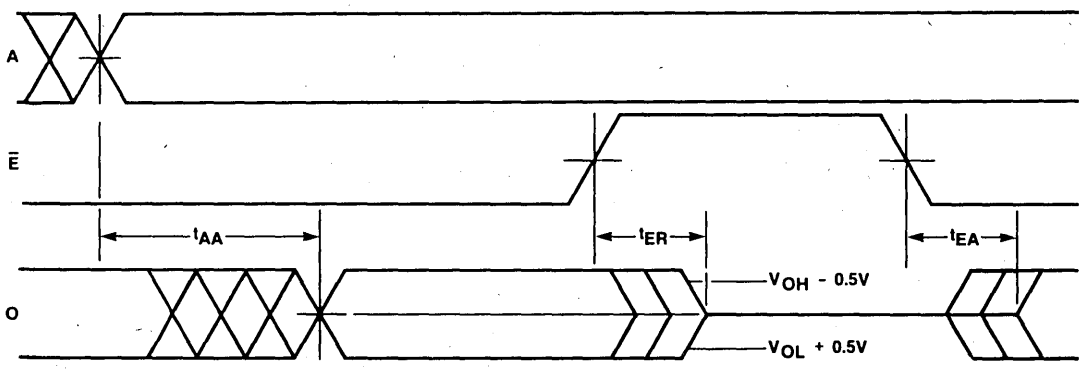
Switching Test Load



Definition of Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

Definition of Waveforms



NOTES: 1. Input pulse amplitude 0V to 3.0V.

2. Input rise and fall times 5ns from 1.0V to 2.0V.
3. Input access measured at the 1.5V level.
4. t_{AA} is tested with switch S_1 closed, C_L = 30pF and measured at 1.5V output level.
5. TEA is measured at the 1.5V output level with C_L = 30 pF. S_1 is open for high impedance to "1" test and closed for high impedance to "1" test and closed for high impednace to "0" test.

   TER is tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH} - 0.5 output level; S_1 is closed for "0" to high impedance test measured at V_{OL} + 0.5V output level.

High Performance 2048x4 PROM Ti-W PROM Family

53/63S841 53/63S841A

Features/Benefits

- 28ns typical access time
- Reliable Titanium-Tungsten fuses (Ti-W)
- Low voltage generic programming
- Pin compatible with standard Schottky PROMs
- PNP inputs for low input current
- Three state outputs

Applications

- Microprogram control stores
- Microprocessor program store
- Look up table
- Character generator
- Code converter

Description

The 5/63S841 features low input current PNP inputs, full Schottky clamping and three-state outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on chip circuitry and extra fuses provide pre-programming testing which assure high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

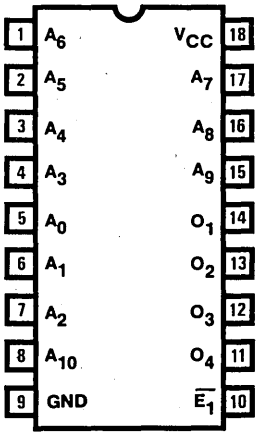
Programming

The 5/63S841 PROM is programmed with the same programming algorithm as all other Monolithic Memories' generic Ti-W PROMs. For details refer to Monolithic Memories' LSI Data Book.

Selection Guide

MEMORY			PACKAGE	PERFORMANCE	PART NUMBER	
SIZE	ORGANIZATION	OUTPUT			0°C to +75°C	-55°C to +125°C
8K	2Kx4	TS	J	STANDARD	63S841	53S841
				ENHANCED	63S841A	53S841A

Pin Configuration



Part Numbering System

63S841A

- TEMPERATURE: 6 = COMMERCIAL; 5 = MILITARY
- PRODUCT: 3 = PROGRAMMABLE READ ONLY MEMORY (PROM)
- FAMILY: S = SCHOTTKY; LS = LOW POWER SCHOTTKY; RX = REGISTERED
- MEMORY SIZE: 0 = 256 BIT; 1 = 1024 BIT; 2 = 2048 BIT; 4 = 4096 BIT; 8 = 8192 BIT; 16 = 16384 BIT
- NUMBER OF OUTPUTS: 4 = 4 BIT; 8 = 8 BIT
- OUTPUT DESIGNATOR: 0 = OPEN COLLECTOR; 1 = THREE STATE
- PERFORMANCE: NONE = STANDARD; A = ENHANCED

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Monolithic Memories

Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 7V
Off-state output voltage 5.5V
Storage temperature ..... –65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	–55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = –18mA				–1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V				–0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	I_{OL} = 16mA	MIL			0.5	V
				COM			0.45	
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL I_{OH} = –2mA		2.4			V
			COM I_{OH} = –3.2mA					
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4V				–40	μA
I_{OZH}			V_O = 2.4V				40	
I_{OS}	Output short-circuit current *	V_{CC} = 5V	V_O = 0V		–20		–90	mA
I_{CC}	Supply current	V_{CC} = MAX All inputs grounded. All outputs open.				110	150	mA

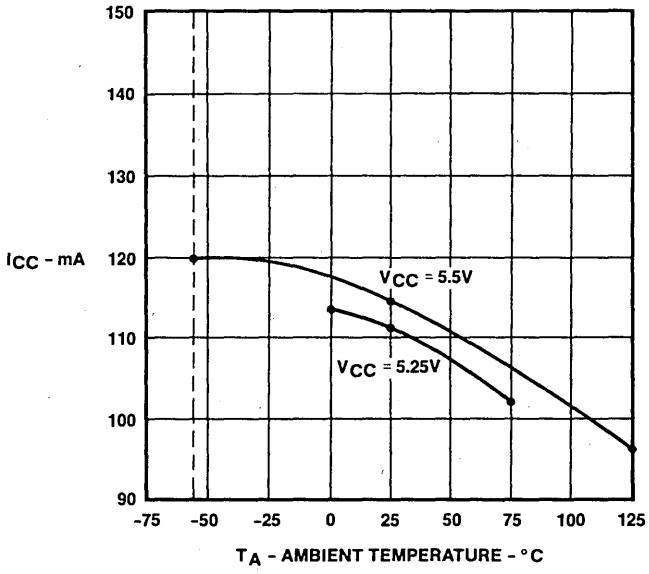
*Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

†Typicals at 5.0V V_{CC} and 25°C T_A.

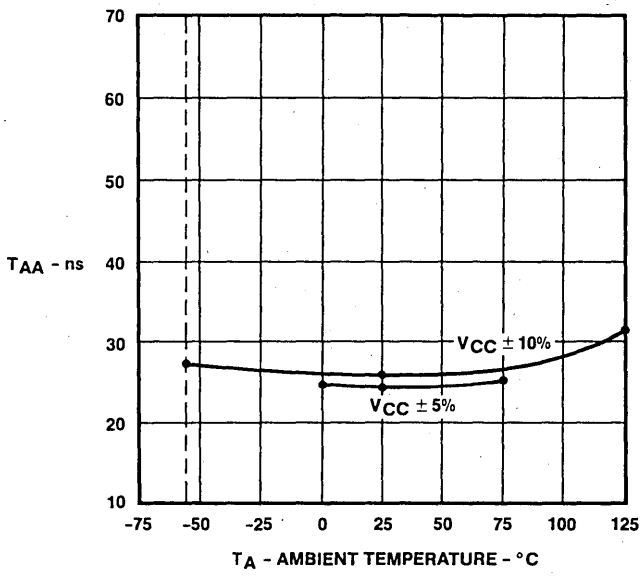
Switching Characteristics Over Operating Conditions

DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME TYP†	t_{AA} (ns) ADDRESS ACCESS TIME MAX	t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME TYP†	t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME MAX	CONDITIONS (See standard test load) R1(Ω)	CONDITIONS (See standard test load) R2(Ω)
63S841	28	50	12	25	300	600
53S841	28	55	12	30		
63S841A	28	35	12	25		
53S841A	28	50	12	30		

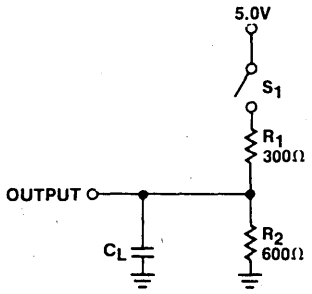
Typical I_{CC} vs Temperature



Typical T_{AA} vs Temperature



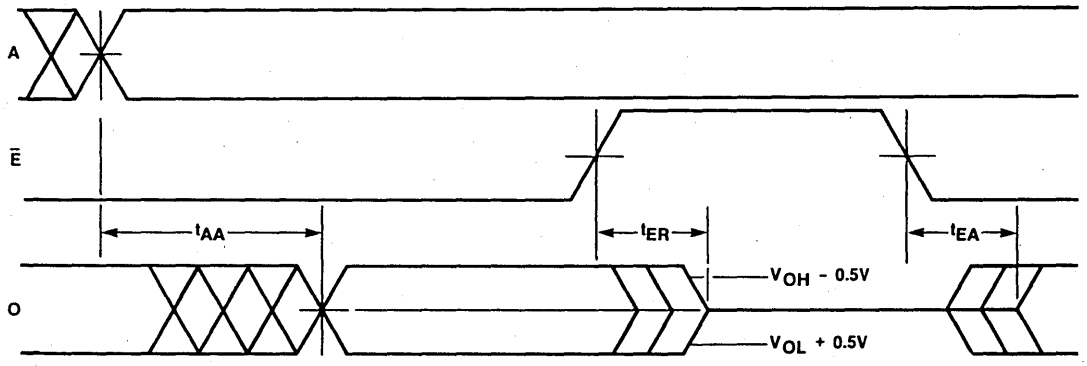
Switching Test Load



Definition of Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

Definition of Waveforms



NOTES: 1. Input pulse amplitude 0V to 3.0V.

2. Input rise and fall times 2-5ns from 1.0V to 2.0V.
3. Input access measured at the 1.5V level.
4. t_{AA} is tested with switch S_1 closed, C_L = 30pF and measured at 1.5V output level.
5. TEA is measured at the 1.5V output level with C_L = 30 pF. S_1 is open for high impedance to "1" test and closed for high impedance to "1" test and closed for high impednace to "0" test.

   TER is tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH} - 0.5 output level; S_1 is closed for "0" to high impedance test measured at V_{OL} + 0.5V output level.

1165 East Arques Avenue, Sunnyvale, CA 94086 Tel: (408) 739-3535 TWX: 910-339-9229

High Performance 4096x4 PROM Ti-W PROM Family

53/63S1641 53/63S1641A

Features/Benefits

- 28ns typical access time
- Reliable Titanium-Tungsten fuses (Ti-W)
- Low voltage generic programming
- Pin compatible with standard Schottky PROMs
- PNP inputs for low input current

Applications

- Microprogram control stores
- Microprocessor program store
- Look up table
- Character generator
- Code converter

Description

The 5/63S1641 features low input current PNP inputs, full Schottky clamping and three-state outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on chip circuitry and extra fuses provide pre-programming testing which assure high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

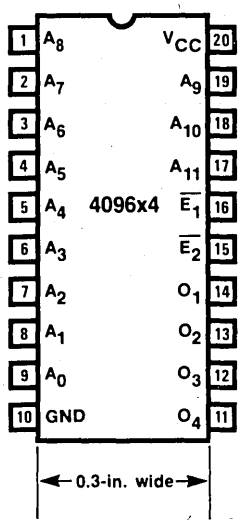
Programming

The 5/63S1641 PROM is programmed with the same programming algorithm as all other Monolithic Memories' generic Ti-W PROMs. For details refer to Monolithic Memories' LSI Data Book.

Selection Guide

MEMORY			PACKAGE	PERFORMANCE	PART NUMBER	
SIZE	ORGANIZATION	OUTPUT			0°C to +75°C	-55°C to +125°C
16K	4Kx4	TS	J	STANDARD	63S1641	53S1641
				ENHANCED	63S1641A	53S1641A

Pin Configuration



Part Numbering System

63S1641A

- TEMPERATURE: 6 = COMMERCIAL; 5 = MILITARY
- PRODUCT: 3 = PROGRAMMABLE READ ONLY MEMORY (PROM)
- FAMILY: S = SCHOTTKY; LS = LOW POWER SCHOTTKY; RX = REGISTERED
- MEMORY SIZE: 0 = 256 BIT; 1 = 1024 BIT; 2 = 2048 BIT; 4 = 4096 BIT; 8 = 8192 BIT; 16 = 16384 BIT
- NUMBER OF OUTPUTS: 4 = 4 BIT; 8 = 8 BIT
- OUTPUT DESIGNATOR: 0 = OPEN COLLECTOR; 1 = THREE STATE
- PERFORMANCE: NONE = STANDARD; A = ENHANCED

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Monolithic Memories

Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 7V
Off-state output voltage 5.5V
Storage temperature ..... −65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	−55		125	0		75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA				−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V				−0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = V_{CC} MAX				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	I_{OL} = 16mA	MIL			0.5	V
				COM			0.45	
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL I_{OH} = −2mA		2.4			V
			COM I_{OH} = −3.2mA					
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4V				−40	μA
I_{OZH}			V_O = 2.4V				40	
I_{OS}	Output short-circuit current*	V_{CC} = 5V	V_O = 0V		−20		−90	mA
I_{CC}	Supply current	V_{CC} = MAX	All inputs grounded. All outputs open.			130	175	mA

*Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
†Typicals at 5.0V V_{CC} and 25°C T_A.

Switching Characteristics Over Operating Conditions

DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME		t_{EA} AND t_{ER} (ns) ENABLE ACCESS TIME RECOVERY TIME		CONDITIONS (See standard test load)	
	TYP†	MAX	TYP†	MAX	R1(Ω)	R2(Ω)
63S1641	28	50	12	25	300	600
53S1641	28	65	12	30		
63S1641A	28	35	12	25		
53S1641A	28	50	12	30		

†Typicals at 5.0V V_{CC} and 25°C T_A.

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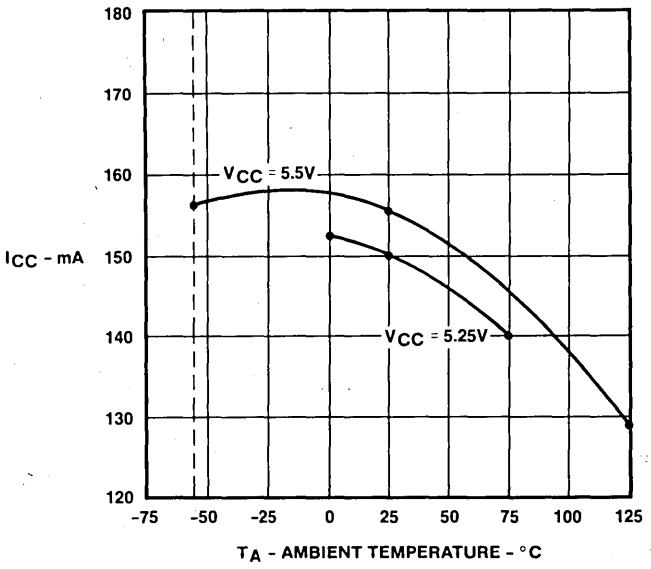
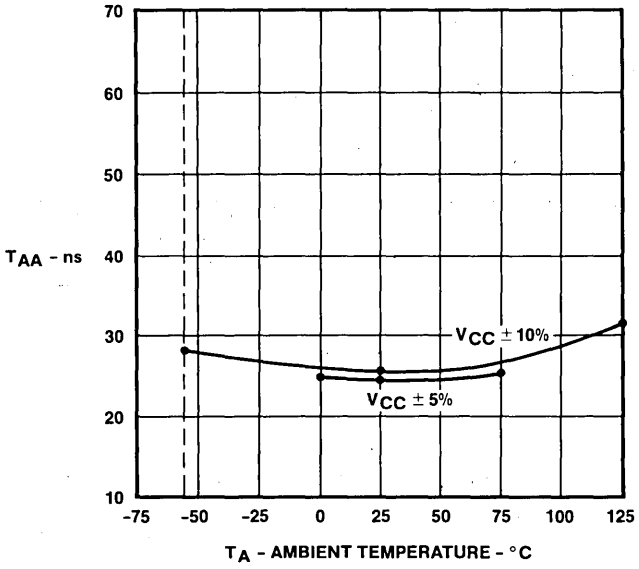
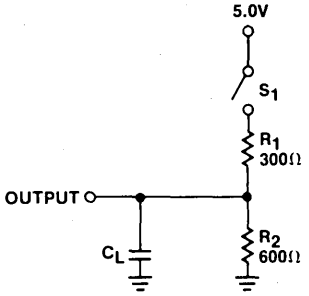
Typical I_{CC} vs Temperature



Typical T_{AA} vs Temperature



Switching Test Load



Definition of Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
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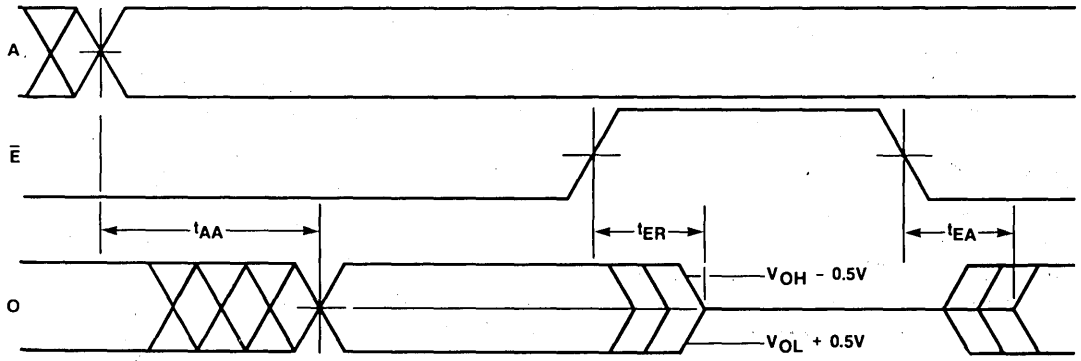
Definition of Waveforms



NOTES: 1. Input pulse amplitude 0V to 3.0V.

2. Input rise and fall times 2-5ns from 1.0V to 2.0V.
3. Input access measured at the 1.5V level.
4. t_{AA} is tested with switch S_1 closed, C_L = 30pF and measured at 1.5V output level.
5. TEA is measured at the 1.5V output level with C_L = 30pF. S_1 is open for high impedance to "1" test and closed for high impedance to "1" test and closed for high impedance to "0" test.
   TER is tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH} - 0.5 output level; S_1 is closed for "0" to high impedance test measured at V_{OL} + 0.5V output level.

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MOTOROLA

SEMICONDUCTORS

3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

Memory Selector Guide

Motorola has developed a very broad range of reliable MOS and bipolar memories for virtually any digital data processing system application. And for those whose requirements go beyond individual components, Motorola also supplies Memory Systems and Micromodules.

New Motorola memories are being introduced continually. This selector guide lists all those available as of December 1982. For later releases, additional technical information or pricing, contact your nearest authorized Motorola distributor or Motorola sales office.

RAMs

MOS DYNAMIC RAMs

Organization	Part Number	Access Time (ns Max)	Power Supplies	No. of Pins
16384 × 1	MCM4116BP15	150	+ 12, ±5 V	16
16384 × 1	MCM4116BP20	200	+ 12, ±5 V	16
16384 × 1	MCM4116BP25	250	+ 12, ±5 V	16
16384 × 1	MCM4517P10	100	+5 V	16
16384 × 1	MCM4517P12	120	+5 V	16
16384 × 1	MCM4517P15	150	+5 V	16
16384 × 1	MCM4517P20	200	+5 V	16
65536 × 1	MCM6664AP15[1]	150	+5 V	16
65536 × 1	MCM6664AP20[1]	200	+5 V	16
65536 × 1	MCM6665AP12	120	+5 V	16
65536 × 1	MCM6665AP15	150	+5 V	16
65536 × 1	MCM6665AP20	200	+5 V	16

MOS STATIC RAMs (+5 Volts)

Organization	Part Number	Access Time (ns max)	No. of Pins
128 × 8	MCM6810	450	24
128 × 8	MCM68A10	360	24
128 × 8	MCM68B10	250	24
1024 × 4	MCM2114P20	200	18
1024 × 4	MCM2114P25	250	18
1024 × 4	MCM2114P30	300	18
1024 × 4	MCM2114P45	450	18
1024 × 4	MCM21L14P20	200	18
1024 × 4	MCM21L14P25	250	18
1024 × 4	MCM21L14P30	300	18
1024 × 4	MCM21L14P45	450	18
2048 × 8	MCM2016HP45*	45	24
2048 × 8	MCM2016HP55*	55	24
2048 × 8	MCM2016HP70*	70	24

CMOS STATIC RAMs (+5 Volts)

Organization	Part Number	Access Time (ns max)	No. of Pins
2048 × 8	MCM65116P12*	120	24
2048 × 8	MCM65116P15*	150	24
2048 × 8	MCM65116P20*	200	24
4096 × 1	MCM65147P55	55	18
4096 × 1	MCM65147P70	70	18

*To be introduced.
(Not all speed selections shown)

[1]Motorola's innovative pin #1 refresh

Operating temperature ranges:
MOS – 0°C to 70°C
ECL – Consult individual data sheets
TTL – Military –55°C to +125°C, Commercial 0°C to 70°C

TTL RAMs

Organization	Part Number	Access Time (ns max)	Output	No. of Pins
256 × 4	MCM93422	45	3-State	22
256 × 4	MCM93L422	60	3-State	22
1024 × 1	MCM93415	45	Open Collector	16
1024 × 4	MCM93425	45	3-State	16

ECL RAMs

Organization	Part Number	Access Time (ns max)	No. of Pins
8 × 2	MCM10143	15	24
16 × 4	MCM10145A	6	16
64 × 1	MCM10148	15	16
128 × 1	MCM10147	15	16
256 × 1	MCM10144	26	16
256 × 1	MCM10152	15	16
256 × 4	MCM10422	15	24
1024 × 1	MCM10146	29	16
1024 × 1	MCM10415	20	16
1024 × 1	MCM10415A	15	16
1024 × 4	MCM10474*	25	24
4096 × 1	MCM10470A*	15	18

EPROMs

MOS EPROMs

Organization	Part Number	Access Time (ns max)	Power Supplies	No. of Pins
8192 × 8	MCM68764C	450	+5 V	24
8192 × 8	MCM68766C	450	+5 V	24
8192 × 8	MCM68766C35	350	+5 V	24

EEPROMs

MOS EEPROMs

Organization	Part Number	Access Time (ns max)	Power Supplies	No. of Pins
16 × 16	MCM2801P	10 μs	+5 V	14
32 × 32	MCM2802P*	15 μs	+5 V	14
4096 × 8	MCM2832P*	150 ns	+5 V	28

ROMs

MOS STATIC ROMs (+5 Volts)

Character Generators[2]

Organization	Part Number	Access Time (ns max)	No. of Pins
128 × (7 × 5)	MCM6670P	350	18
128 × (7 × 5)	MCM6674P	350	18
128 × (9 × 7)	MCM66700P	350	24
128 × (9 × 7)	MCM66710P	350	24
128 × (9 × 7)	MCM66714P	350	24
128 × (9 × 7)	MCM66720P	350	24
128 × (9 × 7)	MCM66730P	350	24
128 × (9 × 7)	MCM66734P	350	24
128 × (9 × 7)	MCM66740P	350	24
128 × (9 × 7)	MCM66750P	350	24
128 × (9 × 7)	MCM66760P	350	24
128 × (9 × 7)	MCM66770P	350	24
128 × (9 × 7)	MCM66780P	350	24
128 × (9 × 7)	MCM66790P	350	24

Binary ROMs (+5 Volts)

Organization	Part Number	Access Time (ns max)	No. of Pins
1024 × 8	MCM68A308P	350	24
1024 × 8	MCM68A308P7[3]	350	24
1024 × 8	MCM68B308P	250	24
2048 × 8	MCM68A316EP	350	24
2048 × 8	MCM68A316EP91[3]	350	24
4096 × 8	MCM68A332P	350	24
4096 × 8	MCM68A332P2[3]	350	24
8192 × 8	MCM68364P35	350	24
8192 × 8	MCM68364P35-3[3]	350	24
8192 × 8	MCM68364P25	250	24
8192 × 8	MCM68364P20	200	24
8192 × 8	MCM68365P25	250	24
8192 × 8	MCM68365P35	350	24
8192 × 8	MCM68366P25	250	24
8192 × 8	MCM68366P35	350	24

CMOS ROMs (+5 Volts)

Organization	Part Number	Access Time (ns max)	No. of Pins
256 × 4	MCM14524	1200	16
2048 × 8	MCM65516P43	430	18
2048 × 8	MCM65516P43M[3]	430	18
2048 × 8	MCM65516P55	550	18

[2]Character generators include shifted and unshifted characters, ASCII alphanumeric control, math, Japanese, British, German, European and French symbols.

[3]Standard Patterns for MOS ROMs:
MCM68A308P7 – MC6800 MIKbug/MINIbug ROM
MCM68A316EP91 – Universal Code Converter and Character Generator
MCM68A332P2 – Sine/Cosine Look-Up Table
MCM68364P35-3 – Log/Antilog Look-Up Table
MCM65516P43M – MC146805 Monitor Program

PROMs

ECL PROMs

Organization	Part Number	Access Time (ns max)	No. of Pins
32 × 8	MCM10139	20	16
256 × 4	MCM10149	25	16

TTL PROMs

Organization	Part Number	Access Time (ns max)	Output	No. of Pins
512 × 4	MCM7621A	60	3-State	16
512 × 8	MCM7641	70	3-State	24
512 × 8	MCM7641A	60	3-State	24
512 × 8	MCM7649*	70	3-State	20
512 × 8	MCM7649A*	50	3-State	20
1024 × 4	MCM7643	70	3-State	18
1024 × 4	MCM7643A	50	3-State	18
1024 × 8	MCM7681	70	3-State	24
1024 × 8	MCM7681A	50	3-State	24
2048 × 4	MCM7685	70	3-State	18
2048 × 4	MCM7685A	55	3-State	18
2048 × 8	MCM76161	70	3-State	24
2048 × 8	MCM76161A	50	3-State	24
4096 × 4	MCM76165*	35	3-State	20

MOTOROLA
SEMICONDUCTORS
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MCM6256

Product Preview

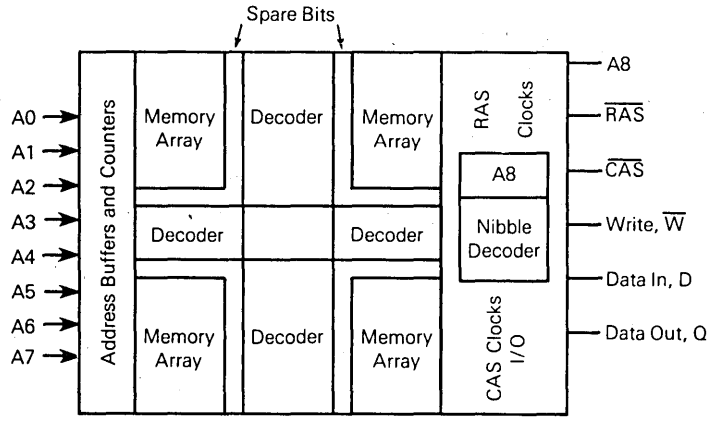
256K-BIT DYNAMIC RAM

The MCM6256 is a 262,144 bit, high-speed, dynamic Random Access Memory. Organized as 262,144 one-bit words and fabricated using Motorola's high-performance silicon-gate MOS (HMOS) technology, this new single +5 volt supply dynamic RAM combines high performance with low cost and improved reliability. The MCM6256 has the capability of using laser fuse redundancy and is manufactured using advanced direct-step on wafer photolithographic equipment.

By multiplexing row and column address inputs, the MCM6256 requires only nine address lines and permits packaging in standard 16-pin 300 mil wide dual-in-line packages. Complete address decoding is done on-chip with address latches incorporated. Data out (Q) is controlled by $\overline{CAS}$ allowing greater system flexibility.

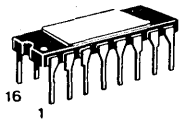
All inputs and outputs, including clocks, are fully TTL compatible. The MCM6256 incorporates a one transistor cell design and dynamic storage techniques. In addition to the $\overline{RAS}$-only refresh mode, a $\overline{CAS}$ before $\overline{RAS}$ automatic refresh is available. Another special feature of the MCM6256 is nibble mode, allowing the user to serially access 4 bits of data at a high data rate. Nibble mode address is controlled by the addresses on pin 1 (A8 row and A8 column).

- Organized as 262,144 Words of 1 Bit
- Single +5 Volt Operation (±10%)
- Maximum Access Time:
  MCM6256-10 = 100 ns
  MCM6256-12 = 120 ns
  MCM6256-15 = 150 ns
- Low Power Dissipation:
  70 mA maximum (Active) MCM6256-10
  4 mA maximum (Standby)
- Three-State Data Output
- Early-Write Common I/O Capability
- 256 Cycle, 4 ms Refresh
- $\overline{RAS}$-Only Refresh Mode
- Automatic ($\overline{CAS}$ before $\overline{RAS}$) Refresh Mode
- Fast Nibble Mode on Read and Write Cycles
  20 ns Access Time
  40 ns Cycle Time



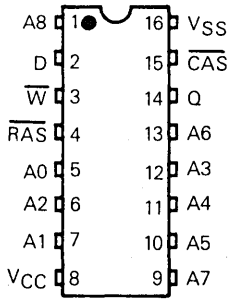
MOS
(N-CHANNEL, SILICON-GATE)

262,144 BIT DYNAMIC RANDOM ACCESS MEMORY



L SUFFIX
CERAMIC PACKAGE
CASE 690

PIN ASSIGNMENT



PIN NAMES	
A0-A8	Address Input
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

NP-352

MOTOROLA
SEMICONDUCTORS
3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MCM6664A

Advance Information

MOS
(N-CHANNEL, SILICON-GATE)

65,536-BIT DYNAMIC RANDOM ACCESS MEMORY

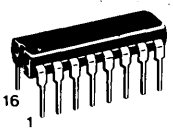
64K-BIT DYNAMIC RAM

The MCM6664A is a 65,536 bit, high-speed, dynamic Random-Access Memory. Organized as 65,536 one-bit words and fabricated using HMOS high-performance N-channel silicon-gate technology, this new breed of 5-volt only dynamic RAM combines high performance with low cost and improved reliability.

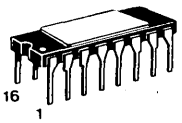
By multiplexing row- and column-address inputs, the MCM6664A requires only eight address lines and permits packaging in standard 16-pin dual-in-line packages. Complete address decoding is done on chip with address latches incorporated. Data out is controlled by $\overline{CAS}$ allowing for greater system flexibility.

All inputs and outputs, including clocks, are fully TTL compatible. The MCM6664A incorporates a one-transistor cell design and dynamic storage techniques. In addition to the $\overline{RAS}$-only refresh mode, the refresh control function available on pin 1 provides two additional modes of refresh, automatic and self refresh.

- Organized as 65,536 Words of 1 Bit
- Single 5 Volt Operation (±10%)
- Maximum Access Time: MCM6664A-12 = 120 ns
  MCM6664A-15 = 150 ns
  MCM6664A-20 = 200 ns
- Low Power Dissipation
  302.5 mW Maximum (Active) (MCM6664A-15)
  22 mW Maximum (Standby)
- Three-State Data Output
- Early-Write Common I/O Capability
- 16K Compatible 128-Cycle, 2 ms Refresh
- Control on Pin 1 for Automatic or Self Refresh
- $\overline{RAS}$-only Refresh Mode
- $\overline{CAS}$ Controlled Output
- Fast Page Mode Cycle Time
- Low Soft Error Rate <0.1% per 1000 Hours (See Soft Error Testing)

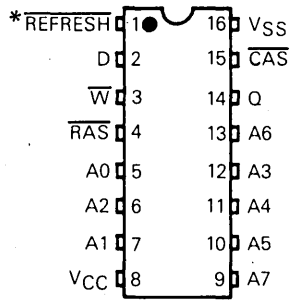


P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 690

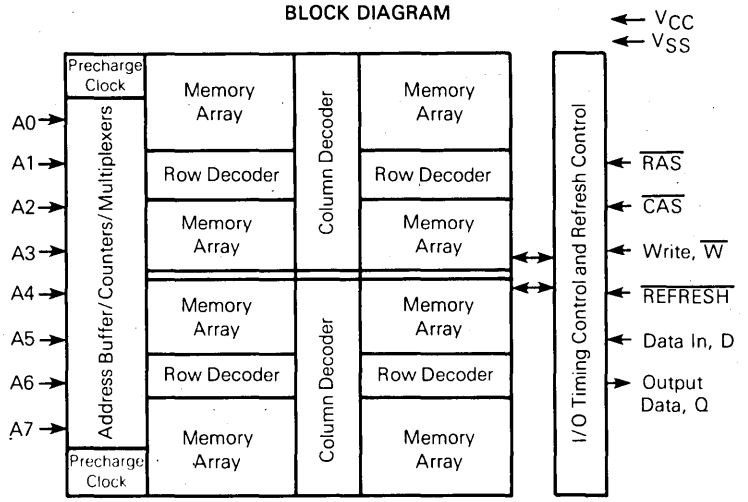
PIN ASSIGNMENT



*If pin is not used, it should be connected to V_{CC} through a 10 k resistor.

PIN NAMES	
$\overline{REFRESH}$	Refresh
A0-A7	Address Input
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground

BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MOTOROLA
SEMICONDUCTORS
3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MCM6665A

MOS
(N-CHANNEL, SILICON-GATE)

65,536-BIT DYNAMIC RANDOM ACCESS MEMORY

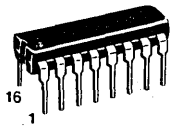
64K BIT DYNAMIC RAM

The MCM6665A is a 65,536 bit, high-speed, dynamic Random-Access Memory. Organized as 65,536 one-bit words and fabricated using HMOS high-performance N-channel silicon-gate technology, this new breed of 5-volt only dynamic RAM combines high performance with low cost and improved reliability.

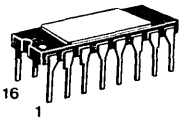
By multiplexing row- and column-address inputs, the MCM6665A requires only eight address lines and permits packaging in standard 16-pin dual-in-line packages. Complete address decoding is done on chip with address latches incorporated. Data out is controlled by $\overline{CAS}$ allowing for greater system flexibility.

All inputs and outputs, including clocks, are fully TTL compatible. The MCM6665A incorporates a one-transistor cell design and dynamic storage techniques.

- Organized as 65,536 Words of 1 Bit
- Single +5 V Operation (±10%)
- Full Power Supply Range Capabilities
- Maximum Access Time
  MCM6665A-12 = 120 ns
  MCM6665A-15 = 150 ns
  MCM6665A-20 = 200 ns
- Low Power Dissipation
  302.5 mW Maximum (Active) (MCM6665A-15)
  22 mW Maximum (Standby)
- Three-State Data Output
- Internal Latches for Address and Data Input
- Early-Write Common I/O Capability
- 16K Compatible 128-Cycle, 2 ms Refresh
- $\overline{RAS}$-only Refresh Mode
- $\overline{CAS}$ Controlled Output
- Upward Pin Compatible from the 16K RAM (MCM4116, MCM4517)
- Fast Page Mode Cycle Time
- Low Soft Error Rate <0.1% per 1000 Hours (See Soft Error Testing)

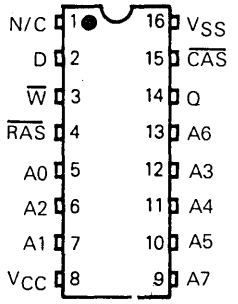


P SUFFIX
PLASTIC PACKAGE
CASE 648



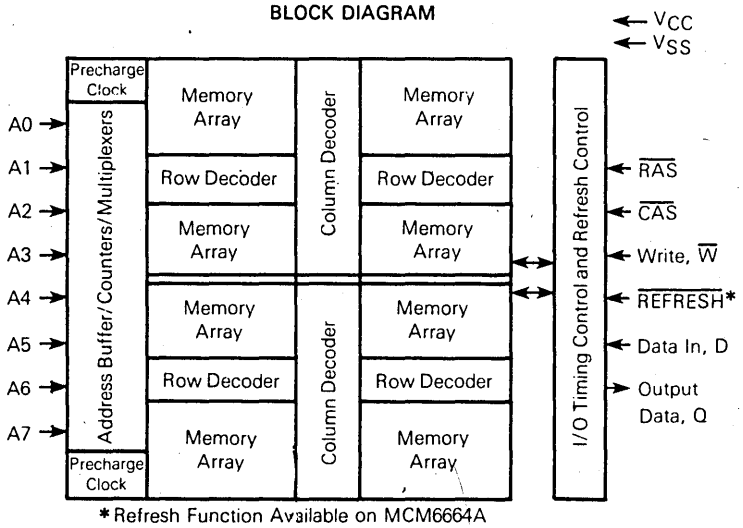
L SUFFIX
CERAMIC PACKAGE
CASE 690

PIN ASSIGNMENT



PIN NAMES	
A0-A7	Address Input
D	Data In
Q	Data Out
W	Read/Write Input
RAS	Row Address Strobe
CAS	Column Address Strobe
VCC	Power (+5 V)
VSS	Ground

BLOCK DIAGRAM



*Refresh Function Available on MCM6664A

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DS-9863
(Replaces ADI-876)

MOTOROLA
SEMICONDUCTORS
3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MCM4517

Advance Information

16,384-BIT DYNAMIC RAM

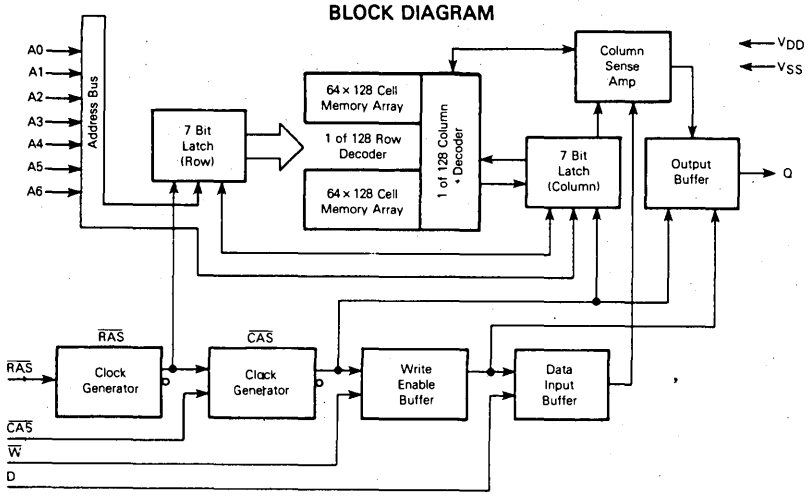
The MCM4517 is a 16,384-bit, high-speed, dynamic Random-Access Memory. Organized as 16,384 one-bit words and fabricated using HMOS high-performance, N-channel, silicon-gate technology. This new breed of 5-volt only dynamic RAM combines high performance with low cost and improved reliability.

By multiplexing row- and column-address inputs, the MCM4517 requires only seven address lines and permits packaging in standard 16-pin dual-in-line packages. Complete address decoding is done on chip with address latches incorporated. Data out is controlled by $\overline{CAS}$ allowing for greater system flexibility.

All inputs and outputs, including clocks, are fully TTL compatible. The MCM4517 incorporates a one-transistor cell design and dynamic storage techniques.

- Organized as 16,384 Words of 1 Bit
- Single +5 Volt Operation
- Fast 100 ns Operation
- Low Power Dissipation:
  - 170 mW Maximum (Active)
  - 14 mW Maximum (Standby)
- Maximum Access Time
  - MCM4517-10 — 100 ns
  - MCM4517-12 — 120 ns
  - MCM4517-15 — 150 ns
  - MCM4517-20 — 200 ns
- Three-State Data Output
- Internal Latches for Address and Data Input
- Early-Write Common I/O Output Capability
- 64K Compatible 128-cycle, 2 ms Refresh
- $\overline{RAS}$-only Refresh Mode
- $\overline{CAS}$ Controlled Output
- Upward Pin Compatibility from the 16K RAM (MCM4116) to the 64K. RAM (MCM6664)
- Allows Undershoot V_{IL} min = −2 V
- Hidden $\overline{RAS}$ Only Refresh Capability

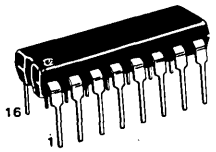
BLOCK DIAGRAM



MOS

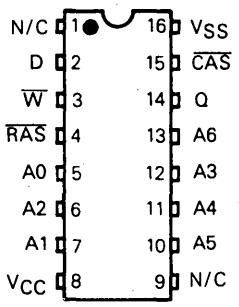
(N-CHANNEL, SILICON-GATE)

16,384-BIT DYNAMIC RAM



P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



PIN NAMES	
A0-A6	Address Input
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ADI-836-R2

MOTOROLA
SEMICONDUCTORS
3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MCM65147

Advance Information

4096-BIT STATIC RANDOM ACCESS MEMORY

The MCM65147 is a 4096-bit static Random Access Memory organized as 4096 words by 1-bit, fabricated using Motorola's high performance CMOS silicon gate technology (HCMOS). It uses a design approach which provides the simple timing features associated with fully static memories and the reduced power associated with CMOS memories. This means low power without the need for clocks, nor reduced data rates due to cycle times that exceed access times.

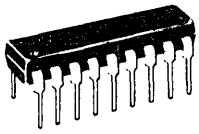
Chip enable ($\overline{E}$) controls the power-down feature. It is not a clock, but rather a chip control that affects power consumption. After $\overline{E}$ goes high, initiating deselect mode, the part automatically reduces its power requirements and remains in this low-power standby mode as long as $\overline{E}$ remains high.

The MCM65147 is in an 18-pin dual in-line package with the industry standard pinout. It is TTL compatible in all respects. The data out has the same polarity as the input data. A data input and a separate three-state output provide flexibility and allow easy OR-ties.

- Single +5 V Supply
- Fully Static Memory — No Clock or Timing Strobe Required
- Maximum Access Time
  MCM65147-55 = 55 ns
  MCM65147-70 = 70 ns
- Automatic Power Down
- Low Power Dissipation
  75 mW Typical (Active)
  125 μW Typical (Standby)
- Low Standby Power Version Available
- Directly TTL Compatible — All Inputs and Output
- Separate Data Input and Three-State Output
- Equal Access and Cycle Time
- High Density 18-Pin Package

HCMOS
(COMPLEMENTARY MOS)

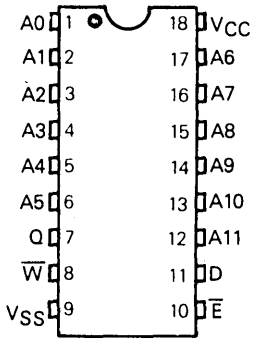
4,096 × 1 BIT STATIC RANDOM ACCESS MEMORY



P SUFFIX
PLASTIC PACKAGE
CASE 707

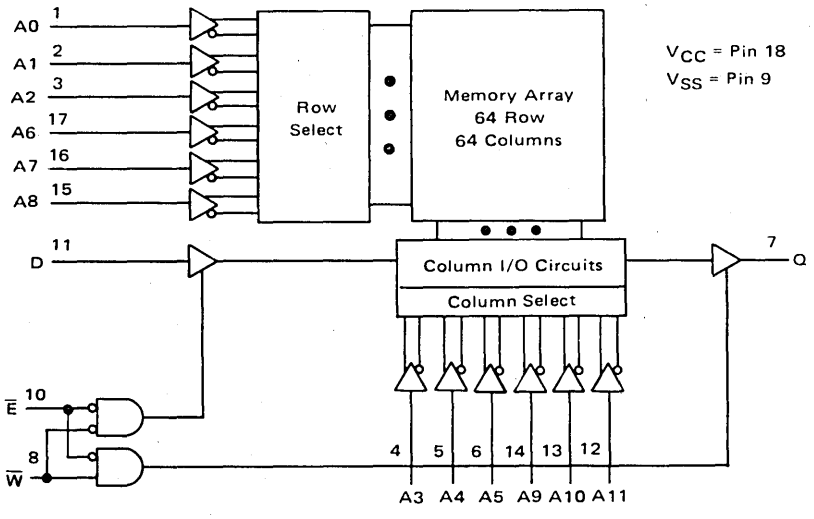
C SUFFIX
FRIT-SEAL CERAMIC PACKAGE
CASE 726

PIN ASSIGNMENTS



PIN NAMES	
A0-A11	Address
$\overline{E}$	Chip Enable
D	Data In
Q	Data Out
$\overline{W}$	Write
V_{CC}	Power (+5 V)
V_{SS}	Ground

BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

ADI-880R1

MOTOROLA
SEMICONDUCTORS
3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MCM2016H

Advance Information

MOS
(N-CHANNEL, SILICON-GATE)

2,048 × 8 BIT
STATIC RANDOM
ACCESS MEMORY

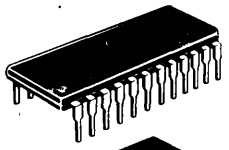
FAST 16K BIT STATIC RAM

The MCM2016H is a 16,384-bit Static Random Access Memory organized as 2048 words by 8 bits, fabricated using Motorola's High-performance silicon-gate MOS (HMOS) technology. It uses an innovative design approach which combines the ease-of-use features of fully static operation (no external clocks or timing strobes required) with the reduced standby power dissipation associated with clocked memories. To the user this means low standby power dissipation without the need for address setup and hold times, nor reduced data rates due to cycle times that are no longer than access times. Perfect for cache and sub-100 ns buffer memory systems, this high speed static RAM is intended for applications that demand superior performance and reliability.

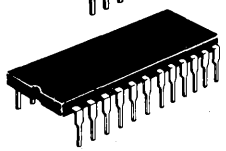
Chip Enable ($\overline{E}$) controls the power-down feature. It is not a clock but rather a chip control that affects power consumption. In less than a cycle time after chip enable ($\overline{E}$) goes high, the part automatically reduces its power requirements and remains in this low-power standby mode as long as the chip enable ($\overline{E}$) remains high. The automatic power-down feature causes no performance degradation.

The MCM2016H is in a 24-pin dual-in-line 600 mil wide package with the industry standard JEDEC approved pinout and is pinout compatible with the industry standard 16K EPROM/ROM. A 24 pin dual-in-line 300 mil wide package will also be available.

- Single +5 Volt Operation (±10%)
- Fully Static: No Clock or Timing Strobe Required
- Fast Access Time: MCM2016H-45 – 45 ns (max)
  MCM2016H-55 – 55 ns (max)
  MCM2016H-70 – 70 ns (max)
- Power Dissipation: 100 mA Maximum (Active)
  70 mA Maximum (Selected, D.C.)
  25 mA Maximum (Standby)
- Three-State Output

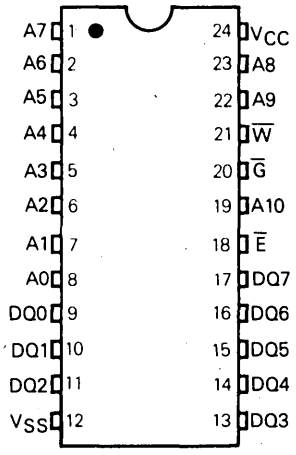


P SUFFIX
PLASTIC PACKAGE
CASE 709

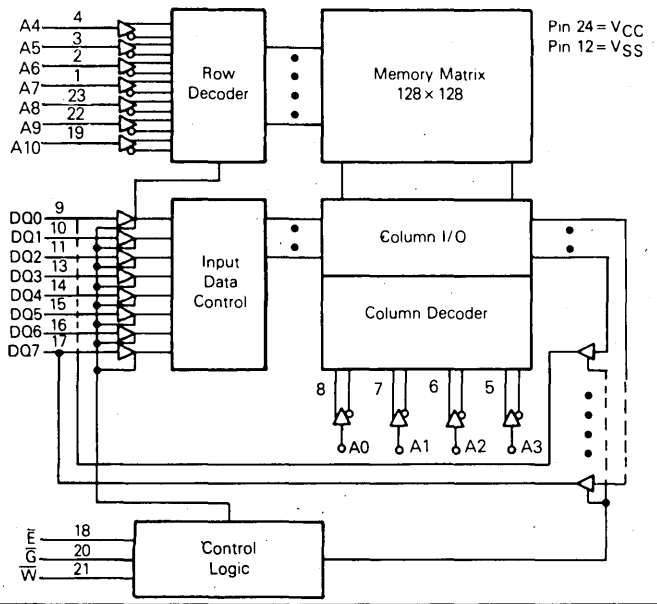


L SUFFIX
CERAMIC PACKAGE
CASE 716

PIN ASSIGNMENTS



BLOCK DIAGRAM



PIN NAMES	
A0-A10	Address Input
DQ0-DQ7	Data Input/Output
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
V_{CC}	Power (+5 V)
V_{SS}	Ground

MEMORY

Motorola Semiconductor

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MOTOROLA
SEMICONDUCTORS
3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MCM2801

Advance Information

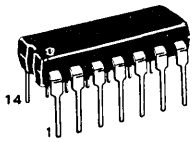
16 × 16-BIT SERIAL ELECTRICALLY ERASABLE PROM

The MCM2801 is a 256-bit serial Electrically Erasable PROM designed for handling small amounts of data in applications requiring both non-volatile memory and in-system information updates.

The MCM2801 offers in-system erase and reprogram capability. It has external control of timing functions and serial format for data and address. The MCM2801 is fabricated in floating gate technology for high reliability and producibility.

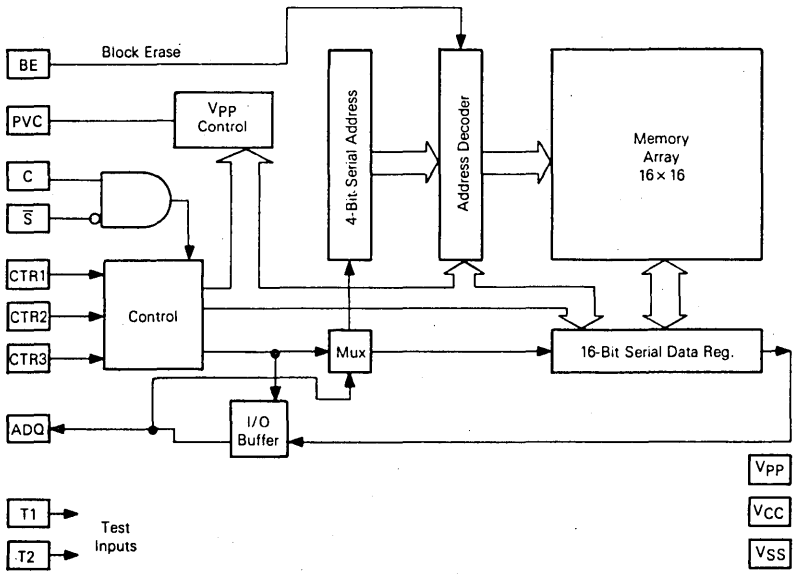
- Single +5 V Power Supply
- Organized as 16 Words of 16 Bits
- MPU Bus Compatible
- Single +25 V Power Supply for Erase and Program
- In-System Program/Erase Capability
- Both Word and Whole Array Erasable

MOS
(N-CHANNEL, SILICON GATE)
16 × 16 BIT ELECTRICALLY ERASABLE PROGRAMMABLE READ ONLY MEMORY

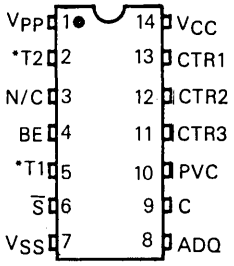


PLASTIC PACKAGE
CASE 646-05

BLOCK DIAGRAM



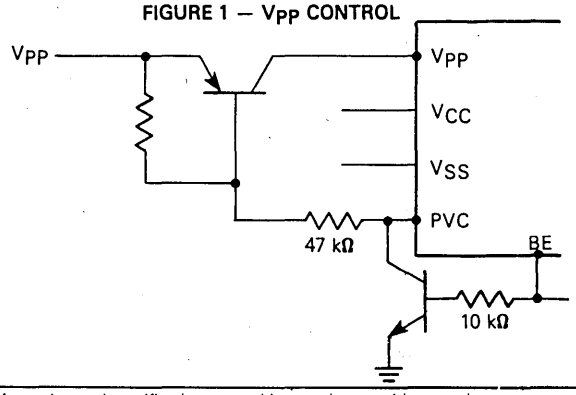
PIN ASSIGNMENT



*For normal operation, these inputs should be hardwired to V_{SS}.

PIN NAMES	
ADQ	Multiplexed Address/ Data-In/Data-Out
C	Clock
PVC	Program Voltage Control
CTR1, 2, 3	Control
BE	Block Erase
$\overline{S}$	Chip Select
T1, T2	Test Pins

FIGURE 1 — V_{PP} CONTROL



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ADI-841 R1

MOTOROLA
SEMICONDUCTORS
3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MCM2832

Product Preview

32K-BIT ELECTRICALLY ERASABLE PROM

The MCM2832 is a 32,768-bit Electrically Erasable Programmable Read Only Memory (E^2PROM) designed for handling data in applications requiring both nonvolatile memory and in-system reprogramming.

The MCM2832 saves time and money because of the in-system erase and reprogram capability. The device operates from a single +5 V power supply in the read mode, while writing and erasing are accomplished by providing an additional +21 V supply. Word erase and write can be controlled entirely by TTL signal levels.

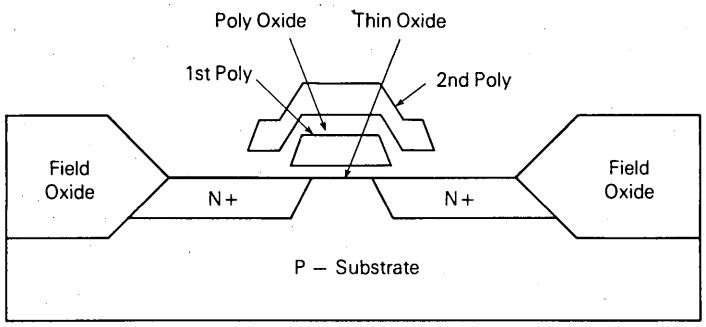
To ease system design, V_{PP} does not need to be pulsed for each program or erase cycle. However, V_{PP} can also be pulsed. The rise and fall times of V_{PP} are noncritical because they are internally controlled. Another ease-of-use feature is the choice of erase modes (bulk, byte, row, or column) to optimize system erase/write time. For microprocessor compatibility, on-chip latches are provided for addresses, data, and controls, allowing the microprocessor to perform other tasks while the MCM2832 is erasing or programming itself.

The MCM2832 is fabricated using Motorola's FETMOS technology, (Floating-gate Electron Tunneling MOS), which has the advantages of good data retention, good endurance and conventional processing. The FETMOS device uses the same active channel area as the tunneling area (instead of a separate thin oxide area) for high density, reliability, and producibility.

The device pinout is part of Motorola's industry standard byte wide Non-Volatile Memory family, providing cost-effective density upgrades.

- Single +5 V Power Supply
- +21 V Power Supply for Erase and Program
- Organized as 4096 Bytes of 8 Bits
- In-System Program/Erase Capability
- Fast Maximum Access Time = 150 ns MCM2832-15
  200 ns MCM2832-20
- Low Power Dissipation
  125 mA Maximum (Active)
  30 mA Maximum (Standby)
- 10 ms for Byte Erase or Program
- Latched Address, Data, and Controls for Program and Erase
- Both Chip Enable and Output Enable for Bus Control
- 28-Pin JEDEC Standard Pinout

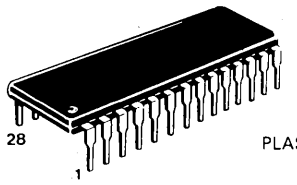
FETMOS
(Floating-Gate Electron Tunneling MOS)



HMOS

(N-CHANNEL, SILICON GATE)

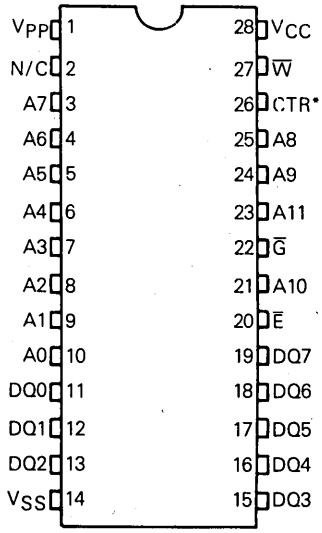
4096 × 8-BIT ELECTRICALLY ERASABLE PROGRAMMABLE READ ONLY MEMORY



P SUFFIX
PLASTIC PACKAGE
CASE 710

L SUFFIX CERAMIC PACKAGE ALSO AVAILABLE — CASE 719

PIN ASSIGNMENT



*For normal operation, Pin 26 should be tied to V_{SS}.

PIN NAMES	
A	Address
DQ	Data Input/Output
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
CTR	Control

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

NP-342R1

MOTOROLA
SEMICONDUCTORS
3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MCM63256

Product Preview

HMOS
(N-CHANNEL, SILICON GATE)

32,768 × 8 BIT
READ ONLY MEMORY

256K BIT READ ONLY MEMORY

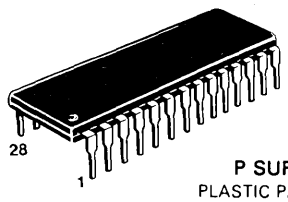
The MCM63256 is a MOS mask programmable byte-organized Read Only Memory (ROM). The MCM63256 is organized as 32,768 bytes of 8 bits and is fabricated using Motorola's high performance N-channel silicon gate technology (HMOS). This device is designed to provide maximum circuit density and reliability with highest possible performance while maintaining low power dissipation and wide operating margins and remaining fully compatible with TTL inputs and outputs.

The active level of the Chip Enable and the Output Enable, along with the memory contents, are defined by the user. The Chip Enable input deselects the output and puts the chip in a power-down mode.

- Single ±10% +5 Volt Power Supply
- Fully Static Periphery — No Clocking Required on Chip Enable
- Automatic Power Down
- Power Dissipation
  100 mA Active (Maximum) (Unloaded)
  15 mA Standby (Maximum)
- Current Surge Suppression When Powering Up Device
- Program Layer Late in Process for Quick Turnaround Time
- 150 ns Maximum Access from Address and Chip Enable
- 28-Pin JEDEC Standard Package and Pinout

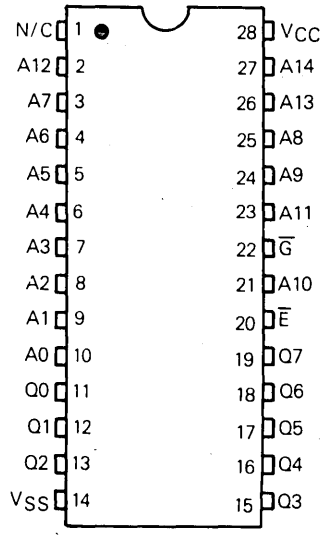
ADDITIONAL FEATURE

- Address (A14) is User Selectable for Either Pin 27 or Pin 1

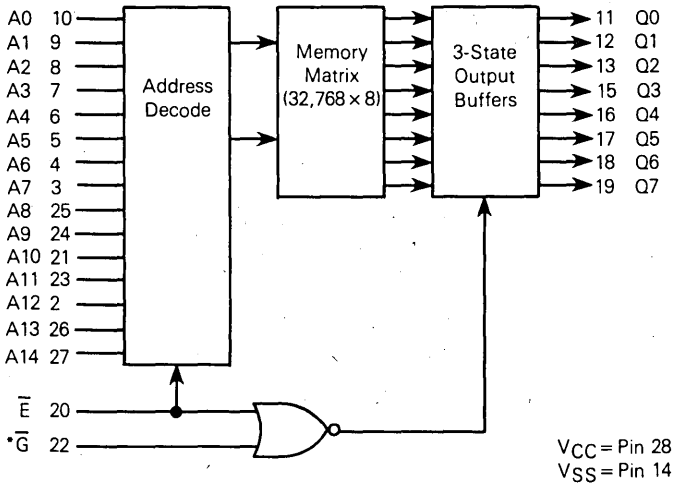


P SUFFIX
PLASTIC PACKAGE
CASE 710

PIN ASSIGNMENT



BLOCK DIAGRAM



*Active level defined by the user.

PIN NAMES	
A0-A14	Address
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
Q0-Q7	Data Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

NP-350

National Semiconductor

PRELIMINARY

DM54/74LS471
(256 X 8) 2048-Bit TTL PROMs

General Description

These Schottky memories are organized in the popular 256 words by 8 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions.

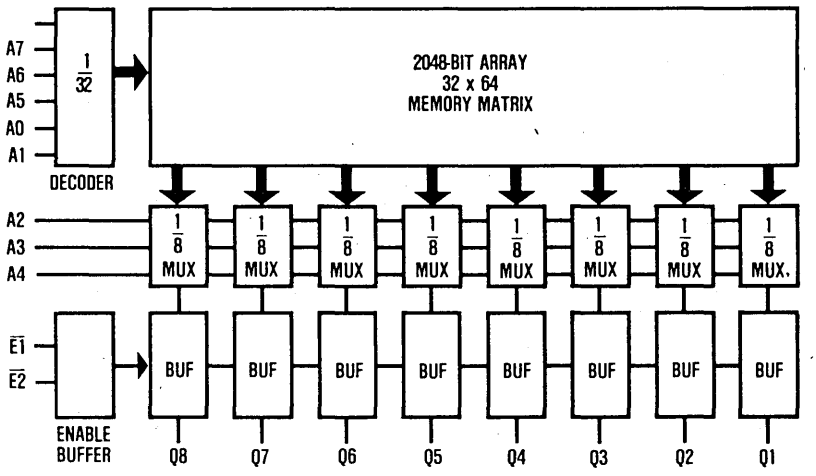
PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

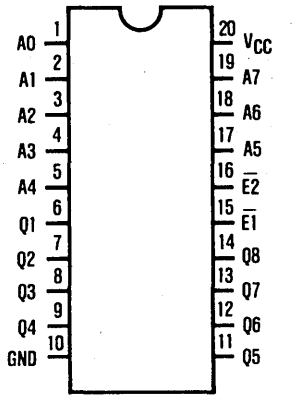
Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—45ns typ
  - Enable access—15ns typ
  - Enable recovery—15ns typ
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74LS471		X		X	N,J
DM54LS471	X			X	J

Block and Connection Diagram





Order Number;
DM74LS471 J,
DM54LS471 J,
See NS Package J20B

Order Number;
DM74LS471 N
See NS Package N20A

National Semiconductor

DM77/87S180, DM77/87S181
DM77/87S280, DM77/87S281
(1024 x 8) 8192-Bit TTL PROMs

General Description

These Schottky memories are organized in the popular 1024 words by 8 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions.

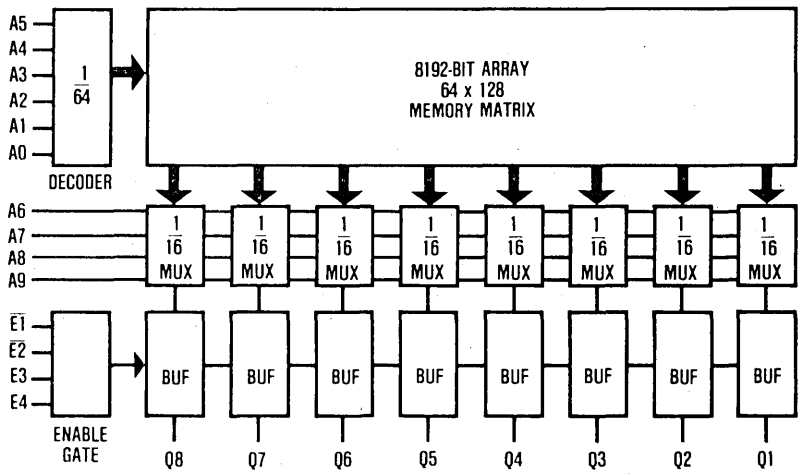
PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

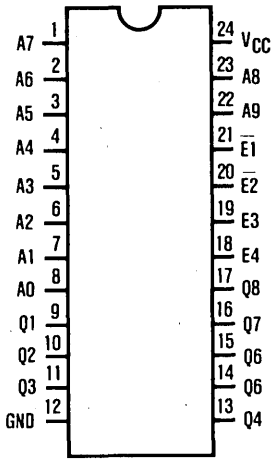
Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—40ns typ
  - Enable access—15ns typ
  - Enable recovery—15ns typ
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming

	Military	Commercial	Open-Collector	TRI-STATE	Package	24-Pin Standard	24-Pin Narrow-Dip
DM87S180		X	X		N,J	X	
DM87S181		X		X	N,J	X	
DM77S180	X		X		J	X	
DM77S181	X			X	J	X	
DM87S280		X	X		N,J		X
DM87S281		X		X	N,J		X
DM77S280	X		X		J		X
DM77S281	X			X	J		X

Block and Connection Diagram





Order Number:
DM87S180 J, DM87S181 J,
DM77S180 J, DM77S181 J
See NS Package J24A

Order Number:
DM87S280 J, DM87S281 J,
DM77S280 J, DM77S281 J
See NS Package J24C

Order Number:
DM87S180 N or DM87S181 N
See NS Package N24A

Order Number:
DM87S280 N, or DM87S281 N
See NS Package N24C

National Semiconductor

PRELIMINARY

DM77/87SR181
(1024 × 8) 8k-Bit Registered TTL PROM

General Description

The DM77/87SR181 is an electrically programmable Schottky TTL read-only memory with D-type, master-slave registers on chip. This devices is organized as 1024-words by 8-bits and is available in the tri-state output version. Designed to optimize system performance, this device also substantially reduces the cost and size of pipelined microprogrammed systems and other designs wherein accessed PROM data is temporarily stored in a register. The DM77/87SR181 also offers maximal flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables. All outputs will go into the "OFF" state if the synchronous chip enable ($\overline{GS}$) is high before the rising edge of the clock, or if the asynchronous chip enable ($\overline{G}$) is held high. The outputs are enabled when $\overline{GS}$ is brought low before the rising edge of the clock and $\overline{G}$ is held low. The $\overline{GS}$ flip-flop is designed to power up to the "OFF" state with the application of V_{CC}.

Data is read from the PROM by first applying an address to inputs A0-A9. During the setup time the output of the array is loaded into the master flip-flop of the data register. During the rising edge (low to high transition) of the clock, the data is then transferred to the slave of the flip-flop and will appear on the output if the output is enabled. Following the rising edge clock transition the addresses and synchronous chip enable can be removed and the output data will remain stable.

The DM77SR181 also features an initialize function $\overline{INIT}$. The initialize function provides the user with an extra word of programmable memory which is accessed with single pin control by applying a low on $\overline{INIT}$. The initialize function is synchronous and is loaded into the output register on the next rising edge of the clock. The unprogrammed state of the $\overline{INIT}$ is all lows.

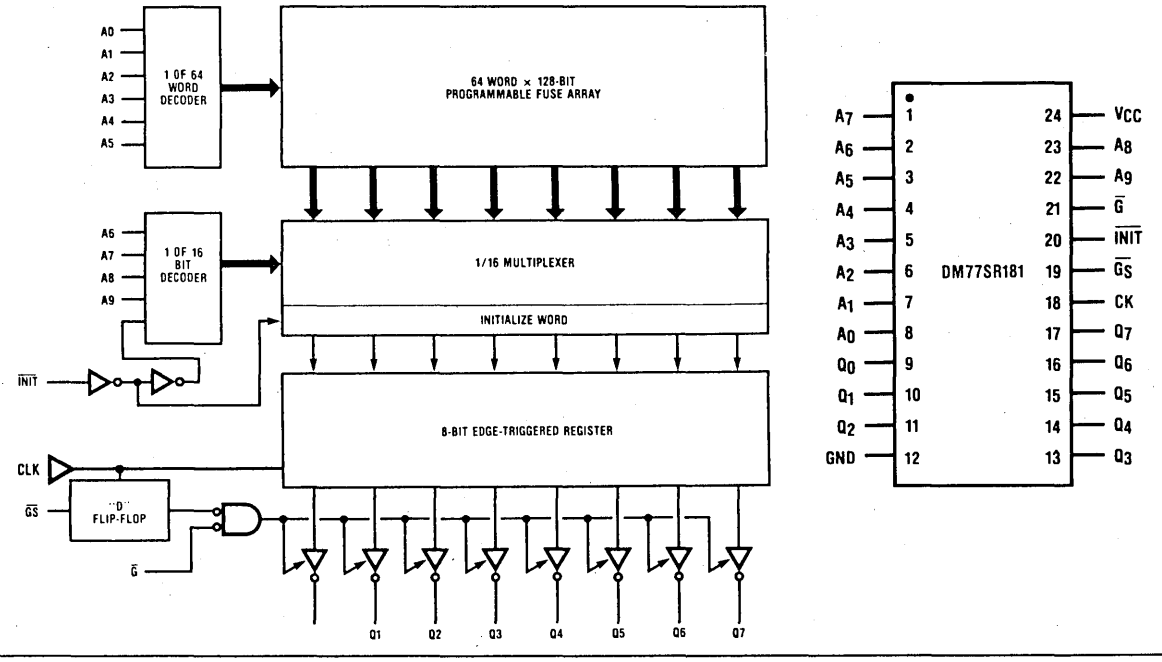
PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

Features

- On-chip, edge-triggered registers
- Synchronous and asynchronous enables for word expansion
- Programmable register INITIALIZE
- 24-pin, 300 mil package
- 40ns address setup and 20ns clock to output for maximum system speed
- Highly reliable, titanium tungsten fuses
- TRI-STATE® outputs
- Low voltage TRI-SAFE™ programming
- All parameters guaranteed over temperature

TRI-STATE is a registered trademark of National Semiconductor Corp.
TRI-SAFE is a trademark of National Semiconductor Corp.

Block and Connection Diagram



National Semiconductor

PRELIMINARY
October 1982

DM77S401/DM87S401, DM77S402/DM87S402 First-In, First-Out (FiFo) 64 x 4, 64 x 5 Serial Memories

General Description

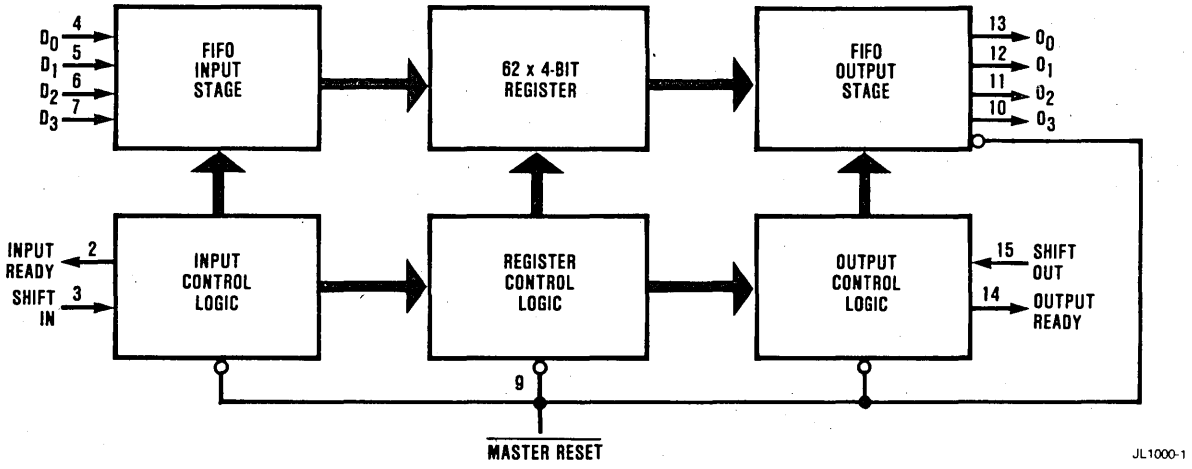
The DM77S401 is an expandable "fall-through" type high-speed First-in, First-out (FiFo) memory organized in 64-word by 4-bit, and 64-word by 5-bit structures respectively. A 20 MHz data rate allows usage in high-speed disc or tape controllers as well as PCM and communications buffer applications.

Features

- 20 MHz shift in, shift out
- TTL inputs and outputs
- Inputs and outputs are symmetrically placed on package
- Easily expandable word and bit dimensions
- Either synchronous or asynchronous operation
- Fairchild F3341 MOS FiFo pin compatible but 20 times faster!
- Twice as fast as MMI's 57/67401
- Choice of 4-bit or 5-bit data width

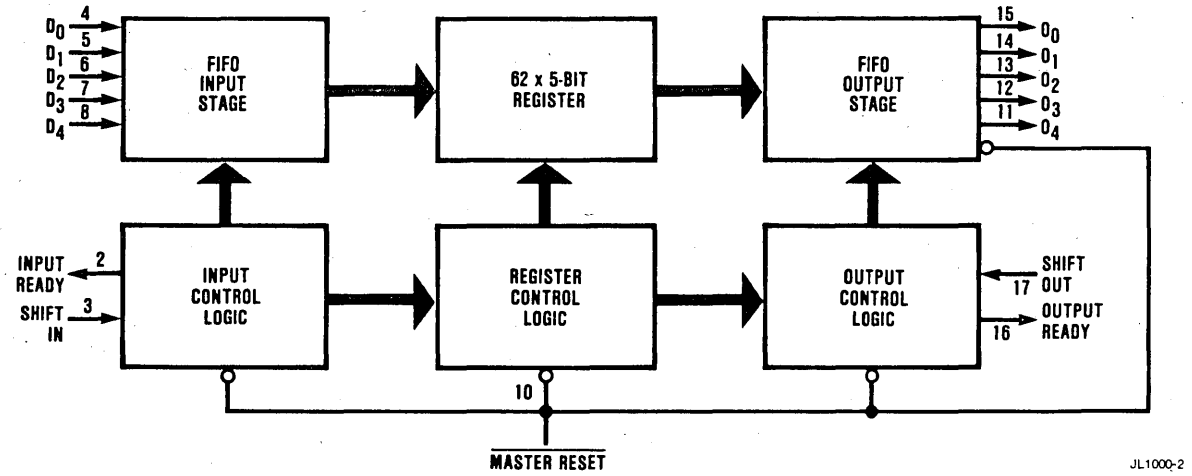
Block Diagrams

DM77/DM87S401
64 x 4



JL1000-1

DM77/DM87S402
64 x 5



JL1000-2

In-H/B25M102/Printed In U.S.A.

National Semiconductor

Bipolar RAMs
PREVIEW

DM10422 1024-Bit (256 × 4) ECL RAM

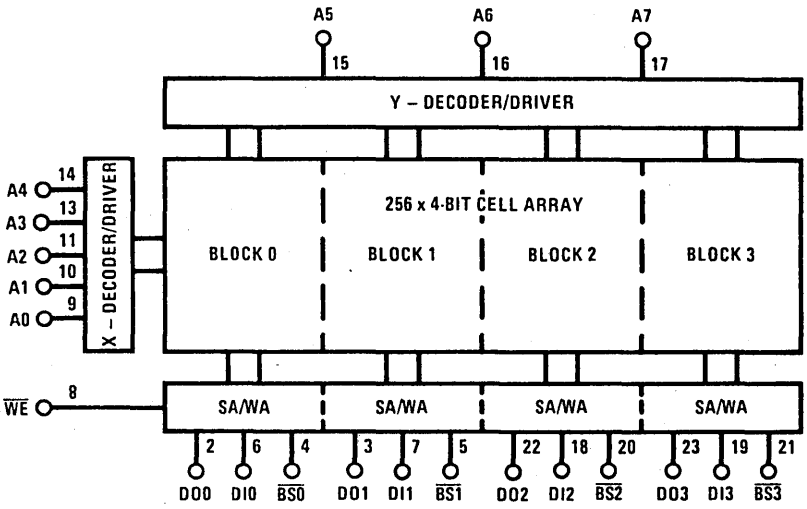
General Description

The DM10422 is normally a 256-word by 4-bit random access memory. However the memory has four Block Select (BS0-BS3) inputs which allow "WIRE OR" of any of the four blocks for a maximum 1024-word by 1-bit memory. The high speed access time allows its use in scratch pad, buffer, and control storage applications. The device is voltage compensated and is compatible with all 10K logic. Separate Data In and Data Out pins allow the set up of data for a write cycle while performing a read.

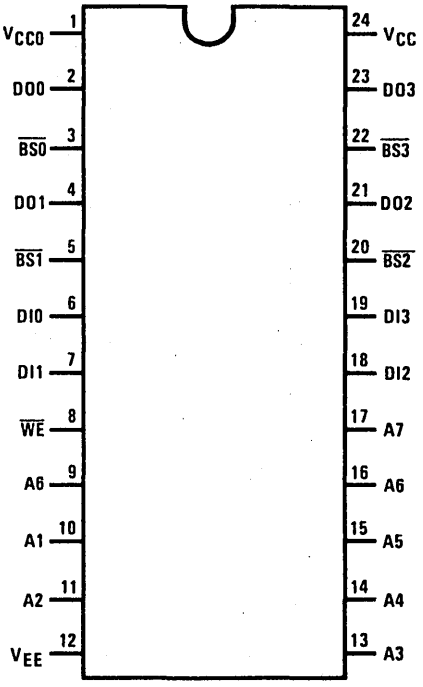
Features

- 4 separate Block Select inputs for from 256 × 4 to 1024 × 1 configuration
- Typical address access time—12 ns
- Block Select access time—4 ns
- 10k logic compatible

Block and Connection Diagrams

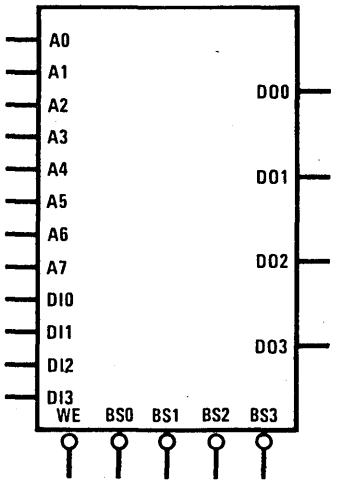


Dual-In-Line Package



TOP VIEW

Logic Symbol



Pin Names

$\overline{BS0}$-$\overline{BS3}$	Block Selects
A0-A7	Address Inputs
$\overline{WE}$	Write Enable
DI0-DI3	Data Inputs
DO0-DO3	Data Outputs

Truth Table (Positive Logic)

Input			Output	Mode
$\overline{BS}$	$\overline{WE}$	DI		
H	X	X	L	Disable
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	DO	Read

National Semiconductor

Bipolar RAMs
PREVIEW

DM10470 4096-Bit (4096 x 1) ECL RAM

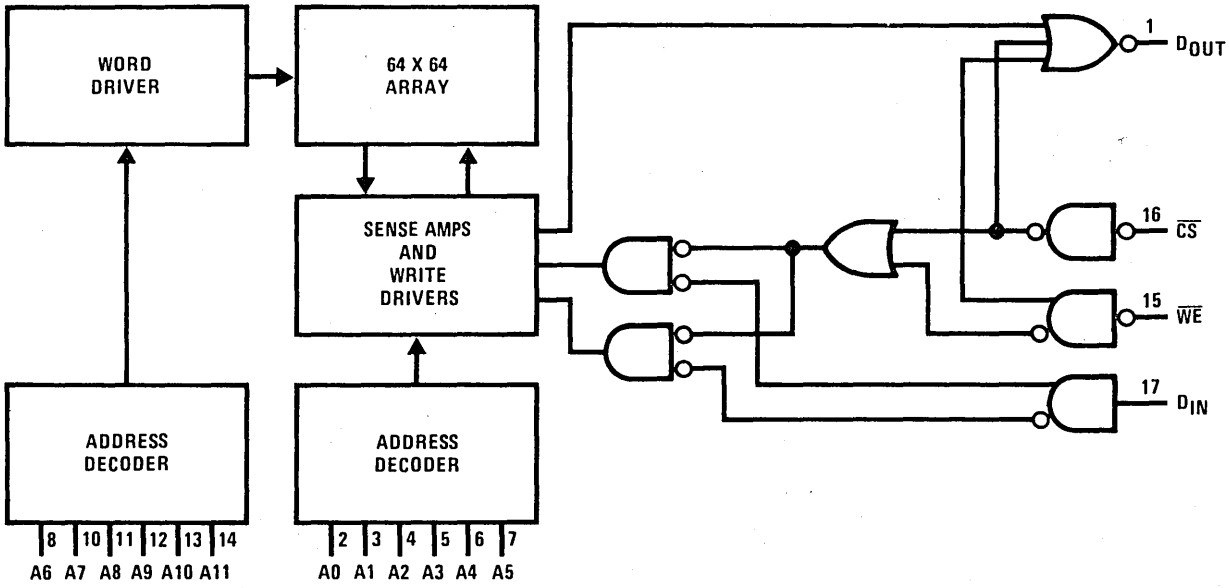
General Description

The DM100470 is a 4096-bit random access memory organized 4096-words by 1-bit. It is designed for high speed scratch pad and buffer storage applications. It is voltage and temperature compensated and compatible with all 100k logic. It has separate Data In and Data Out pins. The active low Chip Select $\overline{CS}$ and open emitter outputs allow easy expansion.

Features

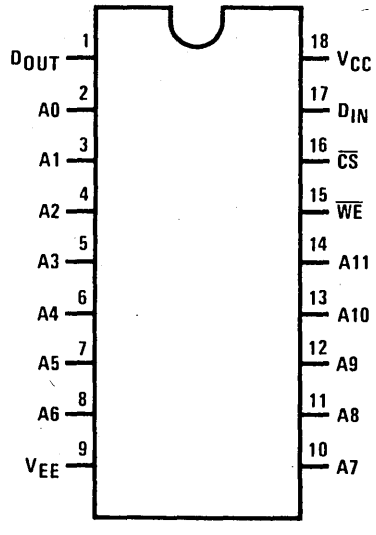
- Typical address access time—18 ns
- Typical Chip Select access time—10 ns
- 100K logic compatible
- Open emitter outputs
- Power dissipation—0.25 mW/bit

Logic Diagram



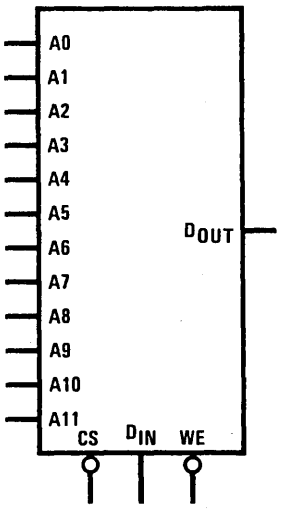
Connection Diagram

Dual-In-Line Package



TOP VIEW

Logic Symbol



Truth Table

Inputs			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}	Open Emitter	
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{OUT}	Read

Pin Names

$\overline{CS}$	Chip Select Inputs
A0-A11	Address Inputs
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output

National Semiconductor

IDM2901A-2 4-Bit Bipolar Microprocessor

General Description

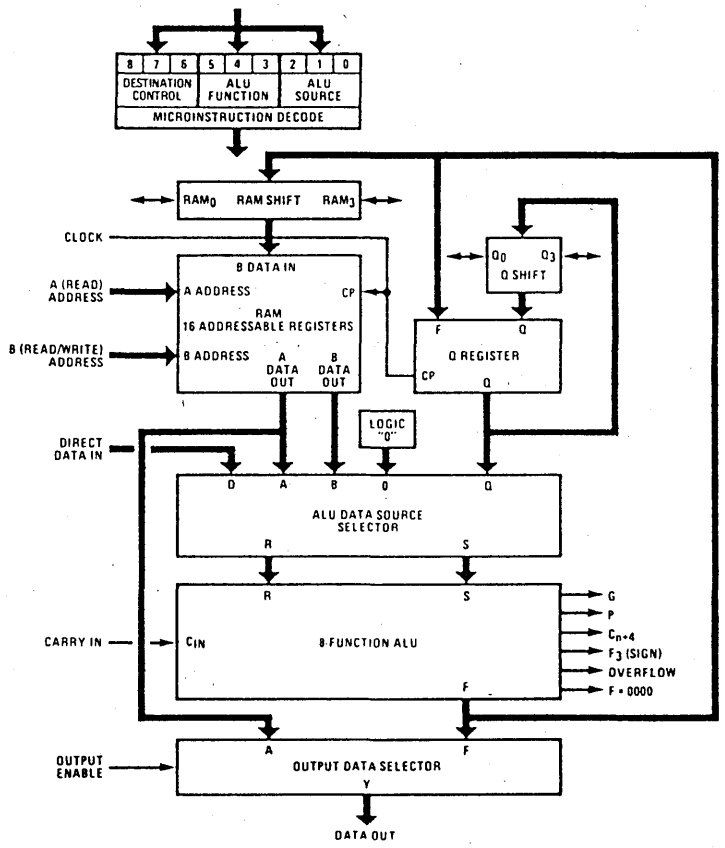
The IDM2901A-2 4-bit bipolar microprocessor slice is a cascadable device designed for use in Central Processing Units, programmable microprocessors, peripheral controllers, and other "high-speed" applications where economy, hardware/software flexibility, and easy expansion are system prerequisites. The building-block architecture and microinstruction format of the IDM2901A-2 permits efficient emulation of most digital-based systems.

As shown in the simplified block diagram, the IDM2901A-2 device consists of a 16-word by 4-bit 2-port RAM, a high-speed ALU, and the required shifting, decoding, and multiplexing circuits. The 9-bit microinstruction word is organized into three groups of three bits each — the first group (bits 0 - 2) selects ALU source operands, the second group (bits 3 - 5) selects the ALU function, and the last group (bits 6 - 8) selects the destination register within the ALU. The slice microprocessor is cascadable with full look-ahead or ripple carry; all outputs are TRI-STATE® and four status-flag outputs are available. To minimize power consumption and to maximize speed and reliability, the 40-pin LSI chip is fabricated using a National state-of-the-art, Low-Power Schottky technology called "SCL".

Features and Benefits

- **Multiple-address architecture** — improves system speed by providing simultaneous yet independent access to two working registers.
- **Multifunction ALU** — performs addition, two subtraction operations, and five logic functions on two source operands.
- **Flexible data-source selection** — for every ALU function, data is selected from five source ports for a total of 203 source operand pairs.
- **Left/right shift independent of ALU** — an arithmetic operation and a left or right shift can be obtained on the same machine cycle.
- **Four status flags** — carry, overflow, zero, and functional sign are available as outputs.
- **Expandable** — Connect any number of IDM2901A-2s together for longer word lengths.
- **Microprogrammable** — three groups of 3 bits each for source operand, ALU function, and destination control.

Block Diagram



National Semiconductor

IDM2910A Microprogram Controller

General Description

The IDM2910A Microprogram Controller is a 12-bit wide address controller packaged in a standard 40-pin dual-in-line package. The IDM2910A features TRI-STATE® outputs and is fabricated using SCL (Schottky ECL) technology. The IDM2910A is a microprogram memory address controller that controls the execution sequence of microinstructions. In addition to being able to sequentially access memory, the IDM2910A is also able to conditionally branch to any microinstruction within the 4096 microinstruction range. A five-level last-in, first-out (LIFO) stack provides microsubroutine return linkage. An internal loop counter is included to provide the repeating instructions or perform up to 4096 loop iterations.

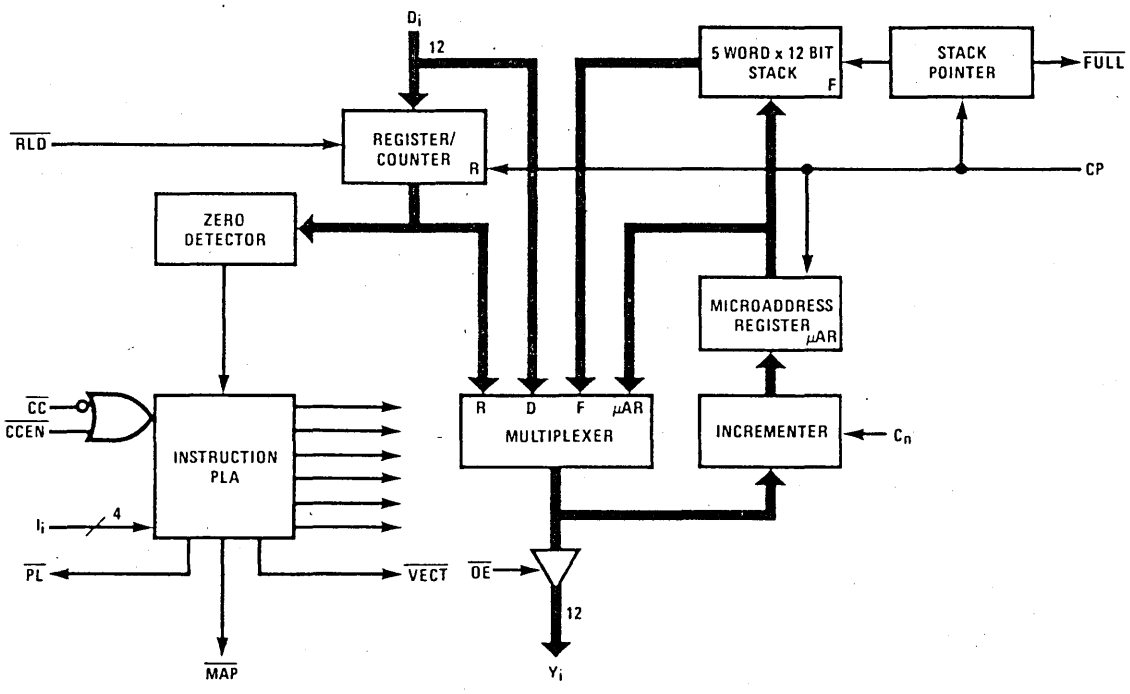
As each microinstruction is executed, the IDM2910A selects a 12-bit address from one of four sources:

1. The Microprogram Address Register which usually contains the increment address of the previous microinstruction.
2. The external Direct Input lines.
3. The Register/Counter which contains an address or data loaded during a previous microinstruction.
4. The LIFO Stack.

Features and Benefits

- Twelve-bit wide address — controls up to 4096 words of microcode with one device
- Internal register/counter — a 12-bit down-counter that may be used to count loop iterations
- Four address sources — the next microprogram address selected from the microprogram address/register data input lines, LIFO stack, or register counter
- Sixteen powerful microinstructions — executes 16 sequence control instructions
- Output enables for three branch address sources — replaces either external decoder or additional bit of microcode
- Positive-edge triggering for all internal registers
- Fast condition-code control — typically a 19ns delay from a condition-code input to an address output
- SCL technology — provides ECL speeds while maintaining low-power Schottky power consumption
- 100% reliability testing in compliance with MIL-STD-883.

IDM2910A Block Diagram



National Semiconductor

August 1982

NMC2114A 1024 x 4 Static RAM

Maximum Access/Current	NMC2114A-1L	NMC2114A-2L	NMC2114A-3L	NMC2114A-4L	NMC2114A-4	NMC2114A-5
Access (t_{AA}—ns)	100	120	150	200	200	250
Active Current (ICC—mA)	40	40	40	40	70	70

General Description

The NMC2114A family of 1024-word by 4-bit static random access memories is fabricated using the XMOS II™ N-channel silicon-gate technology, incorporating poly-load resistors and two poly-silicon layers. All internal circuits are fully static and therefore require no clocks or refreshing for operation. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided. The separate chip select input ($\overline{CS}$) allows easy memory expansion by OR-tying individual devices to a data bus.

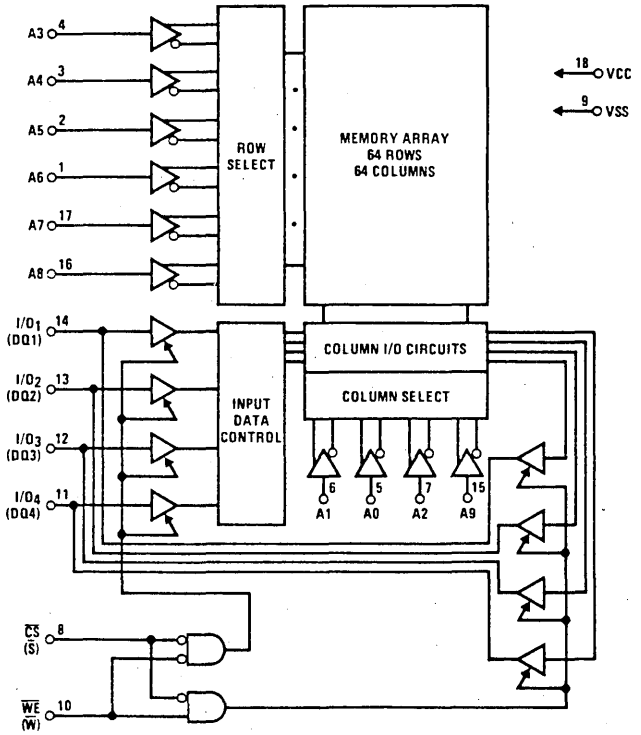
The NMC2114A is designed for memory applications where the high performance and high reliability of XMOS II, low cost and simple interfacing are important design objectives.

Features

- High performance replacement for industry standard MM2114
- All inputs and outputs directly TTL compatible
- Static operation—no clocks or refreshing required
- Low power—220 mW maximum
- High speed—down to 100 ns access time
- TRI-STATE® output for bus interface
- Common data in and data out pins
- Single 5V ± 10% supply
- Standard 18-pin dual-in-line package

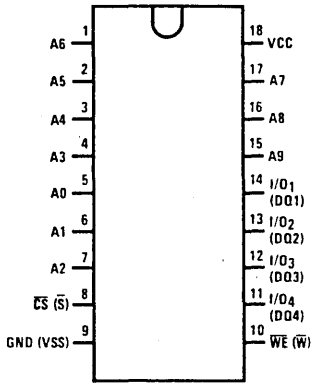
XMOS II™ is a trademark of National Semiconductor Corp.
TRI-STATE® is a registered trademark of National Semiconductor Corp.

Block Diagram*



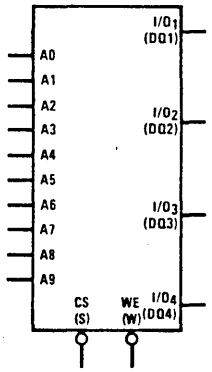
Connection Diagram*

Dual-In-Line Package



TOP VIEW

Logic Symbol*



Truth Table*

$\overline{CS}$ ($\overline{S}$)	$\overline{WE}$ ($\overline{W}$)	I/O (DQ)	Mode
H	X	Hi-Z	Not selected
L	L	H	Write 1
L	L	L	Write 0
L	H	DOUT	Read

X = don't care

*Symbols in parentheses are proposed industry standard

Pin Names*

A0-A9	Address Inputs
$\overline{WE}$ ($\overline{W}$)	Write Enable
$\overline{CS}$ ($\overline{S}$)	Chip Select
I/O_1-I/O_4 (DQ1-DQ4)	Data Input/Output
VCC	Power (5V)
GND (VSS)	Ground

IM-B25M82/Printed in U.S.A.

National Semiconductor

June 1982

NMC2116 2048 × 8 Static RAM

Max Access/Current	NMC2116-15L	NMC2116-20L	NMC2116-25L	NMC2116-15	NMC2116-20	NMC2116-25
Access (TAVQV — ns)	150	200	250	150	200	250
Active Current (ICC — mA)	70	70	70	100	100	100
Standby Current (ISB — mA)	10	10	10	15	15	15

General Description

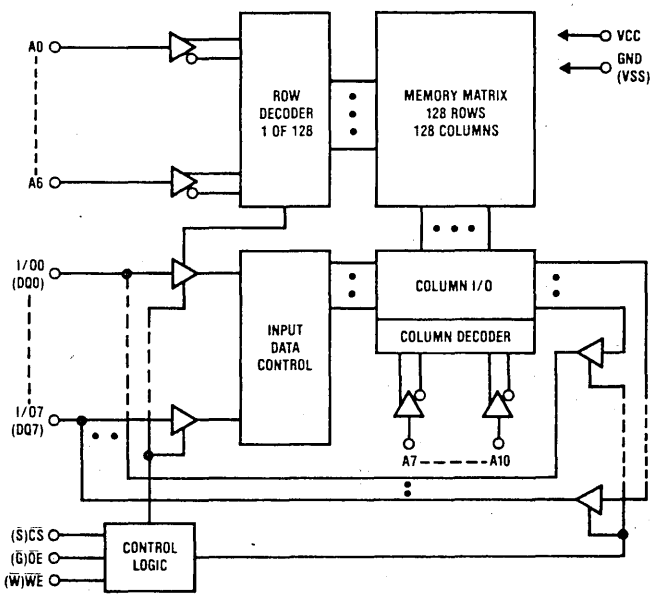
This 2048 × 8 static random access memory is fabricated using N-channel silicon-gate technology incorporating poly-load resistors and two poly-silicon layers. All internal circuits are fully static and therefore require no clocks or refreshing for operation. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

The separate chip select input allows easy memory expansion by OR-tying individual devices to a data bus and automatically powers down the NMC2116.

Features

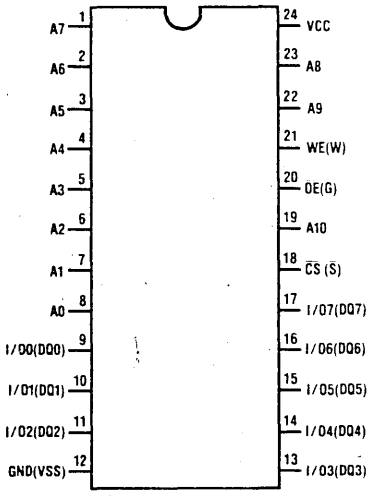
- All inputs and outputs directly TTL compatible
- Static operation—no clocks or refreshing required
- Low power—385 mW max
- 150 ns, 200 ns and 250 ns max access time
- TRI-STATE® output for bus interface
- 24-pin EPROM/ROM compatibility
- Single 5V supply
- Automatic power down
- Common data I/O pins
- Separate $\overline{OE}$ pin

Block Diagram*



Connection Diagram*

Dual-In-Line Package

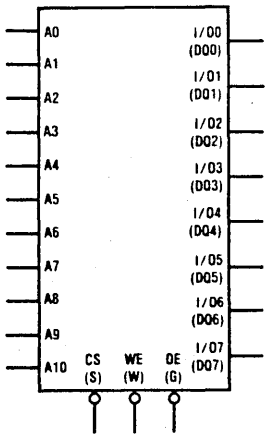


TOP VIEW

Pin Names*

$\overline{CS}$ ($\overline{S}$)	Chip Select
$\overline{OE}$ ($\overline{G}$)	Output Enable
$\overline{WE}$ ($\overline{W}$)	Write Enable
I/O0-I/O7 (DQ0-DQ7)	Data In/Out
A0-A10	Address Inputs
VCC	Power 5V
GND (VSS)	Ground

Logic Symbol*



Truth Table*

$\overline{CS}$ ($\overline{S}$)	$\overline{WE}$ ($\overline{W}$)	$\overline{OE}$ ($\overline{G}$)	I/O	Mode
H	X	X	Hi-Z	Standby
L	L	X	1	Write 1
L	L	X	0	Write 0
L	H	L	DOUT	Read
L	H	H	Hi-Z	Read

*The symbols in parentheses are proposed industry standard.

TRI-STATE® is a registered trademark of National Semiconductor Corp.

IM-B25M62/Printed in U.S.A.

National Semiconductor

MM2716 16,384-Bit (2048 x 8) UV Erasable PROM

General Description

The MM2716 is a high speed 16k UV erasable and electrically reprogrammable EPROM ideally suited for applications where fast turn-around and pattern experimentation are important requirements.

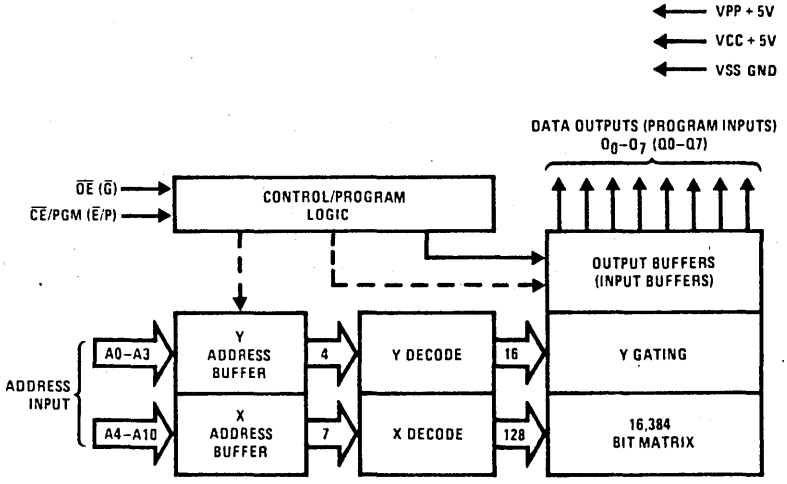
The MM2716 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

This EPROM is fabricated with the reliable, high volume, time proven, N-channel silicon gate technology.

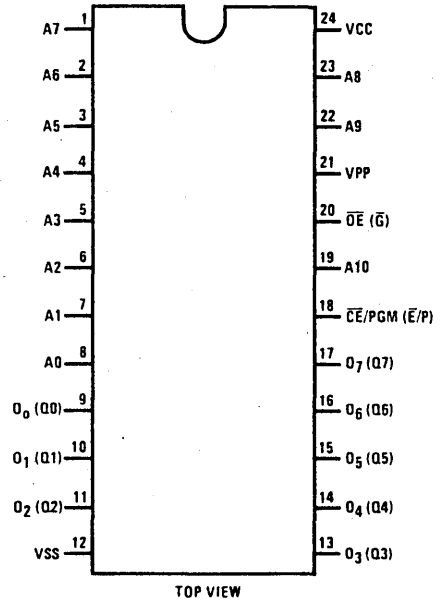
Features

- 2048 x 8 organization
- 525 mW max active power, 132 mW max standby power
- Low power during programming
- Access time—MM2716, 450 ns; MM2716-1, 350 ns; MM2716-2, 390 ns
- Single 5V power supply
- Static—no clocks required
- Inputs and outputs TTL compatible during both read and program modes
- TRI-STATE® output

Block and Connection Diagrams *



Dual-In-Line Package



Order Number MM2716Q, MM2716Q-1 or MM2716Q-2
See NS Package J24CQ

Pin Connection During Read or Program

MODE	PIN NAME/NUMBER				
	CE/PGM (E/P) 18	OE (G) 20	VPP 21	VCC 24	OUTPUTS 9–11, 13–17
Read	VIL	VIL	5	5	DOUT
Program	Pulsed VIL to VIH	VIH	25	5	DIN

*Symbols in parentheses are proposed industry standard

Pin Names

A0–A10	Address Inputs
O0–O7 (Q0–Q7)	Data Outputs
CE/PGM (E/P)	Chip Enable/Program
OE (G)	Output Enable
VPP	Read 5V, Program 25V
VCC	Power (5V)
VSS	Ground

National Semiconductor

PRELIMINARY
April 1982

NMC2816 16k (2k x 8) Electrically Erasable PROM

Max Access/Current	NMC2816-25	NMC2816-35	NMC2816-45
Max Access Time (ns)	250	350	450
Max Active Current (mA)	110	110	110
Max Standby Current (mA)	50	50	50

General Description

The NMC2816 is a 16,384-bit electrically erasable and programmable read-only memory (E^2PROM) fabricated using National's high speed, low power, N-channel double silicon gate technology. The electrical erase/write capability of the NMC2816 makes it ideal for a wide variety of applications requiring in-system, non-volatile erase and write.

The device operates from a 5V power supply in the read mode and, with its very fast read access speed, is compatible with high performance microprocessors.

The NMC2816 is deselected when pin 18 is high and is automatically placed in the standby mode. This mode provides a 52% reduction in power with no increase in access time. The NMC2816 also has an output enable control to eliminate bus contention in a system environment.

The NMC2816 can be easily erased and reprogrammed in a byte-by-byte mode and the entire memory array erased in a chip erase mode. Byte erase mode is identical to byte write mode, with all data inputs at logic ones (TTL high).

Features

- 2048 x 8 organization
- Fully static
- Reliable floating gate technology
- Very fast access time
  - 250 ns max (NMC2816-25)
  - 350 ns max (NMC2816-35)
  - 450 ns max (NMC2816-45)
- Single byte erase/write capability
- 10 ms byte erase/write time
- Chip erase time of 10 ms
- Conforms to JEDEC byte-wide family standard
- Microprocessor compatible architecture
- Low power dissipation
  - 610 mW max (active power ICC + IPP)
  - 295 mW max (standby power ICC + IPP)

Block and Connection Diagrams

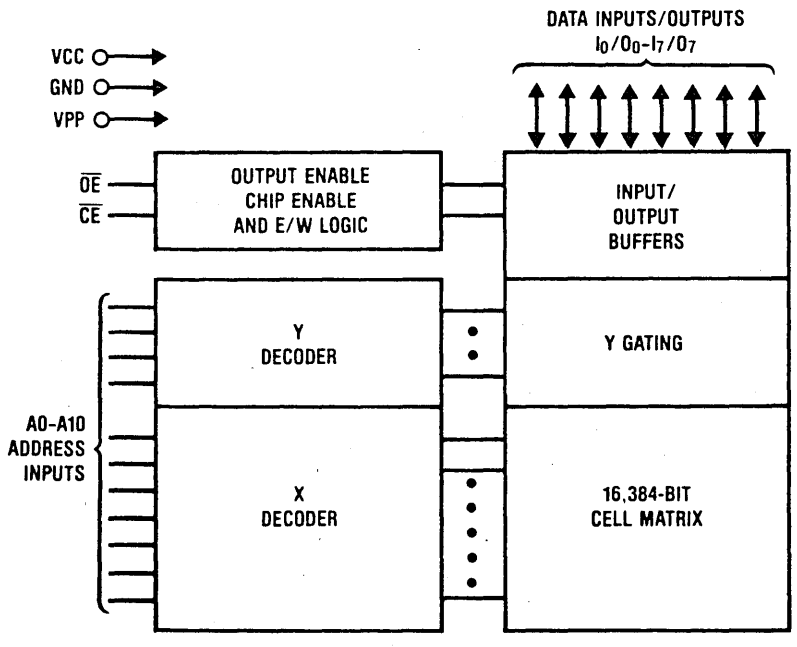
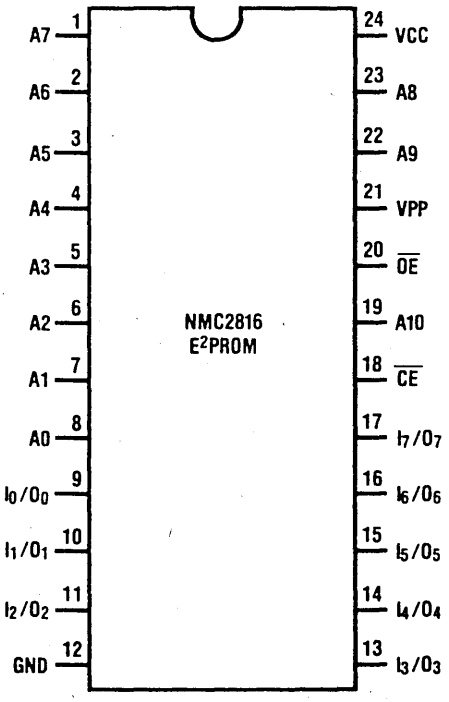


FIGURE 1

Dual-In-Line Package



TOP VIEW

FIGURE 2

Pin Names

A0-A10	Addresses	O_0-O_7	Data Outputs
$\overline{CE}$	Chip Enable	I_0-I_7	Data Inputs
$\overline{OE}$	Output Enable	VPP	Program Voltage

IM-B25M42/Printed in U.S.A.

National Semiconductor

PRELIMINARY
April 1982

NMC2816E 16k (2k x 8) Electrically Erasable PROM

Max Access/Current	NMC2816E-25	NMC2816E-35	NMC2816E-45
Max Access Time (ns)	250	350	450
Max Active Current (mA)	125	125	125
Max Standby Current (mA)	55	55	55

General Description

The NMC2816E is a 16,384-bit electrically erasable and programmable read-only memory (E^2PROM) fabricated using National's high speed, low power, N-channel double silicon gate technology. The electrical erase/write capability of the NMC2816E makes it ideal for a wide variety of applications requiring in-system, non-volatile erase and write.

The device operates from a 5V power supply in the read mode and, with its very fast read access speed, is compatible with high performance microprocessors.

The NMC2816E is deselected when pin 18 is high and is automatically placed in the standby mode. This mode provides a 54% reduction in power with no increase in access time. The NMC2816E also has an output enable control to eliminate bus contention in a system environment.

The NMC2816E can be easily erased and reprogrammed in a byte-by-byte mode and the entire memory array erased in a chip erase mode. Byte erase mode is identical to byte write mode, with all data inputs at logic ones (TTL high).

Features

- 2048 x 8 organization
- Fully static
- Reliable floating gate technology
- Very fast access time
  - 250 ns max (NMC2816E-25)
  - 350 ns max (NMC2816E-35)
  - 450 ns max (NMC2816E-45)
- Single byte erase/write capability
- 10 ms byte erase/write time
- Chip erase time of 10 ms
- Conforms to JEDEC byte-wide family standard
- Microprocessor compatible architecture
- Low power dissipation
  - 720 mW max (active power ICC + IPP)
  - 335 mW max (standby power ICC + IPP)

Block and Connection Diagrams

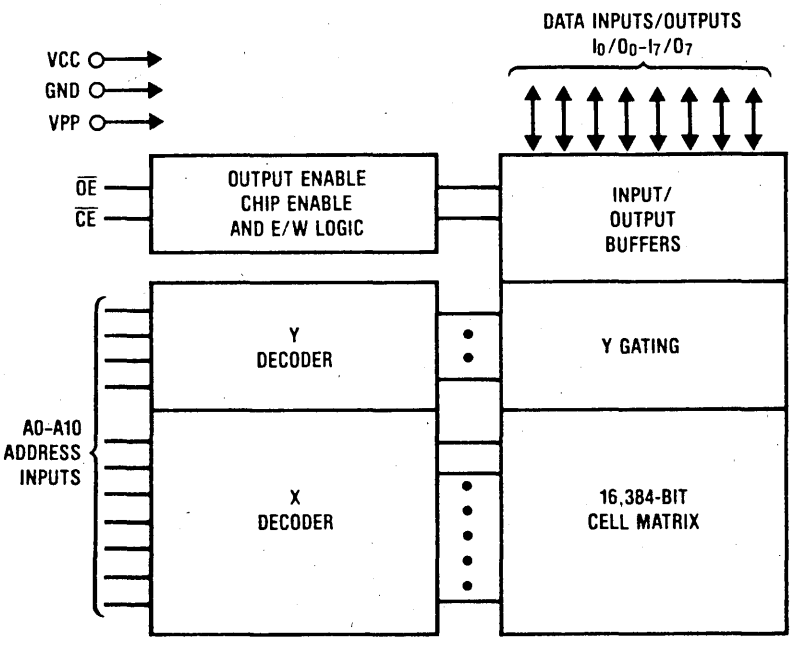
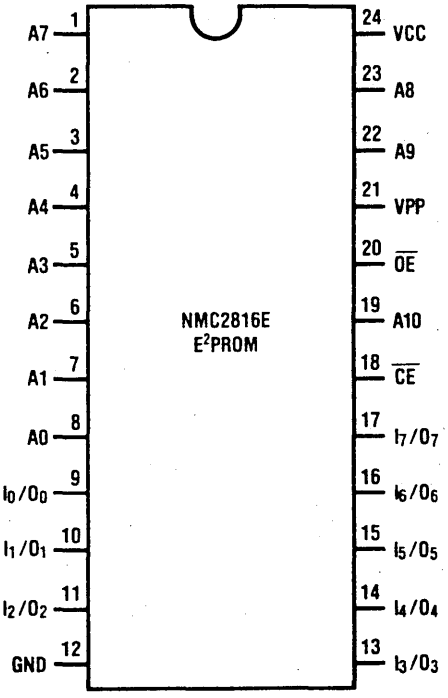


FIGURE 1

Dual-In-Line Package



TOP VIEW

FIGURE 2

Pin Names

A0-A10	Addresses	O_0-O_7	Data Outputs
$\overline{CE}$	Chip Enable	I_0-I_7	Data Inputs
$\overline{OE}$	Output Enable	VPP	Program Voltage

IM-B25M42/Printed in U.S.A

National Semiconductor

PRELIMINARY
April 1982

NMC2816M 16k (2k x 8) Electrically Erasable PROM

Max Access/Current	NMC2816M-25	NMC2816M-35	NMC2816M-45
Max Access Time (ns)	250	350	450
Max Active Current (mA)	140	140	140
Max Standby Current (mA)	60	60	60

General Description

The NMC2816M is a 16,384-bit electrically erasable and programmable read-only memory (E^2PROM) fabricated using National's high speed, low power, N-channel double silicon gate technology. The electrical erase/write capability of the NMC2816M makes it ideal for a wide variety of applications requiring in-system, non-volatile erase and write.

The device operates from a 5V power supply in the read mode and, with its very fast read access speed, is compatible with high performance microprocessors.

The NMC2816M is deselected when pin 18 is high and is automatically placed in the standby mode. This mode provides a 55% reduction in power with no increase in access time. The NMC2816M also has an output enable control to eliminate bus contention in a system environment.

The NMC2816M can be easily erased and reprogrammed in a byte-by-byte mode and the entire memory array erased in a chip erase mode. Byte erase mode is identical to byte write mode, with all data inputs at logic ones (TTL high).

Features

- 2048 x 8 organization
- Fully static
- Reliable floating gate technology
- Very fast access time
  - 250 ns max (NMC2816M-25)
  - 350 ns max (NMC2816M-35)
  - 450 ns max (NMC2816M-45)
- Single byte erase/write capability
- 10 ms byte erase/write time
- Chip erase time of 10 ms
- Conforms to JEDEC byte-wide family standard
- Microprocessor compatible architecture
- Low power dissipation
  - 800 mW max (active power ICC + IPP)
  - 360 mW max (standby power ICC + IPP)

Block and Connection Diagrams

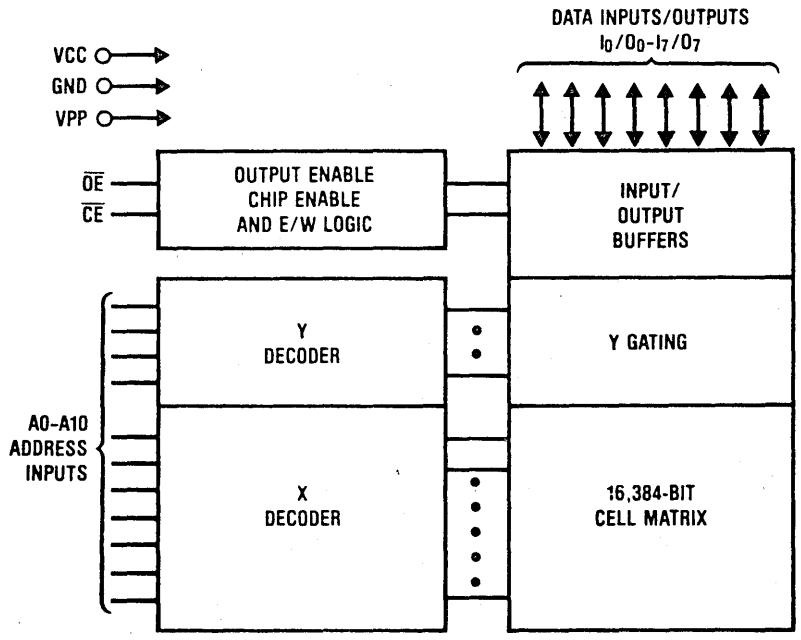
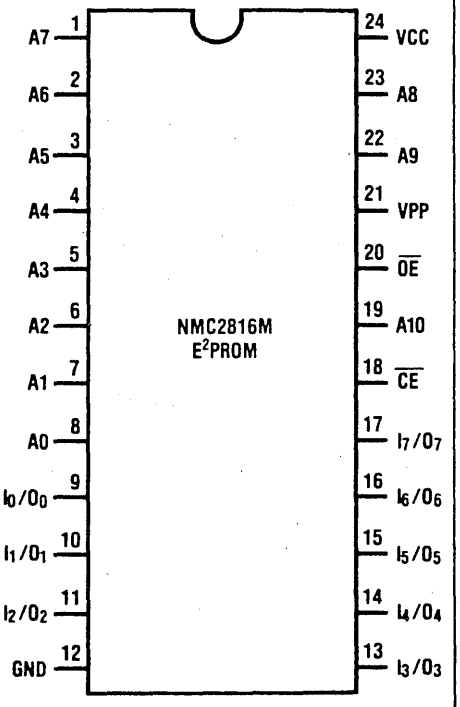


FIGURE 1

Dual-In-Line Package



TOP VIEW

FIGURE 2

Pin Names

A0-A10	Addresses	O_0-O_7	Data Outputs
$\overline{CE}$	Chip Enable	I_0-I_7	Data Inputs
$\overline{OE}$	Output Enable	VPP	Program Voltage

IM-B25M42/Printed in U.S.A

National Semiconductor

PRELIMINARY
May 1982

NMC27C16 16,384-Bit (2048 × 8) UV Erasable CMOS PROM

Parameter/Part Number	NMC27C16Q-45	NMC27C16Q-55	NMC27C16Q-65
Access Time (ns)	450	550	650
Active Current (mA)	5	5	5
Standby Current (mA)	0.1	0.1	0.1

General Description

The NMC27C16 is a high speed 16k UV erasable and electrically reprogrammable CMOS EPROM ideally suited for applications where fast turn-around, pattern experimentation and low power consumption are important requirements.

The NMC27C16 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

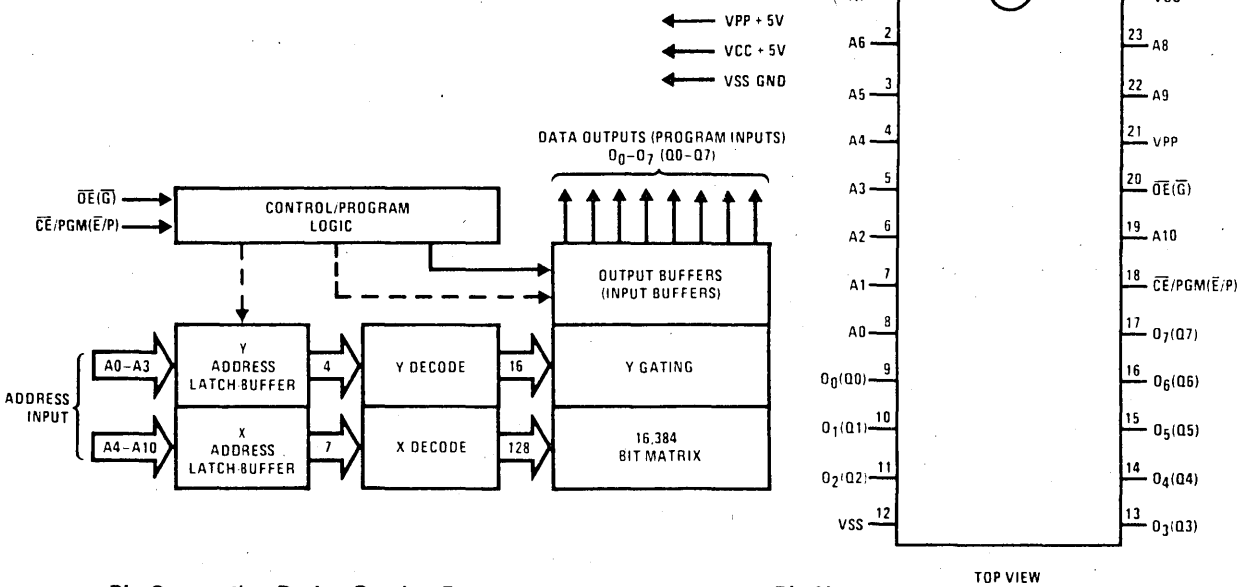
This EPROM is fabricated with the reliable, high volume, time proven, P²CMOS™ silicon gate technology.

P²CMOS™ and NSC800™ are trademarks of National Semiconductor Corp.
TRI-STATE® is a registered trademark of National Semiconductor Corp.

Features

- CMOS power consumption
  - 53 mW max active
  - 5.3 mW max standby
- Performance compatible to NSC800™ CMOS microprocessor and NMC6716 synchronous CMOS EPROM
- 2048 x 8 organization
- Pin compatible to 2716
- Access time down to 450 ns
- Single 5V power supply
- Static—no clocks required
- Inputs and outputs TTL compatible during both read and program modes
- TRI-STATE® output

Block and Connection Diagrams*



Pin Connection During Read or Program

Mode	Pin Name/Number				
	CE/PGM (E/P) 18	OE (G) 20	VPP 21	VCC 24	Outputs 9-11, 13-17
Read	VIL	VIL	5	5	DOUT
Program	Pulsed VIL to VIH	VIH	25	5	DIN

Pin Names

A0-A10	Address Inputs
O0-O7(Q0-Q7)	Data Outputs
CE/PGM (E/P)	Chip Enable/Program
OE (G)	Output Enable
VPP	Read 5V Program 25V
VCC	5V
VSS	Ground

* Symbols in parentheses are proposed industry standard.

IM-B25M52/Printed in U.S.A.

National Semiconductor

PRELIMINARY
May 1982

NMC27C32 32,768-Bit (4096 x 8) UV Erasable CMOS PROM

Parameter/Part Number	NMC27C32Q-35	NMC27C32Q-45	NMC27C32Q-55	NMC27C32Q-65
Access Time (ns)	350	450	550	650
Active Current (mA)	5	5	5	5
Standby Current (mA)	0.1	0.1	0.1	0.1

General Description

The NMC27C32 is a high speed 32k UV erasable and electrically reprogrammable CMOS EPROM ideally suited for applications where fast turn-around, pattern experimentation and low power consumption are important requirements.

The NMC27C32 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

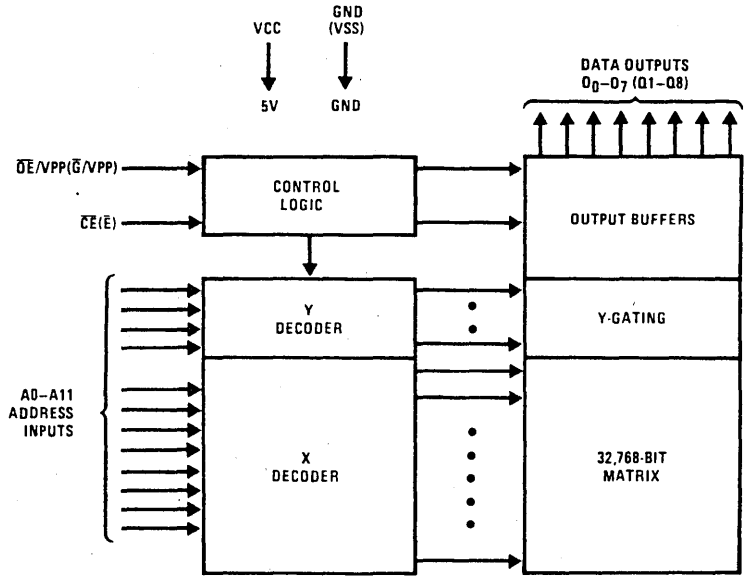
This EPROM is fabricated with the reliable, high volume, time proven. P^2CMOS^{TM} silicon gate technology.

P^2CMOS^{TM} and $NSC800^{TM}$ are trademarks of National Semiconductor Corp.
TRI-STATE® is a registered trademark of National Semiconductor Corp.

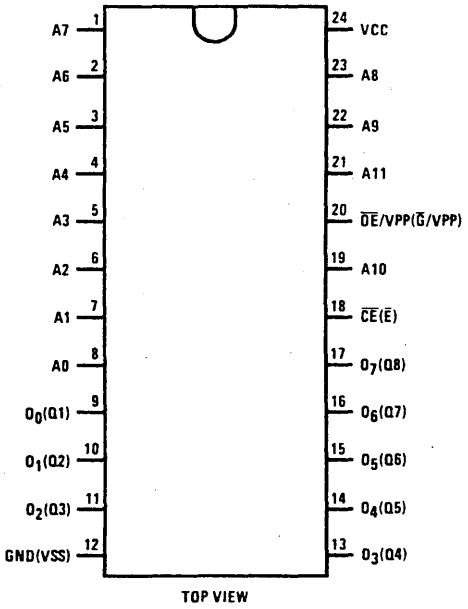
Features

- CMOS power consumption
  53 mW max active
  5.3 mW max standby
- Performance compatible to $NSC800^{TM}$ CMOS microprocessor and NMC6732 synchronous CMOS EPROM
- 4096 x 8 organization
- Pin compatible to 2732
- Access time down to 350 ns
- Single 5V power supply
- Static—no clocks required
- Inputs and outputs TTL compatible during both read and program modes
- TRI-STATE® output

Block and Connection Diagrams*



Dual-In-Line Package



Modes*

Mode	Pin Name/Number			
	CE (E) 18	OE/VPP (G/VPP) 20	VCC 24	Outputs 9-11, 13-17
Read	VIL	VIL	5V	DOUT
Standby	VIH	Don't Care	5V	Hi-Z
Program	VIL	25V	5V	DIN
Program Verify	VIL	VIL	5V	DOUT
Program Inhibit	VIH	25V	5V	Hi-Z

Pin Names*

CE (E)	Chip Enable
OE (G)	Output Enable
A0-A11	Address Inputs
O_0-O_7 (Q1-Q8)	Data Outputs
VPP	Program Power 25V
VCC	Power 5V
GND (VSS)	Ground

*Symbols in parentheses are proposed industry standard.

IM-B25M52/Printed in U.S.A.

National Semiconductor

MM5290*16,384-Bit (16,384 x 1) Dynamic RAM

General Description

The MM5290 is a 16,384 x 1 bit dynamic RAM. It features a multiplexed address input with separate row and column strobes. This added flexibility allows the MM5290 to be used in page mode operation.

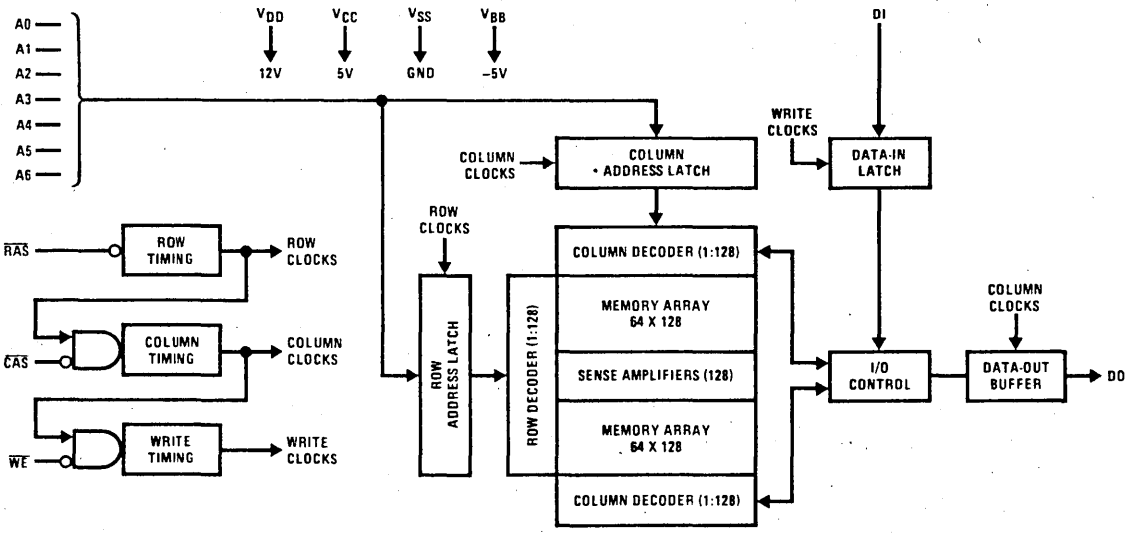
The MM5290 must be refreshed every 2 ms. This can be accomplished by performing any cycle which brings the Row Address Strobe active including a $\overline{RAS}$-only cycle at each of the 128 row addresses.

N-channel double-poly silicon gate technology, developed by National, is used in the manufacture of the MM5290. This process combines high density and performance with reliability. Greater system densities are achievable by the use of a 16-pin dual-in-line package for the MM5290.

Features

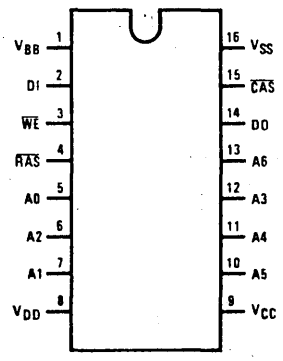
- Access times: 150 ns, 200 ns, 250 ns
- Low power: 528 mW max
- TTL compatible: all inputs and output
- Gated $\overline{CAS}$—noncritical timing
- Read, Write, Read-Modify-Write and $\overline{RAS}$-only Refresh cycles
- Page mode operation
- Industry standard 16-pin configuration

Block Diagram



Connection Diagram

Dual-In-Line Package

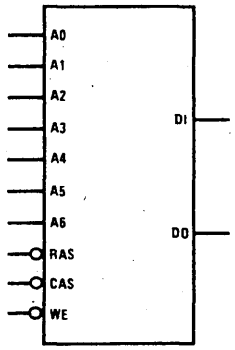


TOP VIEW

Pin Names

$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0–A6	Address Inputs
DI	Data Input
DO	Data Output
V_{DD}	Power (12V)
V_{CC}	Power (5V)
V_{SS}	Ground
V_{BB}	Power (−5V)

Logic Diagram



*See the MST™ Program page 3 of the 1980 Memory Databook.

MST™ is a trademark of National Semiconductor Corp.

National Semiconductor

PRELIMINARY
August 1982

NMC9306/COP494 256-Bit Serial Electrically Erasable Programmable Memory

General Description

The NMC9306/COP494 is a 256-bit non-volatile sequential access memory fabricated using advanced floating gate N-channel E^2PROM technology. It is a peripheral memory designed for data storage and/or timing and is accessed via the simple MICROWIRE™ serial interface. The device contains 256 bits of read/write memory divided into 16 registers of 16 bits each. Each word can be serially read or written by a COP400 series controller. Written information is stored in a floating gate cell with at least 10 years data retention and can be updated by an erase-write cycle. The NMC9306/COP494 has been designed to meet applications requiring up to 1×10^4 erase/write cycles per register. A power down mode reduces power consumption by 70 percent.

Features

- Low cost
- Single supply operation (5V ± 10%)
- TTL compatible
- 16 x 16 serial read/write memory
- MICROWIRE compatible serial I/O
- Compatible with COP400 processors
- Low standby power
- Non-volatile erase and write
- Reliable floating gate technology

Block and Connection Diagrams

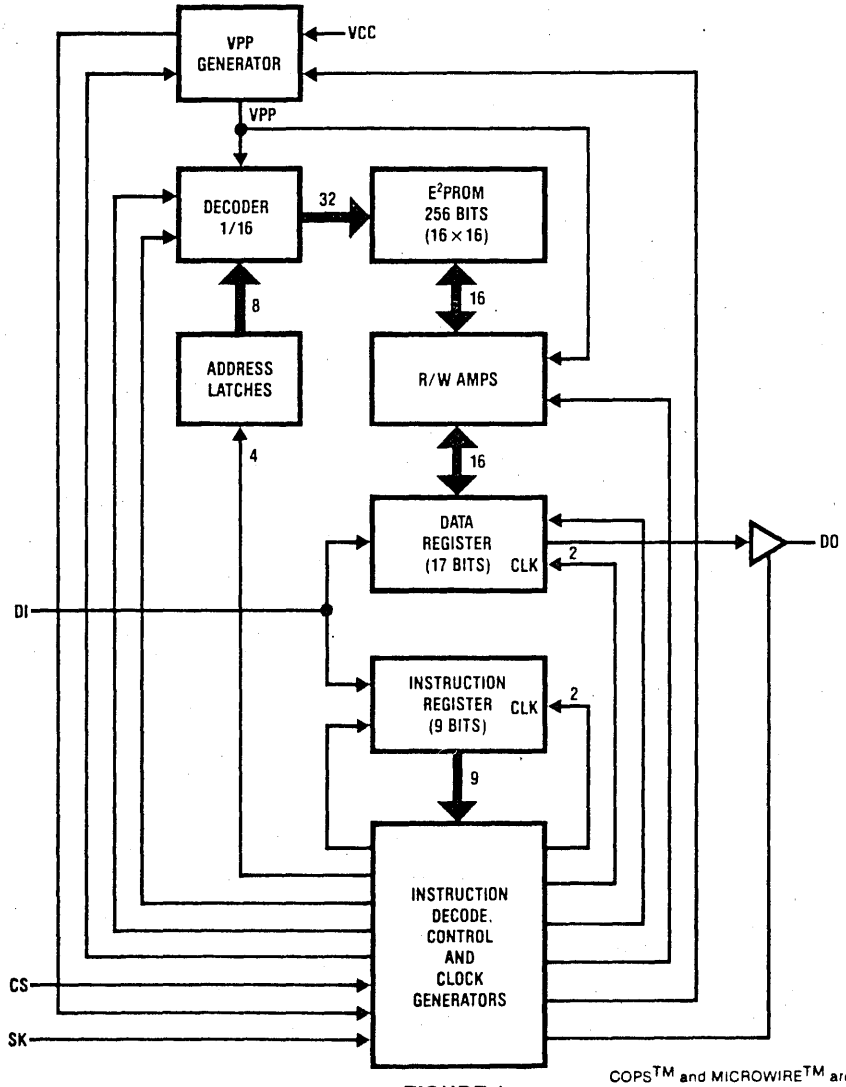


FIGURE 1

Dual-In-Line Package

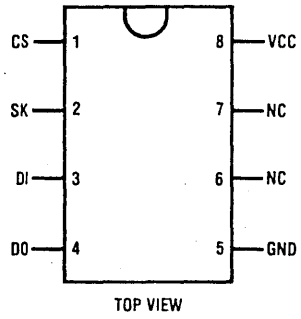


FIGURE 2

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
VCC	Power Supply
GND	Ground

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TRI-STATE® is a registered trademark of National Semiconductor Corp.

IM-B25M82/Printed in U.S.A.

National Semiconductor

PRELIMINARY
April 1982

NMC9716 16k (2k x 8) Electrically Erasable PROM

Max Access/Current	NMC9716-25	NMC9716-35	NMC9716-45
Max Access Time (ns)	250	350	450
Max Active Current (mA)	110	110	110
Max Standby Current (mA)	50	50	50

General Description

The NMC9716 is a 16,384-bit electrically erasable and programmable read-only memory (E^2PROM) fabricated using National's high speed, low power, N-channel double silicon gate technology. The electrical erase/write capability of the NMC9716 makes it ideal for a wide variety of applications requiring in-system, non-volatile erase and write.

The NMC9716 is pin and functionally compatible with the NMC2816 E^2PROM, with the added system feature of erasing/writing with a 5V TTL pulse on chip enable ($\overline{CE}$), while the VPP is held at 21V. The erase/write cycle is very similar to the industry standard 2716 EPROM programming cycle.

The device operates from a 5V power supply in the read mode and, with its very fast read access speed, is compatible with high performance microprocessors.

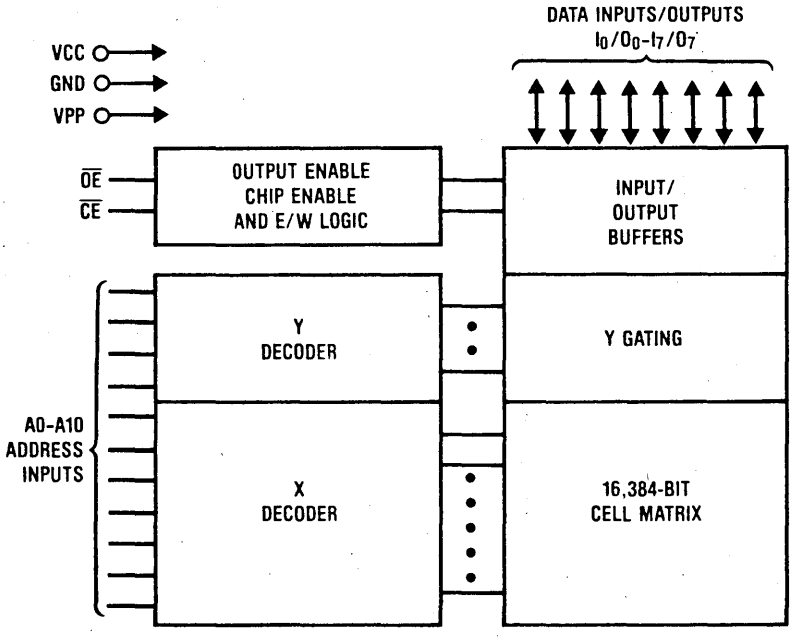
The NMC9716 is deselected when $\overline{CE}$ input is high and is automatically placed in the standby mode. This mode provides a 52% reduction in power with no increase in access time. The NMC9716 also has an output enable control to eliminate bus contention in a system environment.

The NMC9716 can be easily erased and reprogrammed in a byte-by-byte mode and the entire memory array can be erased with a single programming pulse in the chip erase mode. Byte erase is identical to byte write, with all inputs at logic one (TTL high).

Features

- Erase/write with a 5V TTL pulse or a 21V pulse
- Pin and functionally compatible with the NMC2816
- No rise time restriction on erase/write pulse
- 2048 x 8 organization
- Conforms to JEDEC byte-wide family standard
- Microprocessor compatible architecture
- Single byte erase/write capability
- 10 ms byte erase/write time
- 10 ms chip erase mode
- Low power dissipation
  - 610 mW max (active power ICC + IPP)
  - 295 mW max (standby power ICC + IPP)

Block and Connection Diagrams

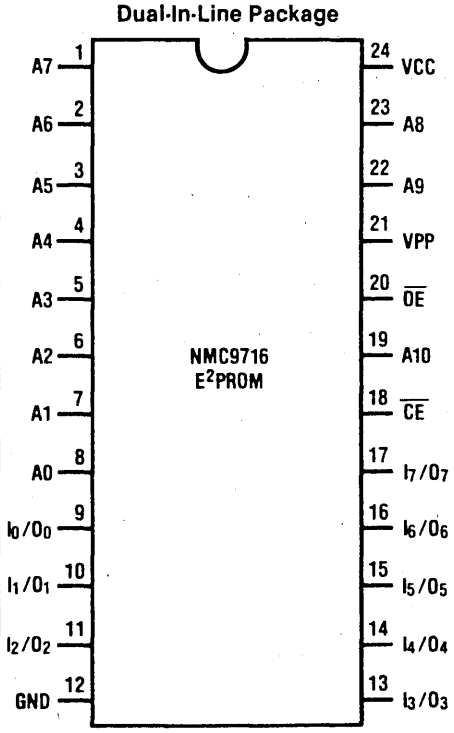


Pin Names

A0-A10	Addresses	O_0-O_7	Data Outputs
$\overline{CE}$	Chip Enable	I_0-I_7	Data Inputs
$\overline{OE}$	Output Enable	VPP	Program Voltage

FIGURE 1

Dual-In-Line Package



TOP VIEW

FIGURE 2

IM-B25M42/Printed in U.S.A.

National Semiconductor

PRELIMINARY
April 1982

NMC9716E 16k (2k x 8) Electrically Erasable PROM

Max Access/Current	NMC9716E-25	NMC9716E-35	NMC9716E-45
Max Access Time (ns)	250	350	450
Max Active Current (mA)	125	125	125
Max Standby Current (mA)	55	55	55

General Description

The NMC9716E is a 16,384-bit electrically erasable and programmable read-only memory (E^2PROM) fabricated using National's high speed, low power, N-channel double silicon gate technology. The electrical erase/write capability of the NMC9716E makes it ideal for a wide variety of applications requiring in-system, non-volatile erase and write.

The NMC9716E is pin and functionally compatible with the NMC2816E E^2PROM, with the added system feature of erasing/writing with a 5V TTL pulse on chip enable ($\overline{CE}$), while the VPP is held at 21V. The erase/write cycle is very similar to the industry standard 2716 EPROM programming cycle.

The device operates from a 5V power supply in the read mode and, with its very fast read access speed, is compatible with high performance microprocessors.

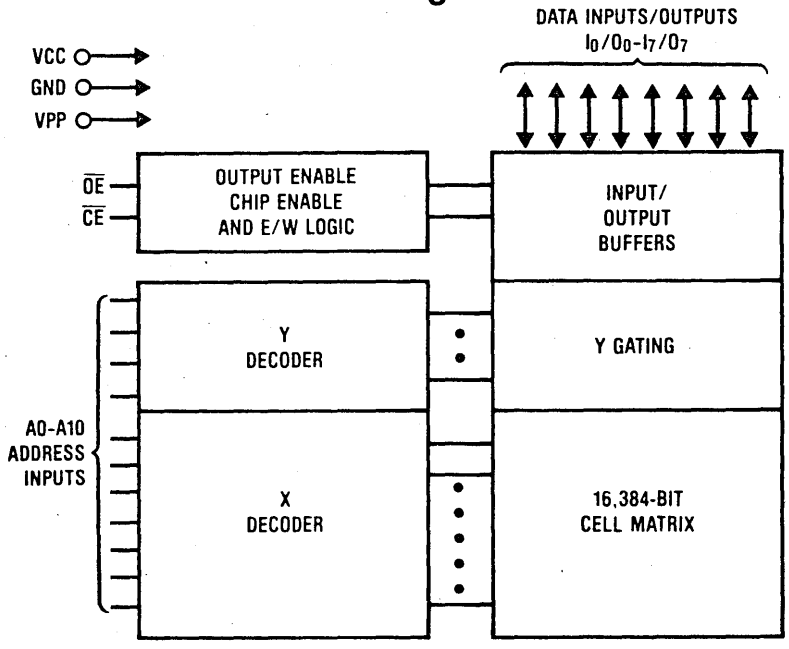
The NMC9716E is deselected when $\overline{CE}$ input is high and is automatically placed in the standby mode. This mode provides a 54% reduction in power with no increase in access time. The NMC9716E also has an output enable control to eliminate bus contention in a system environment.

The NMC9716E can be easily erased and reprogrammed in a byte-by-byte mode and the entire memory array can be erased with a single programming pulse in the chip erase mode. Byte erase is identical to byte write, with all inputs at logic one (TTL high).

Features

- Erase/write with a 5V TTL pulse or a 21V pulse
- Pin and functionally compatible with the NMC2816E
- No rise time restriction on erase/write pulse
- 2048 x 8 organization
- Conforms to JEDEC byte-wide family standard
- Microprocessor compatible architecture
- Single byte erase/write capability
- 10 ms byte erase/write time
- 10 ms chip erase mode
- Low power dissipation
  720 mW max (active power ICC + IPP)
  335 mW max (standby power ICC + IPP)

Block and Connection Diagrams

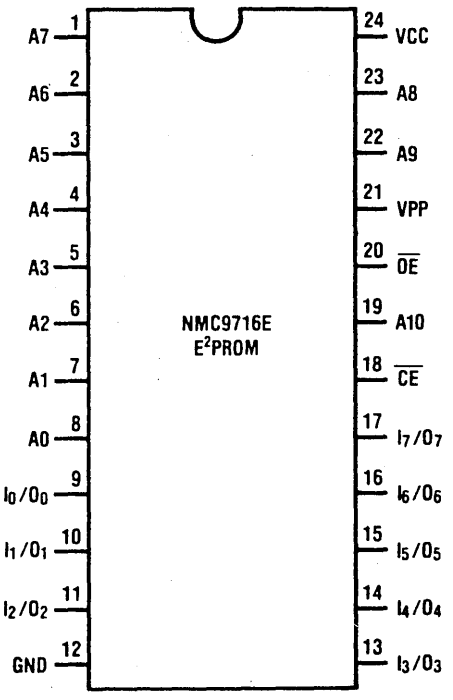


Pin Names

A0-A10	Addresses	O_0-O_7	Data Outputs
$\overline{CE}$	Chip Enable	I_0-I_7	Data Inputs
$\overline{OE}$	Output Enable	VPP	Program Voltage

FIGURE 1

Dual-In-Line Package



TOP VIEW

FIGURE 2

IM-B25M42/Printed in U.S.A.

National Semiconductor

PRELIMINARY
April 1982

NMC9716M 16k (2k x 8) Electrically Erasable PROM

Max Access/Current	NMC9716M-25	NMC9716M-35	NMC9716M-45
Max Access Time (ns)	250	350	450
Max Active Current (mA)	140	140	140
Max Standby Current (mA)	60	60	60

General Description

The NMC9716M is a 16,384-bit electrically erasable and programmable read-only memory (E^2PROM) fabricated using National's high speed, low power, N-channel double silicon gate technology. The electrical erase/write capability of the NMC9716M makes it ideal for a wide variety of applications requiring in-system, non-volatile erase and write.

The NMC9716M is pin and functionally compatible with the NMC2816M E^2PROM, with the added system feature of erasing/writing with a 5V TTL pulse on chip enable ($\overline{CE}$), while the VPP is held at 21V. The erase/write cycle is very similar to the industry standard 2716 EPROM programming cycle.

The device operates from a 5V power supply in the read mode and, with its very fast read access speed, is compatible with high performance microprocessors.

The NMC9716M is deselected when $\overline{CE}$ input is high and is automatically placed in the standby mode. This mode provides a 55% reduction in power with no increase in access time. The NMC9716M also has an output enable control to eliminate bus contention in a system environment.

The NMC9716M can be easily erased and reprogrammed in a byte-by-byte mode and the entire memory array can be erased with a single programming pulse in the chip erase mode. Byte erase is identical to byte write, with all inputs at logic one (TTL high).

Features

- Erase/write with a 5V TTL pulse or a 21V pulse
- Pin and functionally compatible with the NMC2816M
- No rise time restriction on erase/write pulse
- 2048 x 8 organization
- Conforms to JEDEC byte-wide family standard
- Microprocessor compatible architecture
- Single byte erase/write capability
- 10 ms byte erase/write time
- 10 ms chip erase mode
- Low power dissipation
  800 mW max (active power ICC + IPP)
  360 mW max (standby power ICC + IPP)

Block and Connection Diagrams

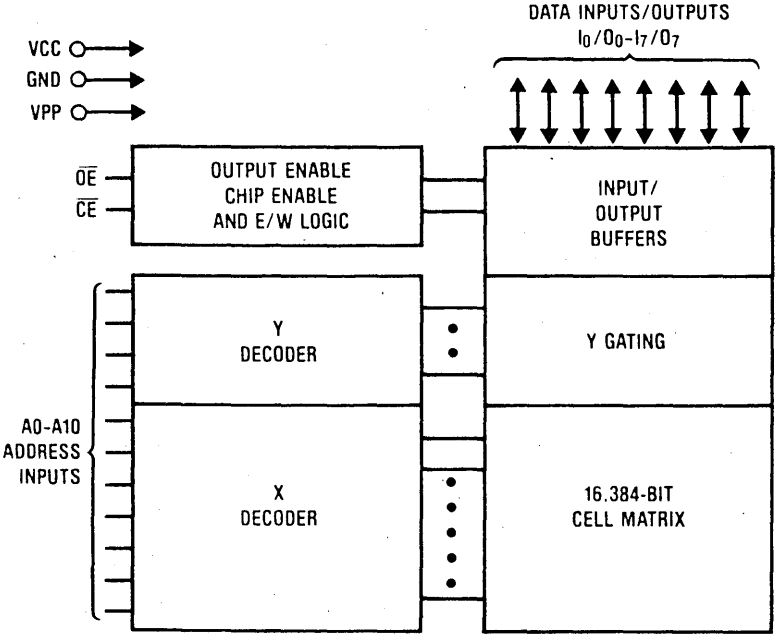


FIGURE 1

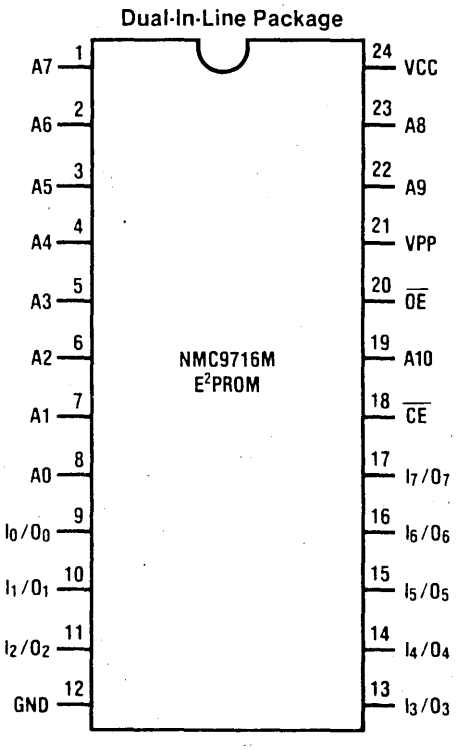


FIGURE 2

Pin Names

A0-A10	Addresses	O_0-O_7	Data Outputs
$\overline{CE}$	Chip Enable	I_0-I_7	Data Inputs
$\overline{OE}$	Output Enable	VPP	Program Voltage

National Semiconductor

PRELIMINARY
June 1982

MA2016 16,384 x 8-Bit CMOS Static RAM Module

General Description

The MA2016 consists of eight 2k x 8-bit CMOS RAMs along with an address decoder capable of decoding up to a 128k x 8-bit low power CMOS RAM. It operates on a single 5V power supply and is able to retain data down to 2V. The MA2016 does not require a refresh and all inputs and outputs are TTL compatible. Multiple MA2016 modules may be stacked in a piggyback fashion or laid out in any manner desired. The low power requirements and versatile layout make the MA2016 very useful for low power hand-held battery powered applications.

Applications

- Portable terminals
- Hand-held devices
- Pos terminals
- Remote instrumentation
- Process controllers
- Microcomputer memory

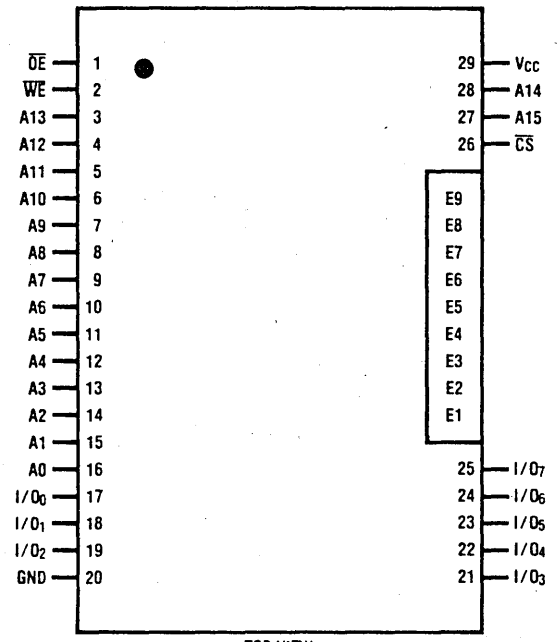
Features

- 16k x 8-bits fully decoded
- Outputs directly TTL compatible
- Low power—typical 400 mW
- 250 ns access time
- Static operation—no clocks or refreshing required
- Single 5V supply ± 10%
- 2V minimum for data retention
- TRI-STATE® outputs for bus operation
- Common data I/O pins
- Separate OE pin
- Internal power supply decoupling

Ordering Information

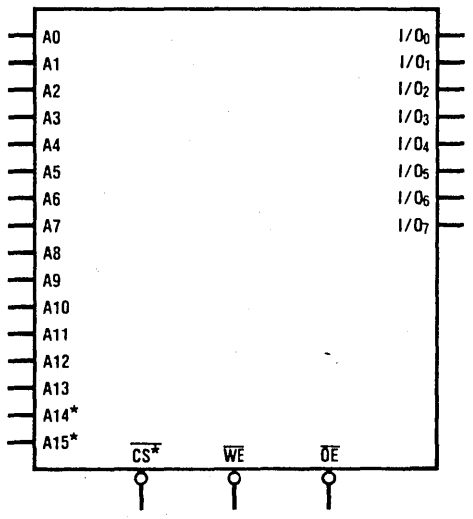
MA2016

Connection Diagram



TOP VIEW

Logic Symbol



* active state user selectable

Pin Names

$\overline{CS}$	Chip Select Input (user programmable)
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O_0-I/O_7	Data Inputs/Outputs
A0-A15	Address Inputs (A14, A15 Block Select, user programmable)
V_{CC}	Power (typical 5V)
GND	Ground

TRI-STATE® is a registered trademark of National Semiconductor Corp.

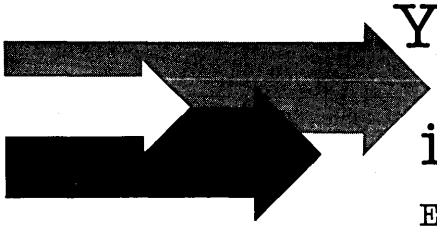
Truth Table

$\overline{CS}$*	$\overline{WE}$	$\overline{OE}$	I/O	Mode
H	X	X	Hi-Z	Standby
L	H	L	D_{OUT}	Read
L	H	H	Hi-Z	Read
L	L	X	D_{IN}	Write

* $\overline{CS}$ state is user selectable. Table shown with jumper E7 to E8 and E4 to E5 installed.

IM-B25M62/Printed in U.S.A.

Call on OKI Semiconductor



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to optimize system design

PART NUMBER	DESCRIPTION
MOS DYNAMIC RAM	
MSM3764-12RS	65536-Word x 1-Bit RAM (NMOS)
MSM3764-15RS	65536-Word x 1-Bit RAM (NMOS)
MSM3764-20RS	65536-Word x 1-Bit RAM (NMOS)
MSM37256AS	256K Word x 1-Bit RAM (NMOS)*
MOS STATIC RAM	
MSM2114L 2RS	1024-Word x 4-Bit RAM (NMOS)
MSM2128-12RS	2048-Word x 8-Bit RAM (NMOS) w/power down
MSM2128-15RS	2048-Word x 8 Bit RAM (NMOS) w/power down
MSM2128-20RS	2048-Word x 8-Bit RAM (NMOS) w/power down
MSM5104-2RS	4096-Word x 1-Bit RAM (CMOS)
MSM5114-2RS	1024-Word x 4-Bit RAM (CMOS)
MSM5115-2RS	1024-Word x 4-Bit RAM (CMOS)
MSM5128-12RS	2048-Word x 8-Bit RAM (CMOS)
MSM5128-15RS	2048-Word x 8-Bit RAM (CMOS)
MSM5128-20RS	2048-Word x 8-Bit RAM (CMOS)
MSM5188RS	8192-Word x 8-Bit RAM (CMOS)†
CMOS ROM	
MSM53256	32K x 8 ROM†
MASK ROM	
MSM2916RS	2048-Word x 8-Bit Mask ROM (NMOS)
MSM2932RS	4096-Word x 8-Bit Mask ROM (NMOS)
MSM2964RS	8192-Word x 8-Bit Mask ROM (NMOS)
MSM38128RS	16384-Word x 8-Bit Mask ROM (NMOS)
MSM28101AS	1083880 Bit Mask ROM (NMOS)
EPROM	
MSM2708AS	1024-Word x 8-Bit EPROM (NMOS)
MSM2716AS	2048-Word x 8-Bit EPROM (NMOS)
MSM2764AS	8192-Word x 8-Bit EPROM (NMOS)
CMOS MICROCOMPUTERS	
MSM5840 RS	4 Bit Micro w/2K x 8 ROM, 128 x 4 RAM
MSM5842 RS	4 Bit Micro w/768 x 8 ROM, 32 x 4 RAM
MSM5845 RS	4 Bit Micro w/1280 x 8 ROM, 64 x 4 RAM
MSM58421 GSK	4 Bit Micro w/1536 x 8 ROM 40 x 4 RAM & LCD Direct Drive Output
MSM58422 RS	4 Bit Micro w/1536 x 8 ROM 40 x 4 RAM & VF Display Direct Drive
MSM5846 GSK	4 Bit Micro w/1728 x 8 ROM 64 x 4 RAM & 62 Segment MUX LCD Outputs
MSM80C48 RS	8 Bit Micro w/1K x 8 ROM, 64 x 8 RAM
MSM80C49 RS	8 Bit Micro w/2K x 8 ROM, 128 x 8 RAM
MSM80C35 RS	8 Bit Micro, 64 x 8 RAM, External ROM
MSM80C39 RS	8 Bit Micro, 128 x 8 RAM, External ROM
CMOS MICROPROCESSOR	
MSM80C85A RS	8 Bit CMOS Version of MSM80C85A
NMOS MICROPROCESSOR	
MSM8085A RS	8 Bit Microprocessor
MICROCOMPUTER DEVELOPMENT PACKAGES	
EASE-40-I/C	Emulator Board System For Series 40 CMOS 4 Bit Microcomputer Family. Hardware, Software, Documentation Compatible with ISIS® or CP/M.®
EASE-49-I/C	Board System For Series 80 CMOS 8 Bit Microcomputer Family (80C48/80C49). Hardware, Software Documentation ISIS® or CP/M® Compatible.

*3Q83 †TBA

PART NUMBER	DESCRIPTION
PERIPHERAL CIRCUITS	
MSM3914ARS	Keyboard Encoder
MSM5832/ 58321RS	Microprocessor Real-Time Clock/Calendar (CMOS)
MSM81C55	256 Word x 8 Bit CMOS Static RAM With I/O
MSM83C55	2K x 8 CMOS ROM With I/O
MSM82C12	CMOS 8 Bit I/O Port
MSM82C53-5	CMOS Programmable Interval Timer
MSM82C55A-5	CMOS Programmable Peripheral Interface
CHARACTER GENERATORS AND DISPLAY DRIVERS	
MSL912RS	Octal +30V Display Driver
MSL915RS	Octal −60V Display Driver
MSL917RS	Octal −60V Display Driver
MSL9510RS	8D Multiplex Control/Decoder
MSL9511RS	8D Multiplex Control/Decoder
MSL9650-01AS	64 ch. 35 Output Character Generator
MSL9662-01RS	64 ch. 16 Seg. Character Generator
MSL9663-01RS	64 ch. 16 Seg. Character Generator
MSL9664-01RS	64 ch. 14 Seg. Character Generator
MSL9665-01RS	64 ch. 14 Seg. Character Generator
MSL966RS	LED Digit Driver
MSM5219GSK	48 Segment CMOS Shift Register Type Static LCD Driver
MSM58282RS	4 Digit LED Driver
MSM58283RS	4 Digit VF Driver
MSM58292RS	5 Digit LCD Driver
MSM58293GS	5 Digit VF Driver
MSM58371RS	Serial input 12 Bit LED Driver
MSM5838RS	LCD Dot Matrix Display Driver (for Row Scanning)
MSM5839GS	LCD Dot Matrix Display Driver (for Column Sources)
TELECOMMUNICATIONS CIRCUITS	
MSM6910AS	CMOS Single Chip Codec with Filters
MSM6917AS	μ-255 Law Companding Codes
MSM6912AS	PCM Channel Filter
MOS VOICE SYNTHESIS	
MSM5218RS	ADPCM Speech Analyzer/Synthesizer
MSM5205RS	ADPCM Speech Synthesizer (External ROM)
MSM6202GSK	ADPCM Speech Synthesizer with ROM
MSM5204RS	8 Bit CMOS Analog to Digital Converter
PHASE-LOCKED LOOP (PLL) AND MOTOR CONTROLLERS	
MSM5816RS	VTR/Turntable Motor Control (PLL)
MSM5819	Turntable Motor Control (PLL)
AUDIO AND RC DEVICES	
MSL2312RS	÷ 10/ ÷ 100 Prescaler
MSM5524RS	VF AM/FM/SW Frequency Counter w/Clock
MSM5525RS	VF AM/FM Frequency Counter
MSM5803GS	LCD AM/FM/SW/LW Frequency Counter w/ALARM Clock
MSL9362RS	4 Channel R/C Transmitter
MSL9363RS	4 Channel R/C Receiver
DIGITAL CLOCKS	
MSM5509RS	MUX LED Clock
MSM5528RS	Static VF Clock
MSM5550RS	VF Alarm Radio Clock
MSM5557RS	MUX LCD Alarm Clock
MSM5558/ 55581RS	Static VF Auto Clock

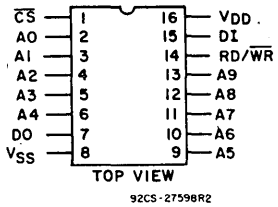
OKI SEMICONDUCTOR

Random Access Memories (RAM's)
CDP, CDM, MWS, CD Series

RCA offers a full line of CMOS RAM's for use with the CDP1800 line of microprocessors or for general-purpose applications. Industry standard pinout devices are represented by the MWS and CD series. RAM sizes range from 32 bits to 4K bits.

All types are available in both plastic and ceramic packages, except for the CDP1821, CD4036, CD4039, and CD4061A, which are available in ceramic packages only.

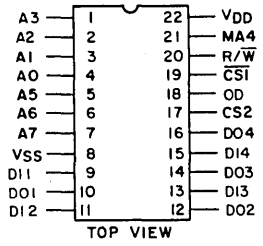
CDP1821
1024 x 1



TOP VIEW

92CS-27598R2

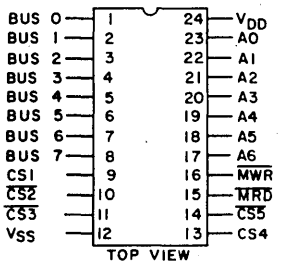
CDP1822
256 x 4



TOP VIEW

92CS-27592R1

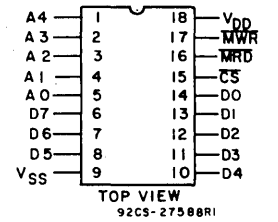
CDP1823
128 x 8



TOP VIEW

92CS-28703R1

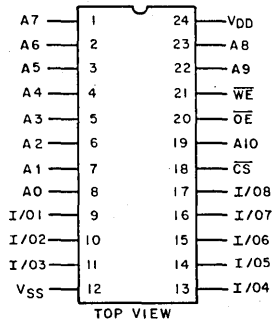
CDP1824
32 x 8



TOP VIEW

92CS-27588R1

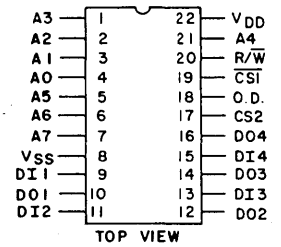
CDM6116
2048 x 8



TOP VIEW

92CS-35043

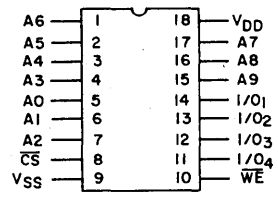
MWS5101, MWS5101A
256 x 4



TOP VIEW

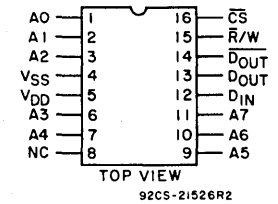
92CS-29976R1

MWS5114
1024 x 4



92CS-30982R1

CD4061A, CD40061A
256 x 1



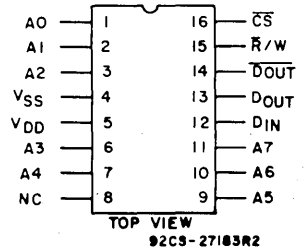
TOP VIEW

92CS-21526R2

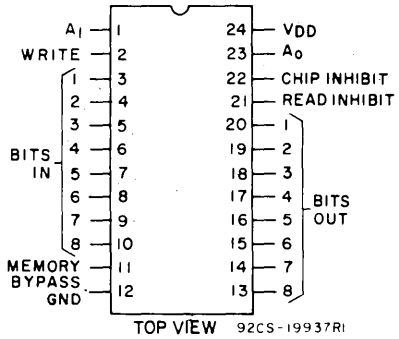
Comparison of RAM Features

Features	CDP				CDM	MWS			CD				Units
	1821	1822	1823	1824	6116	5101	5101A	5114	4036/39	4061A	40061A	40114B	
Organization	1Kx1	256x4	128x8	32x8	2Kx8	256x4	256x4	1Kx4	4x8	256x1	256x1	16x4	Bits
Package Size (Pins)	16	22	24	18	24	22	22	18	24	16	16	16	Pins
Separate Data I/O's	Yes	Yes	—	—	—	Yes	Yes	—	Yes	Yes	Yes	Yes	
3-State Data Out	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	—	Yes	Yes	Yes	
Multiple Chip Select	—	Yes	Yes	—	—	Yes	Yes	—	—	—	—	—	
Common R/W	Yes	Yes	—	—	—	Yes	Yes	Yes	—	Yes	Yes	—	
Byte Wide	—	—	Yes	Yes	Yes	—	—	—	Yes	—	—	—	
TTL Input	—	—	—	—	Yes	—	Yes	Yes	—	—	—	—	
Max. Access Time	Over temp. range of -40°C to +70°C					Over temp. range of 0°C to +70°C			At +25°C				
								300(-1)					
At 5 V	250	450	450	710	250	250(L2)	250(L2)	250(-2)	1000	750	700	650	ns
						350(L3)	350(L3)	200(-3)					
At 10 V	125	250	250	320	—	—	—	—	400	380	265	280	
Max. Quiescent	Over temp. range of -40°C to +85°C					Over temp. range of 0°C to +70°C			At +125°C				
Current	500	500	500	100	100(1)	50(L2)	50(L2)	250(-1)	300	150	10	150	
At 5 V	—	—	—	500(C)	30(2)	200(L3)	200(L3)	100(-2)	—	—	—	—	μA
	—	—	—	—	—	—	—	100(-3)	—	—	—	—	
At 10 V	1000	1000	1000	500	—	—	—	—	600	300	20	300	
Min. Data Reten. Voltage	2.5	2	2	2.5	2	2	2	2	3	3	3	3	V
Data Retention	100	100	50	50	50(1)	10(L2)	10(L2)	125(-1)	—	—	—	—	
Current	—	—	—	250(C)	15(2)	50(L3)	50(L3)	25(-2)	—	—	—	—	μA
								25(-3)	—	—	—	—	
	CDP	CDP	CDP			CDP	CDP	CDP					
Suggested	1859	1858	1859			1858	1858	1866					
Latch/Decoder	1866		1866					1868					
	1868		1867										
			1868										

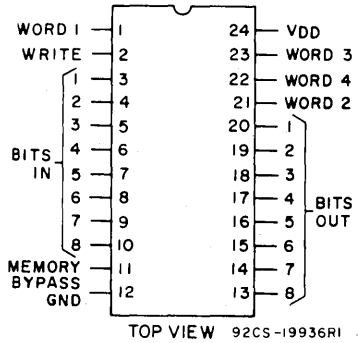
CD40114B
16 x 4



CD4036
4 x 8



CD4039
4 x 8



Read-Only Memories (ROM's)

CDP1831, CDP1833, CDP1835, CDP1837

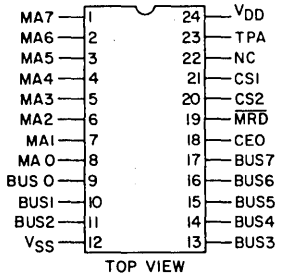
Mask-Programmable ROM's

RCA offers a line of byte-wide read-only memories that are ideal for low-power nonvolatile data storage for 8-bit microprocessor systems. ROM sizes range from 512 to 4096 bytes.

ROM program patterns can be submitted to RCA by using a master device (PROM or EPROM), floppy diskette generated on an RCA development system, or computer punch cards. Complete details for ordering custom ROMs are contained in RCA publication RPP-610.

- **Self-Contained High-Order Address Latch**
- **Interfaces Directly to CDP1800-Series Microprocessors**
- **Chip-Enable Output for RAM Disable**
- **Mask - Programmable Address Location**
- **Polarity Option on Chip Select**
- **Compatible Pinouts on all Types**

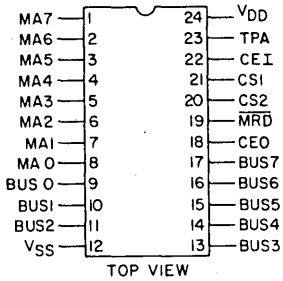
CDP1831
Terminal-Assignment Diagram



NC = NO CONNECTION

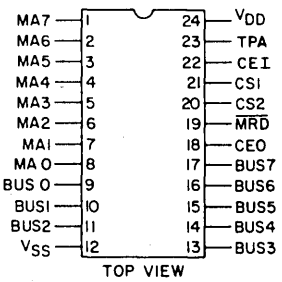
92CS-27584R2

CDP1833, CDP1837
Terminal-Assignment Diagram



92CS-28889R2

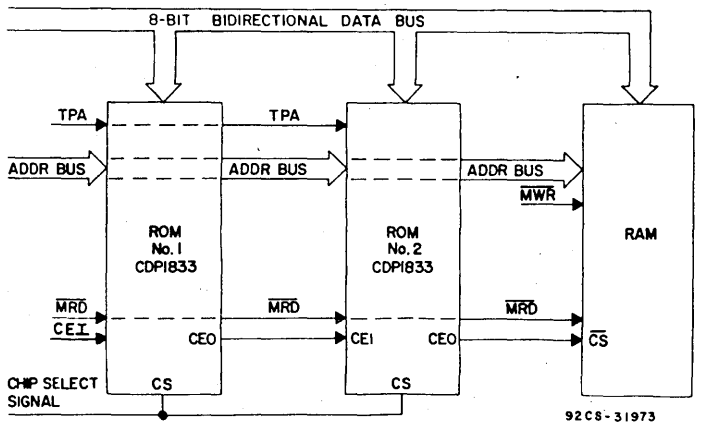
CDP1835
Terminal-Assignment Diagram



92CS-32376

"Daisy Chaining" with CEI inputs and CEO outputs is used to avoid memory conflicts between ROM and RAM in a user system. In the configuration shown, if ROM #1 is masked-programmed for memory locations 0000-03FF$_{16}$ and ROM #2 is masked-programmed for memory locations 0400$_{16}$-07FF$_{16}$, for addresses from 0000-07FF$_{16}$ the RAM is disabled and the ROM enabled. For locations above 07FF$_{16}$ the ROM's are disabled and the RAM enabled.

Daisy Chaining CDP1833 ROM's.



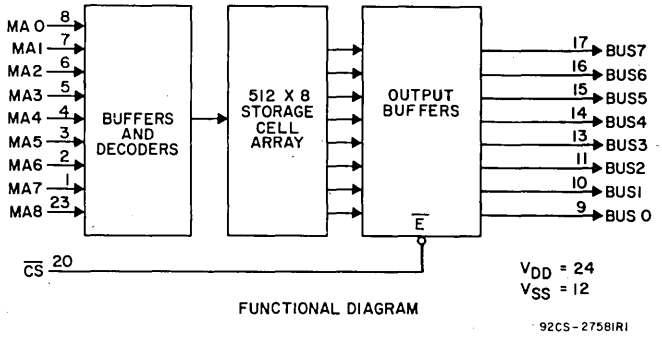
92CS-31973

CDP1832, CDP1834 Mask-Programmable ROM's

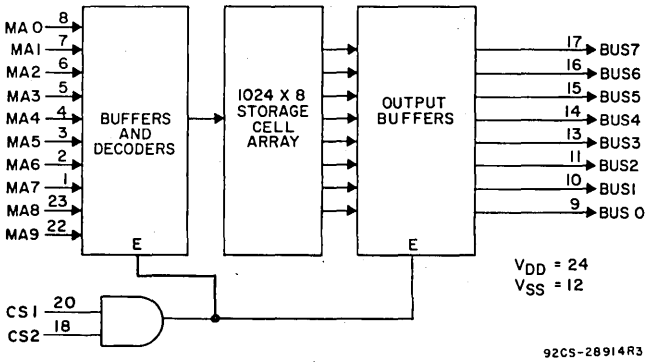
The CDP1832 and the CDP1834 DO NOT have on-board address latches, but are designed primarily as pin-for-pin replacements for industry types 2704 and 2708 respectively.

A typical system with an external address latch that is common with most large systems is shown here.

- **Pin-Compatible with industry types 2704 and 2708**
- **Accepts standard memory address decoding**
- **Polarity options on chip selects**

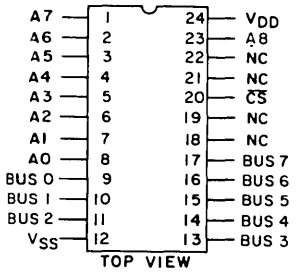


CDP1832 Functional diagram.



CDP1834 Functional diagram.

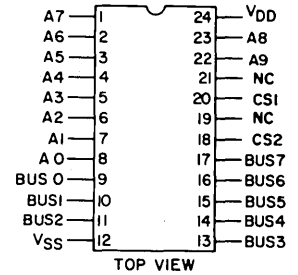
CDP1832
Terminal-Assignment Diagram



NC = NO CONNECTION

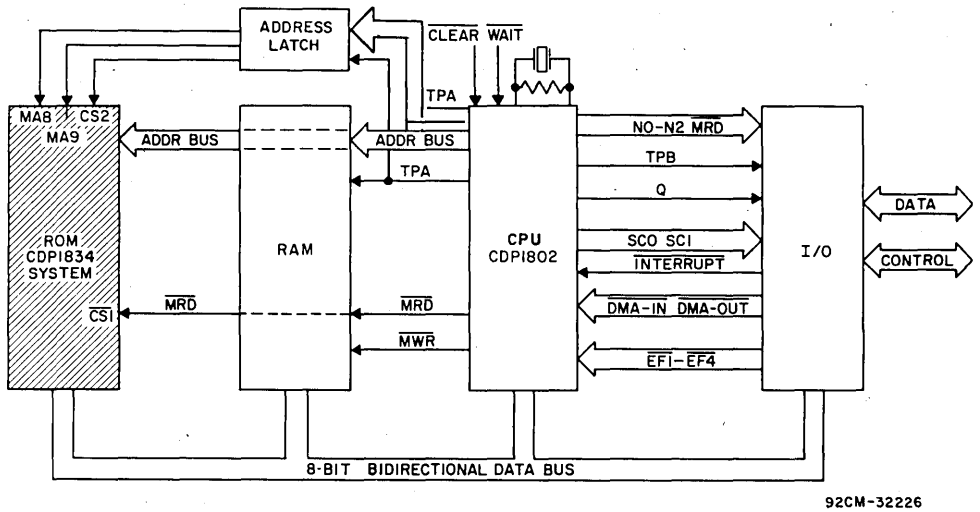
92CS-27579R2

CDP1834
Terminal-Assignment Diagram



NC = NO CONNECTION

92CS-28727RI



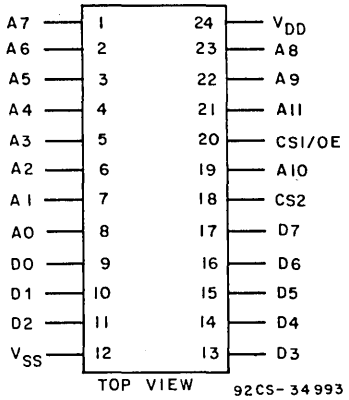
Typical CDP1802 microprocessor system.

CDM5332, CDM5333 Preliminary Data
CMOS 4096-Word x 8-Bit Static Read-Only Memory

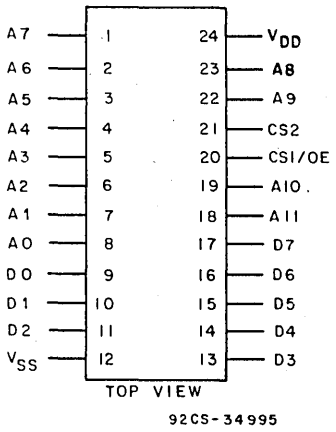
The RCA CDM5332 and CDM5333 are 32,768-bit mask-programmable CMOS Read Only Memories organized as 4096-word x 8-bits and are designed for use in general purpose microprocessor systems, such as the CDP1800-series system. Two chip-select inputs (CS1, CS2) are provided for memory expansion. Chip selects CS1 and CS2 directly gate the output buffers. Chip select CS2 gates the address decoder for the standby mode. The polarity for each chip select is user mask-programmable.

The CDM5332 and CDM5333 differ only in terminal assignments and are pin-compatible with standard industry types. CDM5332 is pin compatible with Intel 2732 and 2332A. CDM5333 is pin compatible with Supertex CM3200, T.I. TMS4732, and Motorola MCM68732 and MCM68A332. The CDM5332 and CDM5333 are supplied in 24-lead dual-in-line ceramic packages (D suffix) and 24-lead dual-in-line plastic packages (E suffix).

- *Low power replacement for NMOS ROMS*
- *Choice of two industry standard pin outs:*
  CDM5332 is pin compatible with INTEL 2732 and 2332A
  CDM5333 is pin compatible with Supertex CM3200, TI TMS 4732, Motorola MCM 68732 and MCM 68A332
- *Fast access time: 450 ns at 5 V*
- *TTL input and output compatible*
- *Three state outputs*
- *Two programmable chip selects*



CDM5332
TERMINAL ASSIGNMENT

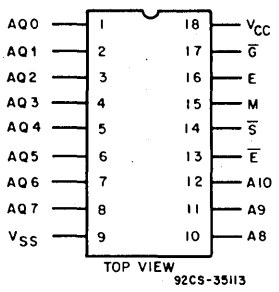


CDM5333
TERMINAL ASSIGNMENT

CDP65516 Objective Data
CMOS 2048-Word x 8-Bit Static Read-Only Memory

The CDP65516 is a complementary MOS mask programmable byte organized read-only memory (ROM). The CDP65516 is organized as 2048 bytes of 8 bits, designed for use in multiplex bus systems. It is fabricated using silicon gate CMOS technology, which offers low-power operation from a single 5-volt supply.

The memory is compatible with CMOS microprocessors that share address and data lines. Compatibility is enhanced by pins 13, 14, 16, and 17 which give the user the versatility of selecting the active levels of each. Pin 17 allows the user to choose active high, active low or a third option of programming which is termed the "MOTEL" mode. If this mode is selected by the user, it provides direct compatibility with the CDP6805E2 type microprocessor series. In the MOTEL operation the ROM can accept either polarity signal on the data strobe input as long as the signal toggles during the cycle. This unique operational feature makes the ROM an extremely versatile part.



TERMINAL ASSIGNMENT

- *2K x 8 CMOS ROM*
- *3 to 6 volt supply*
- *Access time*
  430 ns (5 V) CDP65516-43
  550 ns (5 V) CDP65516-55
- *Low power dissipation*
  15 mA maximum(active)
  30 μA maximum (standby)
- *Directly compatible with muxed bus CMOS microprocessors*
- *Pins 13, 14, 16, and 17 are mask programmable*
- *MOTEL mask option also insures direct compatibility with many NMOS microprocessors*
- *Standard 18-pin package*

Objective Data

CDP1881, C
CDP1882, C

CMOS 6-Bit Latch and Decoder Memory Interfaces

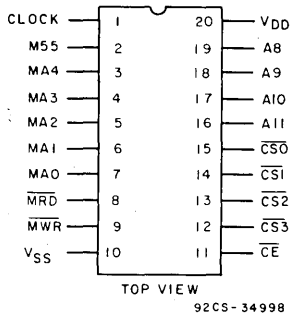
The RCA-CDP1881 and CDP1882 are CMOS 6-bit memory latch and decoder circuits intended for use in CDP1800 series microprocessor systems. They can interface directly with the multiplexed address bus of this system at maximum clock frequency, and up to four 4K x 8-bit random-access memories to provide a 16K-byte RAM system. With four 2K x 8-bit RAMs, an 8K-byte RAM system can be decoded.

The devices are also compatible with non-multiplexed address bus microprocessors. By connecting the clock input to V_{DD}, the latches are in the data-following mode and the decoded outputs can be used in general-purpose memory-system applications.

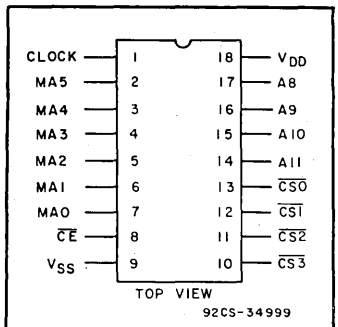
The CDP1881 and CDP1882 are intended for use with 2K or 4K-byte RAMs and are identical except that in the CDP1882 MWR and MRD are excluded.

The CDP1881 and CDP1882 are functionally identical to the CDP1881C and the CDP1882C. They differ in that the CDP1881 and CDP1882 have a recommended operating voltage range of 4 to 10.5 volts and their C versions have a recommended operating voltage range of 4 to 6.5 volts.

The CDP1881 and CDP1882 are supplied in 20-lead and 18-lead packages, respectively. Both the CDP1881 and CDP1882 are available in hermetic, dual-in-line side-brazed ceramic (D suffix) and plastic (E suffix) packages.



CDP1881
Terminal Assignment



CDP1882
Terminal Assignment

Features

- *Performs memory address latch and decoder functions multiplexed or non-multiplexed*
- *Interfaces directly with the CDP1800-series microprocessors*
- *Can replace existing CDP1866 and CDP1867 (upward speed and function capability)*
- *Allows decoding for systems larger than 16K*

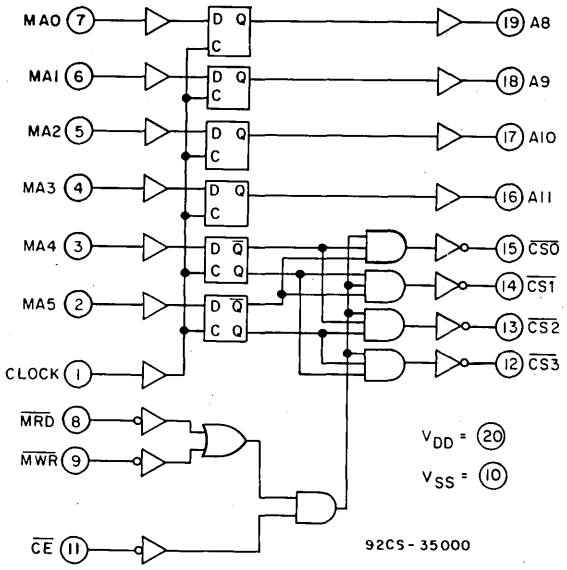


Fig. 1 - Functional diagram for the CDP1881.

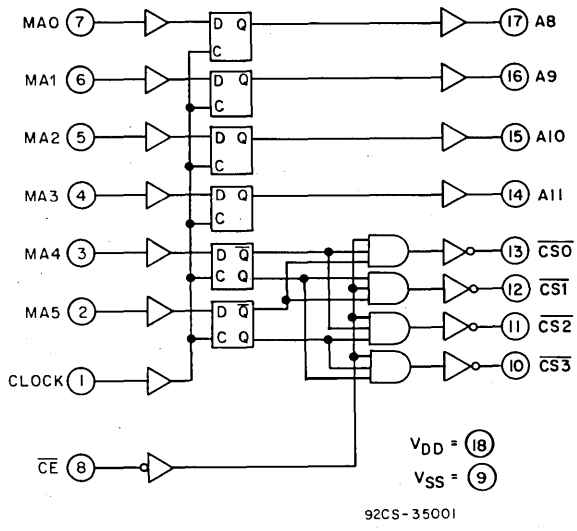


Fig. 2 - Functional diagram for the CDP1882.

RCA RAM Cross Reference Guide
16K RAMS

RCA 2048 x 8 CMOS Static RAMS (a)

RCA Type (b)	Operating Supply Voltage Range	Electrical Charact. Temperature Range	Address Access Time Max. (ns)	Max Chip Select Access Time (ns)	Standby Current Max		Max. Data Retention Current, 2V (μA)	Operating Supply Current, Max. (mA) (C)
					IDDS (mA)	IDDS1 (μA)		
CDM6116-1	4.5-5.5V	0° to +70°C	250	250	2	100	50	35
CDM6116-2	4.5-5.5V	0° to +70°C	200	200	2	30	15	35

NOTES:
a. Specifications at V_{DD} = 5 V, unless otherwise noted.
b. D suffix added for ceramic package, E suffix for plastic package.
c. Outputs open circuited.
d. Standby current test conditions.
   1.) I_{DDS1} at CMOS level inputs.
   2.) I_{DDS} at TTL level inputs.
e. These devices can be directly replaced by the RCA equivalent.

RCA 2048 x 8 CMOS Static RAM Comparison Chart (a)

Manufacturer		Type	Access Time Max. (ns)	Max. Standby Current (d)		Operating Current Max. (mA)	Electrical Charact. Temperature Range	Nearest RCA Equivalent
				IDDS (mA)	IDDS1 (uA)			
Fujitsu	(e)	MB8416	200	2	10	60	0° to + 70°C	CDM6116-2
Hitachi		HM6116P2	120	15	2000	80	0° to + 70°C	CDM6116-2
		HM6116P3	150	15	2000	70	0° to + 70°C	CDM6116-2
	(e)	HM6116P4	200	15	2000	70	0° to + 70°C	CDM6116-2
		HM6116LP2	120	12	100	70	0° to + 70°C	CDM6116-2
		HM6116LP3	150	12	100	60	0° to + 70°C	CDM6116-2
	(e)	HM6116LP4	200	12	100	60	0° to + 70°C	CDM6116-2
Harris		HM6516-2	250	N.A.	1000	10	-55 to +125°C	CDM6116-1
		HM6516-9	250	N.A.	1000	10	-40 to + 85°C	CDM6116-1
		HM65161	55/70/90	N.A.	100	65	N.A.	CDM6116-2
IDT		IDT6116S-70	70	15	2000	100	0° to + 70°C	CDM6116-2
		IDT6116S-90	90	15	2000	80	0° to + 70°C	CDM6116-2
		IDT6116S-120	120	15	2000	80	0° to + 70°C	CDM6116-2
		IDT6116LS-90	90	12	100	80	0° to + 70°C	CDM6116-2
		IDT6116LS-120	120	12	100	70	0° to + 70°C	CDM6116-2
		IDT6116LS-150	150	12	100	60	0° to + 70°C	CDM6116-2
NEC		uPD446	450	N. A.	10	18	-40° to + 85°C	CDM6116-1/2
		uPD446-1	250	N. A.	10	26	-40° to + 85°C	CDM6116-1/2
	(e)	uPD446-2	200	N. A.	10	30	-40° to + 85°C	CDM6116-2
		uPD446-3	150	N. A.	10	38	-40° to + 85°C	CDM6116-2
OKI		MSM5128-12	120	7	50	60	-30 to + 85°C	CDM6116-2
		MSM5128-15	150	7	50	55	-30 to + 85°C	CDM6116-2
	(e)	MSM5128-20	200	7	50	50	-30 to + 85°C	CDM6116-2
Toshiba	(e)	TC5517AP	250	3	30	70	-30 to + 85°C	CDM6116-1/2
		TC5517APL	250	3	1 @ 60°C	70	-30 to + 85°C	CDM6116-2

Type Nomenclature

CDP Series (CDP1800-Series Parts)

In general, the CDP series has pinouts with functions specifically designed to interface directly with an 1800-series CPU. These parts have an operating temperature range of -40°C to +85°C.

Suffix	Description
CD	4-6.5V, ceramic package
CE	4-6.5V, plastic package
D	4-10.5V, ceramic package
E	4-10.5V, plastic package
CH*	4-6.5V, chips
CW*	4-6.5V, chips in wafer form

MWS-Series (Industry standard parts)

The MWS-series generally has standard pinouts with functions equivalent to other CMOS or NMOS devices. These parts have an operating temperature range of 0°C to 70°C.

Suffix	Description
D,DL	4-6.5V, ceramic package
E,EL	4-6.5V, plastic package
H*	4-6.5V, chips
W*	4-6.5V, chips in wafer form

CD Series (General-Purpose Memories)

Suffix	Description
D	Ceramic package
E	Plastic package
F	Ceramic(frit) package
H*	Chips
W*	Chips in wafer form

*In the U.S., designated distributors handle chip orders. Contact your nearest RCA sales office for name and location.

Mask-Programmable ROM's

All RCA mask-programmable ROM's are custom ordered devices. ROM program patterns should be submitted to RCA in accordance with the procedure for ordering custom ROM's. Contact your nearest RCA sales office for details.

- A nonrecurring mask change is included to cover the expense of fabricating the tooling that is specific to each ROM pattern.
- All custom ROM's are supplied in either plastic or ceramic packages with the package suffix designations as specified earlier in the discussion of CDP-series nomenclature.

Cross-Reference Guide

Manufacturer/Type	Description	RCA Nearest Equiv. Type	Pin-for-Pin Compatible
AMI			
S5614	1K x 4 RAM	MWS5114	Yes
S5101	256 x 4 RAM	CDP1822/ MWS5101	Yes
S6508	1K x 1 RAM	CDP1821	Yes
FUJITSU			
MB8414E	1K x 4 RAM	MWS5114	Yes
HARRIS			
6402	UART	CDP6402	Yes
HM6551	256 x 4 RAM	CDP1822/ MWS5101	Yes
HM6508	1K x 1 RAM	CDP1821	Yes
HM6514	1K x 4 RAM	MWS5114	Yes
HITACHI			
HM435101	256 x 4 RAM	CDP1822/ MWS5101	Yes
HM4334	1K x 4 RAM	MWS5114	Yes
HUGHES			
HCMP1802	CPU	CDP1802	Yes
HCMP1822	256 x 4 RAM	CDP1822/ MWS5101	Yes
HCMP1824	32 x 8 RAM	CDP1824	Yes
HCMP1831	512 x 8 ROM	CDP1831	Yes
HCMP1832	512 x 8 ROM	CDP1832	Yes
HCMP1833	1K x 8 ROM	CDP1833	Yes
HCMP1834	1K x 8 ROM	CDP1834	Yes
HCMP1835	2K x 8 ROM	CDP1835	Yes
HCMP1851	I/O Interface	CDP1851	Yes
HCMP1852	I/O/Port	CDP1852	Yes
HCMP1853	N-Bit Decoder	CDP1853	Yes
HCMP1854	UART	CDP1854	Yes
HCMP1855	8-Bit MDU	CDP1855	Yes
HCMP1856/ 1857	Bus Buffer	CDP1856/ CDP1857	Yes
HCMP1858/ 1859	Latch/Decoder	CDP1858/ CDP1859	Yes
HCMP1861	VDC	CDP1861	Yes
HCMP1871	Keyboard Encoder	CDP1871	Yes

Manufacturer/Type	Description	RCA Nearest Equiv. Type	Pin-for-Pin Compatible
INTERSIL			
IM6402	UART	CDP6402	Yes
IM6551	256 x 4 RAM	CDP1822/ MWS5101	Yes
IM6514C	1K x 4 RAM	MWS5114	Yes
IM6316	2K x 8 ROM	CDP1835	No
MITEL			
MD74SC138A	Decoder	CDP1873C	Yes
MD74SC373A	I/O Port	CDP1872C/ CDP1874C	No
MOTOROLA			
MCM6508	1K x 1 RAM	CDP1821	Yes
MCM5101	256 x 4 RAM	CDP1822/ MWS5101	Yes
MCM65114	1K x 4 RAM	MWS5114	Yes
NATIONAL			
MM74C920	256 x 4 RAM	CDP1822/ MWS5101	No
MM74C929	1K x 1 RAM	CDP1821	Yes
NEC			
PD5101	256 x 4 RAM	CDP1822/ MWS5101	Yes
PD444/6514	1K x 4 RAM	MWS5114	Yes
OKI			
MSM5114	1K x 4 RAM	MWS5114	Yes
SSS			
SCM5101	256 x 4 RAM	CDP1822/ MWS5101	Yes
SCM5114	1K x 4 RAM	MWS5114	Yes
SCM5316	2K x 8 ROM	CDP1835	No
SUPERTEX			
CM1600	2K x 8 ROM	CDP1835	No
TOSHIBA			
TC5514P	1K x 4 RAM	MWS5114	Yes
TC5501P	256 x 4 RAM	CDP1822/ MWS5101	Yes
TC5508P	1K x 1 RAM	CDP1821	No
TC5507AP	1K x 4 RAM	MWS5114	No

5213/5213H
E^2
16K Electrically Erasable ROM

PRELIMINARY DATA SHEET September 1982

Features

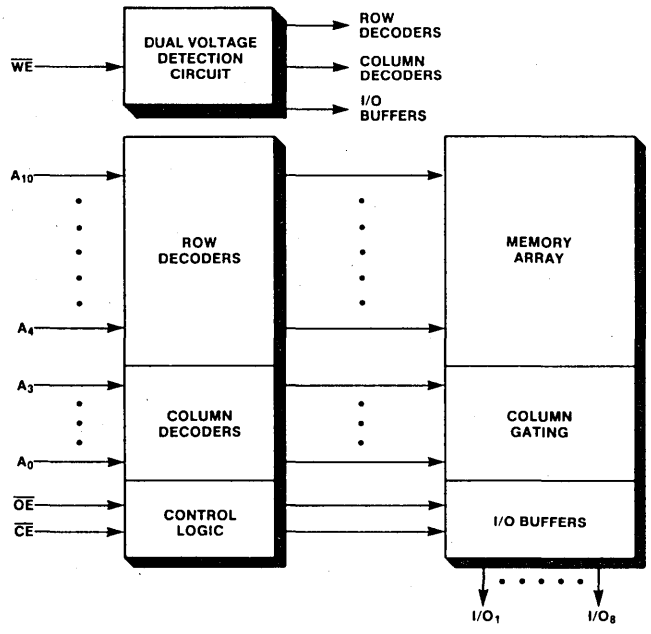
- *5V ±10% 2K x 8 E^2ROM*
- *2816 E^2ROM Compatibility*
- *TTL Byte Erase/Byte Write*
- *1 ms (5213H) or 9 ms Byte Erase/Byte Write*
- *10,000 Erase/Write Cycles per Byte*
- *Chip Erase*
- *Silicon Signature™ and DiTrace™*
- *Fast Read Access Time —250 ns*
- *Infinite Number of Read Cycles*
- *JEDEC Approved 24 Pin Dual-In-Line Pinout*

Description

SEEQ's 5213 is a 2048 x 8 bit 5 volt electrically erasable read only memory (E^2ROM). Data is electrically written by either a TTL pulse or a voltage between 15V and 22V on the Write Enable pin. Once written, which requires under 10 ms, there is no limit to the number of times data may be read. Both byte and chip erase modes are available. The erasure time in either mode is under 10 ms, and each byte may be erased and written 10,000 times. The 5213H has all the features of the 5213 but is enhanced with a fast 1 ms TTL byte erase/byte write time and 5V-only operation.

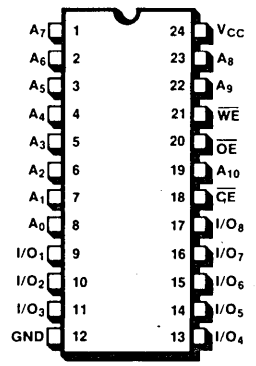
The 5213 and 5213H are ideal for applications that require a non-volatile memory with in-system write and erase capability. Dynamic reconfiguration (the alteration of operating software in real-time) is made possible by these devices. Applications for them will be found in military avionics systems, programmable character generators, self-calibrating instruments/machines, programmable industrial controllers, and an assortment of other systems. Designing the 5213 into eight and sixteen bit microprocessor systems is also simplified by utilizing the fast access time with zero wait states. Extended temperature and military grade versions are available.

Block Diagram



Pin Configuration

5213/5213H



Pin Names

A_0-A_{10}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$ (V_{PP})	WRITE ENABLE
I/O	DATA INPUT (WRITE OR ERASE) DATA OUTPUT (READ)

SEEQ Technology, Incorporated 1849 Fortune Drive, San Jose, California 95131 • (408) 942-1990

SEEQ Technology

MEMORY

Device Operation

SEEQ's 5213 has six modes of operation (see Table 1) and except for the chip erase mode it requires only TTL inputs to operate these modes. The device is 100% backward compatible to the 2816 except for the V_{OE} ($\overline{OE}$ Chip Erase Voltage) minimum specification.

To write a particular location of the 5213, that byte must first be erased. A memory location is erased by enabling the 5213 with Chip Enable at a TTL low, bringing Write Enable to a TTL low while Output Enable is a TTL high, and TTL highs (logical 1's) are being presented to all the I/O lines. The erase operation requires 9 ms for the 5213 and only 1 ms for the 5213H. A write operation is the same as an erase except true data is presented to the I/O lines.

The 5213 is compatible to prior generation E²ROMs which required a high voltage V_{PP} for writing and erasing. In the 5213 there is an internal dual level detection circuit which allows either a TTL low or 21V V_{PP} to be applied to $\overline{WE}$ to execute an erase or write operation. The 5213 specifies no restriction on the rising edge of V_{PP}. The 5213H may only be written or erased with a TTL low applied to Write Enable.

For certain applications, the user may wish to erase the entire memory. A chip erase is performed in the same manner as a byte erase except that Output Enable is between 14V and 22V. All 2K bytes are erased in 9 ms using either the 5213 or the 5213H.

A characteristic of all E²ROMs is that the total number of write and erase cycles is not unlimited. The 5213 has been designed for applications requiring up to 10,000 write and erase cycles per byte. The write and erase cycling characteristic is completely byte independent. Adjacent bytes are not affected during write/erase cycling.

After the device is written, data is read by applying a TTL high to $\overline{WE}$, enabling the chip, and enabling the outputs. Data is available t_{CE} time after Chip Enable is applied or t_{ACC} time from the addresses. System power may be reduced by placing the 5213/5213H into a standby mode. Raising Chip Enable to a TTL high will reduce the active power by over 60%.

SEEQ's 5213 and 5213H are the industry's first devices to incorporate Silicon Signature™ and DiTrace™ fields. The Silicon Signature™ feature is a JEDEC committee-approved method for storing device and programming information on-chip in an extra row of ROM cells. Included in the user-accessible Silicon Signature™ field are the major mask revision of the chip as well as its wafer fabrication location. The DiTrace™ feature is a method for storing production flow information to the wafer level in an extra column of E²ROM cells. As each major manufacturing operation is performed the DiTrace™ field is automatically updated to reflect that process step. These features ensure that shipped product conforms to specifications. Contact SEEQ for additional information on these features.

Table 1. Mode Selection (V_{CC} = 5V ± 10%)

Mode \ PIN	$\overline{CE}$ (18)	$\overline{OE}$ (20)	$\overline{WE}$ (V_{PP}) (21)	I/O (9-11, 13-17)
Read[1]	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Standby[1]	V_{IH}	Don't Care	V_{IH}	High Z
Byte Erase[2]	V_{IL}	V_{IH}	V_{IL}	$D_{IN} = V_{IH}$
Byte Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Chip Erase[2]	V_{IL}	V_{OE}	V_{IL}	$D_{IN} = V_{IH}$
Write/Erase Inhibit	V_{IH}	Don't Care	Don't Care	High Z

Notes:
1. $\overline{WE}$ may be from V_{IH} to 6V in the read and standby mode.
2. $\overline{WE}$ may be at V_{IL} (TTL W/E Mode) or from 15V to 22V (High Voltage W/E Mode) in the byte erase, byte write, or chip erase mode of the 5213.

5213/5213H Specification Differences

Except for the functional differences noted here, the 5213 and 5213H operate to the same specifications, including the TTL W/E mode.

Symbol	Function/Parameter	5213		5213H		Units
		Min.	Max.	Min.	Max.	
t_{WP}	Write Enable Pulse Width					
	Byte Write/Erase	9	70	1	10	ms
	Chip Erase	9	70	9	20	ms
V_{WE}	$\overline{WE}$ Write/Erase Voltage High Voltage Mode	15	22	Not Applicable		V

Power Up/Down Considerations

Care must be taken to prevent an unintentional write (or erase) cycle during power-up or power-down. These cycles can be prevented by applying a signal level of V_{IH} to $\overline{WE}$ (pin 21) whenever V_{CC} is greater than 2.75 volts. When V_{CC} is 2.75 volts or less, the device cannot perform a write (or erase) cycle.

Figure 1 shows a suggested circuit which can be used for power-up or power-down conditions. The power supply used for the 470 ohm pull-up resistor should be the same supply used for the 5213 V_{CC}. When this V_{CC} is outside the normal operating range (4.5 to 5.5 volts), the system power status signal (shown in Figure 1) should be low. Under these conditions, the open collector NAND gate and the 470 ohm resistor protect against an unintentional write (or erase).

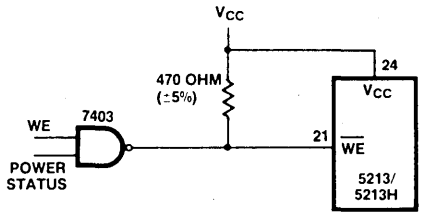


Figure 1.

*Absolute Maximum Stress Ratings**

Temperature
Storage ..... -65° C to +100° C
Under Bias ..... -10° C to +80° C
All Inputs or Outputs with
Respect to Ground ..... +6V to -0.3V
$\overline{WE}$ During Writing/Erasing
with Respect to Ground ..... +22.5V to -0.3V
Duration of $\overline{WE}$ Supply at
22V During W/E Inhibit ..... 24 Hours

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

	Read Mode	Write or Erase Mode
V_{CC} Supply Voltage	5V ± 10%	5V ± 10%
Temperature Range	0 to 70° C	0 to 70° C

5213/5213H D.C. Operating Characteristics During Read or Write/Erase

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{IN}	Input Leakage Current			10	μA	$V_{IN} = V_{CC}$ Max.
I_O	Output Leakage Current			10	μA	$V_{OUT} = V_{CC}$ Max.
I_{WE}	Write Enable Leakage Read Mode		1.0	1.5	mA	$\overline{WE} = V_{IH}$
	TTL W/E Mode			-1.0	mA	$\overline{WE} = V_{IL}$
	High Voltage W/E Mode[2]			1.5	mA	$\overline{WE}$ = 22V, $\overline{CE} = V_{IL}$
	High Voltage W/E Inhibit Mode[2]			1.5	mA	$\overline{WE}$ = 22V, $\overline{CE} = V_{IH}$
	Chip Erase — TTL Mode			-1.0	mA	$\overline{WE} = V_{IL}$
	Chip Erase — High Voltage Mode[2]			1.5	mA	$\overline{WE}$ = 22V
I_{CC1}	V_{CC} Standby Current		15	30	mA	$\overline{CE} = V_{IH}$
I_{CC2}	V_{CC} Active Current		50	80	mA	$\overline{CE} = \overline{OE} = V_{IL}$
V_{IL} (D.C.)	Input Low Voltage (D.C.)	-0.1		0.8	V	
V_{IL} (A.C.)	Input Low Voltage (A.C.)	-0.4			V	Time = 10 ns
V_{IH}	Input High Voltage	2		V_{CC} + 1	V	
V_{WE}	$\overline{WE}$ Read Voltage	2		V_{CC} + 1	V	
	$\overline{WE}$ Write/Erase Voltage TTL Mode	-0.1		0.8	V	
	High Voltage Mode[2]	15	21	22	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -400 μA
V_{OE}	$\overline{OE}$ Chip Erase Voltage	14		22	V	I_{OE} = 10 μA

Notes:
1. Typical values are for T_A = 25° C and nominal supply voltages.
2. Not applicable to 5213H.

A.C. Operating Characteristics During Read

Symbol	Parameter	5213-350 Limits			5213H-350 Limits			Unit	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{ACC}	Address to Data Valid		300	350		300	350	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	Chip Enable to Data Valid		300	350		300	350	ns	$\overline{OE} = V_{IL}$
t_{OE}[1]	Output Enable to Data Valid	10	50	100	10	50	100	ns	$\overline{CE} = V_{IL}$
t_{DF}[2]	Output Enable to High Impedance	0	50	80	0	50	80	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Address, Chip Enable, or Output Enable, whichever Transition Occurred First	0			0			ns	$\overline{CE} = \overline{OE} = V_{IL}$

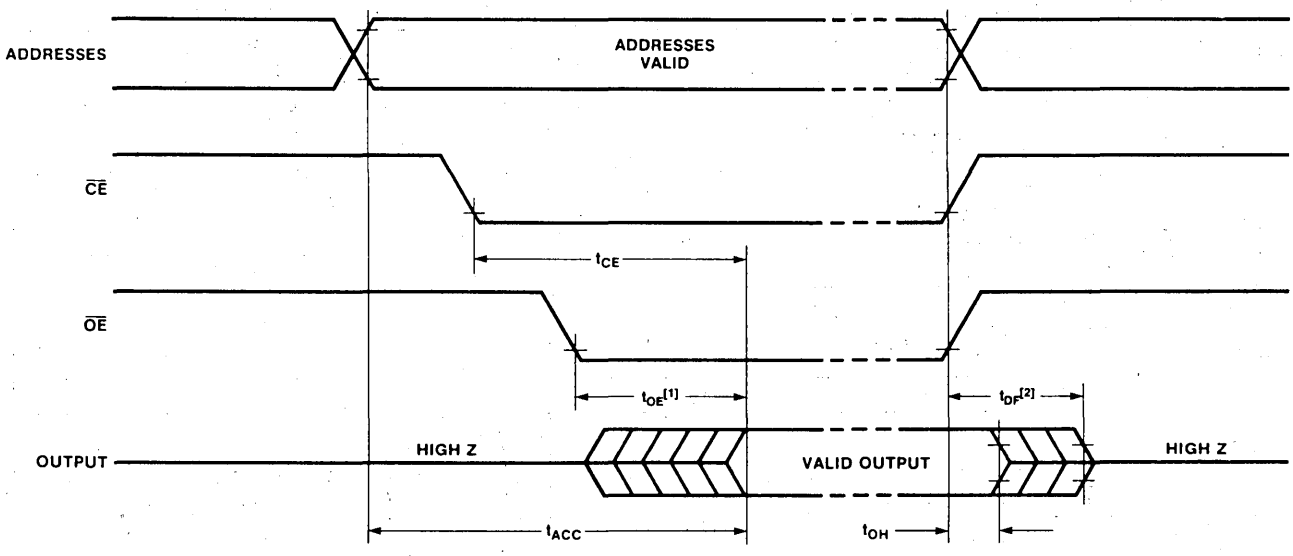
Capacitance[3] $T_A = 25°C$, f = 1MHz

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	5	10	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance		10	pF	$V_{OUT} = 0V$
$C_{V_{CC}}$	V_{CC} Capacitance		500	pF	$\overline{OE} = \overline{CE} = V_{IH}$
$C_{V_{WE}}$	V_{WE} Capacitance		10	pF	$\overline{OE} = \overline{CE} = V_{IH}$

A.C. Test Conditions

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤ 20ns
Input Pulse Levels: 0.45V to 2.4V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

Read Timing



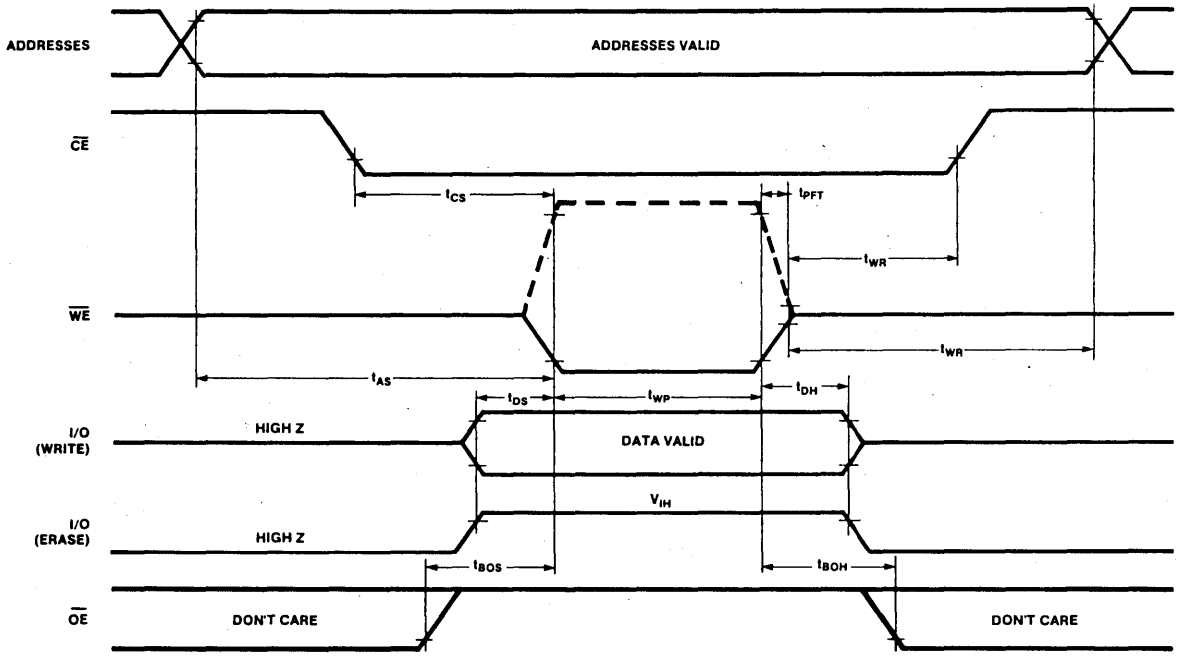
Notes:
1. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
3. This parameter is periodically sampled.

5213/5213H A.C. Operating Characteristics During Write/Erase

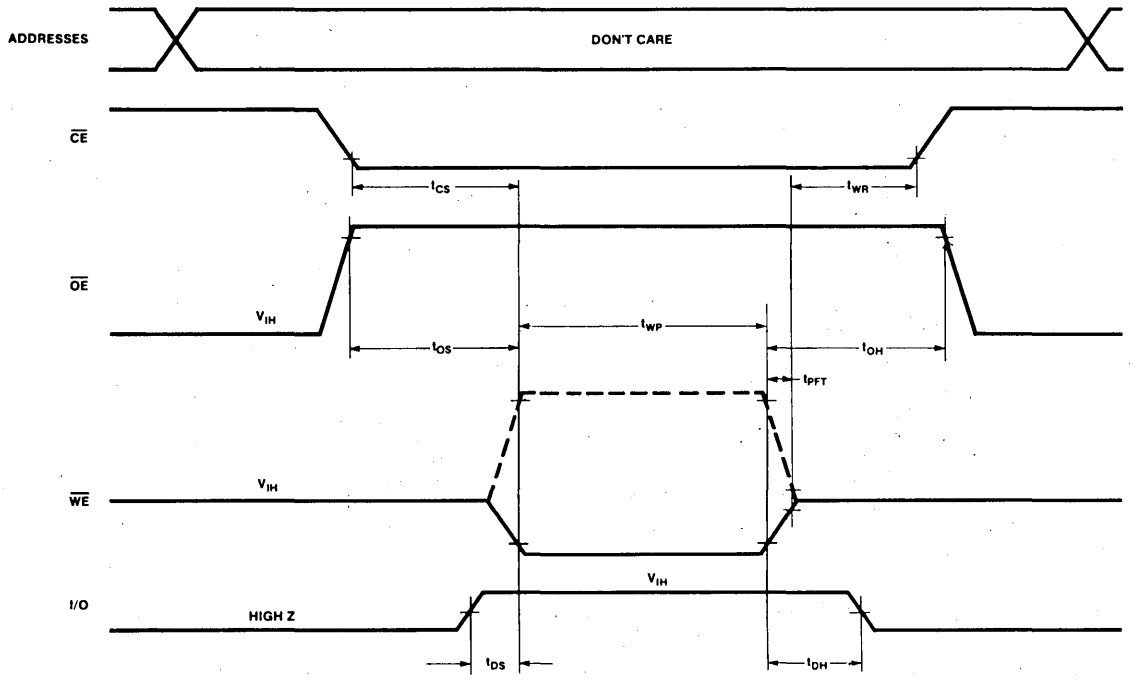
Symbol	Parameter	Limits			Units
		Min.	Typ.	Max.	
Q	Maximum W/E Cycles per Byte			10,000	cycles
t_{AS}	Address to $\overline{WE}$ Set-Up Time	150			ns
t_{CS}	$\overline{CE}$ to $\overline{WE}$ Set-Up Time	150			ns
t_{DS}	Data to $\overline{WE}$ Set-Up Time	0			ns
t_{DH}	Data Hold Time	50			ns
t_{WP}[1]	Write Enable Pulse Width	9		70	ms
t_{WR}[2]	Write Recovery Time	50			ns
t_{OS}	$\overline{OE}$ Set-Up Time (Chip Erase)	0			ns
t_{OH}	$\overline{OE}$ Hold Time (Chip Erase)	0			ns
t_{BOS}	Byte Write/Erase Set-Up Time	0			ns
t_{BOH}	Byte Write/Erase Hold Time	0			ns
t_{PFT}[3]	V_{WE} Fall Time	5			μs

Notes:
1. t_{WP} (min) = 1 ms and t_{WP} (max) = 10 ms for the 5213H in the byte erase and byte write mode. t_{WP} (min) = 9 ms and t_{WP} (max) = 20 ms for the 5213H in the chip erase mode.
2. t_{WR} (min) = 50 ns when in the High Voltage W/E Mode only. When in the TTL W/E Mode, t_{WR} (min) = 700 ns.
3. t_{PFT} applies only when in the High Voltage W/E Mode. t_{PRC} (V_{WE} RC Rise Time Constant) is not applicable to the 5213 or 5213H.

BYTE ERASE OR BYTE WRITE TIMING



CHIP ERASE TIMING



Ordering and Packaging Information

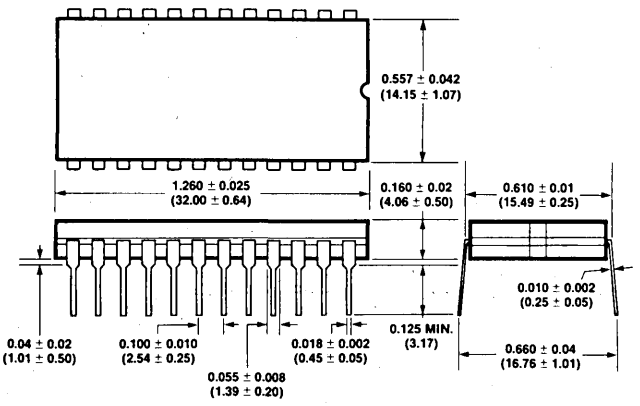
PART NUMBERS

DQ5213 -350

DQ5213H-350

- ACCESS TIME (ns)
- 1 ms WRITE TIME AND 5V ONLY
- PRODUCT: 2K x 8 E^2ROM
- TEMPERATURE RANGE: 0°C to 70°C
- PACKAGE: CERDIP

24-LEAD HERMETIC CERDIP
PACKAGE TYPE D



DIMENSIONS IN INCHES AND (MILLIMETERS).

M5213/E5213

E^2

16K Electrically Erasable ROM

PRELIMINARY DATA SHEET

September 1982

Features

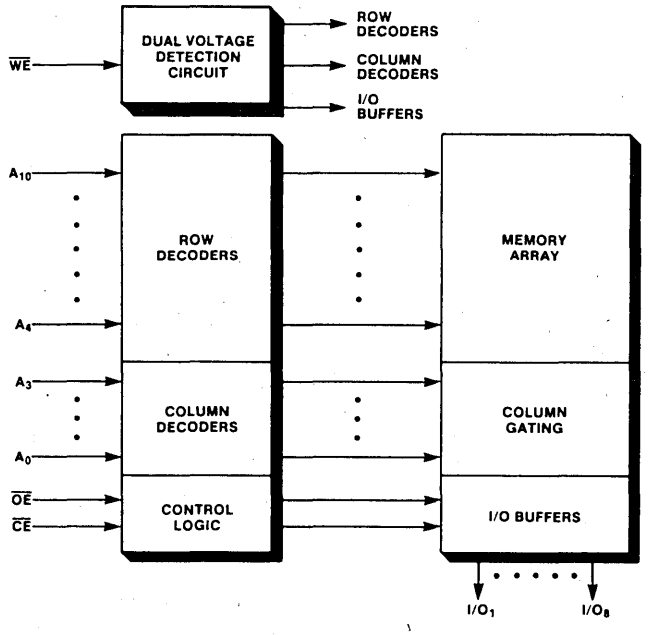
- **Full Military and Industrial Temperature Ranges**
  - **M5213 -55° C to +125° C, MIL-STD-883 Level B**
  - **E5213 -40° C to +85° C**
- **5V ±10% 2K x 8 E^2ROM**
- **2816 E^2ROM Compatibility**
- **9 ms TTL Byte Erase/Byte Write**
- **10,000 Erase/Write Cycles per Byte**
- **Low Power and High System Noise Immunity**
  - **V_{CC} Standby Current 35 mA Max.**
  - **V_{CC} Active Current 90 mA Max.**
  - **V_{IH} Range 2.0 to V_{CC} +1 Volts**
- **Chip Erase**
- **Silicon Signature™ and DiTrace™**
- **Infinite Number of Read Cycles**

Description

SEEQ's M5213 and E5213 are 2048 x 8 bit 5 volt electrically erasable read only memories (E^2ROM). The M5213 is specified over the full military operating range of -55° C to +125° C with MIL-STD-883 Level B screening. The E5213 is specified from -40° C to +85° C. Data is electrically written into both parts by either a TTL pulse or a voltage between 15V and 22V on the Write Enable pin. Once written, which requires 9 ms, there is no limit to the number of times data may be read. Both byte and chip erase modes are available. The erasure time in either mode is 9 ms, and each byte may be erased and written 10,000 times.

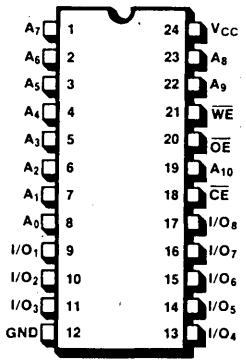
The 5213 family of devices is ideal for applications that require a non-volatile memory with in-system write and erase capability. Dynamic reconfiguration (the alteration of operating software in real-time) is made possible by this family of devices. Applications for the M5213 and E5213 will be found in military avionics systems, industrial robots, self-calibrating instruments/machines, programmable industrial controllers, and an assortment of other systems.

Block Diagram



Pin Configuration

M5213/E5213



Pin Names

A_0-A_{10}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$ V_{PP}	WRITE ENABLE
I/O	DATA INPUT WRITE OR ERASE DATA OUTPUT READ

5223
E^2
32K Electrically Erasable ROM

PRODUCT BRIEF *June 1982*

Features

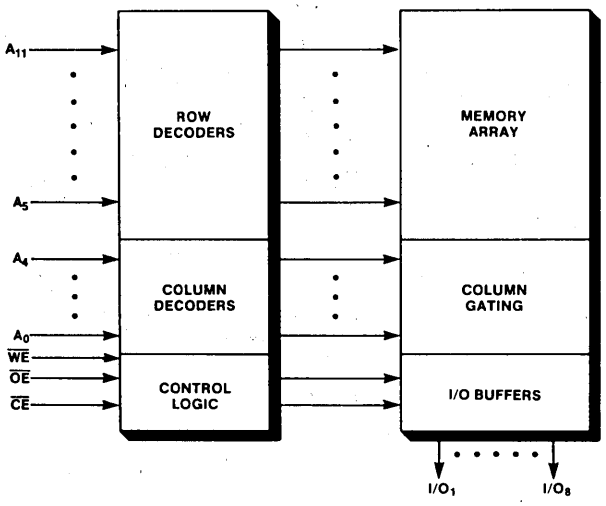
- **TTL Byte Erase/Byte Write**
- **10,000 Erase/Write Cycles per Byte**
- **5 Volt ± 10% Power Supply**
- **Chip Erase**
- **Silicon Signature**
- **Easy Upgrade from 5213 16K E^2ROM**
- **Fast Read Access Time < 250 ns**
- **Infinite Number of Read Cycles**
- **JEDEC Approved 28 Pin Dual-In-Line Pinout**

Description

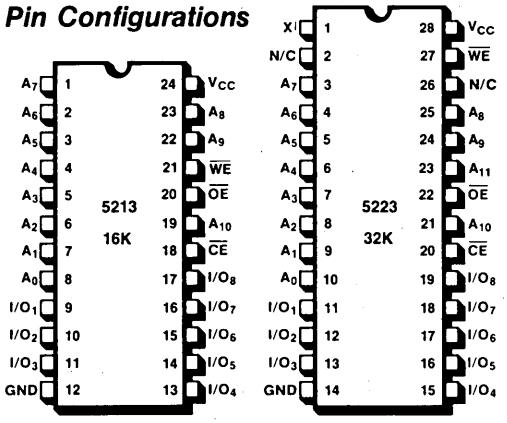
Seeq's 5223 is a 4096 x 8 bit 5 volt electrically erasable read only memory (E^2ROM). As pioneered by Seeq's 5213 2K x 8 bit E^2ROM, data is electrically written into the 5223 by a TTL-compatible Write Enable pulse. Once data is written, which requires only 5 ms, it may be read an unlimited number of times. Both byte and chip erase modes are available, and each byte may be erased and written up to 10,000 times. The erasure time in either mode is less than 10 ms.

The 5223 is ideal for applications that require a non-volatile memory with in-system write and erase capability. Its features make possible dynamic reconfiguration, that is the alteration of operating software in real time. Some uses for the 5223 are in programmable character generators, instrument/machine self-calibrators, and programmable industrial controllers. Designing the 5223 into eight and sixteen bit microprocessor systems is also simplified since the access time is less than 250 ns, allowing zero wait state operation. Extended temperature and military grade devices also will be offered.

Block Diagram



Pin Configurations



Pin Names

A_0-A_{11}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O	DATA INPUT (WRITE OR ERASE) DATA OUTPUT (READ)
N/C	NO CONNECT
X	TTL DON'T CARE OR OPEN

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5133
64K UV EPROM

PRELIMINARY DATA SHEET *October 1982*

Features

- ***JEDEC Approved 8K x 8 EPROM Pinout***
- ***Enhanced 2764 EPROM***
  - ***— 10 ms Typical Programming Time***
- ***Fast Access Time: 350 ns***
- ***Low Power***
  - ***— 70 mA typ. Active***
  - ***— 15 mA typ. Standby***
- ***Standard 28 Pin Dual-in-Line Package***
- ***Silicon Signature™***

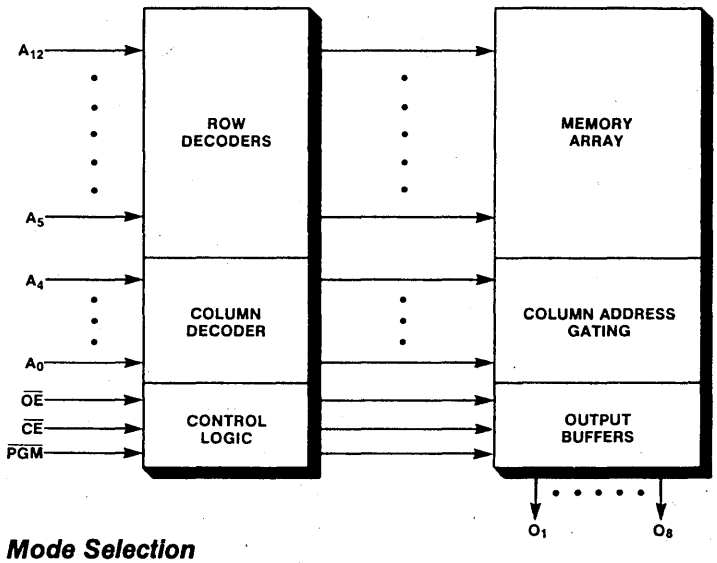
Description

Seeq's 5133 is a 5V only, 8K x 8 (65,536 bits) ultraviolet light erasable EPROM. It is manufactured using Seeq's n-channel floating gate EPROM technology which allows access times under 250 ns. This access time is performance compatible to popular eight and sixteen bit microprocessors. Its performance is achieved without sacrificing power since the 5133's active and standby currents are the lowest of the available 64K EPROMs.

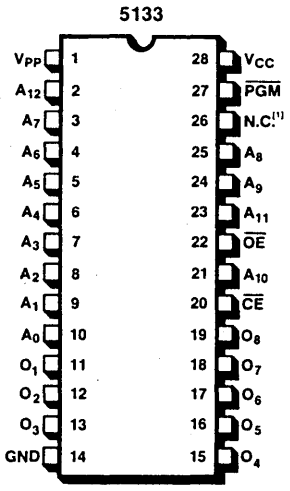
The 5133, being a 64K bit memory, allows 32K EPROM users to double their memory size requirement at half the power. An upgrade to the 5133 is simplified because the 5133's lower 24 pins are compatible to 32K (and 16K) EPROMs. Performance, reduced power/bit, and board density are features which the 5133 gives over lower density EPROMs.

Initially, and after erasure, all bits are in the "1" state. Data is programmed by applying 21V to V_{PP} and a TTL "0" level to $\overline{PGM}$. The programming time, at typically 10 ms, is 4 to 5 times faster than other 64K EPROMs.

Block Diagram



Pin Configuration



Mode Selection

MODE \ PINS	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11-13, 15-19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	X	V_{IL}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	X	X	V_{PP}	V_{CC}	High Z

X can be either V_{IL} or V_{IH}

Pin Names

A_0-A_{12}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS
$\overline{PGM}$	PROGRAM
N.C.	NO CONNECT

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Absolute Maximum Stress Ratings*

Temperature
Storage ..... -65° C to +125° C
Under Bias ..... -10° C to +80° C
All Inputs or Outputs with
Respect to Ground ..... +6V to -0.6V
V_{PP} During Programming with
Respect to Ground ..... +22V to -0.6V

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

	Read Mode	Programming Mode
V_{CC} Supply Voltage	5V ± 5%	5V ± 5%
Temperature Range	0 to 70° C	25 ± 5° C
V_{PP}	5V ± 5%	21V ± 0.5V

DC Operating Characteristics During Read or Programming

Symbol	Parameter		Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{IN}	Input Leakage Current				10	µA	$V_{IN} = V_{CC}$ Max.
I_O	Output Leakage Current				10	µA	$V_{OUT} = V_{CC}$ Max.
I_{PP}[2]	V_{PP} Current	Read Mode		0.8	2	mA	$V_{PP} = V_{CC}$ Max.
		Prog. Mode		25	30	mA	V_{PP} = 21.5V
I_{CC1}[2]	V_{CC} Standby Current			15	30	mA	$\overline{CE} = V_{IH}$
I_{CC2}[2]	V_{CC} Active Current			70	100	mA	$\overline{CE} = \overline{OE} = V_{IL}$
V_{IL}	Input Low Voltage		-0.1		0.8	V	
V_{IH}	Input High Voltage		2		V_{CC} + 1	V	
V_{OL}	Output Low Voltage				0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage		2.4			V	I_{OH} = -400 µA

NOTES:
1. Typical values are for T_A = 25° C and nominal supply voltage.
2. This parametric limit is now being characterized.

A.C. Operating Characteristics During Read

Symbol	Parameter	5133-350 Limits			5133-450 Limits			Unit	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{ACC}[1]	Address to Data Valid		250	350		350	450	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}[1]	Chip Enable to Data Valid		250	350		350	450	ns	$\overline{OE} = V_{IL}$
t_{OE}[1]	Output Enable to Data Valid		90	120		90	150	ns	$\overline{CE} = V_{IL}$
t_{DF}[1,4]	Output Enable to High Impedance		80	100	0	80	130	ns	$\overline{CE} = V_{IL}$
t_{OH}[1]	Output Hold from Addresses, Chip Enable, or Output Enable, whichever transition occurred first	0					0	ns	

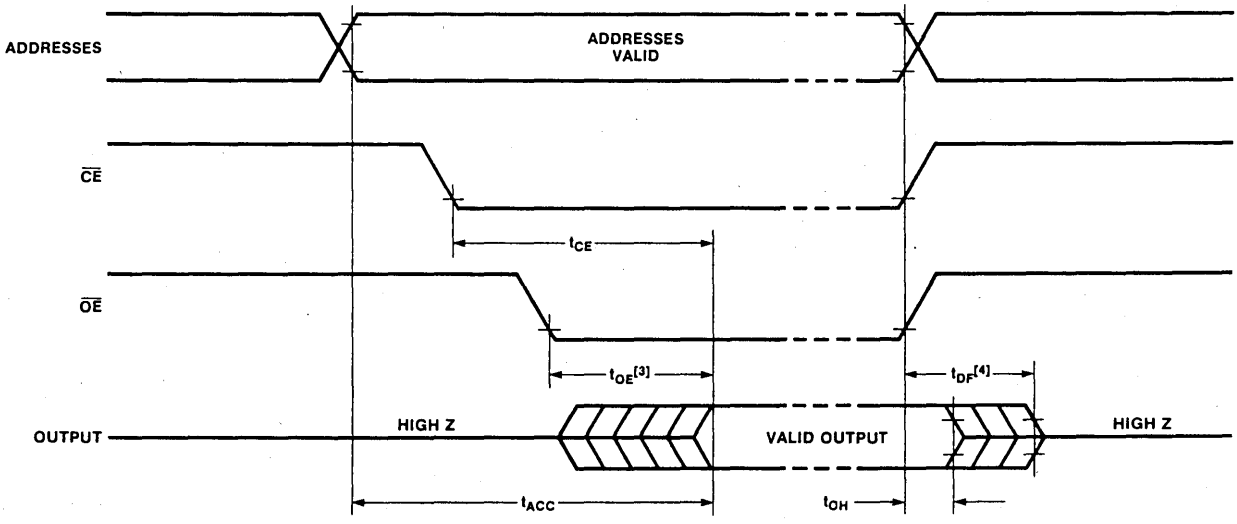
Capacitance[2] T_A = 25°C, f = 1MHz

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

A.C. Test Conditions

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤ 20ns
Input Pulse Levels: 0.45V to 2.4V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

A.C. Waveforms



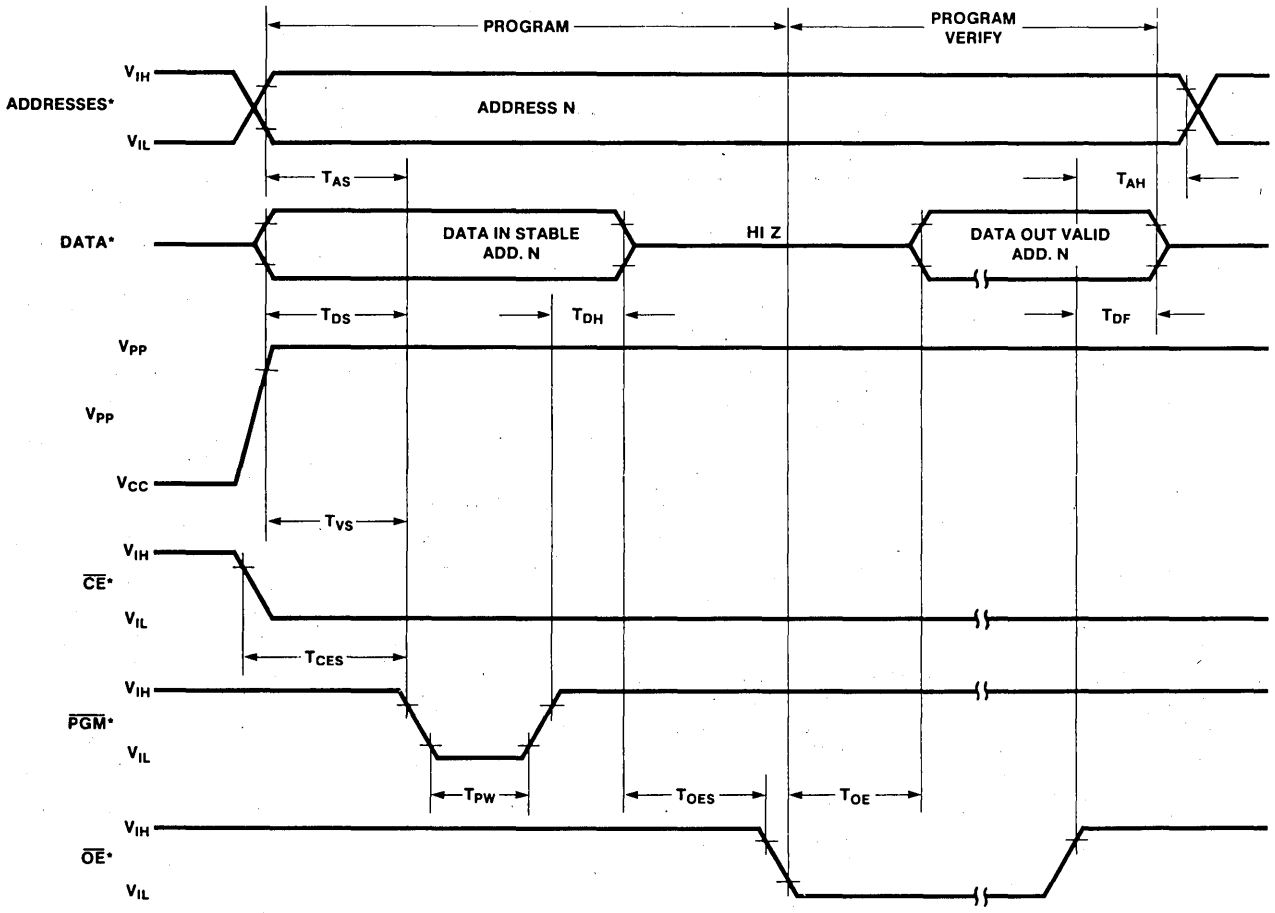
NOTES:
1. This parametric limit is now being characterized. The 5133 family will have maximum access times of 200ns to 450ns.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
4. t_{DF} is specified from OE or CE, whichever occurs first.

AC Programming Characteristics

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
t_{AS}	Address Setup Time	2			μs	
t_{OES}	$\overline{OE}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time From Output Enable	0			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DF}	Output Enable to High Impedance	0		100	ns	$\overline{CE}$ = V_{IL}
t_{VS}	V_{PP} Setup Time	2			μs	
t_{PW}	$\overline{PGM}$ Pulse Width During Programming	TBD[1]	10	55	ms	
t_{CES}	$\overline{CE}$ Setup Time	2			μs	
t_{OE}[1]	Output Enable to Data Valid		100	120	ns	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}

NOTE 1: This parametric limit is now being characterized.

Programming Waveforms



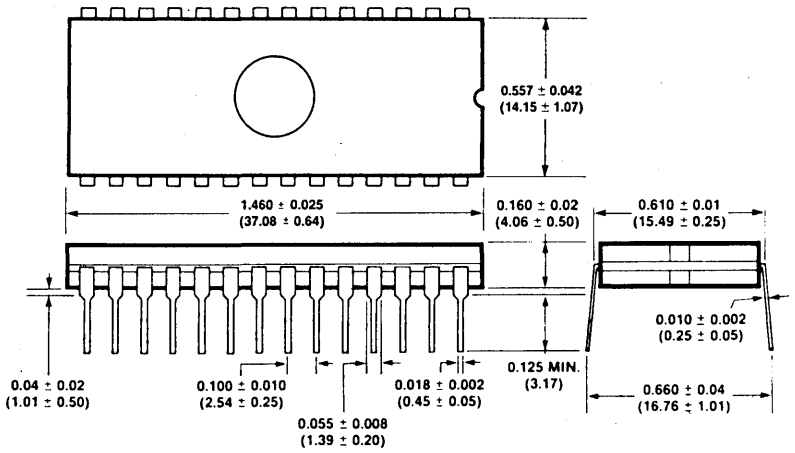
*THE INPUT TIMING REFERENCE LEVEL IS 1V FOR A V_{IL} AND 2V FOR A V_{IH}.

Ordering and Packaging Information

PART NUMBER D Q 5133 - 450 OR DQ5133-350

- 450 — ACCESS TIME (ns)
- 5133 — PRODUCT: 8K x 8 EPROM
- Q — TEMPERATURE RANGE: 0 to 70° C
- D — PACKAGE: CERDIP

28-LEAD HERMETIC CERDIP
PACKAGE TYPE D



DIMENSIONS IN INCHES AND (MILLIMETERS).

5143
128K UV EPROM

PRODUCT BRIEF *June 1982*

Features

- ***JEDEC Approved 16K x 8 EPROM Pinout***
  - ***Easy Upgrade from 8K x 8 EPROM***
- ***Fast Access Time: ≤ 250 ns***
- ***10 ms Maximum Programming Time***
- ***Low Power***
  - ***70 mA typ. Active***
  - ***15 mA typ. Standby***
- ***5 Volt ±10% Supply Operation***
- ***Silicon Signature***
- ***On-Chip Redundancy***
- ***Standard 28 Pin Dual-in-Line Package***

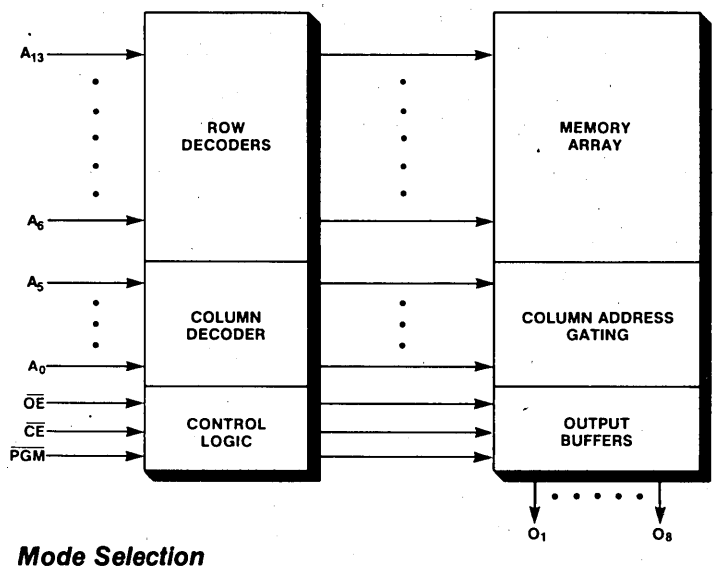
Description

Seeq's 5143 is a 5 volt only, 16,384 x 8 bit ultraviolet light erasable EPROM. It is manufactured using Seeq's n-channel floating gate EPROM technology which allows access times under 250 ns. This access time is performance compatible to popular eight and sixteen bit microprocessors, and it is achieved without sacrificing power. The 5143's active and standby currents are the lowest of the available 128K EPROMs.

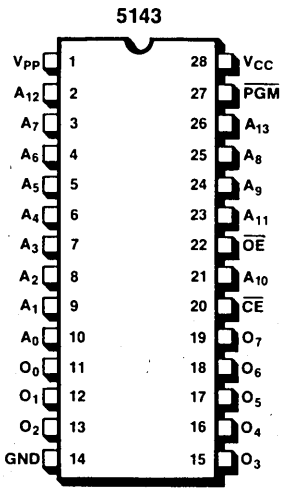
The 5143, being a 128K bit memory, allows 64K EPROM users to double their memory capacity with half the power per bit. Upgrading from Seeq's 5133 or other 64K EPROMs is accomplished by merely adding the 5143's extra address input A_{13} to unused pin 26. Greater board density and lower power per bit make the 5143 advantageous over lower density EPROMs.

Initially, and after erasure, all bits of the 5143 are in the "1" state. Data is programmed by applying 21V to V_{PP} and a TTL "0" level to $\overline{PGM}$. The 5143's fast programming time, at less than 10 ms per byte, minimizes the user's manufacturing cycle time.

Block Diagram



Pin Configuration



Mode Selection

MODE \ PINS	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11-13, 15-19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	X	V_{IL}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	X	X	V_{PP}	V_{CC}	High Z

X can be either V_{IL} or V_{IH}

Pin Names

A_0-A_{13}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS
$\overline{PGM}$	PROGRAM

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32,768-BIT STATIC MOS ROM (4096 x 8) 2332-20/25/30/45

DESCRIPTION

This ROM is designed for memory applications where high performance, large bit storage, and simple interfacing are important design objectives.

The two chip select inputs are programmable. Any combination of active high or low level chip select inputs can be defined by the designer and the desired chip select logic level is fixed during the masking processing. These two programmable chip select inputs, as well as OR-tie compatibility on the outputs, facilitates easy memory expansion.

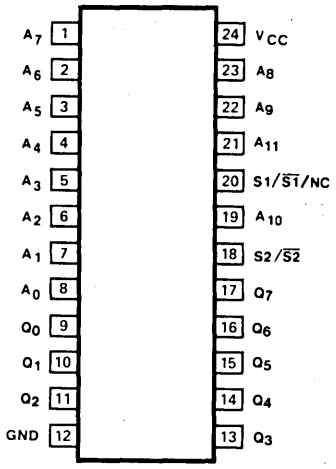
The 2332 Read Only Memory is fabricated with n-channel silicon gate technology. This technology provides the designer with high performance easy-to-use MOS circuits.

FEATURES

- **Fast access time**
  - **—200ns max. 2332-20**
  - **—250ns max. 2332-25**
  - **—300ns max. 2332-30**
  - **—450ns max. 2332-45**
- **Industry standard pinout—JEDEC approved**
- **Low power dissipation**
  - **—357mW max. for 2332-30/45**
  - **—412mW max. for 2332-20/25**
- **Completely TTL compatible**
- **Single +5V ±10% power supply**
- **3-state output—OR-tie capability**
- **Fully decoded—on chip address decode**
- **Inputs protected—all inputs have protection against static charge**
- **Two programmable chip select inputs for easy memory expansion or no connection option.**
- **2732 EPROM compatible**

PIN CONFIGURATION

F,I,N PACKAGE



(TOP VIEW)

PACKAGE AVAILABILITY

F = Cerdip I = Ceramic N = Plastic

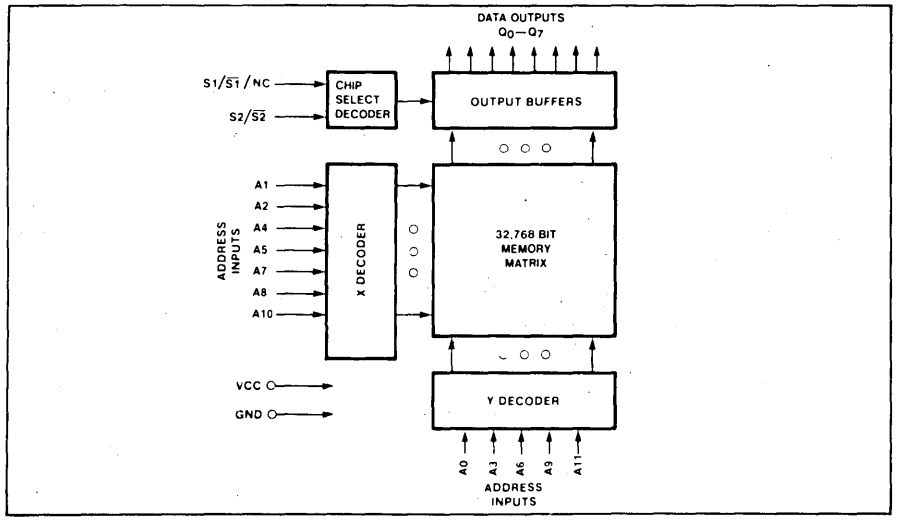
ABSOLUTE MAXIMUM RATINGS (See Note 1)

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_A	Operating	0 to +70	
T_{STG}	Storage	−65 to +150	
	Applied voltage		V
V_I	Input	−2.0 to +7	
V_O	Output	−2.0 to +7	
V_{CC}	Supply voltage to ground potential	−2.0 to +7	V

NOTE

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM



32,768-BIT STATIC MOS ROM (4096×8) 2332-20/25/30/45

DC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 10\%$, unless otherwise specified

PARAMETER		TEST CONDITIONS	2332-20		2332-25		2332-30		2332-45		UNIT
			Min	Max	Min	Max	Min	Max	Min	Max	
	Input voltage										V
V_{IL}	Low (See Note 2)		−2.0	0.8	−2.0	0.8	−2.0	0.8	−2.0	0.8	
V_{IH}	High		2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	
	Output voltage										V
V_{OL}	Low	$I_{OL} = 3.2mA$		.4		.4		.4		.4	
V_{OH}	High	$I_{OH} = -400\mu A$	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	
I_{LI}	Input load current	$0V \le V_{IN} \le 5.5V$		1		1		1		1	μA
I_{LO}	Output leakage	Chip deselected $V_{OUT} = +0.4V$ to V_{CC}		5		5		5		5	μA
I_{CC}	Supply current	Chip deselected $V_{CC} = 5.5V$, $V_{IN} = V_{CC}$		75		75		65		65	mA
	Capacitance (See Note 3)										pF
C_{IN}	Input	$T_A = 25°C$, f = 1MHz all pins except		7		7		7		7	
C_{OUT}	Output	pin under test tied to ground		10		10		10		10	

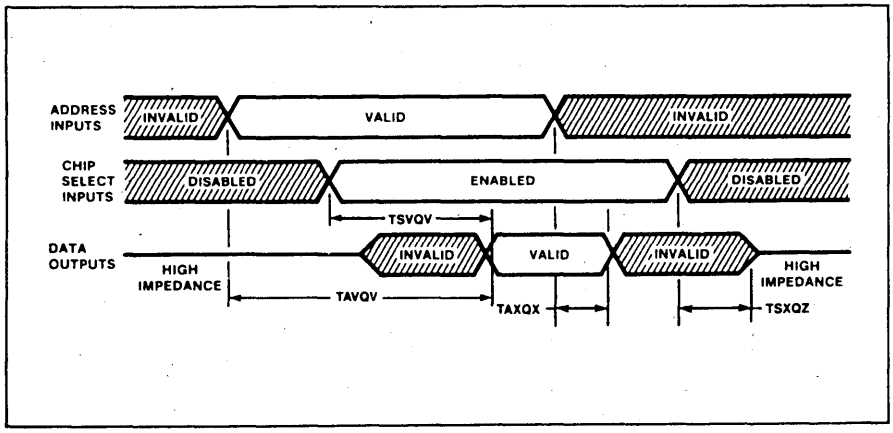
NOTES
2. Input levels that swing more negative than −2.0V may alter AC electrical characteristics.
3. This parameter is periodically sampled and is not 100% tested.

AC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 10\%$, Output load = 2 TTL loads and 100pF, Input transition time ≤ 10ns, Timing reference levels: Input = 1.5V, Output = 0.6V and 2.2V, 0.1μF ceramic capacitor between V_{CC} and GND pins, $V_{IL} \ge -2.0V$.

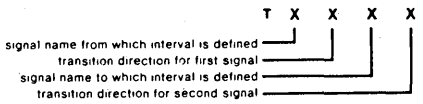
PARAMETER		2332-20		2332-25		2332-30		2332-45		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
T_{AVQV}	Address access time		200		250		300		450	ns
T_{SVQV} (See Note 4)	Chip select delay		100		120		120		150	ns
T_{SXQZ} (See Note 5)	Chip deselect delay		100		100		100		100	ns
T_{AXQX}	Previous data valid after address change delay	0		0		0		0		ns

NOTES
4. T_{SVQV} is at value indicated, provided the valid address leads the chip select by ($T_{AVQV} - T_{SVQV}$) nsec or more.
5. T_{SXQZ} is measured at $V_{OL} = 0.8V$ on the "0" to high Z state transition, with 2 TTL loads connected to the output.

TIMING DIAGRAM



TIMING PARAMETER ABBREVIATIONS



The transition definitions used in this data sheet are
- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedence)
- A = Address
- S = Chip Select
- Q = Output

Nomenclature is adopted from JEDEC JC-42 Committee on Semiconductor Memories Standard

65,536-BIT STATIC MOS ROM (8192×8) 2364-20/25/30/45

DESCRIPTION

This ROM is designed for memory applications where high performance, large bit storage, and simple interfacing are important design objectives.

The 4 chip select inputs are programmable. Active high or active low level chip select input can be defined by the designer and the desired chip select logic level is fixed during the masking process. The programmable chip select input, as well as OR-tie compatibility on the outputs, facilitates easy memory expansion.

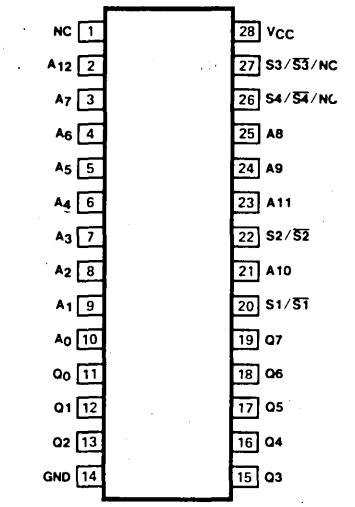
The 2364 Read Only Memory is fabricated with n-channel silicon gate technology. This technology provides the designer with high performance, easy-to-use MOS circuits.

FEATURES

- **Fast access time**
  - **—200ns max. 2364-20**
  - **—250ns max. 2634-25**
  - **—300ns max. 2364-30**
  - **—450ns max. 2364-45**
- **Industry standard pinout—JEDEC approved**
- **Low power dissipation**
  - **—440mW max. for 2364-30/45**
  - **—495mW max. for 2364-20/25**
- **Completely TTL compatible**
- **One +5V ± 10% power supply**
- **3-state output—OR-tie capability**
- **Fully decoded—on chip address decode**
- **Inputs protected—all inputs have protection against static charge**
- **Four programmable chip select inputs for easy memory expansion or no connection option**
- **2764 EPROM compatible**

PIN CONFIGURATION

F,I,N PACKAGE



TOP VIEW

PACKAGE AVAILABILITY

F = Cerdip I = Ceramic N = Plastic

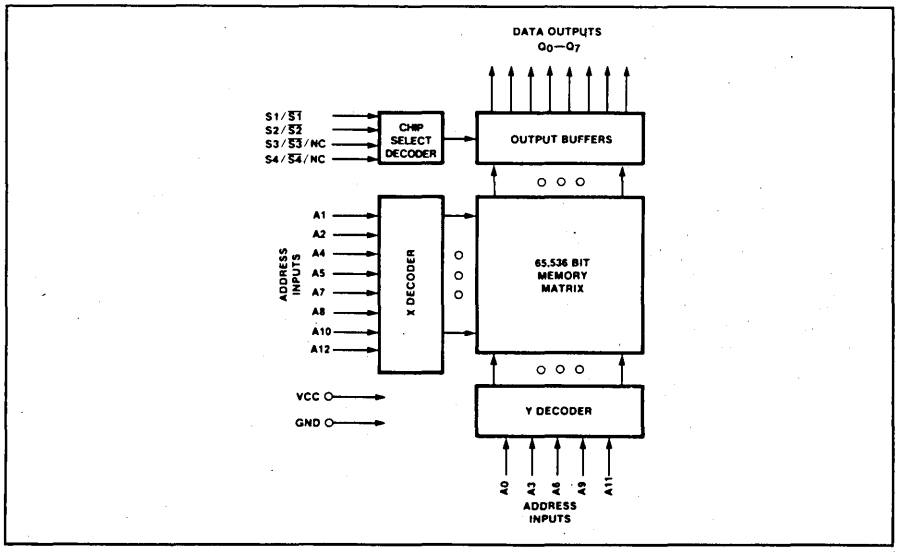
ABSOLUTE MAXIMUM RATINGS (See Note 1)

PARAMETER		RATING	UNIT
	Temperature range		°C
T_A	Operating	0 to +70	
T_{STG}	Storage	−65 to +150	
	Applied voltage		V
V_I	Input	−2.0 to +7	
V_O	Output	−2.0 to +7	
V_{CC}	Supply voltage to ground potential	−2.0 to +7	V

NOTE

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM



Signetics

65,536-BIT STATIC MOS ROM (8192×8)

2364-20/25/30/45

DC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 10\%$, unless otherwise specified

PARAMETER		TEST CONDITIONS	2364-20		2364-25		2364-30		2364-45		UNIT
			Min	Max	Min	Max	Min	Max	Min	Max	
	Input voltage										V
V_{IL}	Low (See Note 2)		−2.0	0.8	−2.0	0.8	−2.0	0.8	−2.0	0.8	
V_{IH}	High		2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	
	Output voltage										V
V_{OL}	Low	$I_{OL} = 3.2mA$		.4		.4		.4		.4	
V_{OH}	High	$I_{OH} = -400\mu A$	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	
I_{LI}	Input load current	$0V \leq V_{IN} \leq 5.5V$		1		1		1		1	μA
I_{LO}	Output leakage	Chip deselected. $V_{OUT} = +0.4V$ to V_{CC}		5		5		5		5	μA
I_{CC}	Supply current	Chip deselected. $V_{CC} = 5.5V$, $V_{IN} = V_{CC}$		90		90		80		80	mA
	Capacitance (See Note 3)										pF
C_{IN}	Input	$T_A = 25°C$, f = 1MHz all pins except		7		7		7		7	
C_{OUT}	Output	pin under test tied to ground		10		10		10		10	

NOTES

2. Input levels that swing more negative than −2.0V may alter AC electrical characteristics.
3. This parameter is periodically sampled and is not 100% tested.

AC ELECTRICAL CHARACTERISTICS

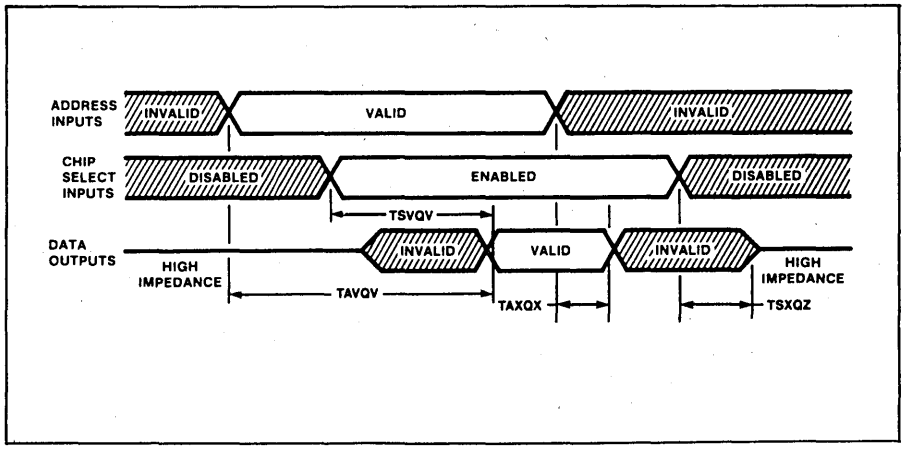
$T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 10\%$, Output load = 2 TTL loads and 100pF, Input transition time ≤ 10ns, Timing reference levels: Input = 1.5V, Output = 0.6V and 2.2V, 0.1μF ceramic capacitor between V_{CC} and GND pins, $V_{IL} \geq -2.0V$.

PARAMETER		2364-20		2364-25		2364-30		2364-45		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
T_{AVQV}	Address access time		200		250		300		450	ns
T_{SVQV} (See Note 4)	Chip select delay		100		120		120		150	ns
T_{SXQZ} (See Note 5)	Chip deselect delay		100		100		100		100	ns
T_{AXQX}	Previous data valid after address change delay	0		0		0		0		ns

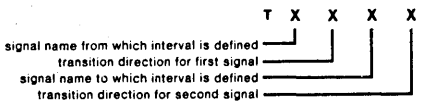
NOTES

4. T_{SVQV} is at value indicated, provided the valid address leads the chip select by ($T_{AVQV} - T_{SVQV}$) nsec or more.
5. T_{SXQZ} is measured at $V_{OL} = 0.8V$ on the "0" to high Z state transition, with 2 TTL loads connected to the output.

TIMING DIAGRAM



TIMING PARAMETER ABBREVIATIONS



The transition definitions used in this data sheet are

- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedence)
- A = Address
- S = Chip Select
- Q = Output

Nomenclature is adopted from JEDEC JC-42 Committee on Semiconductor Memories Standard.

131,072-BIT STATIC MOS ROM (16384×8) 23128-25/30/45

DESCRIPTION

This ROM is designed for memory applications where high performance, large bit storage, and simple interfacing are important design objectives.

The chip select inputs are programmable. Active high or active low level chip select input can be defined by the designer and the desired chip select logic level is fixed during the masking process. The programmable chip select input, as well as OR-tie compatibility on the outputs, facilitates easy memory expansion.

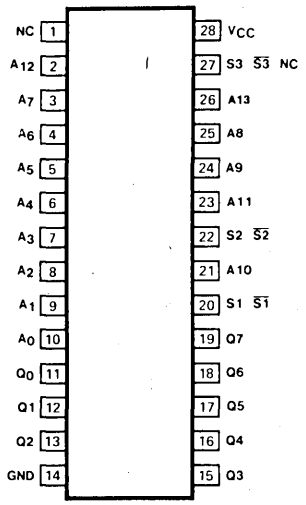
The 23128 Read Only Memory is fabricated with n-channel silicon gate technology. This technology provides.the designer with high performance, easy-to-use MOS circuits.

FEATURES

- **Fast access time**
  - **—250ns max. 23128-25**
  - **—300ns max. 23128-30**
  - **—450ns max. 23128-45**
- **Industry standard pinout—JEDEC approved**
- **Low power dissipation**
  - **— 495mW max for 23128-30/45**
  - **— 550mW max for 23128-25**
- **Completely TTL compatible**
- **One +5V ± 10% power supply**
- **3-state output—OR-tie capability**
- **Fully decoded—on chip address decode**
- **Inputs protected—all inputs have protection against static charge**
- **Three programmable chip select inputs for easy memory expansion or no connection option**

PIN CONFIGURATION

I,N PACKAGE



TOP VIEW

PACKAGE AVAILABILITY

I = Ceramic N = Plastic

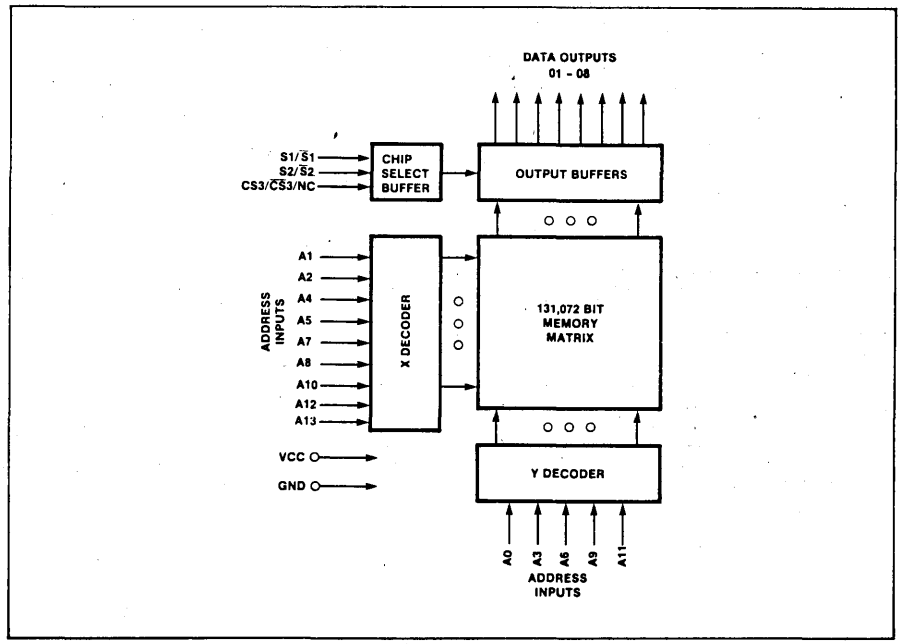
ABSOLUTE MAXIMUM RATINGS (See Note 1)

PARAMETER		RATING	UNIT
	Temperature range		°C
T_A	Operating	0 to +70	
T_{STG}	Storage	−65 to +150	
	Applied voltage		V
V_I	Input	−2.0 to +7	
V_O	Output	−2.0 to +7	
V_{CC}	Supply voltage to ground potential	−2.0 to +7	V

NOTE

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM



131,072-BIT STATIC MOS ROM (16384×8) 23128-25/30/45

DC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 10\%$, unless otherwise specified

PARAMETER		TEST CONDITIONS	23128-25		23128-30		23128-45		UNIT
			Min	Max	Min	Max	Min	Max	
	Input voltage								V
V_{IL}	Low (See Note 2)		−2.0	0.8	−2.0	0.8	−2.0	0.8	
V_{IH}	High		2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	
	Output voltage								V
V_{OL}	Low	$I_{OL} = 3.2mA$		.4		.4		.4	
V_{OH}	High	$I_{OH} = -400\mu A$	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	
I_{LI}	Input load current	$0V \le V_{IN} \le 5.5V$		1		1		1	μA
I_{LO}	Output leakage	Chip deselected $V_{OUT} = +0.4V$ to V_{CC}		5		5		5	μA
I_{CC}	Supply current	Chip deselected $V_{CC} = 5.5V$ $V_{IN} = V_{CC}$		100		90		90	mA
	Capacitance (See Note 3)								pF
C_{IN}	Input	$T_A = 25°C$, f = 1MHz all pins except		7		7		7	
C_{OUT}	Output	pin under test tied to ground		10		10		10	

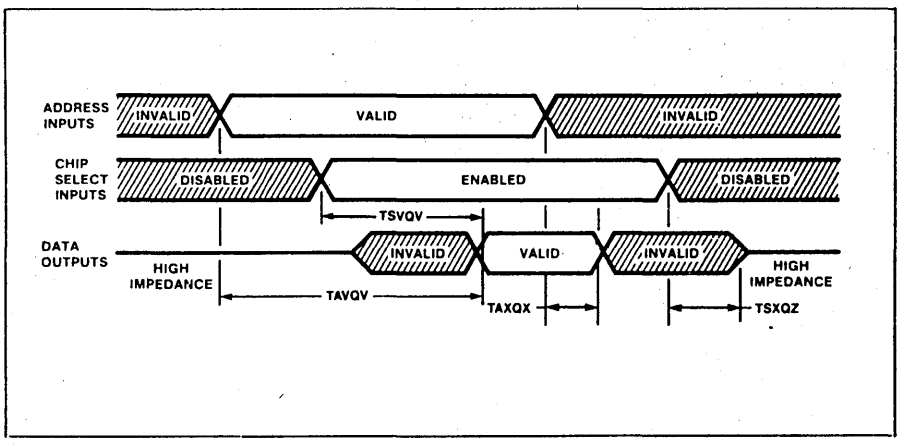
NOTES
2. Input levels that swing more negative than −2.0V may alter AC electrical characteristics.
3. This parameter is periodically sampled and is not 100% tested.

AC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 10\%$, Output load = 2 TTL loads and 100pF, Input transition time ≤ 10ns, Timing reference levels: Input = 1.5V, Output = 0.6V and 2.2V, 0.1μF ceramic capacitor between V_{CC} and GND pins, $V_{IL} \ge -2.0V$.

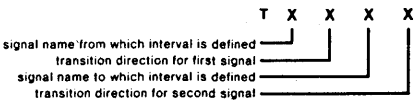
PARAMETER		23128-25		23128-30		23128-45		UNIT
		Min	Max	Min	Max	Min	Max	
T_{AVQV}	Address access time		250		300		450	ns
T_{SVQV} (See Note 4)	Chip select delay		120		120		150	ns
T_{SXQZ} (See Note 5)	Chip deselect delay		100		100		100	ns
T_{AXQX}	Previous data valid after address change delay	0		0		0		ns

NOTES
4. T_{SVQV} is at value indicated, provided the valid address leads the chip select by ($T_{AVQV} - T_{SVQV}$) nsec or more.
5. T_{SXQZ} is measured at $V_{OL} = 0.8V$ on the "0" to high Z state transition, with 2 TTL loads connected to the output.

TIMING DIAGRAM



TIMING PARAMETER ABBREVIATIONS



The transition definitions used in this data sheet are
- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedence)
- A = Address
- S = Chip Select
- Q = Output

Nomenclature is adopted from JEDEC JC-42 Committee on Semiconductor Memories Standard.

Signetics

MEMORY

262,144-Bit Static MOS ROM (32,768 × 8) 23256A

Preview

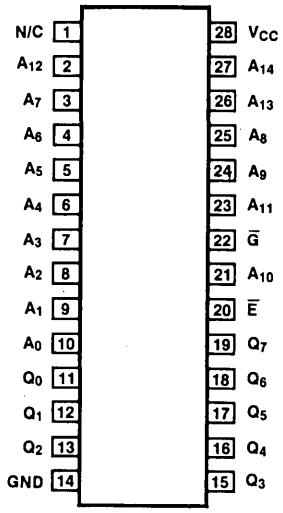
DESCRIPTION

The 23256A is 262,144-Bit Read-Only-Memory organized 32,768 by 8 bits. The pinout conforms to JEDEC standards for byte-wide memories. It is a fully static device with reduced power consumption when the device is deselected.

FEATURES

- **Completely TTL compatible, 2 TTL loads**
- **Single 5 volt ±10% power supply**
- **Tri-state outputs**
- **Fast access time — 200ns**
- **Fully static**
- **Low standby power**
- **JEDEC approved byte wide pinout**
- **Inputs and outputs protected against static charge**

PIN CONFIGURATION



TOP VIEW

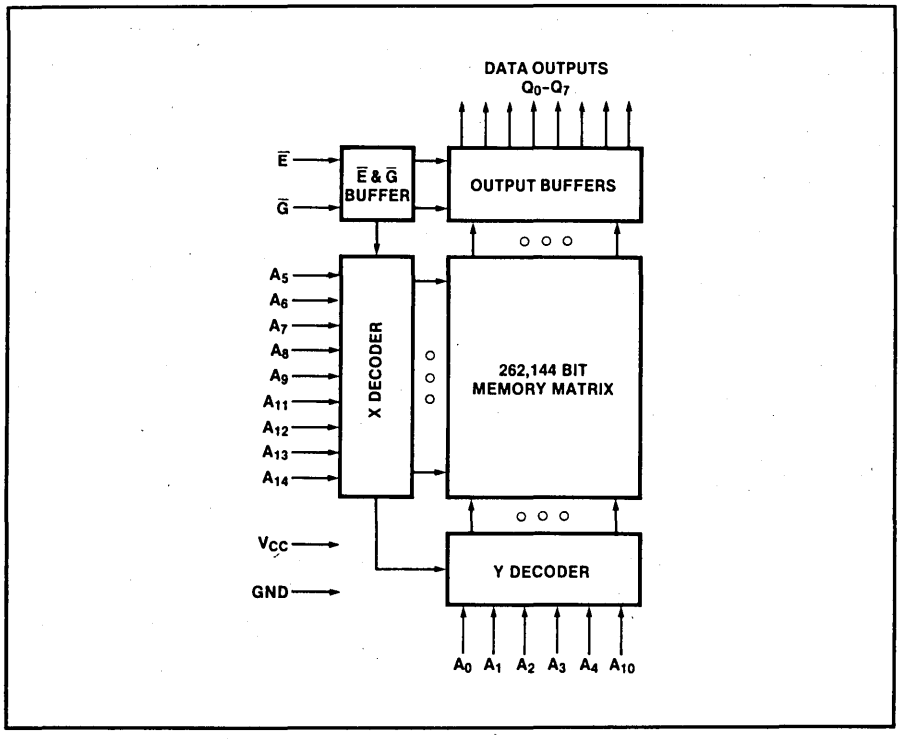
ABSOLUTE MAXIMUM RATINGS (See Note 1)

PARAMETER		RATING	UNIT
	Temperature range		°C
T_A	Operating	0 to +70	
T_{STG}	Storage	−65 to +150	
	Applied voltage		V
V_I	Input	−2.0 to +7	
V_O	Output	−2.0 to +7	
V_{CC}	Supply voltage to ground potential	−2.0 to +7	V

NOTE

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM



Signetics

262,144-Bit Static MOS ROM (32,768 × 8) 23256A

Preview

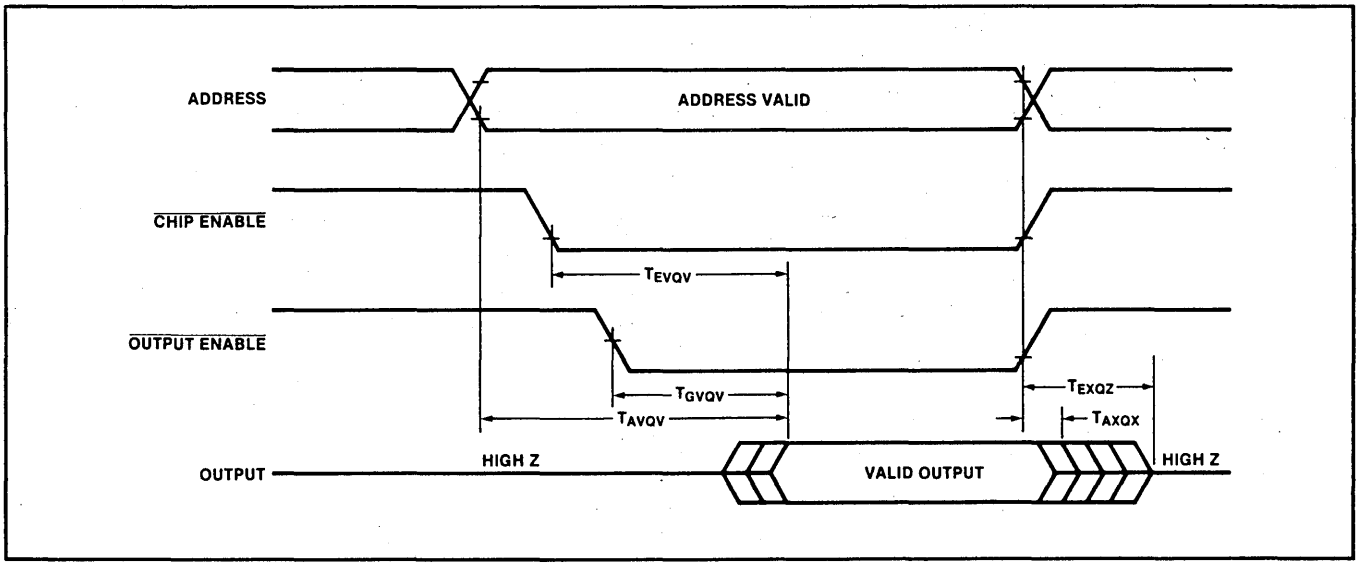
DC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5.0V \pm 10\%$, unless otherwise specified

PARAMETER	TEST CONDITIONS	Min	Max	UNIT
Input Voltage				
V_{IL} Low		−2.0	0.8	V
V_{IH} High		2.0	V_{CC}	V
Output Voltage				
V_{OL} Low	$I_{OL} = 3.2mA$		.4	V
V_{OH} High	$I_{OH} = -400\mu A$	2.4	V_{CC}	V
Input Load Current				
I_{LI}	$0V \le V_{IN} \le 5.5V$		1	μA
Output Leakage				
I_{LO}			5	μA
Supply Current				
I_{CC} (Active)	Output unloaded		100	mA
I_{CC_Z} (Standby)	$\overline{E} = V_{IH}$		15	mA
Capacitance	$T_A = 25°C$, $F = 1MHz$			
C_{IN} Input	All pins except pin under		7	pF
C_{OUT} Output	test tied to ground		12	pF

AC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5.0V \pm 10\%$, Output = 2 TTL Loads and 100pF, Input transition time = 10ns. Timing reference levels: Input = 1.5V, Output = 0.6V and 1.1V, 0.1μf capacitor between V_{CC} and GND

SYMBOL	PARAMETER	Min	Max	UNIT
T_{AVQV}	Address access time		200	ns
T_{EVQV}	Chip enable to output delay		200	ns
T_{GVQV}	Output enable to output valid delay		100	ns
T_{EXQZ}	Chip disable delay ($V_{OL} = 0.8V$ on the "0" to high Z transition with 2 TTL loads)		100	ns
T_{AXQX}	Previous data valid after address change delay	0		ns

AC WAVEFORMS



32,768-BIT STATIC MOS ROM (4096×8) 2632A-20/25/30/45

DESCRIPTION

This ROM is designed for memory applications where high performance, large bit storage, and simple interfacing are important design objectives.

The two chip select inputs are programmable. Any combination of active high or low level chip select inputs can be defined by the designer and the desired chip select logic level is fixed during the masking processing. These two programmable chip select inputs, as well as OR-tie compatibility on the outputs, facilitates easy memory expansion.

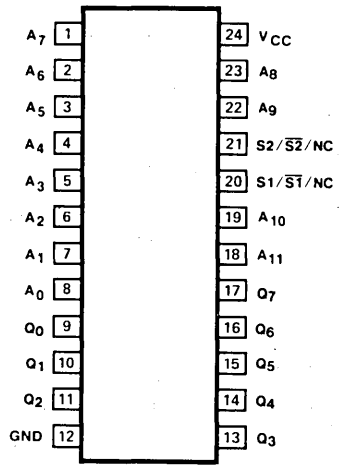
The 2632A Read Only Memory is fabricated with n-channel silicon gate technology. This technology provides the designer with high performance easy-to-use MOS circuits.

FEATURES

- **Fast access time**
  - **—200ns max. 2632A-20**
  - **—250ns max. 2632A-25**
  - **—300ns max. 2632A-30**
  - **—450ns max. 2632A-45**
- **Industry standard pinout—JEDEC approved**
- **Low power dissipation**
  - **— 357mW max. for 2632A-30/45**
  - **— 412mW max. for 2632A-20/25**
- **Completely TTL compatible**
- **Single +5V ±10% power supply**
- **3-state output—OR-tie capability**
- **Fully decoded—on chip address decode**
- **Inputs protected—all inputs have protection against static charge**
- **Two programmable chip select inputs for easy memory expansion or no connection option.**

PIN CONFIGURATION

F,I,N PACKAGE



(TOP VIEW)

PACKAGE AVAILABILITY

F = Cerdip I = Ceramic N = Plastic

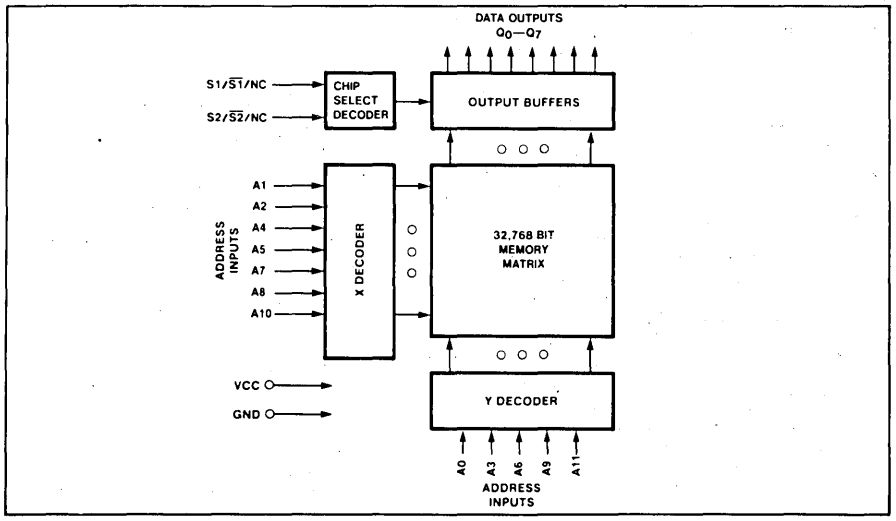
ABSOLUTE MAXIMUM RATINGS (See Note 1)

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_A	Operating	0 to +70	
T_{STG}	Storage	−65 to +150	
	Applied voltage		V
V_I	Input	−2.0 to +7	
V_O	Output	−2.0 to +7	
V_{CC}	Supply voltage to ground potential	−2.0 to +7	V

NOTE

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM



32,768-BIT STATIC MOS ROM (4096 × 8) 2632A-20/25/30/45

DC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 10\%$, unless otherwise specified

PARAMETER		TEST CONDITIONS	2632A-20		2632A-25		2632A-30		2632A-45		UNIT
			Min	Max	Min	Max	Min	Max	Min	Max	
	Input voltage										V
V_{IL}	Low (See Note 2)		−2.0	0.8	−2.0	0.8	−2.0	0.8	−2.0	0.8	
V_{IH}	High		2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	
	Output voltage										V
V_{OL}	Low	$I_{OL} = 3.2mA$		.4		.4		.4		.4	
V_{OH}	High	$I_{OH} = -400\mu A$	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	
I_{LI}	Input load current	$0V \le V_{IN} \le 5.5V$		1		1		1		1	μA
I_{LO}	Output leakage	Chip deselected. $V_{OUT} = +0.4V$ to V_{CC}		5		5		5		5	μA
I_{CC}	Supply current	Chip deselected $V_{CC} = 5.5V$, $V_{IN} = V_{CC}$		75		75		65		65	mA
	Capacitance (See Note 3)										pF
C_{IN}	Input	$T_A = 25°C$, f = 1MHz all pins except		7		7		7		7	
C_{OUT}	Output	pin under test tied to ground		10		10		10		10	

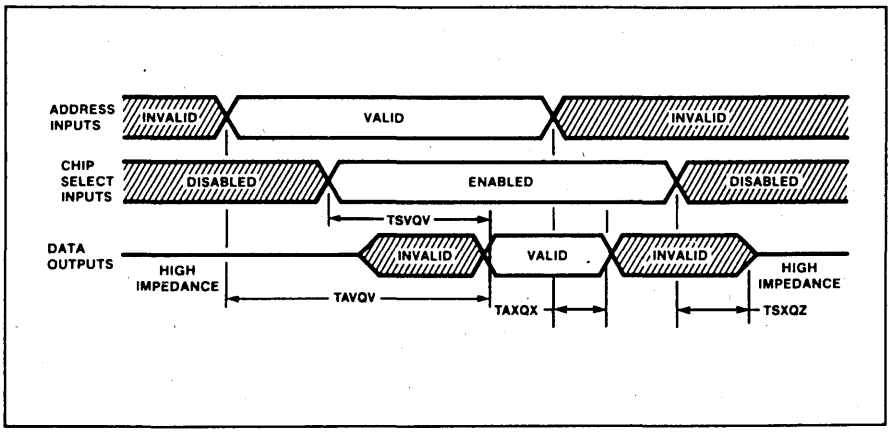
NOTES
2. Input levels that swing more negative than −2.0V may alter AC electrical characteristics.
3. This parameter is periodically sampled and is not 100% tested.

AC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 10\%$, Output load = 2 TTL loads and 100pF, Input transition time ≤ 10ns, Timing reference levels: Input = 1.5V, Output = 0.6V and 2.2V, 0.1μF ceramic capacitor between V_{CC} and GND pins, $V_{IL} \ge -2.0V$.

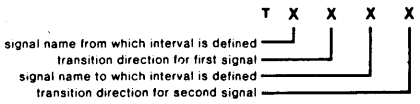
PARAMETER		2632A-20		2632A-25		2632A-30		2632A-45		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
T_{AVQV}	Address access time		200		250		300		450	ns
T_{SVQV} (See Note 4)	Chip select delay		100		120		120		150	ns
T_{SXQZ} (See Note 5)	Chip deselect delay		100		100		100		100	ns
T_{AXQX}	Previous data valid after address change delay	0		0		0		0		ns

NOTES
4. T_{SVQV} is at value indicated, provided the valid address leads the chip select by $(T_{AVQV} - T_{SVQV})$ nsec or more.
5. T_{SXQZ} is measured at $V_{OL} = 0.8V$ on the "0" to high Z state transition, with 2 TTL loads connected to the output.

TIMING DIAGRAM



TIMING PARAMETER ABBREVIATIONS



The transition definitions used in this data sheet are
- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedence)
- A = Address
- S = Chip Select
- Q = Output

Nomenclature is adopted from JEDEC JC-42 Committee on Semiconductor Memories Standard

Signetics

MEMORY

65,536-BIT STATIC MOS ROM (8192×8) 2664A-20/25/30/45

DESCRIPTION

This ROM is designed for memory applications where high performance, large bit storage, and simple interfacing are important design objectives.

The chip select input is programmable. Active high or active low level chip select input can be defined by the designer and the desired chip select logic level is fixed during the masking process. The programmable chip select input, as well as OR-tie compatibility on the outputs, facilitates easy memory expansion.

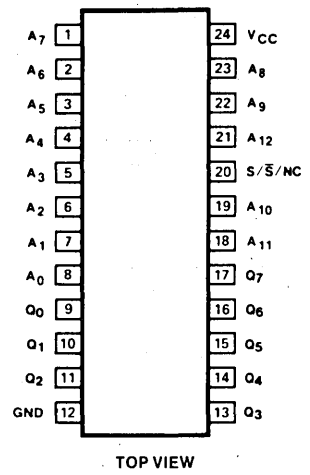
The 2664A Read Only Memory is fabricated with n-channel silicon gate technology. This technology provides the designer with high performance, easy-to-use MOS circuits.

FEATURES

- **Fast access time**
  - **—200ns max. 2664A-20**
  - **—250ns max. 2664A-25**
  - **—300ns max. 2664A-30**
  - **—450ns max. 2664A-45**
- **Industry standard pinout—JEDEC approved**
- **Low power dissipation**
  - **— 440mW max. for 2664A-30/45**
  - **— 495mW max. for 2664A-20/25**
- **Completely TTL compatible**
- **Single +5V ±10% power supply**
- **3-state output—OR-tie capability**
- **Fully decoded—on chip address decode**
- **Inputs protected—all inputs have protection against static charge**
- **One programmable chip select input for easy memory expansion or no connection option.**

PIN CONFIGURATION

N PACKAGE



TOP VIEW

PACKAGE AVAILABILITY
F = Cerdip I = Ceramic N = Plastic

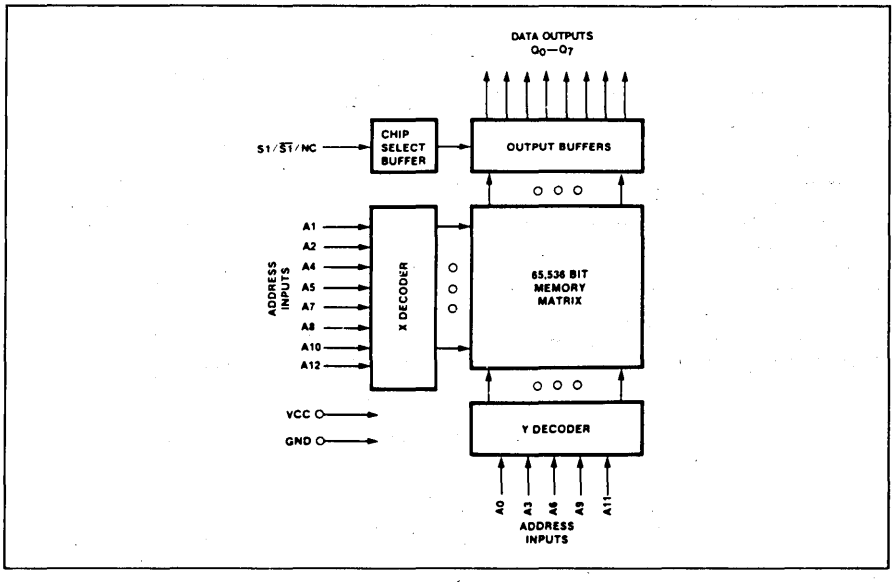
ABSOLUTE MAXIMUM RATINGS (See Note 1)

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_A	Operating	0 to +70	
T_{STG}	Storage	−65 to +150	
	Applied voltage		V
V_I	Input	−2.0 to +7	
V_O	Output	−2.0 to +7	
V_{CC}	Supply voltage to ground potential	−2.0 to +7	V

NOTE

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM



65,536-BIT STATIC MOS ROM (8192×8) 2664A-20/25/30/45

DC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 10\%$, unless otherwise specified

PARAMETER		TEST CONDITIONS	2664A-20		2664A-25		2664A-30		2664A-45		UNIT
			Min	Max	Min	Max	Min	Max	Min	Max	
	Input voltage										V
V_{IL}	Low (See Note 2)		−2.0	0.8	−2.0	0.8	−2.0	0.8	−2.0	0.8	
V_{IH}	High		2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	
	Output voltage										V
V_{OL}	Low	$I_{OL} = 3.2mA$		.4		.4		.4		.4	
V_{OH}	High	$I_{OH} = -400\mu A$	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	
I_{LI}	Input load current	$0V \le V_{IN} \le 5.5V$		1		1		1		1	μA
I_{LO}	Output leakage	Chip deselected $V_{OUT} = +0.4V$ to V_{CC}		5		5		5		5	μA
I_{CC}	Supply current	Chip deselected $V_{CC} = 5.5V$, $V_{IN} = V_{CC}$		90		90		80		80	mA
	Capacitance (See Note 3)										pF
C_{IN}	Input	$T_A = 25°C$, f = 1MHz all pins except		7		7		7		7	
C_{OUT}	Output	pin under test tied to ground		10		10		10		10	

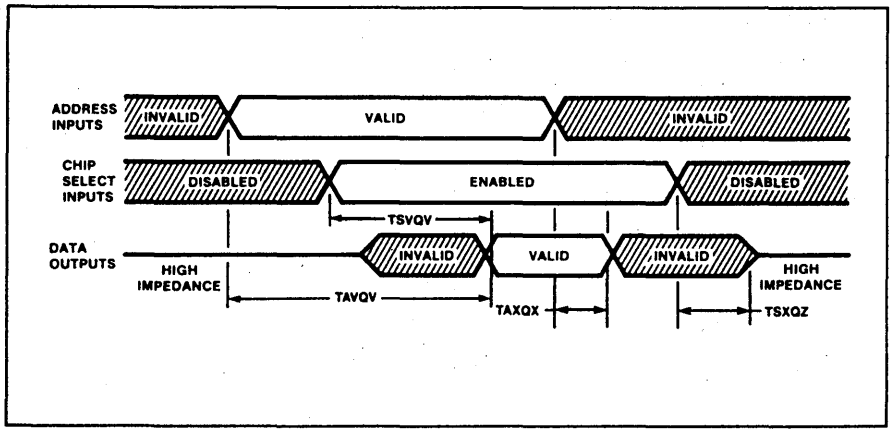
NOTES
2. Input levels that swing more negative than −2.0V may alter AC electrical characteristics.
3. This parameter is periodically sampled and is not 100% tested.

AC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 10\%$, Output load = 2 TTL loads and 100pF, Input transition time = ≤ 10ns, Timing reference levels: Input = 1.5V, Output = 0.6V and 2.2V, 0.1μF ceramic capacitor between V_{CC} and GND pins, $V_{IL} \ge -2.0V$.

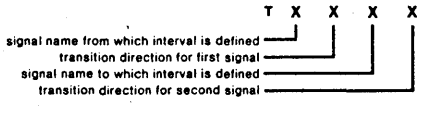
PARAMETER		2664A-20		2664A-25		2664A-30		2664A-45		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
T_{AVQV}	Address access time		200		250		300		450	ns
T_{SVQV} (See Note 4)	Chip select delay		100		120		120		150	ns
T_{SXQZ} (See Note 5)	Chip deselect delay		100		100		100		100	ns
T_{AXQX}	Previous data valid after address change delay	0		0		0		0		ns

NOTES
4. T_{SVQV} is at value indicated, provided the valid address leads the chip select by $(T_{AVQV} - T_{SVQV})$ nsec or more.
5. T_{SXQZ} is measured at $V_{OL} = 0.8V$ on the "0" to high Z state transition, with 2 TTL loads connected to the output.

TIMING DIAGRAM



TIMING PARAMETER ABBREVIATIONS



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- X = transition to invalid or don't care
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- A = Address
- S = Chip Select
- Q = Output

Nomenclature is adopted from JEDEC JC-42 Committee on Semiconductor Memories Standard.

Signetics

MEMORY

SELECTION GUIDE

DEVICE	ORGANIZATION	OUTPUT CIRCUIT[1]	OUTPUT LOGIC[2]	ACCESS TIME[4]	TEMPERATURE[3]	PACKAGE[5]	PINS	MAX I_{CC}
CAMs								
10155	8 × 2	OE	—	13	C	F, N	18	140
RAMs								
3101A	16 × 4	OC	B	35	C	F, N	16	105
54/74S189	16 × 4	TS	B	35	M, C	F, N	16	110
82S21	32 × 2	OC	T	50	C	F, N	16	130
82S16	256 × 1	TS	T	50	M, C	F, N	16	115
82S17	256 × 1	OC	T	50	M, C	F, N	16	115
74S301	256 × 1	OC	B	50	M, C	F, N	16	115
82LS16	256 × 1	TS	T	40	M, C	F, N	16	70
82LS17	256 × 1	OC	T	40	M, C	F, N	16	70
74LS301	256 × 1	OC	B	40	M, C	F, N	16	70
82S09	64 × 9	OC	T	45	M, C	F, N	28	190
82S09A	64 × 9	OC	T	35	C	F, N	28	190
82S19	64 × 9	OC	B	35	M, C	F, N	28	190
82S210	256 × 9	TS	B	60	M, C	F, N	24	185
82S212	256 × 9	TS	B	45	M, C	F, N	22	185
82S212A	256 × 9	TS	B	35	C	F, N	22	185
8X350	256 × 8	TS	B	N/A	M, C	F, N	22	185
ECL								
10415	1024 × 1	OE	B	20	C	F	16	150
10415A	1024 × 1	OE	B	15	C	F	16	150
10415B	1024 × 1	OE	B	10	C	F	16	150
100415	1024 × 1	OE	B	20	C	F	16	150
100415A	1024 × 1	OE	B	15	C	F	16	150
100415B	1024 × 1	OE	B	10	C	F	16	150
100422	256 × 4	OE	B	20	C	F	24	210
10422A	256 × 4	OE	B	15	C	F	24	210
10422B	256 × 4	OE	B	10	C	F	24	210
10470	4096 × 1	OE	B	25	C	F	18	150
10470A	4096 × 1	OE	B	15	C	F	18	150
100470	4096 × 1	OE	B	25	C	F	18	150
100470A	4096 × 1	OE	B	15	C	F	18	150
10474	1024 × 4	OE	B	30	C	F	24	195
10474A	1024 × 4	OE	B	20	C	F	24	195
100474	1024 × 4	OE	B	30	C	F	24	195
100474A	1024 × 4	OE	B	20	C	F	24	195
FPLAs								
82S100	16 × 48 × 8	TS	—	50	M, C	F, N	28	170
82S101	16 × 48 × 8	OC	—	50	M, C	F, N	28	170
82S152	18 × 32 × 10	OC	I/O	40	M, C	F, N	20	155
82S152A	18 × 32 × 10	OC	I/O	30	M, C	F, N	20	155
82S153	18 × 32 × 10	TS	I/O	40	M, C	F, N	20	155
82S153A	18 × 32 × 10	OC	I/O	30	M, C	F, N	20	155
FPGAs								
82S150	18 × 12	OC	I/O	20	M, C	F, N	20	155
82S151	18 × 12	TS	I/O	20	M, C	F, N	20	155
82S102	16 × 9	OC	—	35	M, C	F, N	28	170
82S103	16 × 9	TS	—	35	M, C	F, N	28	170
FPLSs								
82S104	16 × 48 × 8	OC	R	60	M, C	F, N	28	180
82S104A	16 × 48 × 8	OC	R	50	M, C	F, N	28	180
82S105	16 × 48 × 8	TS	R	60	M, C	F, N	28	180
82S105A	16 × 48 × 8	TS	R	50	M, C	F, N	28	180
82S154	16 × 32 × 12	OC	I/O, R	65	M, C	F, N	20	155
82S155	16 × 32 × 12	TS	I/O, R	65	M, C	F, N	20	155
82S156	16 × 32 × 12	OC	I/O, R	65	M, C	F, N	20	155
82S157	16 × 32 × 12	TS	I/O, R	65	M, C	F, N	20	155
82S158	16 × 32 × 12	OC	I/O, R	65	M, C	F, N	20	155
82S159	16 × 32 × 12	TS	I/O, R	65	M, C	F, N	20	155

NOTES on following page

SELECTION GUIDE

DEVICE	ORGANIZATION	OUTPUT CIRCUIT[1]	OUTPUT LOGIC[2]	ACCESS TIME[4]	TEMPERATURE[3]	PACKAGE[5]	PINS	MAX I_{CC}
PROMs								
82S23	32 x 8	OC	—	50	M, C	F, N	16	77
82S23A	32 x 8	OC	—	25	M, C	F, N	16	100
82S123	32 x 8	TS	—	50	M, C	F, N	16	77
82S123A	32 x 8	TS	—	25	M, C	F, N	16	100
82S126	256 x 4	OC	—	50	M, C	F, N	16	120
82S126A	256 x 4	OC	—	35	M, C	F, N	16	120
82S129	256 x 4	TS	—	50	M, C	F, N	16	120
82S129A	256 x 4	TS	—	35	M, C	F, N	16	120
10149	256 x 4	OE	—	20	C	F	16	150
100149	256 x 4	OE	—	20	C	F	16	150
82S130	512 x 4	OC	—	50	M, C	F, N	16	140
82S130A	512 x 4	OC	—	35	M, C	F, N	16	140
82S131	512 x 4	TS	—	50	M, C	F, N	16	140
82S131A	512 x 4	TS	—	35	M, C	F, N	16	140
82S115	512 x 8	TS	—	60	M, C	F, N	24	175
82S140	512 x 8	OC	—	60	M, C	F, N	24	175
82S141	512 x 8	TS	—	60	M, C	F, N	24	175
82S137	1024 x 4	TS	—	60	M, C	F, N	18	140
82S137A	1024 x 4	TS	—	45	M, C	F, N	18	140
82S137B	1024 x 4	TS	—	35	C	F, N	18	140
82S147	512 x 8	TS	—	60	M, C	F, N	16	155
82S147A	512 x 8	TS	—	45	M, C	F, N	20	155
82LS181	1024 x 8	TS	—	150	M, C	F, N	24	80
82S180	1024 x 8	OC	—	70	M, C	F, N	24	175
82S181	1024 x 8	TS	—	70	M, C	F, N	24	175
82S181A	1024 x 8	TS	—	50	M, C	F, N	24	175
82S181B	1024 x 8	TS	—	45	C	F, N	24	175
82S183	1024 x 8	TS	—	60	M, C	F, N	24	175
82S2708	1024 x 8	TS	—	90	M	F, R, G	24	185
82S185	2048 x 4	TS	—	100	M, C	F, N	18	120
82S185A	2048 x 4	TS	—	50	M, C	F, N	18	155
82S185B	2048 x 4	TS	—	45	C	F, N	18	155
82S191	2048 x 8	TS	—	80	M, C	F, N	24	175
82S191A	2048 x 8	TS	—	60	M, C	F, N	24	175
82HS195	4096 x 4	TS	—	35	M, C	F, N	20	155
82S321	4096 x 8	TS	—	80	M, C	F, N	24	175
82HS321	4096 x 8	TS	—	40	M, C	F, N	24	175
82HS641	4096 x 8	TS	—	45	M, C	F, N	24	175

NOTES:
1. Output circuit:
   OE = Open emitter
   OC = Open collector
   TS = 3-State
2. Output logic:
   T = Transparent — input data appears on output during Write
   B = Blanked — output is blanked during Write
   R = Output logic
   I/O = Input/output option
3. Temperature range:
   C = Commercial (0°C to +75°C)
   M = Military (−55°C to +125°C)
4. Commercial (0°C to +75°C)
5. Packages:
   F = Hermetic Cerdip Dual In Line
   N = Plastic Dual In Line
   R = Ceramic Flat Pack
   G = Ceramic Square Leadless Chip Carrier

FIELD PROGRAMMABLE LOGIC ARRAY (16×48×8) 82S100 (T.S.)/82S101 (O.C.)

INTEGRATED FUSE LOGIC
SERIES 28

DESCRIPTION

The 82S100 (tri-state) and 82S101 (open collector) are Bipolar, Fuse-Link Programmable Logic Arrays (FPLA). Each device utilizes the standard AND/OR/Invert architecture to directly implement custom sum of product logic equations.

Each device consists of 16 dedicated inputs and 8 dedicated outputs. Each output is capable of being actively controlled by any or all of the 48 product terms. The true, complement, or don't care condition of each of the 16 inputs ANDed together comprise one P-term. All 48 P-terms are then ORed to each output. The user must then only select which P-terms will activate an output by disconnecting terms which do not affect the output. In addition each output can be fused as active-high$^{(H)}$ or active-low$^{(L)}$.

The 82S100 and 82S101 are fully TTL compatible, and include chip-enable control for expansion of input variables, and output inhibit. They feature either open collector or tri-state outputs for ease of expansion of product terms and application in bus-organized systems.

Both devices are available in commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S100/101, F or N, and for the military temperature range (−55°C to +125°C) specify S82S100/101, F or G, I, R.

FEATURES

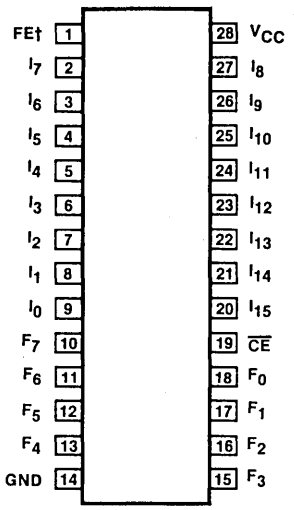
- **Field programmable (Ni-Cr link)**
- **Input variables: 16**
- **Output functions: 8**
- **Product terms: 48**
- **Address access time:**
  S82S100/101 — 80ns max
  N82S100/101 — 50ns max
- **Power dissipation: 600mW typ**
- **Input loading:**
  S82S100/101: −150μA max
  N82S100/101: −100μA max
- **Chip enable input**
- **Output option:**
  82S100: Tri-state
  82S101: Open collector
- **Output disable function:**
  Tri-state — Hi-Z
  Open collector — Hi
- **Separate I/O architecture**

APPLICATIONS

- **CRT display systems**
- **Random logic**
- **Code conversion**
- **Peripheral controllers**
- **Function generators**
- **Look-up and decision tables**
- **Microprogramming**
- **Address mapping**
- **Character generators**
- **Data security encoders**
- **Fault detectors**
- **Frequency synthesizers**
- **16 bit-to-8 bit bus interface**
- **Random logic replacement**

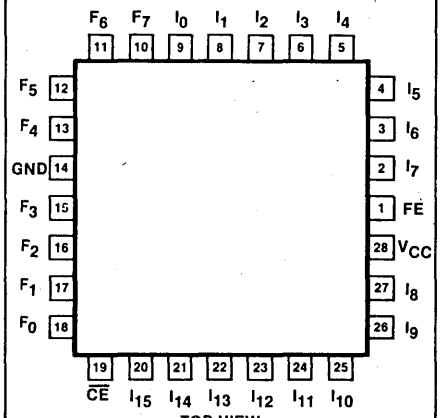
PIN CONFIGURATION

F,I,N,R PACKAGE*



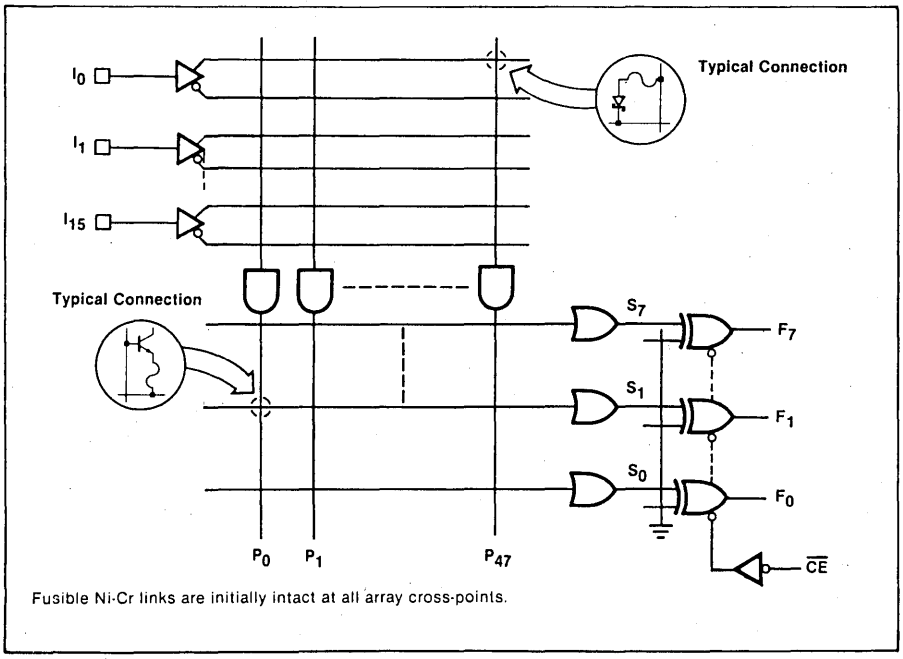
*F = Cerdip I = Ceramic N = Plastic
†Open or grounded during normal operation.

G PACKAGE



G = Leadless TOP VIEW

LOGIC DIAGRAM



Fusible Ni-Cr links are initially intact at all array cross-points.

See Pages 3909-3910 for Product Selector Guides.

FIELD PROGRAMMABLE LOGIC ARRAY (16×48×8) 82S100 (T.S.)/82S101 (O.C.)

INTEGRATED FUSE LOGIC
SERIES 28

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING Min	RATING Max	UNIT
V_{CC}	Supply voltage		+7	Vdc
V_{IN}	Input voltage		+5.5	Vdc
V_{OUT}	Output voltage		+5.5	Vdc
I_{IN}	Input currents	−30	+30	mA
I_{OUT}	Output currents		+100	mA
	Temperature range			°C
T_A	Operating			
	N82S100/101	0	+75	
	S82S100/101	−55	+125	
T_{STG}	Storage	−65	+150	

THERMAL RATINGS

TEMPERATURE	MILITARY	COMMERCIAL
Maximum junction	175°C	150°C
Maximum ambient	125°C	75°C
Allowable thermal rise ambient to junction	50°C	75°C

DC ELECTRICAL CHARACTERISTICS

N82S100/101: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S100/101: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS	N82S100/101 Min	N82S100/101 Typ[2]	N82S100/101 Max	S82S100/101 Min	S82S100/101 Typ[2]	S82S100/101 Max	UNIT
	Input voltage[3]								V
V_{IH}	High	V_{CC} = Max	2			2			
V_{IL}	Low	V_{CC} = Min			0.85			0.8	
V_{IC}	Clamp[3,4]	V_{CC} = Min, I_{IN} = −18mA		−0.8	−1.2		−0.8	−1.2	
	Output voltage	V_{CC} = Min							V
V_{OH}	High (82S100)[3,5]	I_{OH} = −2mA	2.4			2.4			
V_{OL}	Low[3,6]	I_{OL} = 9.6mA		0.35	0.45		0.35	0.50	
	Input current								μA
I_{IH}	High	V_{IN} = 5.5V		<1	25		<1	50	
I_{IL}	Low	V_{IN} = 0.45V		−10	−100		−10	−150	
	Output current	$\overline{CE}$ = High, V_{CC} = Max							
I_{OLK}	Leakage[7]	V_{OUT} = 5.5V		1	40		1	60	μA
$I_{O(OFF)}$	Hi-Z state (82S100)[7]	V_{OUT} = 5.5V		1	40		1	60	μA
		V_{OUT} = 0.45V		−1	−40		−1	−60	
I_{OS}	Short circuit (82S100)[4,8]	$\overline{CE}$ = Low, V_{OUT} = 0V	−20		−70	−15		−85	mA
I_{CC}	V_{CC} supply current[9]	V_{CC} = Max		120	170		120	180	mA
	Capacitance[7]	$\overline{CE}$ = High, V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		8			8		
C_{OUT}	Output	V_{OUT} = 2.0V		17			17		

AC ELECTRICAL CHARACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$
N82S100/101: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S100/101: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TO	FROM	N82S100/101 Min	N82S100/101 Typ[2]	N82S100/101 Max	S82S100/101 Min	S82S100/101 Typ[2]	S82S100/101 Max	UNIT
	Propagation delay									ns
T_{IA}	Input	Output	Input		35	50		35	80	
T_{CE}	Chip enable	Output	Chip enable		15	30		15	50	
	Disable time									ns
T_{CD}	Chip disable	Output	Chip enable		15	30		15	50	

NOTES:
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and only functional operation of the device at these or any other conditions above those indicated in the operation of the device specifications is not implied.
2. All voltages are at V_{CC} = 5V, T_A = 25°C.
3. All voltage values are with respect to network ground terminal.
4. Test one at a time.
5. Measured with V_{IL} applied to $\overline{CE}$ and a logic high stored.
6. Measured with a programmed logic condition for which the output test is at a low logic level. Output sink current is applied through a resistor to V_{CC}.
7. Measured with V_{IH} applied to $\overline{CE}$.
8. Duration of short circuit should not exceed 1 second.
9. I_{CC} is measured with the chip enable input grounded, all other inputs at 4.5V and the outputs open.

FIELD PROGRAMMABLE GATE ARRAY (16×9×9) 82S102 (O.C.)/82S103 (T.S.)

INTEGRATED FUSE LOGIC
SERIES 28

DESCRIPTION

The 82S102 and 82S103 are Bipolar, fuse programmable, gate arrays. The device consists of 9 AND/NAND Gates which share 16 common inputs. The type of gate is selected by programming the output as active-high$^{(H)}$ or active-low$^{(L)}$. Each of the 16 inputs I_0-I_{15} can be programmed to provide the True (H), Complement (L), or Don't Care (—) state to each of the 9 AND/NAND gates. OR/NOR logic functions can also be implemented by complementing the inputs and outputs via on-chip inverting buffers.

Both devices are field-programmable, which means that custom patterns are immediately available.

The 82S102 and 82S103 include chip-enable control for output strobing and inhibit. They feature either open collector or tri-state outputs for ease of expansion of input variables and application in bus-organized systems.

Both devices are available in the commercial and military temperature ranges. For the commercial range (0°C to +75°C) specify N82S102/103, F or N, and for the military range (−55°C to +125°C) specify S82S102/103, F, G, I, and R.

FEATURES

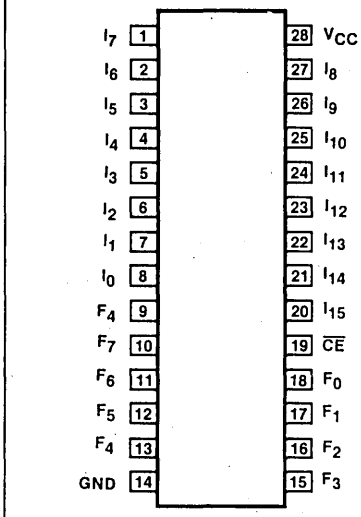
- **Field programmable (Ni-Cr link)**
- **16 input variables**
- **9 output functions**
- **Chip enable input**
- **I/O propagation delay:**
  N82S102/103: 35ns max
  S82S102/103: 50ns max
- **Power dissipation: 600mW typ**
- **Input loading:**
  N82S102/103: -100μA max
  S82S102/103: -150μA max
- **Output options:**
  82S102: Open collector
  82S103: Tri-state
- **Output disable function:**
  82S102: Hi
  82S103: Hi-Z
- **Fully TTL compatible**

APPLICATIONS

- **Random logic**
- **Address decoders**
- **Code detectors**
- **Peripheral selectors**
- **Fault monitors**
- **Machine state decoders**

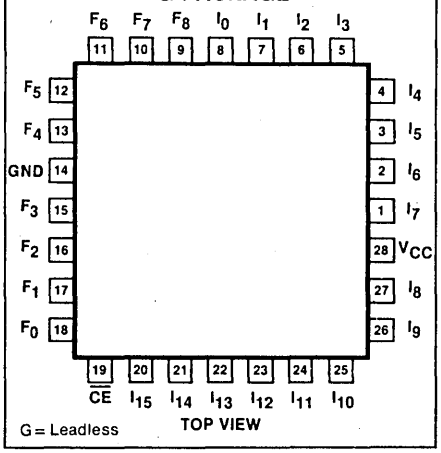
PIN CONFIGURATION

F,I,N,R PACKAGE*



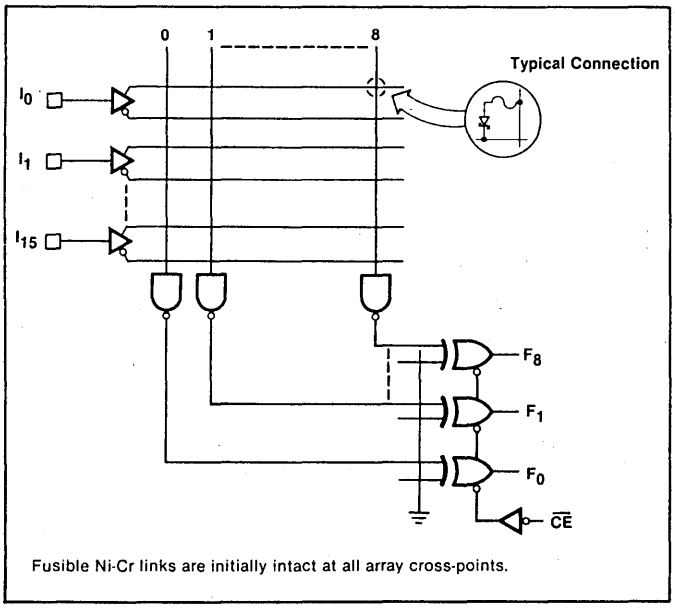
*F = Cerdip N = Plastic
I = Ceramic R = Flat Pack

G PACKAGE



G = Leadless TOP VIEW

LOGIC DIAGRAM



Fusible Ni-Cr links are initially intact at all array cross-points.

FIELD PROGRAMMABLE GATE ARRAY (16×9×9) 82S102 (O.C.)/82S103 (T.S.)

INTEGRATED FUSE LOGIC
SERIES 28

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S102)	+5.5	
V_O	Off-state (82S103)	+5.5	
I_{IN}	Input current	±30	mA
I_{OUT}	Output current	+100	mA
	Temperature range		°C
T_A	Operating		
	N82S102/103	0 to +75	
	S82S102/103	−55 to +125	
T_{STG}	Storage	−65 to +150	

THERMAL RATINGS

TEMPERATURE	MILITARY	COMMERCIAL
Maximum junction	175°C	150°C
Maximum ambient	125°C	75°C
Allowable thermal rise ambient to junction	50°C	75°C

DC ELECTRICAL CHARACTERISTICS

N82S102/103: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S102/103: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER[1]		TEST CONDITIONS	N82S102/103			S82S102/103			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low[1]	V_{CC} = Min			0.85			0.8	
V_{IH}	High[1]	V_{CC} = Max	2.0			2.0			
V_{IC}	Clamp[1,3]	V_{CC} = Min, I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage	V_{CC} = Min							V
V_{OL}	Low[1,4]	I_{OL} = 9.6mA		0.35	0.45		0.35	0.50	
V_{OH}	High (82S103)[1,5]	I_{OH} = -2mA	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V		-10	-100		-10	-150	
I_{IH}	High	V_{IN} = 5.5V		<1	25		<1	50	
	Output current	V_{CC} = Max							
I_{OLK}	Leakage (82S102)[6]	V_{OUT} = 5.5V		1	40		1	60	μA
$I_{O(OFF)}$	Hi-Z state (82S103)[6]	V_{OUT} = 5.5V		1	40		1	60	μA
		V_{OUT} = 0.45V		-1	-40		-1	-60	
I_{OS}	Short circuit (82S103)[3,7]	V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = Max		120	170		120	180	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		8			8		
C_{OUT}	Output[6]	V_{OUT} = 2.0V		15			15		

AC ELECTRICAL CHARACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$
N82S102/103: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S102/103: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TO	FROM	N82S102/103			S82S102/103			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
	Progagation delay									ns
T_{IA}	Input	Output	Input		20	35		20	55	
T_{CE}	Chip enable	Output	Chip enable		15	30		15	45	
	Disable time									ns
T_{CD}	Chip disable	Output	Chip enable		15	30		15	45	

NOTES

1. All voltage values are with respect to network ground terminal.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Test each output one at a time.
4. Measured with a programmed logic condition for which the output under test is at a low logic level. Output sink current is supplied through a resistor to V_{CC}.
5. Measured with V_{IL} applied to $\overline{CE}$ and a logic high at the output.
6. Measured with V_{IH} applied to $\overline{CE}$.
7. Duration of short circuit should not exceed 1 second.
8. I_{CC} is measured with the chip enable input grounded, all other inputs at 4.5V and the outputs open.

FIELD PROGRAMMABLE LOGIC SEQUENCER (16×48×8)

82S104 (O.C.)/82S105 (T.S.)
82S104A (O.C.)/82S105A (T.S.)

INTEGRATED FUSE LOGIC
SERIES 28

DESCRIPTION

The 82S104 (open collector outputs) and the 82S105 (tri-state outputs) are bipolar, programmable state machines of the Mealy type. They contain logic AND-OR gate arrays with user programmable connections which control the inputs of on-chip State and Output registers. These consist respectively of 6 Q_P, and 8 Q_F edge triggered, clocked S/R flip-flops, with an asynchronous Preset option. All flip-flops are unconditionally preset to "1" during power turn on.

The AND array combines 16 external inputs $I_{0\text{-}15}$ with 6 internal inputs $P_{0\text{-}5}$ fed back from the State register to form up to 48 Transition terms (AND terms). All Transition terms can include True, False, or Don't Care states of the controlling variables, and are merged in the OR array to issue next-state and next-output commands to their respective registers on the Low to High transition of the Clock pulse. Both True and Complement Transition terms can be generated by optional use of the internal input variable (C) from the Complement array. Also, if desired, the Preset input can be converted to Output-$\overline{\text{Enable}}$ function, as an additional user programmable option.

Both devices are available in commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S104/105, F or N, and for the military temperature range (−55°C to +125°C) specify S82S104/105, F, I, G or R.

FEATURES

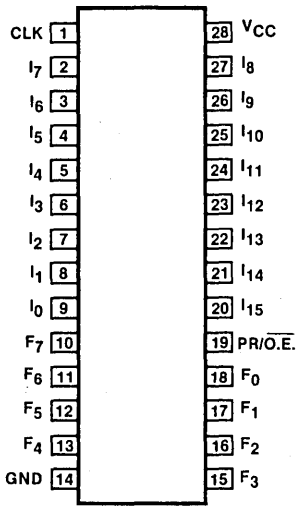
- Field programmable (Ni-Cr link)
- 16 input variables
- 8 output functions
- 48 transition terms
- 6-bit state register
- 8-bit output register
- Transition complement array
- Positive edge trigger clock
- Programmable asynchronous preset or output enable
- Power-on preset to all "1" of internal registers
- f(max) = 20MHz
- 650mW power dissipation (typical)
- TTL compatible
- Single +5V supply
- Open collector and tri-state versions

APPLICATIONS

- Interface protocols
- Sequence detectors
- Peripheral controllers
- Timing generators
- Sequential circuits
- Elevator controllers
- Security locking systems
- Counters
- Shift registers

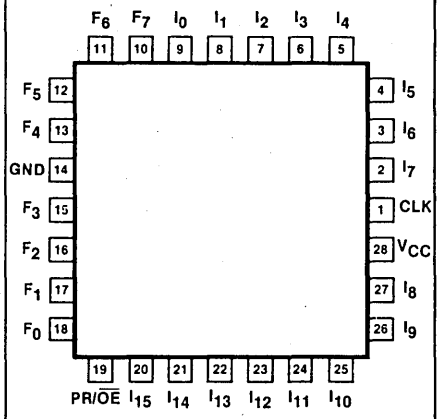
PIN CONFIGURATION

R,I,F,N PACKAGE*



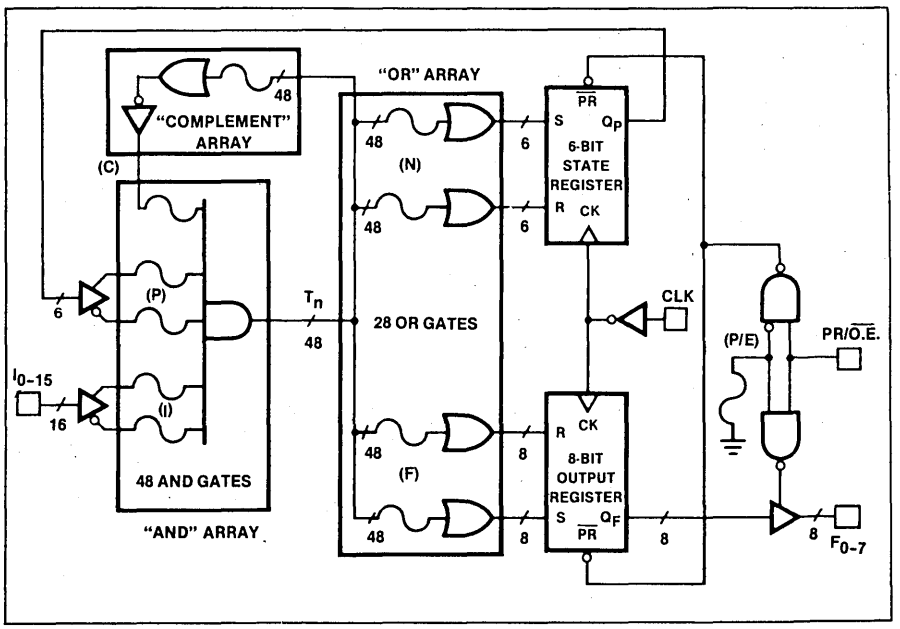
*F = Cerdip R = Flat Pack
N = Plastic I = Ceramic

G PACKAGE



G = Leadless

LOGIC DIAGRAM



Signetics

MEMORY

FIELD PROGRAMMABLE LOGIC SEQUENCER (16×48×8)

82S104 (O.C.)/82S105 (T.S.)
82S104A (O.C.)/82S105A (T.S.)

DC ELECTRICAL CHARACTERISTICS

N82S104/105, N82S104A/105A: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S104/105, S82S104A/105A: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS	N82S104A/105A N82S104/105			S82S104A/105A S82S104/105			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage[3]								V
V_{IH}	High	V_{CC} = Max	2			2			
V_{IL}	Low	V_{CC} = Min			0.85			0.8	
V_{IC}	Clamp[3,4]	V_{CC} = Min, I_{IN} = −18mA		−0.8	−1.2		−0.8	−1.2	
	Output voltage	V_{CC} = Min							V
V_{OH}	High (82S105)[3,5]	I_{OH} = −2mA	2.4			2.4			
V_{OL}	Low[3,6]	I_{OL} = 9.6mA		0.35	0.45		0.35	0.50	
	Input current								μA
I_{IH}	High	V_{IN} = 5.5V		<1	25		<1	50	
I_{IL}	Low	V_{IN} = 0.45V		−10	−100		−10	−150	
$I_{\overline{IL}}$	Low (CK input)	V_{IN} = 0.45V		−50	−250		−50	−350	
	Output current	V_{CC} = Max							
I_{OLK}	Leakage[7]	V_{OUT} = 5.5V		1	40		1	60	μA
$I_{O(OFF)}$	Hi-Z state (82S105)[7]	V_{OUT} = 5.5V		1	40		1	60	μA
		V_{OUT} = 0.45V		−1	−40		−1	−60	
I_{OS}	Short circuit (82S105)[4,8]	V_{OUT} = 0V	−20		−70	−15		−85	mA
I_{CC}	V_{CC} supply current[9]	V_{CC} = Max		120	180		120	185	mA
	Capacitance[7]	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		8			8		
C_{OUT}	Output	V_{OUT} = 2.0V		10			10		

NOTES

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device of these or any other condition above those indicated in the operation of the device specifications is not implied.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. All voltage values are with respect to network ground terminal.
4. Test one at a time.
5. Measured with V_{IL} applied to $\overline{O.E.}$ and a logic high stored, or with V_{IH} applied to PR.
6. Measured with a programmed logic condition for which the output is at a low logic level, and V_{IL} applied to PR/$\overline{O.E.}$ Output sink current is supplied thru a resistor to V_{CC}.
7. Measured with V_{IH} applied to PR/$\overline{O.E.}$.
8. Duration of short circuit should not exceed 1 second.
9. I_{CC} is measured with the PR/$\overline{O.E.}$ input grounded, all other inputs at 4.5V and the outputs open.

AC ELECTRICAL CHARACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$
N82S104/105: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

PARAMETER		TO	FROM	N82S104/105			N82S104/105A			UNIT
				Min	Typ[1]	Max	Min	Typ[1]	Max	
	Pulse width									ns
T_{CKH}	Clock[3] high	CK−	CK+	30	15		25	15		
T_{CKL}	Clock low	CK+	CK−	30	15		25	15		
T_{CKP1}	Period (w/o c-array)	CK+	CK+	90	40		60	40		
T_{CKP2}	Period (w/c-array)	CK+	CK+	120	60		80	50		
T_{PRH}	Preset pulse	PR+	PR−	25	15		25	15		
	Set-up time									ns
T_{IS1}	Input	CK+	Input±	60			40			
T_{IS2}	Input (through Complement array)	CK+	Input±	90			60			
T_{VS}	Power-on preset	CK−	V_{CC}+	0	−10		0	−10		
T_{PRS}	Preset	CK−	PR−	0	−10		0	−10		
	Hold time									ns
T_{IH}	Input	Input±	CK+	5	−10		5	−10		
	Propagation delay									ns
T_{CKO}	Clock	Output±	$\overline{CK}$+		15	30		15	20	
T_{OE}	Output enable	Output−	$\overline{O.E.}$−		20	30		20	30	
T_{OD}	Output disable	Output+	$\overline{O.E.}$+		20	30		20	30	
T_{PR}	Preset	Output+	PR+		18	30		18	30	
T_{PPR}	Power-on preset	Output+	V_{CC}+		0	10		0	10	
	Frequency of operation									MHz
f_{MAX}	w/o c-array					11.11			16.66	
f_{MAX}	w/c-array					8.33			12.5	

See Pages 3909-3910 for Product Selector Guides.

FIELD PROGRAMMABLE GATE ARRAY (18X12) 82S150 (O.C.)/82S151 (T.S.)

Preview

INTEGRATED FUSE LOGIC
SERIES 20

DESCRIPTION

The 82S150 and the 82S151 are single level logic elements, consisting of 12 AND gates with fusible link connections for programming I/O polarity, I/O direction and output enable control.

All gates are linked to 6 inputs (I) and 12 bidirectional I/O lines (B). These yield variable I/O gate configurations via 3 direction control gates (D), ranging from 18 inputs to 12 outputs.

On chip T/C buffers couple either True (I, B) or Complement ($\bar{I}$, $\bar{B}$) input polarities to each AND gate. The polarity of all gate outputs is individually programmable through a set of EX-OR gates for implementing AND/NAND logic functions. Alternately, if desired, OR/NOR logic functions can also be realized by programming for each gate the complement of its inputs and output (DeMorgan's Theorem).

The 82S150 and the 82S151 are field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

Both devices are available in a 20-pin slim line package. For the commercial temperature range (0°C to +75°C) specify N82S150/151 N or F. For the military temperature range (−55°C to +125°C) specify S82S150/151 F only.

FEATURES

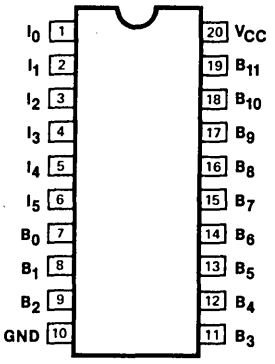
- Field Programmable (Ni-Cr link)
- 6 inputs
- 15 Product Terms:
  - 12 Logic Terms
  - 3 Control Terms
- 12 bidirectional I/O lines
- Active high or low outputs
- Programmable output enable
- Power dissipation: 650mW (typ)
- I/O propagation delay: 25ns (max)
- Input loading
  - N82S150/151: −100μA (max)
  - S82S150/151: −150μA (max)
- Output options
  - 82S150: open collector
  - 82S151: three-state
- TTL compatible

APPLICATIONS

- Random gating functions
- Address decoding
- Code detectors
- Memory mapped I/O
- Fault monitors
- I/O port decoders

PIN CONFIGURATION

F,N PACKAGES



F = Cerdip
N = Plastic

LOGIC FUNCTIONS

Typical Output Functions:

Active-High

$X = A \cdot \bar{B} \cdot C \cdot \ldots\ldots$

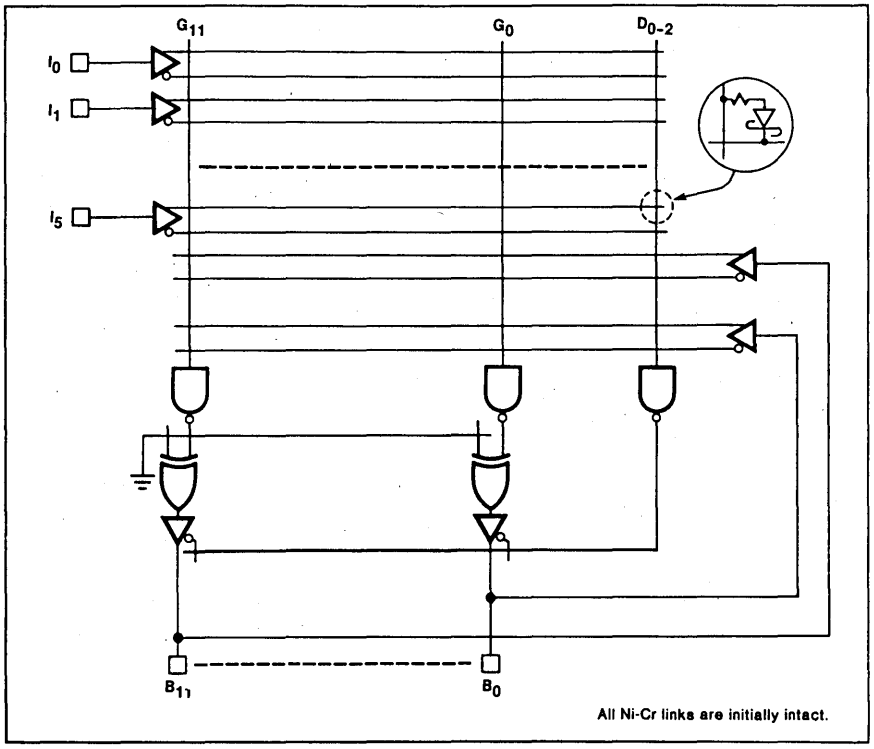
Active-Low

$X = A \cdot \bar{B} \cdot C \cdot \ldots\ldots$

$X = \bar{A} + B + \bar{C} + \ldots\ldots$

NOTES:
1. For each of the 12 outputs, either function X (active-high) or $\bar{X}$ (active-low) is available, but not both. The desired output polarity is programmed via the EX-OR gates.
2. X, A, B, C, etc. are user defined connections to fixed inputs (I) and bidirectional pins (B).

FUNCTIONAL DIAGRAM



All Ni-Cr links are initially intact.

See Pages 3909-3910 for Product Selector Guides.

FIELD PROGRAMMABLE GATE ARRAY (18X12) 82S150 (O.C.)/82S151 (T.S.)

Preview

INTEGRATED FUSE LOGIC
SERIES 20

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING Min	RATING Max	UNIT
V_{CC}	Supply voltage		+7	Vdc
V_{IN}	Input voltage		+5.5	Vdc
V_{OUT}	Output voltage		+5.5	Vdc
I_{IN}	Input currents	−30	+30	mA
I_{OUT}	Output currents		+100	mA
	Temperature range			C°
T_A	Operating			
	N82S150/151	0	+75	
	S82S150/151	−55	+125	
T_{STG}	Storage	−65	+150	

THERMAL RATINGS

TEMPERATURE	Military	Commercial
Maximum junction	175°C	150°C
Maximum ambient	125°C	75°C
Allowable thermal rise ambient to junction	50°C	75°C

DC ELECTRICAL CHACTERISTICS

N82S150/151: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S150/151: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITION[1]	N82S150/151 Min	N82S150/151 Typ[2]	N82S150/151 Max	S82150/151 Min	S82150/151 Typ[2]	S82150/151 Max	UNIT
	Input voltage[3]								V
V_{IL}	Low	V_{CC} = Min			.85			.80	
V_{IH}	High	V_{CC} = Max	2.0			2.0			
V_{IC}	Clamp[3,4]	V_{CC} = Min, I in = − 18mA		−.8	−1.2		−.8	−1.2	
	Output voltage[3]	V_{CC} = Min							V
V_{OL}	Low	I_{OL} = 10mA			.5				
V_{OL}	Low	I_{OL} = 8mA						.5	
V_{OH}	High	I_{OH} = −2mA	2.4			2.4			
	Input Current								μA
I_{IL}	Low	V_{IN} = 0.45V			−100			−150	
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output Current	V_{CC} = max							
I_{OLK}	Leakage (82S150)	V_{OUT} = 5.5V			40			60	μA
$I_{O(OFF)}$	Hi-Z state (82S151)	V_{OUT} = 5.5V			40			60	μA
		V_{OUT} = .45V			−40			−60	
I_{OS}	Short circuit (82S151)[4,5]	V_{OUT} = 0V	−20		−70	−15		−85	mA
I_{CC}	V_{CC} supply current	V_{CC} = max		130	155		130	155	mA
	Capacitance	V_{CC} = 5V							pF
C_{IN}	Input	V_{IN} = 2.0V		8			8		
C_B	I/O	V_B = 2.0V		15			15		

AC ELECTRICAL CHACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1K\Omega$
N82S150/151: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S150/151: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TO	FROM	TEST CONDITIONS	N82S150/151 Min	N82S150/151 Typ[2]	N82S150/151 Max	S82S150/151 Min	S82S150/151 Typ[2]	S82S150/151 Max	UNIT
T_{PD}	Progagation delay	Output ±	Input ±	C_L = 30pF		20	25		20		ns
T_{OE}	Output enable	Output−	Input ±			20	25		20		ns
T_{OD}	Output disable[7]	Output+	Input ±	C_L = 5pF		20	25		20		

NOTES
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device of these or any other condition above those indicated in the operation of the device specifications is not implied.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. All voltage values are with respect to network ground terminal.
4. Test one at a time.
5. Duration of short circuit should not exceed 1 second.
6. Measured at $V_T = V_{OL} + 0.5V$.

FIELD PROGRAMMABLE LOGIC ARRAY (18X32X10)

82S152 (O.C.)/82S153 (T.S.) 82S152A (O.C.)/82S153A (T.S.)

INTEGRATED FUSE LOGIC
SERIES 20

DESCRIPTION

The 82S152 and 82S153 are two-level logic elements, consisting of 32 AND gates and 10 OR gates with fusible link connections for programming I/O polarity and direction.

All AND gates are linked to 8 inputs (I) and 10 bidirectional I/O lines (B). These yield variable I/O gate configurations via 10 direction control gates (D), ranging from 18 inputs to 10 outputs.

On chip T/C buffers couple either True (I, B) or Complement ($\overline{I}$, $\overline{B}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. Their output polarity, in turn, is individually programmable through a set of EX-OR gates for inplementing AND-OR or AND-NOR logic functions.

The 82S152 and the 82S153 are field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

Both devices are available in a 20 pin slim line package. For the commercial temperature range (0°C to +75°C) specify N82S152/153 N or F and N82S152A/153A N or F. For the military temperature range (−55°C to +125°C) specify S82S152/153 F only and S82S152A/153A F only.

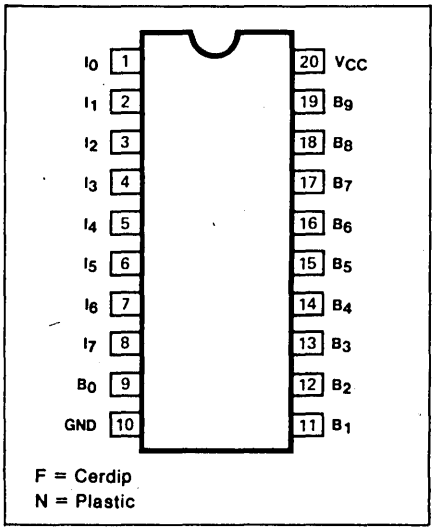
FEATURES

- Field programmable (Ni-Cr links)
- 8 Inputs
- 32 AND gates
- 10 OR gates
- 10 bidirectional I/O lines
- Active high or low outputs
- 42 Product Terms:
  - 32 Logic terms
  - 10 Control terms
- I/O propagation delay:
  - N82S152/153: 40ns (max)
  - N82S152A/153A: 30ns (max)
  - S82S152/153: 60ns (max)
  - S82S152A/153A: 45ns (max)
- Input loading
  - N82S152/153: −100μA (max)
  - S82S152/153: −150μA (max)
- Power dissipation:
  - 650mW (typ)
- Output options:
  - 82S152: open collector
  - 82S153: tri-state
- TTL compatible

APPLICATIONS

- Random logic
- Code converters
- Fault detectors
- Function generators
- Address mapping
- Multiplexing

PIN CONFIGURATION



F = Cerdip
N = Plastic

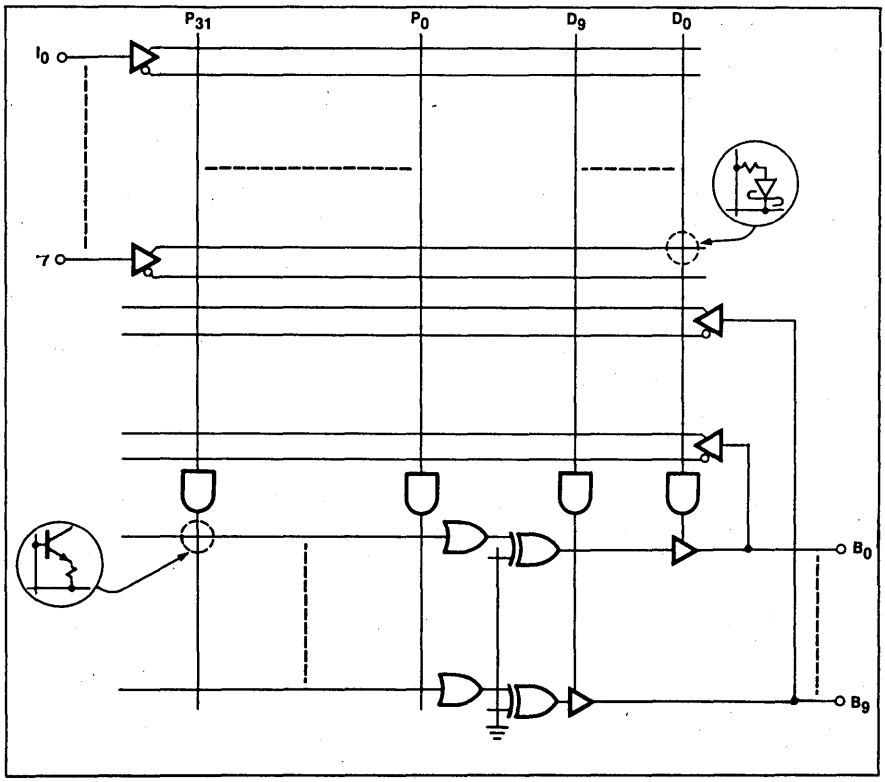
LOGIC FUNCTION

Typical product term:
$Pn = A \cdot \overline{B} \cdot C \cdot D \cdot \ldots\ldots$
Typical logic function:
At Output Polarity = H
$X = P0 + P1 + P2 \ldots\ldots$

At Output Polarity = $\underline{L}$
$X = \overline{P0 + P1 + P2} + \ldots\ldots$
$X = \overline{P0} \cdot \overline{P1} \cdot \overline{P2} \ldots\ldots$

NOTES:
1. For each of the 10 outputs, either function X (active-high) or $\overline{X}$ (active-low) is available, but not both. The desired output polarity is programmed via link (L).
2. X, A, B, C, etc. are user defined connections to fixed inputs (I) and bidirectional pins (B).

FUNCTIONAL DIAGRAM



See Pages 3909-3910 for Product Selector Guides.

FIELD PROGRAMMABLE LOGIC ARRAY (18×32×10)

82S152 (O.C.)/82S153 (T.S.)
82S152A (O.C.)/82S153A (T.S.)

INTEGRATED FUSE LOGIC
SERIES 20

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING Min	RATING Max	UNIT
V_{CC}	Supply voltage		+7	Vdc
V_{IN}	Input voltage		+5.5	Vdc
V_{OUT}	Output voltage		+5.5	Vdc
I_{IN}	Input currents	−30	+30	mA
I_{OUT}	Output currents		+100	mA
	Temperature range			C°
T_A	Operating			
	N82S152/153/152A/153A	0	+75	
	S82S152/153/152A/153A	−55	+125	
T_{STG}	Storage	−65	+150	

THERMAL RATINGS

TEMPERATURE	Military	Commercial
Maximum junction	175°C	150°C
Maximum ambient	125°C	75°C
Allowable thermal rise ambient to junction	50°C	75°C

DC ELECTRICAL CHARACTERISTICS

N82S152/153, N82S152A/153A: $0°C \le T_A \le +75°C$, $4.75 \le V_{CC} \le 5.25V$
S82S152/153, S82S152A/153A: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITION	N82S152/153 Min	N82S152/153 Typ	N82S152/153 Max	S82S152/153 Min	S82S152/153 Typ	S82S152/153 Max	UNIT
	Input voltage								V
V_{IL}	Low	V_{CC} = min			.85			.80	
V_{IH}	High	V_{CC} = max	2.0			2.0			
V_{IC}	Clamp	V_{CC} = min, Iin = −18mA		−.8	−1.2		−.8	−1.2	
	Output voltage	V_{CC} = min							V
V_{OL}	Low	I_{OL} = 15mA			.5				
V_{OL}	Low	I_{OL} = 12mA						.5	
V_{OH}	High	I_{OH} = −2mA	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			−100			−150	
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output current	V_{CC} = max							
I_{OLK}	Leakage (82S152)	V_{OUT} = 5.5V			40			60	μA
$I_{O(OFF)}$	Hi-Z state (82S153)	V_{OUT} = 5.5V			40			60	μA
		V_{OUT} = .45V			−40			−60	
I_{OS}	Short circuit (82S153)	V_{OUT} = 0V	−20		−70	−15		−85	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = max		130	155		130	165	mA
	Capacitance	V_{CC} = 5V							pF
C_{IN}	Input	V_{IN} = 2.0V		8			8		
C_B	I/O	V_B = 2.0V		15			15		

AC ELECTRICAL CHACTERISTICS

$R_A = 470\Omega$, $R_2 = 1K\Omega$
N82S152/153, N82S152A/153A: $0°C \le T_A \le +75°C$, $4.75 \le V_{CC} \le 5.25V$
S82S152/153, S82S152A/153A: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

	PARAMETER	TO	FROM	TEST CONDITIONS	N82S152/153 Min	N82S152/153 Typ	N82S152/153 Max	S82S152/153 Min	S82S152/153 Typ	S82S152/153 Max	UNIT
T_{PD}	Progagation delay	Output ±	Input ±	C_L = 30pF		30	40		30	55	ns
T_{OE}	Output enable	Output−	Input ±			25	35		25	45	
T_{OD}	Output disable	Output+	Input ±	C_L = 5pF		25	35		25	45	ns

	PARAMETER	TO	FROM	TEST CONDITIONS	N82S152A/153A Min	N82S152A/153A Typ	N82S152A/153A Max	S82S152A/153A Min	S82S152A/153A Typ	S82S152A/153A Max	UNIT
T_{PD}	Progagation delay	Output ±	Input ±	C_L = 30pF		20	30		20	45	ns
T_{OE}	Output enable	Output−	Input ±			20	30		20	40	
T_{OD}	Output disable	Output+	Input ±	C_L = 5pF		20	30		20	40	ns

Signetics

MEMORY

See Pages 3909-3910 for Product Selector Guides.

FIELD PROGRAMMABLE LOGIC SEQUENCER (16X32X12)

82S154/6/8 (O.C.)/82S155/7/9 (T.S.)

Preview

INTEGRATED FUSE LOGIC
SERIES 20

DESCRIPTION

The 82S154/155/156/157/158/159 are Open Collector and Tri-state registered logic elements combining AND/OR gate arrays with clocked J/K flip-flops, dynamically convertible to D-type via a "foldback" inverting buffer and control gate F_C. They all have similar organization, featuring respectively 4, 6, or 8 registered I/O outputs (F), in conjunction with 8, 6, or 4 bidirectional I/O lines (B). These yield variable I/O gate and register configurations via control gates (D, L) ranging from 16 inputs to 12 outputs.

The AND/OR arrays consist of 32 logic AND gates, 13 control AND gates, and 21 OR gates with fusible link connections for programming I/O polarity and direction. All AND gates are linked to 4 inputs (I), bidirectional I/O lines (B), internal flip-flop outputs (Q), and Complement Array output ($\overline{C}$). The Complement Array consists of a NOR gate optionally linked to all AND gates for generating and propagating complementary AND terms.

On chip I/C buffers couple either True (I, B, Q) or Complement ($\overline{I}$, $\overline{B}$, $\overline{Q}$, $\overline{C}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. One group of OR gates drives bidirectional I/O lines (B), whose output polarity is individually programmable through a set of EX-OR gates for implementing AND-OR or AND-NOR logic functions. Another group drives the J-K inputs of all flip-flops, as well as asynchronous Preset and Reset lines (P, R), (except the 82S158/159, where AND functions are provided).

All flip-flops are positive edge trigger and can be used as input, output, or I/O (for interfacing with a bidirectional data bus) in conjunction with load control gates (L), steering inputs (I), (B), (Q) and programmable output select lines (E).

The 82SXXX are field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

All devices are available in a 20-pin, slim line package. For the commercial temperature range (0°C to +75°C) specify N82SXXX N or F. For the military temperature range (−55°C to +125°C) specify S82SXXX F only.

FEATURES

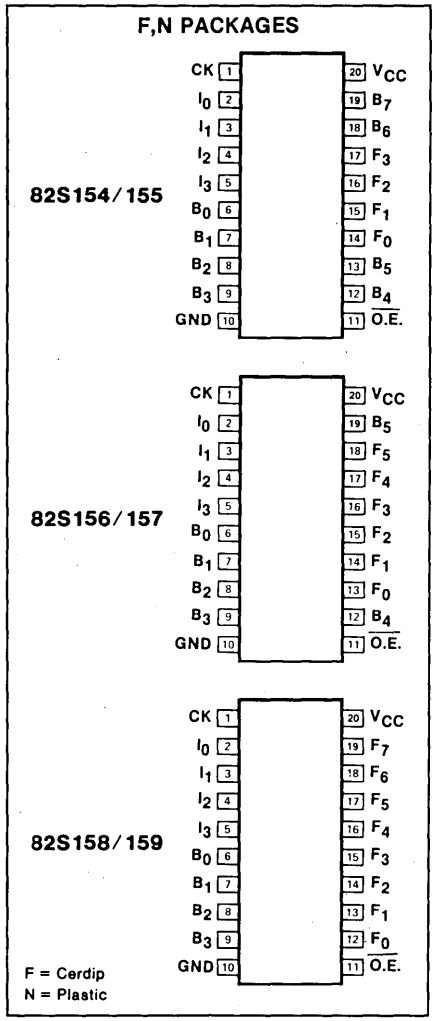
- **Field programmable (Ni-Cr link)**
- **4 Inputs**
- **13 control gates**
- **32 AND gates**
- **21 OR gates**
- **45 product terms:**
  32 logic terms
  13 control terms
- **Bidirectional I/O lines:** 82S154/155—8
  82S156/157—6
  82S158/159—4
- **Bidirectional Registers:** 82S154/155—4
  82S156/157—6
  82S158/159—8
- **J/K, T, or D-type flip-flops**
- **Asynchronous Preset/Reset**
- **Complement Array**
- **Active high or low outputs**
- **Programmable $\overline{O.E.}$ control**
- **Positive edge trigger clock**
- **Power-on reset of all flip-flopw (F_n = "1")**
- **Clock frequency:** N82SXXX: 15 MHz (max)
  S82SXXX: MHz (max)
- **Input loading:** N82SXXX: −100μA (max)
  S82SXXX: −150μA (max)
- **Power dissipation: 650mW (typ)**
- **TTL Compatible**

APPLICATIONS

- **Random sequential logic**
- **Synchronous up/down counters**
- **Shift registers**
- **Bidirectional data buffers**
- **Timing function generators**
- **System controllers/synchronizers**
- **Priority encoder/registers**

PIN CONFIGURATION

F,N PACKAGES



F = Cerdip
N = Plastic

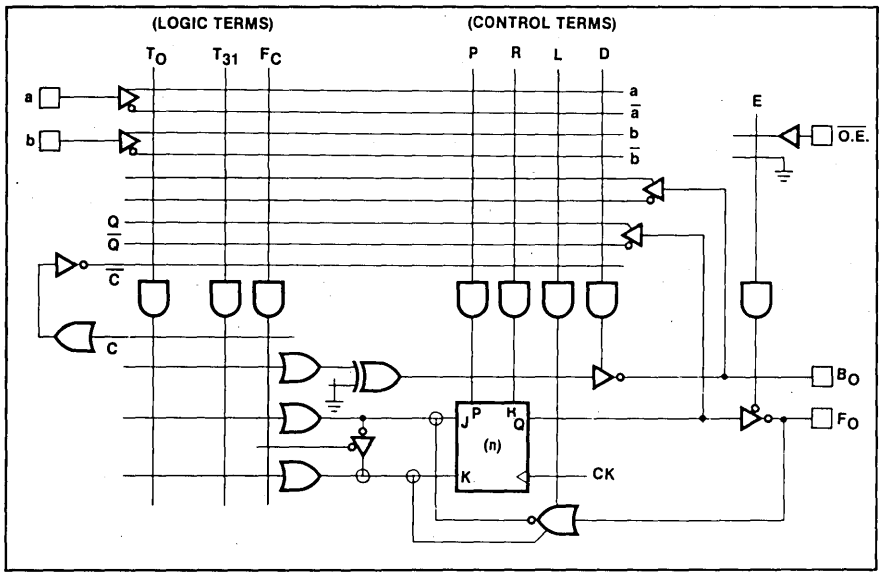
FLIP-FLOP TRUTH TABLE

V_{CC}	$\overline{O.E.}$	L	CK	P	R	J	K	Q	F
	H								H/HI-Z
↑	L	X	X	L	X	X	X	L	H
+5	L	X	X	H	L	X	X	H	L
	L	X	X	L	H	X	X	L	H
	L	L	↑	L	L	L	L	Q	$\overline{Q}$
	L	L	↑	L	L	L	H	L	H
	L	L	↑	L	L	H	L	H	L
	L	L	↑	L	L	H	H	$\overline{Q}$	Q
	H	H	↑	L	L	L	H	L	H*
	H	H	↑	L	L	H	L	H	L*
	+10V	X	↑	X	X	L	H	L	H**
		X	↑	X	X	H	L	H	L**

NOTES

1. Positive Logic:
   $J/K = T_0 + T_1 + T_2 \ldots\ldots T_{47}$
   $T_n = \overline{C} \bullet (I_0 \bullet I_1 \bullet I_2 \ldots) \bullet (Q_0 \bullet Q_1 \ldots) \bullet (B_0 \bullet B_1 \bullet \ldots)$
2. ↑ denotes transition from Low to High level.
3. X = Don't Care
4. * = Forced at F_n pin for loading J/K flip-flop in I/O mode. L must be enabled, and other active T_n disabled via steering input(s) I, B, or Q.
5. At P = R = H, Q = H. The final state of Q depends on which is released first.
6. ** = Forced at F_n pin to load J/K flip-flop independent of program code (Diagnostic mode).

FUNCTIONAL DIAGRAM



FIELD PROGRAMMABLE LOGIC SEQUENCER (16X32X12)

82S154/6/8 (O.C.)/82S155/7/9 (T.S.)

Preview

INTEGRATED FUSE LOGIC
SERIES 20

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING Min	RATING Max	UNIT
V_{CC}	Supply voltage		+7	Vdc
V_{IN}	Input voltage		+5.5	Vdc
V_{OUT}	Output voltage		+5.5	Vdc
I_{IN}	Input currents	−30	+30	mA
I_{OUT}	Output currents		+100	mA
	Temperature range			°C
T_A	Operating			
	N82S154/5/6/7/8/9	0	+75	
	S82S154/5/6/7/8/9	−55	+125	
T_{STG}	Storage	−65	+150	

THERMAL RATINGS

TEMPERATURE	MILITARY	COMMERCIAL
Maximum junction	175°C	150°C
Maximum ambient	125°C	75°C
Allowable thermal rise ambient to junction	50°C	75°C

DC ELECTRICAL CHARACTERISTICS

N82S154/5/6/7/8/9: $0° \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S154/5/6/7/8/9: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS	N82S154/5/6/7/8/9 Min	N82S154/5/6/7/8/9 Typ[2]	N82S154/5/6/7/8/9 Max	S82S154/5/6/7/8/9 Min	S82S154/5/6/7/8/9 Typ[2]	S82S154/5/6/7/8/9 Max	UNIT
	Input voltage[3]								V
V_{IH}	High	V_{CC} = Max	2			2			
V_{IL}	Low	V_{CC} = Min			0.85			0.8	
V_{IC}	Clamp	V_{CC} = Min, I_{IN} = −18mA		−0.8	−1.2		−0.8	−1.2	
	Output voltage[3]	V_{CC} = Min							V
V_{OH}	High (82S155/7/9)	I_{OH} = −2mA	2.4			2.4			
V_{OL}	Low	I_{OL} = 10mA		0.35	0.5				
V_{OL}	Low	I_{OL} = 10mA					0.35	0.5	
	Input current								μA
I_{IH}	High	V_{IN} = 5.5V		<1	40		<1	50	
I_{IL}	Low	V_{IN} = 0.45V		−10	−100		−10	−150	
I_{IL}	Low (CK input)	V_{IN} = 0.45V		−50	−250		−50	−350	
	Output current	V_{CC} = Max							
I_{OLK}	Leakage[5]	V_{OUT} = 5.5V		1	40		1	60	μA
$I_{O(OFF)}$	Hi-Z state (82S155/7/9)[7]	V_{OUT} = 5.5V		1	40		1	60	μA
		V_{OUT} = 0.45V		−1	−40		−1	−60	
I_{OS}	Short circuit (82S155/7/9)[4,6]	V_{OUT} = 0V	−20		−70	−15		−85	mA
I_{CC}	V_{CC} supply current[7]	V_{CC} = Max		130	155		130	155	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		8			8		
C_{OUT}	Output	V_{OUT} = 2.0V		15			15		

NOTES
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device of these or any other condition above those indicated in the operation of the device specifications is not implied.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. All voltage values are with respect to network ground terminal.
4. Test one at a time.
5. Measured with V_{IH} applied to $\overline{O.E.}$
6. Duration of short circuit should not exceed 1 second.
7. I_{CC} is measured with the $\overline{O.E.}$ input grounded, all other inputs at 4.5V and the outputs open.

FIELD PROGRAMMABLE LOGIC SEQUENCER (16X32X12)

82S154/6/8 (O.C.)/82S155/7/9 (T.S.)

Preview

INTEGRATED FUSE LOGIC
SERIES 20

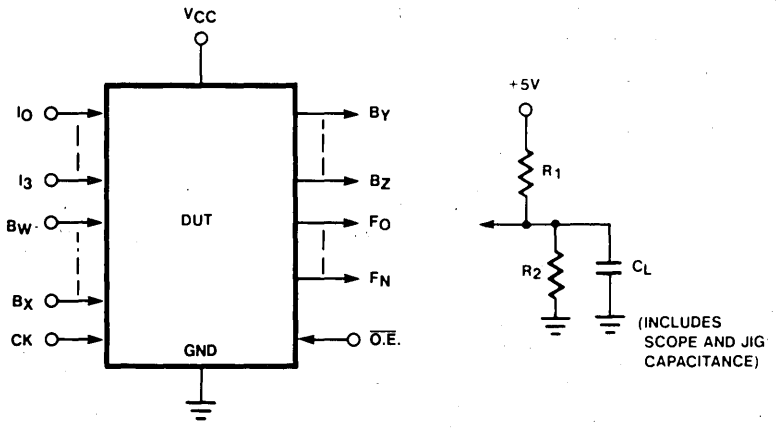
AC ELECTRICAL CHARACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1k\Omega$
N82S154/5/6/7/8/9: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S82S154/5/6/7/8/9: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

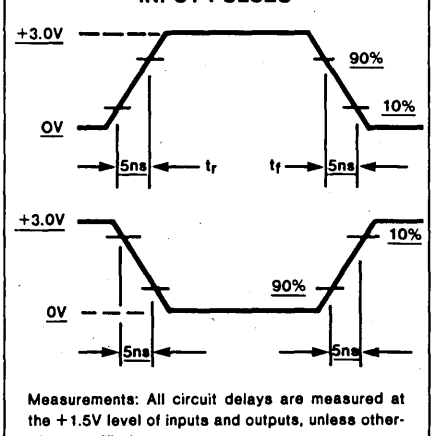
	PARAMETER	TO	FROM	TEST CONDITIONS	N82S154/5/6/7/8/9/ Min	N82S154/5/6/7/8/9/ Typ[1]	N82S154/5/6/7/8/9/ Max	S82S154/5/6/7/8/9 Min	S82S154/5/6/7/8/9 Typ[1]	S82S154/5/6/7/8/9 Max	UNIT
	Pulse width										ns
T_{CKH}	Clock[2] high	CK−	CK+		25	20			20		
T_{CKL}	Clock low	CK+	CK−		25	20			20		
T_{CKP}	Period	CK+	CK+		65	50			50		
T_{PRH}	Preset/Reset pulse	(I,B)+	(I,B)−		25	20			20		
	Set up time										ns
T_{IS1}	Input	CK+	(I,B)±	C_L = 30pF	35	30			30		
T_{IS2}	Input (through F_n)	CK+	F±		10	5			5		
T_{IS3}	Input (through Complement array)[4]	CK+	(I,B)±		45	40			40		
	Hold time										ns
T_{IH1}	Input	CK+	(I,B)±			−10	0		−10		
T_{IH2}		CK+	F±			−5	0		−5		
	Propagation delay										ns
T_{CKO}	Clock	F±	CK+			25	30		25		
T_{OE1}	Output enable	F−	$\overline{O.E.}$−			20	25		20		
T_{OD1}	Output disable[3]	F+	$\overline{O.E.}$+	C_L = 5pF		20	25		20		
T_{PD}	Output	B±	(I,B)±	C_L = 30pF		35	40		35		
T_{OE2}	Output enable	B±	(I,B)+			35	40		35		
T_{OD2}	Output disable[3]	B+	(I,B)−	C_L = 5pF		35	40		35		
T_{PRO}	Preset/Reset	F±	(I,B)+	C_L = 30pF		50	65		50		
T_{PPR}	Power-on preset	F−	V_{CC}+			0	10		0		

NOTE
1. All typical values are at V_{CC} = 5V, T_A = 25°C.
2. To prevent spurious clocking, clock rise time (10%-90%) ≤ 10ns.
3. Measured at $V_T = V_{OL}$ + 0.5 V.
4. When using the Complement Array T_{CKP} = 75ns (min).

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



Measurements: All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

See Pages 3909-3910 for Product Selector Guides.

2304-BIT BIPOLAR RAM (256×9) 82S212A (T.S.)

DESCRIPTION

The organization of the 82S212A allows byte wide storage of data, including parity. Where parity is not required, the ninth bit can be used as a tag for each word stored. The 82S212A is ideal for scratch-pad, pushdown stacks, buffer memories, and other internal memory applications in which space and performance requirements dictate a wide data path in favor of word depth.

The 82S212A data inputs and outputs are common (common I/O) with separate output disable (OD) line that allows ease of read/write operations using a common bus.

The 82S212A is available in the commercial temperature range. For the commercial temperature range (0°C to 75°C) specify N82S212AF or N.

FEATURES

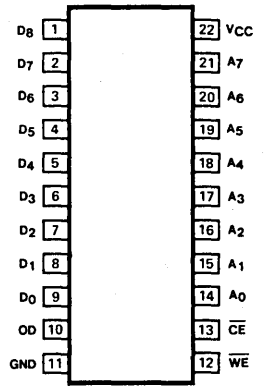
- **Address access time:**
  N82S212A: 35ns max
- **Power dissipation: 0.3mW/bit**
- **Tri-state outputs**
- **Schottky clamped TTL**

APPLICATIONS

- **Cache memory**
- **Buffer storage**
- **Writable control store**

PIN CONFIGURATION

N, F PACKAGE*



*F = Cerdip
N = Plastic

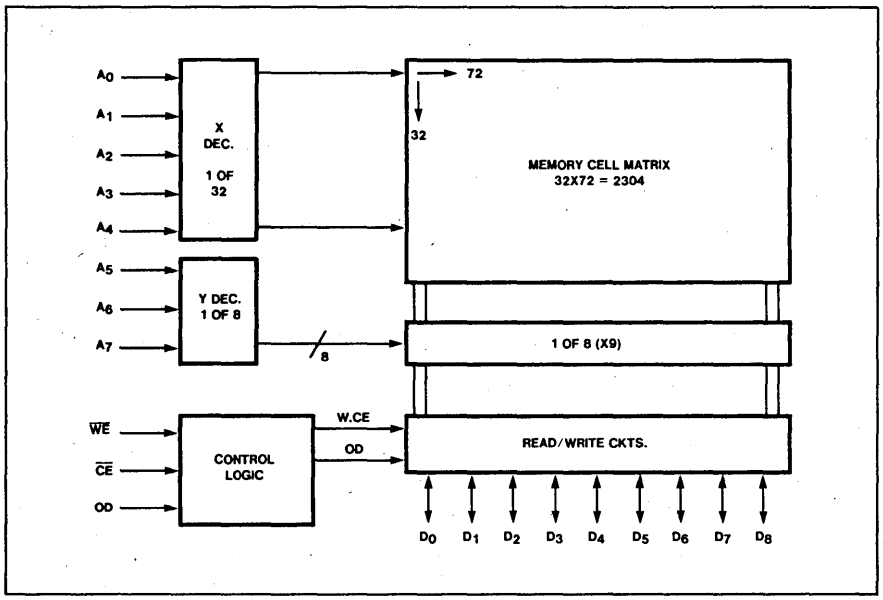
TOP VIEW

TRUTH TABLE

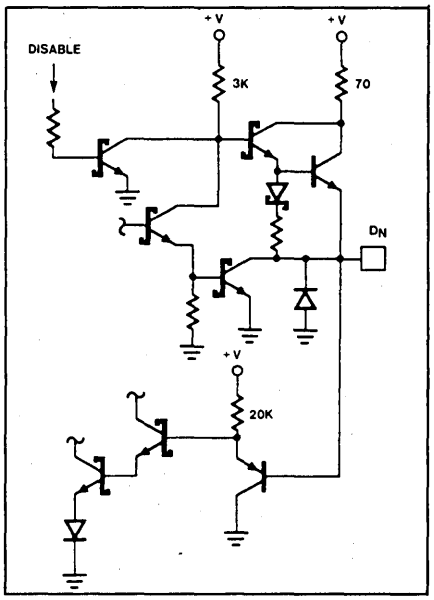
MODE	$\overline{WE}$	$\overline{CE}$	OD	D_N IN/OUT
Disable output	X	X	1	High Z
Disable R/W	X	1	X	High Z
Write	0	0	1	Data in
Read	1	0	0	Data out

X = Don't care

BLOCK DIAGRAM



TYPICAL I/O STRUCTURE



ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
V_O	Off-state output voltage	+5.5	Vdc
	Temperature range		°C
T_A	Operating	0 to +75	
T_{STG}	Storage	−65 to +150	

2304-BIT BIPOLAR RAM (256×9) 82S212A (T.S.)

DC ELECTRICAL CHARACTERISTICS[1] N82S212A: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER		TEST CONDITIONS	N82S212A			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IL}	Low	V_{CC} = Min			.85	
V_{IH}	High	V_{CC} = Max	2.0			
V_{IC}	Clamp[2]	V_{CC} = Min, I_{IN} = −12mA			−1.5	
	Output voltage					V
V_{OL}	Low[3]	V_{CC} = Min, I_{OL} = 8.0mA			0.5	
	Input current					μA
I_{IL}	Low	V_{IN} = 0.45V			−100	
I_{IH}	High	V_{IN} = 5.5V			25	
	Output current					
$I_{O(OFF)}$	Hi-Z state	$\overline{CE}$ = High or OD = High, V_{OUT} = 5.5V			40	μA
		$\overline{CE}$ = High or OD = High, V_{OUT} = 0.5V			−100	
I_{OS}	Short circuit[4, 5]	$\overline{CE}$ = OD = Low, V_{OUT} = 0V	−20		−70	mA
I_{CC}	V_{CC} supply current[5]	V_{CC} = Max		135	185	mA
	Capacitance	V_{CC} = 5.0V				pF
C_{IN}	Input	V_{IN} = 2.0V		5		
C_{OUT}	Output	V_{OUT} = 2.0V		8		

AC ELECTRICAL CHARACTERISTICS[1] R_1 = 470Ω, R_2 = 1kΩ, C_L = 30pF
N82S212A: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER		TO	FROM	N82S212A			UNIT
				Min	Typ[3]	Max	
	Access time						ns
T_{AA}	Address	Output	Address			35	
	Enable time						ns
T_{OE}	Output	Output	OD	5	25		
T_{CE}	Output	Output	Chip enable			25	
	Disable time						ns
T_{OD}	Output	Output	OD			25	
T_{CD}	Output	Output	Chip enable			25	
	Pulse width						ns
T_{WP}	Write			25			
T_{WSC}	Setup time	Write	Chip enable	5			
T_{WHD}	Hold time	Chip enable	Write	5			
T_{WSD}	Setup time	Write	Data	25			
T_{WHD}	Hold Time	Data	Write	5			
T_{WSA}	Setup time	Write	Address	5			
T_{WHA}	Hold time	Address	Write	5			
T_{SO}	Setup time (from disabled state)	Chip enable	OD	5			
T_{HO}	Hold time	OD	Chip enable	5			

NOTES
1. The operating embient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2 minute warmup.
2. All voltages are with respect to network ground terminal.
3. All typical values are at V_{CC} = 5V, T_A = 25°C.
4. Measured on one pin at a time.
5. Duration of I_{OS} test should not exceed one second.

See Pages 3909-3910 for Product Selector Guides.

4096-BIT BIPOLAR PROM (1024×4) 82S137A/82S137B (T.S.)

DESCRIPTION

The 82S137 is field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The 82S137 is supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

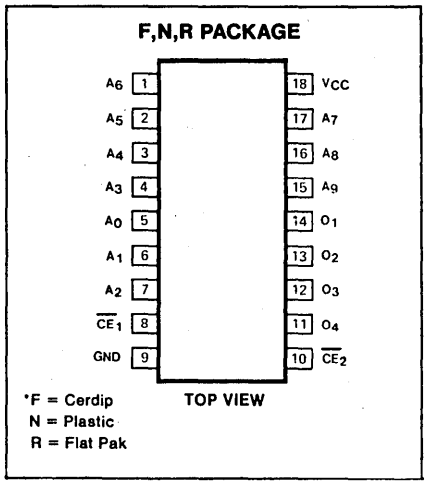
These devices include on-chip decoding and 2 chip enable inputs for ease of memory expansion. They feature tri-state outputs for optimization of word expansion in bused organizations.

The 82S137 device is available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S137AF or N, or N82S137BF or N, and for the military temperature range (−55°C to +125°C) specify S82S137AF or R.

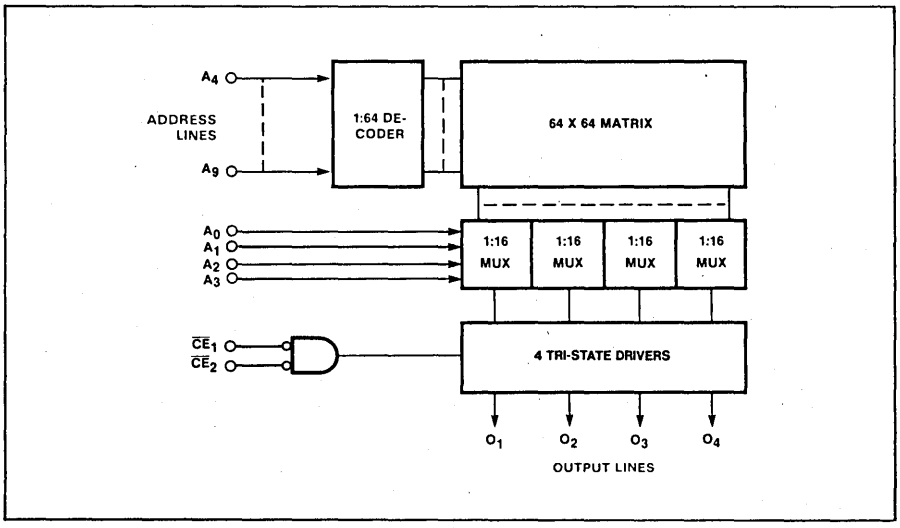
FEATURES

- **Address access time:**
  - **N82S137A: 45ns max**
  - **N82S137B: 35ns max**
  - **S82S137A: 70ns max**
- **Power dissipation: 13mW/bit typ**
- **Input loading:**
  - **N82S137: −100μA max**
  - **S82S137: −150μA max**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_O	Off-state	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S137	0 to +75	
	S82S137	−55 to +125	
T_{STG}	Storage	−65 to +150	

4096-BIT BIPOLAR PROM (1024×4) 82S137A/82S137B (T.S.)

DC ELECTRICAL CHARACTERISTICS

N82S137A/N82S137B: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S137A: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS[1,2]	N82S137A/N82S137B			S82S137A			UNIT
			Min	Typ[5]	Max	Min	Typ	Max	
	Input voltage								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	$I_{IN} = -18mA$		−0.8	−1.2			−1.2	
	Output voltage	$\overline{CE}_{1,2}$ = Low							V
V_{OL}	Low	I_{OUT} = 16mA			0.45			0.5	
V_{OH}	High	$I_{OUT} = -2mA$	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			−100			−150	
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output current								
$I_{O(OFF)}$	Hi-Z state	$\overline{CE}_{1,2}$ = High, V_{OUT} = 0.5V			40			60	μA
		$\overline{CE}_{1,2}$ = High, V_{OUT} = 5.5V			−40			−60	μA
I_{OS}	Short circuit[3]	$\overline{CE}_{1,2}$ = Low, V_{OUT} = 0V, Stored High			40			60	
			−20		−70	−15		−85	mA
I_{CC}	V_{CC} supply current			85	140			150	mA
	Capacitance	$\overline{CE}_{1,2}$ = High, V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

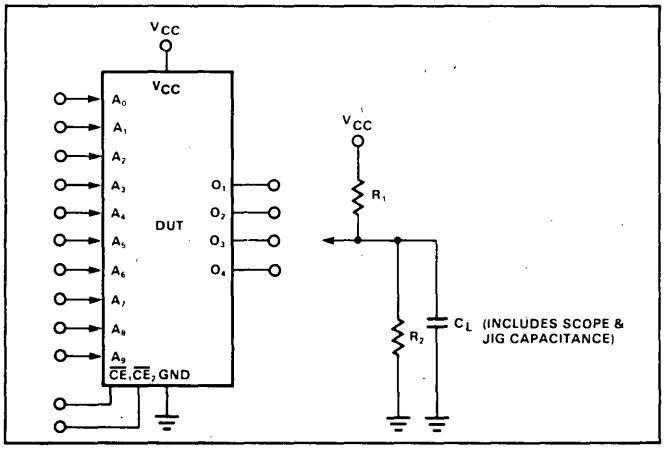
AC ELECTRICAL CHARACTERISTICS

$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$
N82S137A/N82S137B: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S137A: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

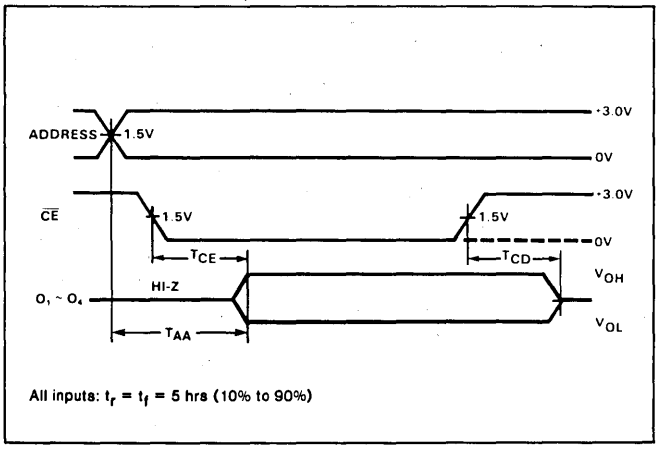
PARAMETER		TO	FROM	N82S137A			N82S137B			S82S137A			UNIT
				Min	Typ[5]	Max	Min	Typ	Max	Min	Typ	Max	
T_{AA}[4]	Access time	Output	Address		35	45		30	35			70	ns
T_{CE}		Output	Chip enable		15	30			25			40	
T_{CD}	Disable time	Output	Chip disable		15	30			25			40	ns

NOTES
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μsec.
5. Typical values are at $V_{CC} = 5V$, $T_A = 25°C$.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



See Pages 3909-3910 for Product Selector Guides.

4096-BIT BIPOLAR PROM (512×8) 82S147A (T.S.)

DESCRIPTION

The 82S147A is field-programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The standard devices are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

The 82S147A includes on-chip decoding and one chip enable input for ease of memory expansion, and features tri-state outputs for optimization of word expansion in bused organizations.

The 82S147A device is available in the commercial temperature range (0°C to +75°C), and is specified as N82S147A, F, N.

FEATURES

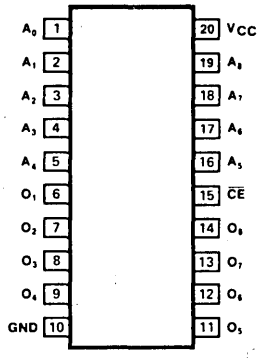
- **Address access time: 45ns max**
- **Power dissipation: 853mW max**
- **Input loading: -100μA max**
- **One chip enable input**
- **On chip address decoding**
- **No separate fusing pins**
- **Fully TTL compatible**

APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION

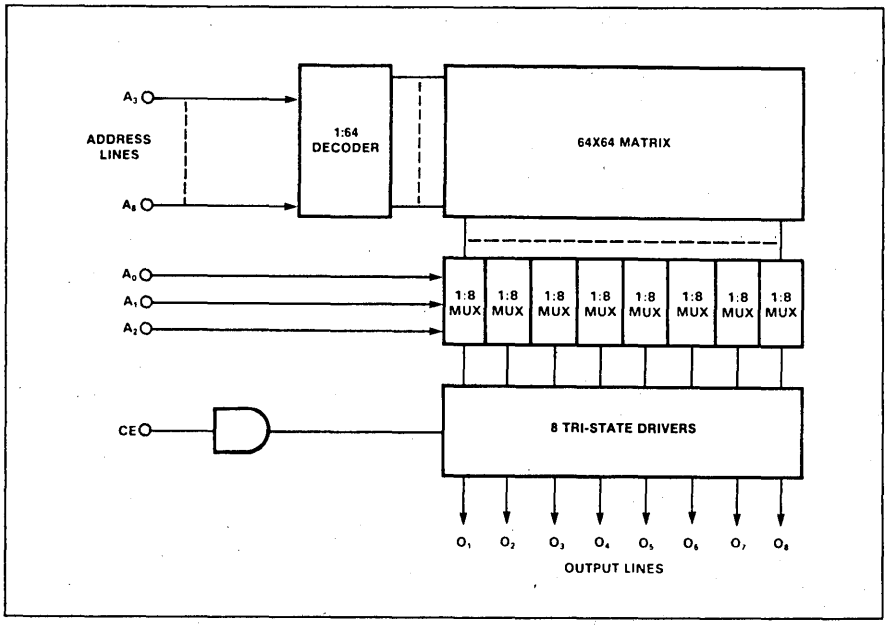
F,N PACKAGE



F = Cerdip
N = Plastic

TOP VIEW

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_O	Off-state	+5.5	Vdc
	Temperature range		°C
T_A	Operating	0 to +75	
T_{STG}	Storage	-65 to +150	

4096-BIT BIPOLAR PROM (512×8) 82S147A (T.S.)

DC ELECTRICAL CHARACTERISTICS $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$.

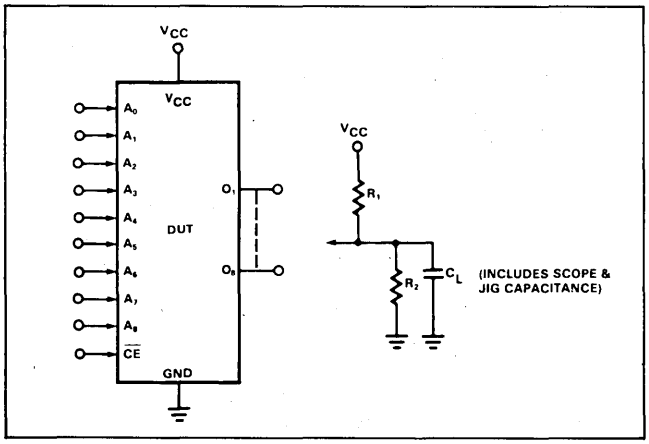
PARAMETER		TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
	Input voltage[2]					V
V_{IL}	Low				.85	
V_{IH}	High		2.0			
V_{IC}	Clamp	I_{IN} = -18mA			-1.2	
	Output voltage					V
V_{OL}	Low	I_{OUT} = 9.6mA			0.45	
V_{OH}	High	$\overline{CE}$ = Low, I_{OUT} = -2mA, High stored	2.4			
	Input current					μA
I_{IL}	Low	V_{IN} = 0.45V			-100	
I_{IH}	High	V_{IN} = 5.5V			40	
	Output current					
I_{OLK}	Leakage	$\overline{CE}$ = High, V_{OUT} = 5.5V			40	μA
$I_{O(OFF)}$	Hi-Z state	$\overline{CE}$ = High, V_{OUT} = 0.5V			-40	μA
		$\overline{CE}$ = High, V_{OUT} = 5.5V			40	
I_{OS}	Short circuit[3]	V_{OUT} = 0V	-20		-70	mA
I_{CC}	V_{CC} supply current				155	mA
	Capacitance	V_{CC} = 5.0V $\overline{CE}$ = High				pF
C_{IN}	Input	V_{IN} = 2.0V		5		
C_{OUT}	Output	V_{OUT} = 2.0V		8		

AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

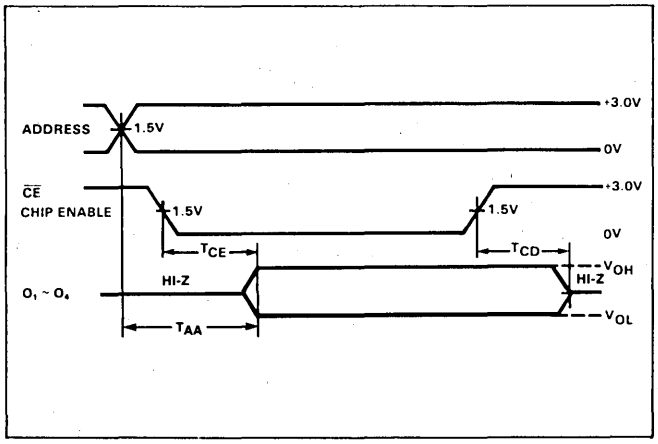
PARAMETER		TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
	Access time						ns
T_{AA}[4]		Output	Address			45	
T_{CE}		Output	Chip enable			30	
T_{CD}	Disable time	Output	Chip disable			30	ns

NOTES
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μsec.
5. Typical values are at V_{CC} = 5V, T_A = 25°C.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



See Pages 3909-3910 for Product Selector Guides.

8192-BIT BIPOLAR PROM (1024×8) 82S181A/82S181B (T.S.)

DESCRIPTION

The 82S181 is field-programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The 82S181 is supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

This device includes on-chip decoding and 4 chip enable inputs for ease of memory expansion. It features 2 tri-state outputs for optimization of word expansion in bused organizations.

The 82S181 is available in both the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S181AF or N or N82S181BF or N, and for the military temperature range (−55°C to +125°C) specify S82S181, R, F, G, I.

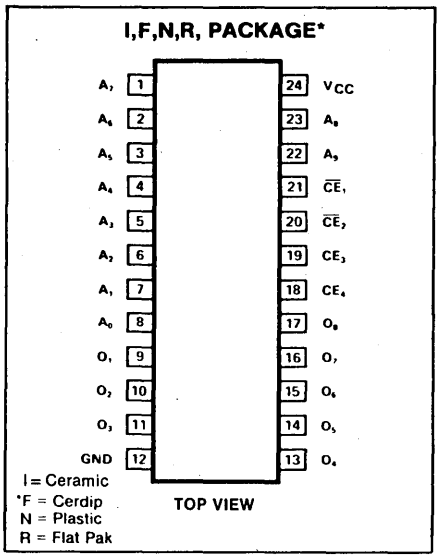
FEATURES

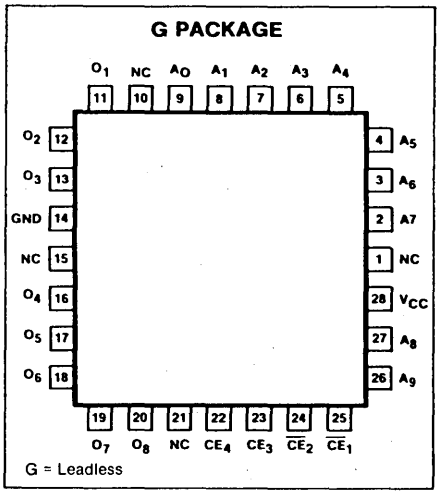
- **Address access time:**
  N82S181A: 55ns max
  N82S181B: 45ns max
  S82S181A: 80ns max
- **Power dissipation: 85μW/bit typ**
- **Input loading:**
  N82S181: −100μA max
  S82S181: −150μA max
- **On-chip address decoding**
- **Output:**
  82S181: tri-state
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

APPLICATIONS

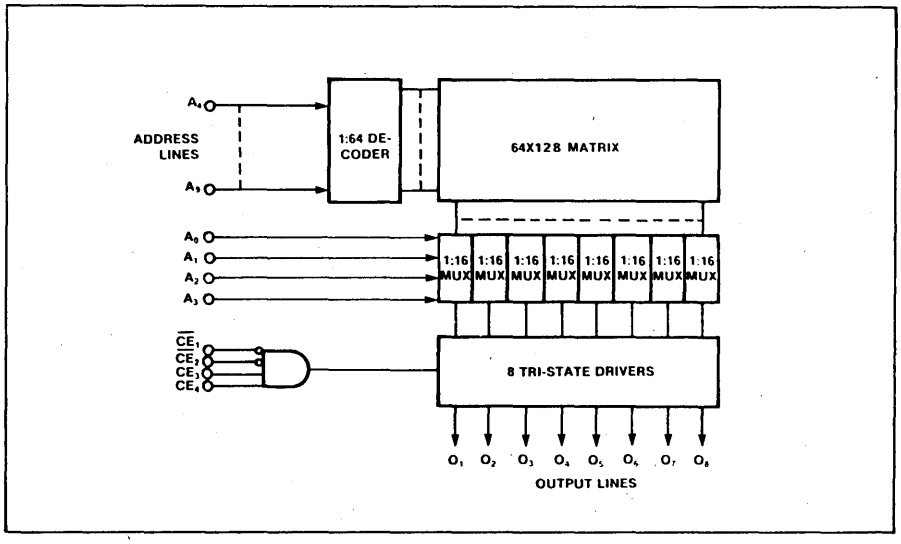
- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION





BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
V_O	Output voltage Off-state	+5.5	Vdc
T_A	Temperature range Operating		°C
	N82S181	0 to +75	
	S82S181	-55 to +125	
T_{STG}	Storage	-65 to +150	

8192-BIT BIPOLAR PROM (1024×8) 82S181A/82S181B (T.S.)

DC ELECTRICAL CHARACTERISTICS

N82S181A/N82S181B: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S181A: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS[1,2]	N82S181A/N82S181B			S82S181A			UNIT
			Min	Typ[5]	Max	Min	Typ	Max	
	Input voltage								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = -18mA		-0.8	-1.2			-1.2	
	Output voltage	$\overline{CE}_{1,2}$ = Low, $CE_{3,4}$ = High							V
V_{OL}	Low	I_{OUT} = 9.6mA			0.45			0.5	
V_{OH}	High	I_{OUT} = -2mA	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output current								
I_{OLK}									
$I_{O(OFF)}$	Hi-Z state	$\overline{CE}_{1,2}$ = High, $CE_{3,4}$ = Low, V_{OUT} = 5.5V			40			-60	μA
		$\overline{CE}_{1,2}$ = High, $CE_{3,4}$ = Low, V_{OUT} = 0.5V			-40			60	μA
I_{OS}	Short circuit[3]	$\overline{CE}_{1,2}$ = Low, $CE_{3,4}$ = High, V_{OUT} = 0V High Stored	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current	$\overline{CE}_{1,2}$ = Low, $CE_{3,4}$ = High		125	175			185	mA
	Capacitance	$\overline{CE}_{1,2}$ = High, V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$
N82S181A/N82S181B: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S181A: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TO	FROM	N82S181A			N82S181B			S82S181A			UNIT
				Min	Typ[5]	Max	Min	Typ	Max	Min	Typ	Max	
T_{AA}[4]	Access time	Output	Address		45	55			45			80	ns
T_{CE}		Output	Chip enable		20	35			30			45	
T_{CD}	Disable time	Output	Chip disable		20	35			30			45	ns

NOTES
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μsec.
5. Typical values are at V_{CC} = 5V, T_A = 25°C.

See Pages 3909-3910 for Product Selector Guides.

8192-BIT BIPOLAR PROM (2048 × 8) 82S185A/82S185B (T.S.)

DESCRIPTION

The 82S185 is field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The standard 82S185 is supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

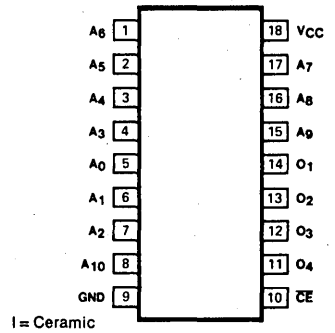
This device includes on-chip decoding and 1 chip enable input for memory expansion. It features tri-state outputs for optimization of word expansion in bused organizations.

The 82S185 device is available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S185A, I, F, N or N82S185B, I, F, or N, and for the military temperature range (−55°C to +125°C) specify S82S185, I, F, or R.

FEATURES

- **Low power dissipation: 70μW/bit typ**
- **Address access time:**
  - **N82S185A: 50ns max**
  - **N82S185B: 45ns max**
  - **S82S185A: 80ns max**
- **Input loading:**
  - **N82S185: −100μA max**
  - **S82S185: −150μA max**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

I,F,N,R PACKAGE



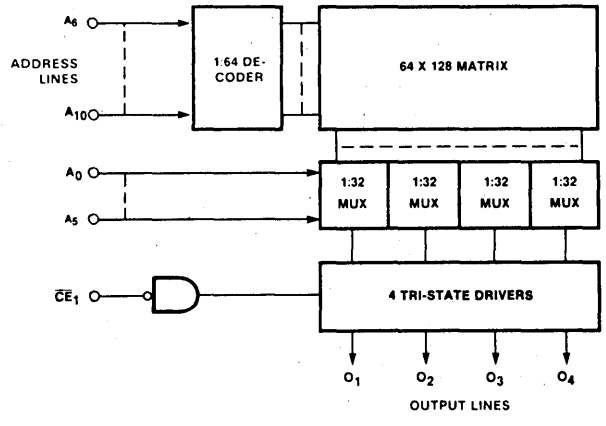
I = Ceramic
F = Cerdip
N = Plastic
R = Flat Pak

TOP VIEW

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_O	Off-state	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S185	0 to +75	
	S82S185	-55 to +125	
T_{STG}	Storage	-65 to +150	

BLOCK DIAGRAM



Signetics

MEMORY

See Pages 3909-3910 for Product Selector Guides.

8192-BIT BIPOLAR PROM (2048 × 8) 82S185A/82S185B (T.S.)

DC ELECTRICAL CHARACTERISTICS

N82S185A/N82S185B: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S185A: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS[1,2]	N82S185A/B			S82S185A			UNIT
			Min	Typ[5]	Max	Min	Typ	Max	
	Input voltage[1]								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = -18mA		-0.8	-1.2			-1.2	
	Output voltage[1]	$\overline{CE}$ = Low							V
V_{OL}	Low	I_{OUT} = 16mA			0.45			0.5	
V_{OH}	High	I_{OUT} = -2mA	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN}= 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output current								
I_O (OFF)	Hi-Z state	$\overline{CE}$ = High, V_{OUT} = 0.5V			-40			-60	μA
		$\overline{CE}$ = High, V_{OUT} = 5.5V			40			60	
I_{OS}	Short circuit[3]	$\overline{CE}$ = Low, V_{OUT} = 0V High Stored	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current			110	155			160	mA
	Capacitance	$\overline{CE}$ = High, V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

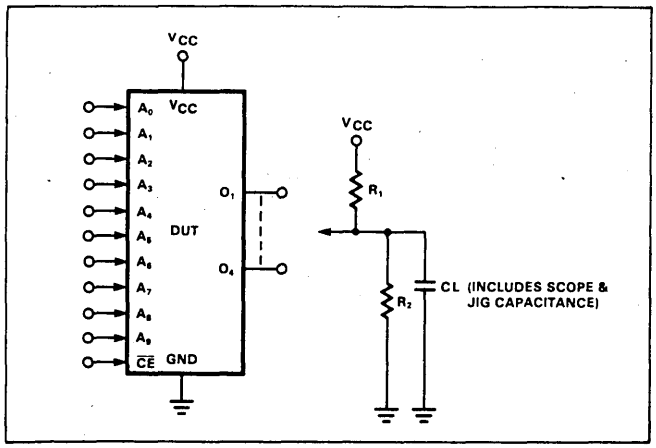
AC ELECTRICAL CHARACTERISTICS

$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$
N82S185A/N82S185B: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S185A: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

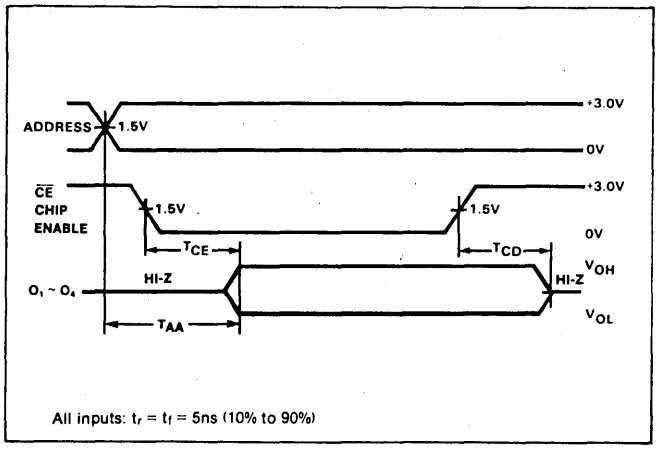
PARAMETER	TO	FROM	N82S185A			N82S185B			S82S185A			UNIT
			Min	Typ[5]	Max	Min	Typ	Max	Min	Typ	Max	
Access time												ns
T_{AA}[4]	Output	Address		40	50			45			80	
T_{CE}	Output	Chip enable		20	30			25			40	
Disable time												ns
TCD	Output	Chip disable		20	30			25			40	

NOTES
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μsec.
5. Typical values are at V_{CC}=5V, T_A=25°C

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



All inputs: $t_r = t_f$ = 5ns (10% to 90%)

See Pages 3909-3910 for Product Selector Guides.

16,384-BIT BIPOLAR PROM (2048×8) 82S191A (T.S.)

DESCRIPTION

The 82S191 is field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The 82S191 is supplied with all outputs at a logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

This device includes on-chip decoding and 3 chip enable inputs for ease of memory expansion. It features tri-state outputs for optimization of word expansion in bused organizations.

The 82S191 device is available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S191A, I or N, and for the military temperature range (−55°C to +125°C) specify S82S191A, I, R or G.

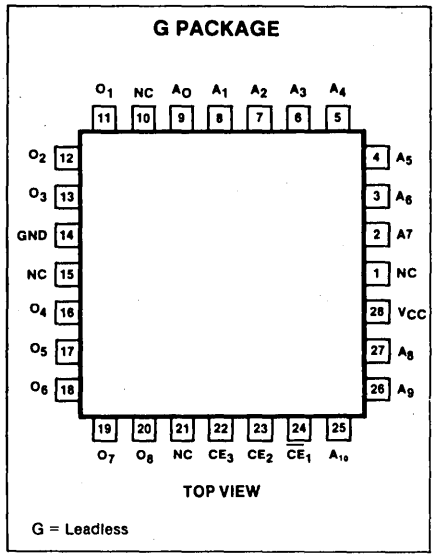
FEATURES

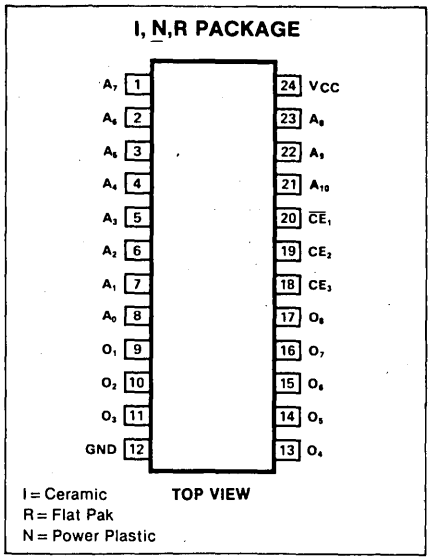
- **Address access time:**
  - **N82S191A: 60ns max**
  - **S82S191A: 80ns max**
- **Power dissipation: 20μW/bit typ**
- **Input loading:**
  - **N82S191A: −100μA max**
  - **S82S191A: −150μA max**
- **3 chip enable inputs**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

APPLICATIONS

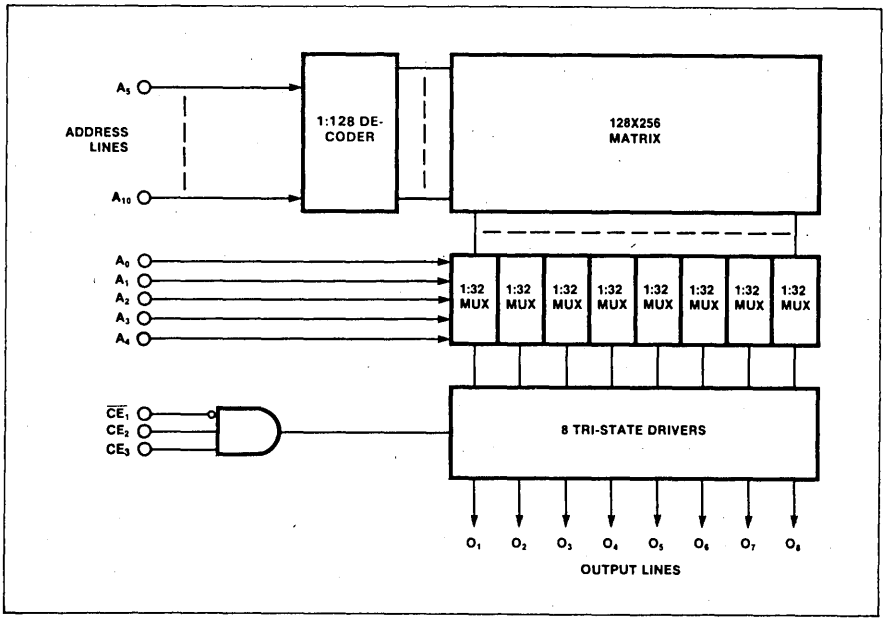
- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS





BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_O	Off-state	+5.5	
	Temperature range		°C
T_A	Operating		
	N82S191	0 to +75	
	S82S191	-55 to +125	
T_{STG}	Storage	-65 to +150	

16,384-BIT BIPOLAR PROM (2048×8) 82S191A (T.S.)

DC ELECTRICAL CHARACTERISTICS

N82S191A: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S191A: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS[1,2]	N82S191A			S82S191A			UNIT
			Min	Typ[5]	Max	Min	Typ	Max	
	Input voltage								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	I_{IN} = -18mA		-0.8	-1.2			-1.2	
	Output voltage	$\overline{CE}_1$ = Low, $CE_{2,3}$ = High							V
V_{OL}	Low	I_{OUT} = 9.6mA			0.45			0.5	
V_{OH}	High	I_{OUT} = -2mA	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V			-100			-150	
I_{IH}	High	V_{IN} = 5.5V			40			50	
	Output current								μA
$I_{O(OFF)}$	Hi-Z state	$\overline{CE}_1$ = High, $CE_{2,3}$ = Low, V_{OUT} = 0.5			-40			-60	
		$\overline{CE}_1$ = High, $CE_{2,3}$ = Low, V_{OUT} = 5.5			40			60	
I_{OS}	Short circuit[3]	$\overline{CE}_1$ = Low, $CE_{2,3}$ = High, V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current			130	175			185	mA
	Capacitance	$\overline{CE}_1$ = High, $CE_{2,3}$ = Low, V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$
N82S191A: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S191A: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER	TO	FROM	N82S191A			S82S191A			UNIT
			Min	Typ[5]	Max	Min	Typ	Max	
Access time									ns
T_{AA}[4]	Output	Address		50	60			80	
T_{CE}	Output	Chip enable		20	35			45	
Disable time									ns
T_{CD}	Output	Chip disable		20	35			45	

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μsec.
5. Typical values are at V_{CC} = 5V, T_A = 25°C.

See Pages 3909-3910 for Product Selector Guides.

16,384-BIT BIPOLAR PROM (4096×4) 82HS195 (T.S.)

Advance Information

DESCRIPTION

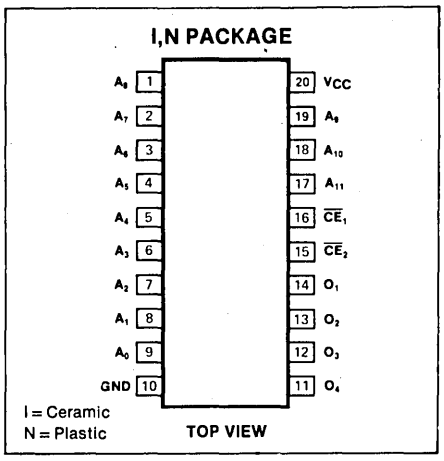
The 82HS195 is field programmable, which means that custom patterns are immediately available by following the focusing procedure given in this data manual. The standard 82HS195 is supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a programmable matrix.

This device includes on-chip decoding and 2 chip enable inputs for memory expansion. It features tri-state outputs for optimization of word expansion in bused organizations.

The 82HS195 device is available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify 82HS195, I or N, and for the military temperature range (−55°C to +125°C) specify S82HS195, I.

FEATURES

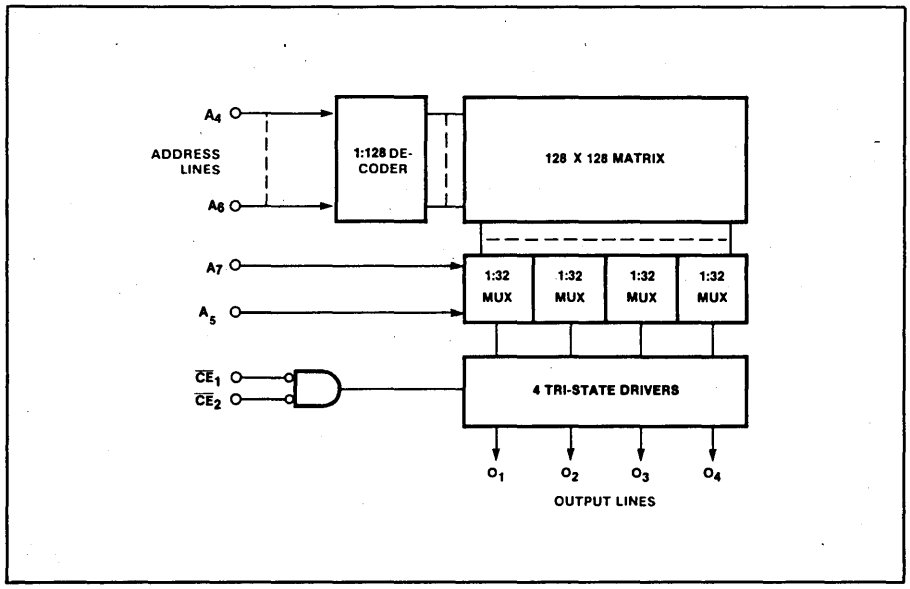
- **Low power dissipation: 35μW/bit typ**
- **Address access time:**
  - **N82HS195: 35ns max**
  - **S82HS195: 50ns max**
- **Input loading:**
  - **N82HS195: −100μA max**
  - **S82HS195: −150μA max**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_O	Off-state	+5.5	
	Temperature range		°C
T_A	Operating		
	N82HS195	0 to +75	
	S82HS195	-55 to +125	
T_{STG}	Storage	-65 to +150	

BLOCK DIAGRAM



Signetics

MEMORY

16,384-BIT BIPOLAR PROM (4096×4) 82HS195 (T.S.)

Advance Information

DC ELECTRICAL CHARACTERISTICS

N82HS195: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82HS195: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS[1,2]	N82HS195			S82HS195			UNIT
			Min	Typ[5]	Max	Min	Typ	Max	
	Input voltage[1]								V
V_{IL}	Low				.85			.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp	$I_{IN} = -18mA$		-0.8	-1.2			-1.2	
	Output voltage[1]	$\overline{CE}_1$ & $\overline{CE}_2$ = Low							V
V_{OL}	Low	$I_{OUT} = 16mA$			0.45			0.5	
V_{OH}	High	$I_{OUT} = -2mA$	2.4			2.4			
	Input current								μA
I_{IL}	Low	$V_{IN} = 0.45V$			-100			-150	
I_{IH}	High	$V_{IN} = 5.5V$			40			50	
	Output current								
I_O (OFF)	Hi-Z state	$\overline{CE}_1$ & $\overline{CE}_2$ = High, $V_{OUT} = 0.5V$			-40			-60	μA
		$\overline{CE}_1$ & $\overline{CE}_2$ = High, $V_{OUT} = 5.5V$			40			60	
I_{OS}	Short circuit[3]	$\overline{CE}_1$ & $\overline{CE}_2$=Low, V_{OUT}=0V High Stored	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current			110	155			165	mA
	Capacitance	$\overline{CE}_1$ & $\overline{CE}_2$ = High, $V_{CC} = 5.0V$							pF
C_{IN}	Input	$V_{IN} = 2.0V$		5			5		
C_{OUT}	Output	$V_{OUT} = 2.0V$		8			8		

AC ELECTRICAL CHARACTERISTICS

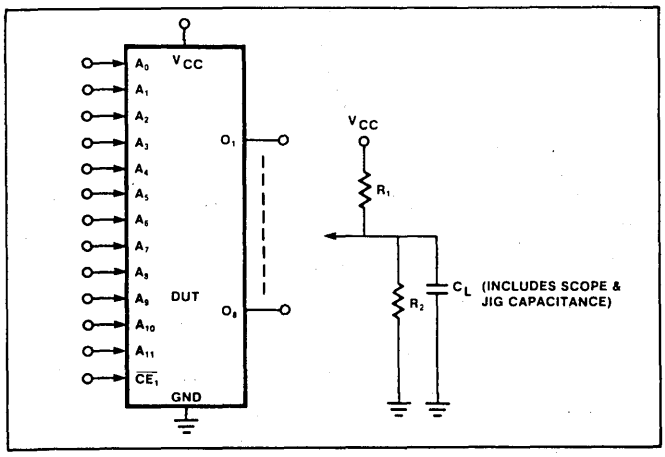
$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$
N82HS195: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82HS195: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER	TO	FROM	N82HS195			S82HS195[5]			UNIT
			Min	Typ[5]	Max	Min	Typ	Max	
Access time									ns
T_{AA}[4]	Output	Address			35			50	
T_{CE}	Output	Chip enable			25			30	
Disable time									ns
T_{CD}	Output	Chip disable			25			30	

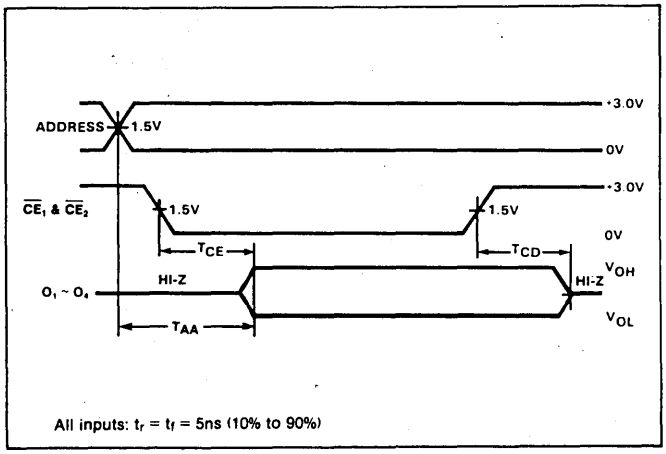
NOTES

1. All voltage values are with respect to network ground terminal.
2. Positive current is defined as into the terminal referenced.
3. Duration of the short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μsec.
5. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



All inputs: $t_r = t_f = 5ns$ (10% to 90%)

Signetics

MEMORY

See Pages 3909-3910 for Product Selector Guides.

256-BIT BIPOLAR RAM (256×1) 82LS16 (T.S.)/82LS17 (O.C.)

DESCRIPTION

The 82LS16 and 82LS17 are Read/Write memory arrays which feature either open collector or 3-state output options for optimization of word expansion in bused organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 chip enable inputs and PNP input transistors which reduce input loading.

During Write operation, the logical state of the output of both devices follows the complement of the data input being written. This feature allows faster execution of Write/Read cycles, enhancing the performance of systems utilizing indirect addressing modes, and/or requiring immediate verification following a Write cycle.

Both devices have fast Read access and Write cycle times, as well as low power requirements and thus are ideally suited in high-speed memory applications such as cache, buffers, scratch pads, writable control stores, where power limitations are of major concern.

Both devices are available in the commercial temperature range (0°C to +75°C) and the military temperature range (−55°C to +125°C). They are specified as: N82LS16F or N or N82LS17F or N for the commercial temperature range, and S82LS16F, G, or W or S82LS17F, G, or W for the military temperature range. Military products are available as fully processed to Mil-Std 883 Level B or Level C; specify either 883B or 883C.

See page 4-9 for Truth Table, Timing Diagrams, Test Circuit and Waveform.

FEATURES

- **Address access time:**
  N82LS16/17: 40ns max
  S82LS16/17: 60ns max
- **Write cycle time:**
  N82LS16/17: 40ns max
  S82LS16/17: 65ns max
- **Power dissipation: 0.98mW/bit typ**
- **Input loading:**
  N82LS16/17: −100μA max
  S82LS16/17: −250μA max
- **Output follows complement of data input during Write**
- **On-chip address decoding**
- **Output option:**
  82LS16 3-state
  82LS17 Open collector
- **Schottky clamped**
- **TTL compatible**

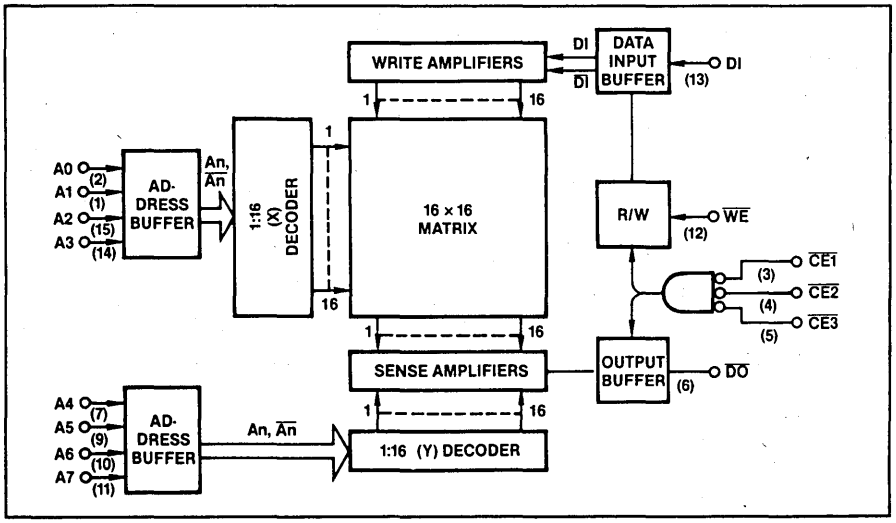
APPLICATIONS

- **Buffer memory**
- **Writable control store**
- **Memory mapping**
- **Push down stack**
- **Scratch pad**

ABSOLUTE MAXIMUM RATINGS

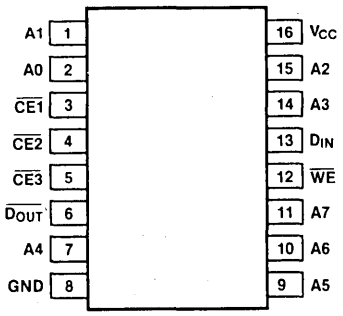
	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OUT}	High (open collector)	+5.5	
	Temperature Range		
T_A	Operating		°C
	N grade	0 to +70	
	S grade	−55 to +125	
T_{STG}	Storage	−65 to +150	°C

BLOCK DIAGRAM



PIN CONFIGURATIONS

F, N, W PACKAGE

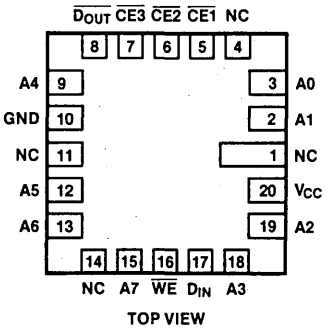


TOP VIEW

Order Numbers:
N82LS16F or N82LS16N
N82LS17F or N82LS17N
S82LS16F or S82LS16W
S82LS17F or S82LS17W

F = Cerdip
N = Plastic
R = Flat Pak

G PACKAGE



TOP VIEW

Order Numbers:
S82LS16G or S82LS17G

G = Leadless

256-BIT BIPOLAR RAM (256 × 1) 82LS16 (T.S.)/82LS17 (O.C.)

DC ELECTRICAL CHARACTERISTICS

N82LS16/17: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82LS16/17: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS	N82LS16/17			S82LS16/17			UNIT
			Min	Typ[1]	Max	Min	Typ[1]	Max	
	Input voltage[2]								V
V_{IH}	High	V_{CC} = max	2.0			2.0			
V_{IL}	Low	V_{CC} = min			0.85			0.8	
V_{IC}	Clamp[3]	V_{CC} = min, I_{IN} = −12mA		−1.0	−1.5		−1.0	−1.5	
	Output voltage[2]	V_{CC} = min							V
V_{OH}	High (82LS16)[4]	I_{OH} = −3.2mA	2.6			2.4			
V_{OL}	Low[5]	I_{OL} = 16mA		0.35	0.45		0.35	0.5	
	Input current[3]	V_{CC} = max							μA
I_{IH}	High	V_{IN} = 5.5V		1	25		1	25	
I_{IL}	Low	V_{IN} = 0.45V		−10	−100		−10	−250	
	Output current								μA
I_{OLK}	Leakage (82LS17)[5]	V_{OUT} = 5.5V		1	40		1	40	
$I_{O(OFF)}$	Hi-Z state (82LS16)[6]	V_{OUT} = 5.5V		1	40		1	50	
		V_{OUT} = 0.45V		−1	−40		−1	−50	
I_{OS}	Short circuit (82LS16)[7]	V_{CC} = max, V_O = 0V	−20		−70	−20		−70	
I_{CC}	V_{CC} supply current[8]	V_{CC} = max		50	70		50	100	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

AC ELECTRICAL CHARACTERISTICS

R1 = 270Ω, R2 = 600Ω, C_L = 30pF
N82LS16/17: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82LS16/17: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TO	FROM	N82LS16/17			S82LS16/17			UNIT
				Min	Typ[1]	Max	Min	Typ[1]	Max	
	Access time									ns
T_{AA}	Address	Output	Address		30	40		30	70	
T_{CE}	Chip enable	Output	Chip enable		15	25		15	40	
T_{CD}	Disable time	Output	Chip enable		15	25		15	40	ns
T_{WD}	Valid time	Output	Write enable		30	40		30	55	ns
	Setup and hold time									ns
T_{WSA}	Setup time	Write enable	Address	0	−5		10	−5		
T_{WHA}	Hold time			0	−5		10	−5		
T_{WSD}	Setup time	Write enable	Data in	25	15		40	15		
T_{WHD}	Hold time			0	−5		10	−5		
T_{WSC}	Setup time	Write enable	$\overline{CE}$	0	−5		10	−5		
T_{WHC}	Hold time			0	−5		10	−5		
	Pulse width									ns
T_{WP}	Write enable[9]			25	15		40	15		

NOTES

1. All typical values are at V_{CC} = 5V, T_A + 25°C.
2. All voltage values are with respect to network ground terminal.
3. Test each input one at a time.
4. Measured with a logic low stored and V_{IL} applied to $\overline{CE1}$, $\overline{CE2}$ and $\overline{CE3}$.
5. Measured with a logic high stored. Output sink current is supplied through a resistor to V_{CC}.
6. Measured with V_{IH} applied to $\overline{CE1}$, $\overline{CE2}$ and $\overline{CE3}$.
7. Duration of the short-circuit should not exceed 1 second.
8. I_{CC} is measured with the Write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
9. Minimum required to guarantee a Write into the slowest bit.

See Pages 3909-3910 for Product Selector Guides.

STATIC RANDOM ACCESS MEMORIES (RAMs) Commercial (T_A = 0°C to 70°C)

Part Number	Organization	Access Time (ns)	Maximum Current (mA)		Power Supply (Volts)	Number of Pins	Package Type (Note 1)
			Operating	Standby			
SY2101-1	256 x 4	500	70	--	+5	22	C, P
SY2101A	256 x 4	350	55	--	+5	22	C, P
SY2101A-2	256 x 4	250	55	--	+5	22	C, P
SY2101A-4	256 x 4	450	55	--	+5	22	C, P
SY2111-1	256 x 4	500	70	--	+5	18	C, D, P
SY2111A	256 x 4	350	55	--	+5	18	C, D, P
SY2111A-2	256 x 4	250	55	--	+5	18	C, D, P
SY2111A-4	256 x 4	450	55	--	+5	18	C, D, P
SY2112-1	256 x 4	500	70	--	+5	16	C, D, P
SY2112A	256 x 4	350	55	--	+5	16	C, D, P
SY2112A-2	256 x 4	250	55	--	+5	16	C, D, P
SY2112A-4	256 x 4	450	55	--	+5	16	C, D, P
SY2114AL-1	1024 x 4	100	40	--	+5	18	C, D, P
SY2114AL-2	1024 x 4	120	40	--	+5	18	C, D, P
SY2114AL-3	1024 x 4	150	40	--	+5	18	C, D, P
SY2114AL-4	1024 x 4	200	40	--	+5	18	C, D, P
SY2114A-4	1024 x 4	200	70	--	+5	18	C, D, P
SY2114A-5	1024 x 4	250	70	--	+5	18	C, D, P
SY2142	1024 x 4	450	100	--	+5	20	C, D, P
SY2142-2	1024 x 4	200	100	--	+5	20	C, D, P
SY2142-3	1024 x 4	300	100	--	+5	20	C, D, P
SY2142L	1024 x 4	450	70	--	+5	20	C, D, P
SY2142L-2	1024 x 4	200	70	--	+5	20	C, D, P
SY2142L-3	1024 x 4	300	70	--	+5	20	C, D, P
SY2148H	1024 x 4	70	150	30	+5	18	C, D
SY2148H-2	1024 x 4	45	150	30	+5	18	C, D
SY2148H-3	1024 x 4	55	150	30	+5	18	C, D
SY2148HL	1024 x 4	70	125	20	+5	18	C, D
SY2148HL-3	1024 x 4	55	125	20	+5	18	C, D
SY2149H	1024 x 4	70	150	--	+5	18	C, D
SY2149H-2	1024 x 4	45	150	--	+5	18	C, D
SY2149H-3	1024 x 4	55	150	--	+5	18	C, D
SY2149HL	1024 x 4	70	125	--	+5	18	C, D
SY2149HL-3	1024 x 4	55	125	--	+5	18	C, D
SY2147	4096 x 1	70	160	20	+5	18	C, D
SY2147-3	4096 x 1	55	180	30	+5	18	C, D
SY2147-6	4096 x 1	85	160	20	+5	18	C, D
SY2147L	4096 x 1	70	140	10	+5	18	C, D
SY2158-1	1024 x 8	90	100	30	+5	24	P
SY2158-2	1024 x 8	120	100	30	+5	24	P
SY2158-3	1024 x 8	150	100	30	+5	24	P
SY2158-4	1024 x 8	200	100	30	+5	24	P
SY2158L-1	1024 x 8	90	70	20	+5	24	P
SY2158L-2	1024 x 8	120	70	20	+5	24	P
SY2158L-3	1024 x 8	150	70	20	+5	24	P
SY2158L-4	1024 x 8	200	70	20	+5	24	P
SY2159-1	1024 x 8	90	100	--	+5	24	P
SY2159-2	1024 x 8	120	100	--	+5	24	P
SY2159-3	1024 x 8	150	100	--	+5	24	P
SY2159-4	1024 x 8	200	100	--	+5	24	P
SY2159L-1	1024 x 8	90	70	--	+5	24	P
SY2159L-2	1024 x 8	120	70	--	+5	24	P
SY2159L-3	1024 x 8	150	70	--	+5	24	P
SY2159L-4	1024 x 8	200	70	--	+5	24	P
SY2128-1	2048 x 8	90	100	30	+5	24	K, C, D, P
SY2128-2	2048 x 8	120	100	30	+5	24	K, C, D, P
SY2128-3	2048 x 8	150	100	30	+5	24	K, C, D, P
SY2128-4	2048 x 8	200	100	30	+5	24	K, C, D, P
SY2128L-1	2048 x 8	90	70	20	+5	24	K, C, D, P
SY2128L-2	2048 x 8	120	70	20	+5	24	K, C, D, P
SY2128L-3	2048 x 8	150	70	20	+5	24	K, C, D, P
SY2128L-4	2048 x 8	200	70	20	+5	24	K, C, D, P
SY2129-1	2048 x 8	90	100	--	+5	24	K, C, D, P
SY2129-2	2048 x 8	120	100	--	+5	24	K, C, D, P
SY2129-3	2048 x 8	150	100	--	+5	24	K, C, D, P
SY2129-4	2048 x 8	200	100	--	+5	24	K, C, D, P
SY2129L-1	2048 x 8	90	70	--	+5	24	K, C, D, P
SY2129L-2	2048 x 8	120	70	--	+5	24	K, C, D, P
SY2129L-3	2048 x 8	150	70	--	+5	24	K, C, D, P
SY2129L-4	2048 x 8	200	70	--	+5	24	K, C, D, P
SY2168[2]	4096 x 4	45-70	125	30	+5	20	K, C, D,
SY2169[2]	4096 x 4	45-70	125	--	+5	20	K, C, D,
SY2167[2]	16384 x 1	45-70	125	30	+5	20	K, C, D,

NOTES:
1. C = Ceramic, D = Cerdip, F = Flatpack, K = Leadless Chip Carrier.
2. Preliminary Information.

Synertek.

SY2114A

1024 x 4 Static Random Access Memory

Features

- 100ns Maximum Access
- Low Operating Power Dissipation 0.1 mW/Bit
- No Clocks or Strobes Required
- Identical Cycle and Access Times
- Single +5V Supply
- Totally TTL Compatible: All Inputs, Outputs, and Power Supply
- Common Data I/O
- 400 mv Noise Immunity
- High Density 18 Pin Package

Description

The SY2114A is a 4096-Bit static Random Access Memory organized 1024 words by 4-bits and is fabricated using Synertek's N-channel Silicon-Gate MOS technology. It is designed using fully DC stable (static) circuitry in both the memory array and the decoding and therefore requires no clock or refreshing to operate. Address setup times are not required and the data is read out nondestructively with the same polarity as the input data. Common Input/Output pins are provided to simplify design of the bus oriented systems, and can drive 1 TTL load.

The SY2114A is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. It is totally TTL compatible in all respects: inputs, outputs, and the single +5V supply. A separate Chip Select ($\overline{CS}$) input allows easy selection of an individual device when outputs are or-tied.

The SY2114A is packaged in an 18-pin DIP for the highest possible density and is fabricated with N-channel, Ion Implanted, Silicon-Gate technology – a technology providing excellent performance characteristics as well as improved protection against contamination.

SY2147H

4096 x 1 Static Random Access Memory

Features

- 35-70 ns Maximum Access Time
- No Clocks or Strobes Required
- Automatic $\overline{CE}$ Power Down
- Identical Cycle and Access Times
- Single +5V Supply (±10%)
- Pinout and Function Compatible to SY2147
- Direct Performance Upgrade For SY2147
- Totally TTL Compatible All Inputs and Outputs
- Separate Data Input and Output
- High Density 18-Pin Package
- Three-State Output

Description

The Synertek SY2147H is a 4096-Bit Static Random Access Memory organized 4096 words by 1-bit and is fabricated using Synertek's new scaled n-channel silicon gate technology. It is designed using fully static circuitry, therefore requiring no clock or refreshing to operate. Address set-up times are not required and the data is read out non-destructively with the same polarity as the input data. Separate data input and output pins provide maximum design flexibility. The three-state output facilitates memory expansion by allowing the outputs to be OR-tied to other devices.

The SY2147H offers an automatic power down feature. Power down is controlled by the Chip Enable input. When Chip Enable ($\overline{CE}$) goes high, thus deselecting the SY2147H, the device will automatically power down and remain in a standby power mode as long as $\overline{CE}$ remains high. This unique feature provides system level power savings a much as 80%.

The SY2147H is packaged in an 18-pin DIP for the highest possible density. The device is fully TTL compatible and has a single +5V power supply.

Synertek

SY2148H/SY2149H

1024 x 4 Static Random Access Memory

Features

- 45 - 70 ns Maximum Access Time
- No Clocks or Strobes Required
- Automatic $\overline{CE}$ Power Down (SY2148H)
- Identical Cycle and Access Times
- Single +5V Supply (±10%)
- Pinout and Function Compatible to SY2148/SY2149
- Performance Upgrade for SY2148/SY2149
- Industry Standard 2114 Pinout
- Totally TTL Compatible All Inputs and Outputs
- Common Data Input and Output
- High Density 18-Pin Package
- Three-State Output

Description

The Synertek SY2148H/SY2149H are 4096-Bit Static Random Access Memories organized 1024 words by 4 bits and are fabricated using Synertek's new scaled n-channel silicon gate technology. It is designed using fully static circuitry, therefore requiring no clock or refreshing to operate. Address set-up times are not required and the data is read out non-destructively with the same polarity as the input data. Common data input and output pins provide maximum design flexibility. The three-state output facilitates memory expansion by allowing the outputs to be OR-tied to other devices.

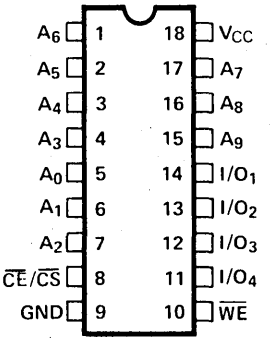
The SY2148H offers an automatic power down feature. Power down is controlled by the Chip Enable input. When Chip Enable ($\overline{CE}$) goes high, thus de-selecting the SY2148H, the device will automatically power down and remain in a standby power mode as long as $\overline{CS}$ remains high. This unique feature provides system level power savings as much as 85%.

The SY2149H offers a Chip Select ($\overline{CS}$) access that is faster than its address access. This feature offers high speed access when the address preceeds the $\overline{CS}$ decode sent to the part.

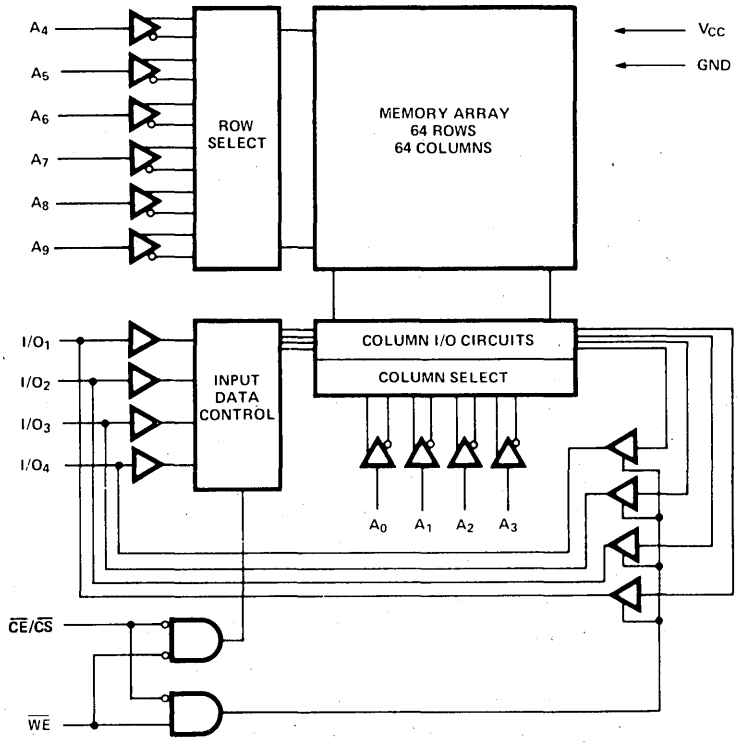
Both parts are packaged in an 18-pin DIP for the highest possible density. Both devices are TTL compatible and have a single +5V power supply.

Pin Configurations

SY2148H/ST2149H



Block Diagram



Ordering Information

Order Number	Access Time (Max)	Operating Current (Max)	Standby Current (Max)
SY2148H	70ns	150mA	30mA
SY2148H-2	45ns	150mA	30mA
SY2148H-3	55ns	150mA	30mA
SY2149H	70ns	150mA	—
SY2149H-2	45ns	150mA	—
SY2149H-3	55ns	150mA	—
SY2148HL	70ns	125mA	20mA
SY2148HL-3	55ns	125mA	20mA
SY2149HL	70ns	125mA	—
SY2149HL-3	55ns	125mA	—

Synertek.

SY2158/SY2159

1024 x 8 Static Random Access Memory

Features

- 120nsec Maximum Access Time
- Fully Static Operation: No Clocks or Strobes Required
- Fast Chip Select Access: 50 ns Max.
- Automatic $\overline{CE}$ Power Down
- Identical Cycle and Access Times
- Single +5V Supply (± 10%)
- Pin Compatible with 2716 16K EPROM
- Totally TTL Compatible: All Inputs and Outputs
- Common Data Input and Output
- Three-State Output
- Output Enable Function ($\overline{OE}$)

Description

The Synertek SY2158/SY2159 are 8192 bit static Random Access Memories organized 1024 words by eight bits and are fabricated using Synertek's new scaled n-channel silicon gate technology. They are designed using fully static circuitry, therefore requiring no clocks or refreshing to operate. The common data input and three-state output pins optimize compatibilty with systems utilizing a bidirectional data bus.

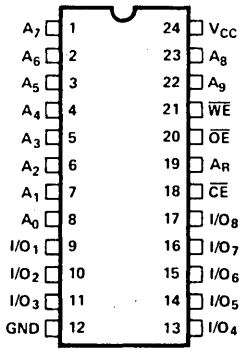
The SY2158 offers an automatic power down feature under the control of the chip enable ($\overline{CE}$) input. When $\overline{CE}$ goes high, deselecting the chip, the device will automatically power down and remain in a standby power mode as long as $\overline{CE}$ remains high. This feature provides significant system level power savings.

The SY2159 offers a chip select access that is faster than its address access. In a typical application, the address access begins as soon as the address is valid. At this time, the high order addresses are decoded and the desired memory is then selected. With the faster chip select access, this decode time will not add to the overall access time thus significantly improving system performance.

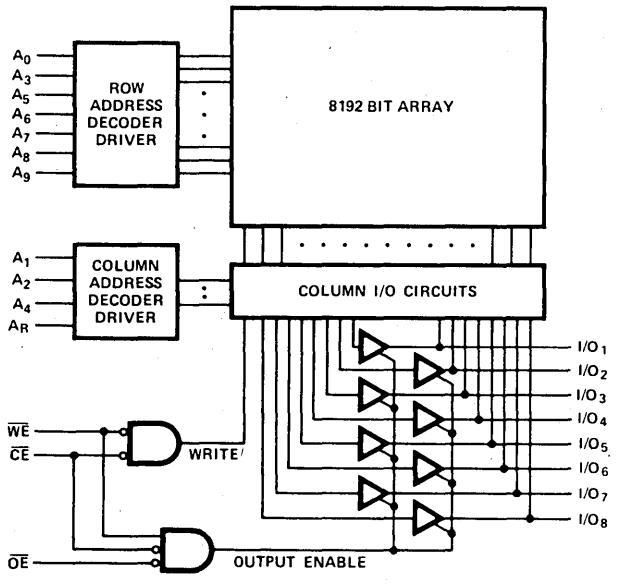
The SY2158/SY2159 are available in two versions. For the "A" version, the select reference input (A_R) must be at V_{IL} and for the "B" version A_R must be at V_{IH}.

The SY2158/SY2159 are pin compatible with 16K ROMs, EPROMs and E²PROMs thus offering the user the flexibility of switching between RAM, ROM, EPROM, and E²PROM with a minimum of board layout changes.

Pin Configuration



Block Diagram



Synertek.

SY2128/SY2129

2048 x 8 Static Random Access Memory

Features

- 100 nsec Maximum Access Time
- Fully Static Operation: No Clocks or Strobes Required
- Fast Chip Select Access Time: 50 ns Max. (SY2129)
- Automatic $\overline{CE}$ Power Down (SY2128)
- Identical Cycle and Access Times
- Single +5V Supply (±10%)
- Pin Compatible with 16K ROMs, EPROMs, and EEPROMs
- Totally TTL Compatible: All Inputs and Outputs
- Common Data Input and Output
- Three-State Output
- JEDEC Approved Pinout

Description

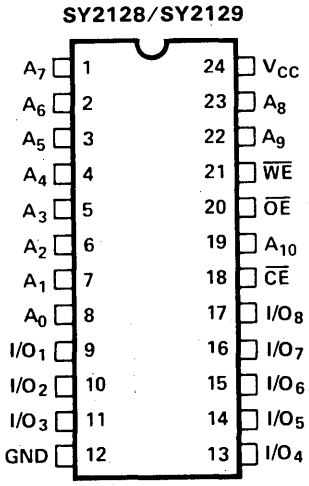
The Synertek SY2128/SY2129 are 16,384 bit static Random Access Memories organized 2048 words by eight bits and are fabricated using Synertek's new scaled n-channel silicon gate technology. They are designed using fully static circuitry, therefore requiring no clock or refreshing to operate. The common data input and three-state output pins optimize compatibility with systems utilizing a bidirectional data bus.

The SY2128 offers an automatic power down feature under the control of the chip enable ($\overline{CE}$) input. When ($\overline{CE}$) goes high, thus deselecting the chip, the device will automatically power down and remain in a standby power mode as long as $\overline{CE}$ remains high. This feature provides significant system level power savings.

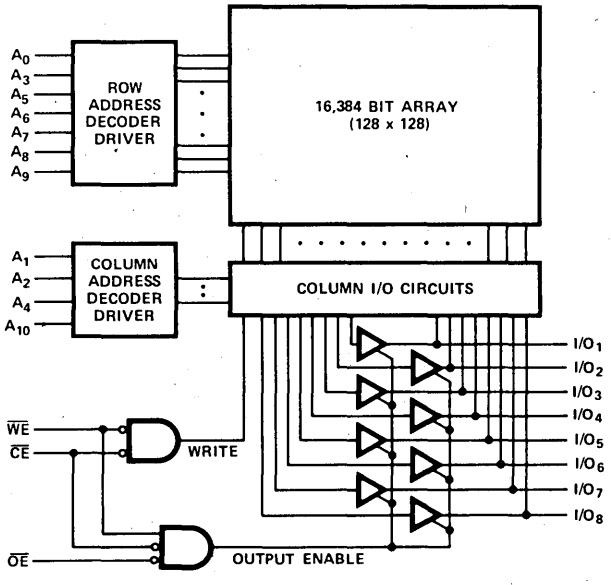
The SY2129 offers a chip select access that is faster than its address access. In a typical application, the address access begins as soon as the address is valid. At this time, the high order addresses are decoded and the desired memory is then selected. With the faster chip select access, this decode time will not add to the overall access time thus significantly improving system performance.

The SY2128/SY2129 are configured in the JEDEC approved pinout for 24 pin byte organized memories and are pin compatible with 16K ROMs, EPROMs and EEPROMs. This offers the user the flexibility of being able to swtich between RAM, ROM, EPROM, or EEPROM as his needs dictate with a minimum of board changes.

Pin Configuration



Block Diagram



Synertek

MEMORY

Synertek.

SY2167

16,384 x 1 Static Random Access Memory

ADVANCED INFORMATION
OCTOBER 1982

Features

- 55 ns Maximum Access
- No Clocks or Strobes Required
- Automatic $\overline{CE}$ Power Down
- Identical Cycle and Access Times
- Single +5V Supply
- Totally TTL Compatible All Inputs and Outputs
- Separate Data Input and Output
- High Density 20 Pin Package
- Three-State Output

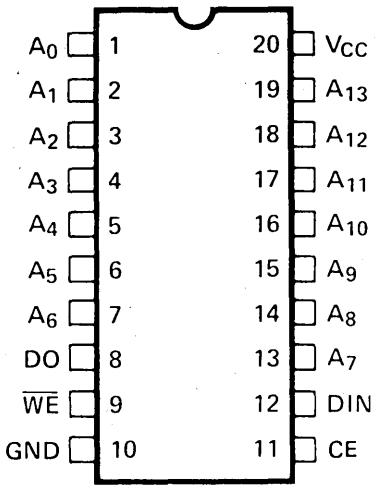
Description

The Synertek SY2167 is a 16,384-Bit Static Random Access Memory organized 16,384 words by 1-bit and is fabricated using Synertek's new N-Channel Double Polysilicon Gate HMOS technology. It is designed using fully static circuitry, therefore requiring no clock or refreshing to operate. Address set-up times are not required and the data is read out non-destructively with the same polarity as the input data. Separate data input and output pins provide maximum design flexibility. The three-state output facilitates memory expansion by allowing the outputs to be OR-tied to other devices.

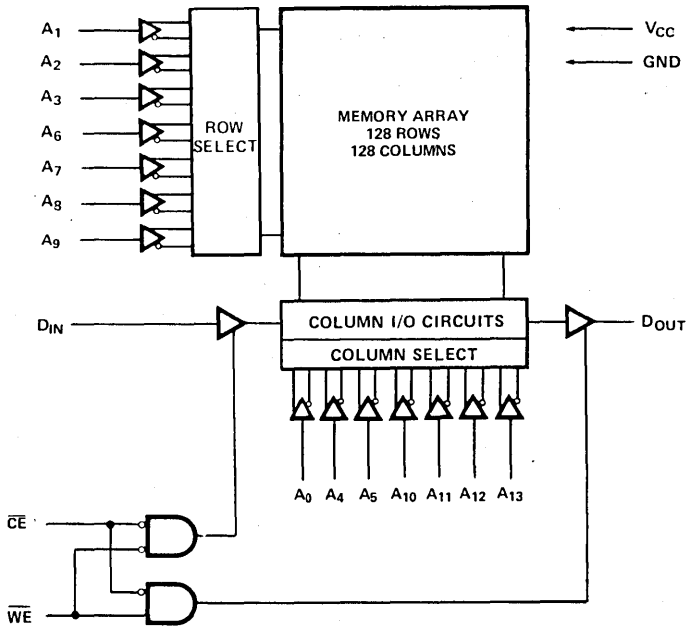
The SY2167 offers an automatic power down feature. Power down is controlled by the Chip Enable input. When Chip Enable ($\overline{CE}$) goes high, thus de-selecting the SY2167, the device will automatically power down and remain in a standby power mode as long as $\overline{CE}$ remains high. This unique feature provides system level power savings as much as 80%.

The SY2167 is packaged in a 20-pin DIP for the highest possible density. The device is fully TTL compatible and has a single +5V power supply.

Pin Configuration



Block Diagram



Synertek.

SY2168/SY2169

4096 x 4 Static Random Access Memory

Advanced Information
October 1982

Features

- 55-70 ns Maximum Access Time
- No Clocks or Strobes Required
- Fast Chip Select Access Time: 40 ns Max. (SY2169)
- Automatic $\overline{CE}$ Power Down (SY2168)
- Identical Cycle and Access Times
- Single +5V Supply (±10%)
- JEDEC Standard Pinout
- Totally TTL Compatible All Inputs and Outputs
- Common Data Input and Output
- High Density 20-Pin Package
- Three-State Output

Description

The Synertek SY2168/SY2169 is a 16,384-Bit Static Random Access Memories organized 4096 words by 4 bits and are fabricated using Synertek's scaled n-channel double poly silicon gate technology. They are designed using fully static circuitry, therefore requiring no clock or refreshing to operate. Address set-up times are not required and the data is read out non-destructively with the same polarity as the input data. Common data input and output pins provide maximum design flexibility. The three-state output facilitates memory expansion by allowing the outputs to be OR-tied to other devices.

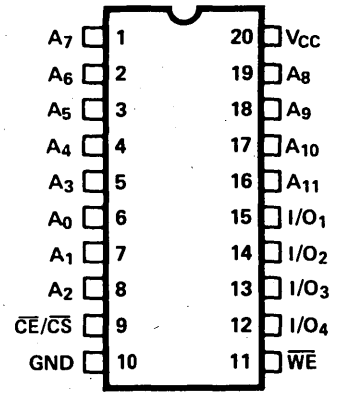
The SY2168 offers an automatic power down feature. Power down is controlled by the Chip Enable input. When Chip Enable ($\overline{CE}$) goes high, thus de-selecting the SY2168, the device will automatically power down and remain in a standby power mode as long as $\overline{CE}$ remains high. This unique feature provides system level power savings as much as 85%.

The SY2169 offers a chip select access that is faster than its address access. In a typical application, the address access begins as soon as the address is valid. At this time, the high order addresses are decoded and the desired memory is then selected. With the faster chip select access, this decode time will not add to the overall access time thus significantly improving system performance.

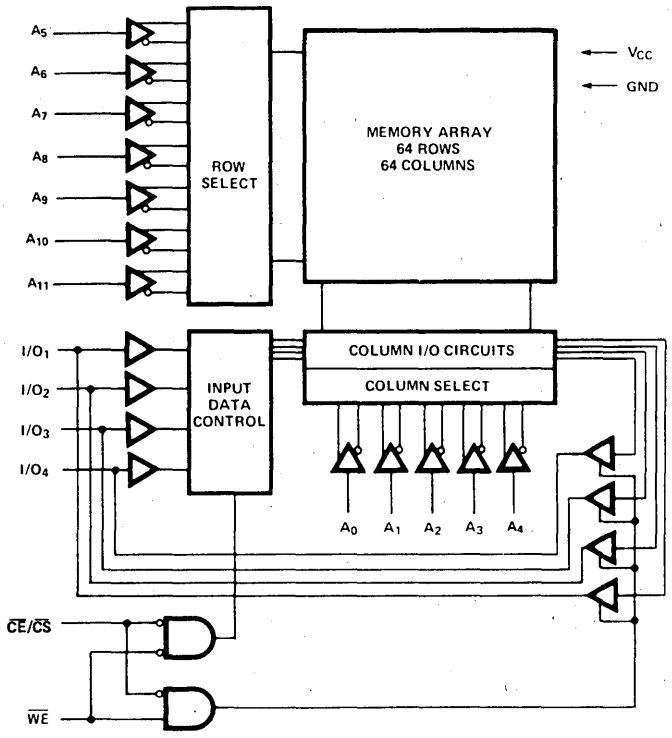
Both parts are packaged in a 20-pin DIP for the highest possible density. Both devices are fully TTL compatible and have a single +5V power supply.

Pin Configuration

SYM2168/SYM2169



Block Diagram



Synertek

MEMORY

Synertek.

SY21D1

1024 x 8 Dual Port Random Access Memory

Features

- 100 ns Address Access Time
- Fully Static Operation
- Full TTL Compatibility
- Interrupt Function ($\overline{INT}$)
- Easy Microprocessor Interface
- Transparent Power Down
- Output Enable Function ($\overline{OE}$)
- Total Left and Right Separation

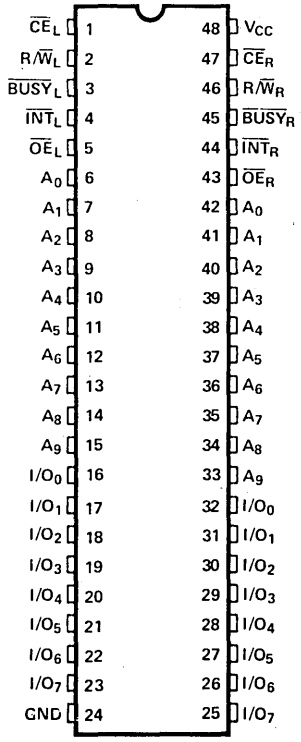
Description

The Synertek SY21D1 is an 8192 Bit Dual Port Random Access Memory organized 1024 words by 8 bits and is fabricated using Synertek's n-channel double poly silicon gate technology. It is designed using fully static circuitry, requiring no clock or refreshing to operate.

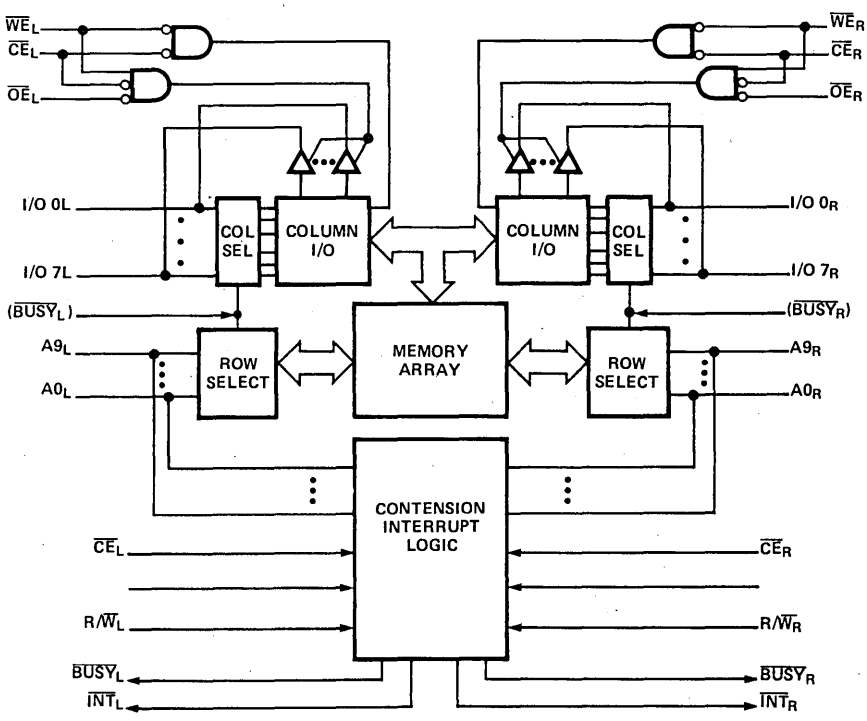
The SY21D1 is a true dual port allowing each side independent access for read or write. The only disallowed state is one where the addresses are identical. In the disallowed state the BUSY goes low. The dual port function is enhanced by the use of onboard control circuitry including BUSY, Interrupt, Output Enable and Chip Enable. The BUSY ($\overline{BUSY}$) goes low when that side tries to access an address that the other side is accessing. The interrupt function ($\overline{INT}$) acts like a writable flag. When the flag's location is written to from one side, the other side's $\overline{INT}$ pin goes low. This pin stays low until the interrupted side reads the flag location. The transparent power down feature is under the control of chip enable ($\overline{CE}$). When $\overline{CE}$ goes high, deselecting the chip, the device automatically powers down. This feature provides significant system level power savings.

The SY21D1 is packaged in a 48-pin DIP for the highest possible density. This device is fully TTL compatible and has a single +5V power supply.

Pin Configuration



Block Diagram



READ ONLY MEMORIES (ROMs) Commercial (T_A = 0°C to 70°C)

Part Number	Organization	Access Time (ns) Max.	Maximum Current (mA) Operating	Maximum Current (mA) Standby	Power Supply (Volts)	Number of Pins	Pin Compatible EPROM/PROM	Package Type (Note 1)
SY3308	1024 x 8	70	120	--	+5	24	82S181	C, D, P
SY2316B	2048 x 8	450	98	--	+5	24	2716	C, D, P
SY2316B-2	2048 x 8	200	98	--	+5	24	2716	C, D, P
SY2316B-3	2048 x 8	300	98	--	+5	24	2716	C, D, P
SY3316	2048 x 8	80	120	--	+5	24	82S191	C, D, P
SY3316A	2048 x 8	80	120	20	+5	24	82S191	C, D, P
SY2332	4096 x 8	450	100	--	+5	24	TMS2532	C, D, P
SY2332-2	4096 x 8	200	100	--	+5	24	TMS2532	C, D, P
SY2332-3	4096 x 8	300	100	--	+5	24	TMS2532	C, D, P
SY2333	4096 x 8	450	100	--	+5	24	2732/A	C, D, P
SY2333-2	4096 x 8	200	100	--	+5	24	2732/A	C, D, P
SY2333-3	4096 x 8	300	100	--	+5	24	2732/A	C, D, P
SY2364	8192 x 8	450	100	--	+5	24	TMS2564	C, D, P, K
SY2364-2	8192 x 8	200	100	--	+5	24	TMS2564	C, D, P, K
SY2364-3	8192 x 8	300	100	--	+5	24	TMS2564	C, D, P, K
SY2364A	8192 x 8	450	100	12	+5	24	TMS2564	C, D, P, K
SY2364A-2	8192 x 8	200	100	12	+5	24	TMS2564	C, D, P, K
SY2364A-3	8192 x 8	300	100	12	+5	24	TMS2564	C, D, P, K
SY2365	8192 x 8	450	100	--	+5	28	2764	C, D, P, K
SY2365-2	8192 x 8	200	100	--	+5	28	2764	C, D, P, K
SY2365-3	8192 x 8	300	100	--	+5	28	2764	C, D, P, K
SY2365A	8192 x 8	450	100	12	+5	28	2764	C, D, P, K
SY2365A-2	8192 x 8	200	100	12	+5	28	2764	C, D, P, K
SY2365A-3	8192 x 8	300	100	12	+5	28	2764	C, D, P, K
SY23128	16,384 x 8	200	100	10	+5	28	--	C, D, P, K
SY23256[2]	32,768 x 8	200	100	10	+5	28	--	C, D, P, K
SY3308R[2]	1024 x 8	35[3]	130	—	+5	24	82S181	C, D, P, K
SY3316R[2]	2048 x 8	35[3]	130	—	+5	24	82S191	C, D, P, K

ELECTRICALLY ERASABLE PROMs Commercial (T_A = 0°C to 70°C)

Part Number	Organization	Access Time (ns) Max	Maximum Current (mA) Operating	Maximum Current (mA) Standby	Power Supply (Volts)	Number of Pins	Package Type (Note 1)
SY2801	64 x 4	450	20	—	+5, +21	16	C, D, P
SY2801A	64 x 4	450	20	—	+5	16	C, D, P
SY2802	256 x 8	—	70	—	+5	18	C, D, P

NOTES:
1. C = Ceramic, D = Cerdip, F = Flatpack, K = Leadless Chip Carrier.
2. Preliminary Information.
3. Effective Access Time (t_{CPA}).

Synertek.

SY2316B

2048 x 8 Static Read Only Memory

Features

- Access Time 200/300/450 ns (max)
- 2048 x 8 Bit Organization
- Single +5 Volt Supply
- Totally Static Operation
- JEDEC Approved Pinout
- Completely TTL Compatible
- Three-State Outputs for Wire-OR Expansion
- Three Programmable Chip Selects
- Pin Compatible with 2716 EPROM
- Replacement for Two 2708s

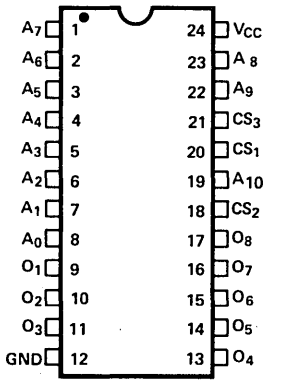
Description

The SY2316B high performance Read Only Memories are organized 2048 words by 8 bits with access times from 200 to 450 ns. The ROMs are designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. This device offers TTL input and output levels with a minimum of 0.4 Volt noise immunity in conjunction with a +5 Volt power supply.

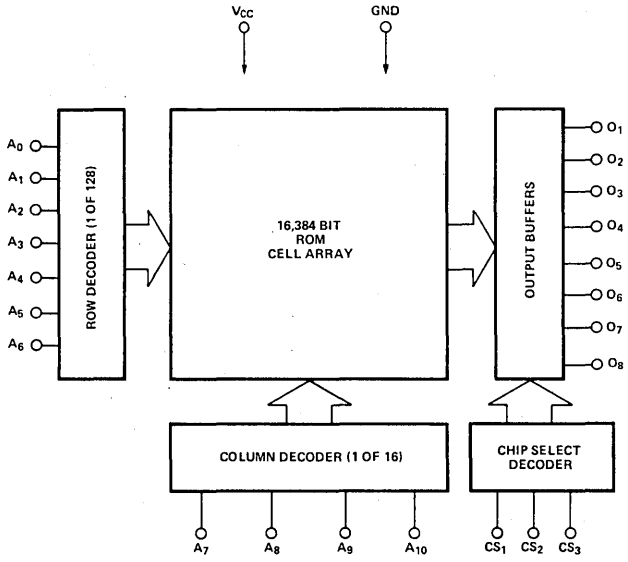
The SY2316B operates totally asynchronously. No clock input is required. The three programmable Chip Select inputs allow eight 16K ROMs to be OR-tied without external decoding. The device offers three-state output buffers for memory expansion.

Designed to replace the 2716 EPROM, the SY2316B can eliminate the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.

Pin Configuration



Block Diagram



Ordering Information

Order Number	Access Time (Max)	Operating Current (Max)	Package Type
SYD2316B	450 ns	98 mA	Cerdip
SYP2316B	450 ns	98 mA	Plastic
SYD2316B-2	200 ns	98 mA	Cerdip
SYP2316B-2	200 ns	98 mA	Plastic
SYD2316B-3	300 ns	98 mA	Cerdip
SYP2316B-3	300 ns	98 mA	Plastic

Synertek.

SY2332/SY2333

4096 x 8 Static Read Only Memory

Features

- SY2332-2532 EPROM Pin Compatible
- 4096 x 8 Bit Organization
- Single +5 Volt Supply (±10%)
- Access Time 200/300/450 ns (max.)
- Totally Static Operation
- Completely TTL Compatible
- SY2333-2732 EPROM Pin Compatible
- Three-State Outputs for Wire-OR Expansion
- Two Programmable Chip Selects
- EPROMS Accepted as Program Data Inputs
- JEDEC Approved Pinouts

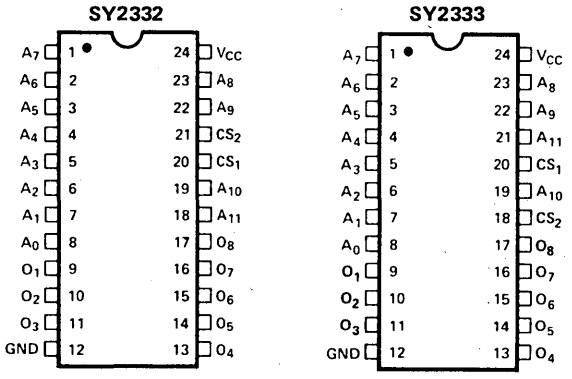
Description

The SY2332 and SY2333 high performance read only memories are organized 4096 words by 8 bits with access times from 200 ns to 450 ns. They are designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. These devices offer TTL input and output levels with a minimum of 0.4 Volt noise immunity in conjunction with a +5 Volt power supply.

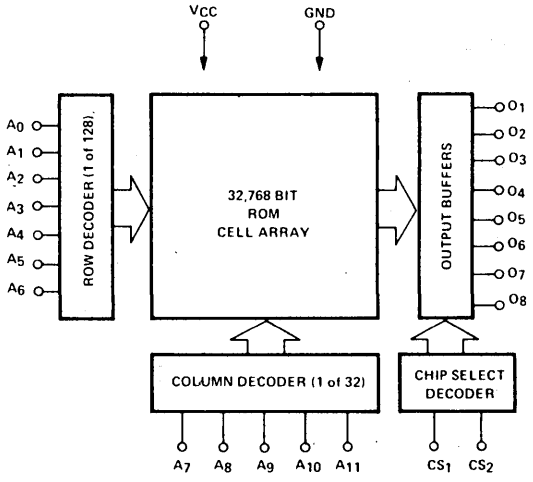
The SY2332 and SY2333 operate totally asynchronously. No clock input is required. The two programmable Chip Select inputs allow four 32K ROMs to be OR-tied without external decoding. Both devices offer three-state output buffers for memory expansion.

Designed to replace 32K EPROMs, the SY2332 and SY2333 can eliminate the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.

Pin Configurations



Block Diagram



Ordering Information

Order Number	Access Time	Operating Current	Package Type
SYD2332	450ns	100mA	Cerdip
SYP2332	450ns	100mA	Plastic
SYD2332-2	200ns	100mA	Cerdip
SYP2332-2	200ns	100mA	Plastic
SYD2332-3	300ns	100mA	Cerdip
SYP2332-3	300ns	100mA	Plastic
SYD2333	450ns	100mA	Cerdip
SYP2333	450ns	100mA	Plastic
SYD2333-2	200ns	100mA	Cerdip
SYP2333-2	200ns	100mA	Plastic
SYD2333-3	300ns	100mA	Cerdip
SYP2333-3	300ns	100mA	Plastic

A custom number will be assigned by Synertek.

Synertek

SY2365/SY2365A

8192 x 8 Static Read Only Memory

Features

- 2764 EPROM Pin Compatible
- 8192 x 8 Bit Organization
- Single +5 Volt Supply
- Access Time — 200/300/450 ns (max)
- Totally Static Operation
- Completely TTL Compatible
- 28 Pin JEDEC Approved Pinout
- SY2365A — Automatic Power Down ($\overline{CE}$)
  — Output Enable Function ($\overline{OE}$)
  — Two Programmable Chip Selects
- SY2365 — Non Power Down Version
  — Four Programmable Chip Selects
- Three State Outputs for Wire-OR Expansion
- EPROMs Accepted as Program Data Input

Description

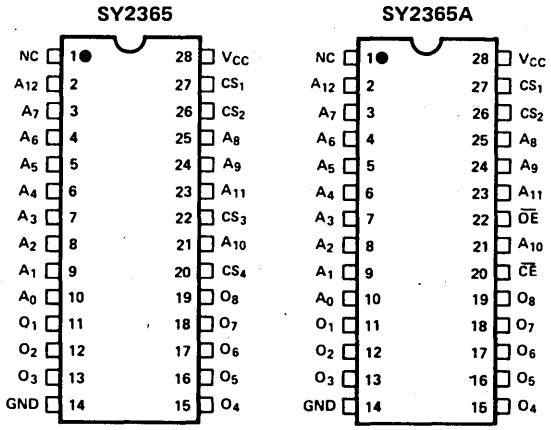
The SY2365 and SY2365A high performance Read Only Memories are organized 8192 words by 8 bits with access times from 200 ns to 450 ns. The ROMs are designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. Both ROMs conform to the JEDEC approved pinout for 28 pin 64K ROMs.

The SY2365 offers the simplest operation (no power down.) Its four programmable chip selects allow up to sixteen 64K ROMs to be OR-tied without external decoding.

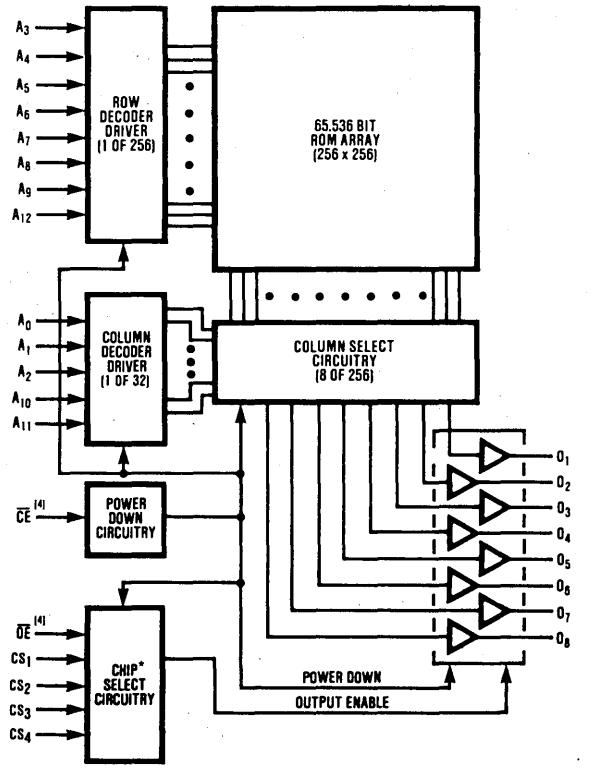
The SY2365A offers an automatic power down feature. Power down is controlled by the Chip Enable ($\overline{CE}$) input. When $\overline{CE}$ goes high, the device will automatically power down and remain in a low power standby mode as long as $\overline{CE}$ remains high. This unique feature provides system level power savings as much as 90%. An additional feature of the SY2365A is the Output Enable ($\overline{OE}$) function. This eliminates bus contention in multiple bus microprocessor systems. The two programmable chip selects allow up to four 64K ROMs to be OR-tied without external decoding.

Both the SY2365 and SY2365A are pin compatible with the 2764 EPROM thus eliminating the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.

Pin Configurations



Block Diagram



*CHIP SELECTS (CS) ARE PROGRAMMABLE LOW ACTIVE, HIGH ACTIVE OR DON'T CARE.

Synertek.

SY23128/SY23128A

16,384 x 8 Static Read Only Memory

Features

- EPROM Pin Compatible
- 16,384 x 8 Bit Organization
- Single +5 Volt Supply
- Access Time — 200/300/450 ns (max)
- Totally Static Operation
- Completely TTL Compatible
- 28 Pin JEDEC Approved Pinout
- SY23128A— Automatic Power Down ($\overline{CE}$)
  - — Output Enable Function ($\overline{OE}$)
  - — One Programmable Chip Select
- SY23128 — Non Power Down Version
  - — Three Programmable Chip Selects
- Three State Outputs for Wire-OR Expansion
- EPROMS Accepted as Program Data Input

Description

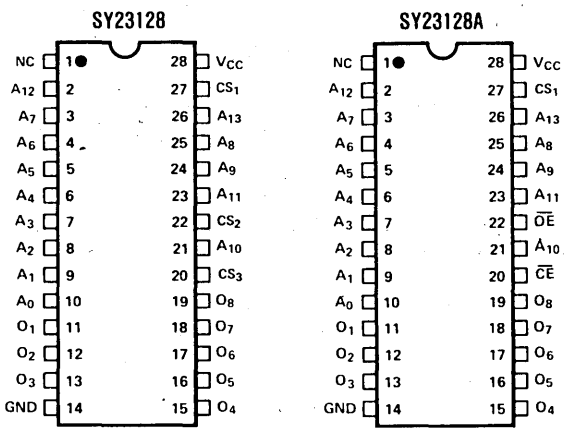
The SY23128 and SY23128A high performance Read Only Memories are organized 16,384 words by 8 bits with access times from 200 ns to 450 ns. The ROMs are designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. Both ROMs conform to the JEDEC approved pinout for 28 pin 128K ROMs.

The SY23128 offers the simplest operation (no power down.) Its three programmable chip selects allow up to eight 128K ROMs to be OR-tied without external decoding.

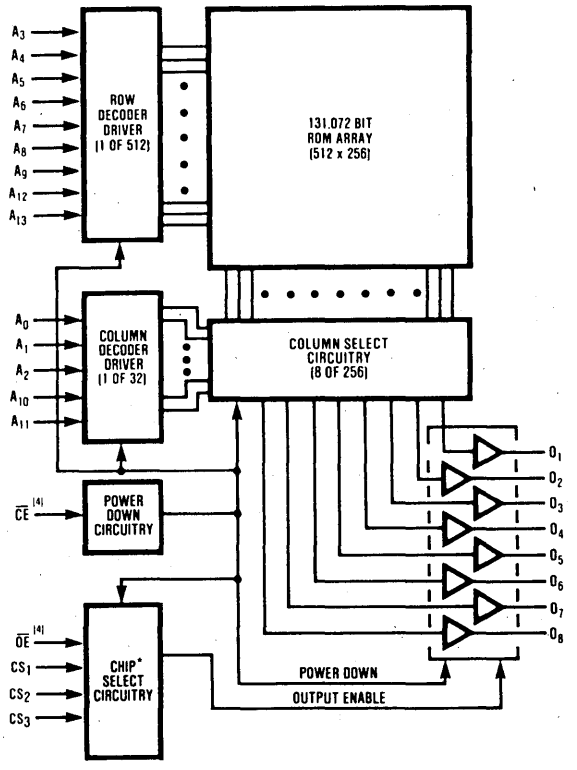
The SY23128A offers an automatic power down feature. Power down is controlled by the Chip Enable ($\overline{CE}$) input. When $\overline{CE}$ goes high, the device will automatically power down and remain in a low power standby mode as long as $\overline{CE}$ remains high. This unique feature provides system level power savings as much as 90%. An additional feature of the SY23128A is the Output Enable ($\overline{OE}$) function. This eliminates bus contention in multiple bus microprocessor systems. The programmable chip select allows two 128K ROMs to be OR-tied without external decoding.

Both the SY23128 and SY23128A are pin compatible with EPROMs thus eliminating the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.

Pin Configurations



Block Diagram



*CHIP SELECTS (CS) ARE PROGRAMMABLE LOW ACTIVE HIGH ACTIVE, OR DON'T CARE

Synertek.

SY23256/SY23256A

32,768 x 8 Static Read Only Memory

Features

- EPROM Pin Compatible
- 32,768 x 8 Bit Organization
- Single +5 Volt Supply
- Access Time — 200/300/450 ns (max)
- Totally Static Operation
- Completely TTL Compatible
- 28 Pin JEDEC Approved Pinout
- SY23256A— Automatic Power Down ($\overline{CE}$)
  - Output Enable Function ($\overline{OE}$)
- SY23256 — Non Power Down Version
  - Two Programmable Chip Selects
- Three State Outputs for Wire-OR Expansion
- EPROMs Accepted as Program Data Input

Description

The SY23256 and SY23256A high performance Read Only Memories are organized 32,768 words by 8 bits with access times from 200 ns to 450 ns. The ROMs are designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. Both ROMs conform to the JEDEC approved pinout for 28 pin 256K ROMs.

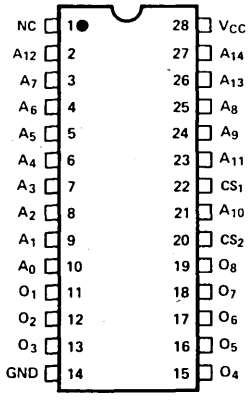
The SY23256 offers the simplest operation (no power down.) Its two programmable chip selects allow up to four 256K ROMs to be OR-tied without external decoding.

The SY23256A offers an automatic power down feature. Power down is controlled by the Chip Enable ($\overline{CE}$) input. When $\overline{CE}$ goes high, the device will automatically power down and remain in a low power standby mode as long as $\overline{CE}$ remains high. This unique feature provides system level power savings as much as 90%. An additional feature of the SY23256A is the Output Enable ($\overline{OE}$) function. This eliminates bus contention in multiple bus microprocessor systems.

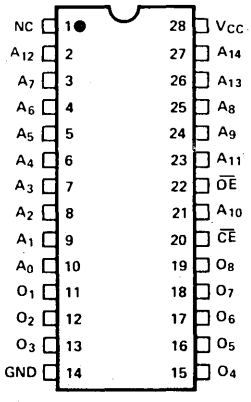
Both the SY23256 and SY23256A are pin compatible with EPROMs thus eliminating the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.

Pin Configurations

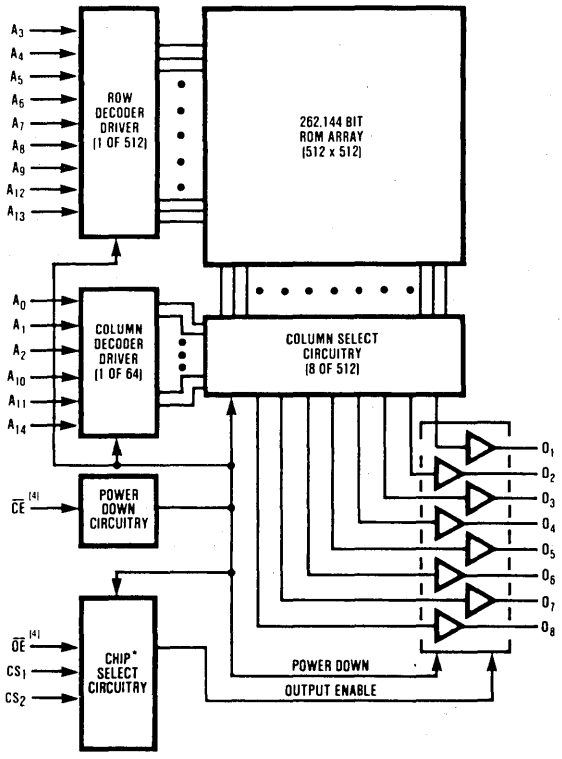
SY23256



SY23256A



Block Diagram



*CHIP SELECTS (CS) ARE PROGRAMMABLE LOW ACTIVE, HIGH ACTIVE, OR DON'T CARE.

Synertek.

SY3308

1024 x 8 High Speed Read Only Memory

Features

- Access Time – 70 ns (max)
- Single +5 Volt Supply
- Contact Programming
- Four Week Prototype Turnaround
- Completely TTL Compatible
- Totally Static Operation
- Pin Compatible with 8K Bipolar PROMs – Replaces 7681 or 82S181
- Three-State Outputs for Wire-OR Expansion
- Four Programmable Chip Selects
- 8K Bipolar PROMs Accepted as Program Data Inputs

Description

The Synertek SY3308 is a high speed 16,384-bit static mask programmable Read Only Memory organized 1024 words by 8 bits. Designed to be compatible with industry standard 8K bipolar PROMs, it eliminates the need to redesign printed circuit boards for volume production after prototyping with PROM's. The device offers full TTL compatibility on all inputs and outputs and operates on a single +5V power supply. The three-state output buffers facilitate system expansion by allowing outputs to be wire-ORed together. These features, combined with a maximum access time of 70 nsec, make the SY3308 suitable for application where high performance, large bit storage and simple interface are important design considerations.

The SY3308 utilizes fully static circuitry and operates asynchronously so no clocks are required. The four chip select buffers are mask programmable to be any combination of high active, low active or don't care that is desired. This allows up to sixteen ROM's to be OR-tied without external decoding.

The SY3308 is fabricated using Synertek's scaled, high performance N-channel MOS technology. This, combined with inovative design techniques, provides the high performance and ease-of-use features associated with non-clocked static memories.

SY3316/SY3316A

2048 x 8 High Speed Read Only Memory

Features

- Access Time — 80ns (max)
- Single +5 Volt Supply (± 10%)
- Contact Programming
- Four Week Prototype Turnaround
- Completely TTL Compatible
- Totally Static Operation
- SY3316A — Automatic Power Down ($\overline{CE}$)
- Pin Compatible with 16K Bipolar PROMs — Replaces 3636 or 82S191
- Three-State Outputs for Wire-OR Expansion
- Three Programmable Chip Selects (two on SY3316A)
- 16K Bipolar PROMs Accepted as Program Data Inputs

Description

The SY3316 and SY3316A are high speed 16,384 bit static mask programmable Read Only Memories organized 2048 words by 8 bits. Designed to be pin compatible with 16K bipolar PROMs, they eliminate the need to redesign printed circuit boards for volume production after prototyping with PROMs.

The SY3316A offers an automatic power down feature. Power down is controlled by the Chip Enable ($\overline{CE}$) input. When $\overline{CE}$ goes high, the device will automatically power down and remain in a standby power mode as long as $\overline{CE}$ remains high. This unique feature provides system level power savings of as much as 80%. The two programmable chip selects (CS) allow as many as four ROMs to be OR-tied without external decoding.

The SY3316 offers somewhat simpler operation than the SY3316A. It's three programmable chip selects allow up to eight ROMs to be OR-tied without external decoding.

Both devices are fabricated using Synertek's scaled high performance N-channel MOS technology. This, combined with innovative design techniques, provides the high performance and ease-of-use features associated with static memories.

Synertek.

SY3308R
1024 x 8 High Speed Read Only Memory

Features

- Effective Access time (t_{CPA}) = 35 ns (max)
- Single 5 Volt Supply
- Contact Programming
- Four Week Prototype Turnaround
- Completely TTL Compatible
- Totally Static Operation
- Pin Compatible with 8K Bipolar PROMs — Replaces 7681 or 82S181
- Registered Outputs
- 8K Bipolar PROMs Accepted as Program Data Inputs

Description

The Synertek SY3308R is a high speed 8192-bit static mask programmable Read Only Memory organized 1024 words by 8 bits. Designed to be compatible with industry standard 8K bipolar PROMs, it eliminates the need to redesign printed circuit boards for volume production after prototyping with PROMs. The device offers full TTL compatibility on all inputs and outputs and operates on a single +5V power supply. The SY3308R has a registered output that allows pipelining. These features, combined with an effective access time of 35 nsec, make the SY3308R suitable for application where high performance, large bit storage and simple interface are important design considerations.

The SY3308R has a latch in the output that allows the memory to stack data so that the effective access time (time from data out to data out) is 35 ns.

The SY3308R is fabricated using Synertek's scaled, high performance N-channel MOS technology. This, combined with innovative design techniques, provides the high performance and ease-of-use features associated with non-clocked static memories.

SY3316R
2048 x 8 High Speed Read Only Memory

Features

- Effective Access time (t_{CPA}) = 35 ns (max)
- Single +5V Supply (±10%)
- Contact Programming
- Four Week Prototype Turnaround
- Completely TTL Compatible
- Totally Static Memory
- Pin Compatible with 16K Bipolar PROMs — Replaces 3636 or 82S191
- Three-State Outputs for Wire-OR Expansion
- 16K Bipolar PROMs Accepted as Program Data Inputs

Description

The S3316R is a high speed 16,384 bit static mask programmable Read Only Memory organized 2048 words by 8 bits. Designed to be pin compatible with 16K bipolar PROMs, they eliminate the need to redesign printed circuit boards for volume production after prototyping with PROMs.

The device offers full TTL compatibility on all inputs and outputs and operates on a single +5V power supply.

The SY3316R has a registered output that allows pipelining. These features, combines with an effective access time of 35 ns, makes the SY3316R suitable for applications where high performance, large bit storage, and simple interface are important design considerations.

The SY3316 has a latch in the output that allows the memory to stack data so that the effective access time (time from data out to data out) is 40 ns.

The device is fabricated using Synertek's scaled high performance N-channel MOS technology. This, combined with innovatove design techniques, provides the high performance and ease-of-use features associated with static memories.

Synertek.

SY2801A

64 x 4 Electrically Erasable Programmable ROM

Features

- 450 ns Address Access Time
- Fully Static Operation
- Low Power Dissipation 110 mW Max.
- Full TTL Compatibility: All Inputs and Outputs
- Three State Outputs
- Single +5V Operation: Both Read and Program Modes
- Single Word Erase/Write Capability
- 10 ms Word Erase/Write Time
- Chip Erase Time of 10 ms
- Erase/Write Specifications Guaranteed 0-70°C

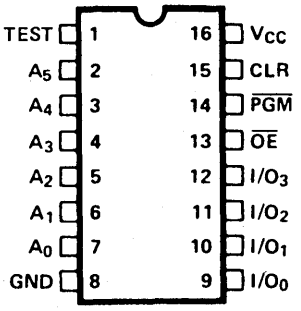
Description

The Synertek SY2801A is a 256 bit electrically erasable programmable read only memory (E^2PROM) organized 64 words by four bits and is fabricated using Synertek's double poly silicon gate n-channel technology. The device can be easily erased and reprogrammed on a word basis. A chip erase function is also provided. The SY2801A utilizes an on-board high voltage generator to provide all the internal voltages necessary to program and erase the chip. The single +5V power supply is the only power supply required.

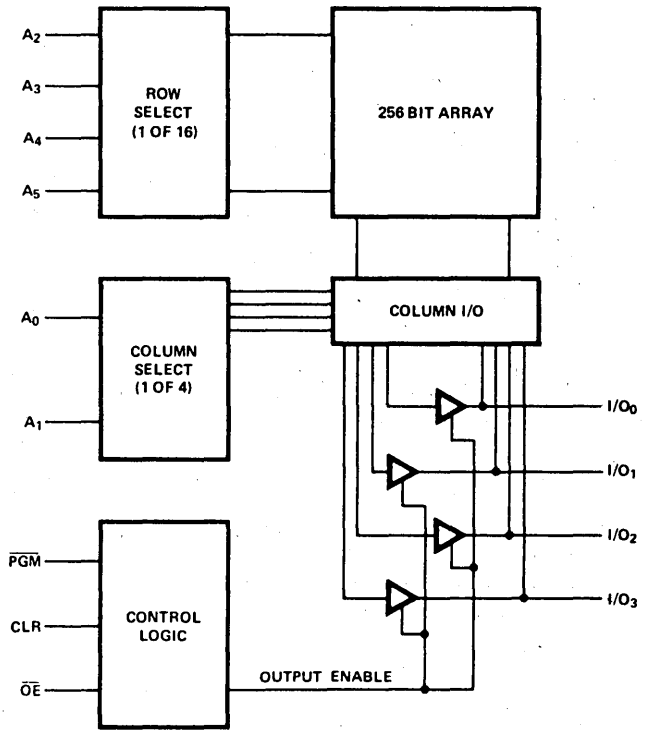
The in-system erase/write capability of the SY2801A makes it suitable for a wide variety of applications requiring a small amount of alterable, non-volatile storage. Any word can be erased or programmed in 10 ms without affecting the rest of the memory. Alternatively, the entire memory can be erased in 10 ms. Both the erase and write operations are accomplished with the applications of a single TTL level pulse.

The SY2801A utilizes fully static circuitry and is completely TTL compatible. The common data input/outputs with three-state output drivers greatly simplifies interface with systems utilizing a bidirectional data bus. The device is packaged in a 16-pin DIP for optimum density.

Pin Configuration



Block Diagram



Synertek.

SY2802E

256 x 8 Electrically Erasable Programmable ROM

Features

- Reliable Floating Gate Technology
- Microprocessor Compatible Architecture
- On-Chip Address/Data Latches
- Single Byte Erase/Write Capability
- Fully TTL Compatible
- Single +5V Operation
- Erase/Write Specifications Guaranteed 0-70°C
- Low Power Dissipation: 385 mW Max.
- On-Chip ERASE/WRITE Control
- Both $\overline{BUSY}$ Signal and Status Register

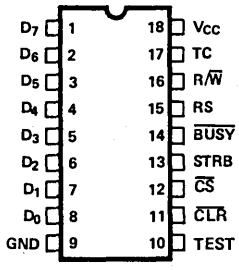
Description

The SY2802E is a 2048 bit electrically erasable programmable read-only memory (E^2PROM) organized as 256 words by eight bits. Fabricated using Synertek's double poly silicon gate n-channel technology, the device utilizes a novel memory architecture that results in the memory operating as a non-volatile register file. A single bidirectional eight bit data port is used for transmitting the address, data and status information. Both address and input data are latched into onboard registers eliminating the need to hold them valid during the long erase/write operation. In addition, all the erase/write control logic is incorporated on chip completely freeing the microprocessor once the erase/write cycle has been initiated. Both a $\overline{BUSY}$ signal and status register are available to facilitate easy interface in a wide variety of microprocessor based systems.

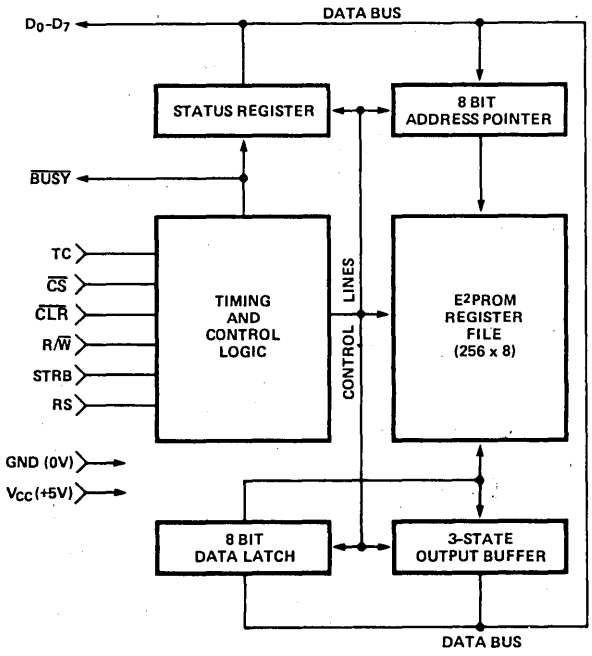
The in-system erase/write capability of the SY2802E make it suitable for a wide variety of applications requiring a small amount of alterable, non-volatile storage. Any byte can be erased and written without affecting the rest of memory. Alternatively, the entire memory can be erased.

The SY2802E utilizes fully static circuitry and is completely TTL compatible in the read and erase/write modes. The device has an on-chip high voltage generator eliminating the need for any high voltage pulses or power supplies. The single +5V power supply is all that is required for any operation.

Pin Configuration



Block Diagram



Ordering Information

Order Number	Select Access Time	Cycle Time (Min)	Supply Current (Max)	Package Type
SYD2802E	110ns	240	70mA	Cerdip
SYP2802E	110ns	240	70mA	Plastic

TMS 4164 JDL, NL, FPL
65,536-BIT DYNAMIC RANDOM-ACCESS MEMORY

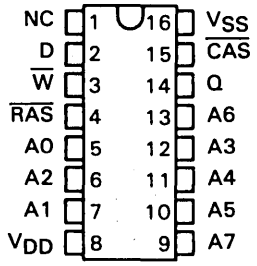
JULY 1980 – REVISED MAY 1982

- 65,536 X 1 Organization
- Single +5 V Supply (10% Tolerance)
- JEDEC Standardized Pin Out in Dual-In-Line Packages
- Upward Pin Compatible with TMS 4116 (16K Dynamic RAM)
- Performance Ranges:

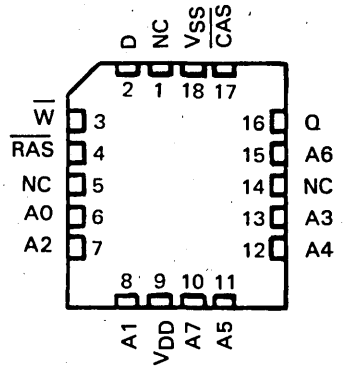
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ, MODIFY, WRITE CYCLE (MIN)
TMS 4164-12	120 ns	75 ns	230 ns	260 ns
TMS 4164-15	150 ns	100 ns	260 ns	285 ns
TMS 4164-20	200 ns	135 ns	330 ns	345 ns
TMS 4164-25	250 ns	165 ns	410 ns	455 ns

- Long Refresh Period . . . 4 milliseconds
- Low Refresh Overhead Time . . . As Low As 1.8% of Total Refresh Period
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Unlatched Output
- Common I/O Capability with "Early Write" Feature
- Page-Mode Operation for Faster Access
- Low Power Dissipation
  - Operating . . . 125 mW (typ.)
  - Standby . . . 17.5 mW (typ.)
- New SMOS (Scaled-MOS) N-Channel Technology

16-PIN CERAMIC AND PLASTIC DUAL-IN-LINE PACKAGES (TOP VIEW)



18-PIN PLASTIC CHIP CARRIER PACKAGE (TOP VIEW)



PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column Address Strobe
D	Data In
NC	No-Connect
Q	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Write Enable
V_{DD}	+5 V Supply
V_{SS}	Ground

description

The TMS 4164 is a high-speed, 65,536-bit, dynamic random-access memory, organized as 65,536 words of one bit each. It employs state-of-the-art SMOS (scaled MOS) N-channel double-level polysilicon gate technology for very high performance combined with low cost and improved reliability.

The TMS 4164 features $\overline{RAS}$ access times of 120 ns, 150 ns, 200 ns, or 250 ns maximum. Power dissipation is 125 mW typical operating, 17.5 mW typical standby.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data-in are latched on chip to simplify system design. Data-out is unlatched to allow greater system flexibility. Pin 1 has no internal connection to allow compatibility with other 64K RAMs that use this pin for an additional function.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TMS 4416 NL
16,384-WORD BY 4-BIT DYNAMIC RAM

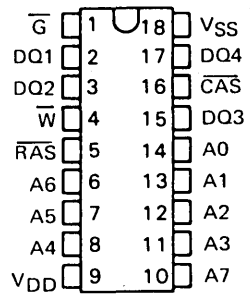
AUGUST 1980 – REVISED JUNE 1982

- 16,384 X 4 Organization
- Single +5 V Supply (10% Tolerance)
- Performance Ranges:

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ, MODIFY, WRITE CYCLE (MIN)
TMS 4416-15	150 ns	80 ns	260 ns	360 ns
TMS 4416-20	200 ns	120 ns	330 ns	440 ns
TMS 4416-25	250 ns	150 ns	410 ns	560 ns

- Long Refresh Period . . . 4 milliseconds
- Low Refresh Overhead Time . . . As Low As 1.7% of Total Refresh Period
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Unlatched Outputs
- Early Write or $\overline{G}$ to Control Output Buffer Impedance
- Page-mode Operation for Faster Access
- Low Power Dissipation
  - Operating . . . 130 mW (typ)
  - Standby . . . 17.5 mW (typ)
- New SMOS (Scaled-MOS) N-Channel Technology

18-PIN PLASTIC DUAL-IN-LINE PACKAGE (TOP VIEW)



PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column Address Strobe
DQ1-DQ4	Data In/Data Out
$\overline{G}$	Output Enable
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Write Enable
V_{DD}	+5 V Supply
V_{SS}	Ground

description

The TMS 4416 NL is a high speed, 65,536-bit, dynamic, random-access memory, organized as 16,384 words of 4 bits each. It employs state-of-the-art SMOS (scaled MOS) N-channel double-level polysilicon gate technology for very high performance combined with low cost and improved reliability.

The TMS 4416 NL features $\overline{RAS}$ access times to 150 ns maximum. Power dissipation is 130 mW typical operating, 17.5 mW typical standby.

New SMOS technology permits operation from a single +5 V supply, reducing system power supply and decoupling requirements, and easing board layout. I_{DD} peaks have been reduced to 60 mA typical, and a −1 V input voltage undershoot can be tolerated, minimizing system noise considerations. Input clamp diodes are used to ease system design.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data-in are latched on chip to simplify system design. Data-out is unlatched to allow greater system flexibility.

The TMS 4416 NL is offered in an 18-pin dual-in-line plastic package and is guaranteed for operation from 0°C to 70°C. Packages are designed for insertion in mounting-hole rows on 300 mil (7.62mm) centers.

ADVANCE INFORMATION
This document contains information on a new product. Specifications are subject to change without notice.

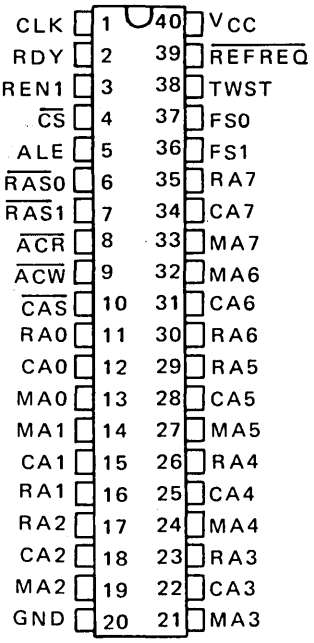
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS TEXAS 75265

TMS 4500A NL
DYNAMIC RAM CONTROLLER

JANUARY 1982

- Controls Operation of 8K/16K/32K/64K Dynamic RAMs
- Creates Static RAM Appearance
- One Package Contains Address Multiplexer, Refresh Control, and Timing Control
- Directly Addresses and Drives Up to 256K Bytes of Memory Without External Drivers
- Operates from Microprocessor Clock
  - No Crystals, Delay Lines, or RC Networks
  - Eliminates Arbitration Delays
- Refresh May Be Internally or Externally Initiated
- Versatile
  - Strap-Selected Refresh Rate
  - Synchronous, Predictable Refresh
  - Selection of Distributed, Transparent, and Cycle-Steal Refresh Modes
  - Interfaces Easily to Popular Microprocessors
- Strap-Selected Wait State Generation for Microprocessor/Memory Speed Matching
- Ability to Synchronize or Interleave Controller with the Microprocessor System (Including Multiple Controllers)
- Three-State Outputs Allow Multiport Memory Configuration

TMS 4500A
40-PIN 600-MIL PLASTIC
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The TMS 4500A is a monolithic DRAM system controller designed to provide address multiplexing, timing, control and refresh/access arbitration functions to simplify the interface of dynamic RAMs to microprocessor systems.

The controller contains a 16-bit multiplexer that generates the address lines for the memory device from the 16 system address bits and provides the strobe signals required by the memory to decode the address. An 8-bit refresh counter generates the 256-row addresses required for refresh.

A refresh timer is provided that generates the necessary timing to refresh the dynamic memories and assure data retention.

The TMS 4500A also contains refresh/access arbitration circuitry to resolve conflicts between memory access requests and memory refresh cycles. The TMS 4500A is offered in a 40-pin, 600-mil dual-in-line plastic package and is guaranteed for operation from 0°C to 70°C.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

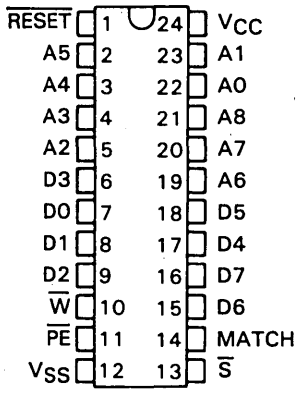
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TMS 2150 JL
CACHE ADDRESS COMPARATOR

MARCH 1982

- Fast Address to Match Valid Delay — Four Speed Ranges: 45 ns, 55 ns, 70 ns, 90 ns
- 512 X 9 Internal RAM
- 300-Mil 24-Pin Ceramic DIP
- Max Power Dissipation: 660 mW
- On-Chip Parity Generation and Checking
- Parity Error Output/Force Parity Error Input
- On-Chip Address/Data Comparator
- Asynchronous, Single-Cycle Reset
- Easily Expandable
- Fully Static, TTL Compatible
- Reliable SMOS (Scaled NMOS) Technology

J PACKAGE
(TOP VIEW)



description

The 8-bit-slice cache address comparator consists of a high-speed 512 X 9 static RAM array, parity generator, and parity checker, and 9-bit high-speed comparator. It is fabricated using N-channel silicon gate technology for high speed and simple interface with MOS and bipolar TTL circuits. The cache address comparator is easily cascadable for wider tag addresses or deeper tag memories. Significant reductions in cache memory component count, board area, and power dissipation can be achieved with this device.

When $\overline{S}$ is low and $\overline{W}$ is high, the cache address comparator compares the contents of the memory location addressed by A0-A8 with the data on D0-D7 plus generated parity. An equality is indicated by a high level on the MATCH output. A low-level output from $\overline{PE}$ signifies a parity error in the internal RAM data. $\overline{PE}$ is an N-channel open-drain output for easy OR-tieing. During a write cycle ($\overline{S}$ and $\overline{W}$ low), data on D0-D7 plus generated even parity are written in the 9-bit memory location addressed by A0-A8. Also during write, a parity error may be forced by holding $\overline{PE}$ low.

A $\overline{RESET}$ input is provided for initialization. When $\overline{RESET}$ goes low, all 512 X 9 RAM locations will be cleared and the MATCH output will be forced high.

The cache address comparator operates from a single +5 V supply and is offered in a 24-pin 300-mil CERPAK. The device is fully TTL compatible and is guaranteed to operate from 0 °C to 70 °C.

MATCH OUTPUT DESCRIPTION

MATCH = V_{OH} if: [A0-A8] = D0-D7 + parity,
or: $\overline{RESET} = V_{IL}$,
or: $\overline{S} = V_{IH}$,
or: $\overline{W} = V_{IL}$

MATCH = V_{OL} if: [A0-A8] ≠ D0-D7 + parity, with $\overline{RESET} = V_{IH}$, $\overline{S} = V_{IL}$, and $\overline{W} = V_{IH}$

FUNCTION TABLE

OUTPUT		FUNCTION
MATCH	$\overline{PE}$	DESCRIPTION
L	L	Parity Error
L	H	Not Equal
H	L	Undefined Error
H	H	Equal

Where $\overline{S} = V_{IL}$, $\overline{W} = V_{IH}$, $\overline{RESET} = V_{IH}$

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

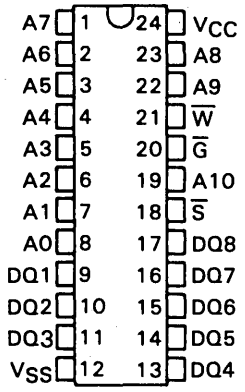
TMS 4016 NL
2048-WORD BY 8-BIT STATIC RAM

FEBRUARY 1981 – REVISED DECEMBER 1981

- 2K X 8 Organization, Common I/O
- Single +5 V Supply
- Fully Static Operation (No Clocks, No Refresh)
- JEDEC Standard Pinout
- 24-Pin 600 Mil (15.2 mm) Package Configuration
- Plug-in Compatible with 16K 5 V EPROMs
- 8-Bit Output for Use in Microprocessor-Based Systems
- 3-State Outputs with $\overline{S}$ for OR-ties
- $\overline{G}$ Eliminates Need for External Bus Buffers
- All Inputs and Outputs Fully TTL Compatible
- Fanout to Series 74, Series 74S or Series 74LS TTL Loads
- N-Channel Silicon-Gate Technology
- Power Dissipation Under 385 mW Max
- Guaranteed dc Noise Immunity of 400 mV with Standard TTL Loads
- 4 Performance Ranges:

	ACCESS TIME (MAX)
TMS 4016-12	120 ns
TMS 4016-15	150 ns
TMS 4016-20	200 ns
TMS 4016-25	250 ns

TMS 4016
24-PIN PLASTIC
DUAL-IN-LINE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A10	Addresses
DQ1-DQ8	Data In/Data Out
$\overline{S}$	Chip Select
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{SS}	Ground
V_{CC}	+5 V Supply

description

The TMS 4016 static random-access memory is organized as 2048 words of 8 bits each. Fabricated using proven N-channel, silicon-gate MOS technology, the TMS 4016 operates at high speeds and draws less power per bit than 4K static RAMs. It is fully compatible with Series 74, 74S, or 74LS TTL. Its static design means that no refresh clocking circuitry is needed and timing requirements are simplified. Access time is equal to cycle time. A chip select control is provided for controlling the flow of data-in and data-out and an output enable function is included in order to eliminate the need for external bus buffers.

Of special importance is that the TMS 4016 static RAM has the same standardized pinout as TI's compatible EPROM family. This, along with other compatible features, makes the TMS 4016 plug-in compatible with the TMS 2516 (or other 16K 5 V EPROMs). Minimal, if any modifications are needed. This allows the microprocessor system designer complete flexibility in partitioning his memory board between read/write and non-volatile storage.

The TMS 4016 is offered in the plastic (NL suffix) 24-pin dual-in-line package designed for insertion in mounting hole rows on 600-mil (15.2 mm) centers. It is guaranteed for operation from 0°C to 70°C.

TEXAS INSTRUMENTS
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TEXAS INSTRUMENTS
INCORPORATED

Bipolar Programmable Read-Only Memories Series 24 and Series 28

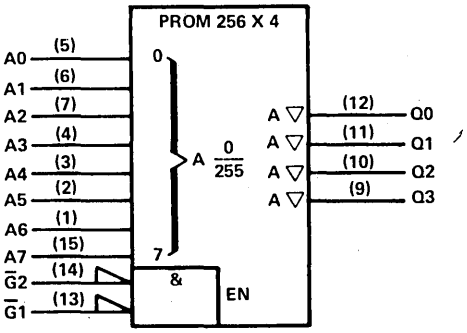
- High-Performance Schottky PROMs
- Low-Power PROMs
- Power-Down PROMs
- Registered-Output PROMs
- Ceramic DIP or Chip Carrier for Military of Industrial Applications
- Plastic DIP or Chip Carrier for Commercial Applications

TBP14S10 ('S287)

PROGRAMMABLE READ-ONLY MEMORIES

- 256 X 4
- Three-state outputs
- Typical address access time . . . 42 ns
- Typical power . . . 500 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A6	9 Q3
2 A5	10 Q2
3 A4	11 Q1
4 A3	12 Q0
5 A0	13 G1
6 A1	14 G2
7 A2	15 A7
8 GND	16 V_{CC}

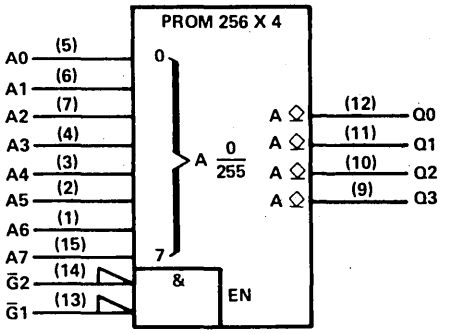
For chip carrier options and information, contact the factory.

TBP14SA10 ('S387)

PROGRAMMABLE READ-ONLY MEMORIES

- 256 X 4
- Open-collector outputs
- Typical address access time . . . 42 ns
- Typical power . . . 500 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A6	9 Q3
2 A5	10 Q2
3 A4	11 Q1
4 A3	12 Q0
5 A0	13 G1
6 A1	14 G2
7 A2	15 A7
8 GND	16 V_{CC}

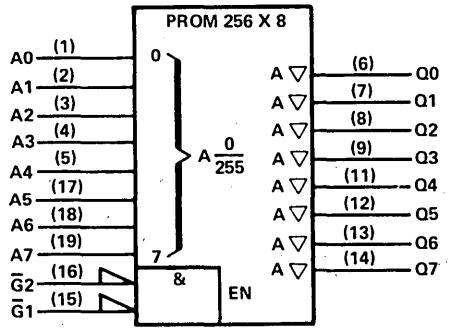
For chip carrier options and information, contact the factory.

TBP18S22 ('S471)

PROGRAMMABLE READ-ONLY MEMORIES

- 256 X 8
- Three-state outputs
- Typical address access time . . . 50 ns
- Typical power . . . 550 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A0	11 Q4
2 A1	12 Q5
3 A2	13 Q6
4 A3	14 Q7
5 A4	15 $\overline{G1}$
6 Q0	16 $\overline{G2}$
7 Q1	17 A5
8 Q2	18 A6
9 Q3	19 A7
10 GND	20 V_{CC}

For chip carrier options and information, contact the factory.

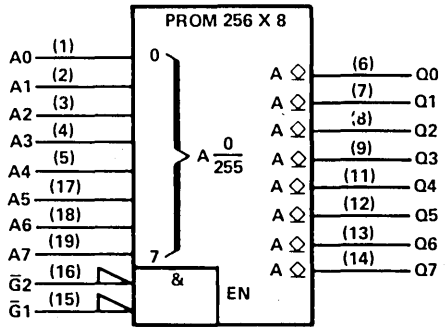
† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TBP18SA22 ('S470)

PROGRAMMABLE READ-ONLY MEMORIES

- 256 X 8
- Open-collector outputs
- Typical address access time . . . 50 ns
- Typical power . . . 550 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A0	11 Q4
2 A1	12 Q5
3 A2	13 Q6
4 A3	14 Q7
5 A4	15 $\overline{G}1$
6 Q0	16 $\overline{G}2$
7 Q1	17 A5
8 Q2	18 A6
9 Q3	19 A7
10 GND	20 V_{CC}

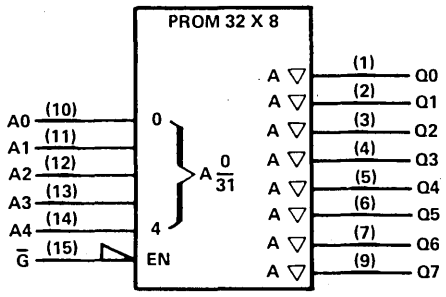
For chip carrier options and information, contact the factory.

TBP18S030 ('S288)

PROGRAMMABLE READ-ONLY MEMORIES

- 32 X 8
- Three-state outputs
- Typical address access time . . . 25 ns
- Typical power . . . 400 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 Q0	9 Q7
2 Q1	10 A0
3 Q2	11 A1
4 Q3	12 A2
5 Q4	13 A3
6 Q5	14 A4
7 Q6	15 $\overline{G}$
8 GND	16 V_{CC}

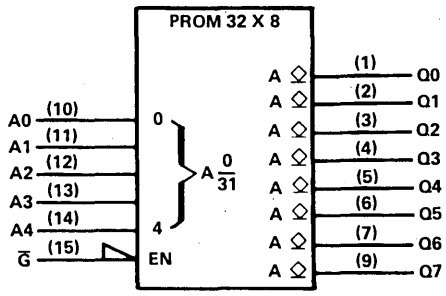
For chip carrier options and information, contact the factory.

TBP18SA030 ('S188)

PROGRAMMABLE READ-ONLY MEMORIES

- 32 X 8
- Open-collector outputs
- Typical address access time . . . 25 ns
- Typical power . . . 400 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 Q0	9 Q7
2 Q1	10 A0
3 Q2	11 A1
4 Q3	12 A2
5 Q4	13 A3
6 Q5	14 A4
7 Q6	15 $\overline{G}$
8 GND	16 V_{CC}

For chip carrier options and information, contact the factory.

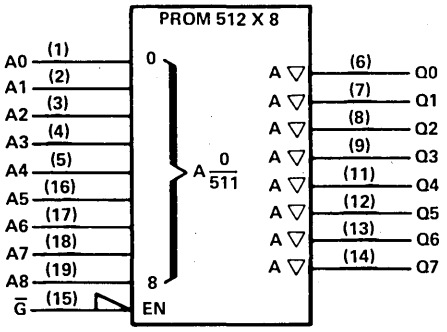
† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TBP18S42 ('S472)

PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Three-state outputs
- Typical address access time . . . 55 ns
- Typical power . . . 600 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A0	11 Q4
2 A1	12 Q5
3 A2	13 Q6
4 A3	14 Q7
5 A4	15 $\overline{G}$
6 Q0	16 A5
7 Q1	17 A6
8 Q2	18 A7
9 Q3	19 A8
10 GND	20 V_{CC}

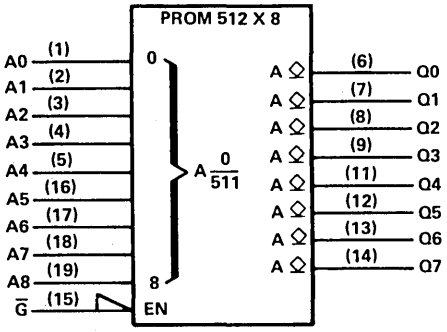
For chip carrier options and information, contact the factory.

TBP18SA42 ('S473)

PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Open-collector outputs
- Typical address access time . . . 55 ns
- Typical power . . . 600 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A0	11 Q4
2 A1	12 Q5
3 A2	13 Q6
4 A3	14 Q7
5 A4	15 $\overline{G}$
6 Q0	16 A5
7 Q1	17 A6
8 Q2	18 A7
9 Q3	19 A8
10 GND	20 V_{CC}

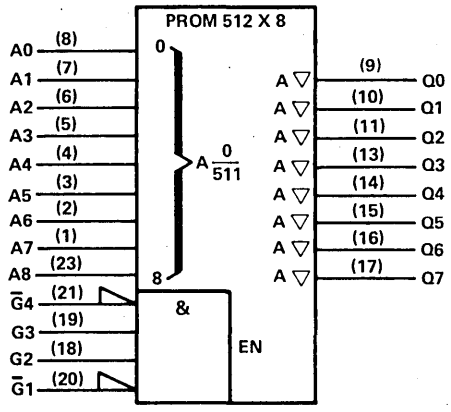
For chip carrier options and information, contact the factory.

TBP18S46 ('S474)

PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Three-state outputs
- Typical address access time . . . 55 ns
- Typical power . . . 600 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G1}$
9 Q0	21 $\overline{G4}$
10 Q1	22 nc
11 Q2	23 A8
12 GND	24 V_{CC}

For chip carrier options and information, contact the factory.

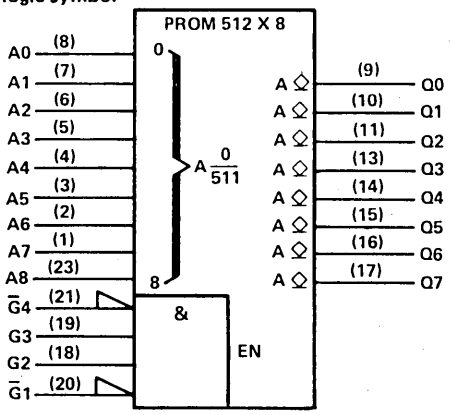
† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TBP18SA46 ('S475)

PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Open-collector outputs
- Typical address access time . . . 55 ns
- Typical power . . . 600 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G1}$
9 Q0	21 $\overline{G4}$
10 Q1	22 nc
11 Q2	23 A8
12 GND	24 V_{CC}

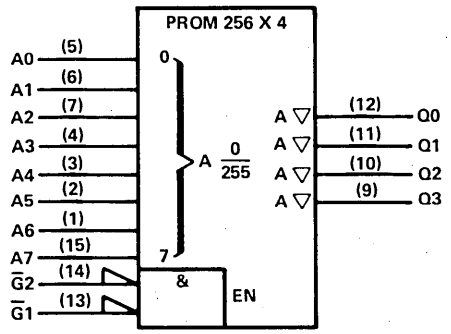
For chip carrier options and information, contact the factory.

TBP24S10

PROGRAMMABLE READ-ONLY MEMORIES

- 256 X 4
- Three-state outputs
- Typical address access time . . . 35 ns
- Typical select time . . . 20 ns
- Typical power . . . 375 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A6	9 Q3
2 A5	10 Q2
3 A4	11 Q1
4 A3	12 Q0
5 A0	13 G1
6 A1	14 G2
7 A2	15 A7
8 GND	16 V_{CC}

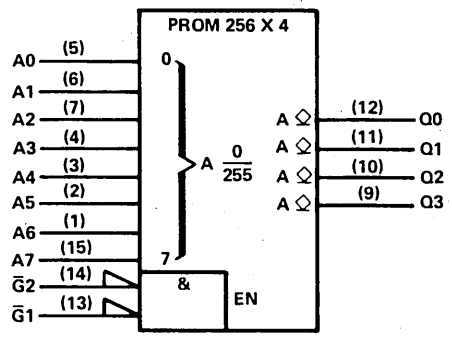
For chip carrier options and information, contact the factory.

TBP24SA10

PROGRAMMABLE READ-ONLY MEMORIES

- 256 X 4
- Open-collector outputs
- Typical address access time . . . 35 ns
- Typical select time . . . 20 ns
- Typical power . . . 375 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A6	9 Q3
2 A5	10 Q2
3 A4	11 Q1
4 A3	12 Q0
5 A0	13 G1
6 A1	14 G2
7 A2	15 A7
8 GND	16 V_{CC}

For chip carrier options and information, contact the factory.

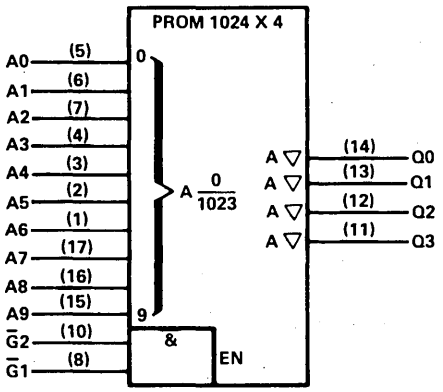
† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TBP24S41 ('S476)

PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 4
- Three-state outputs
- Typical address access time . . . 40 ns
- Typical select time . . . 20 ns
- Typical power . . . 475 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A6	10 $\overline{G}2$
2 A5	11 Q3
3 A4	12 Q2
4 A3	13 Q1
5 A0	14 Q0
6 A1	15 A9
7 A2	16 A8
8 $\overline{G}1$	17 A7
9 GND	18 V_{CC}

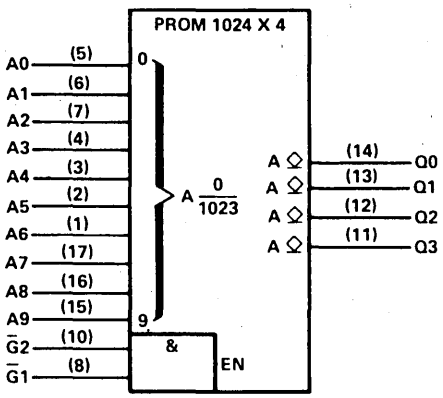
For chip carrier options and information, contact the factory.

TBP24SA41 ('S477)

PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 4
- Open-collector outputs
- Typical address access time . . . 40 ns
- Typical select time . . . 20 ns
- Typical power . . . 475 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A6	10 $\overline{G}2$
2 A5	11 Q3
3 A4	12 Q2
4 A3	13 Q1
5 A0	14 Q0
6 A1	15 A9
7 A2	16 A8
8 $\overline{G}1$	17 A7
9 GND	18 V_{CC}

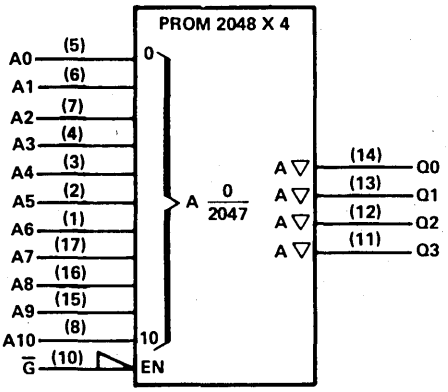
For chip carrier options and information, contact the factory.

TBP24S81 ('S454)
TBP24S81-55

PROGRAMMABLE READ-ONLY MEMORIES

- 2048 X 4
- Three-state outputs
- Typical address access time . . . 45 ns
- TBP24S81-55 maximum address access time . . . 55 ns
- Typical select time . . . 20 ns
- Typical power . . . 625 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A6	10 $\overline{G}$
2 A5	11 Q3
3 A4	12 Q2
4 A3	13 Q1
5 A0	14 Q0
6 A1	15 A9
7 A2	16 A8
8 A10	17 A7
9 GND	18 V_{CC}

For chip carrier options and information, contact the factory.

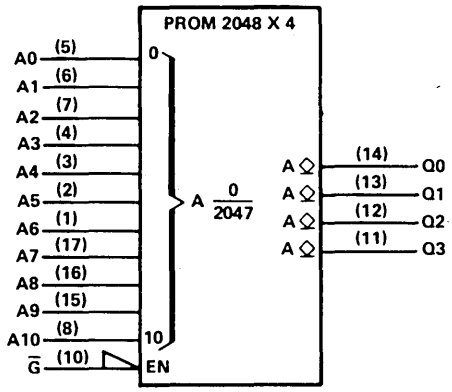
† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TBP24SA81 ('S455)
TBP24SA81-55

PROGRAMMABLE READ-ONLY MEMORIES

- 2048 X 4
- Open-collector outputs
- Typical address access time . . . 45 ns
- TBP24SA81-55 maximum address access time . . . 55 ns
- Typical select time . . . 20 ns
- Typical power . . . 625 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A6	10 $\overline{G}$
2 A5	11 Q3
3 A4	12 Q2
4 A3	13 Q1
5 A0	14 Q0
6 A1	15 A9
7 A2	16 A8
8 A10	17 A7
9 GND	18 V_{CC}

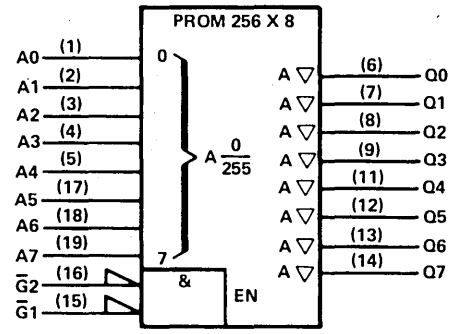
For chip carrier options and information, contact the factory.

TBP28L22

LOW-POWER PROGRAMMABLE READ-ONLY MEMORIES

- 256 X 8
- Three-state outputs
- Typical address access time . . . 45 ns
- Typical select time . . . 20 ns
- Typical power . . . 375 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A0	11 Q4
2 A1	12 Q5
3 A2	13 Q6
4 A3	14 Q7
5 A4	15 $\overline{G1}$
6 Q0	16 $\overline{G2}$
7 Q1	17 A5
8 Q2	18 A6
9 Q3	19 A7
10 GND	20 V_{CC}

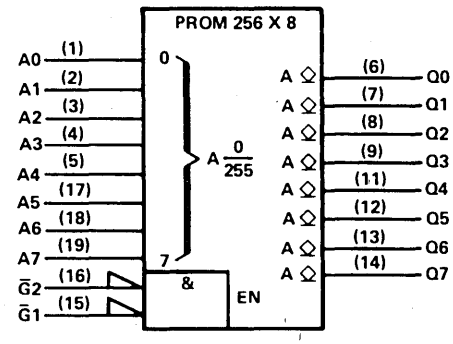
For chip carrier options and information, contact the factory.

TBP28LA22

LOW-POWER PROGRAMMABLE READ-ONLY MEMORIES

- 256 X 8
- Open-collector outputs
- Typical address access time . . . 45 ns
- Typical select time . . . 20 ns
- Typical power . . . 375 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A0	11 Q4
2 A1	12 Q5
3 A2	13 Q6
4 A3	14 Q7
5 A4	15 $\overline{G1}$
6 Q0	16 $\overline{G2}$
7 Q1	17 A5
8 Q2	18 A6
9 Q3	19 A7
10 GND	20 V_{CC}

For chip carrier options and information, contact the factory.

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

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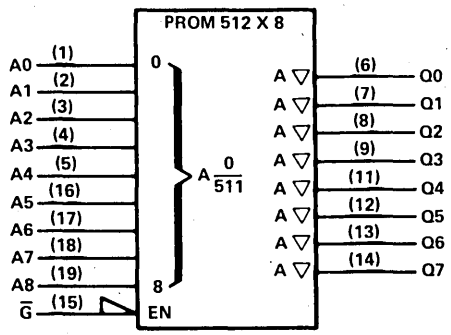
TBP28L42

LOW-POWER PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Three-state outputs
- Typical address access time . . . 55 ns
- Typical select time . . . 25 ns
- Typical power . . . 275 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A0	11 Q4
2 A1	12 Q5
3 A2	13 Q6
4 A3	14 Q7
5 A4	15 $\overline{G}$
6 Q0	16 A5
7 Q1	17 A6
8 Q2	18 A7
9 Q3	19 A8
10 GND	20 V_{CC}

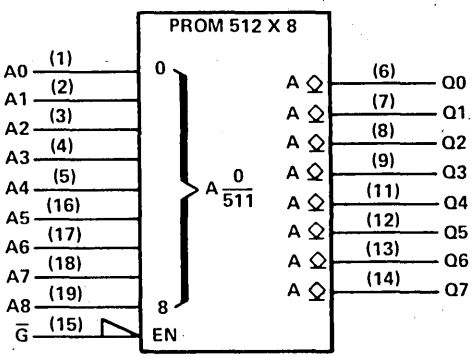
For chip carrier options and information, contact the factory.

TBP28LA42

LOW-POWER PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Open-collector outputs
- Typical address access time . . . 55 ns
- Typical select time . . . 25 ns
- Typical power . . . 275 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A0	11 Q4
2 A1	12 Q5
3 A2	13 Q6
4 A3	14 Q7
5 A4	15 $\overline{G}$
6 Q0	16 A5
7 Q1	17 A6
8 Q2	18 A7
9 Q3	19 A8
10 GND	20 V_{CC}

For chip carrier options and information, contact the factory.

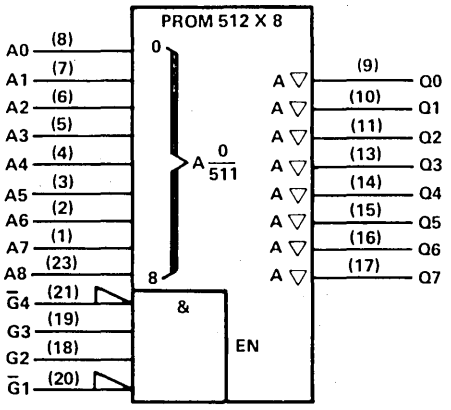
† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TBP28L45
TBP28L46

LOW-POWER PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Three-state outputs
- Typical address access time . . . 55 ns
- Typical select time . . . 25 ns
- Typical power . . . 275 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G1}$
9 Q0	21 $\overline{G4}$
10 Q1	22 nc
11 Q2	23 A8
12 GND	24 V_{CC}

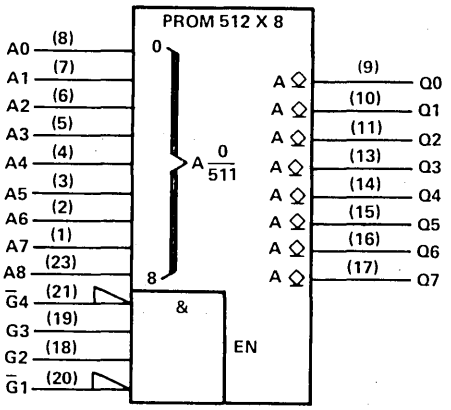
For chip carrier options and information, contact the factory.

TBP28LA45
TBP28LA46

LOW-POWER PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Open-collector outputs
- Typical address access time . . . 60 ns
- Typical select time . . . 30 ns
- Typical power . . . 250 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G1}$
9 Q0	21 $\overline{G4}$
10 Q1	22 nc
11 Q2	23 A8
12 GND	24 V_{CC}

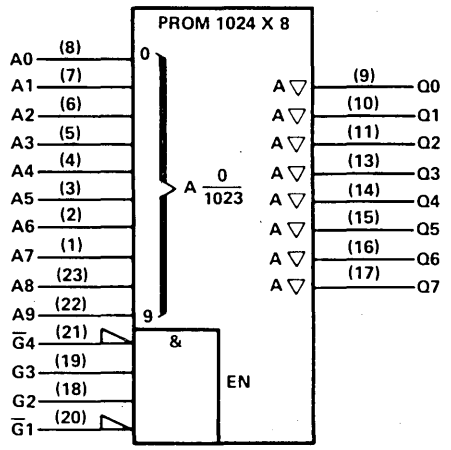
For chip carrier options and information, contact the factory.

TBP28L85A
TBP28L86A

LOW-POWER PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 8
- Three-state outputs
- Typical address access time . . . 65 ns
- Typical select time . . . 30 ns
- Typical power . . . 275 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G1}$
9 Q0	21 $\overline{G4}$
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

For chip carrier options and information, contact the factory.

† Pin numbers shown on logic symbols are for J and N packages only.
nc – no internal connection.

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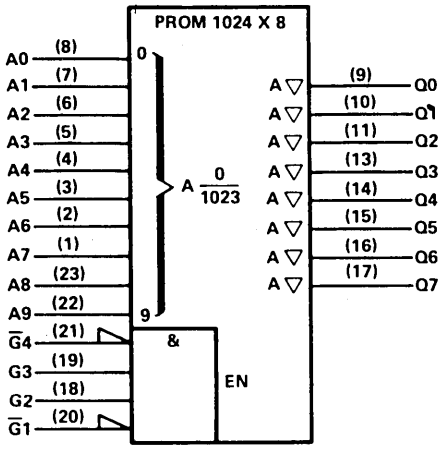
TBP28L86 ('LS478)

LOW-POWER PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 8
- Three-state outputs
- Typical address access address time . . . 80 ns
- Typical select time . . . 35 ns
- Typical power . . . 350 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G}1$
9 Q0	21 $\overline{G}4$
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

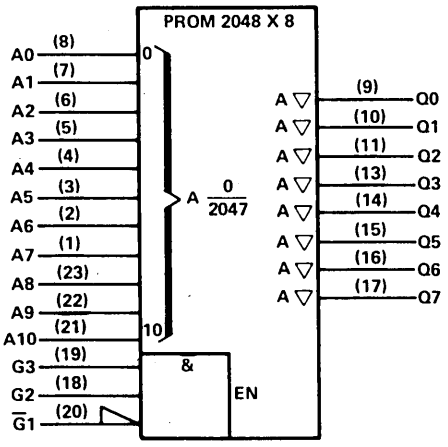
For chip carrier options and information, contact the factory.

TBP28L166A

LOW-POWER PROGRAMMABLE READ-ONLY MEMORIES

- 2048 X 8
- Three-state outputs
- Typical address access time . . . 65 ns
- Typical select time . . . 30 ns
- Typical power . . . 350 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G}1$
9 Q0	21 A10
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

For chip carrier options and information, contact the factory.

† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

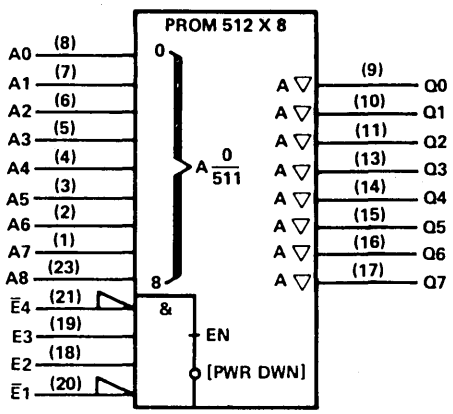
TBP28P45

POWER-DOWN PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Three-state outputs
- Multiple enables
- Typical address access time . . . 35 ns
- Typical select time . . . 55 ns
- Typical power . . . 500/60 mW

See Page 2-13

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 E2
7 A1	19 E3
8 A0	20 $\overline{E1}$
9 Q0	21 $\overline{E4}$
10 Q1	22 nc
11 Q2	23 A8
12 GND	24 V_{CC}

For chip carrier options and information, contact the factory.

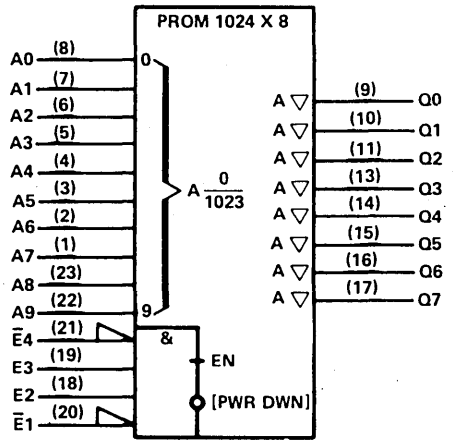
TBP28P85

POWER-DOWN PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 8
- Three-state outputs
- Typical address access time . . . 35 ns
- Typical select time . . . 55 ns
- Typical power . . . 500/60 mW

See Page 2-13

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 E2
7 A1	19 E3
8 A0	20 $\overline{E1}$
9 Q0	21 $\overline{E4}$
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

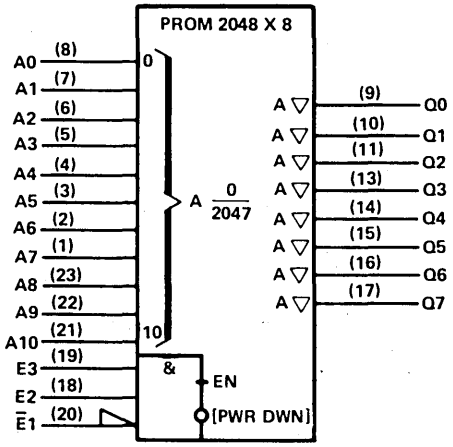
For chip carrier options and information, contact the factory.

TBP28P166

POWER-DOWN PROGRAMMABLE READ-ONLY MEMORIES

- 2048 X 8
- Three-state outputs
- Typical address access time . . . 35 ns
- Typical power . . . 650/125 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 E2
7 A1	19 E3
8 A0	20 $\overline{E1}$
9 Q0	21 A10
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

For chip carrier options and information, contact the factory.

See Page 2-13

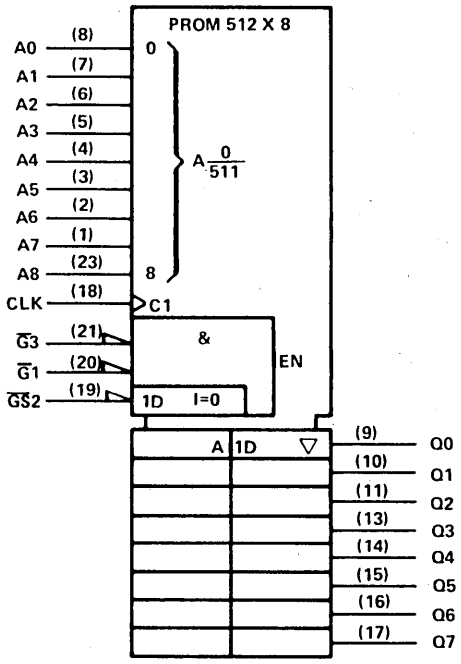
† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TBP28R45
TBP28R46

REGISTERED PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Three-state outputs
- Typical clock-to-output time . . . . 20 ns
- Typical address setup time . . . 20 ns
- Typical power . . . 550 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 CLK
7 A1	19 $\overline{GS2}$
8 A0	20 $\overline{G1}$
9 Q0	21 $\overline{G3}$
10 Q1	22 nc
11 Q2	23 A8
12 GND	24 V_{CC}

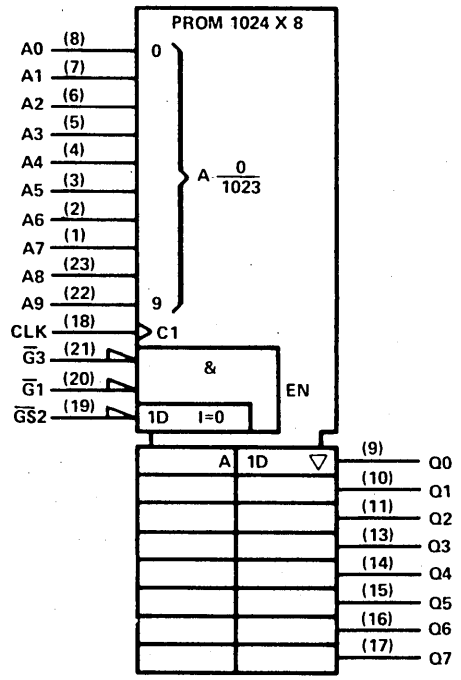
For chip carrier options and information, contact the factory.

TBP28R85A
TBP28R86A

REGISTERED PROGRAMMABLE READ-OUT MEMORIES

- 1024 X 8
- Three-state outputs
- Typical clock-to-output time . . . 20 ns
- Typical address setup time . . . 20 ns
- Typical power . . . 600 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 CLK
7 A1	19 $\overline{GS2}$
8 A0	20 $\overline{G1}$
9 Q0	21 $\overline{G3}$
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

For chip carrier options and information, contact the factory.

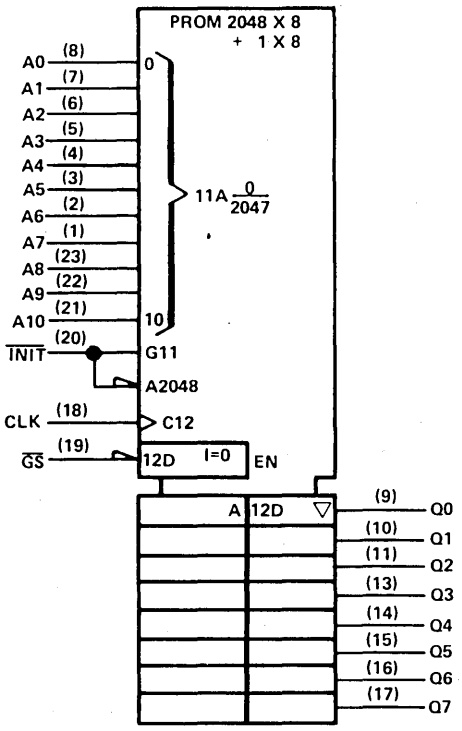
† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TBP28R165A
TBP28R166A

REGISTERED PROGRAMMABLE READ-ONLY MEMORIES WITH INITIALIZE

- Single dedicated input provides output initialize to user-programmed preset, clear, or any state
- 2048 X 8
- Three-state outputs
- Typical clock-to-output time . . . 20 ns
- Typical address setup time . . . 20 ns
- Typical power . . . 700 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 CLK
7 A1	19 $\overline{GS}$
8 A0	20 $\overline{INIT}$
9 Q0	21 A10
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

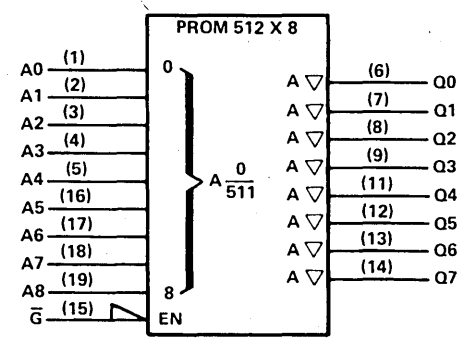
For chip carrier options and information, contact the factory.

TBP28S42

PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Three-state outputs
- Typical address access time . . . 35 ns
- Typical select time . . . 20 ns
- Typical power . . . 500 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A0	11 Q4
2 A1	12 Q5
3 A2	13 Q6
4 A3	14 Q7
5 A4	15 $\overline{G}$
6 Q0	16 A5
7 Q1	17 A6
8 Q2	18 A7
9 Q3	19 A8
10 GND	20 V_{CC}

For chip carrier options and information, contact the factory.

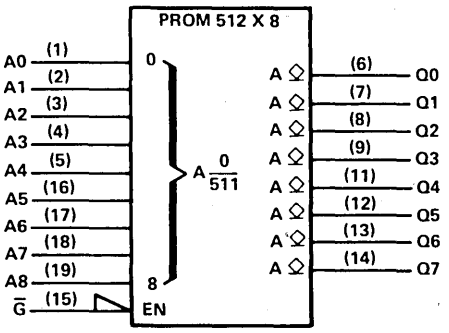
† Pin numbers shown on logic symbols are for J and N packages only.
nc – no internal connection.

TBP28SA42

PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Open-collector outputs
- Typical address access time . . . 35 ns
- Typical select time . . . 20 ns
- Typical power . . . 500 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A0	11 Q4
2 A1	12 Q5
3 A2	13 Q6
4 A3	14 Q7
5 A4	15 $\overline{G}$
6 Q0	16 A5
7 Q1	17 A6
8 Q2	18 A7
9 Q3	19 A8
10 GND	20 V_{CC}

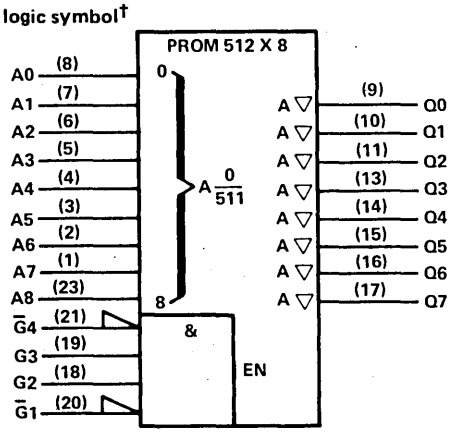
For chip carrier options and information, contact the factory.

TBP28S45
TBP28S46

PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Three-state outputs
- Typical address access time . . . 35 ns
- Typical select time . . . 20 ns
- Typical power . . . 500 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G}$1
9 Q0	21 $\overline{G}$4
10 Q1	22 nc
11 Q2	23 A8
12 GND	24 V_{CC}

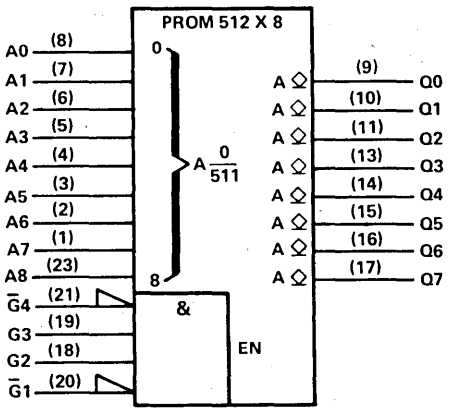
For chip carrier options and information, contact the factory.

TBP28SA45
TBP28SA45

PROGRAMMABLE READ-ONLY MEMORIES

- 512 X 8
- Open-collector outputs
- Typical address access time . . . 35 ns
- Typical select time . . . 20 ns
- Typical power . . . 500 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G}$1
9 Q0	21 $\overline{G}$4
10 Q1	22 nc
11 Q2	23 A8
12 GND	24 V_{CC}

For chip carrier options and information, contact the factory.

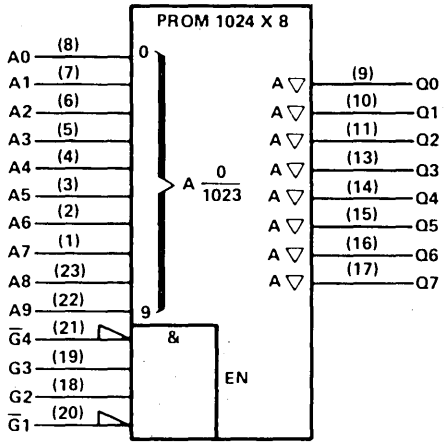
† Pin numbers shown on logic symbols are for J and N packages only.
nc — no internal connection.

TBP28S85A
TBP28S85A-50

PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 8
- Three-state outputs
- Typical address access time . . . 35 ns
- TBP28S85A-50 maximum address access time . . . 50 ns
- Typical select time . . . 20 ns
- Typical power . . . 550 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G}$1
9 Q0	21 $\overline{G}$4
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

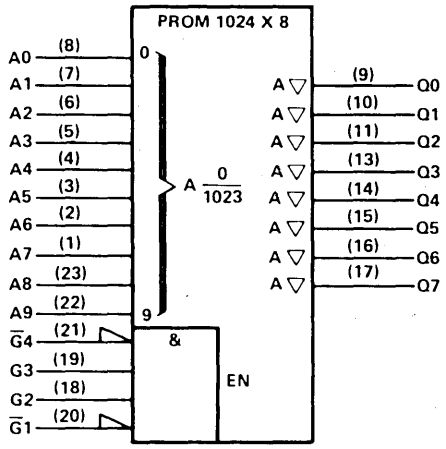
For chip carrier options and information, contact the factory.

TBP28S86 ('S478)
TBP28S86-60

PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 8
- Three-state outputs
- Typical address access time . . . 45 ns
- TBP28S86-60 maximum address access time . . . 60 ns
- Typical select time . . . 20 ns
- Typical power . . . 625 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G}$1
9 Q0	21 $\overline{G}$4
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

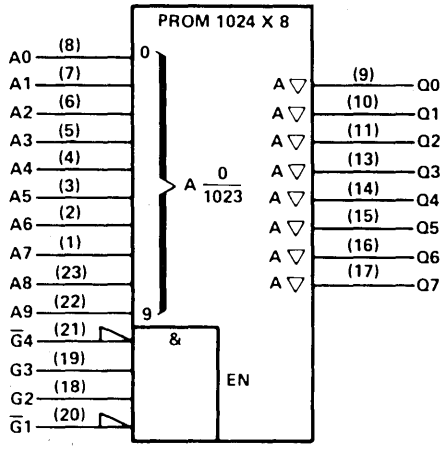
For chip carrier options and information, contact the factory.

TBP28S86A
TBP28S86A-50

PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 8
- Three-state outputs
- Typical address access time . . . 35 ns
- TBP28S86A-50 maximum address access time . . . 50 ns
- Typical select time . . . 20 ns
- Typical power . . . 550 mw

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G}$1
9 Q0	21 $\overline{G}$4
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

For chip carrier options and information, contact the factory.

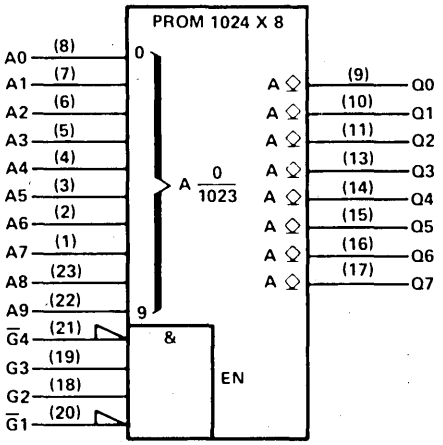
† Pin numbers shown on logic symbols are for J and N packages only.
nc -- no internal connection.

TBP28SA86 ('S479)
TBP28SA86-60

PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 8
- Open-collector outputs
- Typical address access time . . . 45 ns
- TBP28SA86-60 maximum address access time . . . 60 ns
- Typical select time . . . 20 ns
- Typical power . . . 625 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G}$1
9 Q0	21 $\overline{G}$4
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

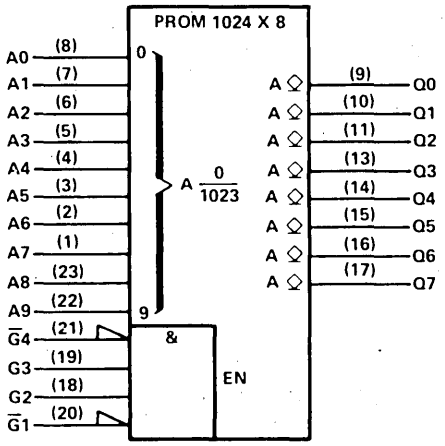
For chip carrier options and information, contact the factory.

TBP28SA86A
TBP28SA86A-50

PROGRAMMABLE READ-ONLY MEMORIES

- 1024 X 8
- Open-collector outputs
- Typical address access time . . . 35 ns
- TBP28SA86A-50 maximum address access time . . . 50 ns
- Typical select time . . . 20 ns
- Typical power . . . 550 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G}$1
9 Q0	21 $\overline{G}$4
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

For chip carrier options and information, contact the factory.

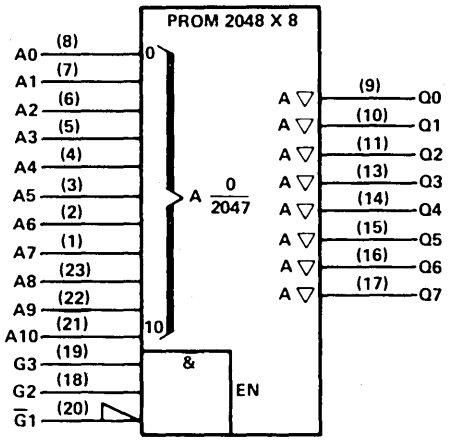
† Pin numbers shown on logic symbols are for J and N packages only.
nc – no internal connection.

TBP28S165A
TBP28S165A-35
TBP28S166
TBP28S166A
TBP28S166A-35

PROGRAMMABLE READ-ONLY MEMORIES

- 2048 X 8
- Three-state outputs
- Typical select time . . . 15 ns

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G}1$
9 Q0	21 A10
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

For chip carrier options and information, contact the factory.

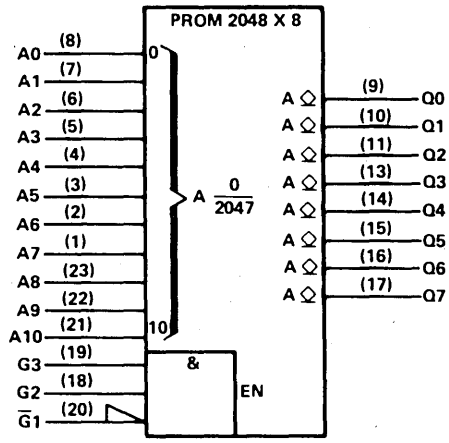
TYPE	PACKAGE ROW SPACING	TYPICAL ADDRESS ACCESS TIME	GUARANTEED MAXIMUM ACCESS TIME	TYPICAL POWER DISSIPATION
TBP28S165A	7.62 mm (0.300 in.)	25 ns		550 mW
TBP28S165A-35	7,62 mm (0.300 in.)	25 ns	35 ns	550 mW
TBP28S166	15,24 mm (0.600 in.)	35 ns		650 mW
TBP28S166A	15,24 mm (0.600 in.)	25 ns		50 mW
TBP28S166A-35	15,24 mm (0.600 in.)	25 ns	35 ns	550 mW

TBP28SA166 ('S453)

PROGRAMMABLE READ-ONLY MEMORIES

- 2048 X 8
- Open-collector outputs
- Typical address access time . . . 35 ns
- Typical select time . . . 15 ns
- Typical power . . . 650 mW

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 G2
7 A1	19 G3
8 A0	20 $\overline{G}1$
9 Q0	21 A10
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

For chip carrier options and information, contact the factory.

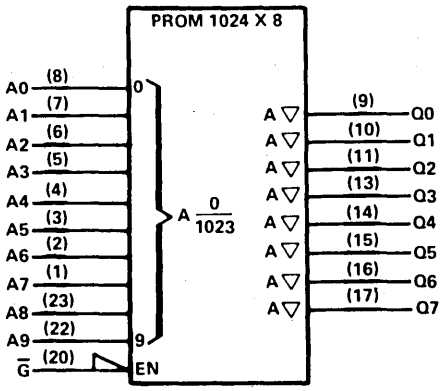
† Pin numbers shown on logic symbols are for J and N packages only.
nc – no internal connection.

TBP28S2708 ('S2708)
TBP28S2708A

PROGRAMMABLE READ-ONL MEMORIES

- 1024 X 8
- Three-state outputs
- Typical select time . . . 20 ns

logic symbol†



pin assignments

J, N PACKAGES	
1 A7	13 Q3
2 A6	14 Q4
3 A5	15 Q5
4 A4	16 Q6
5 A3	17 Q7
6 A2	18 nc
7 A1	19 nc
8 A0	20 $\overline{G}$
9 Q0	21 nc
10 Q1	22 A9
11 Q2	23 A8
12 GND	24 V_{CC}

For chip carrier options and information, contact the factory.

TYPE	TYPICAL ADDRESS ACCESS TIME	POWER POWER DISSIPATION
TBP28S2708	45 ns	625 mW
TBP28S2708A	35 ns	550 mW

† Pin numbers shown on logic symbols are for J and N packages only.
nc – no internal connection.

TIM8228	is the same as SN74S428
TIM8238	is the same as SN74S438
TIM9905	is the same as SN74LS251
TIM9906	is the same as SN74LS259
TIM9907	is the same as SN74148
TIM9908	is the same as SN74LS348

VT2332/33 PRELIMINARY

4096 x 8 STATIC READ ONLY MEMORY

FEATURES

- 4096 x 8-bit organization
- Single +5 V supply
- Access Time—300 ns (max)
- Totally static operation
- Completely TTL compatible
- VT2332 pin compatible with 2532
- VT2333 pin compatible with 2732
- 3-State Outputs for wired-OR expansion
- Two programmable Chip Selects
- 2708/2716/2532/2732 EPROMs accepted as program data inputs

DESCRIPTION

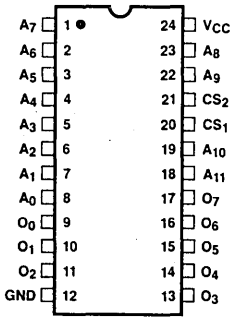
The VT2332/3 high-performance Read Only Memory is organized 4096 words by eight bits with access times of less than 300 ns. This ROM is designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. This device offers TTL input and output levels with a minimum of 0.4 V noise immunity in conjunction with a +5 V power supply.

The VT2332/3 operates totally asynchronously. No clock input is required. The two programmable Chip Selects allow up to four 32K ROMs to be wired-OR without external decoding. Both devices offer 3-state output buffers for memory expansion.

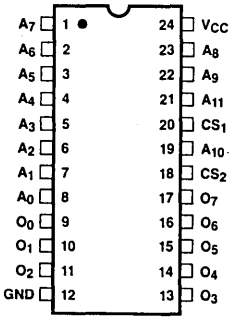
Designed to replace either the 2732 or 2532 32K EPROMs, the VT2332/3 can eliminate the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs.

PIN CONFIGURATIONS

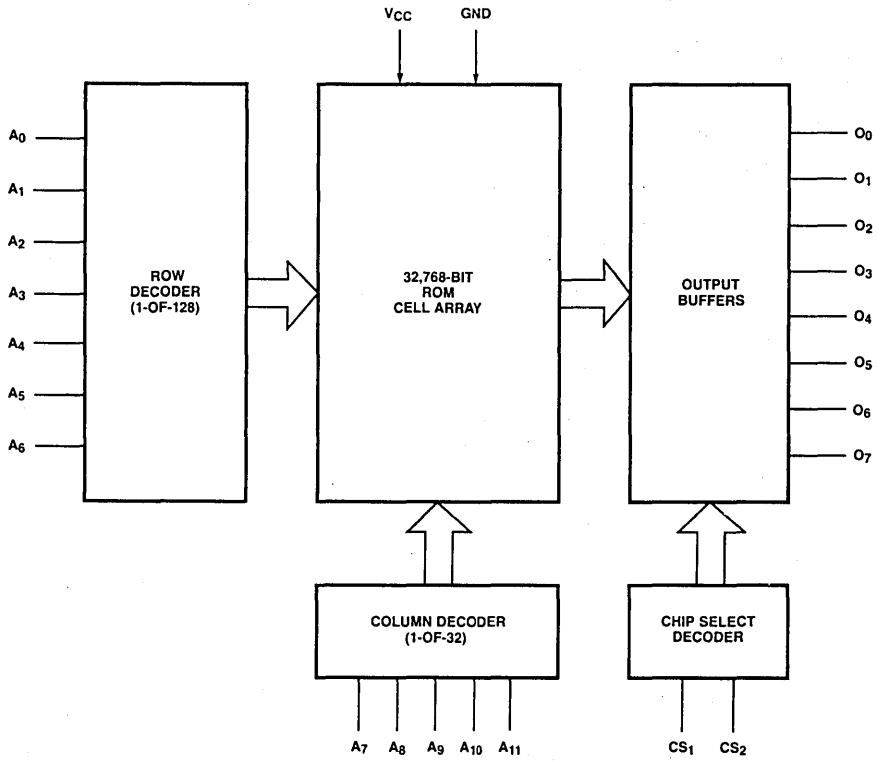
VT2332



VT2333



BLOCK DIAGRAM



VLSI Technology

MEMORY

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	−10 to +80°C
Storage Temperature	−65 to +150°C
Supply Voltage to Ground Potential	−0.5 to +7.0 V
Applied Output Voltage	−0.5 to +7.0 V
Applied Input Voltage	−0.5 to +7.0 V
Power Dissipation	1.0 W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated on the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: T_A = 0 to +70°C, V_{CC} = 5 V ±10% (unless otherwise specified)

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{OH}	Output HIGH Voltage	2.4	V_{CC}	V	V_{CC} = 4.5 V, I_{OH} = −200 µA
V_{OL}	Output LOW Voltage		0.4	V	V_{CC} = 4.5 V, I_{OL} = 2.1 mA
V_{IH}	Input HIGH Voltage	2.0	V_{CC}	V	
V_{IL}	Input LOW Voltage	−0.5	0.8	V	See Note 1
I_{LI}	Input Load Current		10	µA	V_{CC} = 5.5 V, 0 V ≤ V_{IN} ≤ 5.5 V
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = +0.4 V to V_{CC}, Note 2
I_{CC}	Power Supply Current		100	mA	V_{CC} = 5.5 V, V_{IN} = V_{CC}, Note 3

CAPACITANCE: t_A = 25°C, f = 1.0 MHz, Note 4

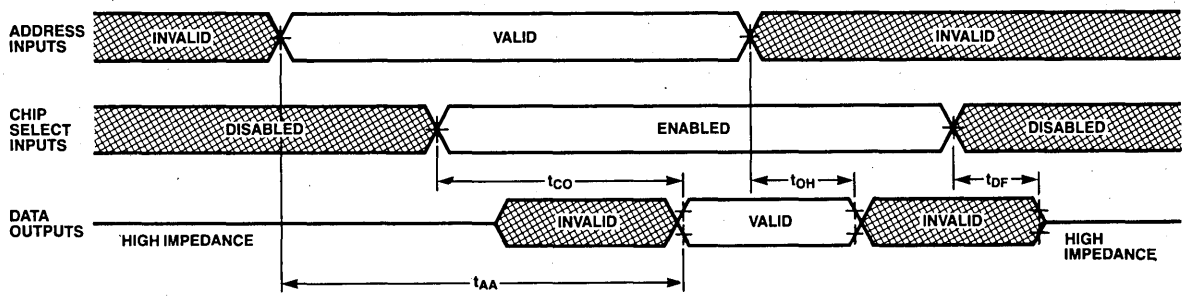
Symbol	Parameter	Min	Max	Unit	Test Conditions
C_I	Input Capacitance		7	pF	All pins except pin under test tied to AC ground
C_O	Output Capacitance		10	pF	

AC CHARACTERISTICS: T_A = 0 to + 70°C, V_{CC} = 5 V ±10% (unless otherwise specified)

Symbol	Parameter	VT2332/33		VT2332A/33A		Unit	Test Conditions
		Min	Max	Min	Max		
t_{AA}	Address Access Time		450		300	ns	Output load: 1 TTL load and 100 pF Input transition time: 20 ns Timing reference levels: Input: 1.5 V Output: 0.8 V and 2.0 V
t_{CO}	Chip Select Delay		150		100	ns	
t_{DF}	Chip Deselect Delay		150		100	ns	
t_{OH}	Output Hold After Address Change	20		20		ns	

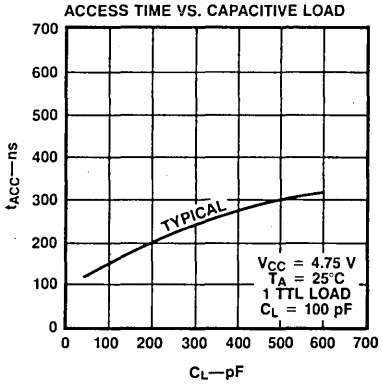
Notes:
1. Input levels that swing more negative than −0.5 V will be clamped and may cause damage to the device.
2. Measured with device deselected.
3. Measured with device selected and outputs unloaded.
4. This parameter is periodically sampled and is not 100% tested.

TIMING DIAGRAM

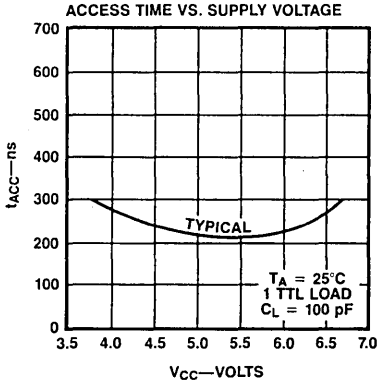


TYPICAL CHARACTERISTICS

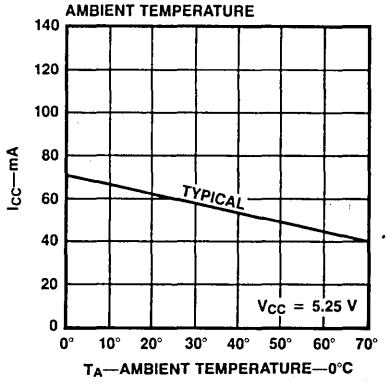
ACCESS TIME VS. CAPACITIVE LOAD



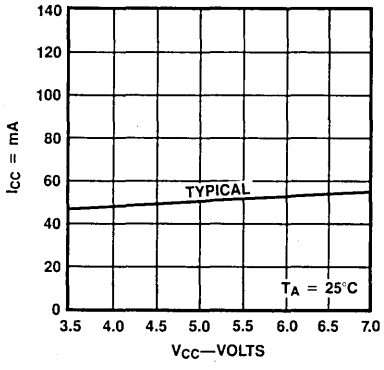
ACCESS TIME VS. SUPPLY VOLTAGE



SUPPLY CURRENT VS. AMBIENT TEMPERATURE

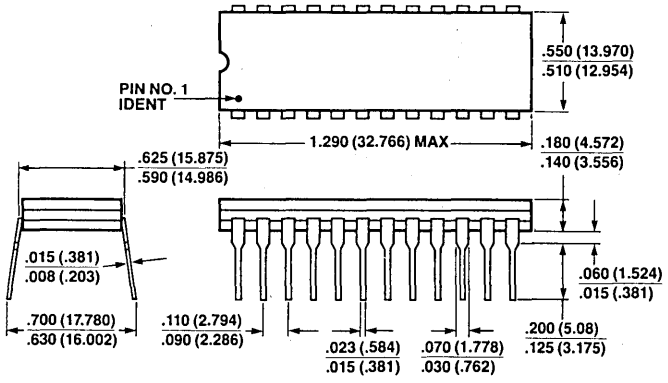


SUPPLY CURRENT VS. SUPPLY VOLTAGE

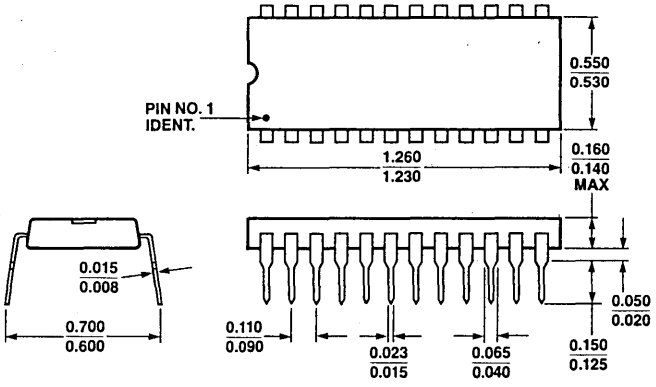


PACKAGE DIAGRAMS

24-LEAD CERDIP DUAL IN-LINE



24-LEAD PLASTIC DUAL IN-LINE



VT2364 PRELIMINARY

8192 x 8 STATIC READ ONLY MEMORY

FEATURES

- 2732 EPROM pin compatible
- 8192 x 8-bit organization
- Single +5 V supply
- Access time—300 ns max
- Totally static operation
- Completely TTL compatible
- Operating Power: 100 mA (max)
- 24-Pin JEDEC approved pin-out
- Programmable Chip Select
- 3-state outputs for wired-OR expansion
- EPROMS accepted as program data input

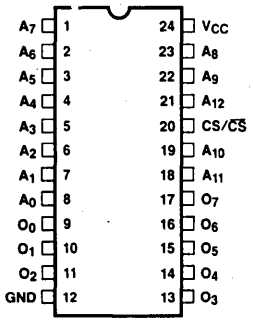
DESCRIPTION

The VT2364 high-performance Read Only Memory is organized as 8,192 words by eight bits with an access time of 300 ns. The ROM is designed to be compatible with all microprocessors and similar applications where high-performance large-bit storage and simple interfacing are important design considerations. It conforms to the JEDEC approved pinouts for 24-pin 64K ROMs.

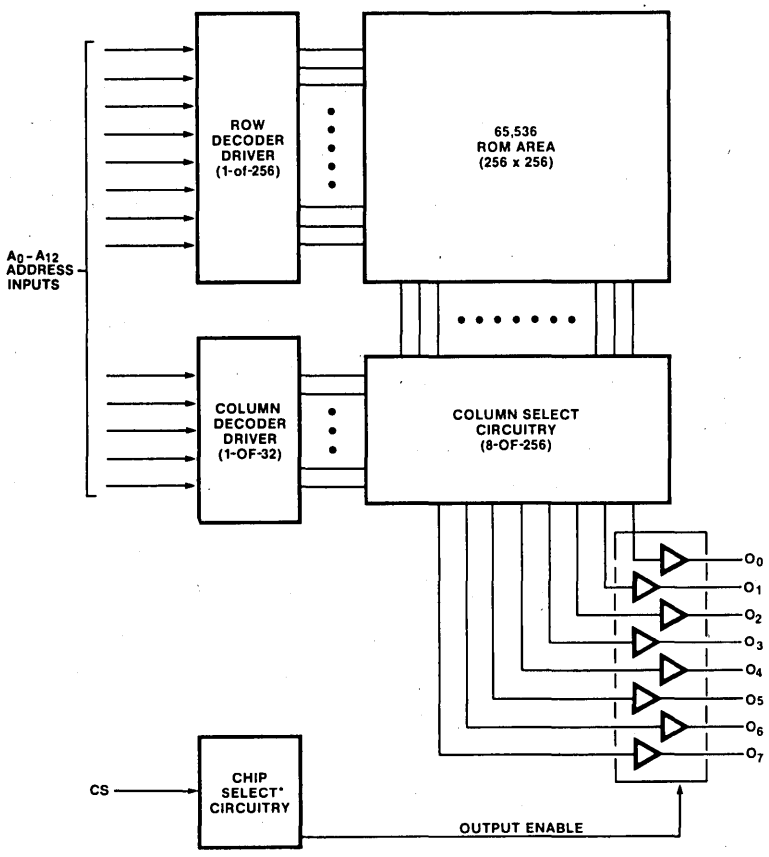
The VT2364 offers very simple operation with no power down. The programmable Chip Select allows two 64K ROMs to be Wired-OR without external decoding. It is pin compatible with the 2732 EPROM thus eliminating the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMS.

PIN CONFIGURATIONS

VT2364



BLOCK DIAGRAM



*CHIP SELECT (CS) IS PROGRAMMABLE ACTIVE LOW OR ACTIVE HIGH.

VLSI Technology

MEMORY

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	−10 to +80°C
Storage Temperature	−65 to +150°C
Supply Voltage to Ground Potential	−0.5 to +7.0 V
Applied Output Voltage	−0.5 to +7.0 V
Applied Input Voltage	−0.5 to +7.0 V
Power Dissipation	1.0 W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated on the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: T_A = 0 to +70°C, V_{CC} = +5 V ± 10%

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{OH}	Output HIGH Voltage	2.4		V_{CC}	V	I_{OH} = −1.0 mA
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 3.2 mA
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
V_{IL}	Input LOW Voltage	−0.5		0.8	V	
I_{LI}	Input Leakage Current			10	µA	V_{IN} = 0 V to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = 0 V to V_{CC}
I_{CC}	Operating Supply Current			100	mA	Note 1
I_{OS}	Output Short Circuit Current			70	mA	Note 2

CAPACITANCE: T_A = 25°C, f = 1.0 MHz, Note 3

Symbol	Parameter	Min	Max	Unit	Conditions
C_I	Input Capacitance		5	pF	V_{IN} = 0 V
C_O	Output Capacitance		5	pF	V_{OUT} = 0 V

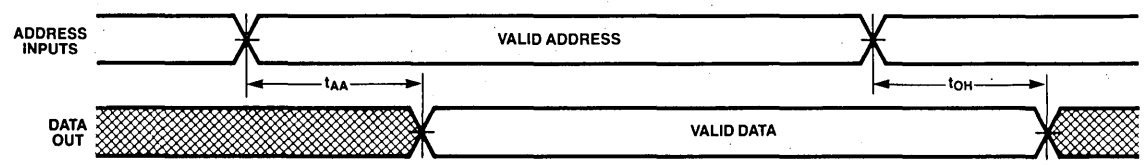
AC CHARACTERISTICS: T_A = 0 to + 70°C, V_{CC} = 5 V ±10% (unless otherwise specified)

Symbol	Parameter	VT2364		VT2364A		Unit	Test Conditions
		Min	Max	Min	Max		
t_{AA}	Address Access Time		450		300	ns	Output load: 1 TTL load and 100 pF Input transition time: 20 ns Timing reference levels: Input: 1.5 V Output: 0.8 V and 2.0 V
t_{CO}	Chip Select Delay		150		100	ns	
t_{DF}	Chip Deselect Delay		150		100	ns	
t_{OH}	Output Hold After Address Change	20		20		ns	

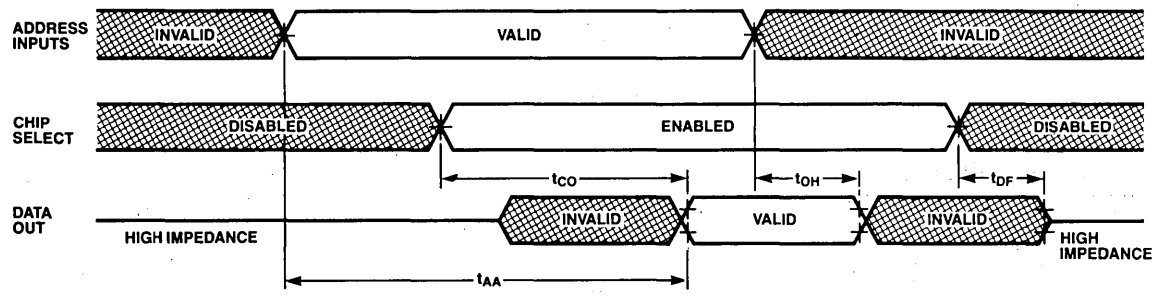
Notes:
1. Measured with device selected and outputs unloaded.
2. For a duration not to exceed 30 seconds.
3. This parameter is periodically sampled and is not 100% tested.

TIMING DIAGRAMS

PROPAGATION DELAY FROM ADDRESS (CS/$\overline{CS}$ = ACTIVE)



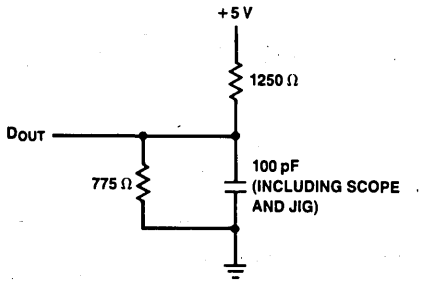
PROPAGATION DELAY FROM CHIP SELECT (ADDRESS VALID)



AC TEST CONDITIONS

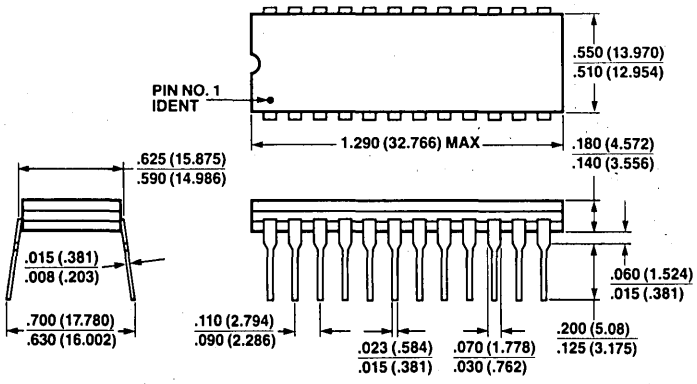
Input Pulse Levels	0.8 to 2.2 V
Input Rise and Fall Times	10 ns
Input Timing Level	1.5 V
Output Timing Level	0.8 and 2.0 V
Output Load	See Figure 1

FIGURE 1

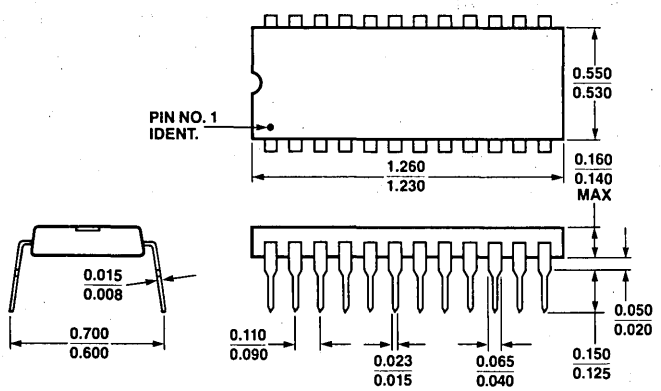


PACKAGE DIAGRAMS

24-LEAD CERDIP DUAL IN-LINE



24-LEAD PLASTIC DUAL IN-LINE



VT 2365/66 PRELIMINARY

8,192 x 8 STATIC READ ONLY MEMORY

FEATURES

- 2764/2564 EPROM pin compatible
- 8,192 x 8-bit organization
- Single +5 V supply
- Access time — 200 ns (max)
- Totally static operation
- Completely TTL compatible
- Power
  - Operating: 100 mA (max)
  - Standby: 15 mA (max)
- 28-Pin JEDEC approved pinout
- Automatic power down ($\overline{CE}$)
- Output Enable function ($\overline{OE}$)
- Programmable Chip Select
- 3-state outputs for wired-OR expansion
- EPROMs accepted as program data input

DESCRIPTION

The VT2365/66 high-performance Read Only Memory is organized 8,192 words by eight bits with an access time of 200 ns. The ROM is designed to be compatible with all microprocessors and similar applications where high-performance large-bit storage and simple interfacing are important design considerations. It conforms to the JEDEC approved pinout for 28-pin 64K ROMs.

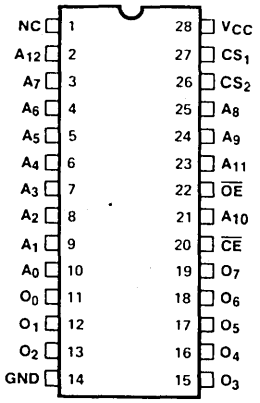
The VT2365/66 offers an automatic power down feature with power down controlled by the Chip Enable. ($\overline{CE}$) input. When $\overline{CE}$ goes HIGH, the device will automatically power down and remain in a low-power standby mode as long as $\overline{CE}$ remains HIGH.

This unique feature provides system level power savings of as much as 90%. The programmable Chip Selects allow up to four 64K ROMs to be wired-OR without external decoding. An additional feature of the VT2365 is the Output Enable ($\overline{OE}$) function which eliminates bus contention in multiple-bus microprocessor systems.

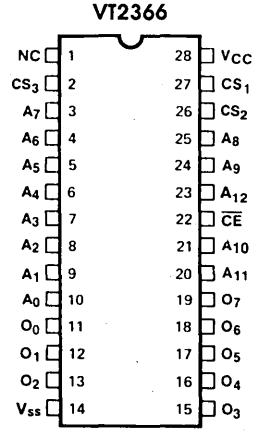
The VT2365 is pin compatible with the 2764 EPROM and the VT2366 is pin compatible with the 2564 EPROM, thus eliminating the need to redesign printed circuit boards for volume mask programmable ROMs after prototyping with EPROMs.

PIN CONFIGURATIONS

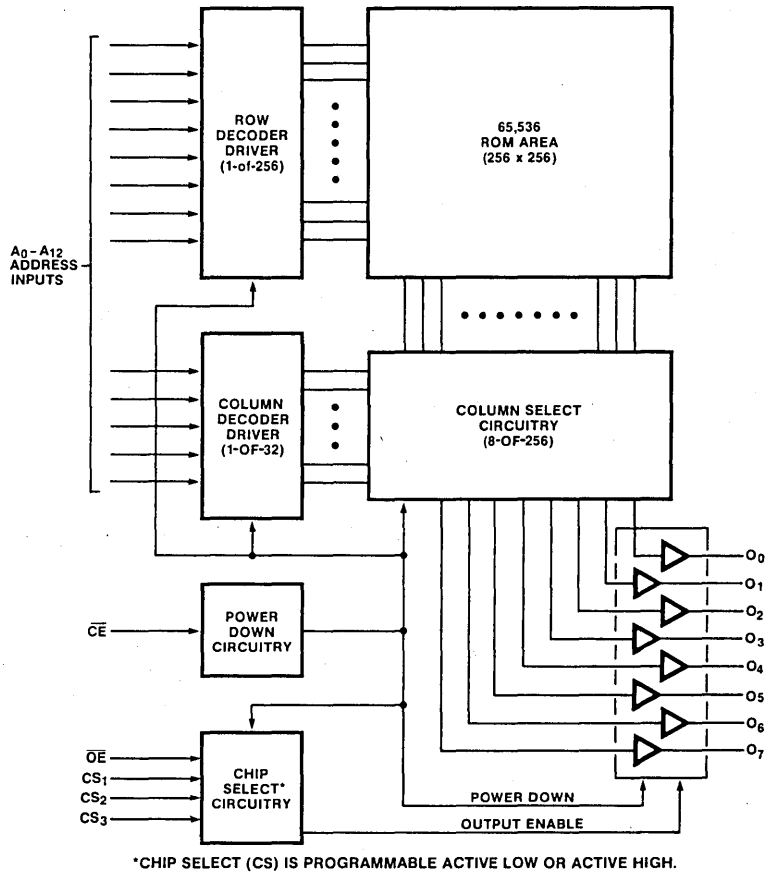
VT2365



VT2366



BLOCK DIAGRAM



*CHIP SELECT (CS) IS PROGRAMMABLE ACTIVE LOW OR ACTIVE HIGH.

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	−10 to +80°C
Storage Temperature	−65 to +150°C
Supply Voltage to Ground Potential	−0.5 to +7.0 V
Applied Output Voltage	−0.5 to +7.0 V
Applied Input Voltage	−0.5 to +7.0 V
Power Dissipation	1.0 W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated on the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: T_A = 0 to +70°C, V_{CC} = +5 V ± 10%

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{OH}	Output HIGH Voltage	2.4		V_{CC}	V	I_{OH} = −1.0 mA
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 3.2 mA
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
V_{IL}	Input LOW Voltage	−0.5		0.8	V	
I_{LI}	Input Leakage Current			10	µA	V_{IN} = 0 V to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = 0 V to V_{CC}
I_{CC}	Operating Supply Current			100	mA	Note 1
I_{SB}	Standby Supply Current			15	mA	
I_{OS}	Output Short Circuit Current			70	mA	Note 2

CAPACITANCE: T_A = 25°C, f = 1.0 MHz, Note 5

Symbol	Parameter	Min	Max	Unit	Conditions
C_I	Input Capacitance		5	pF	V_{IN} = 0 V
C_O	Output Capacitance		5	pF	V_{OUT} = 0 V

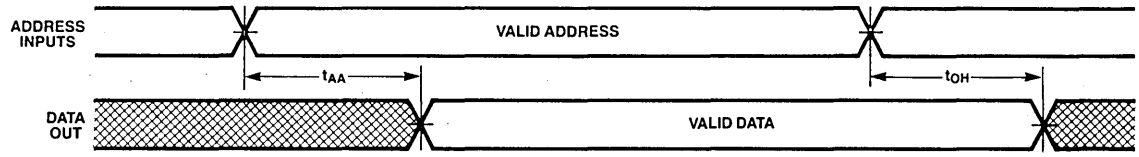
AC CHARACTERISTICS: T_A = 0 to +70°C, V_{CC} = +5 V ± 10%

Symbol	Parameter	VT2365B VT2366B		VT2365A VT2366A		VT2365 VT2366		Unit	Condition
		Min	Max	Min	Max	Min	Max		
t_{CYC}	Cycle Time	200		300		450		ns	
t_{AA}	Address Access Time		200		300		450	ns	
t_{OH}	Output Hold After Address Change	10		10		10		ns	
t_{ACE}	Chip Enable Access Time		200		300		450	ns	
t_{ACS}	Chip Select Access Time		85		100		150	ns	
t_{AOE}	Output Enable Access Time		85		100		150	ns	
t_{LZ}	Output LOW Z Delay	10		10		10		ns	Note 3
t_{HZ}	Output HIGH Z Delay		85		100		150	ns	Note 4
t_{PU}	Power-Up Time	0		0		0		ns	
t_{PD}	Power-Down Time		85		100		150	ns	

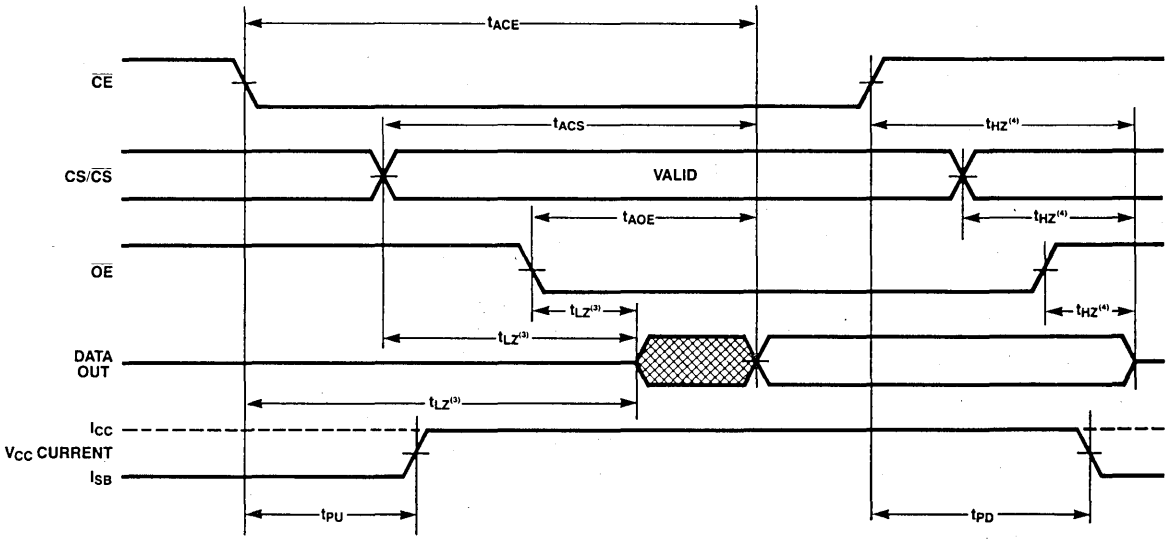
Notes:
1. Measured with device selected and outputs unloaded.
2. For a duration not to exceed 30 seconds.
3. Output LOW impedance delay (t_{LZ}) is measured from $\overline{CE}$ and $\overline{OE}$ going LOW and CS going active, whichever occurs last.
4. Output HIGH impedance delay (t_{HZ}) is measured from either $\overline{CE}$ or $\overline{OE}$ going HIGH or CS going inactive, whichever occurs first.
5. This parameter is periodically sampled and is not 100% tested.

TIMING DIAGRAMS

PROPAGATION DELAY FROM ADDRESS ($\overline{CE}$ = $\overline{OE}$ = LOW, CS/$\overline{CS}$ = ACTIVE)

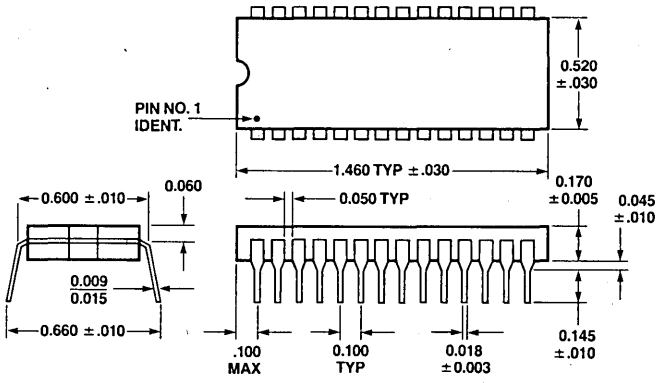


PROPAGATION DELAY FROM CHIP ENABLE, CHIP SELECT OR OUTPUT ENABLE (ADDRESS VALID)

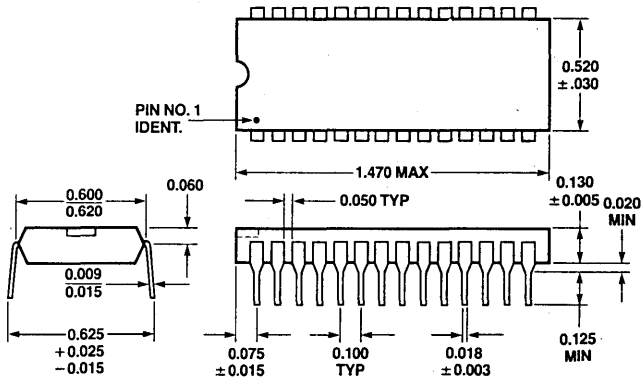


PACKAGE DIAGRAMS

28-LEAD CERDIP DUAL IN-LINE



28-LEAD PLASTIC DUAL IN-LINE



VT23128/29 PRELIMINARY

16,384 x 8 STATIC READ ONLY MEMORY

FEATURES

- 16,384 x 8-bit organization
- Single +5 V supply
- Access time 250 ns max
- Totally static operation
- Completely TTL compatible
- Operating power 100 mA max
- Standby power 20 mA max
- Automatic power down ($\overline{CE}$)
- Output enable function ($\overline{OE}$)
- Programmable Chip Select
- 3-state outputs for wired-OR expansion
- 28-pin JEDEC approved pinouts
- VT23128 pin compatible with the 2764 EPROM
- VT23129 pin compatible with the 2564 EPROM
- EPROMs accepted as program data input

DESCRIPTION

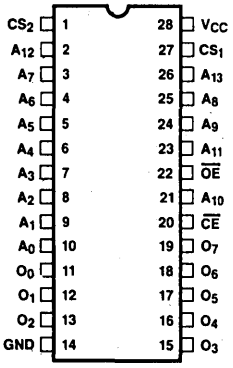
The VT23128/29 high-performance Read Only Memory is organized 16,384 words by eight bits with an access time of 250 ns. It is designed to be compatible with all microprocessors and similar applications where high-performance large-bit storage and simple interfacing are important design considerations.

The VT23128/29 offers automatic power down with power down controlled by the Chip Enable ($\overline{CE}$) input. When $\overline{CE}$ goes HIGH, the device will automatically power down and remain in a low-power standby mode as long as $\overline{CE}$ remains HIGH. This unique feature provides system level power savings of as much as 90%. The VT23128 also has an Output Enable ($\overline{OE}$) function to eliminate bus contention in multiple-bus microprocessor systems. The programmable Chip Select allows up to eight 128K ROMs to be wired-OR without external decoding.

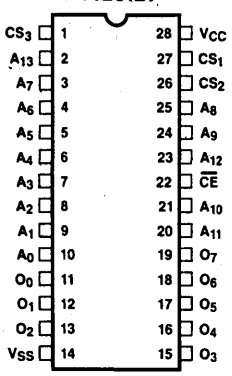
The VT23128 is pin compatible with the 2764 EPROM and the VT23129 is pin compatible with the 2564 EPROM, thus eliminating the need to redesign printed circuit boards for volume mask programmable ROMs after prototyping with EPROMS.

PIN CONFIGURATION

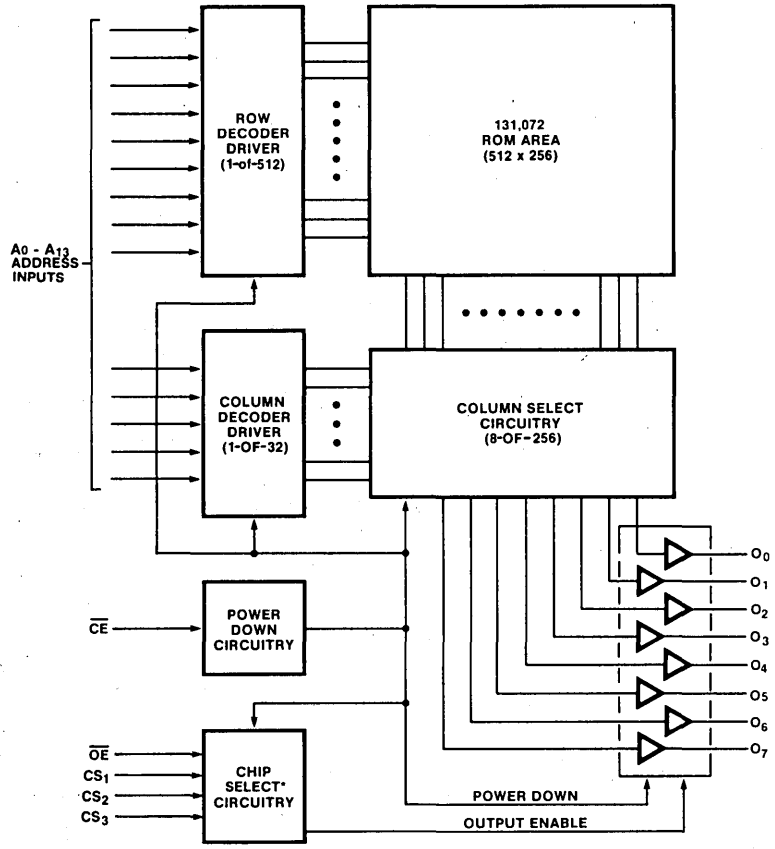
VT23128



VT23129



BLOCK DIAGRAM



*CHIP SELECT (CS) IS PROGRAMMABLE ACTIVE LOW, ACTIVE HIGH, OR DON'T CARE

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	−10 to +80°C
Storage Temperature	−65 to +150°C
Supply Voltage to Ground Potential	−0.5 to +7.0 V
Applied Output Voltage	−0.5 to +7.0 V
Applied Input Voltage	−0.5 to +7.0 V
Power Dissipation	1.0 W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated on the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: T_A = 0 to +70°C, V_{CC} = +5 V ±10%

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{OH}	Output HIGH Voltage	2.4		V_{CC}	V	I_{OH} = −1.0 mA
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 3.2 mA
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
V_{IL}	Input LOW Voltage	−0.5		0.8	V	
I_{LI}	Input Leakage Current			10	µA	V_{IN} = 0 V to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = 0 V to V_{CC}
I_{CC}	Operating Supply Current			100	mA	Note 1
I_{SB}	Standby Supply Current			20	mA	$\overline{CE}$ = V_{IH}
I_{OS}	Output Short Circuit Current			70	mA	Note 2

CAPACITANCE: T_A = 25°C, f = 1.0 MHz, Note 5

Symbol	Parameter	Min	Max	Unit	Conditions
C_I	Input Capacitance		5	pF	V_{IN} = 0 V
C_O	Output Capacitance		5	pF	V_{OUT} = 0 V

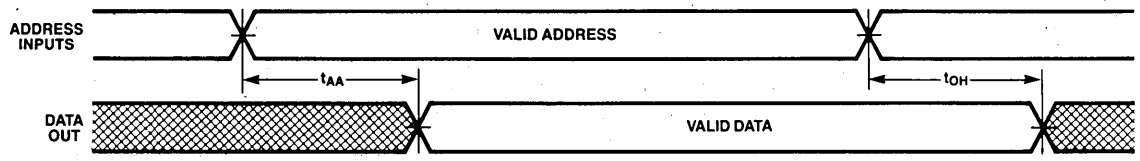
AC CHARACTERISTICS: T_A = 0 to +70°C, V_{CC} = +5 V ±10%

		VT23128A VT23129A		VT23128 VT23129		VT23128B VT23129B			
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Unit	Condition
T_{CYC}	Cycle Time	200		250		450		ns	
t_{AA}	Address Access Time		200		250		450	ns	
t_{OH}	Output Hold After Address Change	10		10		10		ns	
t_{ACE}	Chip Enable Access Time		200		250		450	ns	
t_{ACS}	Chip Select Access Time		85		100		150	ns	
T_{AOE}	Output Enable Access Time		85		100		150	ns	
T_{LZ}	Output LOW Z Delay	10		10		10		ns	Note 3
T_{HZ}	Output HIGH Z Delay		85		100		150	ns	Note 4
t_{PU}	Power-Up Time	0		0		0		ns	
t_{PD}	Power-Down Time		85		100		150	ns	

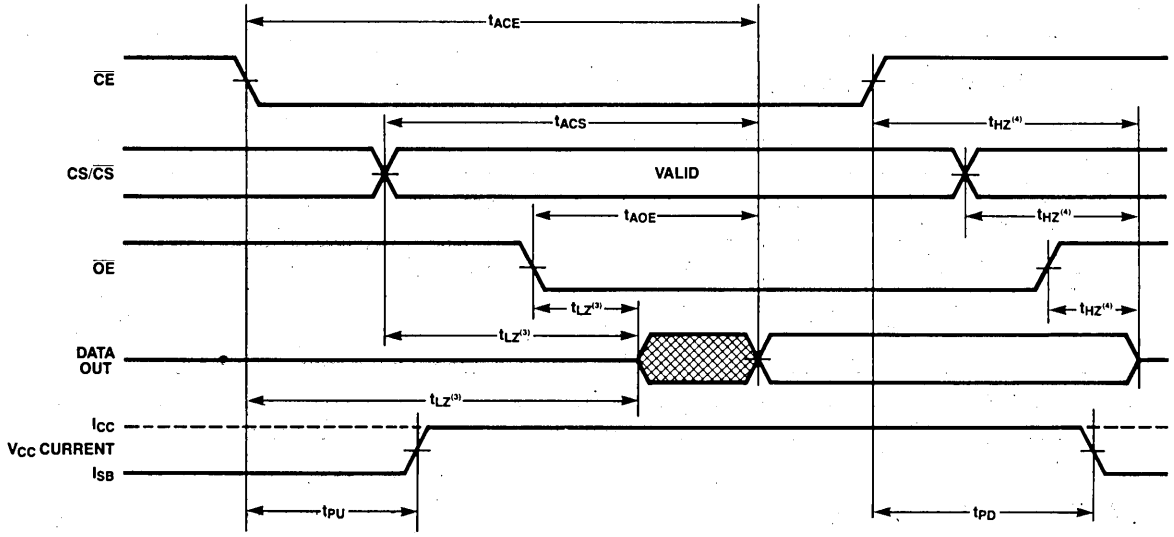
Notes:
1. Measured with device selected and outputs unloaded.
2. For a duration not to exceed 30 seconds.
3. Output LOW impedance delay (T_{LZ}) is measured from $\overline{CE}$ and $\overline{OE}$ going LOW and CS going active, whichever occurs last.
4. Output HIGH impedance delay (t_{HZ}) is measured from either $\overline{CE}$ or $\overline{OE}$ going HIGH or CS going inactive, whichever occurs first.
5. This parameter is periodically sampled and is not 100% tested.

TIMING DIAGRAMS

PROPAGATION DELAY FROM ADDRESS ($\overline{CE}$ = $\overline{OE}$ = LOW, CS/$\overline{CS}$ = ACTIVE)

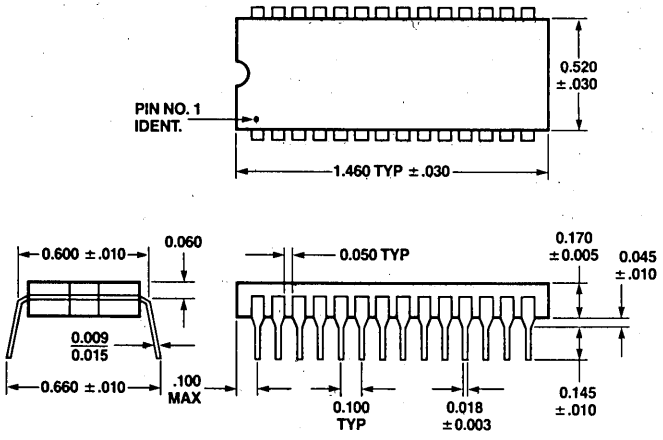


PROPAGATION DELAY FROM CHIP ENABLE, CHIP SELECT OR OUTPUT ENABLE (ADDRESS VALID)

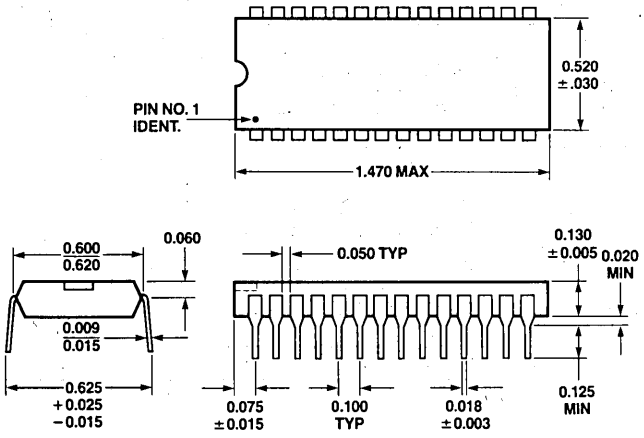


PACKAGE DIAGRAMS

28-LEAD CERDIP DUAL IN-LINE



28-LEAD PLASTIC DUAL IN-LINE



VT23256/57 PRELIMINARY

32,768 x 8 STATIC READ ONLY MEMORY

FEATURES

- 32,768 x 8-bit organization
- Single +5 V supply
- Access time 250 ns max
- Totally static operation
- Completely TTL compatible
- Operating power 100 mA max
- Standby power 15 mA max
- Automatic power down ($\overline{CE}$)
- Programmable Chip Select
- 3-state outputs for wired-OR expansion
- 28-pin JEDEC approved pinouts
- VT23256 pin compatible with the 2764 EPROM
- VT23257 pin compatible with the 2564 EPROM
- EPROMs accepted as program data input

DESCRIPTION

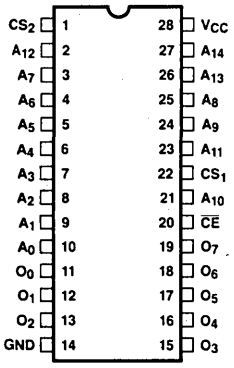
The VT23256/57 high-performance Read Only Memory is organized 32,768 words by eight bits with an access time of 250 ns. It is designed to be compatible with all microprocessors and similar applications where high-performance large-bit storage and simple interfacing are important design considerations.

The VT23256/57 offers automatic power down with power down controlled by the Chip Enable ($\overline{CE}$) input. When $\overline{CE}$ goes HIGH, the device will automatically power down and remain in a low power standby mode as long as $\overline{CE}$ remains HIGH. This unique feature provides system level power savings of as much as 90%. The programmable Chip Select allows up to four 256K ROMs to be wired-OR without external decoding.

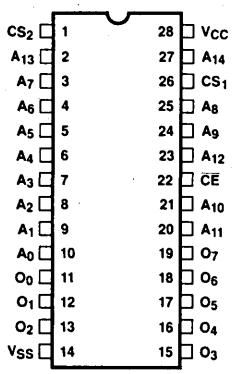
The VT23256 is pin compatible with the 2764 EPROM and the VT23257 is pin compatible with the 2564 EPROM, thus eliminating the need to redesign printed circuit boards for volume mask programmable ROMs after prototyping with EPROMS.

PIN CONFIGURATION

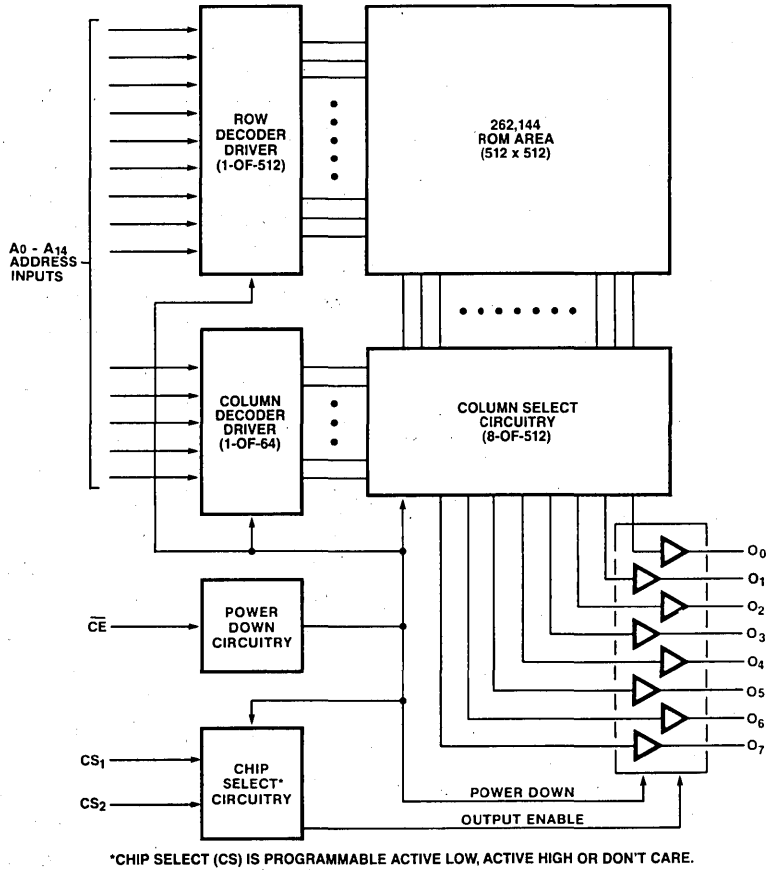
VT23256



VT23257



BLOCK DIAGRAM



*CHIP SELECT (CS) IS PROGRAMMABLE ACTIVE LOW, ACTIVE HIGH OR DON'T CARE.

VLSI Technology, Inc. • 1101 McKay Drive • San Jose, CA 95131 • 408-942-1810

WD1510-00,-01,-02 LIFO/FIFO Buffer Register

FEATURES

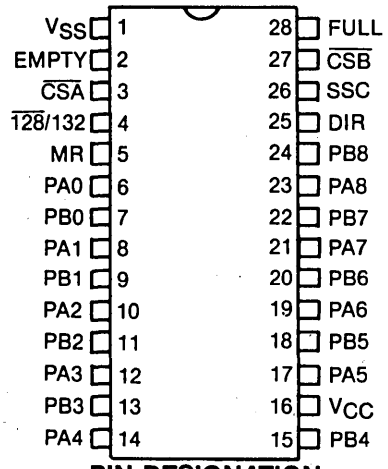
- WORD LENGTH SELECTABLE: 128 OR 132
- 9 BIT WORD WIDTH
- DC TO 650 KHZ (−00), 1 MHz (−01), 1.2 MHz (−02)
- EMPTY AND FULL FLAGS
- THREE-STATE DATA LINES
- 5-VOLT ONLY
- NO EXTERNAL CLOCKS REQUIRED
- TTL COMPATIBLE ON ALL INPUTS AND OUTPUTS
- 28 PIN PLASTIC OR CERAMIC DIP
- CASCADABLE WITH WD1511 SUPPORT CHIP
- FULLY ASYNCHRONOUS DUAL PORT OPERATION

GENERAL DESCRIPTION

The WD1510 is an MOS/LSI Memory Buffer which is organized as a 9-bit by 128 or 132 word stack. The chip has 2 bidirectional data ports and may be read from or written into either port. Thus, the chip can function as a LIFO from either port or it can function as a FIFO, with data flow from either port A to port B or vice versa. The DIRECTION input pin is used to specify the data flow direction. The WD1510 is fabricated in 5-volt only N-channel technology.

APPLICATIONS

POINT OF SALE TERMINALS
COMPUTER-TO-PERIPHERAL BUFFER
CRT BUFFER MEMORY
LINE PRINTER BUFFER
INTERRUPT STACK (LIFO MODE)



PIN DESIGNATION

PIN DEFINITIONS

PIN NUMBER	NAME	SYMBOL	FUNCTION
1	VSS	VSS	Ground
2	EMPTY	EMPTY	Indicates when there is no data in the buffer
3	CHIP SELECT PORT A	$\overline{CSA}$	Used to select Port A for either a Read or Write operation
4	128 OR 132	$\overline{128}$/132	Used to set word length. When low word length = 128, when high word length = 132
5	MASTER RESET	MR	When pulsed will clear the buffer and set the EMPTY pin
6,8,10,12,14, 17,19,21,23	PORT A DATA LINES	PA0-PA8	Bidirectional DATA Port for reading or writing
7,9,11,13,15 18,20,22,24	PORT B DATA LINES	PB0-PB8	Bidirectional DATA Port for reading or writing
16	VCC	VCC	+5 volts ± .25V
25	DIRECTION	DIR	When low DIR specifies that Port A may be read from and Port B may be written into. When high DIR specifies that Port A may be written into and Port B may be read from.
26	SYSTEM SENTINEL™ CHECKOUT	SSC	No connection (For future use)
27	CHIP SELECT PORT B	$\overline{CSB}$	Used to select Port B for either a Read or Write Operation
28	FULL	FULL	Indicates that all 132 or 128 words of memory are loaded with data

PRELIMINARY

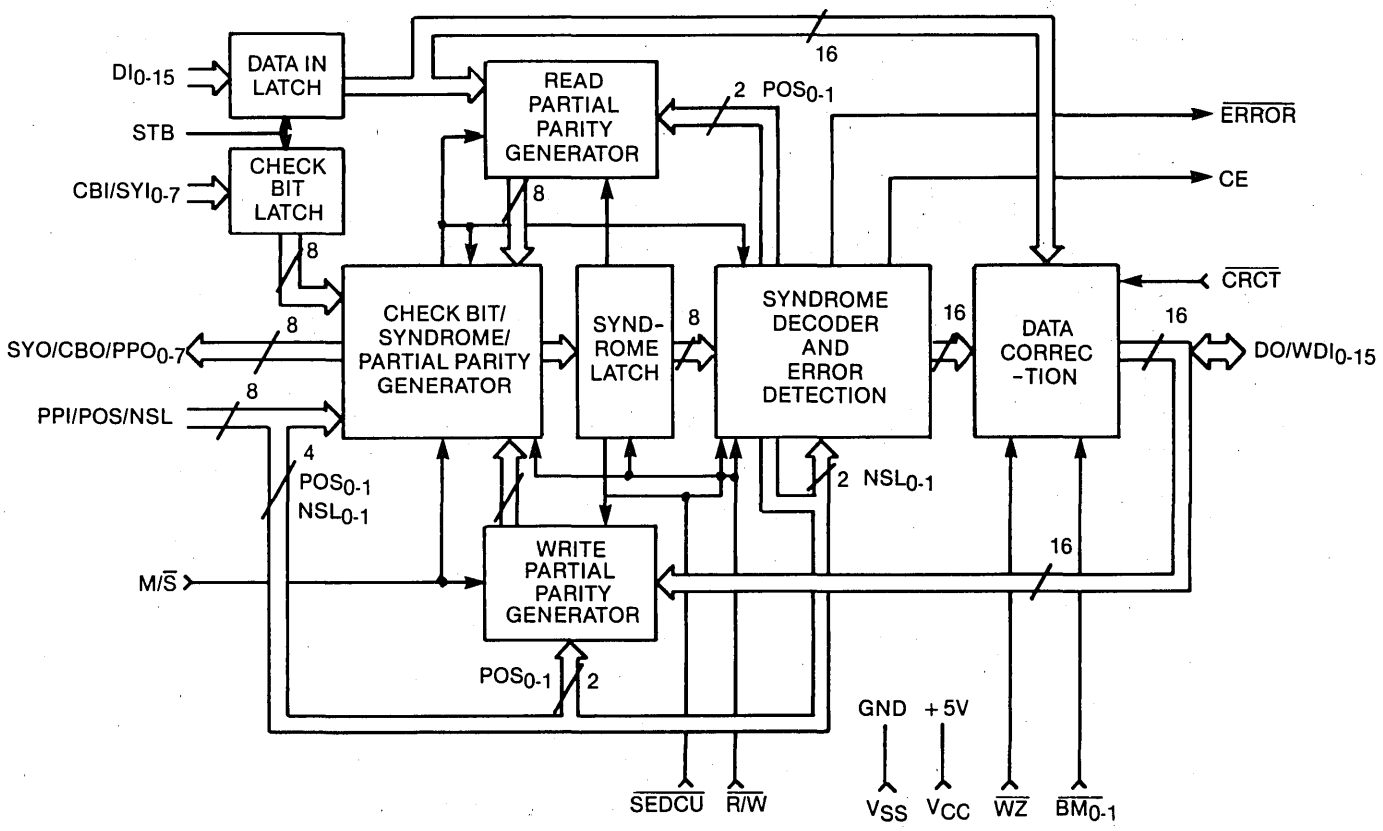
WD8206 Error Detection and Correction Unit

FEATURES

- Detects and Corrects All Single Bit Errors.
- Detects All Double Bit and Most Multiple Bit Errors
- 52 ns Maximum for Detection; 67 ns Maximum for Correction (16 Bit System)
- Expandable to Handle 80 Bit Memories
- Syndrome Outputs for Error Logging
- Separate Input and Output Busses — No Timing Strobes Required
- Supports Reads With and Without Correction, Writes, Partial (Byte) Writes, and Read-Modify-Writes
- HMOS Technology for Low Power
- 68 Pin Leadless JEDEC Package
- Single +5V Supply

GENERAL DESCRIPTION

The HMOS 8206 Error Detection and Correction Unit is a high-speed device that provides error detection and correction for memory systems (static and dynamic) requiring high reliability and performance. Each 8206 handles 8 or 16 data bits and up to 8 check bits. 8206's can be cascaded to provide correction and detection for up to 80 bits of data. Other 8206 features include the ability to handle byte writes, memory initialization, and error logging.



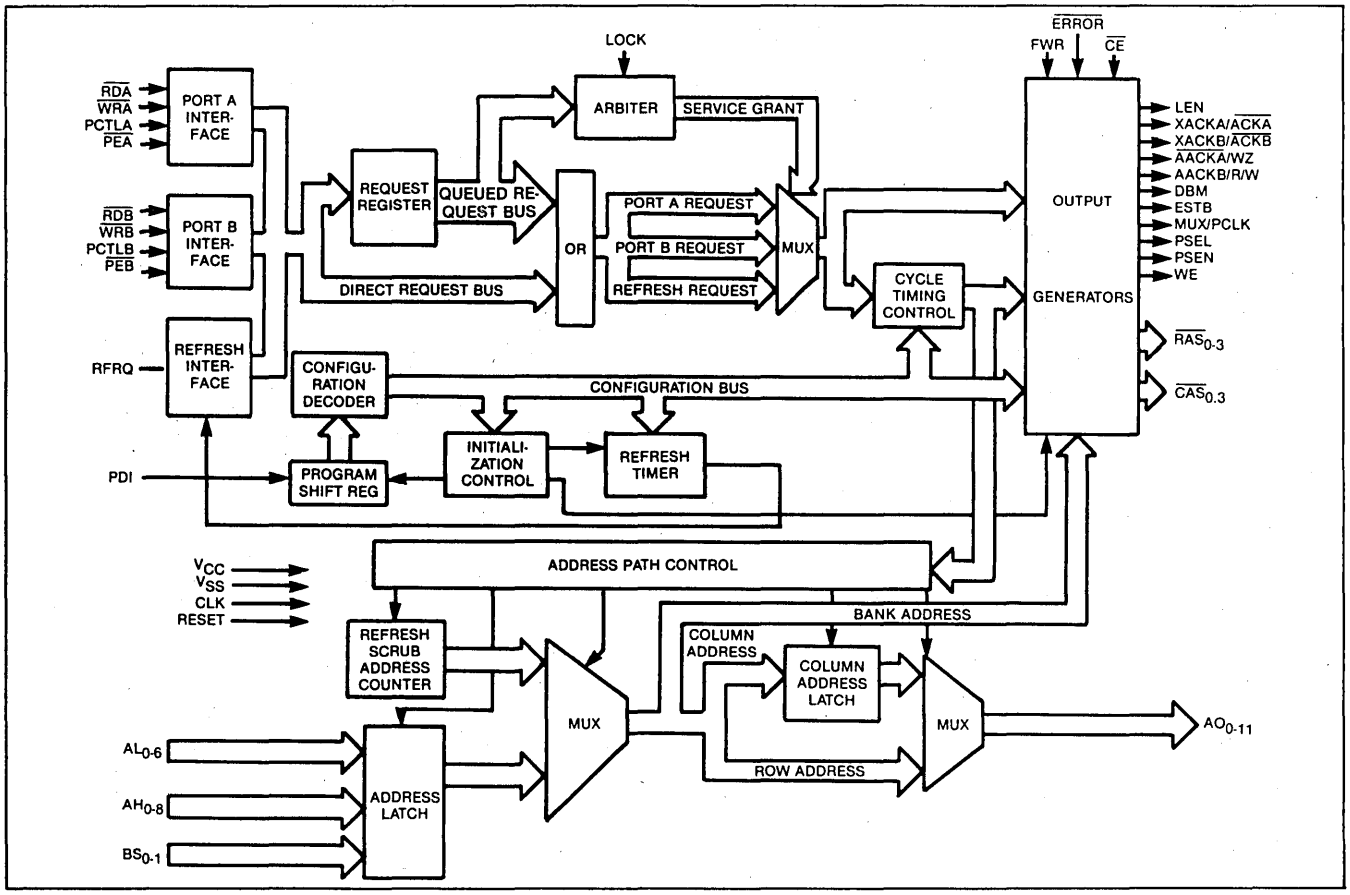
8206 BLOCK DIAGRAM

WD8207 ADVANCED DYNAMIC RAM CONTROLLER

FEATURES

- Provides All Signals Necessary to Control 16K (2118), 64K (2164A) and 256K Dynamic RAMs
- Directly Addresses and Drives up to 2 Megabytes without External Drivers
- Supports Single and Dual-Port Configurations
- Automatic RAM Initialization in All Modes
- Five Programmable Refresh Modes
- Transparent Memory Scrubbing in ECC Mode
- Supports Intel IAPX 86, 88, 186, and 286 Microprocessors
- Data Transfer Acknowledge Signals for Each Port
- Provides Signals to Directly Control the 8206 Error Detection and Correction Unit
- Supports Synchronous or Asynchronous Operation on Either Port
- +5 Volt Only HMOSII Technology for High Performance and Low Power

The WD8207 Advanced Dynamic RAM Controller (ADRC) is a high-performance, systems-oriented, Dynamic RAM controller that is designed to easily interface 16K, 64K and 256K Dynamic RAMs to Western Digital and other microprocessor Systems. A dual-port interface allows two different busses to independently access memory. When configured with an 8206 Error Detection and Correction Unit the 8207 supplies the necessary logic for designing large error-corrected memory arrays. This combination provides automatic memory initialization and transparent memory error scrubbing.



8207 Block Diagram

PRELIMINARY INFORMATION

WD74HC200 256 x 1 CMOS Static RAM

FEATURES

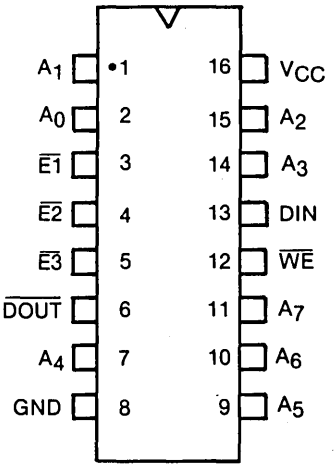
- PIN COMPATIBLE WITH 74LS200
- LOW POWER DISSIPATION .48 MW/BIT TYPICAL
- BATTERY-BACK UP/STANDBY MODE
- COMPLETELY STATIC
- SINGLE +5V SUPPLY
- FULLY TTL COMPATIBLE
- 35 ns TYPICAL ACCESS TIME

GENERAL DESCRIPTION

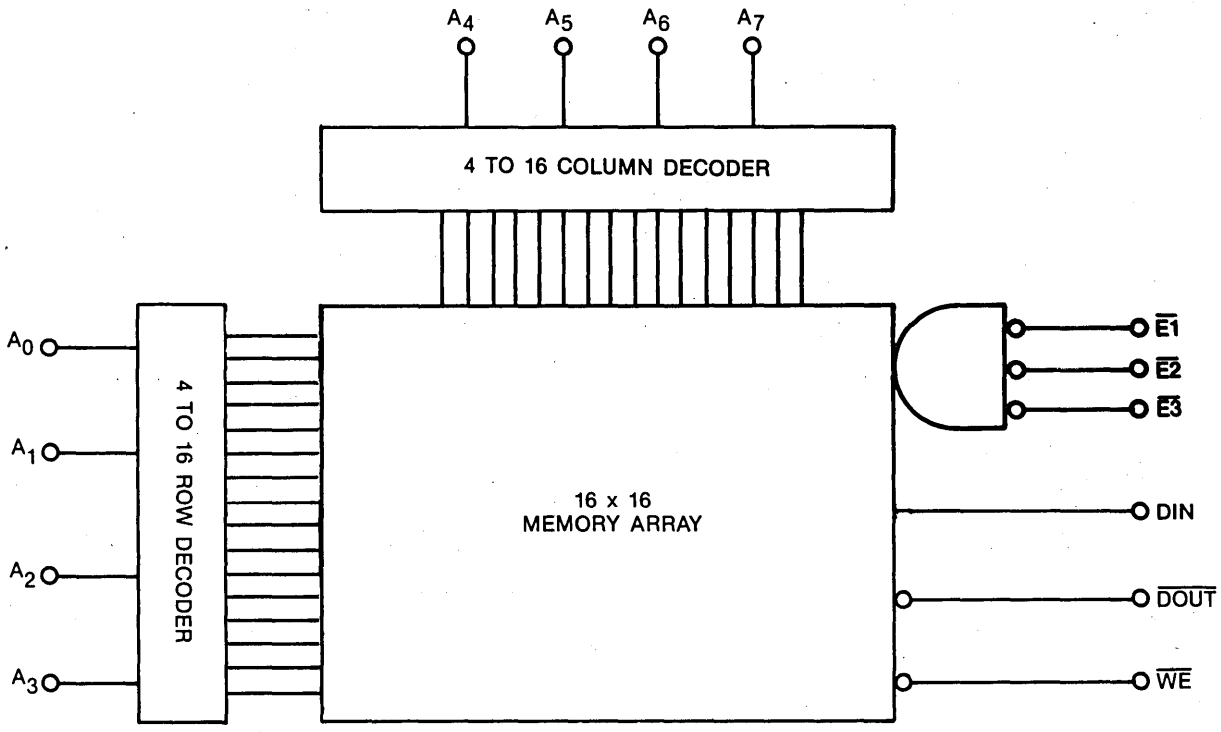
The WD74HC200 256x1 RAM is both pin and speed compatible to the SN74LS200 and AM27LS00. The device is fabricated in CMOS, offering a dramatic decrease in power dissipation and increased noise immunity. It is well suited for high-speed buffer memories in digital systems and bit-slice designs.

The memory is organized as a 256-word by 1-bit width with an 8 bit binary address field and separate data in and data output lines. It has 3 active low chip selects and a three-state output.

The WD74HC200 operates from a single +5 volt supply and is available in a dual-in-line plastic or ceramic package.



PIN DESIGNATION

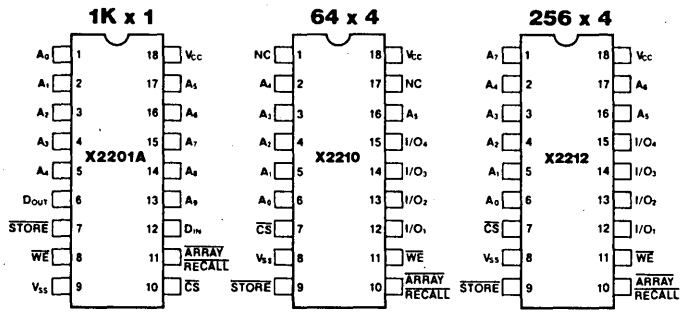


BLOCK DIAGRAM

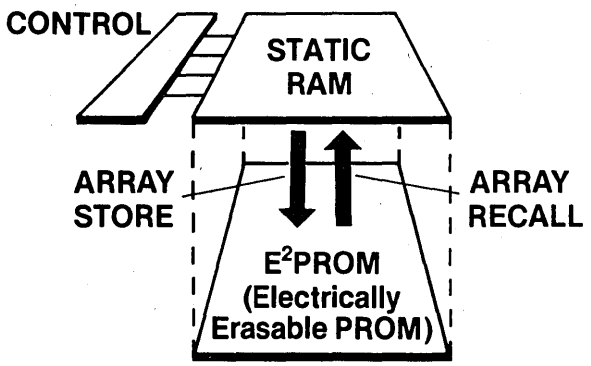
A Growing Family of
Nonvolatile Static RAMS

Commercial,	X2201A	1024 x 1 Bit Nonvolatile Static RAM
Industrial, Military	X2212	256 x 4 Bit Nonvolatile Static RAM
and MIL-STD 883B	X2210	64 x 4 Bit Nonvolatile Static RAM

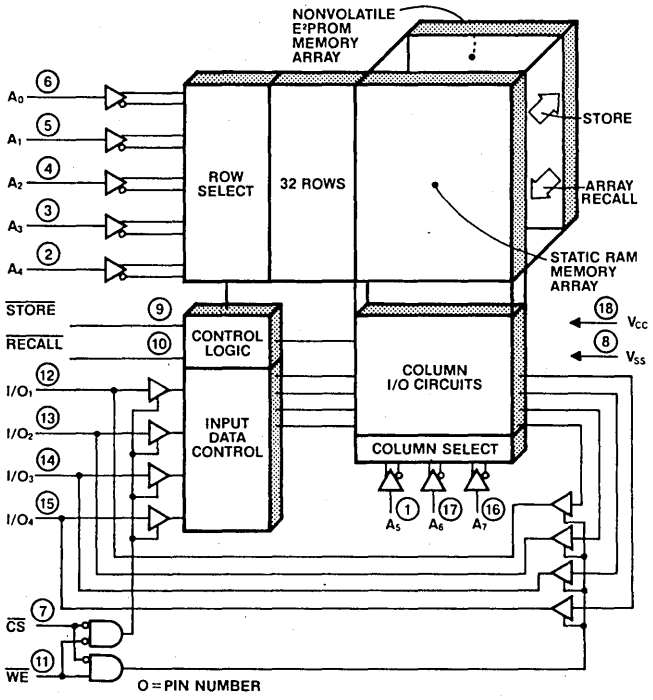
- **NONVOLATILE STATIC RAM:** The **X2201A, X2210,** and **X2212** are organized as conventional static RAMs overlaid bit-for-bit with a nonvolatile Electrically Erasable PROM (E^2PROM). Nonvolatile data can be stored in the E^2PROM and at the same time independent data can be accessed in the RAM memory. At any time, data can be transferred back-and-forth between the RAM and E^2PROM by simple store and array recall signals.
- **5V ONLY:** High-voltage pulses or supplies are never required. A single 5V supply is the *only power source* ever required for any function.
- **EASE-OF-USE:** Unprecedented simplicity, all inputs and outputs are directly TTL compatible. Fully static timing. Three-state output. 18-pin package.
- **PERFORMANCE:** RAM cycle time is less than 300 ns. During the lifetime of the device, data can be recalled from the E^2PROM an unlimited number of times.
- **POWER-FAILURE PROTECTION:** One simple TTL signal saves the entire RAM database. A snap-shot nonvolatile copy of all RAM data is internally stored safe without power and can be recalled to the RAM when power returns. No battery backup required.
- **ORGANIZED FOR MICROCOMPUTER SYSTEMS:** The common data input and output is organized four bits wide on the X2210 and X2212. The X2201A is organized conveniently by one for larger memory applications.
- **Xicor's** products are fabricated with reliable n-channel floating gate MOS technology. For systems where RAM nonvolatility or *in-the-circuit* ROM changes by TTL signals are important, the **Xicor X2201A, X2210,** or **X2212** is the ideal choice.



MEMORY ORGANIZATION



FUNCTIONAL DIAGRAM X2212 (256 x 4)



XICOR, Inc., 851 Buckeye Court, Milpitas, California 95035 (408) 946-6920 TWX 910-379-0033

Commercial, Industrial, Military and MIL-STD 883B

X2816A 2K x 8 Bit Electrically Erasable PROM
X2804A 512 x 8 Bit Electrically Erasable PROM

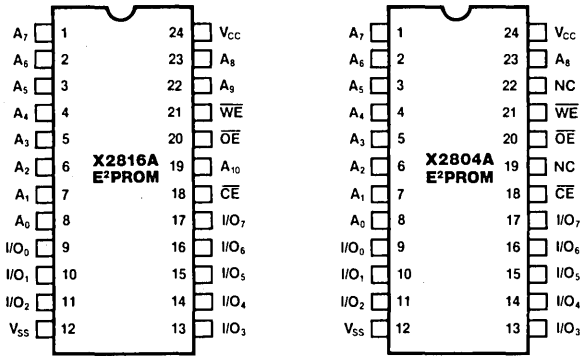
- Simple Byte Write Operation
  - No High Voltages Necessary
  - Single TTL level $\overline{WE}$ Signal Modifies Data
  - Internally Latched Addresses and Data
  - Automatic Write Time-out
  - Noise Protected $\overline{WE}$ Pin
- Reliable N-Channel Floating Gate MOS Technology
- Conforms to JEDEC Byte-wide Standard
- Single 5-Volt Supply
- Byte Write Time: 10ms Max.
- Fast Access Time: 300ns Max.
- Low Power Dissipation
  - Active Current: 110mA Max.
  - Standby Current: 40mA Max.

The Xicor X2816A (16,384 bits) and X2804A (4,096 bits) are electrically erasable programmable read-only memories (E²PROMs) with unprecedented ease-of-use features. Xicor E²PROM data can be modified using simple TTL level signals and a *single 5-volt power supply.* In addition, Xicor E²PROMs are operationally and pin compatible with existing 2K x 8 byte-programmable E²PROMs which require an additional high voltage power supply for programming. (See *optional* high voltage programming compatible mode.) Writing data in Xicor E²PROMs is analogous to writing data in a static RAM. A 200ns TTL low level signal to the $\overline{WE}$ pin initiates a byte write operation which is automatically timed out in a maximum of 10ms. Since addresses and data are internally latched, Xicor E²PROMs free the system for other tasks during the 10ms period, such as programming other Xicor E²PROMs. In addition to byte modification capability, a 10ms total chip erase feature is provided.

Xicor E²PROMs use a 2-line control architecture, $\overline{CE}$ and $\overline{OE}$, to eliminate bus contention in a system environment. A power down mode is featured. In the standby mode, power consumption is reduced by 64% without increasing access time. The standby mode is achieved by applying a $\overline{CE}$ high signal.

The X2816A and X2804A are fabricated with the same reliable n-channel floating gate MOS technology used in Xicor's popular 5-Volt programmable NOVRAM™ memories.

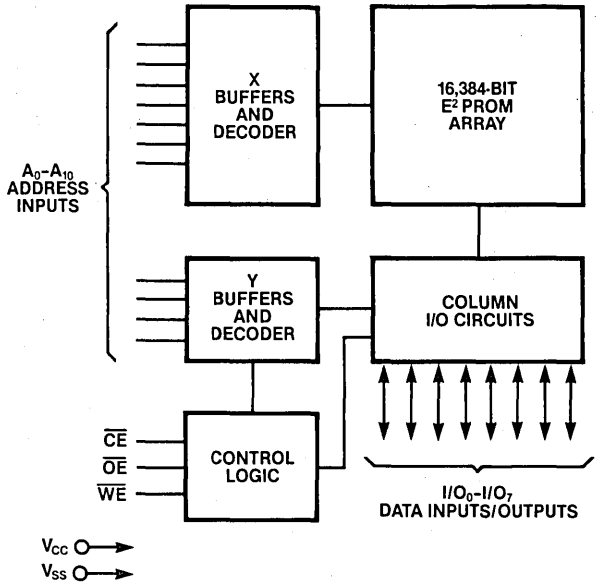
PIN CONFIGURATIONS 24 PIN DIP .600"



PIN NAMES

A_0-A_{10}	ADDRESS INPUTS
I/O_0-I/O_7	DATA INPUTS/OUTPUTS
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
V_{CC}	+5V
V_{SS}	GROUND
NC	NO CONNECT

FUNCTIONAL DIAGRAM X2816 (2K x 8)



NOVRAM™ is a trademark of Xicor, Inc., for its nonvolatile RAM devices.

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INTRODUCTION TO PROM PROGRAMMERS

This section describes instruments used to enter assembly language code into programmable devices such as PROMs, EPROMs, EEPROMs, EAROMs, PALs, PLAs and MPUs. Equipment listed includes programmers designed for system development, production and field-service applications. Manufacturers are sequenced alphabetically, and each system is characterized by pertinent selection factors. These parameters include programmed device types, type of display, personality modules, edit functions, programming checks, self-test features and types of interface ports.

Some manufacturers assign different model numbers to units having capabilities beyond those listed for the model designated at the top of the Master Selection Guide. In these cases the units are covered under "Comments".

Detailed Product Information provided by:

The manufacturers listed above have provided detailed information on their latest and most significant products.

PROM PROGRAMMERS

Manufacturer	Advent Products	Citel, Inc.	Citel, Inc.	Curtis Electro Devices
Model	μP-8	CopyRom 3716	System 37	PR-100A
FOR DETAILED DATA SEE:				
Application	Development	Production	Development, production, field service	Development, production, field service
Capability	Program, copy, compare, read	Copy	Program, copy, compare, read, erase	Program, copy, compare, read, test
Programmed Devices	EPROM	EPROM, EEPROM	EPROM	FPLA: Signetics 82S100, 82S101, 82S106, 82S107
Display	CRT	LED	LED	LED
Maximum PROM Array (bit configuration)	32K x 8	32K x 8	32K x 8	
Personality Modules	Not required — replaced by operator-selectable switches	Software based	Not required; software-based	Dedicated
Maximum Gang Capacity (no. slave sockets)		16	1	
Edit Functions			Insert, move, delete, nibble swap, memory map	Insert, delete
Programming Checks	Verify, program PROM, checksum, erased	Blank, checksum, illegal bit, verify	Blank, checksum, illegal bit, verify	Verify
Self-Test		Keyboard, display, switches	Keyboard, display, switches buffer memory	
Prompting	Audible	Visual, audible	Visual, audible	Visual
Buffer Memory			8K x 8, expandable	
I/O Interface	RS232 serial, selectable baud rates from 2400 to 9600		Parallel TTL, RS232 serial	
Safety Features		Short-circuit protection	Short-circuit protection	
Comments	Operates with any 8080/85/Z80 CP/M-based computer containing a minimum of 32K bytes of RAM and either port or memory-mapped I/O.			

PROM PROGRAMMERS (cont)

Manufacturer	Curtis Electro Devices	Curtis Electro Devices, Inc.	Digelec	Digelec
Model	PM3000S	PD2000S	UPP-801	UP-803
FOR DETAILED DATA SEE:				(Page 4101)
Application	Development, field service	Production	Development, production	Development, production
Capability	Program, read	Program, copy, compare	Program, copy, compare, read, test, erase	Program, copy, compare, read, test, erase
Programmed Devices	Bipolar PROM	Bipolar PROM	Bipolar PROM, CMOS PROM, EPROM, EAROM, PAL, PMUX, MPU	Bipolar PROM, CMOS PROM, EPROM, EEPROM, PAL, PLA, MPU
Display	Lamps, digit switch	Lamps	LED, hexadecimal	CRT
Maximum PROM Array (bit configuration)	4K x 8	4K x 8	50K x 8 (add field 64K x 8BMS)	50K x 8
Personality Modules	Generic	Dedicated	Dedicated, generic	Dedicated, generic, generic gang
Maximum Gang Capacity (no. slave sockets)		1		8
Edit Functions			Move, nibble swap, memory map, complement	Insert, move, delete, memory map
Programming Checks	V_{cc} sensitivity	Illegal bit, V_{cc} sensitivity	Blank, vertify, continuity, window check	Blank, checksum, illegal bit, verify parametric, continuity
Self-Test				Buffer memory, programming voltages, system PROMs
Prompting	Visual	Visual	Visual, audible	Visual, audible
Buffer Memory			4K x 8, 8K x 8, expandable, battery backup, stacking	4K x 8, 8K x 8, 16K x 8, 20K x 8, expandable, battery backup
I/O Interface			Parallel TTL, RS232 serial, current loop, selectable baud rate	Parallel TTL, RS232 serial, current loop, selectable baud rate
Safety Features			Short-circuit protection	Short-circuit protection
Comments			12 interfacing formats; 4 data-entry keyboard formats.	13 interfacing formats; industry STD bus (Multibus). Additional editing functions: search, replace, list of up to 72 addresses, address/data base selectable, complement. Characteristics of selected device displayed on CRT. Interactive system.

PROM PROGRAMMERS (cont)

Manufacturer	Data I/O	Data I/O	Data I/O	Data I/O
Model	29A Universal Programmer	20B Universal NMOS Memory Programmer	M120A Gang Programmer	M121A Gang Programmer
FOR DETAILED DATA SEE:				
Application	Development, field service	Development	Production	Production
Capability	Program, copy (load), compare (verify), read, test	Program, copy, compare, read	Program, copy (load), compare (verify), read, test, EEPROM cycling test	Program, copy (load), compare (verify), read, test, EEPROM cycling test
Programmed Devices	Bipolar PROM, CMOS PROM, EPROM, EEPROM, EAROM, PAL, PLA, MPU, FPGA, FPLA, FPRP, FPLS, prog. I/O port, PMUX	EPROM, EEPROM, MPU	CMOS PROM, EPROM, EEPROM, intelligent algorithms for EPROMs	CMOS PROM, EPROM, EEPROM, intelligent algorithms
Display	Sixteen-character fluorescent	LED	Sixteen-character fluorescent	Fluorescent
Maximum PROM Array (bit configuration)	16K x 8 (MOSpak)	8K x 8	16K x 8, expandable	16K x 8
Personality Modules	Software-selectable Paks (UniPak, MOSPak, LogicPak), generic gang, dedicated	Dedicated (universal NMOS and Intel single-chip microcomputers)	Software programmable	Software programmable
Maximum Gang Capacity (no. slave sockets)	8 (40 pin)	1	20	20
Edit Functions	Insert, move (block), delete, nibble swap, memory map, split, shuffle, clear, complement, fill RAM	Insert, delete, write, fill	Complement RAM, fill RAM, 16-bit mode	Insert, delete, I/O offset, begin RAM, fill RAM, complement RAM, 16-bit mode
Programming Checks	Blank, checksum, illegal bit, verify, overcurrent, backward device	Blank, checksum, illegal bit, verify	Blank, checksum, illegal bit, verify, overcurrent, backward device, mislocated device	Blank, checksum, illegal bit, verify, overcurrent, backward device, mislocated device, variable VCC on verification
Self-Test	Keyboard, display, switches, buffer memory, automatic power-up, program ROM, status of programming electronics	Keyboard, display, switches, buffer memory, automatic power-up, program ROM, status of programming electronics	Keyboard, display, switches, buffer memory, automatic power-up, program ROM, status of programming electronics	Keyboard, display, switches, buffer memory, automatic power-up, program ROM, status of programming electronics
Prompting	Visual, audible	Visual	Visual, audible	Visual, audible
Buffer Memory	8k x 8 (standard), 16k x 8, 64K x 8, expandable	2K x 8	16K x 8, expandable	16K x 8, 32K x 8, 64K x 8
I/O Interface	RS232 serial, current loop, selectable baud rate (50 — 19,200 baud)	RS232 serial, selectable baud rate (110-9600 baud)	RS232 serial, selectable baud rate (110-9600 baud)	RS232 serial (2), selectable baud rate (110-9600 baud)
Safety Features	Short-circuit protection, current-limit protection for programmed device	UL-listed	Short-circuit protection, current-limit protection for programmed device	Short-circuit protection, current-limit protection for programmed device
Comments	Edit in hexadecimal, octal or binary. English-language prompts, menus and error messages. Remote control and 26 development-system format translators are standard.		Remote control and 26 data translation formats are standard. M120A controls 200A Data Control Unit for program storage.	Can segment programs and load each segment into different PROMs simultaneously. Remote control and 26 data translation formats are standard. M121A controls 200A Data Control Unit for program storage.

PROM PROGRAMMERS (cont)

Manufacturer	Data I/O	E-H International	E-H International	Elind
Model	M100A Production Programmer	MicroSupport 1400	MicroSupport 16D	RP400-S
FOR DETAILED DATA SEE:				
Application	Production	Development, production, field service	Production	Development, production, field service
Capability	Copy (load), compare (verify), read, test	Program, copy, compare, read, test	Program, copy, compare, read, test	Program, copy, compare, read
Programmed Devices	Bipolar PROM, CMOS PROM, EPROM, EEPROM, EAROM, PAL, PLA, MPU	EPROM	EPROM	Bipolar PROM, EPROM, MPU
Display	Fluorescent	CRT, LED	LED	CRT
Maximum PROM Array (bit configuration)	16K x 8	8K x 8	8K x 8	8K x 8
Personality Modules	Software-selectable Paks (UniPak, Handler UniPak, MOSPak, LogicPak)	Software-selected	Software-selected	Dedicated, generic, gang
Maximum Gang Capacity (no. slave sockets)	8 (with gang module)	1	16	8
Edit Functions	Insert, delete, I/O offset, begin RAM, fill RAM	Insert, move, delete, nibble swap, memory map	Insert, move, delete, nibble swap, memory map	Insert, delete, Nibble swap
Programming Checks	Blank, checksum, illegal bit, verify, overcurrent, backward device	Blank, checksum, illegal bit, illegal bit, verify	Blank, checksum, verify, PROM integrity	Blank, checksum, illegal bit, verify
Self-Test	Keyboard, display, switches, buffer memory, automatic power-up, program ROM, status of programming electronics	Limited amount	Limited	Display, buffer memory
Prompting	Visual, audible	Visual	Visual, audible	Visual, audible
Buffer Memory	4K x 8, 8K x 8, 16K x 8	4K x 8	4K x 8	6K x 8
I/O Interface	RS232 serial, current loop, selectable baud rate (50 — 19,200 baud)	RS232 serial, current loop, selectable baud rate	RS232 serial, current loop, selectable baud rate.	RS232 serial, current loop, Selectable baud rate, 110 to 9600 baud
Safety Features	Short-circuit protection, current-limit protection for programmed device		Short-circuit protection	Full protection on programmed device
Comments	Operates with Handler Unipak for direct interface to MCT, Delta and other handlers. Remote control and 26 data translation formats are standard. M100A controls 200A Data Control Unit for program storage.	Programs bipolar PROM with addition of MicroSupport 1410 Satellite, and MPUs with addition of MicroSupport 1448 Satellite.		Unit is equipped with three fast programmable power supplies (100 nS/V) for programming voltages.

PROM PROGRAMMERS (cont)

Manufacturer	Intel	International Microsystems Inc.	International Microsystems Inc.	Kontron Electronics
Model	iUP-200/201	IM 3016 Multi-Master Programmer	IM 1010 Universal Programmer	MPP-80
FOR DETAILED DATA SEE:	(Page 1722)			
Application	Development, production	Production, development	Development, field service	Development, production, field service
Capability	Program, copy, compare, read, erase (E^2 only)	Program, copy, compare, read, test, erase	Program, copy, compare, read, test, erase	Program, copy, compare read, test, erase
Programmed Devices	Bipolar PROM, EPROM, EEPROM, MPU	EPROM, EEPROM, CMOS EPROM	Bipolar PROM, CMOS PROM, EPROM, EEPROM, EAROM, PAL	Bipolar PROM, CMOS PROM, EPROM, EEPROM, EAROM, PAL, PLA, FPLA, FPRP, FPGA, FPLS, PMUX
Display	LED	LED	LED	LED
Maximum PROM Array (bit configuration)	32K x 8 bits	16K x 8, 32K x 8	8K x 8	32K x 8
Personality Modules	Generic, gang, generic gang	Software programmable	Generic	Dedicated, generic, gang, generic gang
Maximum Gang Capacity (no. slave sockets)	8	16		8
Edit Functions	Move*, nibble swap*, n byte swap*, memory map*, enter	Move, delete, memory map, I/O offset, fill RAM	Insert, move, delete, nibble swap, memory map, search	Insert, move, delete, nibble swap, memory map, fill, invert
Programming Checks	Blank, checksum, illegal bit, verify, reverse socket detection	Blank, checksum, illegal bit, verify, misaligned or upside-down device, broken or bent pin, over-current	Blank, checksum, illegal bit, verify	Blank, checksum, illegal bit, verify at high and low V_{CC} limits
Self-Test	Buffer memory, motherboard, power supply, module	Keyboard, display, switches, buffer memory, automatic power reset, calibration, programming electronics	Keyboard, display, buffer memory module	Keyboard, display, switches, buffer memory
Prompting	visual, audible*	Visual, audible	Visual	Visual, audible
Buffer Memory	16K x 8, expandable to 32K; virtual buffer*	64K x 9 standard; 128K x 9 and 256K x 9, expandable	16K x 8, 32K x 8	4k x 8, 8k x 8, 16k x 8, 32k x 8 plus mass storage
I/O Interface	RS232 serial, automatic baud rate selection	RS232 serial, selectable baud rate	RS232 serial, current loop, selectable baud rate	RS232 serial, selectable baud rate
Safety Features	UL-listed, short-circuit protection, CSA-listed	UL-listed, circuit-breaker protection	Short-circuit protection	Short-circuit protection
Comments	* iUPS software package feature. Host software driver also provides file manipulation, file mapping, held file, screen editing, data manipulation and other features.	Simultaneous set programming ability, electrically isolated programming sockets, terminal and computer-control package allows the IM3016 to be operated remotely via computer.	PROM Emulation Module option allows user to test and debug programs before committing to PROMs.	Built-in uv source, IC handler interface. MPP 80SAM has acoustic coupler and modem.

PROM PROGRAMMERS (cont)

Manufacturer	Kontron Electronics	Kontron Electronics	Motorola	Oliver Advanced Engineering
Model	MPP-80S	EPP-80	MG8PPS	UPP-2700 EPROM Tester/Duplicator
FOR DETAILED DATA SEE:		(Page 4103)		
Application	Development, production, field service	Development, production	Development, production, field service	Production
Capability	Program, copy, compare, read, test, erase	Program, copy, compare, read, test, erase	Program, copy, verify, read, test, erase, help, odd/even	Program, copy, compare, read, test
Programmed Devices	Bipolar PROM, CMOS PROM, EPROM, EEPROM, EAROM, PAL, PLA, MPU, FPLA, FPGA, FPLS, PMUX	Bipolar PROM, CMOS PROM, EPROM, EEPROM, EAROM, PAL, PLA, MPU, FPLA, FDRP, FPGA, FPLS, PMUX	Bipolar PROM, CMOS PROM, EPROM, EEPROM, EAROM, PLA	EPROM
Display	LED	Fluorescent	CRT via terminal	LED
Maximum PROM Array (bit configuration)	32K x 8	32K x 8	8K x 8	32K x 8
Personality Modules	Dedicated, generic, gang, generic gang	Dedicated, generic, gang, generic gang	Dedicated	Generic gang
Maximum Gang Capacity (no. slave sockets)	8	8	One	16 (32 with Satellite)
Edit Functions	Set, insert, move, delete, nibble swap, memory map, fill, invert	Set, insert, move, delete, nibble swap, memory map, fill, invert, 16-bit split/shuffle, logical AND/OR/XOR, string search	Insert, move, delete, save, memory map, change	None allowed
Programming Checks	Blanks, checksum, illegal bit, verify at high and low V_{cc} limits	Blank, checksum, illegal bit, verify at high and low V_{cc} limits	Blank, illegal bit, verify	Blank, illegal bit, verify, matrix test*
Self-Test	Keyboard, display, switches, buffer memory, firmware integrity	Keyboard, display, switches, buffer, firmware integrity		Keyboard, switches, leakage test on socket matrix
Prompting	Visual, audible	Visual, audible	Visual,audible	Visual, audible
Buffer Memory	8K x 8, expandable to 32K x 8	8K x 8, expandable to 32K x 8	8Kx 8, expandable	None
I/O Interface	RS232 serial, current loop, selectable baud rate (50 to 38400 baud)	Parallel TTL, RS232 serial, current loop, selectable baud rate (50 to 38400 baud), IEEE-488	Proprietary	None
Safety Features	Short-circuit protection, uv eraser safety interlock	Short-circuit protection, uv eraser safety interlock	PROM insert safeguard	Short-circuit protection, UL-listed power supply
Comments	Built-in uv EPROM eraser. IC handler interface. Remote-controllable via RS232 port from terminal or host computer. MPP-80SAM has built-in acoustic coupler, modem and error-tolerant communications protocol.	Built-in uv EPROM eraser with keyboard-programmable timer. Remote-controllable via RS232 and IEEE-488 ports. Error-tolerant communications protocol for long-distance telephone transfers. Compatible with MPP-80S modules.		* Matrix test checks both data and address lines for ESD (electrostatic discharge) damage. Data lines are checked for min. sink and source current capability during both blank and verify tests. 100 — 240 Vac operation 50 or 60Hz.

PROM PROGRAMMERS (cont)

Manufacturer	Oliver Advanced Engineering	Oliver Advanced Engineering	Oliver Advanced Engineering, Inc.	PC/M Inc.
Model	UPP-28000 Scoop	UPP-28000-ZIF	Speed Screener I/II	660
FOR DETAILED DATA SEE:	(Page 4104)			
Application	Production	Production	Development, production, incoming test	Development, field service
Capability	Program, copy, compare, read, test, erase, dc parameters	Program, copy, compare, read, test, erase, dc parameters	Compare, read, pattern test, write RAMs	Program, copy, compare, read, test
Programmed Devices	EPROM, EEPROM, EAROM	EPROM, EEPROM, EAROM	Bipolar PROM, CMOS PROM, EPROM, EEPROM, EAROM, PAL, PLA, MPU	CMOS PROM, EPROM
Display	LED, ASCII	LED, ASCII	CRT, LED	CRT
Maximum PROM Array (bit configuration)	256K x 8	256K x 8	Up to 1 Mbyte x 8	1k x 4, 512k x 8
Personality Modules	Generic gang	Generic gang	Generic	Dedicated
Maximum Gang Capacity (no. slave sockets)	20 (40 with satellite)	18 (36 with satellite)	One each: 16, 18, 20, 24 (300 mil), 24 (600 mil), 28, 40	1
Edit Functions	None allowed	None allowed	Insert, move, delete, nibble swap, memory map, pattern editing	Insert, move, delete, nibble swap, memory map
Programming Checks	Blank, checksum, illegal bit, verify, V_{cc} level tests, matrix test	Blank, checksum, illegal bit, verify, V_{cc} level tests, matrix test.	Blank, checksum, illegal bit, verify, matrix test*, precision access-time screening**	Blank, checksum, verify
Self-Test	Keyboard, switches, leakage test on socket matrix	Keyboard, switches, leakage test on socket matrix	Keyboard, buffer memory, leakage test on socket matrix	Keyboard, display, switches, buffer memory
Prompting	Visual, audible, including voice option	Visual, audible, including voice option	Visual, audible menu driven	Visual, audible
Buffer Memory	None	2 ports for label printer and voice ennunciator	Up to 256K x 8	4k x 8
I/O Interface	2 ports for label printer and voice enunciator	UL-Listed, short-circuit protection, power-fail restart capability	Parallel TTL, Dual RS232 serial, selectable baud rate, automatic baud rate selection	Parallel TTL, RS232 serial current loop, selectable baud rate
Safety Features	UL-Listed, short-circuit protection, power-fail restart capability		UL-listed power supply, short-circuit protection	Short-circuit protection, grounded sockets
Comments			* See Model UPP-2700. ** Speed Selector I Speed Screener I ±5 ns @ 100 ns; Speed Screener II ±2.5 ns @ 100 ns.	

PROM PROGRAMMERS (cont)

Manufacturer	Pro-Log	Pro-Log	Pro-Log	Stag Microsystems Inc.
Model	M910A Control Unit	M980 Control Unit	System 90	PPX Universal PROM Programmer
FOR DETAILED DATA SEE:				(Page 4105)
Application	Development, production, field service	Development, production, field service	Development, production, field service	Development, production, field service
Capability	Copy, compare	Program, copy, compare, read	Program, copy, compare, read, test, erase	Program, copy, compare, read, test, erase
Programmed Devices	Bipolar PROM, CMOS PROM, EPROM, EEPROM, PLA	Bipolar PROM, CMOS PROM, EPROM, EEPROM	Bipolar PROM, CMOS PROM, EPROM, EEPROM, EAROM, PAL, MPU	Bipolar PROM, CMOS PROM, EPROM, EEPROM, EAROM, PAL, PLA, MPU, FPLA, FPLS, FPGA
Display	LED	LED	LED	CRT
Maximum PROM Array (bit configuration)	64K x 16	64K x 16	64K x 16	16K x 8K
Personality Modules	Dedicated, generic, gang, generic gang	Dedicated, generic, gang, generic gang	Dedicated, generic, gang, generic gang	Dedicated, generic, gang generic gang
Maximum Gang Capacity (no. slave sockets)	8	8	8	8
Edit Functions	Insert, move, delete, nibble swap, memory map	Insert, move, delete, nibble swap, memory map	Insert, move, delete, nibble swap, memory map, split/ interweave (4 and 8 bit), invert	Insert, move, delete, nibble swap, memory map, split, shuffle, complement, relocate
Programming Checks	Blank, verify, at high and low V_{cc} limits, checksum	Blank, checksum, illegal bit, verify at high and low V_{cc} limits	Blank, checksum, iillegal bit, verify, backward PROM, shorted address line, overload (V_{cc} and V_{pp})	Blank, checksum, illegal bit, verify, CRC
Self-Test	Keyboard, display, switches, buffer memory	Keyboard, display, switches, buffer memory	Keyboard, display, switches, buffer memory, programmable algorithms	Keyboard, display, switches, buffer memory, (requires CAT plug-in module)
Prompting	Visual, audible	Visual, audible	Visual, audible	Visual
Buffer Memory	8K x 8, 16K x 8, expandable, battery backup CMOS	8K x 8, 16K x 8, expandable, battery backup CMOS	8K x 8, 16K x 8, expandable, battery backup, CMOS	Expandable
I/O Interface	Parallel TTL, RS232 serial, selectable baud rate	Parallel TTL, RS232 serial, selectable baud rate	Parallel TTL, RS232 serial, selectable baud rate, TTY	Parallel TTL, RS232 serial, current loop, selectable baud rate
Safety Features	UL-listed, short-circuit protection	UL-listed, short-circuit protection	UL-Listed, short-circuit protection	
Comments	Two-year warranty. Separate master and copy sockets on personality modules (can duplicate directly from master to copy socket). Fixed V_{pp} power supplies do not require adjustment.	Two-year warranty. Separate master and copy sockets on personality modules (can duplicate directly from master to the copy socket). Fixed V_{pp} power supplies do not require adjustment.		

PROM PROGRAMMERS (cont)

Manufacturer	Structured Design Inc.	Structured Design Inc.	Sunrise Electronics, Inc.	Sunrise Electronics
Model	SD20/24 PAL Development System	PAL Burner SD-1000	ZAP80/ZAP48/ZAP68	Z-1000 & Z-2000 Universal PROM Programmers
FOR DETAILED DATA SEE:	(Page 4106)	(Page 4106)	(Page 4107)	(Page 4107)
Application	Development, production, field service	Development, production, field service	Development, field service	Production
Capability	Program, copy, compare, read, test	Progam, copy, compare, read, test	Program, copy, compare, read, test erase EEPROM and simulate. Devices software selected.	Program, copy, compare, read, test for device programmability, erase EEPROM. Device software
Programmed Devices	PAL	PAL	EPROM, EEPROM, Intel and Motorola MPU's	Bipolar PROM, CMOS PROM, EPROM, EEPROM, PAL, FPLA, MPU
Display	LED	LED	8-character LED	16-character alphanumeric LED
Maximum PROM Array (bit configuration)	2K	2K	128K bits	256K bits
Personality Modules	Dedicated	Dedicated		Slave for FPLA, PAL AIM devices and gang EPROM programming
Maximum Gang Capacity (no. slave sockets)	1	1		24 using 2 gang slaves
Edit Functions	Insert, move, delete, memory map	Insert, move, delete, memory map	Peek, poke, move, clear DATA RAM to state, odd/even byte separate/swap, list, checksum and selected range programming	Peek, poke, move, insert, clear DATA RAM to state, odd/even byte separate/swap, list, find, checksum and selected range programming
Programming Checks	Blank, verify, function test, continuity	Blank, verify, function test, continuity	Blank, checksum, illegal bit, verify	Blank, programmability, checksum, illegal bit, verify
Self-Test	Display, switches, buffer memory	Display, switches, buffer memory	Keyboard, DATA RAM, simulator, programming sockets, display	Keyboard, display, switches, DATA RAM, automatic voltage and timing recalibration before and during programming
Prompting	Visual	Visual	Visual, audio	English word, audible
Buffer Memory	4K x 8	2K x 8	8K x 8 expandable to 16K x 8, battery operated	16K x 8 expandable to 64K x 8
I/O Interface	RS232 serial, selectable baud rate	RS232 serial, selectable baud rate	RS232 serial, selectable formats, parity, baud rates 110-19.2K, terminal and computer control with selectable communications	Dual independent RS232 serial ports, selectable formats, parity, baud rates 110-19.2K, terminal and computer control
Safety Features	Short-circuit protection, continuity	Short-circuit protection	Short circuit protection	Over current and under current sensing
Comments	PALs are designed, simulated, programmed and functionally tested on the SD 20/20. The PAL assembler PALSAM is incorporated to read Bolean Logic equations and Function Tables. PAL specifications may be down loaded from another computer or stored in the on-board tape.	PALs are designed simulated, programmed and functionally tested on the PAL BURNER. PAL design specifications may be down loaded from another computer or stored in the on-board storage media. Programs all MMI, AMD, TI, and NATIONAL 20 and 24 pin PALs.	PROM data display simultaneous with RAM data. ZAP48 has same features as ZAP80 plus programming of Intel's 8748, 8749, 850, 8741, 8755A and 8751 MPU's. ZAP68 has same features as ZAP80 plus programming of Motorola's 68701 and 68705 MPU's.	Z-2000 has same features as Z-1000 except memory is 64K x 8 and has interfaces for 8 inch dual disc drives and IEEE-488.

PROM PROGRAMMERS (cont)

Manufacturer	Sunrise Electronics, Inc.	Sunrise Electronics	
Model	Z-1200 & Z-2400 Gang Programmers	Z-1248	
FOR DETAILED DATA SEE:	(Page 4107)	(Page 4107)	
Application	Production	Production	
Capability	Gang program, copy, compare, read, test for device programmability, EPROMS, EEPROMS and MPU's and erase EEPROMS. Devices software selected.	Gang program, copy, compare, read, test for device programmability	
Programmed Devices	CMOS PROM, EPROM, EEPROM, MPU, PAL, FPLA	8748, 8748H, 8749H, 8741, 8755A, 8751	
Display	Same as Z-1000/Z-2000	LED	
Maximum PROM Array (bit configuration)	Same as Z-1000/Z-2000	256K bits	
Personality Modules	Same as Z-1000/Z-2000	Slave for FPLA, PAL AIM devices and gang EOROM programming	
Maximum Gang Capacity (no. slave sockets)	36 using 2 gang slaves	24 using 2 gang slaves	
Edit Functions	Same as Z-1000/Z-2000	Peek, poke, move, insert, clear DATA RAM to state, odd/even byte separate/ swap, list, find, checksum, and selected range programming	
Programming Checks	Same as Z-1000/Z-2000	Blank, programmability, checksum, illegal bit, verify	
Self-Test	Same as Z-1000/Z-2000	Keyboard, display, switches, DATA RAM, automatic voltage and timing recalibration before and during programming	
Prompting	Same as Z-1000/Z-2000	English word, audible	
Buffer Memory	Same as Z-1000/Z-2000	16K x 8, expandable to 64K x 8	
I/O Interface	Same as Z-1000/Z-2000	Dual RS232 serial ports, selectable formats, parity, baud rates 110 to 19.2K, terminal and computer control, 8-bit parallel port	
Safety Features	Same as Z-1000/Z-2000	Over-current and under-current sensing	
Comments	Z-2400 has same features as Z-1200 except memory is 64K x 8 and has 8 inch dual disc drives and IEEE-488 included.	Z-2448 has same features as Z-1248 except memory is 64K x 8 and it has 8-inch dual disc drives and IEEE-488 included.	

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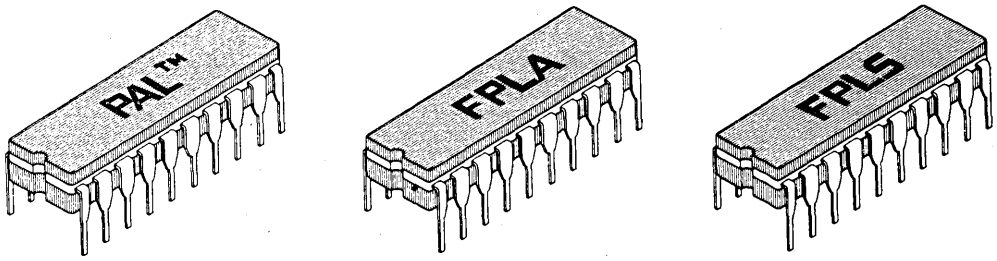

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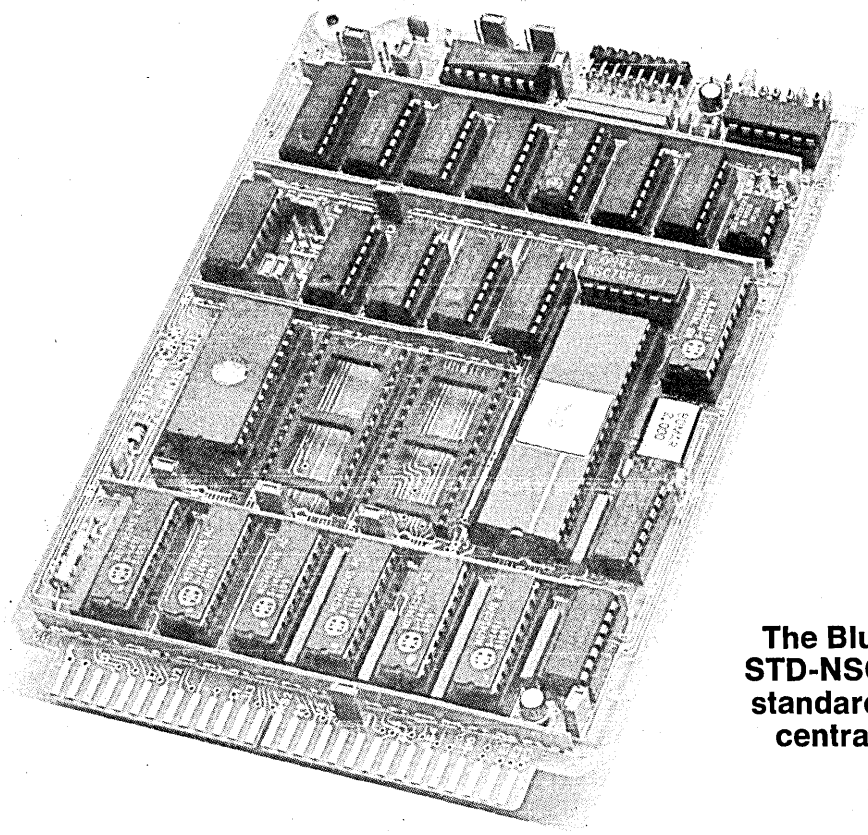

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ICL8212C	Micropower Voltage Detector
MM74PC00	Quad 2-Input NAND Gate
MM74PC32	Quad 2-Input OR Gate
MM74PC08	Quad 2-Input AND Gate
MD74SC139	Octal Decoder/Demultiplexer
MM74PC74	Dual Type-D Flip-Flop
MSC74PC07	Hex Inverter
MM74C30	8-Input NAND Gate

Representative list of ICs on the Blue Chip Computer STD-NSC800 card. Key specifications for all of these ICs can be found in IC MASTER.

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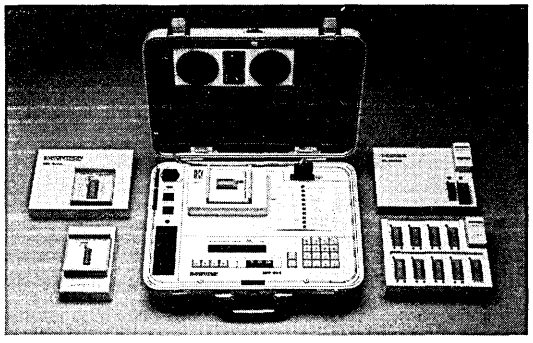

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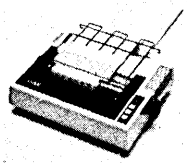

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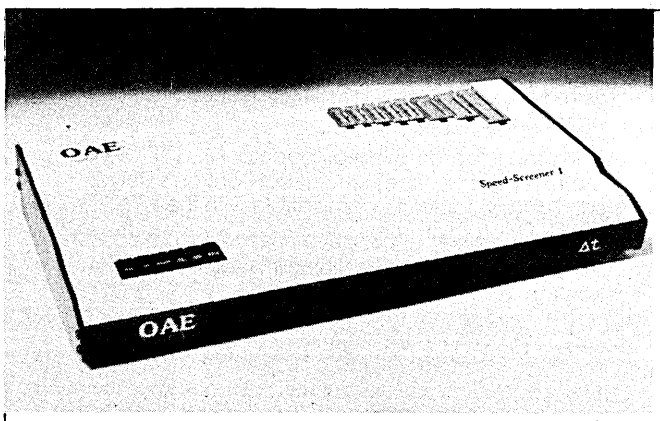

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- Perform both DC & AC parameter screening at the precise speed the part will be used. (Requires less than 4 seconds for a 2K x 8 memory device!)
- High speed handler interface allows one Speed-Screener to test up to 1000 parts per hour.

For more information call the OAE HOTLINE (213) 240-0080

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3B}IC/MST.AD 10/82

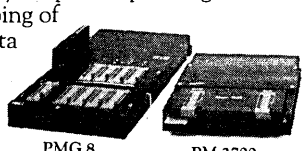
What you see is what you get.

You're looking at *the* PROM programmer available today with an integral CRT display and self-prompting.

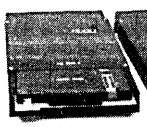
The PPX Universal Programmer from Stag Microsystems.

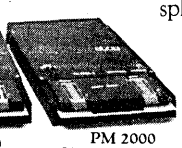
The PPX's fully interactive CRT display simplifies operating procedures and allows complete mapping of memory contents for fast, error-free data editing and automatic verification.

You get total programming capability.
And thanks to a full range of compact, low-cost personality modules that plug into the front panel within seconds, the PPX gives you total programming capability for over 450 PROMs, PALs, MPUs and IFLs, as well as future programmable devices.


PMG 8 Ganged PROM module

PM 2700 Universal EMOS module


PM 2100 Signetics IFL module


PM 2000 Universal PROM module

You get all these special features. Standard.
Firmware based and microprocessor-controlled, the PPX is an exceptionally powerful PROM programmer that's loaded with impressive features like an expandable RAM for data editing, assembly and block moving of data; a built-in, full-sized keyboard for stand-alone operation and large keys for operator comfort; serial and parallel interfaces for microprocessor system downloading and printer output; keyboard selection of input/output formats, including development system formats; front panel loading personality modules for quick, easy changes; relocate, checksum, CRC, split, shuffle and complement of RAM data; ganged modules compatibility; diagnostic capability; system expandability; and more.

All in all, the PPX Universal Programmer represents state-of-the-art design in a highly flexible, easy-to-operate, field proven machine, backed by nationwide service and continual software updates.

But why not see for yourself?

You can get the PPX Universal Programmer right now.
For more information, contact: Stag Microsystems Inc., 528-5 Weddell Drive, Sunnyvale, CA 94086. Phone toll free 800-227-8836 In California, call (408) 745-1991

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PRELIMINARY

SIMPLIFIED METHODOLOGY

Structured Design Provides the Complete PAL® Development System

PAL BURNER

At Structured Design we believe in methods — *complete step-by-step methods* that free your creativity to design hardware that's practical, marketable and tested.

Simplify, Simplify, Simplify

Like all methods that work, ours includes all you need to do your job. The SD1000 PAL Burner is the most complete programmer available today, working without costly add-on equipment or awkward switching of modules.

New PAL Burner Offers Cost-Effective Design Power

PAL Burner combines power with simplicity. It's simple enough that your non-technical staff can easily use it; yet, it's powerful enough to capture and store complex designs. Since PAL Burner includes a structured, menu-driven, user-friendly PAL assembler that prompts you through each step, you virtually eliminate syntax errors saving many design hours and dollars.

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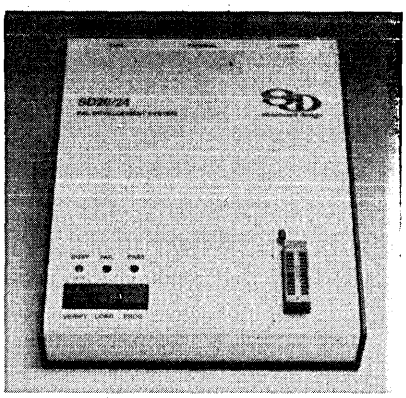
PAL Burner offers other benefits: programs all current PALs (Monolithic Memories, Texas Instruments, National Semiconductor, Advanced Micro Devices), built-in PALASM simulator and portability. Weighing only two pounds, PAL Burner is easy to pack in your briefcase to capture after-hours design inspirations.

In addition, PAL Burner is upward compatible. We can meet new firmware and software developments almost as they're introduced.

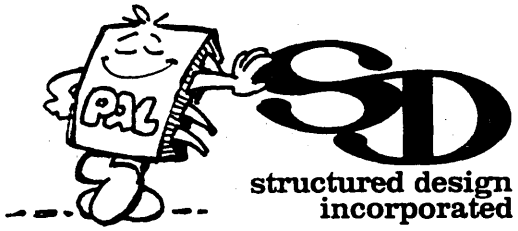
SD1000 PAL Burner

- **Assembles Boolean equations through new menu-driven PALASM**
- **Programs 20-pin and 24-pin PALs**
- **Programs MMI, National, TI, and AMD PALs**
- **Stores PAL design specification in E-PAC**
- **Verifies logic through Function Test**
- **Verifies Boolean equations through SIMULATE function**
- **Scores Function Test with Stuck-High/Stuck-Low FAULT Grading**
- **Verifies socket connection through Continuity Test**
- **Blows security fuse**



Also available is our original PAL Programmer, the SD 20/24 PAL Development System.

Call us first for a simple method — you won't need to call anyone else!



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Telex 172931

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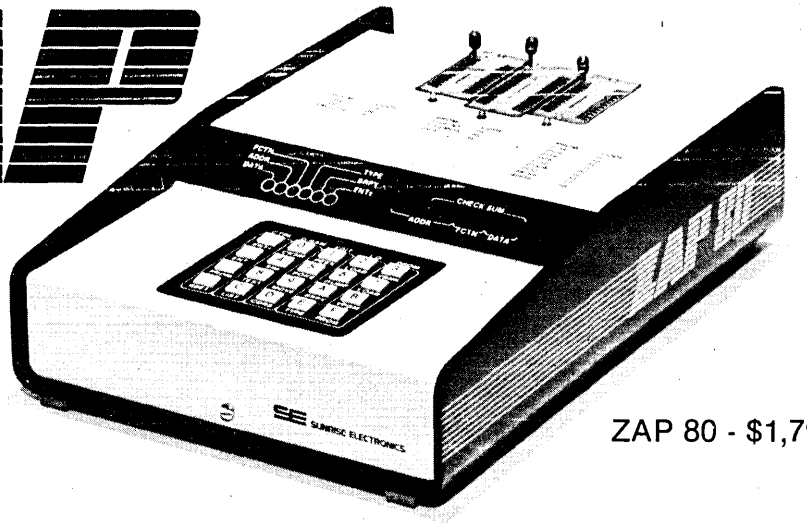
ZAP



ZAP 80 - $1,795

A SERIES OF PROGRAMMING INSTRUMENTS

The ZAP Series of programmers consists of three convenient, cost effective and unique instruments for engineering and field service applications.

- **Programs EPROMs, EEPROMs and microcomputers**
- **Built-in PROM simulator**
- **Serial I/0**
- **Battery Operated, hand held**
- **Automatic self-test**
- **Easy operation with prompt lights**

EASE OF OPERATION

Each system function is clearly printed above the respective key on the ZAP keyboard. The six prompt lights on the left side of the display tell the operator what to do for each step. The socket LED's indicate where to place the device to be programmed or verified.

The bottom cover is printed with complete operating instructions, simulator switch selection and baud rate/ parity code tables.

Operator invoked self test commands test the Data RAM, Processor, Simulator and Programming Circuits.

An extensive editor includes Peek, Poke, Move, Checksum, Clear to State, and List commands; a beeper signals the operator that the function is complete.

Commands are included to separate odd and even bytes for 16 bit microprocessor applications.

HAND HELD BATTERY OPERATION

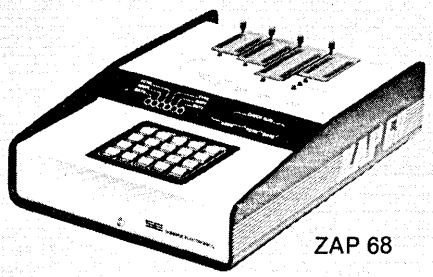
With any of the three ZAPS, the operator can load data at one location and carry the unit to another for programming, simulating or editing. The built in .9AH Nicad battery pack will power the unit in the Edit or Simulate mode for 3-4 hours or program 20 2K EPROMS.

The small A/C Adapter charges the batteries while the unit is in operation or when the unit is turned off.

BUILT IN PROM SIMULATOR

The PROM simulator personality is set with a 10 pole DIP switch on the bottom of the unit. Included is a 36" long simulator cable terminated with a 28 pin DIP plug for interfacing to the host system. Simulator specifications: less than 250ns access time, 30pf load capacitance, LS input levels and loading for address lines and 1 TTL load output drive.

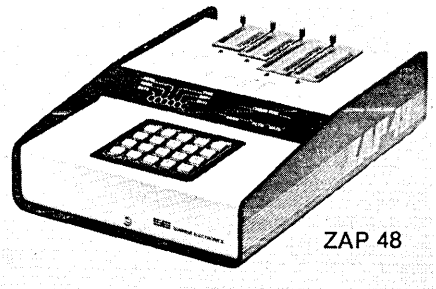
The simulator feature saves time in both hardware and software development and simplifies the task of making object level patches.



ZAP 68

SERIAL I/O

RS-232 and 20ma current loop are standard in each unit. The CTS and DTR lines are used in the RS-232 connection. Baud rates are keyboard setable from 110 to 1200. Terminal and keypad control are implemented by an internal scan algorithm. Formats are included for interfacing to most development systems and computers.



ZAP 48

PROGRAMMING CAPABILITY

Each of the ZAP units simulates and programs all single voltage EPROMS and EEPROMS.
In addition:

- ZAP 48 programs INTEL Microcomputers.
- ZAP 68 programs MOTOROLA Microcomputers.
- ZAP 80 programs three voltage EPROMS.

DEVICE \ UNIT	ZAP 80	ZAP 48	ZAP 68
2716/2516	P/S	P/S	P/S
2732/2532	P/S	P/S	P/S
2764/2564	P/S	P/S	P/S
68764	P/S	P/S	P/S
48016	P/S	P/S	P/S
2708/TMS2716	P/S	S	S
8748/8749		P	
8741/8755A		P	
8751		P	
68701/68705			P
PRICE	$1795.	$2295.	$2295.

P = Program/Verify/Load S = Simulate

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INTRODUCTION TO CUSTOM CIRCUITS

This section describes services and products of companies supplying digital, linear and combined ditigal/linear custom circuits. Listed alphabetically in the Master Selection Guide, the companies are characterized by descriptions of design services, production facilities, process technologies and testing capability. Options for user contribution to custom-circuit projects are outlined by listing the vendor's preferred level of user input which can range anywhere from system concept to a known good device.

Semicustom devices covered are restricted to gate and cell arrays that are customized by a final interconnect process. Field-programmable devices are not included in this section. PALs are listed in the Memory section, and PLAs are found in both Memory and Digital sections.

Detailed Product Information provided by:

The manufacturers listed above have provided detailed information on their latest and most significant products.

EINFÜHRUNG KUNDEN-SPEZIFISCHE ICs

Deiser neue Abschnitt beschreibt Dienstleistungen und produkte von Herstellern, die digitale, lineare und kombinierte digital/lineare kundenspezifische Schaltkreise anbieten. Die Firmen werden in alphabetischer Reihenfolge genannt und anhand ihrer Fähigkeit zum Schaltkreis- Entwurf, ihrer Produktionsanlagen, Prozeßtechniken und Testmöglichkeiten beschrieben. Die verschiedenen Möglichkeiten des Anwenders im Hinblick auf dessen Angaben sind durch eine Auflistung der vom Hersteller gewünschten technischen Details erläutert. Diese können von einer Gundkonzeption bis zu einem bekannten, funktionierenden Bauelement reichen.

Die enthaltenen halb-spezifischen (semicustom) Bauteile beschränken sich auf Gatter- und Zellen-Arrays, die durch die letzte Maske zum kundenspezifischen Schaltkreis werden. Feldprogrammierbare Bauteile sind in diesem Abschnitt nicht enthalten. PALs werden unter Speichern (Memory) aufgeführt und PLAs finden sich sowohl im Memory- als auch im Digitalteil.

INTRODUCTION AUX CIRCUITS FAITS SUR COMMANDE

Nouvelle cette année, cette Section décrit les services et produits fournis par des sociétés fabriquant sur mesure des circuits digitaux, linéaires, digitaux/linéaires. Le Guide Général de Sélection offre sur plusieurs pages un tableau indiquant par fabricant les services offerts, les équipements disponibles, les systèmes technologiques, et les procédés de test utilisés. Les possibilités de collaboration entre le fabricant et le client sont également indiquées dans ce même tableau.

Les produits partiellement faits sur mesure ont été limités aux "portes" et "cellules de mémoire" qui sont individualisées par un procédé final d'interconnexion. Les appareils programmables à l'extérieur ne sont pas considérés dans cette Section. Le PALs sont étudiés dans la Section "Mémoires", et les PLAs se trouvent dans les Sections "Mémoires" et "Systèmes Digitaux".

INTRODUCCIÓN A LOS CIRCUITOS POR PEDIDO

Esta sección, nueva para este año, describe servicios y productos de compañías que ofrecen circuitos por pedido, sea digital, lineal y digital/lineal combinado. Apareciendo en orden alfabético el la Guía Maestra de Selección, las compañías se caracterizan por descripciones de servicio de deseño, taller de producción, technologia de processos y capacidad de distintas pruebas. Opciones de contribución por el operador en los proyectos de circuitos por pedido, están delineados en la lista de nivel de asistencia del operador preferido por el fabricante que abarca de concepto de sistema a pieza comprobada buena.

Componentes a pedido limitado están restringidos a redes de puertas y celdas electrónicas que son "a pedido" en el proceso final de interconección. Componentes programables en el campo no están incluidas en esta sección. Los PALs aparecen en las lista la sección de Memoria y los PLAs se encuentran en ambas secciones bajo Memoria y Digital.

カストムサーキットへの案内

本年新たに加わったこのセクションにはディジタル，リニア，双方兼ねたカストム回路を供給するメーカーのサーヴィスと製品を掲載しています。メーカー名はＡＢＣ順にマスターセレクションガイドにのっていますが，そのメーカー毎に，デザイン，製造設備，プロセス技術，テスト能力を示してあります。カストムサーキットに関するメーカー側のカストマー参加希望はシステムの概念から良く知られている製品の良品迄概略を記載しています。

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Options for Going Custom

For many applications, standard integrated circuits may be inappropriate from the standpoints of cost, size, power consumption or reliability. Moreover, unique features demanded by proprietary products often require entirely new circuit configurations. As a result, customized ICs are assuming an increasingly important role in system design.

Custom IC suppliers report that the chief benefits enjoyed by nearly all custom-circuit users are low-cost parts and cost savings resulting from reduced printed-circuit board space, parts handling, inventory, testing requirements and system maintenance. Obtaining these benefits requires careful consideration of the many options provided by both custom ICs and other approaches which ultimately effect economics.

For example, in addition to standard and custom parts, options for implementing new system designs include semicustom ICs, microcomputers, custom microcomputers, a mixture of microcomputers and custom ICs, or a mixture of all of these. The system development strategy used depends largely upon marketing objectives and may require staged system development, first with standard ICs, then with semicustom ICs and, finally, full custom units. Or, the strategy may dictate developing standard or semicustom prototype systems with concurrent verification of a full custom design.

Another option is to alter a standard microprocessor and other standard circuits, rather than using a full custom design. Customizing standard products can reduce the design costs, turnaround time and risks of a full custom design. In some cases, semicustom or custom circuits can replace microprocessors which have been used in dedicated, mostly controller-type applications. Or, a custom circuit may be a direct integration of several standard ICs, such as op-amps, comparators and resistor networks.

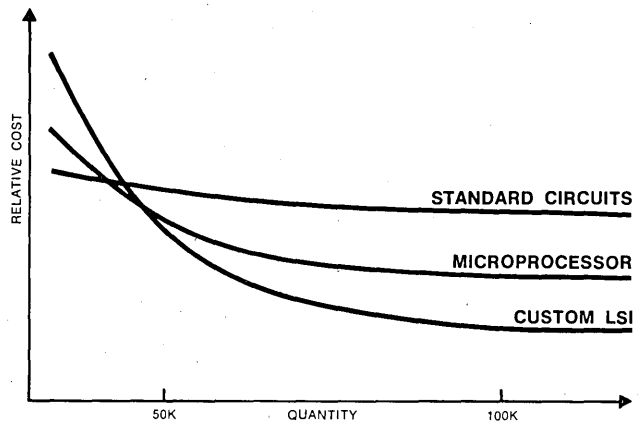
All approaches require up-front decisions involving design, prototype and production turnaround times, volume/cost tradeoffs, alternate sourcing, circuit configuration and process technologies, and the user/supplier interface. The most critical factor, however, is cost.

The cost of a nonstandard IC includes expenses for design and tooling, wafer and chip processing, packaging and testing.

Design and Tooling: Until recently, IC users had just two options for implementing new designs: standard parts and full custom circuits. When standard parts were inadequate, a user had to commit to great production volumes to amortize high development costs. Additionally, development times often extended well over a year, and chances of initial success were relatively slim. However, custom suppliers have minimized these drawbacks by devising new customizing techniques to the extent that few custom circuits now are developed entirely from scratch.

Full Custom: In this approach the circuit designer draws from a collection of time-tested circuit modules and components to customize a chip. These elements of known performance are located on the chip with the assistance of CAD equipment to form optimized interconnect patterns, thereby minimizing chip area and thus cost. Full custom design gives the most efficient use of silicon chip area. Although design turnaround time has been longer than other options, advanced CAD techniques are closing the gap.

Semicustom: This approach produces custom circuits by interconnecting repetetive patterns of preprocessed circuit elements on a chip called a *masterslice*. Because a masterslice is processed just short of the final interconnect pattern, the same part is mass-produced for use by all customers, with customizing occuring at the final interconnect stage.



Standard circuits are recommended for production volumes below 1000 units. Intermediate-volume applications may benefit best from customizing through software, such as with microprocessors. Custom chips have the lowest cost at high-volume production. Source: National Semiconductor

Gate arays are masterslices containing repetitive patterns of transistors connected as logic gates. *Device arrays* are patterns uncommitted transistors and resistors. The next level of customization uses an array of unconnected transistors and resistors called *cells*. Each cell can be interconnected internally to provide a specific logic function, and each cell on the chip interconnected into a customized system. The repertoire of allowable cell functions is called the *cell library*.

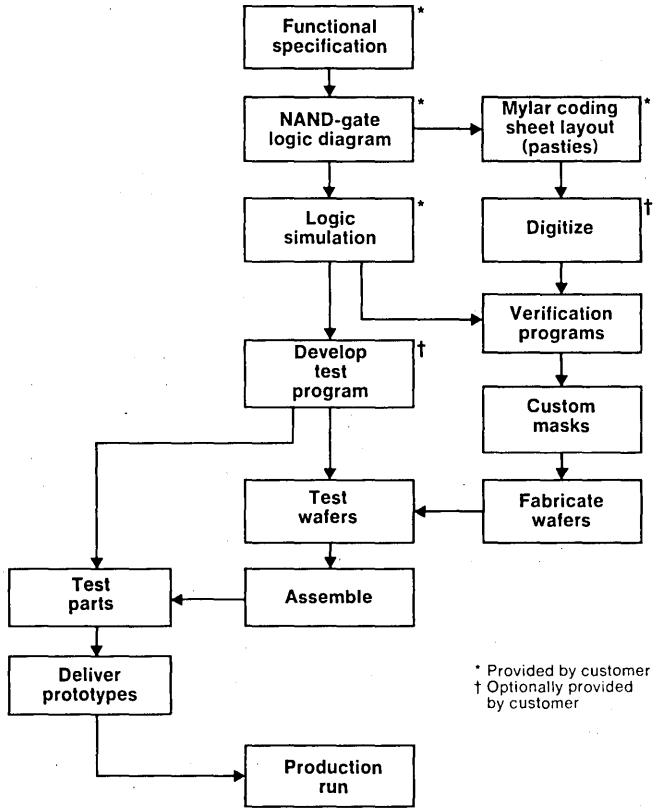
Interconnect design for masterslices can be manual or computer-aided. In all cases, the masterslice approach minimizes design turnaround time. Complex custom-cell library circuits can be obtained in about 18 weeks or less in prototype form; prototypes from gate arrays typically are available in about nine weeks.

One major disadvantage of masterslice circuits has been low circuit density. Circuit and device arrays require channels and alleys for routing interconnects. And because a single pattern must accommodate many different system designs, considerable interconnect routing space can be left unused after the chip is designed. Conversely, in a full custom design, unused space can be minimized. Consequently, a masterslice can be three times larger than an equivalent full-custom chip costing 20% to 60% less.

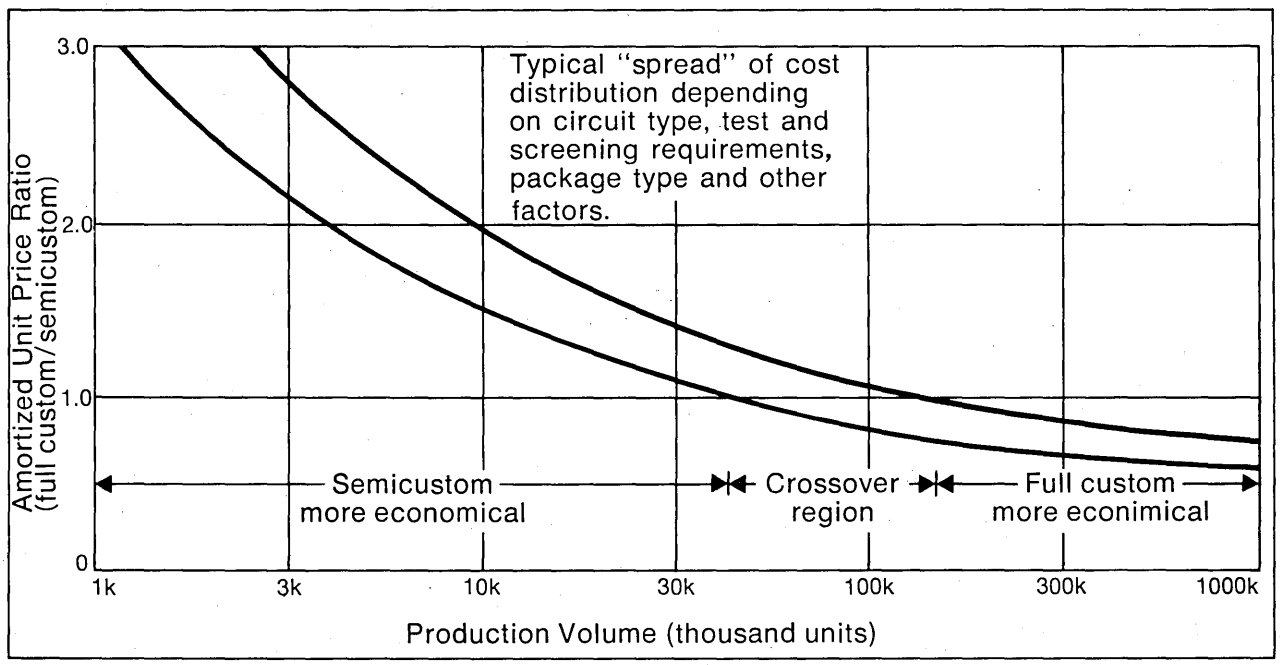
But masterslice manufacturers are increasing circuit densities to bring unit cost closer to that of full-custom circuits purchased in high volume. Circuits with two and three layers of interconnects are being developed to allow more efficient use of chip area. Triple interconnect-level masterslices are already used in a recent generation of IBM computers. So while full-custom designers are reducing design turnaround time, masterslice proponents are reducing unit cost.

Production: IC houses that process custom circuits basically sell a production service, not a design service. Most are concerned first with recovering design costs and then making profit on the volume production of parts. The general rule of thumb calls for total production volume representing at least ten times the supplier's design cost.

Some firms may accept a smaller production volume if engineering costs can be lowered. The customer may satisfy this requirement by using a design specialty firm or the in-house



Developing a custom IC is a multistage process. The degree of user involvement varies between companies. This diagram outlines the development of a custom chip designed from a cell library. Source: Signetics



Production volume influences the choice between full-custom and semicustom parts. However, other considerations (such as design turnaround time) may be overriding factors. Source: Exar

engineering staff. Specialty firms provide services such as design, mask-making, assembly and testing. In many cases a design house controls the evolution of an IC through tooling, fabrication and final delivery.

Selecting a fabrication process based solely on chip cost is not entirely straightforward. For any given process, all wafers cost about the same regardless of circuit complexity. The cost of a chip is determined chiefly by yield, which tends to decrease with chip-area increase. Thus, chip cost varies directly with chip area.

Cost comparison between processes is more complex. Older processes do not necessarily produce higher yields than newer process techniques. And although processes involving more fabrication steps tend to have higher production cost per wafer, a more complex process may also allow circuit designs that produce smaller chips. Similarly, wafers fabricated by newer processes that involve expensive production equipment are usually costly. But, improved processes, although expensive, can produce high yields which tend to lower the die cost. The process must therefore be chosen to get the lowest chip cost consistent with meeting performance requirements.

Packaging: A standard package can cost from a few cents to several dollars. In many custom designs, package cost can be the largest part of unit cost, especially if a custom package is required.

Testing: This cost can be a large portion of the total unit cost. So care must be taken to design the chip for minimum testing requirements. Testing costs depend on the type of test equipment used and the amount of time required to test. Ideally the simplest and most widely available equipment should be used.

Testing cost can range from $50 per hour to several hundred dollars per hour. The manner in which tests are specified can vary test time per part from a few seconds to a minute. It is not economically feasible to test many complex digital circuits for every possible combination of inputs and outputs. And unless complex random logic is designed with testing in mind, it may not be possible to test the final product adequately.

Testing should be considered early in the design phase to minimize cost. Usually it is possible to select a process technology or circuit configuration that eliminates the need for some parametric tests. If timing requirements are critical, for example, using one of the faster process technologies or circuit configurations can eliminate testing speed parameters. Similarly, using a superior process for linear circuits could eliminate the need to test for offset voltages in op-amps.

Terminology

Assembly: Process of mounting a chip into a package and connecting the chip terminal pads to package terminals.

CAD: Computer-aided design. CAD includes computerized equipment that performs circuit simulation, logic simulation, automatic circuit and logic drawing, topological digitizing, topology construction on a CRT terminal, design rule checking and test generation.

Cell: Circuit performing a digital or linear function that is repeatedly used to design an LSI/VLSI chip.

Cell library: Collection of predesigned cell functions stored in a CAD data base. Custom LSI/VLSI devices can be designed by choosing appropriate cells from the library and locating them on a chip to minimize interconnects and maximize performance. The cells are computer characterized for performance much like SSI and MSI ICs with data sheets for each cell.

Custom circuit: In general, a component whose manufacture is under the exclusive control of a customer. The term can refer to full-custom, customized-standard or semicustom parts. In semicustom parts most of the mask layers are common to many customers, and only the final interconnect patterns are special. A customized part is a modification of a standard part to the requirements of a customer. Full-custom parts normally are fabricated from masks configured for the customer.

Design rules: Collection of rules that define minimum dimensions of device topological structures. Design rules also express process-parameter design limits such as gain factor, threshold level, oxide thickness and capacitance.

Die: Rectangular piece of semiconductor material into which electrical circuits have been fabricated. Also called a chip. Plural is dice.

Digitized data base: Recorded digital data representing a topological drawing of an SSI, MSI, LSI or VLSI device. The data include locations and dimensions of rectangles that make up individual circuit elements and interconnects.

Feature size: Dimensions of rectangles, lines and spacings in in an IC topological design.

Gate: Basic digital-logic element producing a binary output depending on the logic state of various inputs.

Gate array: Regular pattern of circuit components on a chip, connected to form regular patterns of gates. The gates are not interconnected until the customer specifies the chip function.

Gate equivalent: Basic unit of measure for digital circuit complexity based on the number of elementary logic gates needed to provide the same circuit function.

LSI: Large-scale integration. Device design integrating from 100 up to thousands of gate equivalents on a chip.

Macrocell array: Regular pattern of grouped, unconnected circuit components. Macrocells are formed into standard logic elements by interconnecting the components to provide specific circuit functions. Interconnects between the cells are specified to perform a specific chip function. The formation of the cell functions and cell interconnects are unique to the customer.

MSI: Medium-scale integration. Device design integrating from 10 to 100 gate equivalents on a chip.

Masterslice: In general, a partially processed chip containing circuit elements for customizing through final metal interconnect patterns. Can refer to gate, device or cell arrays.

Pastie: Scaled decal (usually transparent) representing both function and dimensions of an IC building block such as a gate, flip-flop or I/O buffer. Pasties are a commonly used tool for designing LSI/VLSI chips from a cell library. Each cell type has pastie equivalents.

SSI: Small-scale integration. ICs containing fewer than ten logic-gate equivalents.

Silicon gate: MOS design in which the gate is made of silicon instead of metal. Silicon-gate MOS is faster and more dense than metal-gate MOS.

VLSI: Very-large-scale integration. Device design integrating thousands of gate equivalents on a chip.

Cost: Intense activity in both gate arrays and associated development tools should make the gate-array concept extremely cost competitive with other design approaches. Typical costs for the development of a gate array and a full-custom IC are shown in the accompanying tables.

New gate arrays are currently in widespread development by IC manufacturers; CMOS products with up to 8,000 gates and emitter-coupled-logic (ECL) devices with 100-picosecond gate delays have already been developed. Although most of the attention has been concentrated on CMOS, many bipolar technologies are not being neglected.

Gate arrays are available in a number of bipolar technologies including ECL, Schottky TTL, integrated injection logic, integrated Schottky logic (ISL), and Schottky transistor logic (STL). Gate delays for these devices can be as low as 0.8 nanoseconds. Gate array chips are also available in NMOS and combination CMOS/NMOS versions.

Availability of computer-aided-design (CAD) tools and software support are helping both semicustom and custom products gain acceptance. In some cases, IC suppliers permit customers to use the supplier's in-house CAD facilities. Training courses, running three to five days, are also being offered by many IC manufacturers.

Custom IC cost factors.

Before Process Assembly

- Orders: Issues & Tracking
- Specific Documentation
- Orders: Issues & Tracking
- Purchase Prices
- Cost of Capital
- Inventory: Storage Space/Handling
- Incoming Inspection
- PC Board Space
- Power Consumption

After PC Assembly

- Test: Board
- Failure Diagnostic
- Test Active/Passive Components
- Repair
- Re-Test
- Re-Inventory

Typical costs for the development of a 1000-gate array.

	min.	max.
1. Tooling Development		
A) Circuit Conversion	$500	$1500
B) Layout	$2.5K	$5K
C) Digitization, PG Tape, Masks, 20 prototype units in ceramic DIP, bench tested	$9K	$13K
2. Preproduction		
A) Test Program Development	$4K	$8K
B) Test hardware		
Personality Board	$1K	$2K
Probe Card	$100	$200
Special Supplies, Signal Generator	*	*
Burn-In Board	$500	$2500
Other	*	*
C) Production Qualification Units (Optional)		
Burned-In, Temperature Tested 100 units	3K	$6K
883B Environmental Screening	Extra	
TOTAL	$18K	$40K

* Depends on application

Typical development costs for a full-custom integrated circuit.

		min.	max.
1. Tooling Development			
A) Circuit to LSI Conversion			
B) Layout			
C) Digitization, PG Tape, Masks		$20K	$200K
2. Engineering Evaluations: 5 wafers			
Working Plates	Per Plate	$50	$100
Bipolar: 1-Layer Metal	4-6 weeks	$3K	$6K
2-Layer Metal	6-8 weeks	$5K	$10K
Pt Schottky Diodes - week extra			
CMOS: 1 Poly, 1 Metal	6-8 weeks	$3K	$5K
Same, 4 Micron	6-8 weeks	$4K	$6K
May need several iterations, usually 2 to 4			
3. Prototypes			
A) Establish Waferbank			
30-45 Wafers from Several Runs		$10K	$30K
B) First Look Samples			
100 Untested Dice Packaged in Ceramic Sidebraze		$600	$1500
C) Test Program Development		$5K	$30K
D) Test Hardware			
Personality Board		$1K	$2K
Probe Card		$100	$200
Special Supplies, Signal Generators		*	*
Burn-In Board		$500	$2500
Other		*	*
E) Production Qualification Units (if desired)			
Burned-In, Temperature Tested 100 Units		$3K	$6K
883B Environmental Screening		Extra	
TOTAL		$40K	$280K

* Depends on application

Comparison. The relative ranking of risk factors for alternative design approaches is shown at the right. These ratings will vary depending on the selected suppliers for custom, cell library, gate array or non-LSI devices. Therefore, this chart should be used only as a guide. In the case of linear designs, risks are greater than for digital counterparts. Unless the various circuit blocks assembled from a cell library are compatible with each other from the standpoint of processing, the overall performance of the chip can be less than expected. For instance, the breakdown voltage, beta, sheet resistance, implant dosage, and epi thickness requirements, to say nothing of the starting material, may be mutually exclusive. Also, NPN and PNP transistor configurations cannot both be optimized for performance as is possible with discrete devices.

Comparisons of advantages of various design approaches. A rating of 1 indicates best. (Numbers in parenthesis apply to linear designs.)

	Full Custom	Cell Library	Gate Array	Non-LSI
Design Costs	4(3)	3(4)	2	1
Design Time	4(3)	2(4)	3(2)	1
Mask Costs	4	4	2	1
Redesign Flexibility	4	3	2	1
Test Program Costs	3	3	2	1
Circuit Purchase Price	1	2	3	4
System Power Required	1	2	2	4
Reliability	1	2	2	4
PC Board & Costs	1	2	2	4
Production Labor	1	2	2	4
Security	1	3	2	4
Added Features/ Board	1	3	3	4

CUSTOM CONSIDERATIONS

Benefits provided by custom, related to cost factors, are described in the following paragraphs:

Specification Documentation: Since a single custom IC can replace as many as 100 MSI circuits (plus assorted external active and passive components, such as decoupling capacitors, diodes, and transistors), paperwork needed is greatly reduced.

Purchasing: The purchasing function is not a "free" activity in any company. It costs money to issue purchase orders, and to track them through various delivery dates and procedures with phone calls and computer time. The lower parts count significantly reduce this paper load.

Purchase Price: Depending on the complexity of the chip, the price for a custom device can be lower, at, or above that of all the components to be replaced. It is important to count all of the passive peripheral components involved, such as sockets, resistors, capacitors, inductors, and perhaps even connector pins to the outside.

Cost of Capital: This cost varies with prevailing interest rate. If a company has to borrow development money, usually at about three or four percent over prime rate, then this interest is also an expense incurred by the project. But even if cash is available, there still may be an opportunity cost. This is the income that could have been earned if the cash had been used on short-term projects (such as buying more inventory — provided the sales to turn the inventory over exists).

Inventory: Once the material is in the plant, it has to be handled (including counting, sorting, and paperwork), and stored. Usually, storage space is predefined, and, since it already exists, it is not considered to be an additional expense. However, one has to remember that real estate value on a per-footage basis is substantial and that other departments might make a more cost effective use of any space available. Hence, an additional cost is incurred for each additional component that has to be stored and accounted for. Also, components may become obsolete before the inventory is used up. Custom ICs contribute to decreasing inventory expenses.

Incoming Inspection: Unless pre-aged and pre-screened components are bought to prevent early failures (infant mortality), it is advantageous to inspect active components as they come in. Again, a reduction in the number and variety of devices to be tested adds to profits.

Printed Circuit Board Space: Fewer components mean less space needed to mount them, less auxiliary components, less artwork for interconnect lines, fewer holes to be drilled, and less insertion time and effort — as well as a smaller board.

Power Consumption: The power consumption of the entire system is usually dramatically reduced, making savings possible with lowered power supply and cooling requirements.

CUSTOM/SEMICUSTOM

Manufacturer	Alphatron	American Microsystems, Inc.	California Devices
FOR DETAILED DATA SEE:		(Page 4301)	(Page 4309)
Customized Standard Circuits		Digital, Linear, Combined Digital/Linear	Digital
Gate Array		3μ and 5μ silicon-gate CMOS	Silicon- or metal-gate CMOS
Chip Density Range (equiv. gates)	Up to 4400 2-input gates	300 to 1200 2-input gates (5μ) 500 to 5000 2-input gates (3μ)	50 to 1780 2-input gates
Cell Library	CMOS	Yes	Silicon- or metal-gate CMOS
Design Kit Available	Yes	Yes	Yes
Full Custom Circuits Digital	Silicon- or metal-gate PMOS, NMOS, CMOS	Silicon- or metal-gate PMOS, NMOS, CMOS with high-voltage output capability.	
Linear	Silicon- or metal-gate PMOS, NMOS, CMOS	Silicon-gate NMOS, CMOS, filter, amplifier to rf	Bipolar linear arrays
Combined Digital/Linear	Silicon- or metal-gate PMOS, NMOS, CMOS	Silicon-gate NMOS, CMOS, 14-bit resolution, VHF-rf	
Provide Design Assistance	Yes	Yes - class instruction	Yes
Acceptable Customer Input (in order of preference)	Functional description or block diagram.	Logic diagram, functional specification, data-base tape, PG tape, masks, COT.	Logic diagram with test vectors and PG tape; circuit diagram with data-base tape and composite drawing; breadboard.
Design Aids	Logic simulation, breadboard assistance, design rule checks, decals.	Complete CAD assistance for logic circuit simulation design rule checks, breadboard assistance.	Logic and circuit simulation; breadboard assistance; design rule checks.
Production	In-house and procured	Masks, fabrication and assembly in-house.	In-house and procured
Preferred Delivered Product	Any upon request	DIP, chip carriers, die-on-board packages, wafers, die to commercial or military specifications.	Scribed dice, packaged dice, substrate-mounted device.
Test Program Generation	Yes	Yes, CAD supported	Yes
Production Test	Functional, parametric, burn-in, thermal shock, environmental, MIL.	Functional, parametric, burn-in, thermal shock, environmental, MIL.	Functional, parametric, burn-in, thermal shock, environmental, MIL.
Electrical Test Systems Available	In-house designed, customer-supplied, or outside service.	Sentry, Teradyne, Xincom, LTX, General Radio.	Sentry VII, Sentry Series 20
Comments	Multiple sourcing. Cell library and design rule handbook.	Complete custom capability including design, instruction, CAD and process licensing and technology sales. CAD also available through timesharing and at Design Centers.	Si-gate isolated oxide CMOS has TTL/LSTTL interfacing capability, high-speed performance.

CUSTOM/SEMICUSTOM (cont)

Manufacturer FOR DETAILED DATA SEE:	AWI	Comlinear Corporation	Custom Integrated Circuits
Customized Standard Circuits	Linear, Digital, Combined Digital/Linear	Yes	Digital, Linear, Combined Digital/Linear
Gate Array	Bipolar, CMDS, silicon-gate MOS, hybrids	Linear	I^2L, Linear Master Slice, design on other companies' gate arrays
Chip Density Range (equiv. gates)	10 to 10,000		50 to 8000 (5-input gates)
Cell Library	Over 2600 type		I^2L
Design Kit Available	Yes		
Full Custom Circuits Digital	Yes		I^2L, CMOS, TTL and other bipolar devices
Linear	All processes	Bipolar — FET	Bipolar
Combined Digital/Linear	All processes		I^2L/Linear, TTL/Linear, CMOS/Linear
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Functional schematic, circuit diagram	Functional specification	No preference
Design Aids	Users manual	Computer simulation	Logic simulation, circuit simulation, design rule checks, breadboarding, complete Calma layout system, in-house CAD software, engineering assistance.
Production	In-house robotics and automation	In-house or procured	Procured
Preferred Delivered Product	Printed card mounted, packaged units	Packaged circuit, printed card mounted units	No preference
Test Program Generation	No	Yes	Yes
Production Test	Functional	Functional, burn-in, thermal shock, linear, MIL.	All
Electrical Test Systems Available	Customer supplied	Complete time domain and frequency domain testing from DC to 18 GHz.	HP, MCC
Comments		Specialties include amplifiers with extremely wide bandwidth and fast settling time, fast sample-hold and A to D conversion products.	Total IC development from concept through product delivery. Any subset of the development cycle (design, layout, etc.)

CUSTOM/SEMICUSTOM (cont)

Manufacturer	Cherry Semiconductor	Custom MOS Arrays	Exar Integrated Systems
FOR DETAILED DATA SEE:		(Page 4311)	(Page 4312)
Customized Standard Circuits	Digital, Linear, Combined Digital/Linear	CMOS	Digital, Linear, Combined Digital/Linear
Gate Array	I^2L, LSI^2L, ECL and other bipolar		Metal-gate CMOS; I^2L Si-gate CMOS
Chip Density Range (equiv. gates)	64 to 150 gates/mm²	448 to 1568 (2 inputs)	100 to 1250
Cell Library	I^2L, LSI^2L, ECL and other bipolar	Yes	Metal-gate CMOS; I^2L Si-gate CMOS
Design Kit Available	Yes		Yes
Full Custom Circuits Digital	I^2L, LSI^2L, ECL and other bipolar		Metal-gate CMOS; I^2L Si-gate CMOS
Linear	I^2L, LSI^2L, ECL and other bipolar		No
Combined Digital/Linear	I^2L, LSI^2L, ECL and other bipolar		I^2L, other bipolar
Provide Design Assistance	Yes		Yes
Acceptable Customer Input (in order of preference)	Customer-owned tooling; circuit diagram; logic diagram; breadboard.		Complete layout, breadboard, circuit diagram, logic diagram, functional diagram.
Design Aids	Logic simulation; breadboard assistance; design rule checks.		Logic simulation; breadboard assistance; design rule checks.
Production	In-house		In-house
Preferred Delivered Product	Packaged dice; flip chips		Probed wafers, scribed dice, packaged dice.
Test Program Generation	Yes		Yes
Production Test	All except military		Functional, parametric, environmental, burn-in
Electrical Test Systems Available	Teradyne 1259, A310, A311		Sentry; Fairchild 5000, Teradyne J273, A311; Amdahl
Comments	Dice can be solder-bump flip chips with nitride passivation; packaged dice can be delivered from COT for full custom.		

CUSTOM/SEMICUSTOM (cont)

Manufacturer	Fairchild	Ferranti	Fujitsu
FOR DETAILED DATA SEE:	**(Page 4316)**		**(Page 4318)**
Customized Standard Circuits	Digital	Digital, Combined Digital/Linear	Digital
Gate Array	Bipolar ECL	CDI RTL, CML, buffered CML	Silicon-gate CMOS, LSTTL, LSI^2L
Chip Density Range (equiv. gates)	20 to 1000 3-Input NAND	100 to 10,000*	208 to 2108 3-Input NAND
Cell Library		Yes	Silicon-gate CMOS, LSTTL, LSI^2L
Design Kit Available		Yes	Yes
Full Custom Circuits Digital		CDI	Silicon-gate CMOS, LSTTL, LSI^2L
Linear			
Combined Digital/Linear		CDI	
Provide Design Assistance		Yes	Yes
Acceptable Customer Input (in order of preference)		No Preference	Logic diagram and test timing data (Fujitsu format).
Design Aids	Logic simulation, breadboard assistance, design rule checks.	Computer simulation, design rule checks, layout check, test program verification. Remote CAD system. Breadport parts.	Logic simulation, design rule checks; complete CAD system.
Production	In-house	In-house	In-house
Preferred Delivered Product		Packaged dice	Packaged dice
Test Program Generation		Yes	Automatic
Production Test		All	Parametric, functional
Electrical Test Systems Available	FARCAD	Membrain, Genrad, Teradyne, LTX, Tektronix	
Comments	Remote access to FARCAD via telephone link	ULA designer; low cost, remote interactive CAD system available for on-site use. * Over 50 array types available.	Dual-layer metal; CAD system verifies design; auto placement and routing from customer's diagram.

CUSTOM/SEMICUSTOM (cont)

Manufacturer	GTE Microcircuits	Holt	Hycom
FOR DETAILED DATA SEE:		(Page 4431)	
Customized Standard Circuits		Digital, Linear, Combined Digital/Linear	
Gate Array	ISO-CMOS	Silicon or metal-gate CMOS, bipolar	
Chip Density Range (equiv. gates)	504 — 2500	98 to 1500*	
Cell Library	ISO-CMOS	Silicon and metal-gate CMOS	
Design Kit Available	Yes	Yes	
Full Custom Circuits Digital	ISO-CMOS	Silicon and metal-gate CMOS, bipolar	Silicon- or metal-gate PMOS, NMOS, or CMOS
Linear	ISO-CMOS	Silicon and metal-gate CMOS, bipolar	
Combined Digital/Linear	ISO-CMOS	Silicon and metal-gate CMOS, bipolar	
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Calma tapes, PG tapes, masks	Functional specification; logic diagram; circuit diagram, breadboard, PG tape, pencil-interconnected layout.	Functional specification; logic diagram; circuit diagram.
Design Aids	Design rule checks, Logic simulation	Logic simulation, breadboard assistance; design rule checks; CAD, breadboard parts, evaluation parts.	Circuit simulation; logic simulation.
Production	In-house	Procured	Procured
Preferred Delivered Product	Packaged die, probed wafers, mapped wafers	Probed wafers; scribed dice; packaged dice; substrate-mounted dice; p-c card-mounted packages.	No preference
Test Program Generation	Yes	Yes	Yes
Production Test	Functional, parametric, burn-in	Functional; parametric; burn-in, thermal shock, environmental, MIL.	Functional, burn-in
Electrical Test Systems Available	Sentry LTX, H.P., Mega, XINCOM	Imperial Technology IT-200; custom testers.	In-house designed
Comments		Specializing in low-voltage circuitry, CMOS analog circuitry design. *Equivalent gates are 2-input NAND/NOR.	Services: design, layout, testing. Service industry used for photomasks, fabrication, and assembly.

CUSTOM/SEMICUSTOM (cont)

Manufacturer FOR DETAILED DATA SEE:	Integrated Circuit Engineering	Integrated Circuit Systems	Integrated Technology Corporation
Customized Standard Circuits	Linear, Digital, Combined Digital/Linear	Digital, Linear, Combined Digital/Linear	
Gate Array			
Chip Density Range (equiv. gates)			
Cell Library		All MOS processes	
Design Kit Available	No		
Full Custom Circuits Digital	Silicon- or metal-gate PMOS, NMOS, CMOS; TTL, STTL, I^2L	MOS	Silicon- or metal-gate MOS; TTL, STTL, LSTTL, I^2L, ECL, other bipoar
Linear	Silicon- or metal-gate CMOS; TTL, STTL	MOS	Silicon- or metal-gate CMOS; bipolar
Combined Digital/Linear	Silicon- or metal-gate CMOS; TTL, STTL	MOS	Silicon- or metal-gate CMOS; bipolar
Provide Design Assistance	Yes	For full custom	
Acceptable Customer Input (in order of preference)	Functional specification; logic diagram; circuit diagram; breadboard; known good device; customer owned tooling; test vectors.	For full custom: Functional specification; logic diagram; breadboard.	
Design Aids	Logic simulation; breadboard assistance; design rule checks; graphics CAD.	Logic simulation; circuit simulation; breadboard assistance.	Logic simulation; breadboard assistance; design rule checks; transient analysis.
Production	Procured	Procured	Procured
Preferred Delivered Product	Packaged dice		Mapped wafers; probed wafers; packaged dice; PC-mounted packaged units; design tooling; complete systems.
Test Program Generation	No	Megatest Q8000	Yes
Production Test	No		Functional; parametric
Electrical Test Systems Available			Siemens
Comments		Services: Design, layout, chip/PCB artwork, test generation, product engineering.	Services: Design, tooling for custom ICs; service industry used for photomasks, wafer fab, assembly, some testing. System design and production with custom IC's.

CUSTOM/SEMICUSTOM (cont)

Manufacturer	Interdesign	International Microcircuits	International Microelectronic Products
FOR DETAILED DATA SEE:	(Page 4433)		(Page 4435)
Customized Standard Circuits	Digital, Linear, Combined Digital/Linear	Digital	Digital, Combined Linear/Digital
Gate Array	CDI RTL and CML, metal-gate CMOS, silicon-gate NMOS; bipolar	Silicon- or metal-gate CMOS	No
Chip Density Range (equiv. gates)	See Comments	50 to 5000	200 to 10,000
Cell Library	For all except linear bipolar	Yes	Silicon-gate CMOS
Design Kit Available	Yes	Yes	Yes
Full Custom Circuits Digital	Silicon-gate NMOS; metal-gate CMOS		Silicon-gate NMOS and CMOS
Linear	Bipolar		
Combined Digital/Linear	Some linear functions		Silicon-gate NMOS and CMOS
Provide Design Assistance	Yes		Yes
Acceptable Customer Input (in order of preference)	Pencil-connected layout: logic diagram; specification; PG tapes; circuit diagram and breadboard (for linear bipolar); reticles.		Functional specification, logic diagram, circuit diagram, breadboard, test vectors, customer-owned tooling (pattern-generator tape, composite drawing), known good device.
Design Aids	Computer simulation; breadboard parts; layout sheets; functional overlays; evaluation parts.		Logic simulation, breadboard assistance, design rule checks, engineering assistance.
Production	Metallized wafers procured; other functions in-house.	In-house and procured	In-house
Preferred Delivered Product	Packaged dice, bare dice, probed wafers.	Scribed dice; packaged dice	Mapped wafers, probed wafers, scribed dice, packaged dice, or special packages.
Test Program Generation	Yes	Yes	Yes
Production Test	Functional; parametric; burn-in; MIL 883B; environmental.	Functional, parametric, burn-in, thermal shock, environmental, MIL.	Functional, parametric, burn-in
Electrical Test Systems Available	Teradyne J325; LTX CP/TS70; LOMAC LM325; Fairchild 5000; LOMAC LM25; custom tester.	GenRad, Sentry	Sentry 20, Kiethley
Comments	CDI RTL: 255 logic cells; CDI CML: 450-880 2-input NOR; Metal-gate CMOS: 112-420 2/3-input; Silicon-gate NMOS: 224 4-input NOR; Lnear bipolar: 11-812 components.		

CUSTOM/SEMICUSTOM (cont)

Manufacturer	LSI Computer Systems	LSI Logic	Master Logic
FOR DETAILED DATA SEE:	(Page 4436)		
Customized Standard Circuits		Digital	Digital
Gate Array		Silicon-gate CMOS, HCMOS and ECL	Silicon- or metal-gate CMOS
Chip Density Range (equiv. gates)		300 to 10,000	500 to 1000, silicon-gate 50 to 600, metal-gate
Cell Library		7400/4000 CMOS & HCMOS; ECL10K — SSI/MSI functions	In manual
Design Kit Available		Yes	Yes
Full Custom Circuits Digital	Metal-gate PMOS, CMOS	No	Silicon- or metal-gate CMOS
Linear	Metal-gate PMOS, CMOS		
Combined Digital/Linear	Metal-gate PMOS, CMOS		Yes
Provide Design Assistance	Yes		Yes
Acceptable Customer Input (in order of preference)	Logic diagram; customer-owned tooling (pattern-generation tape, composite drawing); circuit diagram; breadboard; functional specification.		Any
Design Aids	Design rule checks, computer-aided transient analysis.	LSI Design System (LDS), including design entry, circuit simulation, logic simulation, PG and test tape generation via remote terminal or factory based.	Manual
Production	Procured	In-house	Procured
Preferred Delivered Product	Packaged dice	Packaged dice	Any
Test Program Generation	Yes	Yes	No
Production Test	Functional, parametric, burn-in; thermal shock, environmental; MIL.	Functional, parametric to MIL 883B.	Procured
Electrical Test Systems Available	Macrodata 107 and customized equipment.	Industry Standard Tester	
Comments	Multiple-sourced production	Multiple sourced	Multiple sourced

CUSTOM/SEMICUSTOM (cont)

Manufacturer	Micro-Circuit Engineering	Microcircuits Technology, Inc.	Micro Innovators
FOR DETAILED DATA SEE:	(Page 4437)		
Customized Standard Circuits	Linear, Digital, Combined Linear/Digital, Bipolar, CMOS	Digital, Linear, Digital/Linear	Digital
Gate Array	CMOS, ECL, Dielectric Isolation, I^2L, Linear	Linear bipolar, metal gate NMOS, CMOS; silicon gate CMOS	
Chip Density Range (equiv. gates)	50 to 10,000 gates	250 to 6000 gates	50 to 250 mil^2
Cell Library	Yes	Silicon gate or metal gate NMOS, CMOS, linear bipolar	
Design Kit Available	Yes	No	No
Full Custom Circuits Digital	CMOS, TTL, LSTTL, I^2L, ECL, Linear	Silicon gate CMOS, Metal Gate CMOS	Silicon- or metal-gate PMOS, NMOS, CMOS, other MOS
Linear	Up to 75 Volt	Bipolar, CMOS	Silicon- or metal-gate PMOS, NMOS, CMOS, other MOS
Combined Digital/Linear	Up to 20 Volt	CMOS and bipolar	Silicon- or metal-gate PMOS, NMOS, CMOS, other MOS
Provide Design Assistance	Yes	Yes	
Acceptable Customer Input (in order of preference)	MCE will interface with customer anywhere in design sequence. UniDES; software.	Logic diagram, breadboard, block diagram, functional specifications.	Functional specification; logic diagram; circuit diagram; breadboard; test vectors; customer-owned tooling.
Design Aids	Logic simulation; breadboard assistance; design rule checks; UNIDES.	Calma CAD, logic simulation, circuit simulation.	Logic simulation; breadboard assistance; design rule checks.
Production	In-house manufacturing; 4" Wafer Fab	In-house, procured	In-house
Preferred Delivered Product	Mapped wafers; probed wafers; scribed dice; substrate-mounted dice; packaged dice; custom packaging.	Packaged units	Probed wafers; packaged dice
Test Program Generation	Yes	Yes	Yes
Production Test	Functional; parametric	Functional, parametric, burn-in, environmental, MIL, linear	Functional; parametric; burn-in
Electrical Test Systems Available	Teradyn J273 and A300 with laser trim; Pragmatic Inspector 200 (72 pin digital IC); Kiethley 300.	Fairchild Sentry	Sentry, Teradyne, Comparator
Comments	Functional arrays available CMOS MGA and SGA series; also linear function cells.	MOS: 3 and 5 micron channel lengths.	Tooling can be used by at least two MOS wafer manufacturers to ensure alternate sourcing.

CUSTOM/SEMICUSTOM (cont)

Manufacturer FOR DETAILED DATA SEE:	Micro Power Systems	Micro-Sciences	Monosil
Customized Standard Circuits		Digital	Digital
Gate Array		CMOS	CMOS
Chip Density Range (equiv. gates)		300 to 1260	50 to 600
Cell Library	Mily-gate CMOS, bipolar LSI, thin film on silicon	CMOS	Metal-gate CMOS
Design Kit Available	No	No	Yes
Full Custom Circuits Digital	Low-voltage, poly-gate CMOS	Silicon- or metal-gate PMOS, NMOS, CMOS	Silicon- or metal-gate PMOS, NMOS, CMOS; bipolar, I^2L
Linear	High-gain/low current analog bipolar; thin-film resistor		Bipolar
Combined Digital/Linear	Bipolar and CMOS		CMOS
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Circuit/logic diagram; breadboard; functional specifications; customer-owned tooling.	Logic diagram; circuit diagram; functional specification; breadboard; customer-owned tooling; known good device.	Logic diagram; circuit diagram; functional specification; breadboard.
Design Aids	Breadboard assistance; cooperative design from logic/circuit diagrams.	Logic simulation; breadboard assistance.	Design rule checks
Production	In-house	Procured	In-house
Preferred Delivered Product	Custom packaging; all standard configurations except mapped wafers.	Packaged dice	Scribed dice; packaged dice; substrate-mounted dice; PC-mounted packaged units.
Test Program Generation	Yes	Yes	Yes
Production Test	All	Functional; parametric; burn-in	Functional parametric; burn-in
Electrical Test Systems Available	Fairchild, Datatron, Macrodata, custom.		Dedicated, J193 Acutest, Sentry
Comments		Chip debugging with portable micro prober on customer's premises.	CMOS and PMOS 4-bit microprocessor available for custom tailoring. (See Microprocessor section).

CUSTOM/SEMICUSTOM (cont)

Manufacturer	Motorola	Motorola	Murray Consulting
FOR DETAILED DATA SEE:	(Page 4479)	(Page 4479)	
Customized Standard Circuits	Digital	Digital	Linear, Digital, Combined Linear/Digital
Gate Array	MCA 600 ECL/1200 ECL	MCA 500 ALS/1300 ALS	CMOS
Chip Density Range (equiv. gates)	652/1192	533/1280	1 to 100
Cell Library	120 functions	80 functions	BiMOS
Design Kit Available	Manuals	Manuals	No
Full Custom Circuits Digital	NMOS, CMOS, ECL	NMOS, CMOS, ECL	Silicon-gate CMOS; TTL
Linear	No	No	
Combined Digital/Linear	No	No	Silicon-gate CMOS; bipolar
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	CAD interface, logic simulation, circuit documentation.	CAD interface, logic simulation, circuit description.	Breadboard; circuit diagram; functional specification.
Design Aids	Computer aided design package	Computer aided design package	Design rule checks
Production	High volume capability	High volume capability	In-house, procured
Preferred Delivered Product	Choice of packages	Choice of packages	Packaged dice; PC-mounted packaged units.
Test Program Generation	Yes	Yes	No
Production Test	100% AC and DC and functional	100% AC and DC and functional	Functional
Electrical Test Systems Available	Fairchild Sentry VIII and Series 21	Fairchild Sentry VIII and Series 21	
Comments	ECL 10K compatible, ECL 10 KH compatible, remote design centers available.	TTL-LS compatible, remote design centers.	Develop photo-integrated circuits: CMOS, MOS, bipolar, BiMOS.

CUSTOM/SEMICUSTOM (cont)

Manufacturer	National	Nitron	I. S. Oscar Associates, Inc.
FOR DETAILED DATA SEE:	(Page 4481)		
Customized Standard Circuits	Digital	Digital	Digital, standard cell
Gate Array	Silicon-gate CMOS	Metal-gate CMOS	None
Chip Density Range (equiv. gates)	To 2400	50 to 600	500-2500 2-input NAND/NOR
Cell Library	Yes	Macro library of common functions (overlays)	CMOS, NMOS
Design Kit Available	Yes	Yes	Yes
Full Custom Circuits Digital	Metal-gate PMOS, metal-or Silicon-gate NMOS, high voltage metal-gate CMOS, low voltage metal- and silicon-gate CMOS, metal double poly silicon-gate CMOS, dual layer XMOS, oxide isolated and Schottky devices, I^2L.	Metal-gate PMOS, CMOS	Silicon or metal gate CMOS and NMOS
Linear	Same as above	Metal-gate PMOS, CMOS	None
Combined Digital/Linear	Same as above	Metal-gate PMOS, CMOS	Some linear functions
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Any	Customer-owned tooling with debugged test program; logic diagram, electrical specification with test vectors.	Functional specifications, block diagram, logic diagram
Design Aids	Computer aided circuit analysis, logic and systems simulation, digitizing cell plotting and editing, design rule check, pattern generation, photolithography.	All available	In-house CAE system provides: silicon compiler for data paths, PLAs and random logic; functional simulator to verify timing requirements; circuit extractor and design rule checker for layout verification.
Production	In-house	In-house	Procured
Preferred Delivered Product	Packaged dice	Packaged dice	Packaged prototype dice and mask set; packaged dice; scribed dice; tested wafers.
Test Program Generation	Yes	Yes	Yes, with fault simulation
Production Test	All except linear	All commercial and full military	Functional, parametric, burn-in
Electrical Test Systems Available	Century VI and VII, Sentinel, Teradyne, Megatest.	Sentry	Sentry VII; Isolab-C
Comments			Complete design service emphasizing fast-turnaround for full custom designs. Unique CAE design tools provide the capability to design full-custom ICs at costs competitive with gate arrays.

CUSTOM/SEMICUSTOM (cont)

Manufacturer	Pico Design	Plessey Semiconductors	Polycore Electronics Inc.
FOR DETAILED DATA SEE:		(Page 4501)	
Customized Standard Circuits		Digital, Linear, Combined Digital/Linear	
Gate Array		ECL and ISO CMOS	
Chip Density Range (equiv. gates)		ECL to 1K, CMOS to 2K	
Cell Library		NMOS and CMOS to 2K Gates	
Design Kit Available		No	
Full Custom Circuits Digital	Silicon- or metal-gate PMOS, NMOS, CMOS, other MOS.	PMOS, NMOS, CMOS; I^2L, ECL	
Linear		CMOS, I^2L, ECL; other bipolar	Bipolar
Combined Digital/Linear		CMOS, I^2L, ECL	Power Interface/Driver Circuits
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Logic diagram, circuit schematic, breadboard, functional specification.	Logic diagram, breadboard, customer-owned tooling, data base tape.	Schematics, Performance specs.
Design Aids	Logic and circuit simulation; design rule checks; other.	Logic simulation, design rule check	Breadboard simulation
Production	Procured	In-house	In-house wafer fabrication procurred assembly
Preferred Delivered Product	All except PC-mounted packaged units.	Packaged tested dice, scribed dice, probed wafers, mapped wafers.	Packaged units, dice
Test Program Generation	Yes	Yes	Yes
Production Test	Functional; parametric	Functional, parametric, burn-in, MIL-STD-883.	Functional, parametric, burn-in; thermal shock, environmental, MIL.
Electrical Test Systems Available	Sentry VII	Teradyne J274, Fairchild, Sentry special in-house.	MCT 200
Comments			Also provide silicon foundry service in linear, I^2L and CMOS metal gate.

CUSTOM/SEMICUSTOM (cont)

Manufacturer	Precision Monolithics, Inc.	Raytheon	RCA
FOR DETAILED DATA SEE:			(Page 4517)
Customized Standard Circuits	Linear	Linear, Digital	Digital
Gate Array	From customer-owned tooling	Silicon-gate TTL, ISL	Silicon-gate, metal-gate CMOS
Chip Density Range (equiv. gates)		300 to 2000	168 to 840
Cell Library	Standard parts available in chip form	Yes, TTL	CMOS
Design Kit Available	Kit parts	No	No
Full Custom Circuits Digital	TTL, LSTTL, ISL, I^2L, ECL, ISO/CMOS-SiGate	TTL	Silicon-gate, metal-gate CMOS
Linear	20, 40, 60V supply voltage	Bipolar	
Combined Digital/Linear	I^2L, ECL, TTL, LSTTL		
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Customer-owned tooling (pattern-generator tape, composite drawing), known good device.		
Design Aids	Kit parts		Logic simulation; breadboard assistance; design rule checks.
Production	In-house 3″, 4″ lines		In-house
Preferred Delivered Product	Mapped wafers, probed wafers, packaged units.		Probed wafers, scribed dice, packaged dice.
Test Program Generation	Yes	Yes	Yes
Production Test	Functional, parametric, burn-in, thermal shock, environmental, MIL, linear.		Functional, parametric, burn-in
Electrical Test Systems Available	LTX, F-5000		Teradyne; Century 7; J273, J193, J283, J325; LTX; Tester; MTS 77.
Comments	Ion implantation; dual layer metallization; nitride passivation; thin film resistors; MIL 38510 qualified.		

CUSTOM/SEMICUSTOM (cont)

Manufacturer	Semi Process Inc.	Signetics	Signetics
FOR DETAILED DATA SEE:		(Page 4522)	
Customized Standard Circuits	Digital	Digital	Digital
Gate Array	Silicon-gate CMOS	See below "Full custom"	ECL 100K and 10 K compatibility (0.5 ns)
Chip Density Range (equiv. gates)	80 to 1000	300-1000	500-800
Cell Library	Yes	SSI, pre-characterized macros	Macrocell Library
Design Kit Available	Yes	Yes	Yes
Full Custom Circuits Digital		Composite Cell Logic, a standard cell approach made up of two libraries. Integrated Schottky Logic (4 ns typical) and extended performance library (3 ns typical).	
Linear			
Combined Digital/Linear			
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Logic diagram; circuit diagram; test vectors; custom-owned tooling; breadboard; functional specification.	Logic diagram plus simulation results; Calma tape plus simulation results; Mylar symbolic representation plus simulation results.	Calma tapes plus simulation results; Mylar symbolic representation plus simulation results.
Design Aids	Design rule checks, logic simulation, circuit simulation	Logic simulation, design rule checks, layout to simulation check, generate Sentry test tape.	Logic simulation, CAD design rule checks, layout to simulation check, test generation, design manual, training sessions.
Production	In-house	In-house	In-house
Preferred Delivered Product	As requested	Packaged units	Packaged units
Test Program Generation	Yes	Yes	Yes
Production Test	Functional; parametric; burn-in A.C.	Functional, parametric and AC burn-in option. Full MIL available.	Functional parametric and AC
Electrical Test Systems Available	Sentry, Genrad, Pragmatic	Sentry VII and VIII	Tektronix (25 MHz)
Comments	Breadboard assistance using SPI's proprietary 74HC low power CMOS logic IC's.	Design manual — 1 day workshop (in customer facilities) and 4 day training in our facilities.	

CUSTOM/SEMICUSTOM (cont)

Manufacturer	Signetics	Signetics	Silicon Systems
FOR DETAILED DATA SEE:	(Page 4522)	(Page 4522)	(Page 4528)
Customized Standard Circuits	Digital	Digital	
Gate Array	Silicon-gate CMOS	ACE; 600-2200 gates 8A; 1200-2100 gates	
Chip Density Range (equiv. gates)	330-1700	See above	
Cell Library	Silicon-gate CMOS — some T^2L		
Design Kit Available	Yes		
Full Custom Circuits Digital	No		Silicon- or metal-gate PMOS, NMOS, CMOS, Bipolar, TTL, STL, SRTL, LSTTL, ECL, I^2L.
Linear			Silicon- or metal-gate PMOS, NMOS, CMOS, Bipolar.
Combined Digital/Linear			Silicon- or metal-gate CMOS, Bipolar, TTL, SRTL, I^2L, STL.
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Logic diagram plus simulation	Computer simulation	Functional specification, logic diagram, circuit diagram, breadboard, test vectors.
Design Aids	Complete simulation, auto route, auto test generation.	Design manual; seminars	Breadboards, logic and circuit stimulation, design-rule checks, test-program development.
Production	In-house	In-house	Procured and in-house
Preferred Delivered Product	Packaged units	Packaged units	Packaged units and tested dice
Test Program Generation	yes	Yes	Yes
Production Test	Functional parametric burn-in	Sentry VII	Automatic testers for analog and digital devices.
Electrical Test Systems Available	Sentry VII and VIII		
Comments	Design manual and workshop in preparation		Water fabrication for COT available for CMOS first quarter 1982; bipolar, third quarter 1982.

CUSTOM/SEMICUSTOM (cont)

Manufacturer	Siltronics	Solid State Scientific	Sprague Electric Co.
FOR DETAILED DATA SEE:			
Customized Standard Circuits			Linear
Gate Array			
Chip Density Range (equiv. gates)			
Cell Library			
Design Kit Available			No
Full Custom Circuits Digital	TTL, STTL, LSTTL, I^2L, ECL, other bipolar	Silicon-gate CMOS, NMOS metal-gate CMOS	
Linear	TTL, STTL, LSTTL, I^2L, ECL, other bipolar	Silicon-gate CMOS, NMOS	
Combined Digital/Linear	TTL, STTL, LSTTL, I^2L, ECL, other bipolar	Silicon-gate NMOS, CMOS	
Provide Design Assistance		Yes	
Acceptable Customer Input (in order of preference)		Minimum of functional diagram; breadboard; pattern generator tape or database tape.	Composite drawing
Design Aids	Breadboard assistance; design-rule checks.	Logic simulator assistance, breadboard assistance, design rule checks.	
Production	Breadboard wafers; in-house assembly.	In-house	In-house
Preferred Delivered Product	Fully tested assembled package.	No preference	Wafers, dice, packaged devices
Test Program Generation	Yes	Yes	
Production Test	Customized to suit	Full screening available including burn-in and full environmental screening.	
Electrical Test Systems Available	J259-style equipment; custom testers.	Sentry VII, Sentinal, Teradyne	
Comments	Specialize in mixed analog/ digital bipolar. Die sizes to 20,000 mil^2.	Capabilities include: design, layout, CAP, mask shop, wafer fabrication assembly, and test.	ULN-2350C and ULN-2351C basic unmetallized circuit.

CUSTOM/SEMICUSTOM (cont)

Manufacturer FOR DETAILED DATA SEE:	Standard Microsystems	Sunshine Semiconductor	Supertex
Customized Standard Circuits	Digital, Combined Digital/Linear	Digital, Combined Linear/Digital	Linear, Digital
Gate Array			Silicon- or metal-gate CMOS
Chip Density Range (equiv. gates)			50 to 2000
Cell Library	Silicon-gate NMOS, CMOS		
Design Kit Available	No		No
Full Custom Circuits Digital	Metal-gate PMOS; silicon-gate NMOS, CMOS	Silicon-gate CMOS, metal-gate CMOS, NMOS, nonvolatile CMOS	Silicon- or metal-gate CMOS
Linear			Silicon- or metal-gate CMOS
Combined Digital/Linear	Silicon-gate NMOS, CMOS	Metal Gate CMOS	Silicon- or metal-gate CMOS
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Functional specification, logic diagram, Calma database tape, other.	Product description, block diagram with specifications, logic diagram.	Breadboard with functional specification and logic diagram; customer-owned tooling.
Design Aids	Logic simulation; breadboard design rule checks, electrical rule checks, transient analysis	Breadboard, circuit and logic simulation, DRC, graphics, NCC	Logic simulation; breadboard assistance.
Production	In-house	Procured	In-house
Preferred Delivered Product	Packaged devices preferred. All others available.	Packaged dice, bare dice, design and layout	Probed wafers; inspected dice; packaged dice.
Test Program Generation	Yes	Yes	Yes
Production Test	Full testing and screening, including burn-in.	Procured	Functional; parametric; burn-in; environmental.
Electrical Test Systems Available	Megatest Q8000; SMC; dedicated testers, Fairchild, Sentry and Sentinal.		Teradyne J193; GenRad 2225
Comments	Specialize in digital MOS/LSI and VLSI; will also customize by modifying MOS/LSI standard parts. Second sources available.	Services include product and specification finalization, logic and circuit design, layout, test definition.	

CUSTOM/SEMICUSTOM (cont)

Manufacturer	Synertek	Telephonics LSI	Telmos
FOR DETAILED DATA SEE:	(Page 4531)		
Customized Standard Circuits			Digital
Gate Array		Silicon-gate CMOS, NMOS	Silicon-gate and metal-gate CMOS
Chip Density Range (equiv. gates)		300 to 1260	50 to 1260 gates
Cell Library		Silicon-gate CMOS, NMOS	Silicon-gate and metal-gate CMOS digital
Design Kit Available	Yes	No	
Full Custom Circuits Digital	Silicon-gate CMOS, NMOS	CMOS, NMOS, PMOS	Custom designs are performed
Linear	Same as above	CMOS, NMOS, PMOS	
Combined Digital/Linear	Same as above	CMOS, NMOS, PMOS	Silicon-gate analog/digital
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Functional specification, customer owned tooling, logic diagram, circuit diagram, breadboard.	Specification, logic diagram, circuit diagram, system requirements, breadboard, test vectors, customer-owned tooling.	Schmatic I/O requirements, functional spec. breadboard, test vectors, customer owned tooling, known good device.
Design Aids	Logic simulation breadboard assistance, continuity check, design rule check.	Custom cell library, logic simulation, breadboard, design rule checks.	Aspec, Spice IIG — transient analysis logic, Tegas IV — logic simulation, Sentry VII — test.
Production	In-house	Procured	In-house wafer fab facility
Preferred Delivered Product	Packaged dice, scribed dice	Packaged dice, dice	Wafer, dual in line packages, chip carriers.
Test Program Generation	Yes	Yes	Yes
Production Test	All	Functional, parametric, burn-in, linear.	Functional, parametric burn-in thermal shock, environmental.
Electrical Test Systems Available	Century, Xincom	Dedicated, HP, Fairchild series 10, Gen Rad.	
Comments	Customer interface ranges from "black box" specification to COT. Company will work with customer engineers to develop in-house capability for designing future COT.	More than one source available. No minimum production requirement. All design services: layout, digitizing, test generation, assembly, plotting, etc.	

CUSTOM/SEMICUSTOM (cont)

Manufacturer FOR DETAILED DATA SEE:	Telmos	Texas Instruments	Topanga Data Systems
Customized Standard Circuits	Digital/Linear	Digital	
Gate Array	Silicon-gate analog/digital Silicon-gate high voltage	LPS, silicon-gate CMOS, STL	
Chip Density Range (equiv. gates)		540 to 4000	
Cell Library	100 to 1200 gates	Software functions — bipolar CMOS MACROS	
Design Kit Available	Yes	Yes	No
Full Custom Circuits Digital		LPS, STL, I^2L, CMOS, NMOS	Silicon- or metal-gate PMOS, NMOS, CMOS
Linear		Yes	
Combined Digital/Linear	Silicon-gate analog/digital	Yes	
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Schematic I/O requirements, functional spec. breadboard, test vectors, customer owned tooling, known good device.	Logic diagram, PG tape, HDL/TDL design input, functional specification.	
Design Aids	Aspec, Spice IIG — transient analysis logic, Tegas IV — logic simulation, Sentry VII — test.	Simulaion, testability analysis, test grading, load checker. Texas Instruments logic array design utility — TILADS.	Logic simulation; breadboard assistance; design rule checks; CAD; design verification.
Production	In-house wafer fab facility	In-house	
Preferred Delivered Product	Wafer, dual in line packages, chip carriers.	Packaged devices	
Test Program Generation	Yes	Yes	No
Production Test	Functional, parametric burn-in thermal shock, environmental.	Functional, parametric, burn-in, MIL.	
Electrical Test Systems Available		Sentry 20, in-house	
Comments			

CUSTOM/SEMICUSTOM (cont)

Manufacturer	Universal Semiconductor	VLSI Technology	Western Digital
FOR DETAILED DATA SEE:		(Page 4561)	(Page 4563)
Customized Standard Circuits	Digital		Digital
Gate Array	Silicon-gate ISO-CMOS		Up to 1000 gates, Silicon-gate NMOS
Chip Density Range (equiv. gates)	360 to 1800		
Cell Library	Silicon-gate ISO-CMOS		
Design Kit Available	Yes		Yes
Full Custom Circuits Digital	Silicon-gate ISO-CMOS	NMOS, HMOS, CMOS	
Linear	Same as above	NMOS, CMOS	
Combined Digital/Linear	Same as above	NMOS, CMOS	
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)	Customer-owned tooling, logic diagram, circuit diagram, functional specification, breadboard.	Functional specification, logic diagram, breadboard, customer-owned tooling — data-base tape, PG tape, mask.	Functional specification logic system
Design Aids	Logic simulation, breadboard assistance, design rule checks.	PRISM VLSI design system, including high-level design language, circuit extraction, logic and circuit simulation, design-rule checks, plotting, STIX.	Logic simulation, design rule checks, test program development.
Production	In-house	In-house	In-house
Preferred Delivered Product	Mapped wafers, probed wafers, scribed dice, packaged parts.	Packaged dice preferred. Any on request.	Packaged units and tested dice
Test Program Generation	Yes	Yes	Yes
Production Test	Functional, parametric, burn-in, thermal shock, environmental, MIL.	Functional, parametric, burn-in, thermal shock, environmental, MIL.	Functional, burn-in
Electrical Test Systems Available	Micro Manipulator, Sentry II, VI, VII, Sentry System 20, pragmatic functional tester.	Sentry 20/120 Accutest	
Comments		Multiple-sourcing compatibility, foundry services, training and CAD aids to support User-Designed VLSI and Mead-Designed VLSI.	Uncommitted logic arrays, 20 pin DIP, 130 prefabricated logic elements or 28/40 pin DIP, 400 prefabricated logic elements.

CUSTOM/SEMICUSTOM (cont)		RADIATION HARDENED
Manufacturer	**Zymos (formerly Custom MOS, Inc.)**	**Harris**
FOR DETAILED DATA SEE:		**(Page 4321)**
Customized Standard Circuits	Digital, combined digital/linear	For detailed data on Harris' radiation hardened devices, see pages 4321 to 4430.
Gate Array	Up to 2500 gates, metal-gate CMOS 3000 gates, silicon-gate CMOS 4000 gates, NMOS.	
Chip Density Range (equiv. gates)		
Cell Library	Metal-gate CMOS, silicon-gate CMOS, NMOS	
Design Kit Available	Yes	
Full Custom Circuits Digital	Metal-gate CMOS, silicon-gate CMOS, NMOS	
Linear	CMOS	
Combined Digital/Linear	CMOS	
Provide Design Assistance	Yes	
Acceptable Customer Input (in order of preference)	Logic input through ZyP CAD system, logic diagram, functional specification, customer-owned tooling.	
Design Aids	Circuit simulation, logic simulation, test program generation, artwork generation all linked to common data base, design rule checks, breadboard assistance.	
Production	In-house	
Preferred Delivered Product	Packaged dice preferred, any on request	
Test Program Generation	Yes	
Production Test	Functional, parametric	
Electrical Test Systems Available	Sentry, VII, Lomac	
Comments	ZyP CAD system — logic level design at customer's facility, CMOS and NMOS silicon level simulation.	

CUSTOM/SEMICUSTOM

CUSTOM/SEMICUSTOM

Semi-Custom Arrays (digital and linear circuits customized in final metalization)

Function	Device	Source		Line
	GA1000	**AMI**	**(4307)**	
	GA1500	**AMI**	**(4307)**	
	GA2000	**AMI**	**(4307)**	
	GA2000D	**AMI**	**(4307)**	
	GA2500	**AMI**	**(4307)**	
	GA3000D	**AMI**	**(4307)**	
	GA4000D	**AMI**	**(4307)**	
	GA500	**AMI**	**(4307)**	
	GA5000D	**AMI**	**(4307)**	
	UA-1	AMI		
	UA-2	AMI		
	UA-3	AMI		10
	UA-4	AMI		
	UA-5	AMI		
	UA-6	AMI		
	CDI1100	Cal Devices		
	CDI2100	Cal Devices		
	CDI3200	Cal Devices		
	CDI4200	Cal Devices		
	CDI500	Cal Devices		
	CDI6100	Cal Devices		20
	CDI8800	Cal Devices		
	CLIC-A	Cal Devices		
	CLIC-B	Cal Devices		
	CLIC-C	Cal Devices		
	CLIC-D	Cal Devices		
	CLIC-E	Cal Devices		
	CLIC-F	Cal Devices		
	CLIC-G	Cal Devices		
	CLIC-H	Cal Devices		
	CLIC-J	Cal Devices		30
	CLIC-L	Cal Devices		
	CLIC-M	Cal Devices		
	HC10000	Cal Devices		
	HC12600	Cal Devices		
	HC17800	Cal Devices		
	HC3100	Cal Devices		
	HC4100	Cal Devices		
	HC5400	Cal Devices		
	HC7700	Cal Devices		
	HCSSeries	Cal Devices		40
	CS1200	Cherry		
	CS1300	Cherry		
	CS1400	Cherry		
	CS2000	Cherry		
	CS3000F	Cherry		
	CS3000FX	Cherry		
	CS3200L	Cherry		
	CS3200LX	Cherry		
	CS3500	Cherry		
	CS3500X	Cherry		50
	CS4000M	Cherry		
	CS4000MX	Cherry		
	CAE2000	**CAE**	**(4310)**	
	CMA1550	**CMA**	**(4311)**	
	CMA448	**CMA**	**(4311)**	
	CMA950	**CMA**	**(4311)**	
	X100	Exar		
	XR-A100	Exar		
	XR-B100	Exar		60
	XR-C100A	**Exar**	**(4314)**	
	XR-CHIP	Exar		
	XR-D100	**Exar**	**(4314)**	
	XR-F100	**Exar**	**(4314)**	
	XR-G100	**Exar**	**(4314)**	
	XR-I32L-CHIP	Exar		
	XR-J100	**Exar**	**(4314)**	
	XR-X100	**Exar**	**(4314)**	

(Continued)

Semi-Custom Arrays (digital and linear circuits customized in final metalization) (Cont'd)

Function	Device	Source		Line
	XR200	Exar		
	XR300	Exar		70
	XR400	Exar		
	XR500	Exar		
	XRCMA	Exar		
	XRCMB	Exar		
	XRCMC	Exar		
	XRCMD	Exar		
	9480	Fairchild		
	ECL-Array	Fairchild		
	F200	Fairchild		
	F201	Fairchild		80
	F380	Fairchild		
	GE0020	**Fairchild**	**(4316)**	
	GE0500	**Fairchild**	**(4316)**	
	GE0750	Fairchild		
	GE1000	**Fairchild**	**(4316)**	
	GE2000	**Fairchild**	**(4316)**	
	B200	Fujitsu		
	B2000	Fujitsu		
	B500	Fujitsu		
	C1275	Fujitsu		90
	C2000	Fujitsu		
	C3900	Fujitsu		
	C770	Fujitsu		
	HI4000	Holt		
	MCE	**Interdesign**	**(4433)**	
	MCF	**Interdesign**	**(4433)**	
	MCG	**Interdesign**	**(4433)**	
	MDA	**Interdesign**	**(4433)**	
	MLA	**Interdesign**	**(4433)**	
	MOA	**Interdesign**	**(4433)**	100
	MOB	**Interdesign**	**(4433)**	
	MOC	**Interdesign**	**(4433)**	
	MOD	**Interdesign**	**(4433)**	
	MOE	**Interdesign**	**(4433)**	
	MOF	**Interdesign**	**(4433)**	
	MOG	**Interdesign**	**(4433)**	
	MOH	**Interdesign**	**(4433)**	
	MOJ	**Interdesign**	**(4433)**	
	MOL	**Interdesign**	**(4433)**	
	MOM	**Interdesign**	**(4433)**	110
	MON	**Interdesign**	**(4433)**	
	MONOCHIP	Interdesign		
	MOP	**Interdesign**	**(4433)**	
	MOQ	**Interdesign**	**(4433)**	
	MPA	**Interdesign**	**(4433)**	
	MPB	**Interdesign**	**(4433)**	
	MPC	**Interdesign**	**(4433)**	
	MPD	**Interdesign**	**(4433)**	
	MPX	**Interdesign**	**(4433)**	
	MRA	**Interdesign**	**(4433)**	120
	MRB	**Interdesign**	**(4433)**	
	MRC	**Interdesign**	**(4433)**	
	MRD	**Interdesign**	**(4433)**	
	MRE	**Interdesign**	**(4433)**	
	MSA	**Interdesign**	**(4433)**	
	MSA450	Interdesign		
	MSB	**Interdesign**	**(4433)**	
	MSB880	Interdesign		
	MSC	**Interdesign**	**(4433)**	
	MUA	**Interdesign**	**(4433)**	130
	MUA-225	Interdesign		
	MUB	**Interdesign**	**(4433)**	
	MUC	**Interdesign**	**(4433)**	
	G4312	IMI		
	ISeries	IMP		
	LC-10000	LSI Logic		
	LC-12600	LSI Logic		
	LC-3100	LSI Logic		

(Continued)

Semi-Custom Arrays (digital and linear circuits customized in final metalization) (Cont'd)

Function	Device	Source		Line
	LC-4100	LSI Logic		
	LC-5400	LSI Logic		140
	LC-7700	LSI Logic		
	LCA-1200-ECL	LSI Logic		
	LCA-600-ECL	LSI Logic		
	LSI-5080	LSI Logic		
	LSI-5140	LSI Logic		
	LSI-5220	LSI Logic		
	LSI-5320	LSI Logic		
	LSI-5420	LSI Logic		
	LSI-5600	LSI Logic		
	LSI-7080	LSI Logic		150
	LSI-71000	LSI Logic		
	LSI-7140	LSI Logic		
	LSI-7200	LSI Logic		
	LSI-7320	LSI Logic		
	LSI-7420	LSI Logic		
	LSI-7600	LSI Logic		
	LSI-7800	LSI Logic		
	ML600	Master Logic		
	ML7005	Master Logic		
	ML7010	Master Logic		160
	ML7015	Master Logic		
	ML7020	Master Logic		
	MONOCHIP	Master Logic		
	A75X	Micro Eng		
	A75XS	Micro Eng		
	MCE-A20A	**Micro Eng**	**(4437)**	
	MCE-A20AS	**Micro Eng**	**(4437)**	
	MCE-A20B	**Micro Eng**	**(4437)**	
	MCE-A20BS	**Micro Eng**	**(4437)**	
	MCE-A20C	**Micro Eng**	**(4437)**	170
	MCE-A20CS	**Micro Eng**	**(4437)**	
	MCE-A20E	**Micro Eng**	**(4437)**	
	MCE-A20ES	**Micro Eng**	**(4437)**	
	MCE-A20F	**Micro Eng**	**(4437)**	
	MCE-A20FS	**Micro Eng**	**(4437)**	
	MCE-A20G	**Micro Eng**	**(4437)**	
	MCE-A20GS	**Micro Eng**	**(4437)**	
	MCE-A20H	**Micro Eng**	**(4437)**	
	MCE-A20HS	**Micro Eng**	**(4437)**	
	MCE-A20J	**Micro Eng**	**(4437)**	180
	MCE-A20JS	**Micro Eng**	**(4437)**	
	MCE-A20L	**Micro Eng**	**(4437)**	
	MCE-A20LS	**Micro Eng**	**(4437)**	
	MCE-A20M	**Micro Eng**	**(4437)**	
	MCE-A20MS	**Micro Eng**	**(4437)**	
	MCE-A20W	Micro Eng		
	MCE-A20WS	**Micro Eng**	**(4437)**	
	MCE-A40A	Micro Eng		
	MCE-A40AS	**Micro Eng**	**(4437)**	
	MCE-A40B	Micro Eng		190
	MCE-A40BS	**Micro Eng**	**(4437)**	
	MCE-A40D	**Micro Eng**	**(4437)**	
	MCE-A40DS	**Micro Eng**	**(4437)**	
	MCE-AD15C	**Micro Eng**	**(4437)**	
	MCE-B20A	Micro Eng		
	MCE-B20B	Micro Eng		
	MCE-B40A	Micro Eng		
	MCE-B40B	Micro Eng		
	MCE-D15A	**Micro Eng**	**(4437)**	
	MCE-D15B	**Micro Eng**	**(4437)**	200
	MCE-D15D	**Micro Eng**	**(4437)**	
	MCE-P20A	Micro Eng		
	MCE-P40A	Micro Eng		
	MCE4194	**Micro Eng**	**(4440)**	
	MCE565A	**Micro Eng**	**(4440)**	
	MCE566A	**Micro Eng**	**(4440)**	
	MCE570	**Micro Eng**	**(4440)**	
	MCE571	**Micro Eng**	**(4440)**	

(Continued)

CUSTOM/SEMICUSTOM (Cont'd)

CUSTOM/SEMICUSTOM

Semi-Custom Arrays (digital and linear circuits customized in final metalization) (Cont'd)

Function	Device	Source	Line
	MCE574	**Micro Eng (4440)**	
	MCE6012	**Micro Eng (4440)**	
	MCEL165	**Micro Eng (4440)**	
	MCELM10	**Micro Eng (4440)**	
	MCETCA365	**Micro Eng (4440)**	
	MCEVFC32	**Micro Eng (4440)**	
	MGB110A	**Micro Eng (4437)**	
	MGB160B	**Micro Eng (4437)**	
	MGB210C	**Micro Eng (4437)**	
	MGB270E	**Micro Eng (4437)**	10
	MGB350D	**Micro Eng (4437)**	
	MGB50	**Micro Eng (4437)**	
	MGB500	**Micro Eng (4437)**	
	MGB600	**Micro Eng (4437)**	
	MGC110A	**Micro Eng (4437)**	
	MGC160B	**Micro Eng (4437)**	
	MGC210C	**Micro Eng (4437)**	
	MGC350D	**Micro Eng (4437)**	
	MGC50	**Micro Eng (4437)**	
	MGC500	**Micro Eng (4437)**	20
	MGC600	**Micro Eng (4437)**	
	MT32003	**Micro Eng (4440)**	
	MT34006	**Micro Eng (4440)**	
	MT34009	**Micro Eng (4440)**	
	MT70003	**Micro Eng (4440)**	
	MT70014	**Micro Eng (4440)**	
	MT80001	**Micro Eng (4440)**	
	Unides	Micro Eng	
	MC707	Micro Tech	
	MC717	Micro Tech	30
	MC727	Micro Tech	
	MC737	Micro Tech	
	MA5000	Mitel	
	MA5050	Mitel	
	MA5100	Mitel	
	MA5150	Mitel	
	MASTERMOS	Monosil	
	M10900	**Motorola (4479)**	
	MC10900Z	**Motorola (4479)**	
	MC10901Z	**Motorola (4479)**	40
	MC10902Z	**Motorola (4479)**	
	MC10904Z	**Motorola (4479)**	
	MC10905Z	**Motorola (4479)**	
	MCA1000RECL	**Motorola (4479)**	
	MCA1200ECL	**Motorola (4479)**	
	MCA1300ALS	**Motorola (4479)**	
	MCA2800ALS	**Motorola (4479)**	
	MCA500ALS	**Motorola (4479)**	
	MCA600ECL	**Motorola (4479)**	
	XC160	Motorola	50
	XC177	Motorola	
	XC400	Motorola	
	SLX6320	National	
	SLX6360	National	
	ECL-ARRAY	NEC-Electron	
	NC5050	Nitron	
	NC5100	Nitron	
	NC5150	Nitron	
	NC5200	Nitron	
	NC5350	Nitron	60
	NC5500	Nitron	
	NC5600	Nitron	
	NC91200	Nitron	
	NC91500	Nitron	
	NC9360	Nitron	
	NC9540	Nitron	
	NC9720	Nitron	
	NC9960	Nitron	
	BAA1000	**Plessey (4514)**	

(Continued)

Semi-Custom Arrays (digital and linear circuits customized in final metalization) (Cont'd)

Function	Device	Source	Line
	BAA2000	**Plessey (4514)**	70
	CLA10XX	Plessey	
	CLA12XX	Plessey	
	CLA15XX	Plessey	
	CLA18XX	Plessey	
	SCD-1000	Plessey	
	SCD-2000H	Plessey	
	SCD-2000L	Plessey	
	SCD-2000M	Plessey	
	SCD-4000	Plessey	
	SCD-4000H	Plessey	80
	SCD-4000L	Plessey	
	SCD-4000M	Plessey	
	SCD-5000	Plessey	
	SP9131	Plessey	
	SPD-4000	Plessey	
	CGA1800	Raytheon	
	CGA300	Raytheon	
	MA10150	**RCA (4518)**	
	MA10250	**RCA (4518)**	
	MA10350	**RCA (4518)**	90
	MA10500	**RCA (4518)**	
	MA30150	**RCA (4518)**	
	MA30250	**RCA (4518)**	
	MA60150	**RCA (4518)**	
	MA60250	**RCA (4518)**	
	MA60400	**RCA (4518)**	
	MA60550	**RCA (4518)**	
	MA60800	**RCA (4518)**	
	PA20250	**RCA (4518)**	
	PA20450	**RCA (4518)**	100
	PA20650	**RCA (4518)**	
	PA20850	**RCA (4518)**	
	PA21000	**RCA (4518)**	
	PA40650	**RCA (4518)**	
	PA40850	**RCA (4518)**	
	PA41000	**RCA (4518)**	
	PA41200	**RCA (4518)**	
	PA60650	**RCA (4518)**	
	PA61200	**RCA (4518)**	
	8A1200	Signetics	110
	8A1260	Signetics	
	8A1542	Signetics	
	MLA24	Signetics	
	MLA36	Signetics	
	SCC700	**Signetics (4524)**	
	ULN-2350C	Sprague	
	ULN-2351C	Sprague	
	SY7100	**Synertek (4536)**	
	SY7110	**Synertek (4537)**	
	SY7111	**Synertek (4537)**	120
	TM5000	Telmos	
	HCM1200	Universal	
	HCM1500	Universal	
	HCM360	Universal	
	HCM540	Universal	
	HCM720	Universal	
	HCM960	Universal	
	WD1820	**Western (4563)**	
	WD1840	**Western (4564)**	

Standardized CMOS Array, to Build Custom Circuits by Changing Final Metalization

Function	Device	Source	Line
	C2000H	Fujitsu	130
	C3900H	Fujitsu	
	LA03	GI	
	LA05	GI	
	LA10	GI	
	LA15	GI	
	LA20	GI	
	G50500	GTE Micro	

(Continued)

Standardized CMOS Array, to Build Custom Circuits by Changing Final Metalization (Cont'd)

Function	Device	Source	Line
	G51000	GTE Micro	
	G51500	GTE Micro	
	HI1000	Holt	140
	HI3700	Holt	
	MCA	**Interdesign (4433)**	
	MCB	**Interdesign (4433)**	
	MCC	**Interdesign (4433)**	
	MCD	**Interdesign (4433)**	
	G4060	IMI	
	G4112	IMI	
	G4160	IMI	
	G4220	IMI	
	G4264	IMI	150
	G4321	IMI	
	G4364	IMI	
	G4420	IMI	
	G4480	IMI	
	G70200	IMI	
	G70360	IMI	
	G70640	IMI	
	G71000	IMI	
	G71440	IMI	
	G71960	IMI	160
	MCA	Master Logic	
	MCB	Master Logic	
	MCC	Master Logic	
	MCD	Master Logic	
	ML100	Master Logic	
	ML150	Master Logic	
	ML200	Master Logic	
	ML350	Master Logic	
	ML50	Master Logic	
	ML75	Master Logic	170
	MC606	Micro Tech	
	MC616	Micro Tech	
	MC626	Micro Tech	
	MC636	Micro Tech	
	MONOLOGIC	Monosil	
	SCX6324	National	
	SLX6324	National	
	TM3050	Telmos	
	TM3100	Telmos	
	TM3150	Telmos	180
	TM3200	Telmos	
	TM3350	Telmos	
	TM3500	Telmos	
	TM3600	Telmos	
	TM4000	Telmos	
	TM6000	Telmos	

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ABBREVIATIONS OF COMPANY NAMES

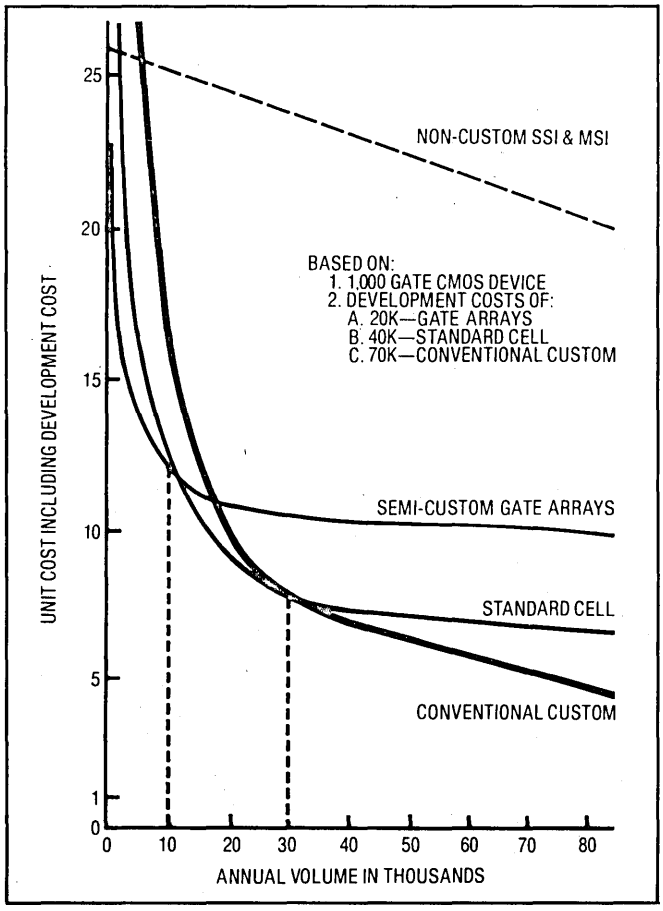
Action Ins	Action Instruments
AD	Analog Devices
ADT	Advanced Digital Technology
Adapt Sci	Adaptive Science Corp.
Advent	Advent Products, Inc.
Alphatron	Alphatron
AMA	American Automation
AMD	Advanced Micro Devices
AMI	American Microsystems, Inc.
Amperex	Amperex Electronic Corp.
Analogic	Analogic
Analog Sys	Analog Systems
APC	Applied Micro Circuits
Apex	Apex Microtechnology
APM	Applied Microsystems Corp.
Appl Sys	Applied Systems Corp.
APT	Applied Microtechnology
Aptek	Aptek Microsystems
Array Tech	Array Technology
AWI	Analog West
Bedford	Bedford Computer Systems Inc.
Burr-Brown	Burr-Brown Research
CAE	Computer Aided Engineering
Cal Devices	California Devices
Cent Data	Central Data Corp.
Cermetek	Cermetek
CGRS	CGRS Microtech Inc.
Cherry	Cherry Semiconductor
CIC	Custom Integrated Circuits
Citel	Citel, Inc.
Comlinear	Comlinear Corporation
CMA	Custom MOS Arrays
Comark	Comark Corp.
Comdial	Comdial Semiconductor
Comp Auto	Computer Automation
Compas	Compas Microsystems
Cont Logic	Control Logic Inc.
Control Sys	Control Systems Microsystems Div.
CreMicro	Creative Micro Systems
Cromemco	Cromemco, Inc.
CSG	Commodore Semiconductor Group
Cubit	Cubit Inc.
Curtis	Curtis Electro Devices, Inc.
Cybernetic	Cybernetic Micro Systems
Cybersys	Cybersystems
Cybertek	Cybertek Inc.
Data General	Data General
Data I/O	Data I/O
Data Trans	Data Translation
Datel	Datel-Intersil
Datricon	Datricon Corporation
DDC	Data Devices Corporation
DEC	Digital Equipment Corporation
Delco	Delco Electronics
DGM	Digital Microsystems
Digelec	Digelec Corp.
Digitek	Digitek, Inc.
Dionics	Dionics Inc.
Dist Comp	Distributed Computer Systems
Divers Tech	Diversified Technology
E-HI	E-H International, Inc.
Elind	Elind Elettronica Industriale
EL Instr	E & L Instruments
EMM	EMM
Emulogic	Emulogic Inc.
Epson	Epson America, Inc.
ETI Micro	ETI Micro
Exar	Exar Integrated Systems
Fairchild	Fairchild
Ferranti	Ferranti Electric
Fujitsu A	Fujitsu America
Fujitsu	Fujitsu Microelectronics, Inc.
GI	General Instrument
GMS	General Microsystems
GTE Micro	GTE Microcircuits
Harris	Harris Semiconductor
Heurikon	Heurikon Corp.
Hilevel	Hilevel Technology, Inc.
Hitachi	Hitachi America, Ltd.
Holt	Holt Inc.
HP	Hewlett-Packard
Hughes	Hughes Aircraft, Solid State Products
Hybrid Sys	Hybrid Systems
Hycom	Hycom Incorporated
IDT	Integrated Device Technology
IMI	International Microcircuits, Inc.
IMP	International Microelectronic Products
IMS	Industrial Micro-systems Inc.
Inconix	Inconix Corporation
Ind Tech	Inductive Technology
Inmos	Inmos
IntCirEng	Integrated Circuit Engineering
IntCirSys	Integrated Circuit Systems
IntCompSys	Integrated Computer Systems
IntCyber	International Cybernetics
Int Micro	International Microsystems
Int Tech	Integrated Technology Corp.
Intech/FMI	Intech/Function Modules Inc.
Intel	Intel
Interdesign	Interdesign
Intersil	Intersil
Intronics	Intronics
IPI	Integrated Photomatrix Inc.
ITT	ITT Semiconductors
Kinetic Sys	Kinetic Systems
Kontron	Kontron Electronics
Lambda	Lambda Semiconductor
Laserdyne	Laserdyne
LSI Comp	LSI Computer Systems
LSI Logic	LSI Logic Corporation
Master Logic	Master Logic Corporation
Matrix	Matrix Corp.
Matrox	Matrox Electronic Systems
MCC	Microcomputer Control
Micrel	Micrel
Micro Eng	Micro Circuit Engineering
Micro Innov	Micro Innovators
Micropac	Micropac Industries
Micro Net	Micro Networks
Micro Pwr	Micro Power Systems
Micro Sci	Micro Sciences Corp.
Micro Tech	Microcircuits Technology
Micro-Link	Micro-Link Corporation
Micron	Micron Technology
MilerTron	MilerTronics
Miller	Miller Technology
Mitel	Mitel Semiconductor
Mitsubishi	Mitsubishi Electronics
MMI	Monolithic Memories, Inc.
Monosil	Monosil
MonSys	Monolithic Systems Corp.
Mostek	Mostek
Motorola	Motorola Semiconductor
MRC	MRC Systems
Murray	Murray Consulting
National	National Semiconductor
NCR	NCR Corp., Microelectronics Division
NEC-EA	NEC/Electronic Arrays Division
NEC Electron	NEC/Electron Division
NEC Micro	NEC/Microcomputer Division
Nitron	Nitron
Nortek	Nortek
OAE	Oliver Advanced Engineering
Octagon	Octagon Systems Corp.
OEI	Optical Electronics Inc.
Ohio Sci	Ohio Scientific
OKI	OKI Semiconductor
Omnibyte	Omnibyte Corp.
Oscar	I. S. Oscar Assoc.
Panasonic	Panasonic
PC/M	Pacific/Cyber Metrix
Percom	Percom Data Co.
Phoenix	Phoenix Digital Corp.
Pico Design	Pico Design
Polycore	Polycore Electronics
Plessey	Plessy Semiconductors
PMI	Precision Monolithics, Inc.
PragDes	Pragmatic Design Inc.
PREMA	PREMA GmbH
Pro-Log	Pro-Log Corp.
Quay	Quay Corp.
Raytheon	Raytheon Semiconductor
RCA	RCA Solid State Division
RCI Data	RCI Data
RELMS	Relational Memory Systems
Reticon	Reticon
RIFA	RFIA
Rockwell	Rockwell, Microelectronic Devices
RTC	Riehl Time Corporation
Sanken	Sanken Electric
Sanyo	Sanyo
SEEQ	SEEQ Technology, Inc.
Semi Proc	Semi Processes
Siemens	Siemens
Signetics	Signetics
SGS	SGS-ATES Semiconductor
Sharp	Sharp
Silicon G	Silicon General
Siliconix	Siliconix
Silicon Sys	Silicon Systems Inc.
Siltronics	Siltronics
SMC	Standard Microsystems Corp.
Solarise	Solarise Enterprises
Solitron	Solitron Devices
Sprague	Sprague Electric Company
SSM	Solid State Micro Technology for Music
SSS	Solid State Scientific
Stag	Stag Microsystems
Struc. Des.	Structured Design Inc.
Stynetic	Stynetic Systems
Sunrise	Sunrise Electronics
Sunshine	Sunshine Semiconductor
Supertex	Supertex Inc.
Symtek	Symtek Corp.
Synapse	Synapse Corp.
Synertek	Synertek
Sys Innov	Systems Innovations
Tau Zero	Tau Zero Inc.
Tektronix	Tektronix
Telaris	(See Laserdyne)
Teledyne C	Teledyne Crystalonics
Teledyne P	Teledyne Philbrick
Teledyne S	Teledyne Semiconductor
Telefunken	Telefunken
Telephonics	Telephonics LSI
Telmos	Telmos
Teltone	Teltone Corporation
TI	Texas Instruments
Thomson-CSF	Thompson-CSF Components Corp.
TMX	TMX
Topanga	Topanga Data Systems
Toshiba	Toshiba America
Trans-Data	Trans-Data
TRW	TRW-LSI Products
Unitrode	Unitrode
Universal	Universal Semiconductor, Inc.
Vantage	Vantage Data Products
VTI	VLSI Technology, Inc.
Votrax	Votrax
Weitek	Weitek Corporation
Western	Western Digital
Wintek	Wintek Corp.
Xicor	Xicor, Inc.
Xycom	Xycom
Zendex	Zendex Corp.
Zilog	Zilog
Zymos	Zymos Corporation

THE SPECTRUM OF SOLUTIONS.

The decision to use a custom circuit depends on your system design requirements—such things as complexity, features, size and power limitations. But no longer is your custom decision limited by low volume or short development time—not when you come to AMI.

AMI has a full-spectrum of custom solutions to assure you get that solution which meets your system performance and time-to-market requirements at the lowest possible cost.

AMI's spectrum of solutions bridges the total span of volume, timing and interface needs of our customers. From semi-custom gate arrays, to standard cell custom designs, to full custom design—somewhere on the spectrum, your development time and volume requirements can be met. For customers who already have their designs, AMI can provide custom fabrication for the customer's tooling. We will even teach custom design if that's what our customers need. And we can even go a step further and license the technology for a customer to set up his own fabrication capability. No other company offers such a spectrum of solutions. And no other company has more experience at helping you pick the best solution for your needs.



Cost vs Volume Alternatives in Custom

Gate Arrays.

Short development time
Low development costs
Fast production turn-on

Our semi-custom gate arrays are the best solution for circuits of moderate complexity in low to medium volume applications.

AMI CMOS semi-custom gate arrays are standard logic layouts of everything except the final metal interconnect pattern. Since only the final pattern needs to be developed to customize your circuits, both development time spans and development costs are dramatically reduced. Because wafers containing arrays are preprocessed and inventoried, production lead times are short. Gate arrays are especially attractive for applications requiring circuit volumes from 1,000 to 50,000 units per year.

For complete information on AMI's Gate Arrays, refer to AMI's 3μ data sheet.

Standard Cell Custom.

Reduced development time
Low development costs
Lower production costs

Standard cells are full-custom circuits which are designed from computer stored modular cells. The computer assembles the cells into a collection of functional blocks to form a custom circuit. Since standard cells utilize predesigned cells, development time is reduced dramatically and development costs are cut 30 to 50 percent over conventional custom design. Circuit size is likely to be slightly larger than a conventional custom circuit, so they are most appropriate where rapid development is more important than minimal size. Standard cells are cost-effective in volume levels beginning around 10,000 circuits.

With the standard cell approach, your designs can be hand tailored to add certain functions, such as analog, not in the standard cell library.

AMI has a larger family of 5μ and 3μ NMOS and CMOS cells available. For a partial listing refer to the tables at the end of AMI's Custom Solution section.

Conventional Custom Design.

Lowest production costs
Minimum circuit size
Lowest power requirements

With conventional custom, circuit size is shrunk to the absolute minimum. Since less silicon is used, production costs are dramatically reduced. Where end product volume is high—beyond 50,000 units per year—or where special requirements for lowest

power, minimal space or highest performance exist, the solution is likely to be conventional custom design.

Computer speeds design.

Instrumental in the design of custom circuits is our Symbolic Interactive Design System (SIDS).

The design is done primarily with SIDS where a layout designer works with symbols directly at a large screen alphanumeric color CRT. After the SIDS circuit design has been completed and verified, the symbols are converted to polygons and a 10X reticle tape is prepared.

SIDS uses on-line, real-time design rule checking capability to isolate design rule errors in the layout. This allows immediate correction which greatly reduces the development span time.

Also a nodal trace function permits a designer to trace and highlight a given electrical node. In this way, the designer can manually ensure that the node is connected as specified in the master logic description.

Full background real-time design rule checking on windows, cells, and chips is supported, as is full background continuity checking against the master logic description. This eliminates the delay from digitizing and batch processed computer checking of circuits for accuracy.

With SIDS, error correction, circuit modification and area relocations take only minutes. That significantly reduces design cycle time and development costs.

Computer-aided hand drawn layouts are used to reduce extremely complex circuits to the absolute smallest size. Development time and costs are higher, but in certain cases, size or complexity requirements may require the hand-drawn approach.

Customer Designed Solutions.

Design cycle control
Maximum proprietary control of designs
Versatile process capability

Many of our customers have their own circuit designs. In this case AMI can provide custom circuit fabrication for customer-owned tooling.

Over the past ten years, AMI has manufactured over 800 MOS/VLSI circuits that were designed either by our customers or by firms our customers hired as designers. From this extensive experience, we have developed documented procedures which make customer-manufacturer interface smooth and easy.

The complete job—tape conversion, mask making, fabrication in any of 25 variations of MOS processes, probe, assembly, packaging and final test—is done in-house. That means we're directly accountable to you in every aspect.

AMI also has documented design rules for all of its 25 variations of CMOS, NMOS and PMOS processes, including industry standard, advanced CMOS II and NMOS II. Design cycles can be dramatically shortened by using AMI's standard cells and advanced CAD technology, and design training is available for your designs and engineers, as well.

AMI also works closely with many outside design houses who can assist the customer in his design. And all of the design aids that are available to AMI designers can be made available to a customer to aid in his design.

AMI can accept a customer's fabrication job at any level: working plates, pattern generation tape or data base tapes accompanied with a developed test program and specification. Close cooperation between the customer and AMI simplifies circuit debug and facilitates manufacture at circuit completion. At the same time it gives you complete proprietary protection and control over design and production scheduling.

Through our diversity of MOS process types, engineering support, test equipment and package options, we provide you a degree of flexibility no one else can offer.

You can get your circuits any way you like, as wafers, die, tested or untested assemblies, with development spans which will keep your project on schedule.

Method	Development Time	Production* Turn-On	Total Time to Production
Gate Arrays	7 weeks	6 weeks	13 weeks
Standard Cells	12 weeks	8 weeks	20 weeks
Full Custom	26 weeks	8 weeks	34 weeks
Custom Fabrication	(Customer)	8 weeks	8 weeks

*After Customer Approval

Comparative Time-To-Market Requirements for Custom Design Approaches

AMI technologies and development spans.

	NMOS		CMOS	
FEATURE	NMOS I	NMOS II	CMOS I	CMOS II
(Effect) Channel Lgth.	2.6 μM	2.1 μM	3.0 μM	2.1 μM
(Drawn)	3.5 μM	3.0 μM	5.0 μM	3.0 μM
Field Ox Pitch	7.5 μM	6.0 μM	10.0 μM	6.0 μM
Poly Pitch	7.5 μM	6.0 μM	10.0 μM	6.0 μM
Metal Pitch	8.5 μM	7.0 μM	10.0 μM	7.0 μM
Channel Width (Drawn)	4.0 μM	3.0 μM	5.0 μM	3.0 μM
Contact Size	3×3 μM	3×3 μM	5×5 μM	3×3 μM
Inverter Delay (FO = 1)	2.5 NS	1.5 NS	2.9 NS	1.7 NS
Power Supply	5-12V	5V	5-12V	5V
Development Spans Weeks To Cut & Go's	5	6	5	6

Joint Development Teams.

Circuit design training
Design capability in-house
Fabrication technology licensing

Through a Joint Development Team (JDT) we can teach a customer to design his own MOS/VLSI circuits.

The JDT is a combination of technically skilled people from the partner company and AMI who function as a design group concentrating on the customer's products alone. The JDT partner brings his system staff and AMI brings the MOS/VLSI circuit design staff with their design technology. The partner becomes part of an in-house AMI design group. Each JDT is customized to meet the needs of the partner company. The end result is a design capability for the partner company for circuits that AMI will fabricate.

A JDT can be set up either as an on-going group or as a short-term team for design training.

In the on-going JDT there is continuous interaction between the partner system engineer and the AMI circuit design staff. All CAD (computer-aided design) tools are available to the members of a JDT. This on-going JDT gives the customer the advantage of controlling an in-house design group at AMI which is dedicated solely to the partner company's products and requirements.

The short-term JDT can be used where a customer wishes to train and establish a design center in-house or to upgrade an existing design center.

Technology Transfers.

If you want to go beyond designing your own circuits, to operate your own manufacturing/pilot line, AMI will license the necessary technology in those situations where a long-term business relationship can be established between the partner company and AMI.

Leading CAD Technology.

Shorten design span
Reduce risk
Lower design cost

At almost all levels of the spectrum computer-aided design (CAD) software and hardware aids are employed to assure correctness of design each step of the way and to shorten design spans reducing customer risk and lowering design cost. Highly efficient programs have been implemented to assist in logic design and simulation, layout planning, switched capacitor analysis routines and symbolic interactive design layout, to name just a few.

Hardware design aids include:

- ☐ On-site Burroughs 7760 computer with multiprocessing capability
- ☐ Computer terminals built around a Prime computer and engineering design facilities which tie in to the on-site 7760 and time-sharing services
- ☐ Computervision interactive graphics system which provides on-line generation and editing of composite drawings; includes drafting surfaces and CRT displays
- ☐ Calma graphics system for both production digitizing and on-line changes
- ☐ Calma GDS-II high-speed electronstatic plotter
- ☐ Calcomp 748 Flatbed Plotter
- ☐ High-speed, high-resolution Electromask 9-track pattern generator

Software design aids include:

- ☐ BOLT—Block Oriented Logic Translator—Bolt is a logic description compiler that generates a common data base used by SIDS, SIMAD, LPA, Continuity Check, PATH and CIPAR
- ☐ SIMAD—Simulation With Assignable Delays
- ☐ PATH—Path Analysis Timing Verification
- ☐ AMI Spice Circuit Simulator
- ☐ AMI Aspec Circuit Simulator
- ☐ CIPAR—Custom Circuit Interactive Placement and Routing—This software package creates error free mask data in the shortest time by interactive placement and routing of standard/special cell
- ☐ GAPAR—Gate Array Placement Routing
- ☐ DELAY—Drop delays on actual mask layout capacitance
- ☐ Trace and Continuity Checking
- ☐ RTL—Register Transfer Language
- ☐ LPA—Layout Planning Aid—This software program shortens the span time for topological plan preparation and helps evaluate many different topological options. It will help create the optimum topological plan for mask design on the SIDS system
- ☐ SIDS—Symbolic Interactive (Mask) Design System
- ☐ DRC—Geometrical Design Rule Checking
- ☐ SCAR—Switched Capacitor Analysis Routine
- ☐ Test Pattern Generator
- ☐ Test Program Generation

MOS Process Flexibility.

25 variations
Process compatibility

At AMI you get the widest selection of MOS alternatives and capabilities in the industry. Our core processing technologies range from the mature PMOS metal gate, to silicon gate N-Channel, to the advanced, small geometry, high performance silicon gate CMOS.

A total of over 25 variations of core process in PMOS, NMOS, and CMOS are available. This variety provides both the optimum process for new designs and compatibility with existing customer designed circuits.

Digital and Analog Combinations.

Save space
Increase reliability
Minimize system complexity

AMI is a leading innovator in combining digital and analog functions on a single chip. We can combine any of the following functions into an optimum circuit configuration to meet your needs.

Digital	Analog
PLA	OP AMP
ALU	Oscillator
Inverter	Comparator
RAM and ROM	Voltage Reference
Shift Register	A/D and D/A Converters
Interface Driver	Switched Capacitor Filters
Automatic Power Down	Programmable Power Down Phase-locked loops

Unique combinations of these functions are already used in many applications in the communications, consumer and industrial marketplace including: thermostat controller, audio multiplexer, single-chip microcomputer, single-chip Codec tone receiver, spectrum analyzer, echo cancellor, speech synthesizer, modems, repertory dialer, touch-tone generator.

AMI Delivers Quality.

AMI quality controls for in-process wafer inspection and final assembly and test are the best in the industry. Our care in fabrication, assembly and test means that you get products that meet your specifications for reliability. Because over 70 percent of our total production is custom, we perform many checks routinely that would only be done on special orders and at additional cost by other manufacturers. In fact, our own in-house standards are tougher than most of our customers require. Most importantly, AMI is committed to making sure that everything we do is done right, every time we do it.

The industry's highest standard.

AMI has consistently pursued product excellence and has reached for higher quality levels in finished products shipped. Circuits are inspected to 0.1% AQL or your specifications, whichever is more stringent.

This 0.1% AQL can put you in a superior competitive position. Your incoming test and assembly costs come down since there's less reworking on the line. And your customer's receive a more reliable product.

Quality Checks.

Among the routine quality controls exercised over every product at AMI are:

- ☐ Full logic design checks against system specifications
- ☐ Circuit simulation to verify performance against objectives
- ☐ Working plates check on automatic checkers
- ☐ Automated mask fabrication checks
- ☐ In process wafer fabrication checks
- ☐ Wafer sort tests
- ☐ 100% optical inspection at dicing
- ☐ 100% die attach checking
- ☐ 100% lead bonding inspection prior to package sealing
- ☐ Seal checks, fine and gross leak tests
- ☐ Final digital and analog tests
- ☐ Customer specified environmental tests

Meticulous in-process checks are performed on design and workmanship at every step, to ensure a fully manufacturable device. In manufacture, lot process and yield data are captured and examined as a matter of routine.

A Capability and a Commitment.

As the world's largest company dedicated to custom MOS/VLSI circuitry design and manufacturing, AMI has worked with practically every type of MOS/VLSI circuit. We developed the first single chip microcomputer. We were first with watches, calculators, combined analog/digital circuits, and a host of other innovations in consumer electronics, electronic data processing and telecommunications.

More than sixteen years of experience with 1500 different custom and customer designed circuits has taught us a lot about the special requirements beyond custom design. Such things as efficient production controls for small lot manufacture. Custom tailored quality assurance and reliability programs. Design and product security. And the wide range of custom approaches needed to achieve optimum cost-effectiveness for our customers.

Whatever your requirements or questions about a custom or semi-custom MOS/VLSI circuit, we can help you find the right solution. Because no other company offers you more services, experience, and capability in a single place than AMI.

Table 1. Combinational and I/O Elements

CELL NAME	DESCRIPTION	CMOS EQUIV	TTL EQUIV	2-IN GATE EQUIV	AREA $IN^2 \times 10^{-6}$	SPEED (TYP) nsec	POWER (TYP) μW
NND2L1	2-Input NAND (L.P.)	4011	74LS00	1.0	10.0	70	112
NND2L3	2-Input NAND (STD)	4011	74LS00	1.0	10.0	15	500
NND2L4	2-Input NAND (H.S.)	4011	74LS00	1.0		D10	
NND3L1	3-Input NAND (L.P.)	4023	74LS10	1.3	12.6	85	112
NND3L3	3-Input NAND (STD)	4023	74LS10	1.3	12.6	22	500
NND3L4	3-Input NAND (H.S.)	4023	74LS10	1.3		D13	
NND4L1	4-Input NAND (L.P.)	4012	74LS20	1.7	14.9	85	112
NND4L3	4-Input NAND (STD)	4012	74LS20	1.7	14.5	26	500
NND4L4	4-Input NAND (H.S.)	4012	74LS20	1.7		D15	
NOR2L1	2-Input NOR (L.P.)	4001	74LS02	1.0	9.3	80	112
NOR2L3	2-Input NOR (STD)	4001	74LS01	1.0	9.3	15	500
NOR2L4	2-Input NOR (H.S.)	4001	74LS01	1.0		D10	
NOR3L1	3-Input NOR (L.P.)	4025	74LS27	1.3	11.9	95	112
NOR3L3	3-Input NOR (STD)	4025	74LS27	1.3	13.8	19	500
NOR3L4	3-Input NOR (H.S.)	4025	74LS27	1.3		D13	
NOR4L1	4-Input NOR (L.P.)	4002	—	1.3	16.4	95	112
NOR4L3	4-Input NOR (STD)	4002	—	1.3	17.1	19	500
NOR4L4	4-Input NOR (H.S.)	4002	—	1.3		D15	
INVRL1	Inverter (L.P.)	4069	74LS04	0.7	10.0	65	112
INVRL3	Inverter (STD)	4069	74LS04	0.7	7.4	15	500
INVRL4	Inverter (H.S.)	4069	74LS04	0.7		D10	
ITTLF0*	Input Buffer for TTL (L.P.)	4050	—	—	76.6	56	250
ITTLT0*	Input Buffer for TTL (L.P.)	4050	—	—	84.8	52	250
ITTLF1*	Input Buffer for TTL STD. Speed Power	—	—	—	76.5	19	1200
ITTLT1*	Input Buffer for TTL STD. Speed Power	—	—	—	84.8	34	1200
ITTLF2*	Input Buffer for TTL (H.S.)	—	—	—	76.6	13	1500
ITTLT2*	Input Buffer for TTL (H.S.)	—	—	—	84.8	10	1500
OBAAT1*	Output Buffer	4050	—	—	84.8	100	2640
OBAAT2						D70	
OBAAF1*	Output Buffer	4050	—	—	90.0	100	2640
OBAAF2						D70	
OBTSF1*	Tri-State Output Buffer	—	—	—	116.0	65	1140
OBTSF2						D50	
OBTST1*	Tri-State Output Buffer	—	—	—	107.6	60	1140
OBTST2						D50	
XOR2S1	Exclusive OR (L.P.)	—	74LS266	2	12.6	80	112
XOR2S3	Exclusive OR (STD)		74LS266	2	15.3	19	1000
XOR2S4	Exclusive OR (H.S.)		74LS266	2		D13	
XNR2S1	Exclusive NOR (L.P.)	—	74LS266	2	13.8	100	112
XNR2S3	Exclusive NOR (STD)	—	74LS266	2	12.6	23	1000
XNR2S4	Exclusive NOR (H.S.)	—	74LS266	2		D15	
OBODF1*	Open Drain Output Buffer	—	—	—	90.0	52	640
OBODT1*	Open Drain Output Buffer	—	—	—	84.8	52	640
ANRIL2	AND-NOR-INV Gate (L.P.)	4019	74LS51	2	17.9	75	112
ANRIL3	AND-NOR-INV Gate (STD)	4019	74LS51	2	17.9	17	500
ANRIL4	AND-NOR-INV Gate (H.S.)	4019	74LS51	2		D13	
MUX4L1	4 to 1 Multiplexer (L.P.)	4052	74LS153	6	34.8	112	450
MUX4L3	4 to 1 Multiplexer (STD)	4052	74LS153	6	40.1	34	2000
MUX4L4	4 to 1 Multiplexer (H.S.)	4052	74LS153	6		D20	
ADDRL1	Full Adder (L.P.)	4008	74LS83	9.7	49.1	285	560
ADDRL3	Full Adder (STD)	4008	74LS83	9.7	55.4	95	2500
ADDRL4	Full Adder (H.S.)	4008	74LS82				

*NOTE: Suffix F - Scribe line to power bus minimized
Suffix T - Pad spacing minimized

L.P. Low Power
STD Standard
H.S. High Speed (in development)

Table 1. (continued) Storage and Transfer Elements

CELL NAME	DESCRIPTION	CMOS EQUIV	TTL EQUIV	2-IN GATE EQUIV	AREA $IN^2 \times 10^{-6}$	MAX OPERATING SPEED (TYP) nsec	POWER (TYP) μW
CKDRL1	Clock Driver (L.P.)	—	—	2.7	12.6	2.5	225
CKDRL3	Clock Driver (STD)			3.3	16.8	12.0	1000
CKDRL4	Clock Driver (H.S.)					D 16.0	
SNCAS1	Synchronous Counter Bit, Cascadeable (L.P.) W/Asyn Reset	4518	—	8.3	33.7	2.7	560
SNCAS3	Synchronous Counter Bit, Cascadeable (STD) W/Asyn Reset	4518	—	8.3	39.3	12.0	2500
SNCAS4	Synchronous Counter Bit, Cascadeable (H.S.) W/Asyn Reset	4518				D 16.0	
SNCBS1	Synchronous Counter Bit, W/Asyn Reset (L.P.)	4518	—	8.3	34.8	2.4	560
SNCBS3	Synchronous Counter Bit, W/Asyn Reset (STD)	4518	—	8.3	39.4	12.0	2500
SNCBS4	Synchronous Counter Bit, W/Asyn Reset (H.S.)	4518	—	8.3		D 16.0	
	Note: SNCA & SNCB are in alternating pairs						
UDCAS1	UP/DOWN Counter Bit; Cascadeable Alternating A&B. Sync. Parallel Load, W/Async. Reset (L.P.)	4029	74LS193	9.0	37.8	2.7	560
UDCAS3	UP/DOWN Counter Bit; Cascadeable Alternating A&B. Sync. Parallel Load, W/Async. Reset (STD)	4029	74LS193	9.0	39.3	12.0	2500
UDCAS4	UP/DOWN Counter Bit; Cascadeable Alternating A&B. Sync. Parallel Load, W/Async. Reset (H.S.)	4029	74LS193	9.0		D 16.0	
UDCBS1	UP/DOWN Counter Bit; Cascadeable Alternating A&B. Sync. Parallel Load, W/Async. Reset (L.P.)	4029	74LS193	9.0	36.7	2.7	560
UDCBS3	UP/DOWN Counter Bit; Cascadeable Alternating A&B. Sync. Parallel Load, W/Async. Reset (STD)	4029	74LS193	9.0	38.6	9.0	2500
UDCBS4	UP/DOWN Counter Bit; Cascadeable Alternating A&B. Sync. Parallel Load, W/Async. Reset (H.S.)	4029	74LS193	9.0		D 14.0	
	Note: UDCA&UDCB are used in alternating pairs						
RIPCS1	Ripple Counter Bit W/Async Set & Reset (L.P.)	4020	74LS93	6.0	23.9	2.1	337
RIPCS3	Ripple Counter Bit W/Async Set & Reset (STD)	4020	74LS93	6.0	26.2	9.0	1500
RIPCS4	Ripple Counter Bit W/Async Set & Reset (H.S.)	4020		6.0		D 14.0	
JKFFS1	Flip Flop W/Async Set & Reset (L.P.)	4027	74LS112	9.7	40.4	2.5	670
JKFFS3	Flip Flop W/Async Set & Reset (STD)	4027	74LS112	9.7	43.4	13.0	3000
JKFFS4	Flip Flop W/Async Set & Reset (H.S.)					D 16.0	
BBSRD1	Dynamic Serial Shift Register (L.P.)	4015	74LS164	2.0	9.3	3.2	120
BBSRD3	Dynamic Serial Shift Register (STD)	4015	74LS164	2.0	11.5	12.0	500
SRPLS1	Shift Register Bit W/Sync Parallel Load + Common Async Reset (L.P.)	4035	—	6.0	28.0	2.7	337
SRPLS3	Shift Register Bit W/Sync Parallel Load + Common Async Reset (STD)	4035	—	6.0	28.0	12.0	1500
SRPLS4	Shift Register Bit W/Sync Parallel Load + Common Async Reset (H.S.)	4035		6.0		D 16.0	
LTCHS1	D-Latch (L.P.)	4042	74LS75	2.7	13.0	3.5	225
LTCHS3	D-Latch (STD)	4042	74LS75	2.7	13.4	16.0	1000
LTCHS4	D-Latch (H.S.)	4042	74LS75	2.7		D 20.0	
DFFLS1	D-Flip Flop (L.P.) Async Set & Reset	4013	74LS74	6.0	30.7	3.0	337
DFFLS3	D-Flip Flop (STD) Async Set & Reset	4013	74LS74	6.0	32.5	13.0	1500
DFFLS4	D-Flip Flop (H.S.) Async Set & Reset	4013	74LS74	6.0		D 18.0	

AMERICAN MICROSYSTEMS, INC.

HIGH PERFORMANCE GATE ARRAYS

3μSILICON GATE CMOS TECHNOLOGY

Features

- ☐ Typical Delay: 2ns/gate
- ☐ Up to 5000 Equivalent 2-Input Gates
- ☐ Total I/O Flexibility
- ☐ 36 to 134 Pins Available
- ☐ Power Supply Range: 2.5V to 5V ± 10%
- ☐ Temperature Range: −55°C to 125°C
- ☐ TTL or CMOS Compatible I/O
- ☐ Input Protection Networks on All Pads
- ☐ High External/Internal Noise Immunity
- ☐ Virtually Latch-Up Free
- ☐ Fully Integrated Software Support

General Description

The GA-series of gate arrays are fabricated using state-of-the-art 3 micron, oxide-isolated, isoplanar, silicon-gate CMOS technology. This process, called CMOS-II, features effective channel lengths for P-and N-channel transistors of approximately 2 micro-meters, allowing circuit complexities of up to 5000 equivalent 2-input gates with typical propagation delays of 2ns.

Gate arrays are pre-designed and pre-fabricated silicon chips that contain matrices of uncommitted CMOS transistor pairs used to implement combinatorial and sequential logic functions by connecting the available components with a unique metal pattern tailored to satisfy user requirements. The number of customized masks is dependent on the number of metal layers used to interconnect the uncommitted devices on the array, and it affects the development and manufacturing costs since more engineering effort and lower yields are associated with multi-level metal personalization. As shown below, the GA-series of gate arrays comprises a single metal interconnect option with gate densities ranging from 500 to 2500 gates, and a double metal family with up to 5000 gates.

Table 1. 3μ Single Metal Family

Part No.	Eq. 2-Input Gates	Bonding Pads	Die Size (Mils)	*Typical Development Span (weeks)
GA-2500	2500	84	265×244	14
GA-2000	2025	74	245×219	12
GA-1500	1500	64	224×195	10
GA-1000	1020	52	199×166	8
GA-500	500	36	162×127	7

Table 2. 3μ Double Metal Family

Part No.	Eq. 2-Input Gates	Bonding Pads	Die Size (Mils)	*Typical Development Span (weeks)
GA-5000 D	4995	134	350^2	14
GA-4000 D	4012	120	320^2	12
GA-3000 D	3080	102	290^2	10
GA-2000 D	2070	84	260^2	8
GA-1000 D	1000	62	230^2	7

*Assumes customer supplies breadboard schematic, and device specifications

Absolute Maximum Ratings

Supply Voltage, V_{DD}	−.5V to +7V
Input Voltage, V_{IN}	−.5V to V_{DD} +.5V
D.C. Input Current, I_I	±10mA
Storage Temperature, T_{STG}	−65° to 150°C

D.C. Electrical Characteristics: $V_{DD}=5V\pm10\%$, $V_{SS}=0V$, $T_A=-55°$ to 125°C

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_{DD}	Quiescent Supply Current		10	50	μA	$V_I=V_{DD}$ or V_{SS}
V_{OL}	Low Level Output Voltage			.05	V	$I_{OL}=1\mu A$
				.4	V	$I_{OL}=3.2mA$
V_{OH}	High Level Output Voltage	4.95			V	$I_{OH}=-1\mu A$
		2.40			V	$I_{OH}=-5mA$
V_{IL}	Low Level Input Voltage	−.5		.8	V	TTL Interface
		−.5		1.5	V	CMOS Interface
V_{IM}	High Level Input Voltage	2.0		V_{DD} +.5	V	TTL Interface
		3.5		V_{DD} +.5	V	CMOS Interface
I_{IN}	Input Leakage Current			1	μA	$V_{IN}=V_{DD}$
I_{OZ}	High Impedance Output Leakage Current	−10	.001	10	μA	$V_{OH}=V_{DD}$ or V_{SS}
C_{IN}	Input Capacitance		5		pF	Any Input

Switching Characteristics: $V_{DD}=4.5V$, $C_L=.2pF$

Logic Macro	Parameter	$T_A=25°C$	$T_A=70°C$	Units
Inverter	tpd	1.7	2.5	Ns
2-In NAND	tpd	2.5	4	Ns
D-Flip Flop	Max Frequency	40	25	MHz

$$tpd=\frac{t_{LH}+t_{HL}}{2}$$

Test System	Function	Local Memory	Freq.	Pins
S-600	Digital	1K/Pin	5 MHz	60 I/O
S-II	Digital	2K/Pin	10 MHz	60 I/O
S-VII	Digital	4K/Pin	10 MHz	60 I/O
Sentinel	Digital	4K/Pin	10 MHz	60 I/O
GR-16	Digital	4K/Pin	30 MHz	96/144
		Future Systems		
Series 20	Digital	4K/Pin	20 MHz	120 I/O
GR-16	Digital	4K/Pin	30 MHz	144 I/O

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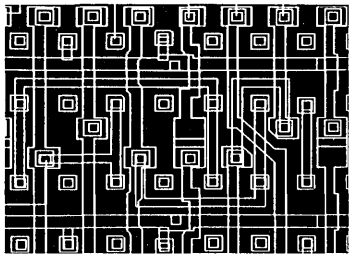

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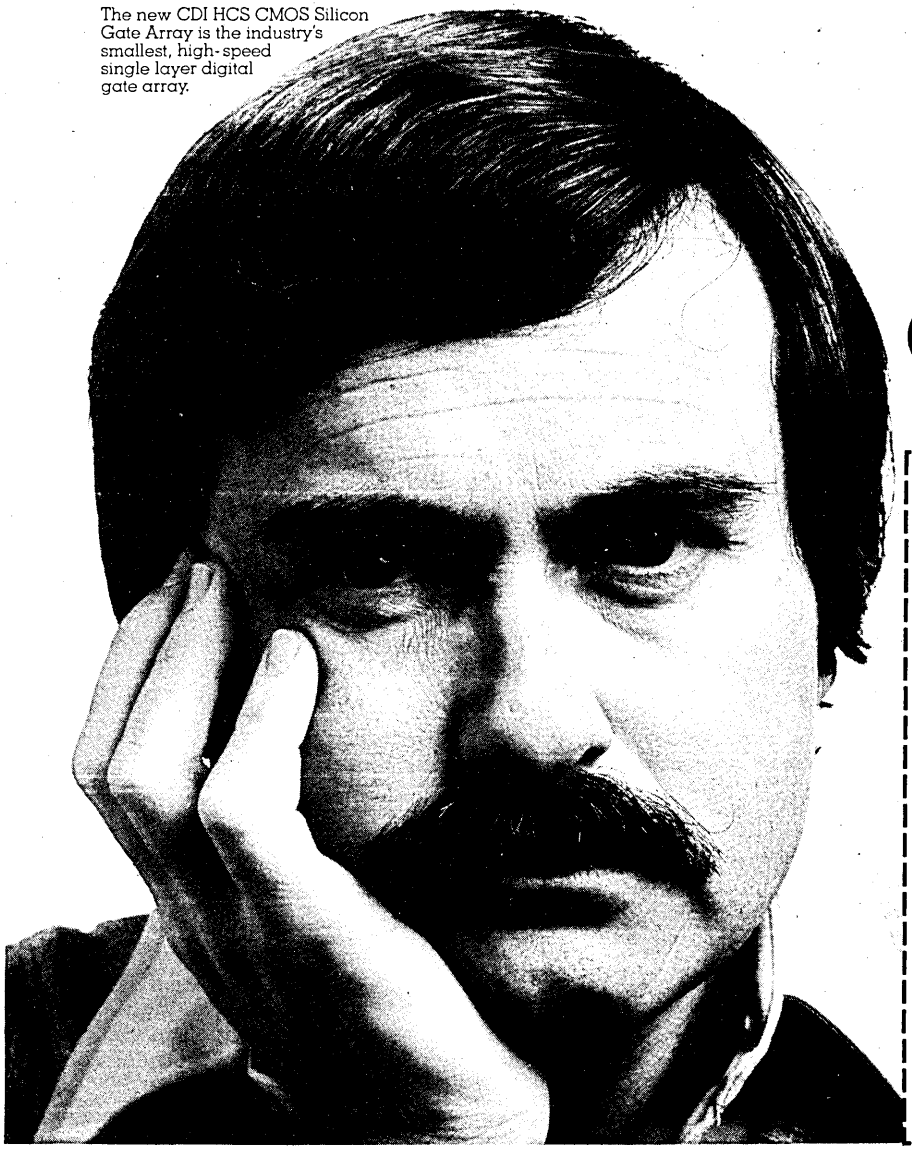

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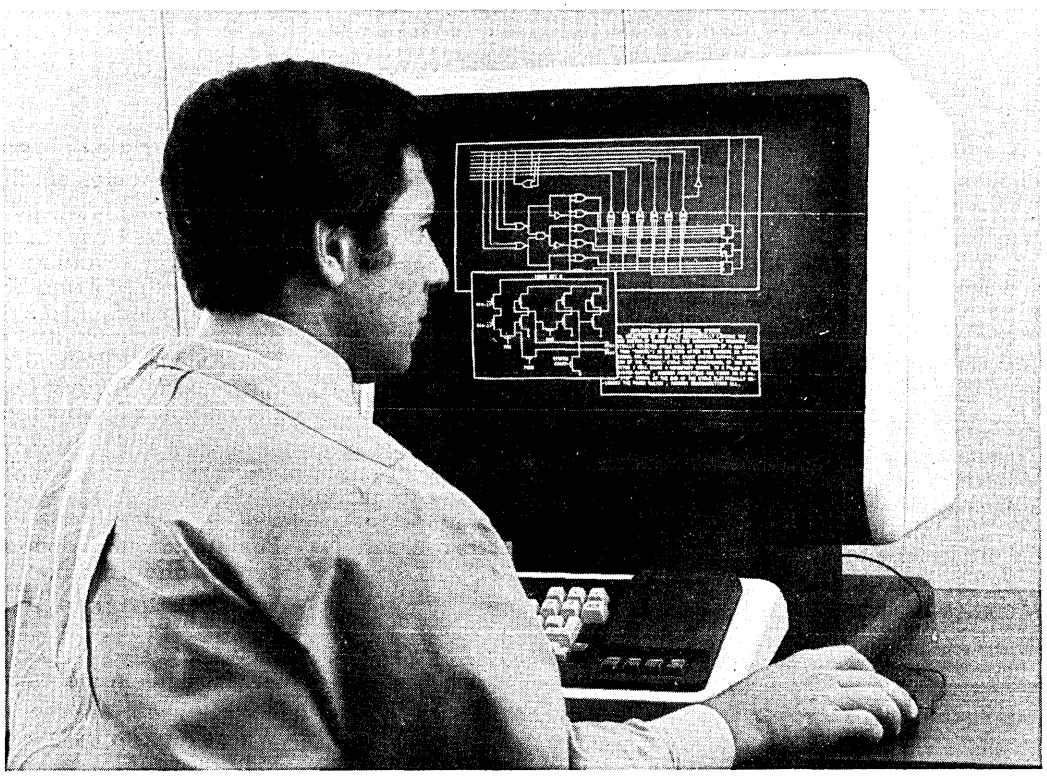
*Applied to purchase of a design

Guiltspur Micro Systems, 74/76 Northbrook Street NEWBURY, BERKS RG 13 1AE, UNITED KINGDOM, TEL: (0635) 45406 Telex: 84 85 07

Neutron GmbH, Berliner Strasse 308, D-6050 OFFENBACH/M, WEST GERMANY, TEL: (0611) 81 39 30 Telex: 4185414

European Operations, California Devices Inc., 53, Rue de Chambourcy, 78300 POISSY, FRANCE, TEL: (3) 074-11-46 Telex: 695477

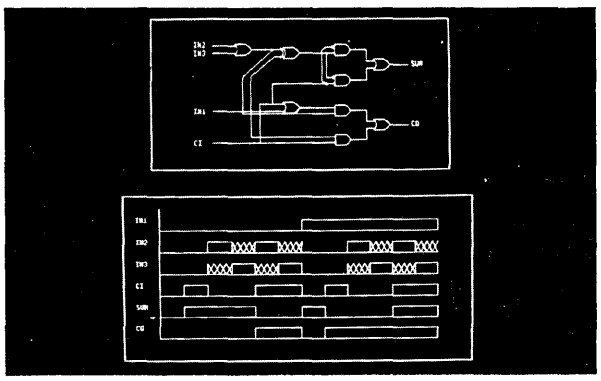


The CAE 2000 Makes Short Work of Your IC Design Problems

Gate Arrays to Full Custom Circuits

It takes the right tools to design an LSI circuit in a reasonable amount of time from conception through circuit design to final chip layout. More importantly, the tool should insure that the circuit works right the first time, eliminating costly revision cycles. That's why Computer Aided Engineering, Inc. developed the CAE 2000, the first system that incorporates all IC development tools in one easy-to-use interactive design station.

Designed for engineers by engineers, the user interface is powerful, yet simple to use. You can give instructions by selecting *Commands From Menus* on the display simply by touching them with a cursor. No need for typing or worrying about syntax. *Using a Simple Graphics Editor*, you quickly generate function, logic and circuit diagrams. The system automatically labels nodes and checks the connections for shorts and opens.



Emulating an electronic lab workbench, the CAE 2000 can function both as a *Programmable Waveform Generator* to generate waveform data for documentation and simulation and as an oscilloscope, allowing you to view the simulation results, scroll in time and expand scales. A high-performance *Timing Verifier* lets you detect timing errors throughout all design phases. *Interactive Simulation*, in real time, validates selected logic sections to locate errors and optimize performance. The CAE 2000 also automatically generates an interface to SPICE for in-depth circuit simulation.

There is more to engineering design than just capturing graphics. With the CAE 2000 design station, you can perform *What-If Analysis* locally instead of passing it to a host computer and waiting for results. You can interactively create electronic spread sheets and analyze power, area, capacitance net values and rise and fall times. An *Online Engineering Notebook* lets you keep track of notes and assumptions throughout the design, interspersing them with complete graphics.

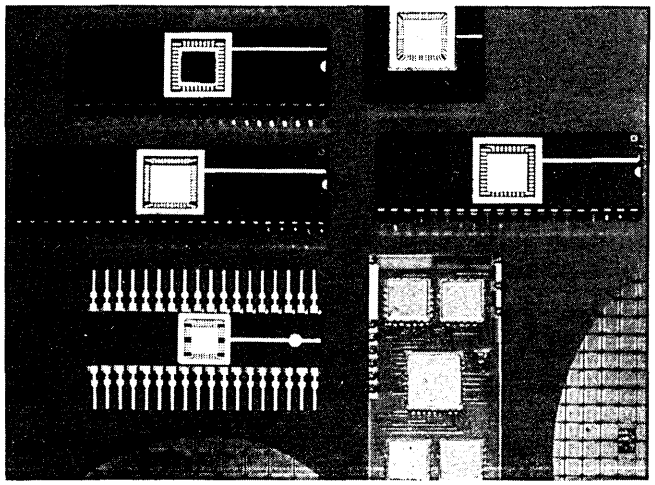
More than a simple workstation, the CAE 2000 is a powerful 32-bit superminicomputer, with up to 3.5M bytes of main memory and up to 158M bytes of Winchester disk. You can start with one design station, then add others as you need, linking them with a 12M bits-per-second local area network. Of course, you may install plotters, printers and mass-storage devices anywhere along the network.

Computer Aided Engineering Inc., 1333 Bordeaux Drive, Sunnyvale, California 94086; (408) 745-1440.

CAE Computer Aided Engineering, Inc.

CUSTOM MOS ARRAYS, INC.

GATE ARRAY FAMILY



BENEFITS

- Fast and inexpensive realization of complex LSI circuits
- High reliability
- Reduced component count
- Reduced size
- Reduced power consumption

TECHNICAL FEATURES

Parameter	CMA 448	CMA 950	CMA 1550
Gate Complexity (2 Inputs)	448 plus 40 peripheral I/O cells	950 plus 56 peripheral I/O cells	1568 plus 76 peripheral I/O cells
Number of Transistors	1,992	4,144	6,652
Typical Utilization	60 to 80%	60 to 80%	60 to 80%
Operating Supply Voltage	3 to 10 volts	3 to 10 volts	3 to 10 volts
Typical Quiescent Current (25 °C)	10 μA	20 μA	50 μA
Output Drive	TTL "B" Series CMOS	TTL "B" Series CMOS	TTL "B" Series CMOS
Package (DIP or Chip Carrier)	14-pin through 40-pin	24-pin through 48-pin	24-pin through 64-pin
Operating Temperature Range	0 °C to +70 °C (Note 2)	0 °C to +70 °C (Note 2)	0 °C to +70 °C (Note 2)

NOTES:
1. To use all 56 input/output cells, a 64-pin package would be required.
2. Also available in full military temperature range.

AC CHARACTERISTICS

Specified at $V_{DD} = 5V \pm 10\%$, fanout of 2.

Propagation delay (t_{PD}) = $\frac{t_{PLH} + t_{PHI}}{2}$

Macrocell	t_{PD}(nsec)		
	Min.	Typ.[2]	Max.[3]
Inverter		3	8
2-Input NAND		5	12
2-Input NOR		5	14
3-Input NAND		8	20
3-Input NOR		9	24
4-Input NAND		12	25
4-Input NOR		14	32
D Flip-Flop[1]		15	33

NOTES:
1. From clock transition. 2. At $T_A = 25$ °C 3. At $T_A = 70$ °C

CUSTOM MOS ARRAYS, INC.
211 Topaz Street Milpitas, CA 95035 (408) 946-9111 TWX 910-338-2304

Semi-Custom Development

SEMI-CUSTOM BIPOLAR PROGRAM

The Exar bipolar semi-custom design program offers a variety of semi-custom chips to fulfill various application performance requirements and complexities.

These semi-custom chips offer a unique method of manufacturing an almost unlimited variety of custom linear and digital integrated circuits, with greatly reduced cost and development time. Exar makes this possible by stocking wafers that are completely fabricated except for the final process step of device interconnection, which metalizes the selected components together in the required circuit configurations.

Chip Type	Chip Size in Mils	Breakdown Voltage	NPN	PNP	JFET's
A100	73 x 83	20V	60	18	
B100	85 x 85	20V	69	12	
C100A	56 x 62	20V	23	8	
D100	80 x 80	36V	50	16*	
E100	80 x 81	20V	48	15	
F100	91 x 110	20V	97	32*	
G100	90 x 90	20V	60	18*	
H100	82 x 92	20V	72	22*	
J100	61 x 65	20V	38	12*	
L100	86 x 105	20V	80	24	
M100	176 x 121	20V	149	52	
U100	**	36V	**	**	**
V100	130 x 100	36V	**	**	**
W100	130 x 160	36V	200	68	8
X100	115 x 95	75V	34	16	

* Dual collector PNP transistors
** Contact Custom Product Application Engineering for more details.

Exar offers a design kit which contains simple instructions and guidelines for designing the metal mask as well as the actual breadboard components (consisting of npn and pnp arrays and integrated resistors), which are representative of the devices available on the semi-custom chips. This provides the design engineer with the ability to closely evaluate his design's performance prior to integrating it on a monolithic chip.

SEMI-CUSTOM I^2L PROGRAM

With the introduction of the I^2L Gate Array chips, Exar has extended its semi-custom design program to the Integrated Injection Logic (I^2L) technology. This unique method of custom LSI development technique now makes it possible to manufacture an almost unlimited variety of digital or analog/digital circuits using I^2L technology, with greatly reduced development cost and time.

I^2L Semi-Custom Chips

Characteristics	CHIP SIZE XR-200	XR-300	XR-400	XR-500
Chip Size (mils)	98 x 119	104 x 146	119 x 156	122 x 185
I^2L Gates	192	288	256	520
Max. Operating Voltage	7V	7V	7V	7V
Bipolar I/O Interfaces	24	28	18	40
Bonding Pads	30	34	40	42

The XR-300 and XR-500 gate arrays are intended primarily for digital LSI designs. The XR-400 gate array features the advantage of combining analog and digital functions on the same IC chip. These I^2L gate array chips are customized by three custom mask patterns, which are simultaneously generated from a pencil layout, using Exar's unique computerized mask generation technique. In this manner, the chip layout is greatly simplified and gate utilization efficiency is increased.

Exar also offers an I^2L design kit which is intended to familiarize the designer with the basic features of I^2L technology, provides helpful design guidelines in reducing his design concept to breadboard and, finally, the IC layout stage.

TYPICAL FLOW FOR
SEMI-CUSTOM DEVELOPMENT
⇩
BREADBOARD
ANALYSIS
⇩
COMPUTER SIMULATION
FOR WORST CASE ANALYSIS
OR LOGIC SIMULATION
⇩
CHIP PENCIL LAYOUT
⇩
CUSTOMER DATA PACKAGE
SUBMITTAL
⇩
TECHNICAL FEASIBILITY
AND COST PROPOSAL
⇩
CUSTOMER/EXAR
INITIAL DESIGN REVIEW
⇩
MASK TAPING
OR DIGITIZING
FOR CUSTOM METALIZATION
⇩
MASK TOOLING
⇩
PROTOTYPE WAFER
FABRICATION
⇩
PROTOTYPE ASSEMBLY
AND EVALUATION

Semi-Custom Development

SEMI-CUSTOM CMOS PROGRAMS

Metal Gate CMOS

Exar now offers two families of CMOS Gate Arrays. The first family consists of four chips featuring from 112 to 544 uncommitted logic gates, fabricated with 7.5μ metal gate technology.

CMOS Master-Chips

Chip Type	CMOS Gates	I/O Cells	Bonding Pads
XR-CMA	112	29	32
XR-CMB	162	34	38
XR-CMC	216	40	44
XR-CMD	544	46	53

A CMOS design kit is also available to familiarize the designer with the basic features of CMOS technology and to assist in the breadboarding layout of the IC chip.

Silicon Gate CMOS

The newest family of semi-custom Master-Chips to be added to Exar's product line is a series of four silicon gate arrays (4μ channel length drawn approximately 3μ actual) and range in size from 500 gates to 1600 gates. These devices feature dual layer metal and an extensive library of standard cells. Please contact Exar Custom Product Applications Engineering for more information.

ECONOMICS OF SEMI-CUSTOM

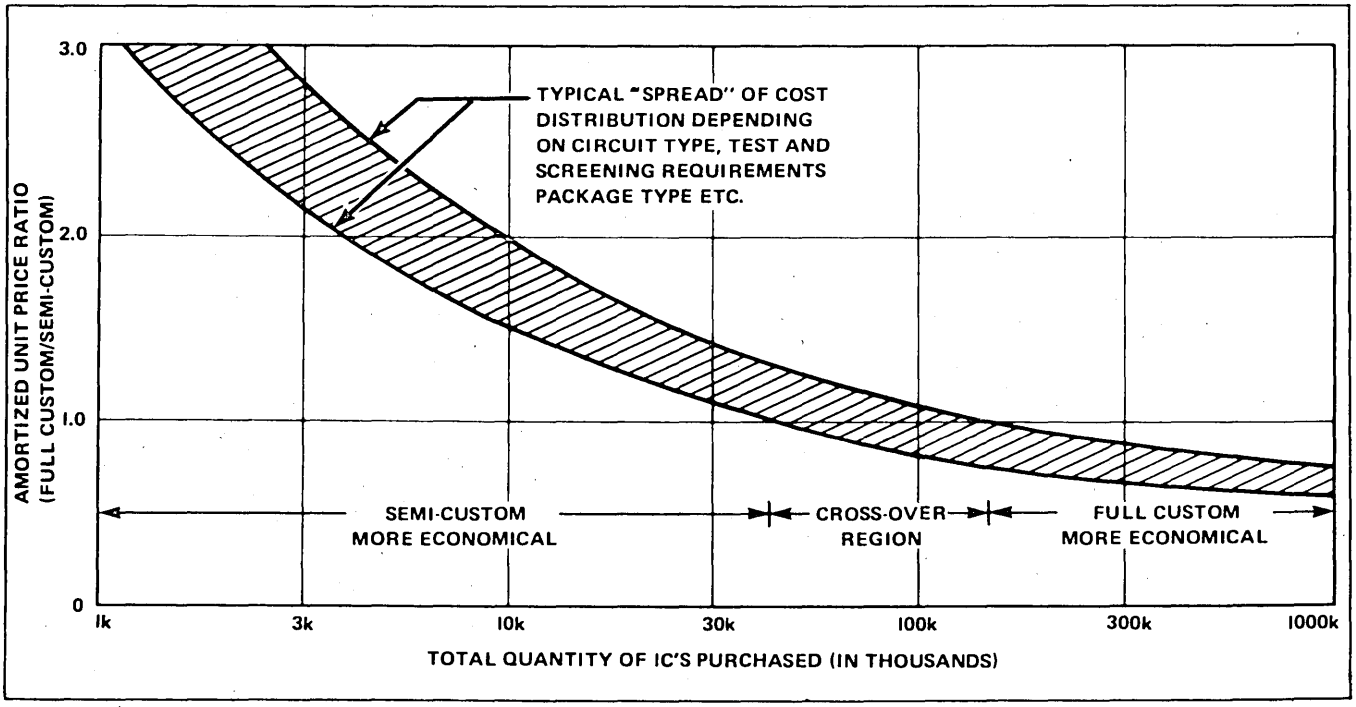
As the Amortized Unit Price Ratio graph in the figure below indicates, for production runs of 50,000 units or less, development costs are a significant influence, and a semi-custom program is clearly the best option. Over 150,000 pieces, production costs become the most important factor, and you are better off with a full custom chip.

Converting Semi-Custom To Full Custom

When production levels get closer to 150,000 units, converting from semi-custom to full custom is most cost effective. The conversion is simple and you get the lower production cost advantages of full custom without giving up the development benefits of semi-custom. In addition, the semi-custom prototypes often serve as a monolithic breadboard to optimize and debug the final design. The actual conversion is a relayout, rather than a redesign. The unused undedicated components are eliminated, and the circuit is laid out on a smaller chip.

Cost Savings Of Two-Step Conversion

Semi-custom design requires only 10-20% of the full custom development costs. Conversion from semi-custom to full custom costs about 50% of the total cost of full custom development. Therefore, the total development costs of the two-step conversion are only 60-70% of a complete full custom program.

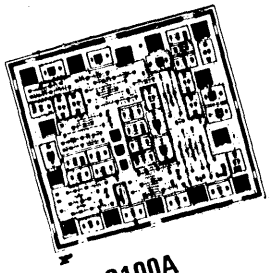


Typical Cost vs. Quantity Comparison of Full Custom and Semi-Custom Designs

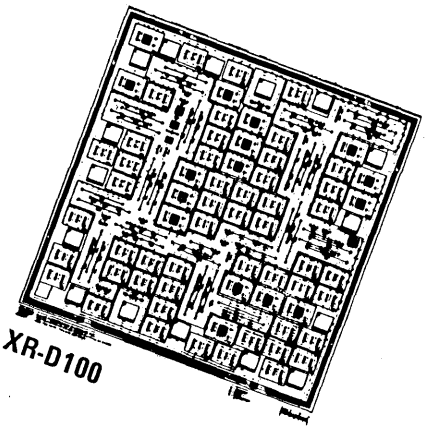
EXAR Integrated Systems, Inc., 750 Palomar Ave., Sunnyvale, CA 94086 * (408) 732-7970

EXAR

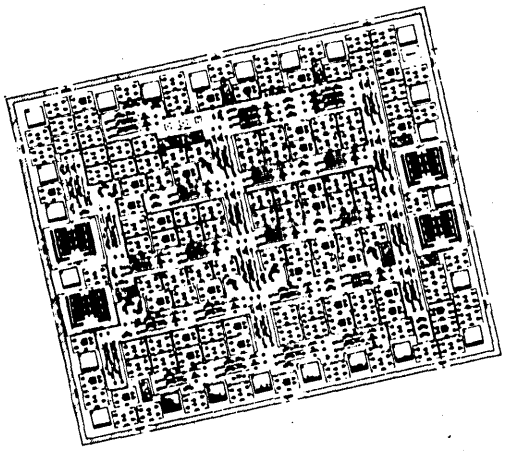
Semi-Custom Arrays



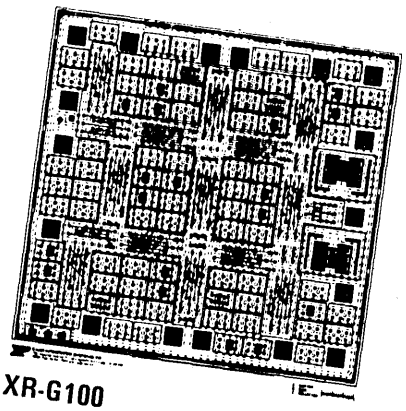
XR-C100A



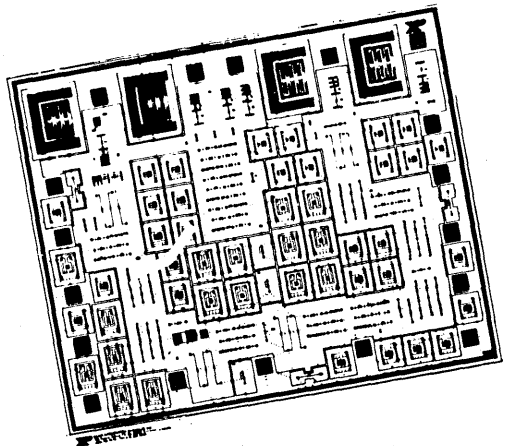
XR-D100



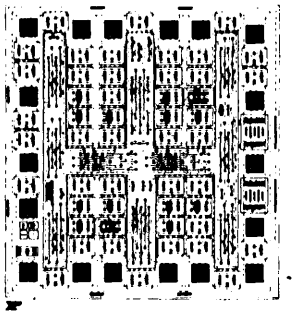
XR-F100



XR-G100



XR-X100



XR-J100

. . . . . Just a few of the many Semi-Custom Arrays available from Exar.

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Full Custom Development

Exar offers a complete design and production capability for full custom IC development, using Exar's bipolar, I^2L, and CMOS technologies. This provides an excellent complement to Exar's unique semi-custom capability.

Exar's full custom IC development and production capabilities offer complete flexibility to meet changing customer needs or design problems. We can develop a complete custom IC starting from your black box specifications, or reduce your working breadboard prototype to a monolithic chip. Alternately, if you have the facilities and resourses to do the IC design and layout, Exar will provide you with the device characteristics and IC layout rules for the particular process suitable to your design, and review your IC layout for you. Then, Exar can generate the IC tooling and fabricate your IC prototypes for you.

WAFER FOUNDARY SERVICE

Exar's bipolar process technology is compatible with the manufacturing processes available from many of the other IC manufacturers. Thus, if you have developed a set of IC tooling with another manufacturer and would like an alternate (or substitute) supplier for your custom IC product, in most cases the existing IC tooling will be directly compatible with Exar's technology.

Exar's Engineering department has two custom IC design groups dedicated to the development of linear and digital custom LSI. We pride ourselves in our flexibility and quick response to your needs.

CONVERTING SEMI-CUSTOM TO FULL CUSTOM

Exar offers the unique ability to start a program using a combination of semi-custom bipolar and/or I^2L, and CMOS arrays, during the early phases of a customer's product, taking full advantage of the low tooling cost and short development cycle. As a customer's product matures, and its market expands, resulting in higher volume production run rates, Exar can convert the multiple semi-custom chip approach into a single custom IC, achieving a cost reduction, and in many cases a performance improvement. The significant advantage of this type of program is that the risk associated with a custom development is greatly reduced; the IC design approach has been proven, production "bugs" are out of your product, and your production line continues to flow during the full custom chip development. Once the custom chip is completely characterized and found acceptable, the semi-custom IC system in your product can be phased-out while the full custom IC is being phased-in.

Exar is the only company that can offer you the advantages of semi-custom and full custom bipolar design programs, because of our complete in-house semiconductor manufacturing capability.

YOUR FIRST STEP

The following technical data package is required in order for Exar to provide you with a firm quotation for your full custom development program:

1. Circuit block diagram with sub-blocks (as necessary).
2. Circuit schematic or logic diagram.
3. Description of circuit operation, and pertinent application information.
4. Preliminary or objective device specification indicating min/max conditions, and limits for the critical parameters (i.e., input/output voltage and current levels, operating frequency, timing diagrams, input/output impedances, power dissipation, etc.).
5. Production requirements and the desired development timetable.

TYPICAL FLOW FOR FULL CUSTOM DEVELOPMENT

⇩

TECHNICAL FEASIBILITY AND COST PROPOSAL

⇩

CUSTOMER/EXAR INITIAL DESIGN REVIEW

⇩

BREADBOARD ANALYSIS

⇩

COMPUTER SIMULATION FOR WORST CASE DESIGN ANALYSIS

⇩

CUSTOMER/EXAR PROPOSED INTEGRATION DESIGN REVIEW

⇩

CHIP ARCHITECTURE DEFINITION

⇩

CHIP DIGITIZING

⇩

PATTERN GENERATION PHOTOMASKING

⇩

PROTOTYPE WAFER FABRICATION

⇩

PROTOTYPE ASSEMBLY

⇩

PROTOTYPE EVALUATION

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FAIRCHILD
A Schlumberger Company

Bipolar Gate Arrays

Fairchild's high performance gate arrays feature a wide range of gate counts and offer minimal circuit delays. The GE1000 and GT0750 series complement the F100K ECL and FAST™ TTL logic families, allowing for easy integration of standard SSI/MSI functions into a unique LSI chip. Designs for all arrays are implemented using pre-defined SSI/MSI functions (macros). Fairchild's complete computer-aided design system, FAIRCAD™, reduces development time and assures first time success.

Product	GE0020	GE0500	GE1000	GE2000	GT0750
Gate Equivalents*	20	500	1000	2000	1000
Internal Technology	ECL	ECL	ECL	ECL	FAST
I/O Levels	100K ECL	100K ECL/ TTL	100K ECL/ TTL	100K ECL/ TTL	TTL
Internal Gate Delay (Typ)	0.35 ns	0.35–0.95 ns	0.35–0.95 ns	0.35–0.95 ns	1.8 ns
Input Buffer Delay (Typ)	N/A	N/A	N/A	N/A	1.5 ns
Output Buffer Delay (Typ)	0.60 ns	0.55 ns	0.55 ns	0.55 ns	3.0 ns
Power Dissipation (Typ)	0.5 W	1.5–4 W	2.5–6 W	4–9 W	1.0 W
I/O	21	72	86	126	76
Packaging	24 F/P	84-pin cc 84-pin grid	96-pin cc 96-pin grid	132-pin cc 132-pin grid	68, 84-pin cc 68, 84-pin grid
CAD Support	✓	✓	✓	✓	✓

*3 — Input NAND Equivalents in Random Logic

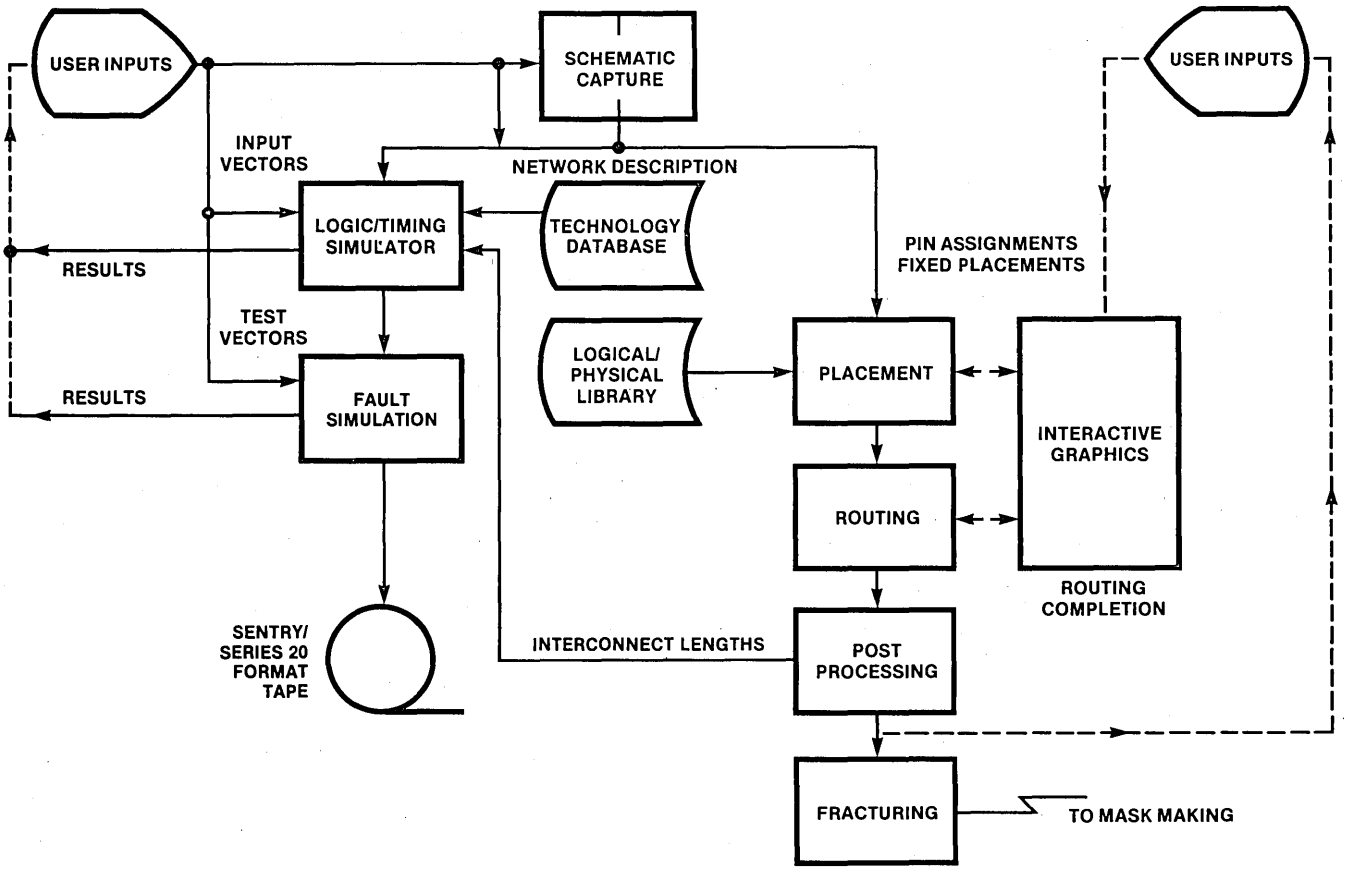
For further information on product availability, CAD training and design schedules write to: Gate Array Marketing, 1801 McCarthy Blvd., Milpitas, CA 95035 or call 408-942-2672.

FAIRCAD Computer-Aided Design System

A user friendly computer-aided design system is employed in all phases of the design cycle to assure fast turnaround times. Major functions performed by the FAIRCAD system include schematic capture, logic and timing simulation, test vector grading, automatic placement and routing and design rules checking. The user's logic description is input either interactively using a graphics workstation or entered in netlist form. Fairchild's FAIRLOGS™ simulator is used to verify array logic and timing. A fault simulator grades the effectiveness of a user supplied test vector sequence. Placement and routing can be highly interactive processes, allowing the user to assign pins and pre-place critical path functions. Automatic routing eliminates tedious manual steps, thereby reducing routing design time from weeks to minutes. Upon routing completion, the circuit is resimulated using actual macro interconnect delays as a final verification of functionality and system performance. Design rules checking insures that process imposed geometry constraints are not violated.

The FAIRCAD system uses a multiple CPU configuration to insure high system availability. Remote access via telephone link is available and additional design centers are being planned worldwide. The FAIRCAD system is product and technology transparent, allowing new gate arrays and technologies to be easily integrated into the system.

FAIRCAD System



Fairchild Camera and Instrument Corporation, Gate Array Division
1801 McCarthy Blvd., Milpitas, California 95035
(408) 942-2672 TWX 910 338 2275

FUJITSU MICROELECTRONICS

TTL GATE ARRAYS

B200 B500 B2000

GENERAL DESCRIPTION

Fujitsu Microelectronics' bipolar gate arrays have many similarities. The B200 and B500 operate on a single 5 volt supply, however, the B2000 requires an additional 2.3V supply. All are LSTTL compatible and both use NAND-type logic. The bipolar gate array family has two layer metallization for gate interconnect, automatic interconnect routing and proven device reliability. They feature DC parametic and DC functional testing as well as AC parametric testing. User defined macros are available to further enhance design versatility.

THE FUJITSU TTL GATE ARRAY FAMILY

DEVICE NAME	B200	B500	B2000
DEVICE NUMBERING	MB14K Series	MB15K Series	MB17K Series
TECHNOLOGY	Low Power Schottky TTL	Low Power Schottky TTL	Low Power Schottky TTL
INTERNAL CELLS	208-3 input NAND	512-3 input NAND	2108-3 input NAND
CELL SPEED	6.5 ns typical	2.2 ns typical	1.5 ns typical
PERIPHERIAL BUFFERS	26 Input, Output or I/O	60 Input, Output or I/O 48 connected outputs max.	112 Input, Output or I/O 72 connected outputs max.
PACKAGING	16, 18, 20, 22, 24, 28-pin DIP	28,40,42,48-pin DIP 64-pin RIT (square)	135-pin RIT (square)
INTERFACE	Logic diagrams and waveform sheets	Logic diagram and formatted test data	Logic diagram and formatted test data
MACRO LIBRARY	54 fully designed; User defined macros allowed	47 fully designed; User defined macros allowed	34 fully designed; User defined macros allowed
TURNAROUND TIME	12 weeks after validation	14 weeks after validation	16 weeks after validation
PRICE	Call Your FMI Sales Office	Call Your FMI Sales Office	Call Your FMI Sales Office

DC AND AC CHARACTERISTICS

	B200	B500	B2000
DC SPECIFICATIONS	Input $V_{IH} = 2.0V$. Input $V_{IL} = 0.8V$. Input $I_{IH} = 20\mu A$. Input $I_{IL} = -0.70mA$	Input $V_{IH} = 2.0V$. Input $V_{IL} = 0.8V$. Input $I_{IH} = 20\mu A$. Input $I_{OL} = -0.25mA$	Input $V_{IH} = 2.0V$. Input $V_{IL} = 0.8V$. Input $I_{IH} = 20\mu A$. Input $I_{OL} = -200\mu A$
	Output $V_{OL} = 0.5V$ Output $V_{OH} = 2.7V$ Output $I_{OZ} = \pm 100\mu A$ Output $I_{OS} = -5$ to $-40mA$	Output $V_{OL} = 0.5V$ Output $V_{OH} = 2.7V$ Output $I_{OZ} = \pm 100\mu A$ Output $I_{OS} = -25$ to $-100mA$	Output $V_{OL} = 0.5V$@8mA Output $V_{OH} = 2.4V$@2.6mA Output $I_{OZ} = \pm 100\mu A$ Output $I_{OS} = -15$ to $-100mA$
AC SPECIFICATIONS	Input Buffer 7.0 ns typical	Input Buffer 3.0 ns typical	Input Buffer 3.5 ns typical (NAND)
	Output Buffer 7.0 ns typical	Output Buffer 6.4 ns typical	Output Buffer 8.5 ns typical (NAND)

For complete data sheets contact: Fujitsu Microelectronics • 2985 Kifer Road • Santa Clara, CA 95051 • (408) 727-1700 • Telex I/II: 910-338-0190

FUJITSU
MICROELECTRONICS

CMOS GATE ARRAYS

C440H
C770(H)
C1275(H)
C2000(H)
C3900(H)
C8000(H)

GENERAL DESCRIPTION

Fujitsu Microelectronics' CMOS gate arrays are alike in many respects. All CMOS arrays are silicon gate, two layer metallization devices. The design geometries are exact therefore all CMOS arrays have the same gate performance. The CMOS gate array macro library is common to all six CMOS devices and contains approximately 100 macro elements to date. The CMOS gate arrays have similar topology with only the number of cells changing.

THE FUJITSU CMOS GATE ARRAY FAMILY

DEVICE NAME	C440H	C770(H)	C1275(H)	C2000(H)	C3900(H)	C8000(H)
DEVICE NUMBERING	MB64HK Series	MB62K Series (MB62HK Series)	MB63K Series (MB63HK Series)	MB60K Series (MB60HK Series)	MB61K Series (MB61HK Series)	MB66VHK Series
INTERNAL CELLS	440-2 input	770-2 input	1275-2 input	2000-2 input	3900-2 input	8000-2 input
CELL SPEED	4.0 nS	5-15 nS	5-15 nS	5-15 nS (4.0 nS)	5-15 nS (4.0 nS)	2.5 nS
PERIPHERIAL BUFFERS	64 I/O pins max.	46 Input Output or I/O, 14 Inputs (70 I/O pins max.)	64 Input Output or I/O (80 I/O pins max.)	72 Input Output or I/O	72 Input Output or I/O	160 Input Output or I/O
PACKAGING	16, 18, 20,22, 24, 28, 40, 42-pin DIP 64-pin RIT (square)	24,28,40,42 48-pin DIP 64-pin RIT (square)	28,40,42 48-pin DIP 64-pin RIT (square)	40,42,48-pin DIP 64-pin RIT	64-pin RIT (square)	135,179-pin RIT (square)
INTERFACE	Logic Diagrams and formatted test data	Logic Diagrams and formatted test data	Logic Diagrams and formatted test data	Logic Diagrams and formatted test data	Logic Diagrams and formatted test data	
TURNAROUND TIME	14-weeks after validation	14-weeks after validation	14-weeks after validation	14-weeks after validation	14-weeks after validation	
PRICE	Call Your FMI Sales Office	Call Your FMI Sales Office	Call Your FMI Sales Office	Call Your FMI Sales Office	Call Your FMI Sales Office	

DC ELECTRICAL CHARACTERISTICS (ALL CMOS ARRAYS)

PARAMETER	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (V_{DD})	4.5	5.0	5.5	V
INPUT HIGH VOLTAGE	2.0	—	V_{DD}	V
INPUT LOW VOLTAGE	V_{SS}	—	0.8	V
OUTPUT HIGH VOLTAGE at I_{OH} = −0.4 mA	2.4	—	—	V
OUTPUT LOW VOLTAGE at I_{OL} = 2.0 mA	—	—	0.4	V

For complete data sheets contact: Fujitsu Microelectronics • 2985 Kifer Road • Santa Clara, CA 95051 • (408) 727-1700 • Telex I/II: 910-338-0190

FUJITSU
MICROELECTRONICS

GATE ARRAY PACKAGE OPTIONS

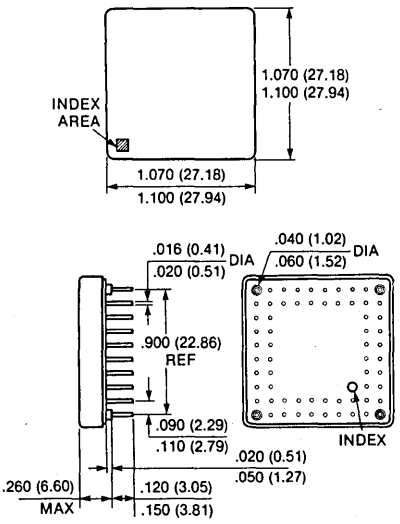
Fujitsu has a wide variety of standard device packaging available for your gate array design as shown below. If you have packaging requirements that are not on this table (Flat Pack, LCC), a Fujitsu applications engineer will be happy to discuss your needs for special packaging.

	DIP-16	DIP-18	DIP-20	DIP-22	DIP-24	DIP-28	DIP-40	DIP-42	DIP-48	DIP-64	RIT-64	RIT-88	RIT-135	RIT-179
B200	● ■	● ■	● ■	● ■	● ■	● ■								
B500						● ■	● ■	● ■	●		●			
B2000													●	
C440	● ■	● ■	● ■	● ■	● ■	● ■	● ■	■			●			
C770					● ■	● ■	● ■	● ■	●	■	●			
C1275						● ■	● ■	● ■	●	■	●			
C2000							●	●	●		●	●		
C3900											●	●		
C8000													●	●

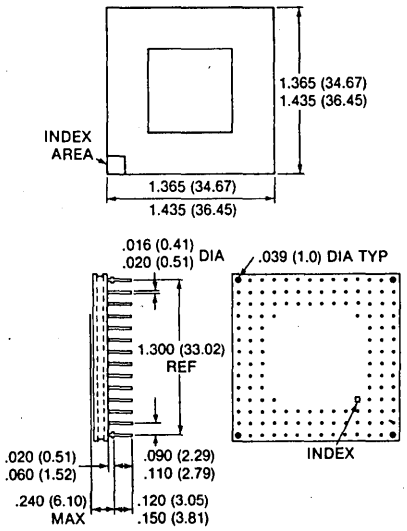
● CERAMIC ■ PLASTIC

(RIT) PIN SQUARE PACKAGE DIMENSIONS Dimensions in inches (millimeters)

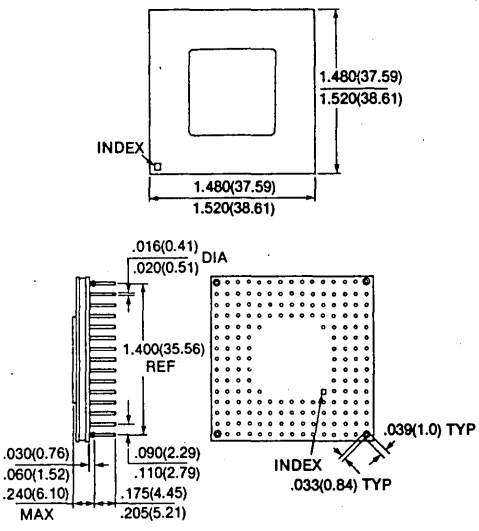
64-PIN SQUARE CERAMIC PACKAGE



135-PIN SQUARE CERAMIC PACKAGE



179-PIN SQUARE CERAMIC PACKAGE



ABOUT FUJITSU MICROELECTRONICS

FUJITSU MICROELECTRONICS, INC.— A U.S. ORGANIZATION

Fujitsu Microelectronics Inc. (FMI) is a U.S. subsidiary of Fujitsu Limited of Tokyo. A California Corporation, FMI is responsible for the marketing and sales of all semiconductor products in North, Central and South America.

Fujitsu Limited manufactures and markets advanced data processing and telecommunications systems, semiconductors and electronic components on a worldwide scale. Fujitsu Limited is ranked as Japan's number one computer manufacturer with sales in the $2 billion range.

A LEADER IN LARGE SCALE LOGIC

Since 1974, Fujitsu Microelectronics has executed over 3,000 gate array designs. Gate arrays from Fujitsu give your designs a significant performance edge. In 1982, we introduced our CMOS device with 8,000 gates and 2.5 ns delay times. Our leadership Schottky TTL gate array is the first with 2,000 gates and 0.95 ns delays. Our leadership ECL arrays, with 400-picosecond delays are the fastest production arrays in the world.

Fujitsu's logic products offer leading edge technology, a complete selection of both bipolar and si-gate CMOS devices; and experience that can serve you through the coming generations of logic products.

ABOUT FUJITSU MICROELECTRONICS

Fujitsu Microelectronics has completed a new assembly and test facility in order to better service our North American customers. The 66,000 square-foot facility is located in Kearny Mesa Industrial Park near downtown San Diego. The building was dedicated in June 1981 and is now fully operational.

HARRIS

HS-3273

CMOS Bus Interface Unit

Mil-Std 1553B Protocol

Bus Interface Circuit Type I

Preliminary

Description

The HS-3273 is an LSI chip for a high performance CMOS Bus Interface Unit (BIU) that is intended to meet the requirements of Mil-Std-1553B. It is fabricated using junction isolated, self-aligned, silicon gate technology. With the HS-3273, an interface can be established whereby a group of up to 31 BIU's help an equal or higher number of hosts transfer information between each other on the serial Manchester data bus.

At the Manchester Bus Interface, the HS-3273 accepts or generates serial bi-phase data. At the host electronics interface, the HS-3273 accepts instruction from the host to transfer parallel data to and from the host. Within a host box, the BIU of which the HS-3273 is a component, resides between a transmitter/receiver unit and the internal parallel data and address busses as shown in Figure 1.

Within Mil-Std 1553B protocol, the BIU's relate to each other as "remotes" and "controller". At any one instant, one BIU is assigned to be the bus controller, all remaining BIU's (up to 30) are assigned as remotes. Provision is made in Mil-Std 1553B and the HS-3273 to allow for dynamic reassignment of these roles.

As a remote, The HS-3273 is first programmed by its host through the use of I/O control transfers. Then as a remote BIU the HS-3273 is capable of carrying out data transfers to and from host memory via Direct Memory Access (DMA). In this situation the BIU is stimulated by command words from the serial data bus. Remote terminal BIU's using the HS-3273 require little assistance from the host to handle serial data bus communications.

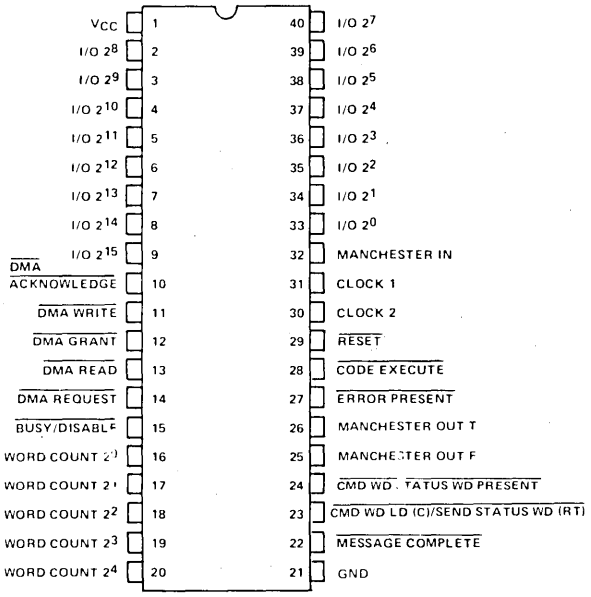
As a controller, the HS-3273 is first programmed by its host as above. After programming, the controller BIU is capable of executing the program code which is stored in host memory. Designs of controller BIU's, using the HS-3273 only, require a higher number of components and host assistance than designs of remote terminal BIU's. A second LSI chip, HS-3274, is presently in conceptual design at Harris. Using the two chips in controller BIU designs will significantly reduce component and host assistance requirements.

Features

- MIL-STD-1553B COMPATIBLE
- UP TO 5 MHz DATA RATE FOR NON MIL-STD-1553B APPLICATIONS
- SERIAL TO PARALLEL RECEIVER DATA CONVERSION
- PARALLEL TO SERIAL TRANSMITTER DATA CONVERSION
- 8/16 BITS HOST I/O INTERFACE
- SINGLE 5 VOLT SUPPLY
- FULL MILITARY TEMPERATURE RANGE

Pinout

TOP VIEW



Specifications

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS

V_{CC} = +5V ± 5%, -55°C ≤ T_A ≤ 125°C

SYMBOL	PARAMETER	MIN	MAX	TEST CONDITIONS
I_{CCOP}	Operating Supply Current		25 mA	V_{CC} = 5.25V, Data Rate = 1 Mbps
V_{IL}	Logic "0" Input Voltage		0.5V	
V_{IH1}	Logic "1" Input Voltage	V_{CC}-1.25V		Except Pins 30, 31, 32
V_{IH2}	Logic "1" Input Voltage	V_{CC}-0.5V		Pins 30, 31, 32
I_{IL1}	Input Leakage Current	-1 μA	1 μA	Pins 15, 28-32
I_{IL2}	Input Current	-3mA	100μA	Pins 2-9, 27, 33-40
I_{IL3}	Input Current	-100μA	10μA	Pins 10, 12
I_{IL4}	Input Current	-10 μA	10 μA	Pin 23
C_I	Input Capacitance		15 pF	
V_{OL}	Logic "0" Output Voltage		0.4V	I_{OL} = 800 μA
V_{OH}	Logic "1" Output Voltage	V_{CC}-0.4V		I_{OH} = -100 μA
f_c	Clock 1 Frequency*		20 MHz	Data Rate = 2 Mbps
f_c	Clock 2 Frequency*		10 MHz	Data Rate = 5 Mbps
t_r,t_f	Output Rise Time, Fall Time		100 ns	Pins 16-20, 22-24 C_L ≤ 50 pF
t_r,t_f	Output Rise Time,** Fall Time		100 ns	Pins 10-14, 27 C_L ≤ 50 pF
t_r,t_f	Output Rise Time,** Fall Time		150 ns	Pins 2-9, 33-40 C_L ≤ 75 pF Data Rate = 5 Mbps
t_r,t_f	Output Rise Time, Fall Time		10 ns	Pins 25, 26 C_L ≤ 25 pF Data Rate = 5 Mbps
t_s	Output Pulse Symmetry	-2 ns	2 ns	Pins 25, 26 $C_L25 = C_L26 \leq 25$ pF
t_{ir},t_{if}	Input Rise Time, Fall Time		25 ns	Pins 30, 31 Data Rate = 5 Mbps

*Input clock duty cycle: 35%-65%, **Hi-Z pull-ups connected internally.

Note: All AC time limits are guaranteed but not tested.

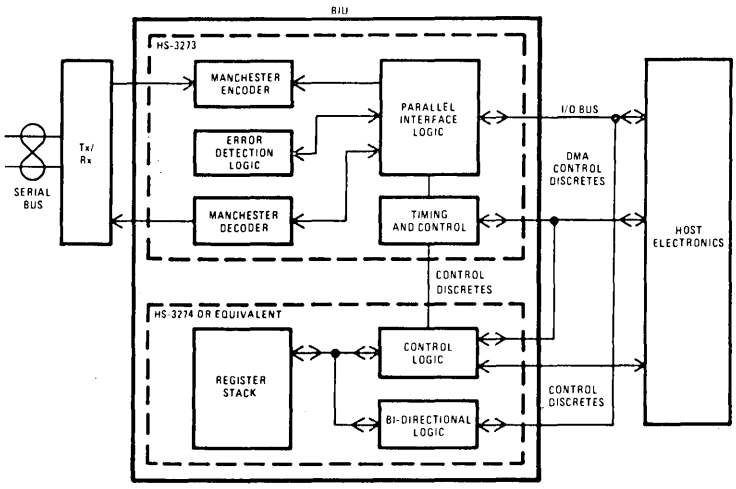


FIGURE 1

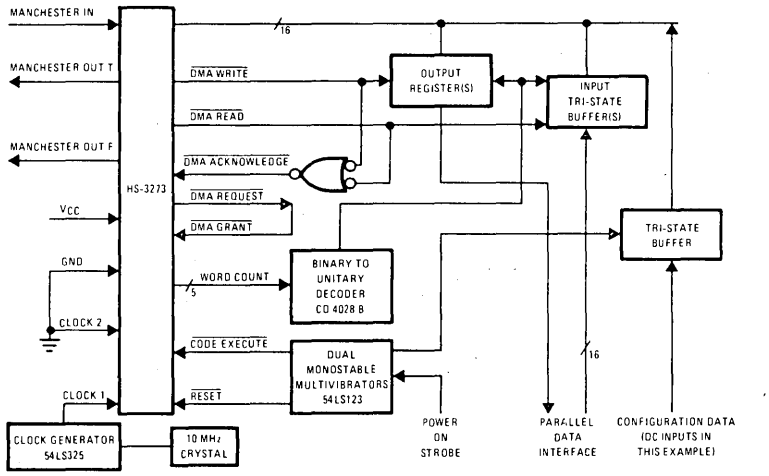


FIGURE 2. SIMPLE REMOTE TERMINAL

HS-3273 - A Simple Remote Terminal

As previously stated, the BIU consists of two LSI circuits, HS-3273 and HS-3274. In the most elemental applications, HS-3273 can be used without HS-3274 to perform the remote terminal function. The basic block diagram of HS-3273 is depicted in Figure 1. Referring to Figure 1, some of the control lines allow for initialization and for transfer of words (command words, status words and error words) through the circuit's I/O interface. The DMA control lines allow for the transfer of data words through the I/O.

Figure 2 illustrates HS-3273 embedded in a host that is functioning as a simple remote terminal. In this configuration, the various logic elements are assumed to be CMOS compatible and connect directly to the HS-3273 device. The application is set up with output registers ready to accept data from the HS-3273 when it outputs data on its I/O bus. Data is supplied to the HS-3273 I/O bus when requested through input tri-state buffers. The flow of data is controlled by word count decodes and the $\overline{\text{DMA READ}}$ and $\overline{\text{DMA WRITE}}$ lines. The binary-to-unitary decoder (CD4028B) converts the word count into discrete lines which select both an input tri-state buffer and an output register. Input or output is then determined by an active $\overline{\text{DMA READ}}$ or active $\overline{\text{DMA WRITE}}$. To satisfy the DMA handshake requirements in this case, a $\overline{\text{DMA REQUEST}}$ is fed into the $\overline{\text{DMA GRANT}}$ input and the "OR" of $\overline{\text{DMA WRITE}}$ or $\overline{\text{DMA READ}}$ is fed into the $\overline{\text{DMA ACKNOWLEDGE}}$ input. Initialization is satisfied by sending the HS-3273 configuration information through a separate tri-state buffer. Initialization occurs when the $\overline{\text{RESET}}$ line is pulsed and followed by the $\overline{\text{CODE EXECUTE}}$ line going active with the 2^0 bit of the I/O bus set high. Under these conditions the HS-3273 treats I/O bits 2^{15}-2^1 as configuration data. This data includes mode information (8-bit/16-bit and controller/remote), box address, bus-accept status and manchester input configuration control. The system PWR ON STROBE can be used to enable passage of configuration data to the HS-3273 and can be used to generate the $\overline{\text{RESET}}$ and $\overline{\text{CODE EXECUTE}}$ signals as shown.

HS-3273 Pin Function List

PIN	FUNCTION
1	V_{CC} - Power Supply Pin = +5V ± 5%
2	I/O 2^8 - Bidirectional data bus utilized for command and data transfer between the host electronics including HS-3274 or equivalent and HS-3273.
3	I/O 2^9 - Bidirectional data bus utilized for command and data transfer between the host electronics including HS-3274 or equivalent and HS-3273.
4	I/O 2^{10} - Bidirectional data bus utilized for command and data transfer between the host electronics including HS-3274 or equivalent and HS-3273.
5	I/O 2^{11} - Bidirectional data bus utilized for command and data transfer between the host electronics including HS-3274 or equivalent and HS-3273.
6	I/O 2^{12} - Bidirectional data bus utilized for command and data transfer between the host electronics including HS-3274 or equivalent and HS-3273.
7	I/O 2^{13} - Bidirectional data bus utilized for command and data transfer between the host electronics including HS-3274 or equivalent and HS-3273.
8	I/O 2^{14} - Bidrectional data bus utilized for command and data transfer between the host electronics including HS-3274 or equivalent and HS-3273.
9	I/O 2^{15} - Bidirectional data bus utilized for command and data transfer between the host electronics including HS-3274 or equivalent and HS-3273.
10	$\overline{\text{DMA ACKNOWLEDGE}}$ - Input from host electronics indicating that a DMA write cycle has been completed or during a read cycle, that data for the BIU is present on the I/O bus.
11	$\overline{\text{DMA WRITE}}$ - Output to host electronics issued following receipt of $\overline{\text{DMA GRANT}}$ indicating that the I/O bus contains data to be written to memory.
12	$\overline{\text{DMA GRANT}}$ - Input from host electronics following issuance of $\overline{\text{DMA REQUEST}}$ indicating that the I/O bus is inactive and that the host is ready to proceed with the DMA.
13	$\overline{\text{DMA READ}}$ - Output to host electronics issued following receipt of $\overline{\text{DMA GRANT}}$ indicating that the HS-3273 desires data from its host's memory.
14	$\overline{\text{DMA REQUEST}}$ - Output to host electronics indicating that HS-3273 is ready to perform a DMA transfer.
15	$\overline{\text{BUSY/DISABLE}}$ - Input which indicates to the BIU that the host is busy. This signal inhibits DMA activity within HS-3273; it will also result in setting the busy bit in the status word and only returning the status word if the $\overline{\text{BUSY/DISABLE}}$ line is active during the trailing edge time of $\overline{\text{CMD WD LD (C)/SEND STATUS WD (RT)}}$.
16	WORD COUNT 2^0 - Output and least significant bit of a word indicating the number of DMA cycles required to fulfill a command.
17	WORD COUNT 2^1 - Output and 2^1 bit of a word indicating the number of DMA cycles required to fulfill a command.
18	WORD COUNT 2^2 - Output and 2^2 bit of a word indicating the number of DMA cycles required to fulfill a command.
19	WORD COUNT 2^3 - Output and 2^3 bit of a word indicating the number of DMA cycles required to fulfill a command.
20	WORD COUNT 2^4 - Output and most significant bit of a word indicating the number of DMA cycles required to fulfill a command.
21	GND - Circuit ground.
22	$\overline{\text{MESSAGE COMPLETE}}$ - Output to host electronics indicating completion of transmission onto the serial bus or completion of message reception. Once a message handling process is started, HS-3273 implements the appropriate algorithm and always follows that with a message-complete indication.
23	$\overline{\text{CMD WD LD(C)/SEND STATUS WD(RT)}}$ - Input (in Controller Mode) used to stimulate HS-3273 to accept for transmission a command word present on the 16 bit I/O bus. In the Remote Mode, pin 23 is an output used by HS-3273 to indicate a command word for the terminal being processed; in the Remote Mode, HS-3273 expects to receive status-word-related data (Terminal-Fail flag, subsystem flag and service request) on 16-bit I/O bus bits 2^0, 2^1, 2^2, respectively.
24	$\overline{\text{CMD WD/STATUS WD PRESENT}}$ - Output to host electronics indicating that HS-3273 has presented a command or status word on the I/O bus resulting from reception of the beginning of a message.
25	MANCHESTER OUT T - True encoder output to serial bus transmitter. Held at logic "1" when HS-3273 encoder is inactive.

HS-3273 Pin Function List (Continued)

PIN	FUNCTION
26	MANCHESTER OUT F - False encoder output to serial bus transmitter. Held at logic "1" when HS-3273 is inactive.
27	$\overline{\text{ERROR PRESENT}}$ - Discrete output to host electronics indicating that an error has been detected in a received or transmitted message. During the time when HS-3273 output is active, $\overline{\text{ERROR PRESENT}}$ becomes an input; a "1" or "0" present on pin 27 during the time of the trailing edge of $\overline{\text{CMD WD/STATUS WD PRESENT}}$ will be transferred into the status word's message-error bit position. This feature allows the RT to indicate to the controller that some aspect of the command word just received was invalid.
28	$\overline{\text{CODE EXECUTE}}$ - Input from host electronics which enables the HS-3273 command decoder to accept configuration and/or command data present on the I/O bus. The $\overline{\text{CODE EXECUTE}}$ strobe keys on the state of 2^0 of the I/O bus. When $2^0 = 1$ during the strobe time, the data on the I/O bus is considered to be configuration information (see configuration data format); otherwise, HS-3273 interprets I/O bus bits 2^2 and 2^1 as follows:

2^2	2^1	Function
0	0	HS-3273 reset
0	1	Next message will be RT-to-RT (controller only)
1	0	Output Error Data
1	1	(Not Used)

Note, when the command to "output error data" is issued, HS-3273 will respond with data on its lower byte. The data output will remain stable until the host issues a second $\overline{\text{CODE EXECUTE}}$ strobe. This second strobe (with the host's I/O bus drivers in the high impedance state) will unlatch a flip flop in HS-3273 and cause the HS-3273 lower byte I/O bus drivers to enter the high impedance state.

PIN	FUNCTION
29	$\overline{\text{RESET}}$ - Initializes the HS-3273. HS-3273 is inhibited after receipt of a $\overline{\text{RESET}}$ strobe until HS-3273 is configured by $\overline{\text{CODE EXECUTE}}$ together with appropriate configuration data on the I/O bus.
30	CLOCK 2 - For data rates greater than 2 Mbps, CLOCK 2 is to be an asynchronous clock at 2X data rate. For data rates less than 2 Mbps, CLOCK 2 is to be grounded.
31	CLOCK 1 - For data rates greater than 2Mbps, CLOCK 1 is to be a synchronized 2X clock to MANCHESTER IN. For data rates less than 2 Mbps, CLOCK 1 is to be an asychronous 10X data rate clock.
32	MANCHESTER IN - Input from serial bus received in single-ended bi-phase manchester form.
33	I/O 2^0 - Bidirectional data bus utilized for command and data transfer between the host electronics including HS-3274 or equivalent and HS-3273.
34	I/O 2^1 - Bidirectional data bus utilized for command and data transfer between the host electronics including HS-3274 or equivalent and HS-3273.
35	I/O 2^2 - Bidirectional data bus utilized for command and data transfer between the host electronics including HS-3274 or equivalent and HS-3273.
36	I/O 2^3 - Bidirectional data bus utilized for command and data transfer between the host electronics including HS-3274 or equivalent and HS-3273.
37	I/O 2^4 - Bidirectional data bus utilized for command and data transfer between the host electronics including HS-3274 or equivalent and HS-3273.
38	I/O 2^5 - Bidirectional data bus utilized for command and data transfer between the host electronics including HS-3274 or equivalent and HS-3273.
39	I/O 2^6 - Bidirectional data bus utilized for command and data transfer between the host electronics including HS-3274 or equivalent and HS-3273.
40	I/O 2^7 - Bidirectional data bus utilized for command and data transfer between the host electronics including HS-3274 or equivalent and HS-3273.

HS-3273 Configuration Data Format

I/O 2^0 - 1 says data on other I/O bits is configuration information.

I/O 2^1 - 1 says HS-3273 operates in 16-bit mode;
0 says HS-3273 operates in 8-bit mode.

I/O 2^2 - 1 says HS-3273 internal sampler will be used.
0 says HS-3273 will be supplied with sampled manchester.

I/O 2^3 - 1 says HS-3273 will accept bus control if offered controller terminal function.
0 says HS-3273 refuses controller terminal function.

I/O 2^4 - 1 means RT to RT data is stored.
0 means RT to RT data is not stored.

I/O 2^5 - 1 says HS-3273 is to be a controller terminal.
0 says HS-3273 is to be remote terminal.

I/O 2^6 - Don't care.

I/O 2^7 - Don't care.

I/O 2^8 - 1 says data on the I/O pins is configuration information.

I/O 2^9 - Don't care.

I/O 2^{10} - Don't care.

I/O 2^{11} - Terminal address bit 2^0.

I/O 2^{12} - Terminal address bit 2^1.

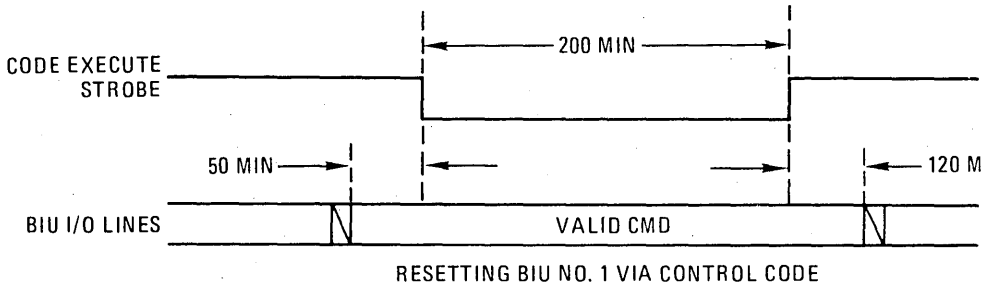
I/O 2^{13} - Terminal address bit 2^2.

I/O 2^{14} - Terminal address bit 2^3.

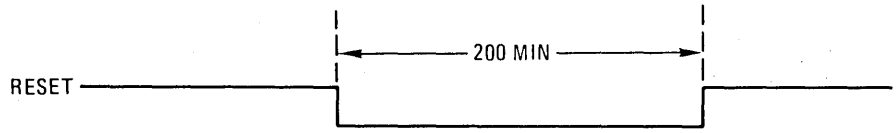
I/O 2^{15} - Terminal address bit 2^4.

NOTE: When operating in the 8-bit mode, the I/O pins in the lower byte must be paired off to the corresponding I/O pins in the upper byte.

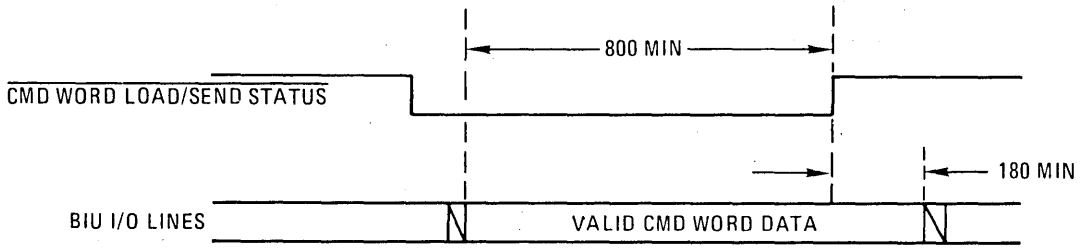
Timing Diagram



RESETTING BIU NO. 1 VIA CONTROL CODE

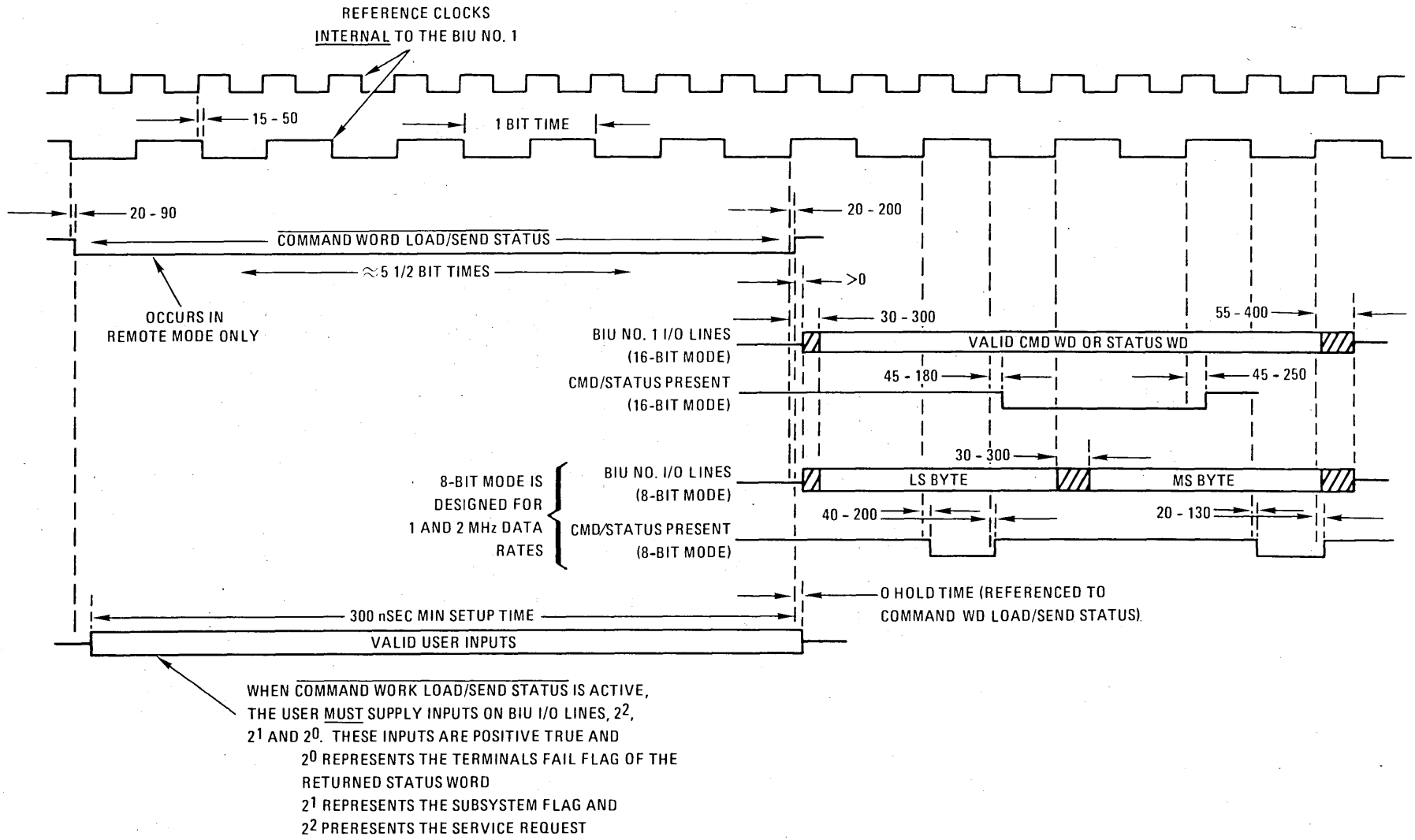


RESET BIU NO. 1 VIA RESET PIN

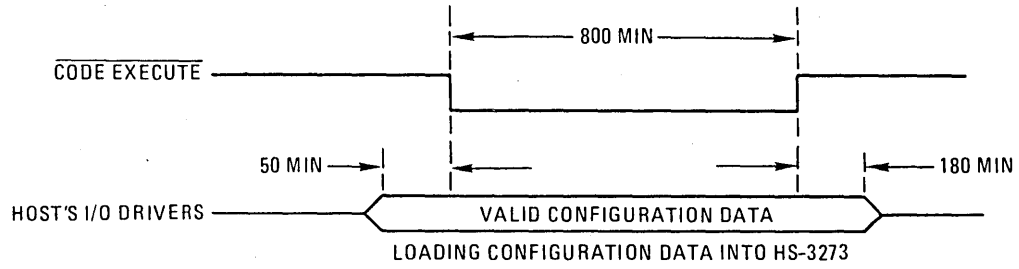


LOADING BIU NO. 1 (AS CONTROLLER) WITH A COMMAND WORD FOR TRANSMISSION

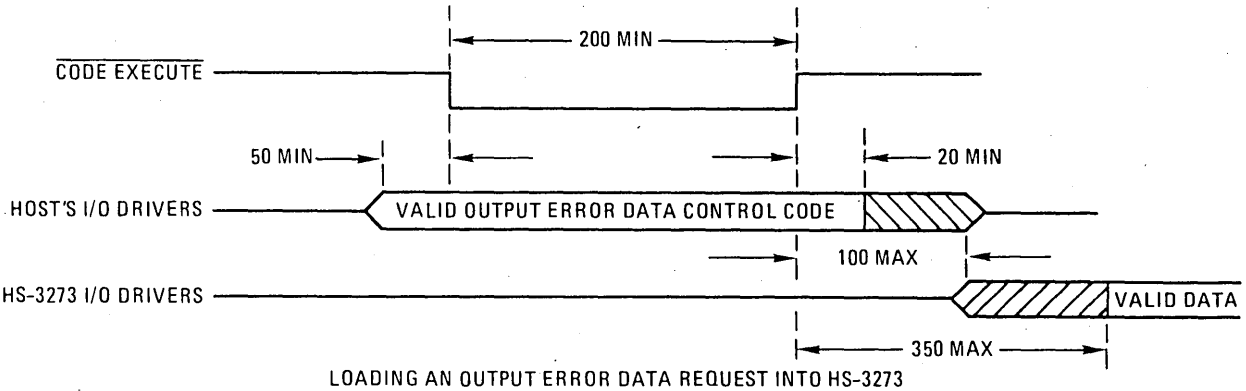
NOTE: ALL TIMES IN nSEC



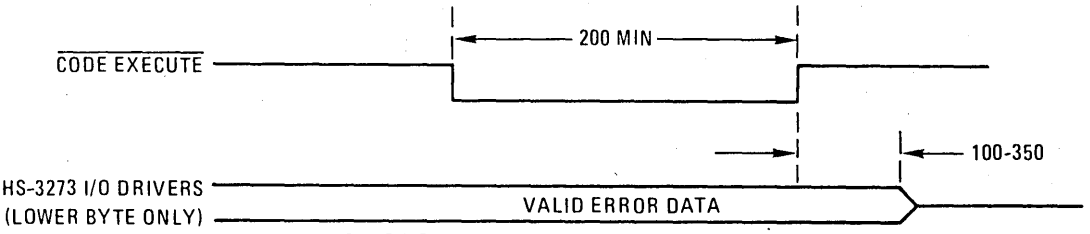
RECEPTION OF A COMMAND WORD (RT) OR STATUS WORD (C)



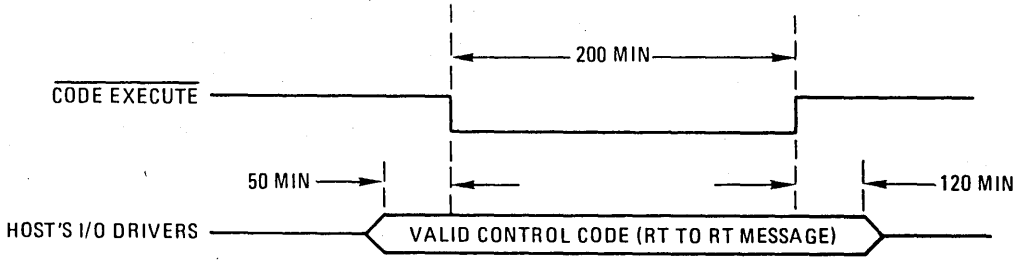
LOADING CONFIGURATION DATA INTO HS-3273



LOADING AN OUTPUT ERROR DATA REQUEST INTO HS-3273

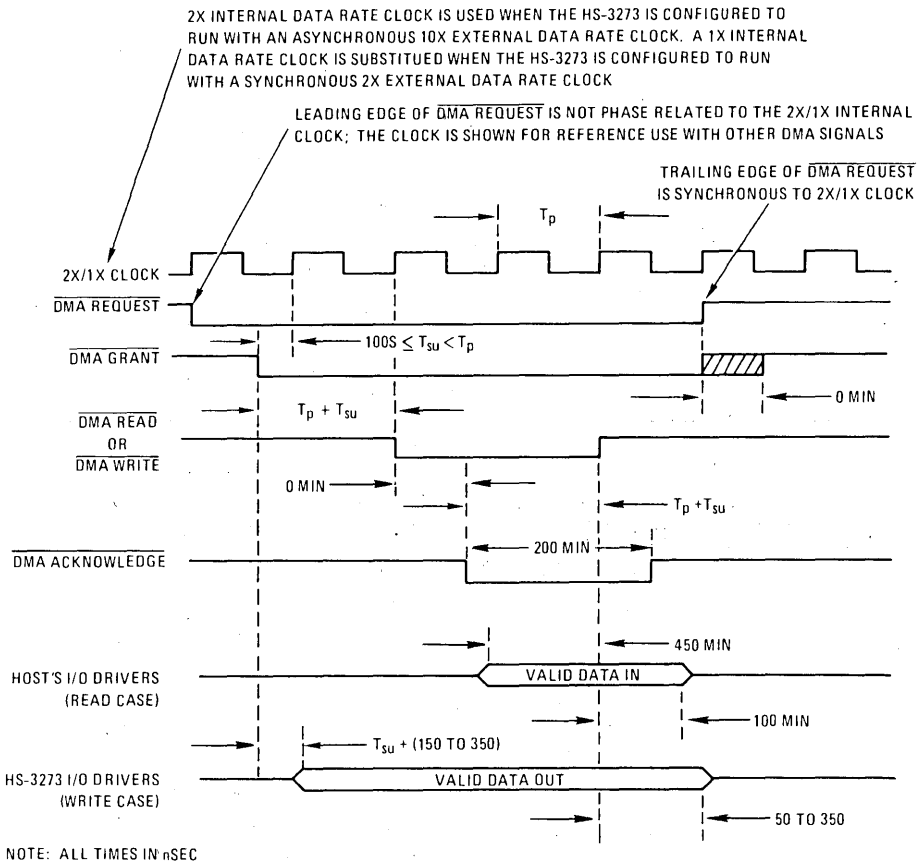


CAUSING THE HS-3273 LOWER BYTE TO ENTER HI-Z STATE
AFTER HOST HAS READ THE HS-3273 ERROR DATA

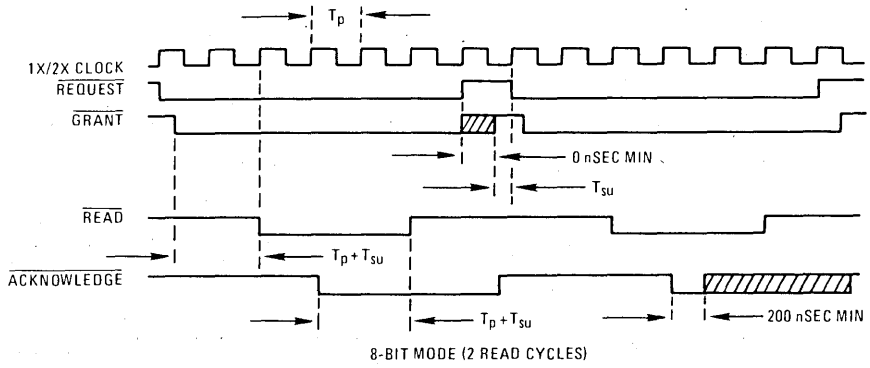


LOADING A "NEXT MESSAGE WILL BE RT-TO-RT"
REQUEST INTO HS-3273

NOTE: ALL TIMES IN NANOSECONDS

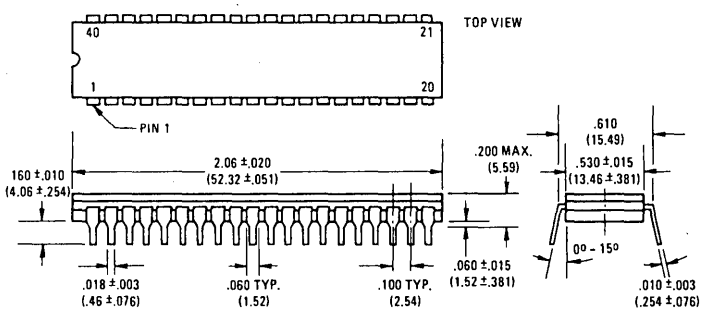


DMA SEQUENCE FOR HS-3273
(CONFIGURED FOR 16-BIT I/O DATA BUS)



DMA CONTROL SEQUENCE FOR BIU NO. 1

Packaging



1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions ± .010 (± 0.25mm) unless otherwise shown.

Test Product Flow

HARRIS SEMICONDUCTOR PRODUCT FLOW
MIL-M-38510/MIL-STD-883, METHOD 5004 CLASS B
100% SCREENING PROCEDURE

	SCREEN	MIL-STD-883 METHOD/COND.
1	Internal Visual	2010 Cond. B.
2	Stabilization Bake	1008 Cond. C (24 hrs. minimum)
3	Temperature Cycling	1010 Cond. C
4	Constant Acceleration	2001 Cond. E, Y1 plane
5	Seal: (A) Fine (B) Gross	1014 Cond. A or B 1014 Cond. C2
6	Initial Electrical	Harris Specifications
7	Burn-In Test	1015, 160 hrs. @ 125°C (or equivalent) (Burn-In circuits enclosed)
8	Final Electrical 100% go-no-go	Tested at Worst Case Operating Conditions
9	External Visual	2009 Sample Inspection

Note: Traceability: All devices are assigned date code identification that provides traceability back to the inspection lot.

Branding: All devices are branded with the part number and EIA date code.

Aged Products: Product that has been held for more than 24 months will be reinspected prior to shipment to group A inspection requirements.

Additional Requirements: Sample Group A electrical tests are performed on a lot acceptance basis.

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HARRIS

CUSTOM INTEGRATED CIRCUITS DIVISION

HS-3182

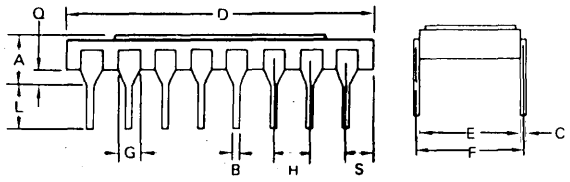
ARINC 429 Bus Interface Line Driver Circuit

Features

- INPUTS T^2L AND CMOS COMPATIBLE
- ADJUSTABLE RISE AND FALL TIMES VIA 2 EXTERNAL CAPACITORS
- PROGRAMMABLE OUTPUT DIFFERENTIAL RANGE VIA VOLTAGE REFERENCE INPUT (V_{REF})
- POWER STROBE INPUT PERMITS LOW QUIESCENT POWER OF < 20mW
- OUTPUTS ARE INHIBITED (0 VOLTS) IF DATA (A) AND DATA (B) INPUTS ARE BOTH IN THE "LOGIC ONE" STATE
- CAN OPERATE UP TO A 100 KILOBITS DATA RATE
- OUTPUT SHORT CIRCUIT PROOF AND CONTAINS OVERVOLTAGE PROTECTION
- DATA "A" AND DATA "B" SIGNALS ARE "AND'D" WITH CLOCK AND SYNC SIGNALS
- FULL MILITARY TEMPERATURE RANGE

Package

16 LEAD BRAZED DIP



LEAD COUNT	DIM A	DIM B	DIM C	DIM D	DIM E	DIM F	DIM G	DIM H	DIM L	DIM Q	DIM S
16	MIN.	.014	.008		.220	.290	.030	.100	.125	.015	
	MAX.	.023	.015	.840	.310	.320	.070	BSC	.200	.060	.060

NOTE: DIMENSIONS IN INCHES

Description

The HS-3182 ARINC 429 bus interface driver circuit is a monolithic dielectrically isolated bipolar differential line driver designed to meet the specifications of ARINC 429. This device is intended to be used with a companion chip, HS-3282 CMOS ARINC bus interface circuit, which provides the data formatting and processor interface function.

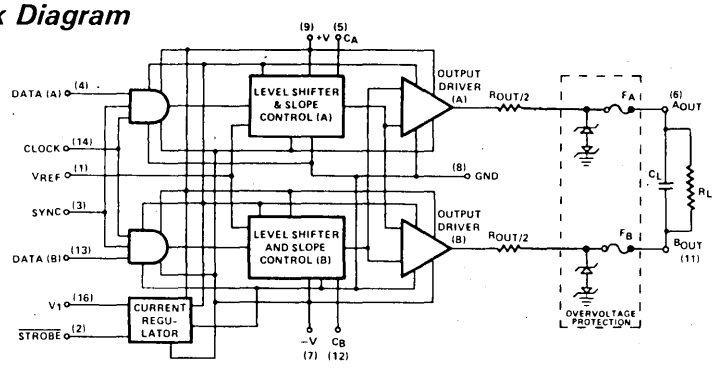
All logic inputs are T^2L and CMOS compatible. In addition to the DATA(A) and DATA(B) inputs there are also inputs for a CLOCK and SYNC signal which are AND'D with the DATA inputs. This feature was added to enhance system performance and to allow the HS-3182 to be used with devices other than the HS-3282. Also adding to system performance is the $\overline{\text{STROBE}}$ input. To minimize power consumption the $\overline{\text{STROBE}}$ input can be asserted to place the chip in the power-down mode where it draws substantially less current. Four power supplies are required; +V = +15V ±10%, -V = -15V ±10%, V_1 = 5V ±5% and V_{REF}. V_{REF} is used to program the output voltage swing, such that V_{OUT} (DIFF) = $\pm 2V_{REF}$. Typically, $V_{REF} = V_1 = 5V \pm 5\%$.

The driver output impedance is 75Ω ±20% at 25°C. Output rise and fall times are programmed through the use of two external capacitors, C_A and C_B. To meet the requirements for rise and fall times as specified in ARINC 429, $C_A = C_B = 75pF$ for the high speed operation (100 KBPS) and 500 pF for the low speed operation (12-14.5 KBPS). The outputs are protected against overvoltage and short circuit as shown in the Block Diagram. This device is designed to operate with a case temperature range of -55°C to +125°C.

Truth Table

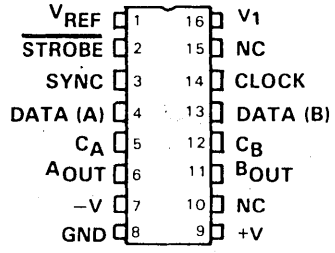
$\overline{\text{STROBE}}$	SYNC	CLOCK	DATA (A)	DATA (B)	A_{OUT}	B_{OUT}	COMMENTS
H	X	X	X	X	HI-Z	HI-Z	Power-Down State
L	X	L	X	X	OV	OV	NULL
L	L	X	X	X	OV	OV	NULL
L	H	H	L	L	OV	OV	NULL
L	H	H	L	H	$-V_{REF}$	$+V_{REF}$	LOW
L	H	H	H	L	$+V_{REF}$	$-V_{REF}$	HIGH
L	H	H	H	H	OV	OV	NULL

Block Diagram



Pinout

TOP VIEW



ABSOLUTE MAXIMUM RATINGS

Voltage Between	
+V and −V terminals	40V
V_1	7V
V_{REF}	6V
Logic Input Voltage	(Gnd − 0.3V) to (V_1 + 0.3V)
Output Short Circuit Duration	See Note 1
Output Overvoltage Protection	See Note 3

OPERATING RANGE

Operating Voltage:	
+V	+15V ± 10%
−V	−15V ± 10%
V1	5V ± 5%
V_{REF} (for ARINC 429)	5V ± 5%
V_{REF} (applications other than ARINC)	0V to 6V
Operating Case Temperature	−55°C to +125°C
Storage Temperature	−65°C to +150°C

ELECTRICAL CHARACTERISTICS

$+V = +15V \pm 10\%$, $-V = -15V \pm 10\%$, $V_1 = V_{REF} = 5V \pm 5\%$
Case Temperature: −55°C to +125°C

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	TEST CONDITION
I_{CCPD} (+V)	Supply Current +V (Power Down)	−475	+10	475	μA	$\overline{STROBE}$ = H
I_{CCPD} (−V)	Supply Current −V (Power Down)	−475	+10	475	μA	$\overline{STROBE}$ = H
I_{CCOP} (+V)	Supply Current +V (Operating)		11	16	mA	No Load (0-100 kBps)
I_{CCOP} (−V)	Supply Current −V (Operating)		−10	−16	mA	No Load (0-100 kBps)
I_{CCOP} (V_1)	Supply Current V_1 (Operating)		600	975	μA	No Load (0-100 kBps)
I_{CCOP} (V_{REF})	Supply Current V_{REF} (Operating)	−1.0	−0.4	−0.15	mA	No Load (0-100 kBps)
V_{IH}	Logic "1" Input Voltage	2.0			V	
V_{IL}	Logic "0" Input Voltage			0.6	V	
V_{OH}	Output Voltage High (Output to ground)	V_{REF} (−250 mV)	V_{REF}	V_{REF} (+250mV)		No Load (0-100 kBps)
V_{OL}	Output Voltage Low (Output to ground)	$-V_{REF}$ (−250mV)	$-V_{REF}$	$-V_{REF}$ (+250mV)		No Load (0-100 kBps)
V_{NULL}	Output Voltage Null	−250	0	+250	mV	No Load (0-100 kBps)
I_{IL}	Input Current (Input Low)		−1	−20	μA	
I_{IH}	Input Current (Input High)		1	10	μA	
I_{OHSC}	Output Short Circuit Current (Output High)	−80	−100		mA	Short to GND
I_{OLSC}	Output Short Circuit Current (Output Low)	80	100		mA	Short to GND
C_{IN}	Input Capacitance			15	pF	
I_{SC} (+V)	Supply Current +V (Short Circuit)			150	mA	Short to GND
I_{SC} (−V)	Supply Current −V (Short Circuit)			−150	mA	Short to GND

NOTES:

① Heat sink may be required for 100KBPS @ +125°C and output short circuit @ +125°C.
Thermal Characteristics: $T_{CASE} = T_{(Junction)} - \Theta_{(Junction\ -\ Case)} P_{(Dissipation)}$.

Where: $T_{(Junction\ Max)} = +175°C$
$\Theta_{(Junction-Case)} = 19.6°C/W$
$\Theta_{(Junction-Ambient)} = 86.5°C/W$

② Full Load for ARINC 429: $R_L = 400\Omega$ and $C_L = 30{,}000pF$ in parallel between A_{OUT} and B_{OUT}. (See Block Diagram).

③ Output Overvoltage Protection: The fuses used for output overvoltage protection may be blown by a fault at each output of greater than ±6.5V relative to GND.

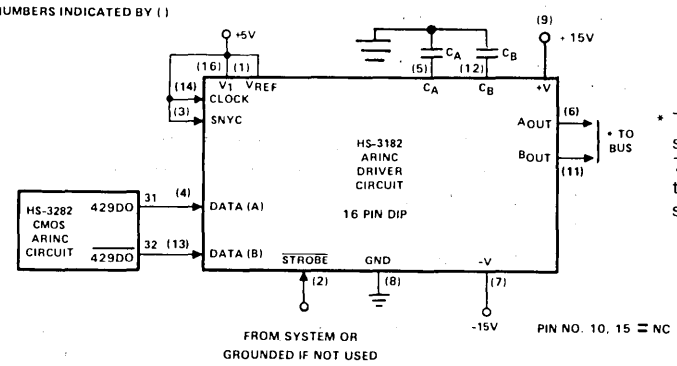
POWER SPECIFICATIONS

NOMINAL POWER @25°C, +V = 15V, −V = −15V, $V_1 = V_{REF} = 5V$

DATA RATE (KBPS)	LOAD	+V	−V	V_1	CHIP POWER	POWER DISSIPATION IN LOAD
0−100	No Load	11 mA	−10 mA	600 μA	325 mW	0
12.5−14	Full Load*	24 mA	−24 mA	600 μA	660 mW	60 mW
100	Full Load*	46 mA	−46 mA	600 μA	1 watt	325 mW

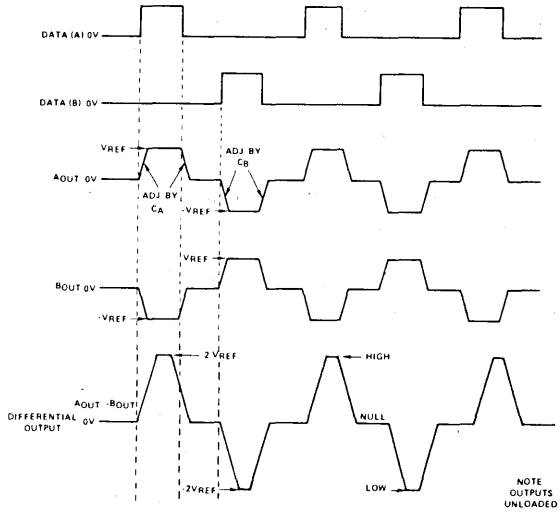
*See Note (2) above.

Typical Application



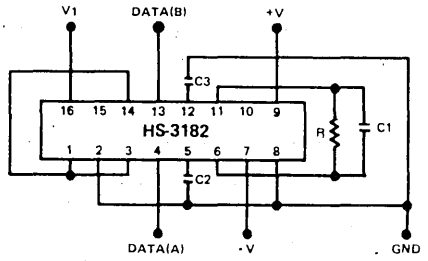
* The rise and fall time of the outputs are set to ARINC specified values by C_A and C_B. Typical $C_A = C_B =$ 75pF for high speed and 500pF for low speed operation. The output HI and low levels are set to ARINC specifications by V_{REF}.

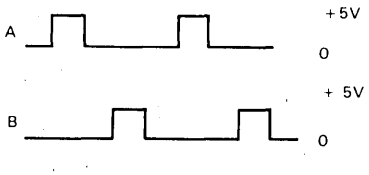
Driver Waveforms



When the Data (A) input is in the Logic One state and the Data (B) input is in the Logic Zero state, A Out is equal to V_{REF} and B Out is equal to $-V_{REF}$:his constitutes the Output High state. Data (A) and Data (B) both in the Logic Zero state causes both A Out and B Out to be equal to 0V which designates the output Null state. Data (A) in the Logic Zero state and Data (B) in the Logic One state cause A Out to be equal to $-V_{REF}$ and B Out to be equal to V_{REF} which is the Output Low state. Both A Out and B Outputs are high impedance when the transmitter is disabled via the power strobe input.

Burn-In Schematic





R = 400Ω, ¼ watt.
C1 = 0.03μF
C2 = C3 = 500 pF, NPO.
+V = +15V ± 10%.
-V = -15V ± 10%.
V_1 = +5V ± 10%.

A 0.01 F decoupling capicitor is required on each of the three supply lines (+V, -V, and V_1) at every 3rd Burn-in socket.

Ambient Temp. Max = +125°C
Package = 16 Lead Brazed Dip
Pulse Conditions =
A & B = 6.25KHz, 25% on & 75% off duty cycle.
B is delayed one-half cycle and in sync with A.

HARRIS SEMICONDUCTOR PRODUCT FLOW
MIL-STD-883, METHOD 5004 CLASS B

100% SCREENING PROCEDURE

	SCREEN	MIL-STD-883 METHOD/COND.
1	Internal Visual	2010 Cond. B.
2	Stabilization Bake	1008 Cond. C (24 hrs. minimum)
3	Temperature Cycling	1010 Cond. C
4	Constant Acceleration	2001 Cond. E; Y1 plane
5	Seal: (A) Fine (B) Gross	1014 Cond. A or B 1014 Cond. C2
6	Initial Electrical	Harris Specifications
7	Burn-In Test	1015, 160 hrs. @ 125°C (or equivalent) (Burn-In circuits enclosed)
8	Final Electrical 100% go-no-go	Tested at Worst Case Operating Conditions
9	External Visual	2009 Sample Inspection

Note:

Traceability: All devices are assigned date code identification that provides traceability back to the inspection lot.

Branding: All devices are branded with the part number and EIA date code.

Aged Products: Product that has been held for more than 24 months will be reinspected prior to shipment to group A inspection requirements.

Additional Requirements: Sample Group A electrical tests are performed on a lot acceptance basis.

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McLean, Virginia 22102
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106 Seventh Street
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(305) 851-9450

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HARRIS

CUSTOM INTEGRATED CIRCUITS DIVISION

HS-3282

CMOS ARINC Bus Interface Circuit

Description

The Harris HS-3282 is a high performance CMOS bus interface circuit that is intended to meet the requirements of ARINC Specification 429, and similar encoded, time multiplexed serial data protocols. The ARINC 429 bus interface circuit consists of two (2) receivers and a transmitter operating independently as shown in Figure 1. The two receivers operate at a frequency that is ten (10) times the receiver data rate, which can be the same or different from the transmitter data rate. Although the two receivers operate at the same frequency, they are functionally independent and each receives serial data asynchronously. The transmitter section of the ARINC bus interface circuit consists mainly of a First-In First-Out (FIFO) memory and timing circuit. The FIFO memory is used to hold eight (8) ARINC data words for transmission serially. The timing circuit is used to correctly separate each ARINC word as required by ARINC Specification 429.

Even though ARINC Specification 429 specifies a 32-bit word, including parity, the HS-3282 can be programmed to also operate with a word length of 25 bits. The incoming receiver data word parity is checked, and a parity status is stored in the receiver latch and is outputted on Pin BD08 during the 1st word. [A logic "0" indicates that an odd number of logic "1"s were received and stored; a logic "1" indicates that an even number of logic "1"s were received and stored]. In the transmitter the parity generator will generate either odd or even parity depending upon the status of PARCK control signal. A logic "0" on BD12 will cause odd parity to be generated and inputted to the output data stream. Conversely, a logic "1" on BD12 will result in the generation of even parity that will be inputted to the output data stream.

More versatility is provided in both the transmitter and receiver by the addition of an external TTL clock input allowing the bus interface circuit to operate at data rates from 0 to 1 megabits. The TTL external clock must be ten (10) times the data rate to insure no data ambiguity.

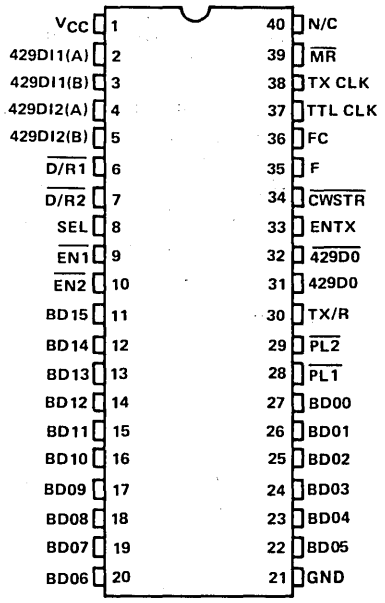
The ARINC bus interface circuit is fully guaranteed to support the data rates of ARINC specification 429 over both the voltage (± 10%) and full military temperature range. It interfaces with TTL, CMOS or NMOS support circuitry, and uses the standard 5-volt V_{CC} supply.

Features

- ARINC SPECIFICATION 429 COMPATIBLE
- DATA RATES OF 100 KILOBITS OR 12.5 KILOBITS
- SEPARATE RECEIVER AND TRANSMITTER SECTION
- DUAL AND INDEPENDENT RECEIVERS, CONNECTING DIRECTLY TO ARINC BUS
- SERIAL TO PARALLEL RECEIVER DATA CONVERSION
- PARALLEL TO SERIAL TRANSMITTER DATA CONVERSION
- WORD LENGTHS OF 25 OR 32 BITS
- PARITY STATUS OF RECEIVED DATA
- GENERATE PARITY OF TRANSMITTER DATA
- AUTOMATIC WORD GAP TIMER
- SINGLE 5-VOLT SUPPLY
- LOW POWER DISSIPATION
- FULL MILITARY TEMPERATURE RANGE

Pinout

TOP VIEW



ABSOLUTE MAXIMUM RATINGS

Voltage at any Pin (Except 2, 3, 4, & 5)	$-0.3V$ to $V_{CC} + 0.3V$
Voltage at Pins 2, 3, 4, & 5	$-29V$ to $+29V$
Maximum V_{CC}	7.0V
Operating Temperature Range	$-55°C$ to $+125°C$
Storage Temperature	$-65°C$ to $+150°C$

CAUTION: To prevent permanent damage to this device, care should be exercised to insure that the absolute maximum ratings for supply voltages, temperature and voltage or current at any pin is not exceeded during both static and dynamic operation.

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ± 5% TA = Operating Temperature Range

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
	ARINC INPUTS					
V_{IH}	Logic "1" Input Voltage	6.7	10	13	V	Pin 2-3, 4-5
V_{IL}	Logic "0" Input Voltage	−6.7	−10	−13	V	Pin 2-3, 4-5
V_{IN}	Null Input Voltage	−2.5	0	+2.5	V	
V_{CH}	Common Mode V			±5	V	
I_{IH}	Input Leakage	75	135	200	μA	$V_{IN} = V_{CC}$
I_{IL}	Input Leakage	−200	−325	−450	μA	$V_{IN} = 0$
R_I	Differential Input Impedance	6			KΩ	
R_H	Input Impedance to V_{CC}	12			KΩ	
R_G	Input Impedance to GND	12			KΩ	
C_I	Differential Input Capacitance*			20	pF	
C_H	Input Capacitance to V_{CC}*			20	pF	
C_G	Input Capacitance to GND*			20	pF	
	BI-DIR. INPUTS					
V_{IH}	Logic "1" Input Voltage	2.1			V	
V_{IL}	Logic "0" Input Voltage			0.7	V	
I_I	Input Leakage	−1.5		−1.5	μA	$0 < V_{IN} < V_{CC}$
	ALL OTHER INPUTS					
V_{IH}	Logic "1" Input Voltage	3.5			V	
V_{IL}	Logic "0" Input Voltage			0.7	V	
I_{IH}	Input Leakage (Except Pin 36)			10	μA	$V_{IN} = V_{CC}$
	Input Leakage (Pin 36)			50	μA	$V_{IN} = V_{CC}$
I_{IL}	Input Leakage			−10	μA	$V_{IN} = 0$
C_I	Input Capacitance*			15	pF	
	OUTPUTS (Including Bi-directional Outputs)					
V_{OH}	Logic "1" Output	2.7			V	$I_{OH} = -1.5mA$
V_{OL}	Logic "O" Output			0.4	V	$I_{OL} = 1.8mA$
C_O	Output Capacitance*			15	pF	
I_{CC_1}	Supply Current Stand-by			20.0	mA	$V_{CC} = 5.5$, $V_{IN} = 0$
I_{CC_2}	Supply Current Operation			20.0	mA	

*Guaranteed but not tested.

ELECTRICAL CHARACTERISTICS (Continued)

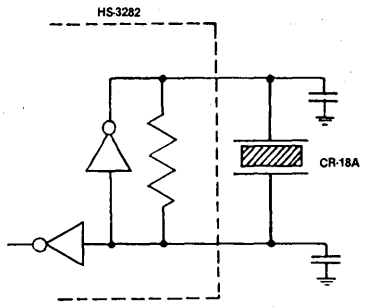
SYMBOL	PARAMETER	DATA RATE = 100 KBFS MIN	DATA RATE = 100 KBFS MAX	DATA RATE = 12.5 KBFS MIN	DATA RATE = 12.5 KBFS MAX	UNITS	TEST CONDITIONS
F_C[1]	Clock Frequency		1		1	MHz	≈50% Duty Cycle
F_D	Data Rate		100		12.5	KHz	
T_{LHC}	TTL Clock Rise Time		10		10	ns	
T_{HLC}	TTL Clock Fall Time		10		10	ns	
T_{MR}	Master Reset Pulse Width	200		200		ns	
	RECEIVER TIMING						
$T_{D/R}$[2]	Receiver Device Ready Time From 32nd Data Bit		16		128	μs	
$T_{D/REN}$	Device Ready to Enable Time	0		0		ns	
T_{EN}	Data Enable Pulse Width	200		200		ns	
T_{ENEN}	Data Enable to Data Enable Time	50		50		ns	
$T_{END/R}$	Data Enable to Device Ready Reset Time		200		200	ns	
T_{ENDATA}	Output Data Valid to Enable Time		200		200	ns	
T_{ENSEL}	Data Enable to Data Select Time	20		20		ns	
T_{SELEN}	Data Select to Data Enable Time	20		20		ns	
T_{DATAEN}	Output Data Disable Time		30		30	ns	
	CONTROL WORD TIMING						
T_{CWSTR}	Control Word Register Strobe Pulse Width	130		130		ns	
T_{CWSET}	Control Word Setup Time	130		130		ns	
T_{CWHLD}	Control Word Hold Time	0		0		ns	
	TRANSMITTER FIFO WRITE TIMING						
T_{PL}	Parallel Load Pulse Width	200		200		ns	
T_{PL12}	Parallel Load 1 to Parallel Load 2 Delay	0		0		ns	
$T_{TX/R}$	Transmitter Ready Delay Time		840		840	ns	
T_{DWSET}	Data Word Setup Time	110		110		ns	
T_{DWHLD}	Data Word Hold Time	0		0		ns	
	TRANSMITTER OUTPUT TIMING						
T_{ENDAT}	Enable Transmit to Output Data Valid Time		25		200	μs	
T_{BIT}	Output Data BIT Time	4.95	5.05	39.6	40.4	μs	
T_{NUL}	Output Data Nul Time	4.95	5.05	39.6	40.4	μs	
$T_{DTX/R}$	Data Transmission Word to TX/R Set Time		50		50	ns	
$T_{ENTX/R}$	Enable Transmit Turn Off Time	0		0		ns	
T_{GAP}	Data Word Gap Time	39.6	40.4	316.8	323.2	μs	
	REPEATER OPERATION TIMING						
T_{ENPL}	Data Enable to Parallel Load Delay Time	0		0		ns	
T_{PLEN}	Data Enable Hold For Parallel Load Time	0		0		ns	
$T_{TX/REN}$	Enable Transmit Delay Time	0		0		ns	

1. 60-40 Duty Cycle Acceptable 2. Same Delay For 25 bit Word Format

Crystal Specifications

PARAMETER	TYPICAL CRYSTAL SPEC
Frequency	1.000 MHz "AT" Cut
Series Resistance (Max)	250Ω
Unwanted Modes	−6.0 dB (Min)
Type of Operation	Parallel
Load Capacitance	32pF ±0.5pf

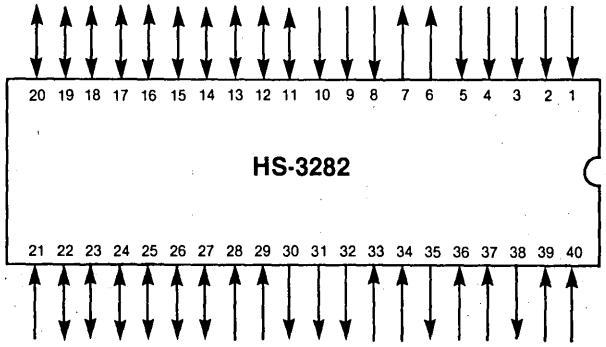
HARRIS RECOMMENDS CRYSTAL CR-18A



Pin Assignments

PIN	SYMBOL	SECTION	DESCRIPTION
1	V_{CC}	Receiver/ Transmitter	Supply pin. 5 volts ±10%.
2	429 DI1 (A)	Receiver	ARINC 429 data input to Receiver 1.
3	429 DI1 (B)	Receiver	ARINC 429 data input to Receiver 1.
4	429 DI2 (A)	Receiver	ARINC 429 data input to Receiver 2.
5	429 DI2 (B)	Receiver	ARINC 429 data input to Receiver 2.
6	$\overline{D/R1}$	Receiver	Device ready flag output from Receiver 1 indicating a valid data word is ready to be fetched.
7	$\overline{D/R2}$	Receiver	Device ready flag output from Receiver 2 indicating a valid data word is ready to be fetched.
8	SEL	Receiver	Bus Data Selector - input signal to select one of two 16-bit words from either Receiver 1 or 2.
9	$\overline{EN1}$	Receiver	Input signal to enable data from Receiver 1 onto the data bus.
10	$\overline{EN2}$	Receiver	Input signal to enable data from Receiver 2 onto the data bus.
11	BD15	Receiver/ Transmitter	Bi-directional data bus for fetching data from either of the Receivers, or for loading data into the Transmitter memory or control word register. See Control Word Table for description of Control Word bits.
12	BD14	Receiver/ Transmitter	See pin 11.
13	BD13	Receiver/ Transmitter	See pin 11.
14	BD12	Receiver/ Transmitter	See pin 11.
15	BD11	Receiver/ Transmitter	See pin 11.
16	BD10	Receiver/ Transmitter	See pin 11.
17	BD09	Receiver/ Transmitter	See pin 11.
18	BD08	Receiver/ Transmitter	See pin 11.
19	BD07	Receiver/ Transmitter	See pin 11.
20	BD06	Receiver/ Transmitter	See pin 11.
21	GND	Receiver/ Transmitter	Circuit ground.
22	BD05	Receiver/ Transmitter	See pin 11.
23	BD04	Receiver/ Transmitter	See pin 11. Control Word function not applicable.
24	BD03	Receiver/ Transmitter	See pin 11. Control Word function not applicable.
25	BD02	Receiver/ Transmitter	See pin 11. Control Word function not applicable.
26	BD01	Receiver/ Transmitter	See pin 11. Control Word function not applicable.
27	BD00	Receiver/ Transmitter	See pin 11. Control Word function not applicable.
28	$\overline{PL1}$	Transmitter	Parallel load input signal loading the first 16-Bit word into the Transmitter memory.

Pinout



PIN	SYMBOL	SECTION	DESCRIPTION
29	$\overline{PL2}$	Transmitter	Parallel load input signal loading the second 16-Bit word into the Transmitter memory and initiates data transfer into the memory stack.
30	TX/R	Transmitter	Transmitter flag output to indicate the memory is empty.
31	429D0	Transmitter	Data output from Transmitter.
32	$\overline{429D0}$	Transmitter	Data output from Transmitter.
33	ENTX	Transmitter	Transmitter Enable Input signal to initiate data transmission from FIFO memory.
34	$\overline{CWSTR}$	Receiver/ Transmitter	Control word input strobe signal to latch the control word from the data bus into the control word register.
35	F	Receiver/ Transmitter	Output of crystal oscillator stage, used to excite crystal. (See Crystal Oscillator). If using TTL clock, this pin should be left open.
36	FC	Receiver/ Transmitter	Input of crystal oscillator stage. (See Crystal Oscillator). If using TTL clock, this pin may be left open or tied low but never tied high.
37	TTLCLK	Receiver/ Transmitter	External clock input. May be either ten (10) or eighty (80) times the data rate. If using both ARINC data rates it must be ten (10) times the highest data rate. (Typically 1 MHz). If using crystal oscillator, this pin may be left open or tied high but never tied low.
38	TXCLK	Transmitter	Transmitter Clock output. Delivers a clock frequency equal to the transmitter data rate.
39	$\overline{MR}$	Receiver/ Transmitter	Master Reset. Active low pulse used to reset FIFO, bit counters, gap timmer, word count signal, TX/R and various other flags and controls. Usually only used on Power-Up or System Reset.
40	—	—	No connection.

Operational Description

The HS-3282 is designed to support ARINC Specification 429 and other serial data protocols that use a similar format by collecting the receiving, transmitting, synchronizing, timing and parity functions on a single, low power LSI circuit. It goes beyond the ARINC requirements of providing for either odd or even parity, and giving the user a choice of either 25 or 32 bit word lengths. The receiver and transmitter sections operate independently of each other. The serial-to-parallel conversion required of the receiver and the parallel-to-serial conversion requirements of the transmitter have been incorporated into the bus interface circuit.

Provisions have been made through the addition of an external TTL clock input to provide data rate flexibility. This requires an external TTL clock that is 10 times the data rate.

To obtain the flexibility discussed above, a number of external control signals are required. To reduce the pin count requirements, an internal control word register is used. The control word is latched from the data bus into the register by the Control Word Strobe ($\overline{CWSTR}$) signal going to a logic "0". Eleven (11) control functions are used, and along with the bus data (BD) line are listed below:

CONTROL WORD

PIN NAME	SYMBOL	FUNCTION
BD05	SLFTST	Connects the self test signal from the transmitter directly to the receiver shift registers, bypassing the input receivers. Receiver 1 receives Data true and Receiver 2 receives Data not. Note that the transmitter output remains active. (Logic "0" on SLFTST Enables Self Test).
BD06	SDENB1	Signal to activate the Source Destination (SD) Decoder for Receiver 1. (Logic "1" activates SD Decoder).
BD07	X1	If SDENB1 = "1" then this bit is compared with ARINC Data Bit #9. If Y1 also matches (see Y1), the word will be accepted by the Receiver 1. If SDENB1 = "0" this bit becomes a don't care.
BD08	Y1	If SDENB1 = "1" then this bit is compared with ARINC Data Bit #10. If X1 also matches (see X1), the word will be accepted by the Receiver 1. If SDENB1 = "0" this bit becomes a don't care.
BD09	SDENB2	Signal to activate the Source Destination (SD) Decoder for Receiver 2. (Logic "1" activates SD Decoder).
BD10	X2	If SDENB2 = "1" then this bit is compared with ARINC Data Bit #9. If Y2 also matches (see Y2), the word will be accepted by the Receiver 2. If SDENB2 = "0" this bit becomes a don't care.
BD11	Y2	If SDENB2 = "1" then this bit is compared with ARINC Data Bit #10. If X2 also matches (see X2), the word will be accepted by the Receiver 2. If SDENB2 = "0" this bit becomes a don't care.
BD12	PARCK	Signal used to invert the transmitter parity bit for test of parity circuits. Logic "0" selects normal odd parity. Logic "1" selects even parity.
BD13	TXSEL	Selects high or low Transmitter data rate. If TXSEL = "0" then transmitter data rate is equal to the clock rate divided by ten (10). If TXSEL = "1" then transmitter data rate is equal to the clock rate divided by eighty (80).
BD14	RCVSEL	Selects high or low Receiver data rate. If RCVSEL = "0" then the received date rate should be equal to the clock rate divided by ten (10). If RCVSEL = "1" then the received data rate should be equal to the clock rate divided by eighty (80).
BD15	WLSEL	Selects word length. If WLSEL = "0" a 32-bit word format will be selected. If WLSEL = "1" a 25-bit word format will be selected.

ARINC 429 DATA FORMAT as input to the Receiver and output from the Transmitter is as follows:

TABLE 1 - ARINC 429 DATA FORMAT

ARINC BIT #	FUNCTIONS
1 - 8	Label
9 - 10	SDI or Data
11	LSB
12 - 27	Data
28	MSB
29	Sign
30, 31	SSM
32	Parity

This format is shuffled when seen on the sixteen bi-directional input/outputs. The format shown below is used from the receivers and input to the transmitter:

TABLE 2 - WORD 1 FORMAT

BIDIRECTIONAL BIT #	FUNCTION	ARINC BIT #
15, 14		13, 12
13	LSB	11
12, 11	SDI or Data	10, 9
10, 9	SSM Status	31, 30
8	Parity	32
7 - 00	Label	1 - 8

TABLE 3 - WORD 2 FORMAT

BIDIRECTIONAL BIT #	FUNCTION	ARINC BIT #
15	Sign	29
14	MSB	28
13 - 00	Data	27 - 14

If the receiver input data word string is broken before the entire data word is received, the receiver will reset and ignore the partially received data word.

If the transmitter is used to transmit consecutive data words, each word will be separated by a four (4) bit "null" state (both positive and negative outputs will maintain a zero (0) volt level).

RECEIVER OPERATION

Since the two receivers are functionally identical, only one will be discussed in detail, and the block diagram will be used for reference in this discussion. The receiver consists of the following circuits:

- The Line Receiver functions as a voltage level translator. It transforms the 10 volt differential line voltage, ARINC 429 format, into 5 volt internal logic level.
- The output of the Line Receiver is one of two inputs to the Self-Test Data Selector (SEL). The other input to the Data Selector is the Self-Test Signal from the Transmitter section.
- The incoming data, either Self-Test or ARINC 429, is double sampled by the Word Gap Timer to generate a Data Clock. The Receiver sample frequency (RCVCLK), 1 MHz, or 125 KHz, is generated by the Receiver/Transmitter Timing Circuit. This sampling frequency is ten times the Data Rate to ensure no data ambiguity.
- The derived data clock then shifts the data down a 32-bit long Data Shift Register (Data S/R1). The Data Word Length is selectable for either 25-Bits or 32-Bits long by the Control Signal (WLSEL). As soon as the data word is completely received, an internal signal (WDCNT1) is generated by the Word Gap Timer Circuit.
- The Source/Destination (S/D) Decoder compares the user set code (X and Y) with Bits 9 and 10 of the Data Word. If the two codes are matched, a positive signal is generated to enable the WDCNT1 signal to latch in the received data. Otherwise, the data word is ignored and no latching action takes place. The S/D Decoder can be Enabled and Disabled by the control signal S/D ENB. If the data word is latched, an indicator flag ($\overline{D/R1}$) is set. This indicates a valid data word is ready to be fetched by the user.
- The parity of the incoming word is checked and the status (i.e., logic "0" for odd parity and logic "1" for even parity) stored in the receiver latch and outputted on BD08 during the Word No. 1.
- Assuming the user desires to access the data, he first sets the Data Select Line (SEL) to a Logic "0" level and pulses the Enable ($\overline{EN1}$) line. This action causes the Data Selector (SEL1) to select the first-data word, which contains the label field and Enable it onto the Data Bus. To obtain the second data word, the user sets the SEL line to a Logic "1" level and pulse the Enable ($\overline{EN1}$) line again. The Enable pulse duration is matched to the user circuit requirement needed to latch in the Data Word from the Data Bus. The second Enable pulse is also used to reset the Device Ready ($\overline{D/R1}$) flip-flop. This completes a receiving cycle.

TRANSMITTER OPERATION

The Transmitter section consists of an 8-word deep by 31-Bit long FIFO Memory, Parity Generator, Transmitter Word Gap Timing Circuit and Driver Circuit.

- The FIFO Memory is organized in such a way that data loaded in the input register is automatically transferred to the output register for Serial Data Transmission. This eliminates a large amount of data managing time since the data need not be clocked from the input register to the output register. The FIFO input register is made up of two sets of 16 D-type flip-flops, which are clocked by the two parallel load signals ($\overline{PL1}$ and $\overline{PL2}$). The data from the Data Bus is clocked into the D-type flip-flop on the positive going edge of the $\overline{PL}$ signals. If the FIFO memory is initially empty, or the stack is not full, the data will be automatically transferred down the Memory Stack and into the output register or to the last empty FIFO storage register. If the

Transmitter Enable signal (ENTX) is not active, a Logic "0", the data remains at the output register. The FIFO Memory has storage locations to hold eight 31-Bit words. If the memory is full and new data is again strobed with $\overline{PL}$, the old data at the input register is written over by the new data. Data will remain in the Memory until ENTX goes to a Logic "1". This activates the FIFO Clock and data is shifted out serially to the Transmitter Driver.

- The Output Register of the FIFO is designed such that it can shift out a word of 25-Bits long or 32-Bits long. This word length is again controlled by the WLSEL bit. The TX Word Gap Timer Circuit also automatically inserts a gap equivalent to 4-Bit Times between each word. This gives a minimum requirement of 29-Bit time or 36-Bit time for each word transmission. Assuming the signal, ENTX, remains at a Logic "1", a transfer to stack signal is generated to transfer the data down the Memory Stack one position. This action is continued until the last word is shifted out of the FIFO memory. At this time a Transmitter Ready (TX/R) flag is generated to signal the user that the Transmitter is ready to receive eight more data words.

- A Bit Counter is used to detect the last Bit shifted out of the FIFO memory and replaces it with the Parity Bit generated by the Parity Generator. The Parity Generator has a control signal, Parity Check (PARCK), which establishes whether odd or even parity is inserted into the output data word. PARCK set to a logic "0" will result in odd parity and when set to a logic "1" will result in even parity.

SAMPLE INTERFACE TECHNIQUE

From Figure 1, one can see that the Data Bus is time shared between the Receiver and the Transmitter. Therefore, bus controlling must be synchronously shared between the Receiver and the Transmitter. Figure 2 shows the typical interface timing control of the ARINC Chip for Receiving function and for Transmitting function. Timing sequence for loading the Transmitter FIFO Memory is shown in Timing Interval A. A Transmitter Ready (TX/R) Flag signals the user that the Transmitter Memory is empty. The user then Enables the Transmitter Data, a 16-Bit word, on the Data Bus and strobes the Transmitter with a Parallel Load ($\overline{PL1}$) Signal. The second part of the 32-Bit word is similarly loaded into the Transmitter with $\overline{PL2}$, which also initiates data transfer to stack. This is continuous until the Memory is full, which is eight 31-Bit words. The user must keep track of the number of words loaded into the Memory to ensure no data is written over by other data. During the time the user is loading the Transmitter, he does not have to service the Receiver, even if the Receiver flags the user with the signal $\overline{D/R1}$ that a valid received word is ready to be fetched. This is shown by the Timing Interval B. If the user decides to obtain the received data before the Transmitter is completely loaded, he sets the two parallel load signals ($\overline{PL1}$ and $\overline{PL2}$) at a Logic "1" state, and strobe $\overline{EN1}$ while the signal SEL is at a Logic "0" state. After the negative edge of $\overline{EN1}$, the first 16-Bit segment of the received word becomes valid on the Data Bus. At the positive edge of $\overline{EN1}$, the user should toggle the signal SEL to ready the Receiver for the second 16-Bit word. Strobing the Receiver with $\overline{EN1}$, the second time, enables the second 16-Bit word and resets the Receiver Ready Flag $\overline{D/R1}$. The user should now reset the signal SEL to a Logic "0" state to ready the Receiver for another Read Cycle. During the time period that the user is fetching the received words, he can load the transmitter. This is done by interlacing the $\overline{PL}$ signals with the $\overline{EN}$ signals as shown in the Timing Interval B. Servicing the Receiver 2 is similar and is illustrated by Timing Interval C. Timing Interval D shows the rest of the Transmitter loading sequence and the beginning of the transmission by switching the signal TX Enable to a Logic "1" state. Timing Interval E is the time it takes to transmit all data from the FIFO Memory, either 288 Bit times or 232 Bit times.

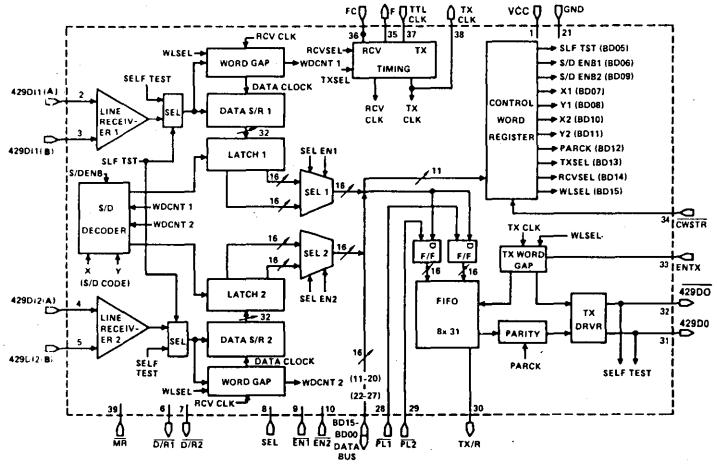


FIGURE 1. SINGLE CHIP ARINC 429 INTERFACE FUNCTIONAL BLOCK DIAGRAM.

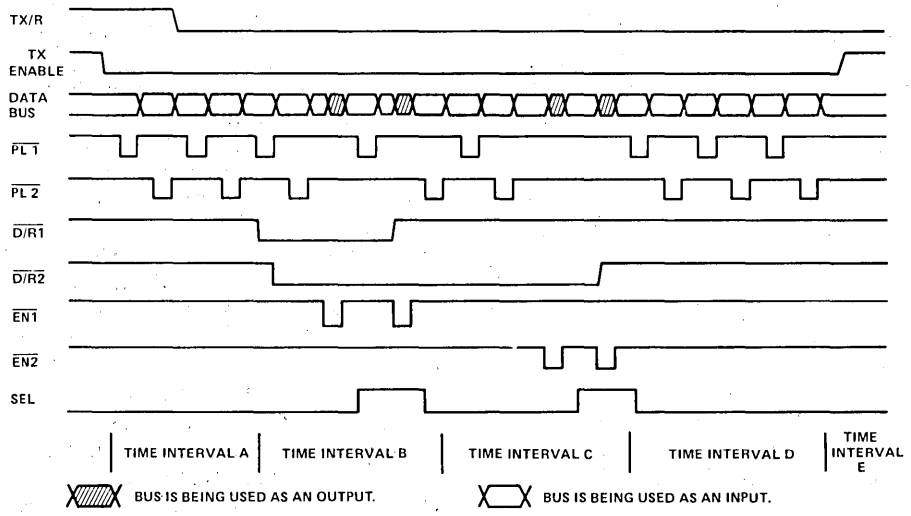


FIGURE 2. TYPICAL INTERFACE TIMING SEQUENCE

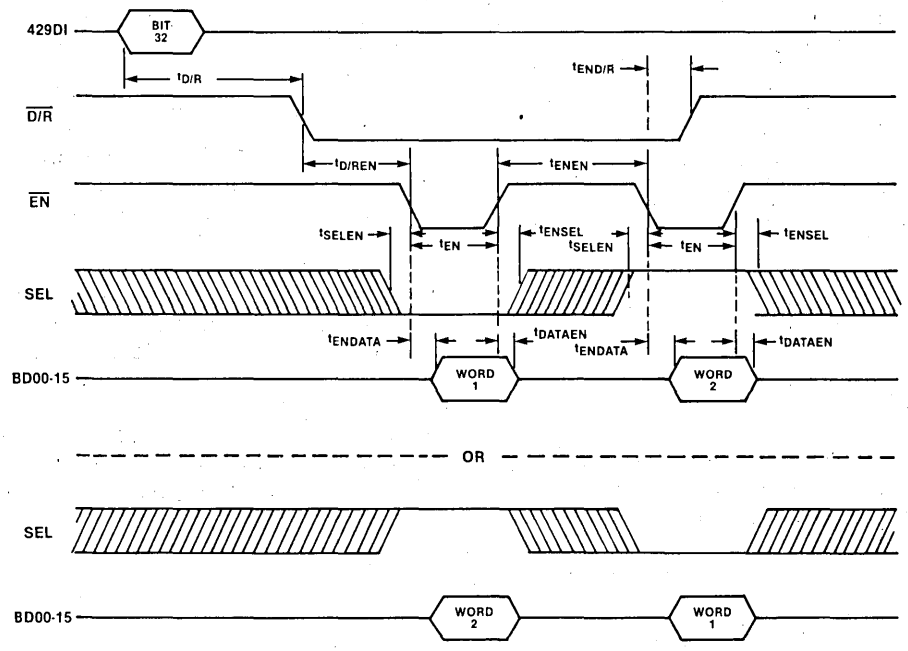


FIGURE 3 RECEIVER TIMING

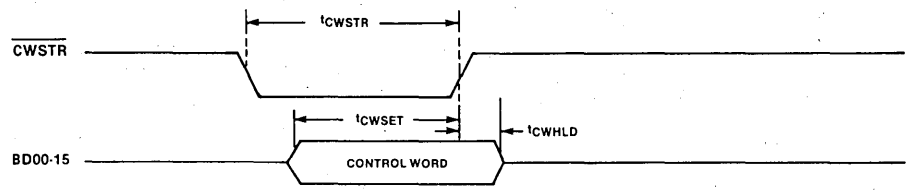


FIGURE 4 CONTROL WORD TIMING

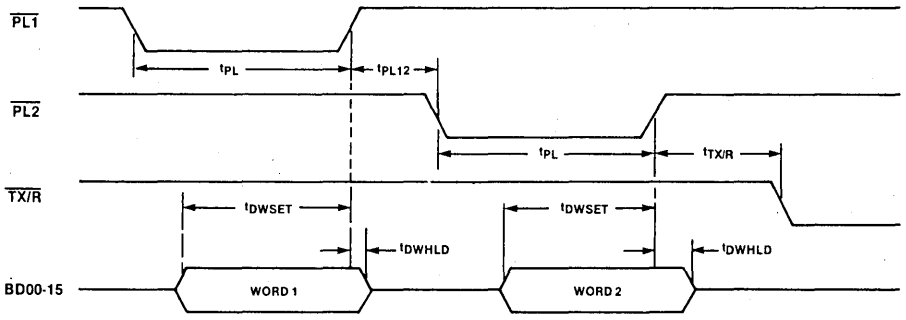


FIGURE 5 TRANSMITTER FIFO WRITE TIMING

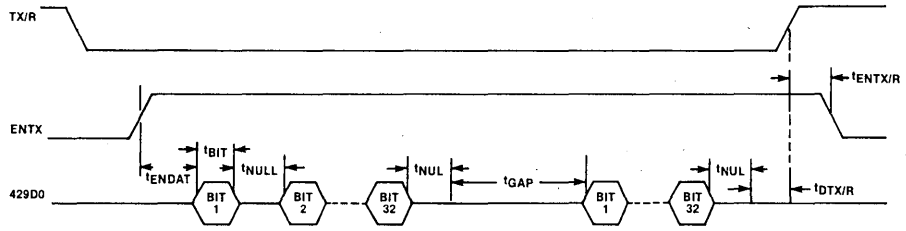


FIGURE 6 TRANSMITTER OUTPUT TIMING

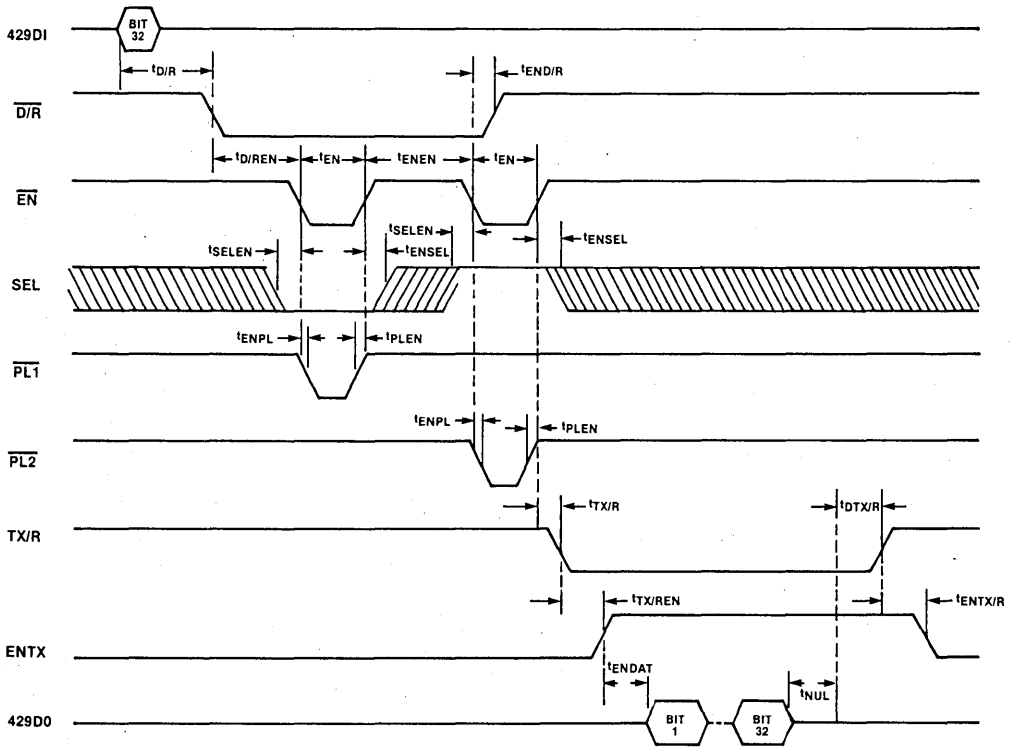
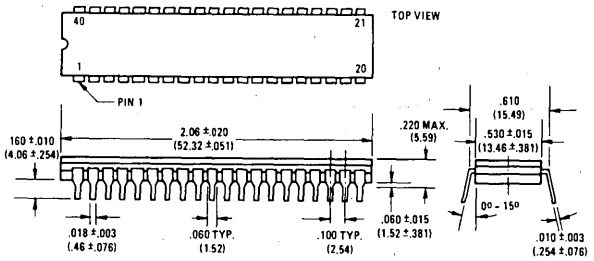


FIGURE 7 REPEATER OPERATION TIMING

Packaging

40-PIN CER-DIP



Ordering Information

HS 1-3282-2

- HS: HARRIS CUSTOM INTERGRATED CIRCUITS DIVISION
- 1-3282: DEVICE NUMBER
- PACKAGE CODE: 1: Ceramic
- TEMPERATURE: 2: −55°C to +125°C; 8: Mil. Std. 883B; 9: −40°C to +85°C

1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions ±.010 (±0.25mm) unless otherwise shown.

Test Product Flow

HARRIS SEMICONDUCTOR PRODUCT FLOW
MIL-STD-883, METHOD 5004 CLASS B
100% SCREENING PROCEDURE

	SCREEN	MIL-STD-883 METHOD/COND.
1	Internal Visual	2010 Cond. B.
2	Stabilization Bake	1008 Cond. C (24 hrs. minimum)
3	Temperature Cycling	1010 Cond. C
4	Constant Acceleration	2001 Cond. E, Y1 plane
5	Seal: A Fine B Gross	1014 Cond. A or B 1014 Cond. C2
6	Initial Electrical	Harris Specifications
7	Burn-In Test	1015, 160 hrs. @ 125°C (or equivalent) (Burn-In circuits enclosed)
8	Final Electrical 100% go-no-go	Tested at Worst Case Operating Conditions
9	External Visual	2009 Sample Inspection

Notes:
- Traceability: All devices are assigned date code identification that provides traceability back to the inspection lot.
- Branding: All devices are branded with the part number and EIA date code.
- Aged Products: Product that has been held for more than 24 months will be reinspected prior to shipment to group A inspection requirements.
- Additional Requirements: Sample Group A electrical tests are performed on a lot acceptance basis.

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United Kingdom
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HARRIS

CUSTOM INTEGRATED CIRCUITS DIVISION

HARRIS

HS-3819

Preliminary

Video Character Generator

SEPTEMBER 1982

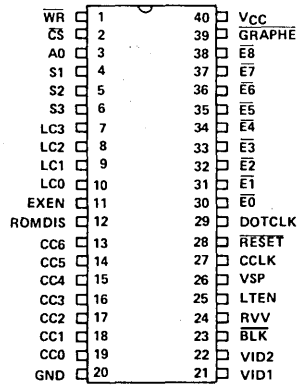
Features

- OPERATION (DOT CLOCK) FROM 1.0 TO 27 MHz
- DESIGNED TO INTERFACE WITH INTEL 8275 PROGRAMMABLE CRT CONTROLLER
- DIRECTLY DECODES (FROM ON-CHIP ROM);
  - ASCII 96 CHARACTER SET
  - 32 PSEUDO-GRAPHIC CHARACTERS
  - 10 OVERLAY PATTERNS
- EXPANDABLE CHARACTER TABLE
- 9 X 12 DOT MATRIX WITH DESCENDER CAPABILITY
- HANDLES VIDEO MODIFIERS;
  - BLANK
  - VIDEO SUPPRESS
  - REVERSE VIDEO
  - LIGHT ENABLE

Description

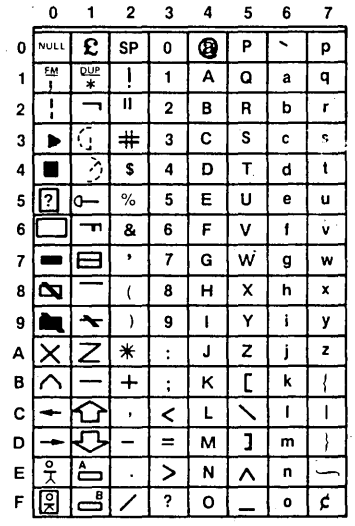
The HS-3819 is a CMOS/LSI Video Character Generator designed to help interface an Intel 8275 Programmable CRT Controller to a video monitor. The character generator must be supplied with a clock frequency of between 1 and 27 MHz which will be used as the dot clock. This signal is then divided by nine to form the character clock output needed by the CRT Controller. The HS-3819 then converts character data into a video output signal, through use of an internal (ROM) character table. Stored in this ROM are the standard 96 ASCII characters, 32 pseudo-graphic characters and 10 overlay patterns used to modify characters. Additional characters, if needed, can easily be decoded from an external memory field.

Pinout

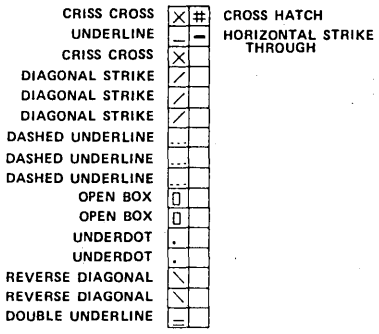


LC0-3 – LINE COUNT
CC0-6 – CHARACTER CODE
ROMDIS – ROM DISABLE
LTEN – LIGHT ENABLE
RVV – REVERSE VIDEO
VSP – VIDEO SUPPRESS
BLK – BLANK
S1-3 – SPECIAL FUNCTION
EXEN – EXPANSION ENABLE
E0-8 – EXPANSION INPUTS
GRAPHE – GRAPHICS ENABLE
WR – WRITE
CS – CHIP SELECT
A0 – ADDRESS 0
VID1-2 – VIDEO OUTPUTS
RESET – RESET
DOTCLK – DOT CLOCK
CCLK – CHARACTER CLOCK

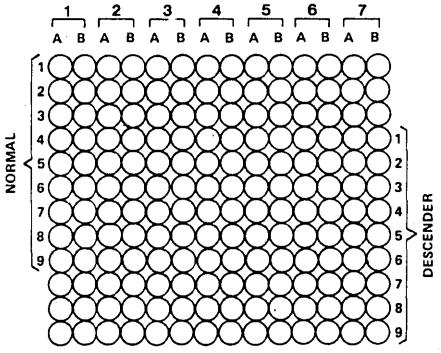
Standard Character Set



Overlay Patterns



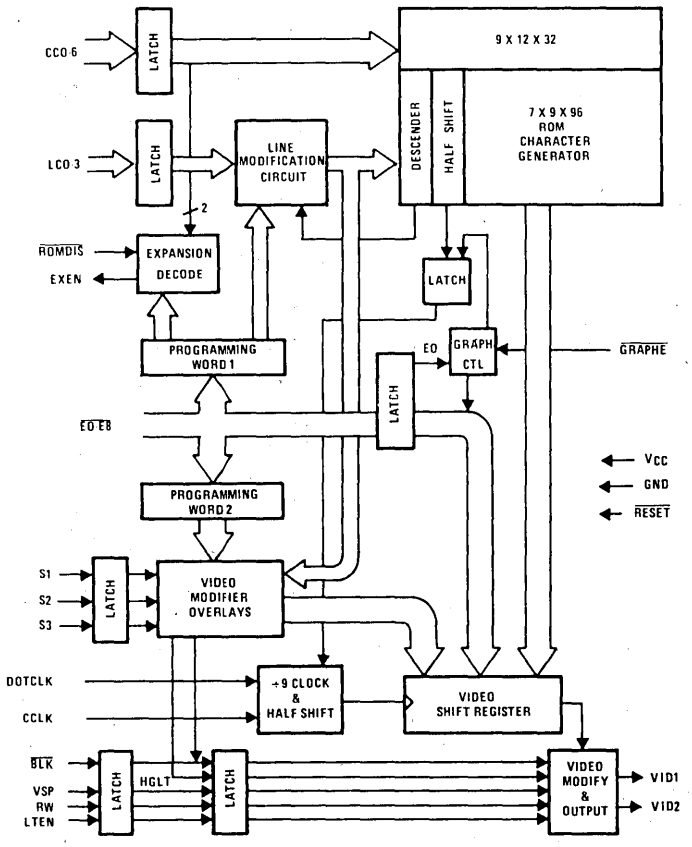
Dot Matrix



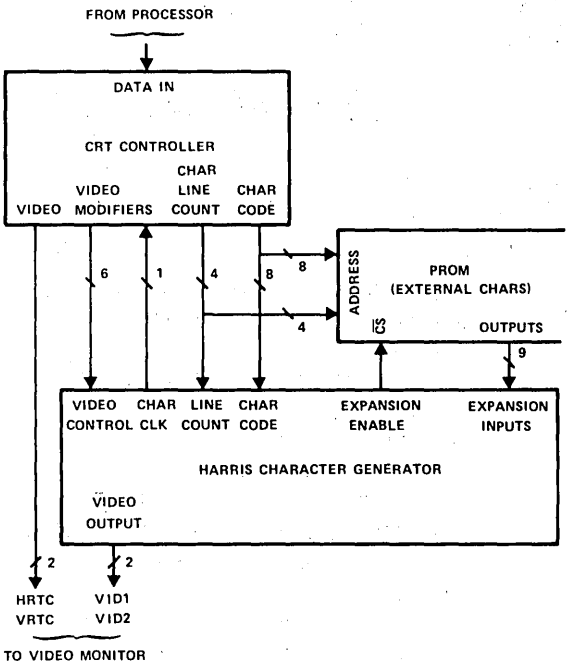
NOTES:

1. EACH ROW MAY HAVE DOTS IN SET A OR SET B ONLY.
2. EACH CHARACTER MAY HAVE DOTS IN NORMAL SET OR DESCENDER SET ONLY.

HS-3819 Block Diagram



System Application



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TWX: 848174

HARRIS

CUSTOM INTEGRATED CIRCUITS DIVISION

HARRIS

ADVANCE

SEPTEMBER 1982

HS-3604

AM Stereo Demodulator

Features

- BANDWIDTH (IF) >1MHz
- ADVANCED SYNCHRONOUS DETECTOR
- DUAL BANDWIDTH PLL
- AUTOMATIC SYNCHRONOUS/ENVELOPE SWITCHING
- AUTOMATIC STEREO/MONO SWITCHING

Applications

- AM STEREO RECEIVERS
- SYNCHRONOUS DEMODULATION
- PHASE LOCKED LOOPS

Pinout

TO BE DETERMINED

Description

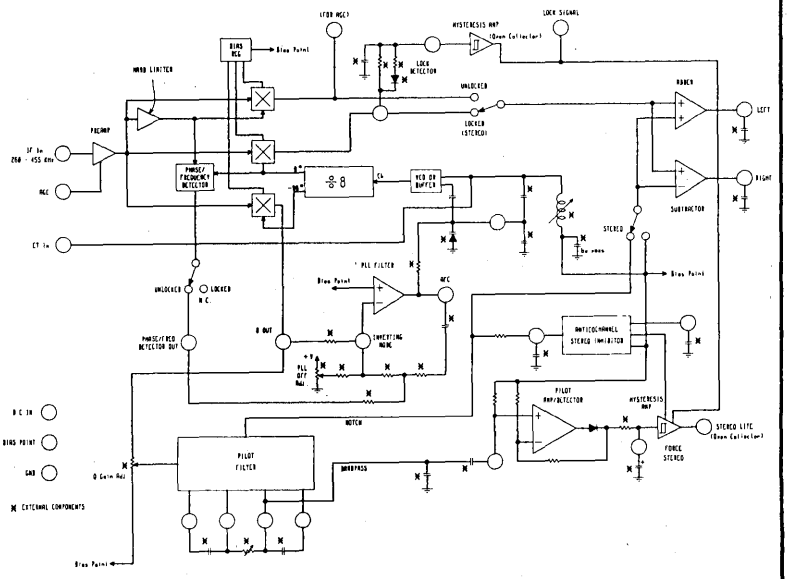
The HS-3604 demodulator is designed specifically for the Harris V-CPM AM stereo system. By using pure synchronous detection in both the sum and difference channels, the HS-3604 takes full advantage of the linear characteristics of the Harris system. The HS-3604 is suitable for use in battery operated portables, car radios, table radios, and in the finest component stereo equipment. The HS-3604 is applicable to both synthesized and conventional mechanically tuned designs.

The demodulator accepts an IF signal (100KHz to 1MHz) and produces left and right outputs. Additional outputs include open collectors for stereo and PLL lock indicators, VCO control voltage for tuning meters, and envelope detector for AGC of preceeding IF and RF amplifiers.

The basic demodulator functions comprise a type two PLL for carrier recovery, I and Q demodulators, a pilot detection circuit, and a sum and difference audio matrix. Supporting functions include a dual bandwidth loop with phase/frequency detector (for mechanically tuned radios), automatic switching between envelope and synchronous detectors (to avoid audio beat notes), and automatic stereo/mono switching.

When used in a synthesized radio design, the VCO is operated as a buffer, accepting an 8 X IF signal from the radio time base. The PLL loop filter output is available for application to a VCXO radio time base.

Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltage VCC	+24V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage VCC	7.0V to 16V
Operating Temperature	-35°C to +70°C

CAUTION: To prevent permanent damage to this device, care should be exercised to insure that the absolute maximum ratings for supply voltages, temperature and voltage or current at any pin is not exceeded during both static and dynamic operation.

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
Supply Current		60	75	mA	
Lamp Driver Saturation		1.3		V	30mA current
Pilot Level for Lamp On	5	5.5	6	%	200mV RMS IF
Pilot Level for Lamp Off	4	4.5	5	%	200mV RMS IF
Input Level for Lock	15	20	25	mV RMS	
Envelope Detector THD		0.2	0.5	%	85% AM
Synchronous Detector THD		0.1	0.3	%	85% AM
Stereo THD		0.3	0.5	%	50% L or R
Stereo Separation	30	40		dB	50% L or R 1KHz AUDIO TEST TONE
Audio Output	180	200	220	mV RMS	200mV RMS IF 100% AM L = R
Signal to Noise Ratio	55	60		dB	200mV RMS IF 100% AM L = R

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HARRIS

CUSTOM INTEGRATED CIRCUITS DIVISION

Harris Custom Integrated Circuits Division Gate Array Family

CMOS GATE ARRAY FAMILY

Product Number	No. Gates	No. I/O's	Available
HGA-C00600	600	40	October, 1982
HGA-C01200	1200	64	October, 1982
HGA-C02500	2500	120	October, 1982
HGA-C01200RH	1200 (radiation resistant)	64	January, 1983

Features

- 3 ns typical gate delay
- 5 μW/MHz/ gate power dissipation
- TTL compatible I/O's
- Single 5-volt supply

BIPOLAR GATE ARRAY FAMILY

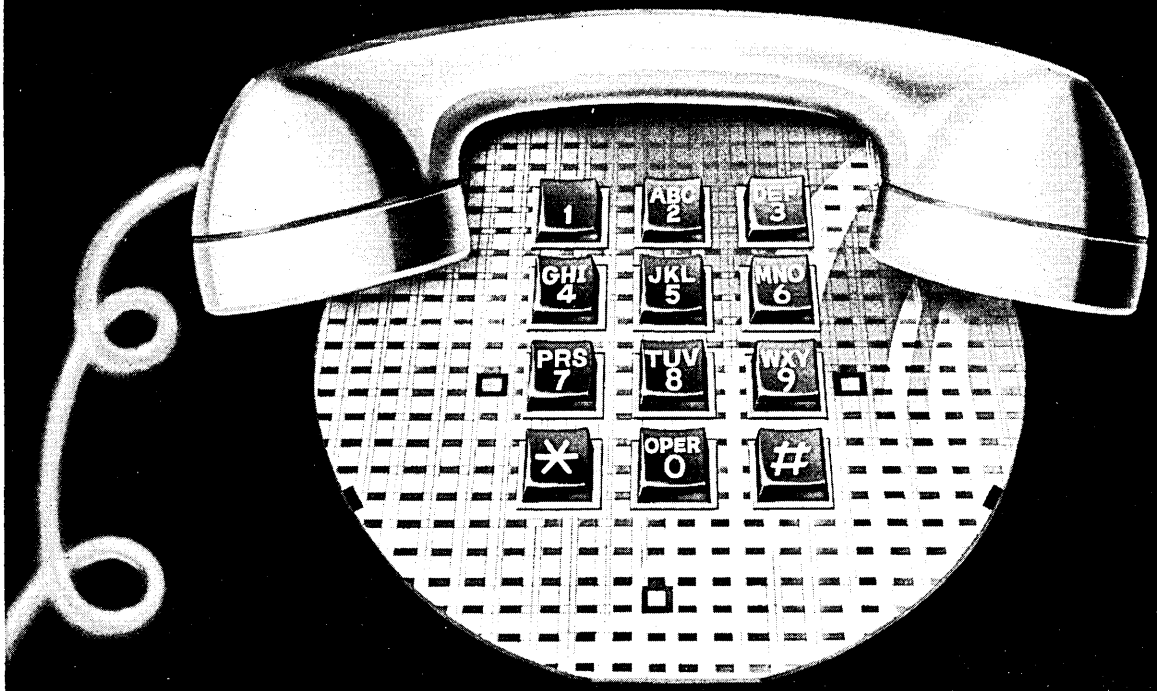
Product Number	No. Gates	No I/O's	Available
HGA-B01200	1200	100	January, 1983
HGA-B03000	3000	120	January, 1983

Features

- 1.2 ns typical gate delay
- 200 μW gate power dissipation
- TTL compatible I/O's
- Choice of 5-volt and 2-volt power supplies

HARRIS

Harris introduces the ultimate in custom/semi-custom design services:



DIAL-A-CHIP℠

A design automation system with a new access design service that puts an entire circuit design facility at your fingertips. All you need is a terminal and a telephone to access the entire Harris design software library. Develop your own custom gate array or standard cell products — from logic through layout. Harris lets you choose the level at which you participate in product development:

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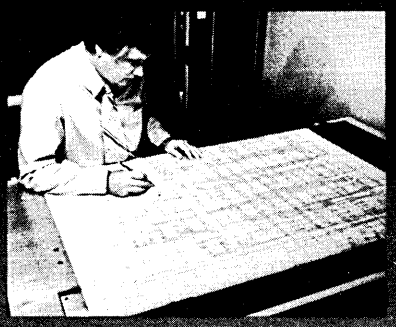

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HARRIS

HS-1553ORH

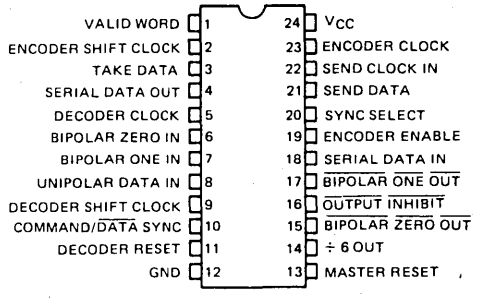
Radiation Resistant CMOS Manchester Encoder-Decoder

JUNE 1982

Features

- SUPPORT OF MIL-STD-1553
- 1.0 MEGABIT/SEC DATA RATE
- SYNC IDENTIFICATION AND LOCK-IN
- CLOCK RECOVERY
- MANCHESTER II ENCODE, DECODE
- SEPARATE ENCODE AND DECODE
- LOW OPERATING POWER: 50mW AT 5 VOLTS
- FULL MILITARY TEMPERATURE RANGE
- FUNCTIONAL TOTAL DOSE . . . 1 x 10^4 RAD(Si)
- LATCH-UP FREE TO . . . . . 5 x 10^{11} RAD (Si)/sec

Pinout



Description

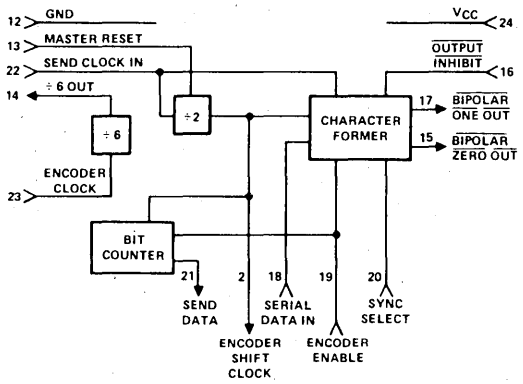
The Harris HS-15530RH is a high performance, radiation resistant, CMOS device intended to service the requirements of MIL-STD-1553 and similar Manchester II encoded, time division multiplexed serial data protocals. This LSI chip is divided into two sections, an Encoder and a Decoder. These sections operate completely independent of each other, except for the Master Reset function.

This circuit provides many of the requirements of MIL-STD-1553. The Encoder produces the sync pulse and the parity bit as well as the encoding of the data bits. The Decoder recognizes the sync pulse and identifies it as well as decoding the data bits and checking parity.

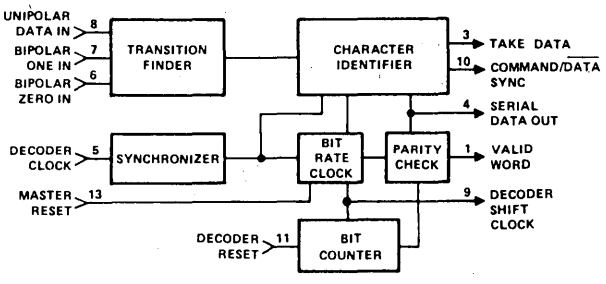
This integrated circuit is fully guaranteed to support the 1MHz data rate of MIL- STD-1553 over both temperature and voltage while residing in a radiation environment. It interfaces with CMOS, TTL or N channel support circuitry, and uses a standard 5 volt supply.

Block Diagrams

ENCODER



DECODER



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} + 0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	−55°C to +125°C

ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ±5% T_A = Operating Temperature Range

	SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	TEST CONDITIONS
D.C.	V_{IH}	Logical "1" Input Voltage	70% V_{CC}			V	
	V_{IL}	Logical "0" Input Voltage			20% V_{CC}	V	
	V_{IHC}	Logical "1" Input Voltage (Clock)	V_{CC} -0.5			V	
	V_{ILC}	Logical "0" Input Voltage (Clock)			GND +0.5	V	
	I_{IL}	Input Leakage	-1.0		+1.0	µA	$0V \leqslant V_{IN} \leqslant V_{CC}$
	V_{OH}	Logical "1" Output Voltage	2.4			V	I_{OH} = -3mA
	V_{OL}	Logical "0" Output Voltage			0.4	V	I_{OL} = 1.8mA
	I_{CCSB}	Supply Current Standby		0.5	2	mA	$V_{IN} = V_{CC}$ = 5.25V Outputs Open
	I_{CCOP}	Supply Current Operating*		8.0	10.0	mA	V_{CC} = 5.25V, f = 1MHz
	C_{IN}	Input Capacitance*		5.0	7.0	pF	
	C_O	Output Capacitance*		8.0	10.0	pF	

*Guaranteed and sampled but not 100% tested.

ENCODER TIMING V_{CC} = 5.0V ±5% T_A = Operating Temperature Range

A.C.	F_{EC}	Encoder Clock Frequency			13	MHz	C_L = 50pF
	F_{ESC}	Send Clock Frequency			2.16	MHz	
	T_{ECR}	Encoder Clock Rise Time			8	ns	
	T_{ECF}	Encoder Clock Fall Time			8	ns	
	F_{ED}	Data Rate			1.08	MHz	
	T_{MR}	Master Reset Pulse Width	150			ns	
	T_{E1}	Shift Clock Delay			125	ns	
	T_{E2}	Serial Data Setup	75			ns	
	T_{E3}	Serial Data Hold	75			ns	
	T_{E4}	Enable Setup	90			ns	
	T_{E5}	Enable Pulse Width	80			ns	
	T_{E6}	Sync Setup	55			ns	
	T_{E7}	Sync Pulse Width	150			ns	
	T_{E8}	Send Data Delay	−10		50	ns	
	T_{E9}	Bipolar Output Delay			130	ns	

DECODER TIMING V_{CC} = 5.0V ±5% T_A = Operating Temperature Range

A.C.	F_{DC}	Decoder Clock Frequency			13	MHz	C_L = 50pF
	T_{DCR}	Decoder Clock Rise Time			8	ns	
	T_{DCF}	Decoder Clock Fall Time			8	ns	
	F_{DD}	Data Rate			1.08	MHz	
	T_{DR}	Decoder Reset Pulse Width	150			ns	
	T_{DRS}	Decoder Reset Setup Time	75			ns	
	T_{MR}	Master Reset Pulse Width	150			ns	
	T_{D1}	Bipolar Data Pulse Width	T_{DC} +10			ns	①
	T_{D2}	Sync Transition Span		18T_{DC}		ns	①
	T_{D3}	One Zero Overlap			T_{DC} -10	ns	①
	T_{D4}	Short Data Transition Span		6T_{DC}		ns	①
	T_{D5}	Long Data Transition Span		12T_{DC}		ns	①
	T_{D6}	Sync Delay (ON)		40	110	ns	
	T_{D7}	Take Data Delay (ON)		50	110	ns	
	T_{D8}	Serial Data Out Delay		80	80	ns	
	T_{D9}	Sync Delay (OFF)		90	110	ns	
	T_{D10}	Take Data Delay (OFF)		110	110	ns	
	T_{D11}	Valid Word Delay		90	110	ns	

NOTE ①: $15T_{DC}$ +10 = [15 (Decoder Clock Period)] +10ns T_{DC} = Decoder Clock Period = $\frac{1}{F_{DC}}$

These parameters are guaranteed but not 100% tested.

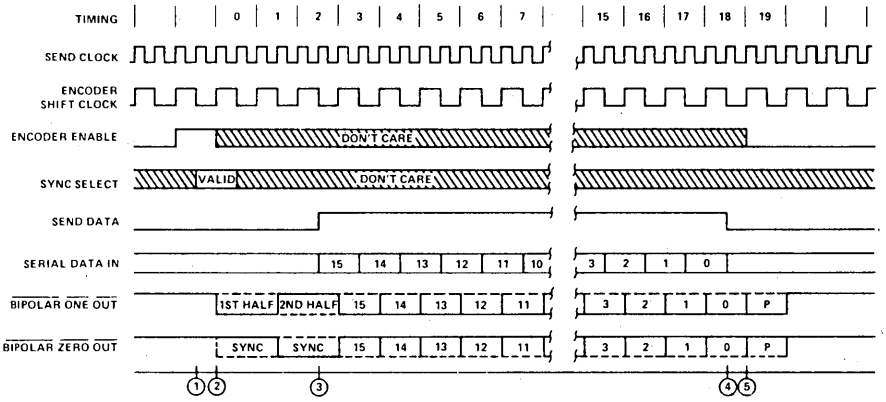
PIN	SECTION	NAME	DESCRIPTION
1	Decoder	VALID WORD	Output high indicates receipt of a valid word.
2	Encoder	ENCODER SHIFT CLOCK	Output for shifting data into the Encoder. This clock shifts data on a low-to-high transition.
3	Decoder	TAKE DATA	Output is high during receipt of data after identification of a sync pulse.
4	Decoder	SERIAL DATA OUT	Delivers received data in correct NRZ format.
5	Decoder	DECODER CLOCK	Input drives the transition finder, and the synchronizer which in turn supplies the clock to the balance of the Decoder.
6	Decoder	BIPOLAR ZERO IN	A high input should be applied when the bus is in its negative state. This pin must be held high when the Unipolar input is used.
7	Decoder	BIPOLAR ONE IN	A high input should be applied when the bus is in its positive state, this pin must be held low when the Unipolar input is used.
8	Decoder	UNIPOLAR DATA IN	With pin 6 high and pin 7 low, this pin enters unipolar data into the transition finder circuit. If not used this input must be held low.
9	Decoder	DECODER SHIFT CLOCK	Output which delivers a frequency (Decoder Clock ÷ 12), synchronized by the recovered serial data stream.
10	Decoder	COMMAND SYNC	Output of a high from this pin occurs during output of decoded data which was preceded by a Command (or Status) synchronizing character. A low output indicates a Data synchronizing character.
11	Decoder	DECODER RESET	A high input to this pin during a rising edge of DECODER SHIFT CLOCK resets the decoder bit counting logic to a condition ready for a new word.
12	Both	GROUND	Ground supply pin.
13	Both	MASTER RESET	A high on this pin clears 2:1 counters in both the Encoder and Decoder.
14	Encoder	÷ 6 OUT	Output from 6:1 divider which is driven by the ENCODER CLOCK.
15	Encoder	$\overline{\text{BIPOLAR ZERO OUT}}$	An active low output designed to drive the zero or negative sense of a bipolar line driver.
16	Encoder	$\overline{\text{OUTPUT INHIBIT}}$	A low on this input forces pin 15 and pin 17 high, the inactive states.
17	Encoder	$\overline{\text{BIPOLAR ONE OUT}}$	An active low output designed to drive the one or positive sense of a bipolar line driver.
18	Encoder	SERIAL DATA IN	Accepts a serial data stream at a data rate equal to ENCODER SHIFT CLOCK.
19	Encoder	ENCODER ENABLE	A high on this input initiates the encode cycle. (Subject to the preceding cycle being complete.)
20	Encoder	SYNC SELECT	Actuates command sync for an input high and data sync for an input low.
21	Encoder	SEND DATA	Is an active high output which enables the external source of serial data.
22	Encoder	SEND CLOCK IN	Clock input at a frequency equal to the data rate X2.
23	Encoder	ENCODER CLOCK.	Input to the 6:1 divider.
24	Both	V_{CC}	Positive supply pin.

Encoder Operation

The Encoder requires a single clock with a frequency of twice the desired data rate applied at the SEND CLOCK input. An auxillary divide by six counter is provided on chip which can be utilized to produce the SEND CLOCK by dividing the DECODER CLOCK.

The Encoder's cycle begins when ENCODER ENABLE is high during a falling edge of ENCODER SHIFT CLOCK ①. This cycle lasts for one word length or twenty ENCODER SHIFT CLOCK periods. At the next low-to-high transition of the ENCODER SHIFT CLOCK, a high at SYNC SELECT input actuates a command sync or a low will produce a data sync for that word ② . When the Encoder is ready to accept data, the SEND DATA output will go high and remain high for sixteen ENCODER SHIFT CLOCK periods ③ . During these sixteen periods the data should be clocked into the SERIAL DATA input with every low-to-high transition of the ENCODER SHIFT CLOCK ③ – ④ . After the sync and the Manchester II coded data are transmitted through the $\overline{\text{BIPOLAR ONE}}$ and $\overline{\text{BIPOLAR ZERO}}$ outputs, the Encoder adds on an additional bit which is the parity for that word ⑤ . At any time a low on $\overline{\text{OUTPUT INHIBIT}}$ input will force both bipolar outputs to a high state but will not affect the Encoder in any other way.

To abort the Encoder transmission a positive pulse must be applied at MASTER RESET. Anytime after or during this pulse, a low to high transition on SEND CLOCK clears the internal counters and initializes the Encoder for a new word.



Decoder Operation

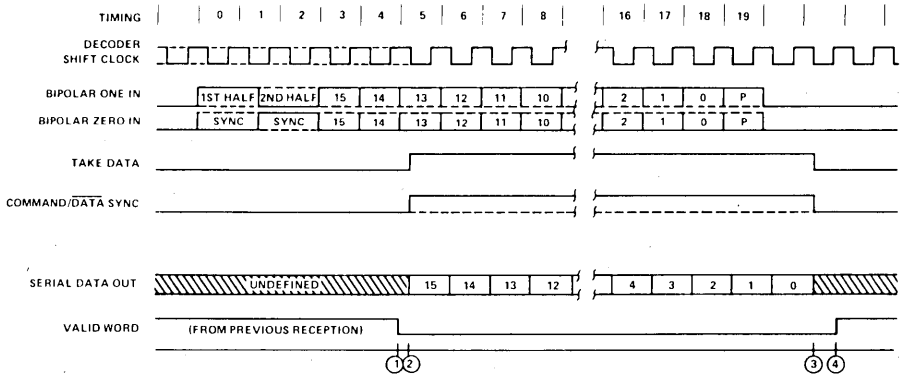
The Decoder requires a single clock with a frequency of 12 times the desired data rate applied at the DECODER CLOCK input. The Manchester II coded data can be presented to the Decoder in one of two ways. The BIPOLAR ONE and BIPOLAR ZERO inputs will accept data from a comparator sensed transformer coupled bus as specified in Military Spec 1553. The UNIPOLAR DATA input can only accept non-inverted Manchester II coded data. (e.g. from $\overline{\text{BIPOLAR ZERO OUT}}$ of an Encoder.)

The Decoder is free running and continuously monitors its data input lines for a valid sync character and two valid Manchester data bits to start an output cycle. When a valid sync is recognized ①, the type of sync is indicated on COMMAND/$\overline{\text{DATA}}$ SYNC output. If the sync character was a command sync, this output will go high ② and remain high for sixteen DECODER SHIFT CLOCK periods ③ , otherwise it will remain low. The TAKE DATA output will go high and remain high ② – ③ while the Decoder is transmitting the decoded data through SERIAL DATA OUT. The decoded data available at SERIAL DATA OUT is in a NRZ format. The DECODER SHIFT CLOCK is provided so that the decoded bits can get shifted into an external register on every low-to-high transition of this clock ② – ③.

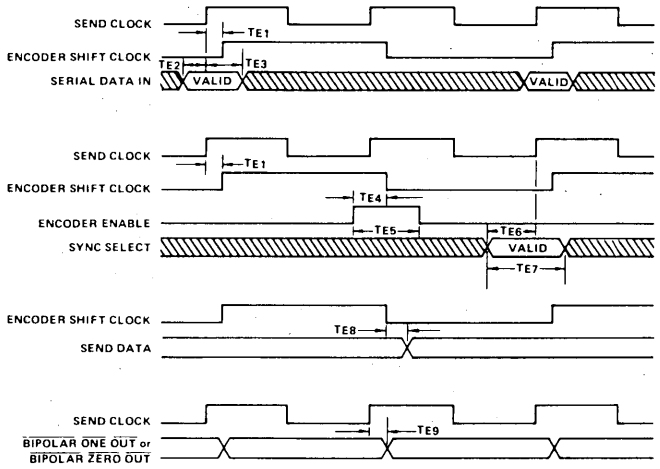
After all sixteen decoded bits have been transmitted ③ the data is checked for odd parity. A high on VALID WORD output ④ indicates a successful reception of a word without any Manchester or parity errors. At this time the Decoder is looking for a new sync character to start another output sequence.

At any time in the above sequence a high input on DECODER RESET during a low-to-high transition of DECODER SHIFT CLOCK will abort transmission and initialize the Decoder to start looking for a new sync character.

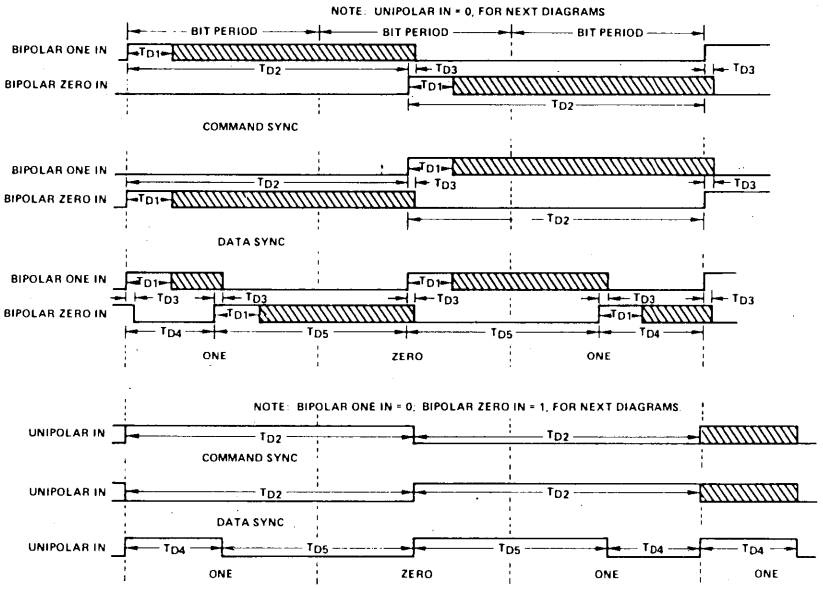
Decoder Operation (continued)



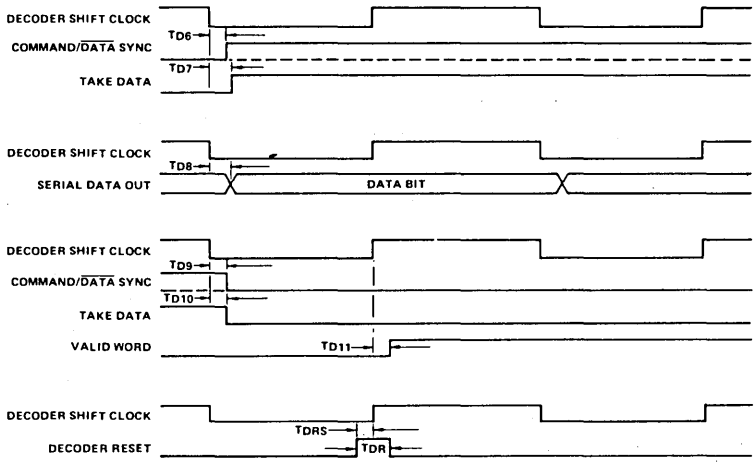
Encoder Timing



Decoder Timing

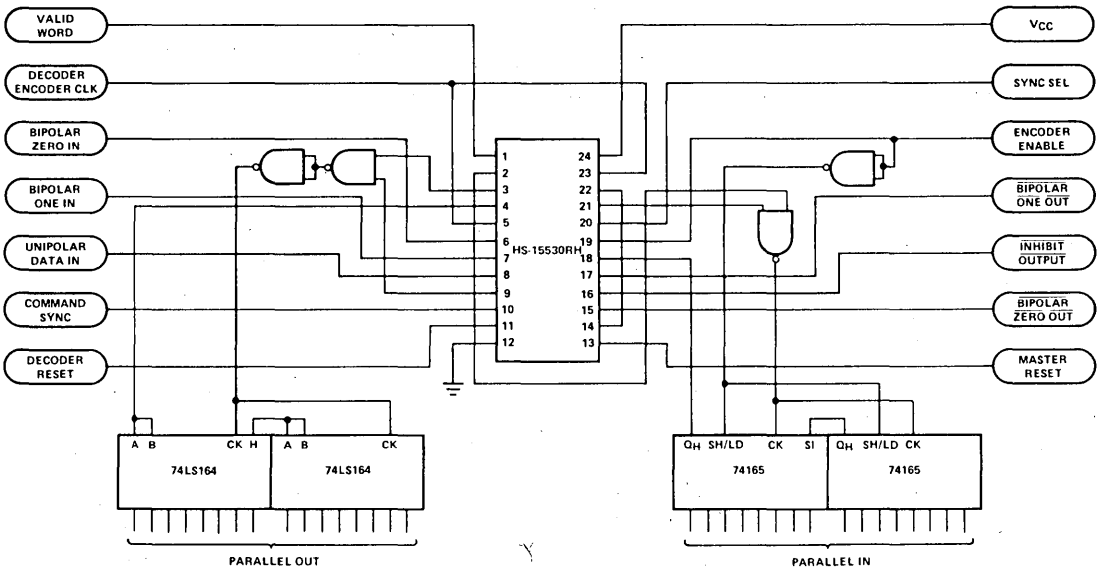


Decoder Timing (continued)

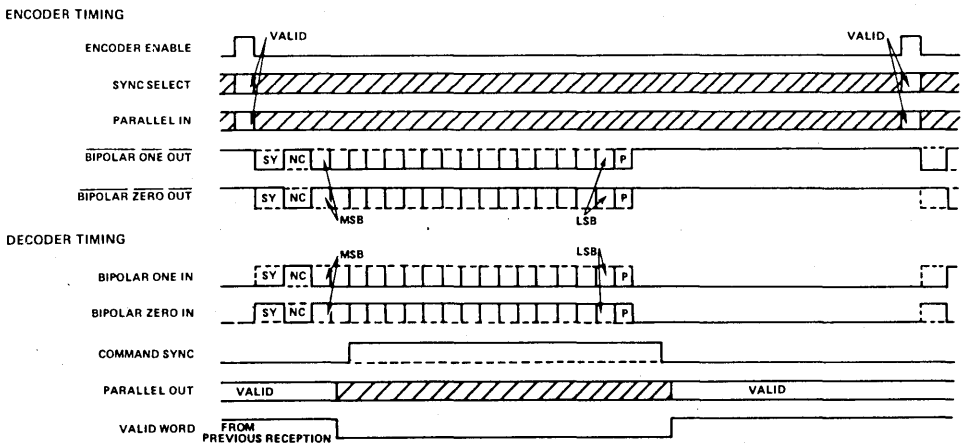


Applications

How to Make Our MTU Look Like a Manchester Encoded UART



Typical Timing Diagrams for a Manchester Encoded UART



The 1553 standard defines a time division multiplexed data bus for application within aircraft. The bus is defined to be bipolar, and encoded in a Manchester II format, so no DC component appears on the bus. This allows transformer coupling and excellent isolation among systems and their environment.

The HS-15530RH supports the full bipolar configuration, assuming a bus driver configuration similar to that in Figure 1. Bipolar inputs from the bus, like Figure 2, are also accommodated.

The signaling format in MIL-STD-1553 is specified on the assumption that the network of 32 or fewer terminals are controlled by a central control unit by means of Command Words, and Data. Terminals respond with Status Words, and Data. Each word is preceded by a synchronizing pulse, and followed by parity bit, occupying a total of 20 μsec. The word formats are shown in Figure 4. The special abbreviations are as follows:

P	Parity, which is defined to be odd, taken across all 17 bits.
R/T	Receive on logical zero, transmit on ONE.
ME	Message Error if logical 1.
TF	Terminal Flag, if set, calls for controller to request self-test data.

The paragraphs above are intended only to suggest the content of MIL-STD-1553, and do not completely describe its bus requirements, timing or protocols.

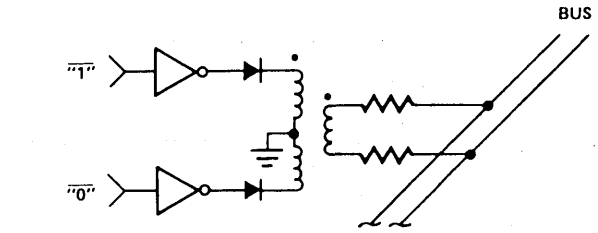


FIGURE 1 – Simplified MIL-STD-1553 Driver

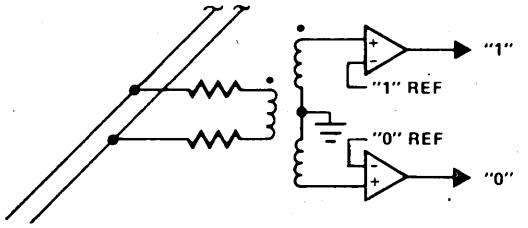


FIGURE 2 – Simplified MIL-STD-1553 Receiver

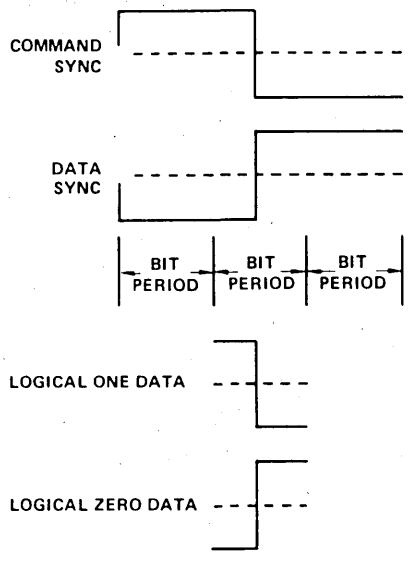


FIGURE 3 – MIL-STD-1553 Character Formats

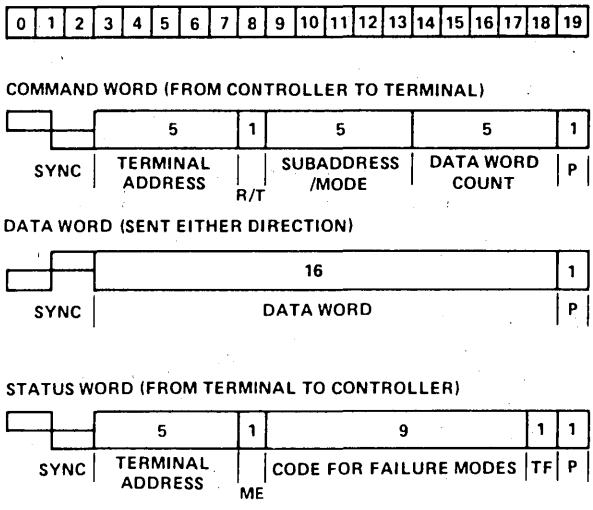


FIGURE 4 – MIL-STD-1553 Word Formats

NOTE: This page is a summary of MIL-STD-1553 and is not intended to describe the operation of the HS-15530RH

Radiation Screening Procedure

(1) Two (2) probed good samples per wafer will be selected from $\geq$20% of the wafers in a run. (All wafers in a "run" will have been processed together through all high temperature processing steps and through metallization.)

(2) The sample die shall be assembled and tested for functionality.

(3) The sample devices shall be subjected to a Total Dose Radiation level of 1 x 10^4 Rad(Si +10% from a Gamma Cell 220 Cobalt 60 source or equivalent. The samples shall be biased at 5 volts with all inputs high. The dose rate shall be between 50 rads/sec and 200 rads/sec.

(4) I_{CCSB} at V_{CC} = 5 volts will be measured and recorded for each device within one hour (±15 minutes) after irradiation. The lot will be accepted only if the average of these measure values is $\leq$5mA.

Radiation Effects

The HS-15530/31RH is processed with the same mask set as is used for HARRIS' equivalent commercial part. Latchup free operation, achieved by the use of special starting material and improved total dose hardness, is obtained with special high temperature processing cycles. These process techniques can, in principal, be applied to any standard HARRIS CMOS product.

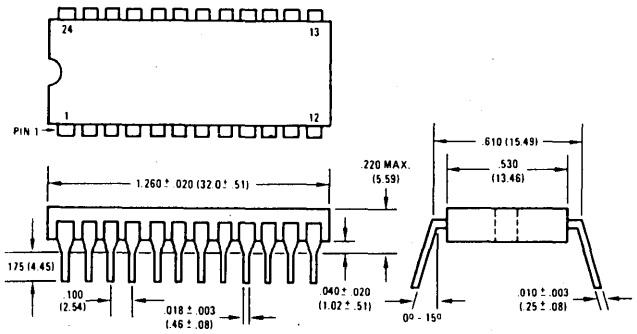
The primary failure mode under exposure to ionizing radiation is an increase in static leakage current (I_{CCSB}). Functional failure due to the increased leakage currents will typically occur for dose levels in excess of 5 x 10^4 RAD-Si. AC and DC parameters other than I_{CC} will change less than 10% for total dose levels under 5 x 10^4 RAD-Si. The excess leakage currents will anneal at room temperature and are typically reduced by a factor of 3-10 within 24 hours after irradiation.

On a production basis, HARRIS is able to perform screens only for a total dose hardness. Transient radiation tests, however, have shown the following results:

Latchup free doses $\geq$ 5 x 10^{11} rads/sec. Upset (loss of stored data) typically $\geq 10^8$ rads/sec.

Package

24 LEAD DIP



1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions ±.010 (±0.25mm) unless otherwise shown.

Ordering Information

HS 1 -15530RH- 2

- HS — HARRIS
- 1 — PACKAGE: 1 — Cerdip, 9 — Flatpack
- 15530RH — DEVICE NUMBER
- 2 — TEMPERATURE: 2 — -55°C to +125°C, 8 — MIL-STD-883B

Sales Offices

EASTERN REGION

8300 Greensboro Drive
McLean, Virginia 22102
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Burlington, MA 01803
(617) 273-1020
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United Kingdom
Tel: 34666
TWX: 848174

HARRIS

CUSTOM INTEGRATED CIRCUITS DIVISION

HS-6504RH

4096 x 1 CMOS RAM

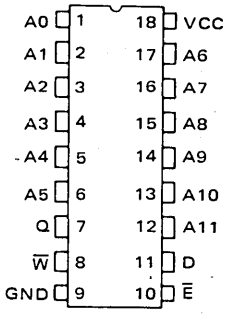
SEPTEMBER 1982 **Preliminary**

Features

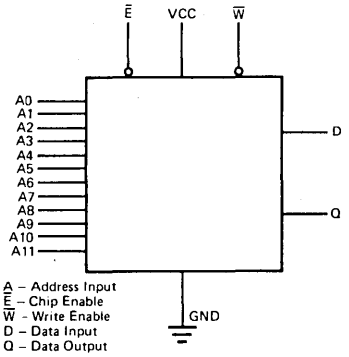
- LOW POWER STANDBY . . . . . 550 μW MAX.
- LOW POWER OPERATION . . . . . 35mW/MHz MAX.
- EXTREMELY LOW SPEED POWER PRODUCT
- FUNCTIONAL TOTAL DOSE . . . . . 1×10^5 RAD Si
- DATA UPSET . . . . . $>10^8$ RAD Si/SEC
- LATCH - UP FREE TO . . . . . $>5 \times 10^{11}$ RAD Si/SEC
- TTL COMPATIBLE INPUT/OUTPUT
- THREE - STATE OUTPUT
- STANDARD JEDEC PINOUT
- FAST ACCESS TIME . . . . . 200nsec TYP
- MILITARY TEMPERATURE RANGE
- 18 PIN PACKAGE FOR HIGH DENSITY
- ON CHIP ADDRESS REGISTER

Pinout

TOP VIEW



Logic Symbol



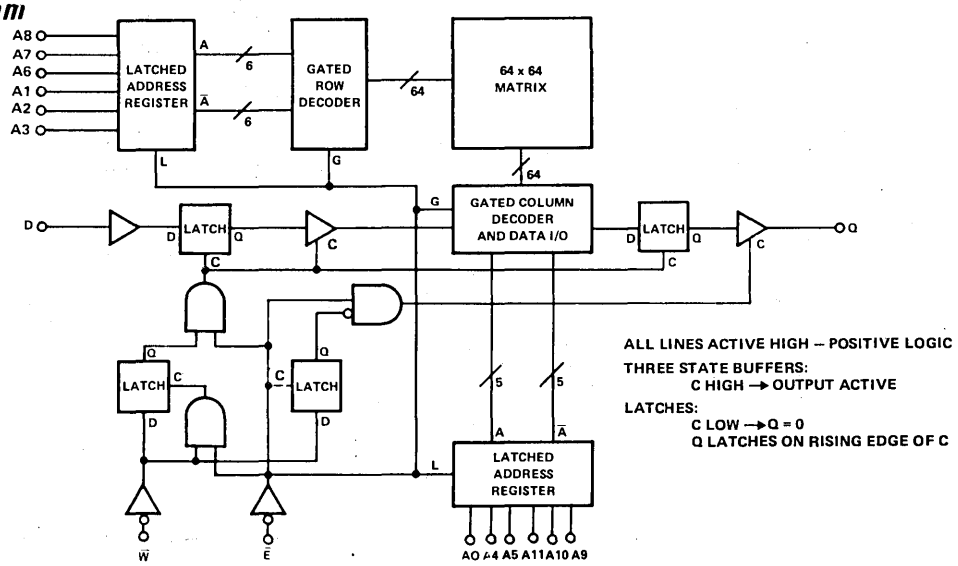
Description

The HS–6504RH is a 4096 x 1 static CMOS RAM fabricated using the Harris Custom Integrated Circuits Division radiation hardened self-aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

On-chip latches are provided for addresses, data input and data output allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance for use in expanded memory arrays.

The HS–6504RH is a fully static RAM and may be maintained in any state for an indefinite period of time.

Functional Diagram



Information on this device is preliminary. Data is subject to change unless otherwise specifically agreed. No obligations are assumed for notice of change or future manufacture of this device.

CAUTION: These devices are sensitive to electrostatic discharge.

Symbols and Abbreviations

This data sheet utilizes a new set of specification nomenclature. This new format is an IEEE and JEDEC supported standard for semiconductor memories. It is intended to clarify the symbols, abbreviations and definitions, and to make all memory data sheets consistent. We believe that, once acclimated, you will find this standardized format easy to read and use.

ELECTRICAL PARAMETER ABBREVIATIONS

All abbreviations use upper case letters with no subscripts. The initial symbol is one of these four characters:

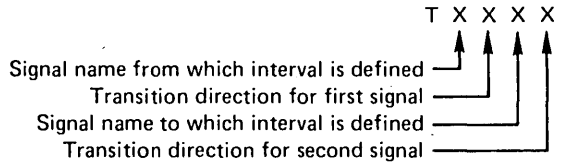
V (Voltage)
I (Current)
P (Power)
C (Capacitance)

The second letter specifies input (I) or output (O), and the third letter indicates the high (H), low (L) or off (Z) state of the pin during measurements. Examples:

VIL — Input Low Voltage
IOZ — Output Leakage Current

TIMING PARAMETER ABBREVIATIONS

All timing abbreviations use upper case characters with no subscripts. The initial character is always T and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal point specify the signal name and the signal transitions. Thus the format is:



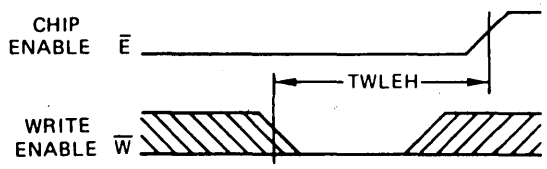
Signal Definitions:

A = Address
D = Data In
Q = Data Out
W = Write Enable
E = Chip Enable
S = Chip Select
G = Output Enable

Transition Definitions:

H = Transition to High
L = Transition to Low
V = Transition to Valid
X = Transition to Invalid or Don't Care
Z = Transition to Off (High Impedance)

EXAMPLE:



The example shows Write pulse setup time defined as TWLEH-Time from Write enable Low to chip Enable High.

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address set-up time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WAVEFORMS

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	—	HIGH IMPEDANCE

ABSOLUTE MAXIMUM RATINGS

Supply Voltage - (VCC - GND)	-0.3V to +7.0V
Input or Output Voltage Applied	(GND -0.3V) to (VCC +0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage	4.5V to 5.5V
Operating Temperature	-55°C to +125°C

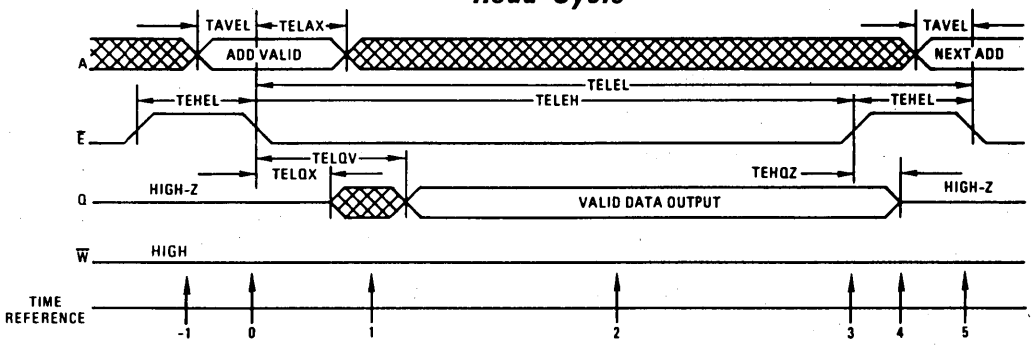
CAUTION: To prevent permanent damage to this device, care should be exercised to insure that the absolute maximum ratings for supply voltages, temperature and voltage or current at any pin is not exceeded during both static and dynamic operation.

ELECTRICAL CHARACTERISTICS ⑤

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP = 25°C ① VCC = 5.0V TYPICAL PRE RAD	TEMP = 25°C ① VCC = 5.0V TYPICAL POST RAD	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100	5	5	µA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		7	4.5		mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Current		50	3	3	µA	IO = 0, VCC = 3.0 VI = VCC or GND
	VCCDR	Data Retention Voltage		3	2.6	1.8	V	
	II	Input Leakage Current	−1	+1	0	0	µA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	−10	+10	±0.5	±0.5	µA	GND ≤ VI ≤ VCC
	VIL	Input Low Voltage	−0.3	0.8	1.5	1.3	V	
	VIH	Input High Voltage All inputs except $\overline{E}$ R/$\overline{W}$	VCC −2.0	VCC +0.3	2.7	2.3	V	
	VIH	Input High Voltage for $\overline{E}$ R/$\overline{W}$	VCC −1.5	VCC +0.3	2.9	1.9	V	
	VOL	Output Low Voltage		0.4	0.2	0.15	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.6	4.0	V	IO = −1.0mA
	CI	Input Capacitance ③		8.0	5.0	5.0	pF	f = 1MHz VI = VCC or GND
	CO	Output Capacitance ③		10.0	6.0	6.0	pF	f = 1MHz VI = VCC or GND
A.C.	TELQV	Chip Enable Access Time		300	150	180	ns	④
	TAVQV	Address Access Time		320	140	180	ns	④
	TELQX	Chip Enable Output Enable Time		100	50	60	ns	④
	TEHQZ	Chip Enable Output Disable Time		100	50	60	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		150	180	ns	④
	TEHEL	Chip Enable Pulse Positive Width	120		40	80	ns	④
	TAVEL	Address Setup Time	20		−10	0	ns	④
	TELAX	Address Hold Time	50		30	35	ns	④
	TWLWH	Write Enable Pulse Width	80		20	30	ns	④
	TWLEH	Write Enable Pulse Setup Time	200		140	140	ns	④
	TWLEL	Early Write Pulse Setup Time	0		−15	−10	ns	④
	TWHEL	Write Enable Read Mode Setup Time	0		−15	−10	ns	④
	TELWH	Early Write Pulse Hold Time	80		40	50	ns	④
	TDVWL	Data Setup Time	0		−15	−10	ns	④
	TDVEL	Early Write Data Setup Time	0		−15	−10	ns	④
	TWLDX	Data Hold Time	80		50	60	ns	④
	TELDX	Early Write Data Hold Time	80		50	60	ns	④
	TELWL	Early Write Output Hi-Z Time	0		−10	−10	ns	④
	TQVWL	Data Valid to Write Time	0		0	0	ns	④
	TELEL	Read or Write Cycle Time	420		190	260	ns	④

NOTES:
1. All devices guaranteed at worst case limits. Room temp., 5 volt data provided for information and not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Post Rad Data @ TD = 1 x10^5.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC test Conditions: Inputs: TRISE = TFALL ≤ 20nsec; Outputs: 1TTL Load and 50 pF. All timing measurements at 1/2 VCC.
5. Pre-Radiation and Post-Radiation limits.

Read Cycle

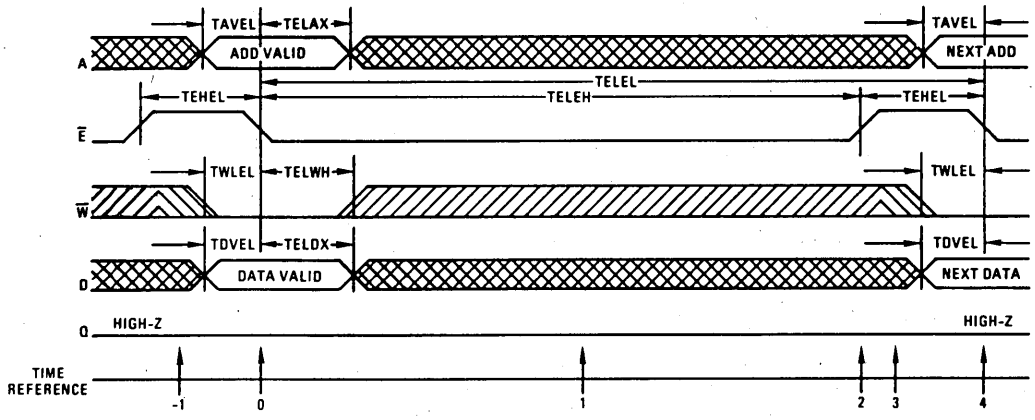


TRUTH TABLE

TIME REFERENCE	INPUTS Ē	W̄	A	OUTPUT Q	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	↘	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	OUTPUT ENABLED
2	L	H	X	V	OUTPUT VALID
3	↗	H	X	V	READ ACCOMPLISHED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address set up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but data is not valid until during time (T = 2). $\overline{W}$ must remain high until after time (T = 2). After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the output buffer and ready the RAM for the next memory cycle (T = 4).

Early Write Cycle

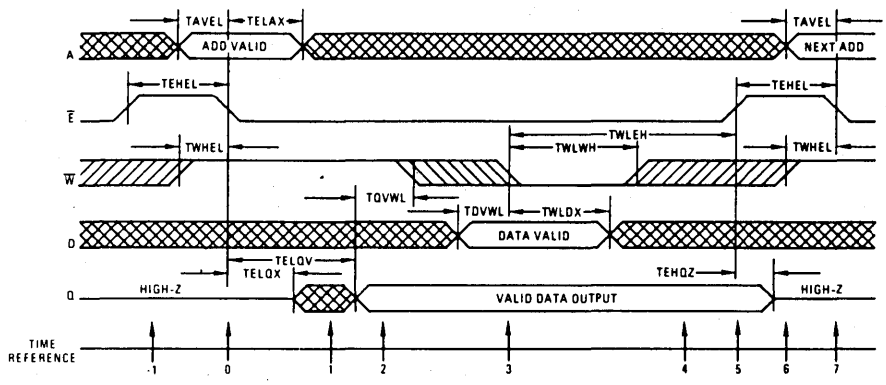


TRUTH TABLE

TIME REFERENCE	INPUTS Ē	W̄	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↘	L	V	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	X	X	X	Z	WRITE IN PROGRESS INTERNALLY
2	↗	X	X	X	Z	WRITE COMPLETED
3	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
4	↘	L	V	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The early write cycle is the only cycle where the output is guaranteed not to become active. On the falling edge of $\overline{E}$ (T = 0), the addresses, the write signal, and the data input are latched in on chip registers. The logic value of $\overline{W}$ at the time $\overline{E}$ falls determines the state of the output buffer for that cycle. Since $\overline{W}$ is low when $\overline{E}$ falls, the output buffer is latched into the high impedance state and will remain in that state until $\overline{E}$ returns high (T = 2). For this cycle, the data input is latched by $\overline{E}$ going low; therefore data set up and hold times should be referenced to $\overline{E}$. When $\overline{E}$ (T = 2) returns to the high state the output buffer disables and all signals are unlatched. The device is now ready for the next cycle.

Read Modify Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↘	H	V	X	Z	CYCLE BEGINS; ADDRESS ARE LATCHED
1	L	H	X	X	X	OUTPUT ENABLED
2	L	H	X	X	V	OUTPUT VALID, READ AND MODIFY TIME
3	L	↘	X	V	V	WRITE BEGINS, DATA IS LATCHED
4	L	X	X	X	V	WRITE IN PROGRESS INTERNALLY
5	↗	X	X	X	V	WRITE COMPLETED
6	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
7	↘	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The read modify write cycle begins as all other cycles on the falling edge of $\overline{E}$ (T= 0). The $\overline{W}$ line should be high at (T = 0) in order to latch the output buffers in the active state. During (T = 1) the output will be active but not valid until (T = 2). On the falling edge of the $\overline{W}$ (T = 3) the data present at the output and input are latched. The $\overline{W}$ signal also latches itself on its low going edge. All input signals excluding $\overline{E}$ have been latched and have no further effect on the RAM. The rising edge of $\overline{E}$ (T = 5) completes the write portion of the cycle and unlatches all inputs and output . The output goes to a high impedance and the RAM is ready for the next cycle.

NOTES: In the above descriptions the numbers in parenthesis (T = n) refer to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

Radiation Screening Procedure

(1) Two (2) probed good samples per wafer will be selected from $\geq$ 20% of the wafers in a run. (All wafers in a "run" will have been processed together through all high temperature processing steps and through metallization.)

(2) The sample die shall be assembled and tested to the production test program for proper operation.

(3) The sample devices shall be subjected to a Total Dose Radiation level of 1×10^5 Rad Si ($\pm$ 10%) from a Gamma Cell 220 Cobalt 60 source or equivalent. The samples shall be biased at 5 volts with all inputs high. The dose rate shall be between 50 rads/sec and 200 rads/sec.

(4) The samples will be tested to the data sheet limits within one hour ($\pm$15 minutes) after irradiation. The lot will be accepted only if all units, exclusive of non-radiation failures, meet the data sheet limits.

Radiation Effects

The HS-6504RH is an RH memory designed to survive in a radiation environment and to meet the electrical characteristics and be pin compatible to the Harris equivalent commercial part. Latchup free operation, achieved by the use of special starting material and improved total dose hardness, is obtained with special high temperature processing cycles. These process techniques can, in principle, be applied to any standard HARRIS CMOS product.

On a production basis, HARRIS only performs screens for total dose hardness to a level of 1×10^5 rad-Si. Transient radiation tests, however, have shown the following results:

Latchup free to doses $\geq 5 \times 10^{11}$ rads/sec.
Upset (loss of stored data) typically $\geq 10^8$ rads/sec.

Test Product Flow

HARRIS SEMICONDUCTOR PRODUCT FLOW
MIL-STD-883, METHOD 5004 CLASS B

100% SCREENING PROCEDURE

	SCREEN	MIL-STD-883 METHOD/COND.
1	Internal Visual	2010 Cond. B.
2	Stabilization Bake	1008 Cond. C (24 hrs. minimum)
3	Temperature Cycling	1010 Cond. C
4	Constant Acceleration	2001 Cond. E; Y1 plane
5	Seal: A Fine B Gross	1014 Cond. A or B 1014 Cond. C2
6	Initial Electrical	Harris Specifications
7	Burn-In Test	1015, 160 hrs. @ 125°C (or equivalent) (Burn-In circuits enclosed)
8	Final Electrical 100% go-no-go	Tested at Worst Case Operating Conditions
9	External Visual	2009 Sample Inspection

Notes:

Traceability: All devices are assigned date code identification that provides traceability back to the inspection lot.

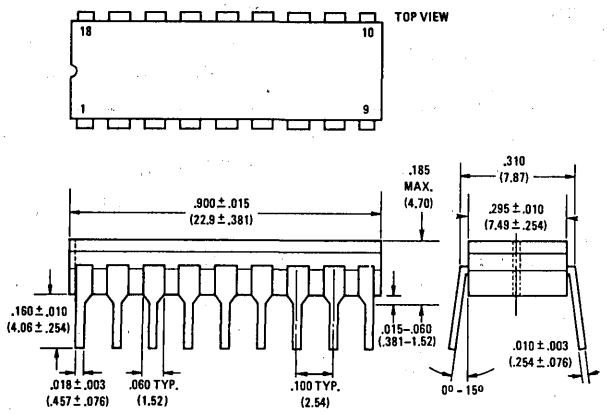
Branding: All devices are branded with the part number and EIA date code.

Aged Products: Product that has been held for more than 24 months will be reinspected prior to shipment to group A inspection requirements.

Additional Requirements: Sample Group A electrical tests are performed on a lot acceptance basis.

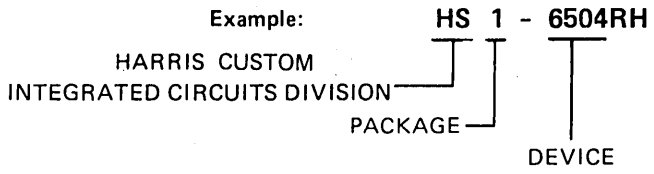
Packaging

18 LEAD CERAMIC DIP



1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions ± .010 (± 0.25mm) unless otherwise shown.

Ordering Information



PACKAGE

FLAT PACK	9-
CERDIP	1-

NOTICE: Harris Semiconductor's products are sold by description only. Harris Semiconductor reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders.

Sales Offices

EASTERN REGION

8300 Greensboro Drive
McLean, Virginia 22102
(703) 448-5400
TWX: 710-833-0340

Five Old Concord Road
Burlington, MA 01803
(617) 273-1020
TWX: 710-332-1074

106 Seventh Street
Garden City, NY 11530
(516) 747-6776
TWX: 510-220-1527

WESTERN REGION

1503 South Coast Drive
Suite 320
Costa Mesa, CA 92626
(714) 957-6557
TWX: 910-595-1533

EAST COAST

7040 Lake Ellenor Drive
Suite 113
Orlando, FL 32809
(305) 851-9450

MIDWEST REGION

2850 Metro Office Park
Bloomington, MN 55420
(612) 854-3224
TWX: 910-576-3418

HOME OFFICE

P.O. Box 883
Melbourne, FL 32901
(305) 729-5585
TWX: 510-959-6259

EUROPEAN

Harris Systems Ltd.
Semiconductor Programs Division
P.O. Box 27
145 Farnham Road
Slough SL1 4XD
United Kingdom
Tel: 34666
TWX: 848174

HARRIS

CUSTOM INTEGRATED CIRCUITS DIVISION

HARRIS

HS-6508RH

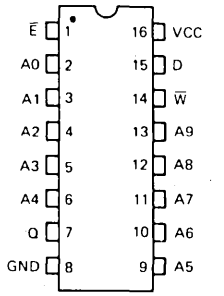
1024 x 1 CMOS RAM

Features

- FUNCTIONAL TOTAL DOSE . . . . . 2×10^4 RAD Si
- LATCH-UP FREE TO . . . . . 5.0×10^{11} RAD Si/sec
- LOW STANDBY POWER . . . . . 550 μW MAX
- LOW OPERATING POWER . . . . . 25mW/MHz MAX
- FAST ACCESS TIME . . . . . 300nsec MAX
- TTL COMPATIBLE IN/OUT
- HIGH OUTPUT DRIVE – 2 TTL LOADS
- HIGH NOISE IMMUNITY
- ON-CHIP ADDRESS REGISTER
- MILITARY TEMPERATURE RANGE
- THREE-STATE OUTPUTS
- 16 PIN PACKAGE FOR HIGH DENSITY

Pinout

TOP VIEW



A – Address Input
$\overline{E}$ – Chip Enable
$\overline{W}$ – Write Enable
D – Data Input
Q – Data Output

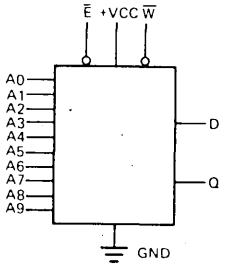
Description

The HS-6508RH is a 1024 by 1 static CMOS RAM fabricated using the HARRIS Programs Division radiation hardened self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

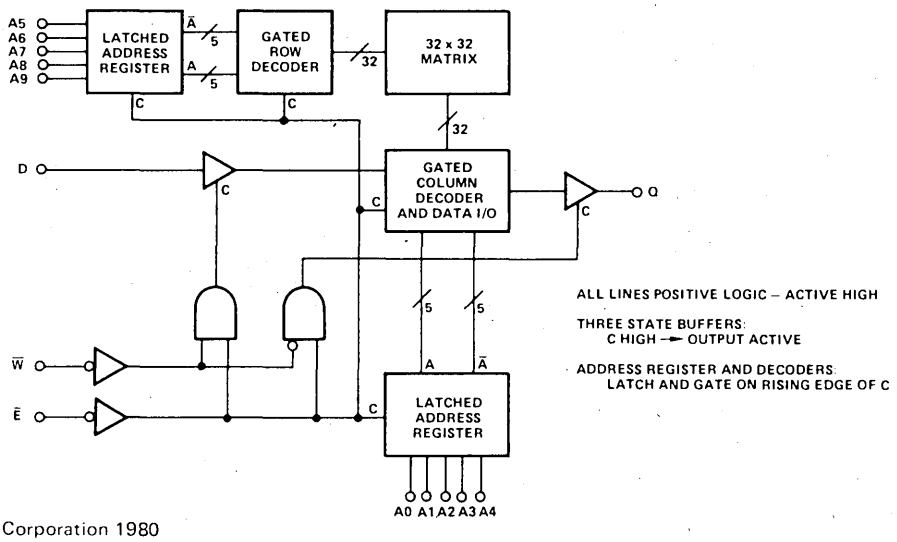
On-chip latches are provided for addresses allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HS-6508RH is a fully static RAM and may be maintained in any state for an indefinite period of time.

Logic Symbol



Functional Diagram



ALL LINES POSITIVE LOGIC – ACTIVE HIGH

THREE STATE BUFFERS:
C HIGH → OUTPUT ACTIVE

ADDRESS REGISTER AND DECODERS:
LATCH AND GATE ON RISING EDGE OF C

Symbols and Abbreviations

This data sheet utilizes a new set of specification nomenclature. This new format is an IEEE and JEDEC supported standard for semiconductor memories. It is intended to clarify the symbols, abbreviations and definitions, and to make all memory data sheets consistent. We believe that, once acclimated, you will find this standardized format easy to read and use.

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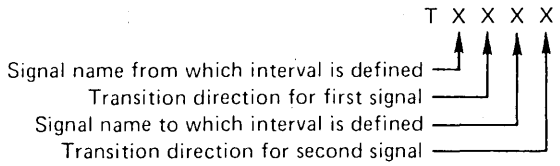
I (Current)
P (Power)
C (Capacitance)

The second letter specifies input (I) or output (O), and the third letter indicates the high (H), low (L) or off (Z) state of the pin during measurements. Examples:

VIL — Input Low Voltage
IOZ — Output Leakage Current

TIMING PARAMETER ABBREVIATIONS

All timing abbreviations use upper case characters with no subscripts. The initial character is always T and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal point specify the signal name and the signal transitions. Thus the format is:



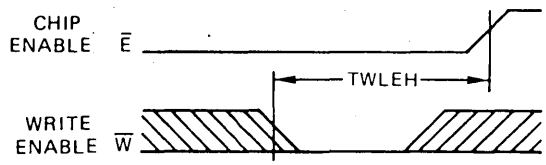
Signal Definitions:

A = Address
D = Data In
Q = Data Out
W = Write Enable
E = Chip Enable
S = Chip Select
G = Output Enable

Transition Definitions:

H = Transition to High
L = Transition to Low
V = Transition to Valid
X = Transition to Invalid or Don't Care
Z = Transition to Off (High Impedance)

EXAMPLE:



The example shows Write pulse setup time defined as TWLEH-Time from Write enable Low to chip Enable High.

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address set-up time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WAVEFORMS

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	—	HIGH IMPEDANCE

ABSOLUTE MAXIMUM RATINGS

Supply Voltage -VCC	-0.3V to 7.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

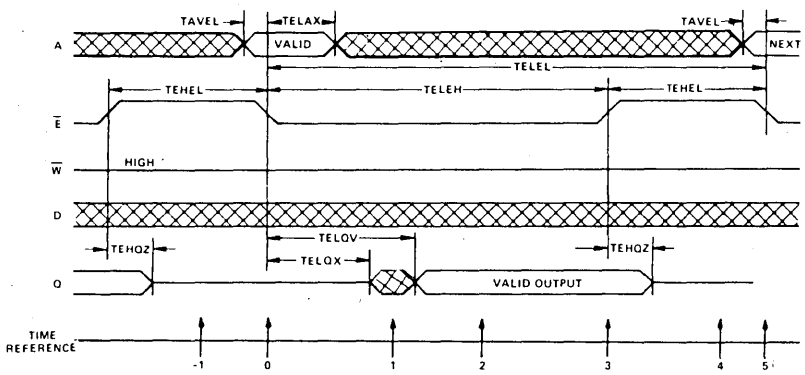
Operating Supply Voltage -VCC	4.5V to 5.5V
Operating Temperature	-55°C to +125°C

ELECTRICAL CHARACTERISTICS ⑤

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100		10	100	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VI ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3		1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5		5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 3.2mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -3mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10		6	10	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300		160	250	ns	④
	TAVQV	Address Access Time		310		160	260	ns	④
	TELQX	Chip Enable Output Enable Time		200		60	170	ns	④
	TWLQZ	Write Enable Output Disable Time		200		60	170	ns	④
	TEHQZ	Chip Enable Output Disable Time		200		60	170	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		250	160		ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		130	90		ns	④
	TAVEL	Address Setup Time	10		10	0		ns	④
	TELAX	Address Hold Time	70		50	40		ns	④
	TDVWH	Data Setup Time	130		100	80		ns	④
	TWHDX	Data Hold Time	0		0	0		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	160		130	100		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	160		130	100		ns	④
	TWLWH	Write Enable Pulse Width	160		130	100		ns	④
	TELEL	Read or Write Cycle Time	450		380	250		ns	④

NOTES:
1. All devices guaranteed at worst case limits. Room temp., 5 volt data provided for information and not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC Test Conditions: Inputs – TRISE = TFALL = 20nsec; Outputs – 1 TTL load and 50pF. All timing measurements at 1/2 VCC.
5. Pre-Radiation characteristics. See Radiation effects section for Post-Radiation characteristics.

Read Cycle

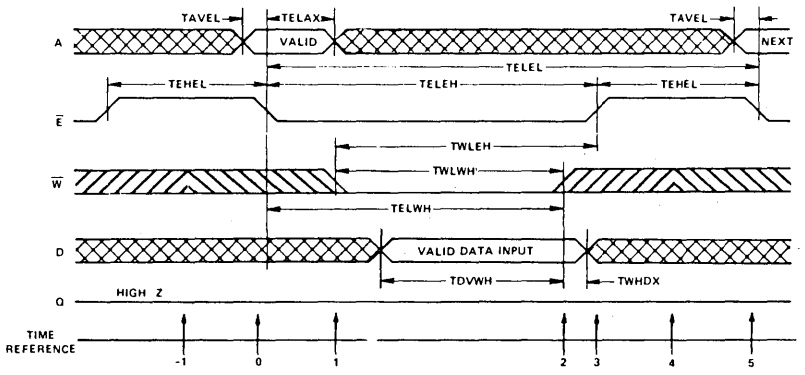


TRUTH TABLE

TIME REFERENCE	INPUTS Ē	W̄	A	D	OUTPUTS Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↘	H	V	X	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	X	OUTPUT ENABLED
2	L	H	X	X	V	OUTPUT VALID
3	↗	H	X	X	V	READ ACCOMPLISHED
4	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

In the HS-6508RH Read Cycle, the address information is latched into the on-chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address setup and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the data output becomes enabled; however, the data is not valid until during time (T = 2). $\overline{W}$ must remain high for the read cycle. After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the chip and force the output buffer to a high impedance state. After the required $\overline{E}$ high time (TEHEL) the RAM is ready for the next memory cycle (T = 4).

Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS Ē	W̄	A	D	OUTPUTS Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↘	X	V	X	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	↘	X	X	Z	WRITE PERIOD BEGINS
2	L	↗	X	V	Z	DATA IS WRITTEN
3	↗	H	X	X	Z	WRITE COMPLETED
4	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The write cycle is initiated by the falling edge of $\overline{E}$ which latches the address information into the on-chip registers. The write portion of the cycle is defined as both $\overline{E}$ and $\overline{W}$ being low simultaneously. $\overline{W}$ may go low anytime during the cycle provided that the write enable pulse setup time (TWLEH) is met. The write portion of the cycle is terminated by the first rising edge of either $\overline{E}$ or $\overline{W}$. Data setup and hold times must be referenced to the terminating signal.

If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may remain low until all desired locations have been written. When this method is used, data setup and hold times must be referenced to the rising edge of $\overline{E}$. By positioning the $\overline{W}$ pulse at different times within the $\overline{E}$ low time (TELEH), various types of write cycles may be performed.

If the $\overline{E}$ low time (TELEH) is greater than the $\overline{W}$ pulse (TWLWH) plus an output enable time (TELQX), a combination read write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH). The data input and data output pins may be tied together for use with a common I/O data bus structure. When using the RAM in this method allow a minimum of one output disable time (TWLQZ) after $\overline{W}$ goes low before applying input data to the bus. This will insure that the output buffers are not active.

Radiation Screening Procedure

(1) Two (2) probed good samples per wafer will be selected from $\geq$20% of the wafers in a run. (All wafers in a "run" will have been processed together through all high temperature processing steps and through metallization.)

(2) The sample die shall be assembled and tested for functionality.

(3) The sample devices shall be subjected to a Total Dose Radiation level of 2×10^4 Rad Si ($\pm$10%) from a Gamma Cell 220 Cobalt 60 source or equivalent. The samples shall be biased at 5 volts with all inputs high. The dose rate shall be between 50 rads/sec and 200 rads/sec.

(4) I_{CCSB} at V_{CC} = 5 volts will be measured and recorded for each device within one hour ($\pm$15 minutes) after irradiation. The lot will be accepted only if the average of these measured values is $\leq$10mA.

Radiation Effects

The HS-6508RH is a radiation hardened memory processed with the same mask set as is used for HARRIS' equivalent commercial part. Latchup free operation, achieved by the use of special starting material and improved total dose hardness, is obtained with special high temperature processing cycles. These process techniques can, in principal, be applied to any standard HARRIS CMOS product.

The primary failure mode under exposure to ionizing radiation is an increase in static leakage current (ICCSB). Functional failure due to the increased leakage currents will typically occur for dose levels in excess of 5×10^4 RAD-SI. AC and DC parameters other than ICC will change less than 10% for total dose levels under 5×10^4 RAD-SI. The excess leakage currents will anneal at room temperature and are typically reduced by a factor of 3-10 within 24 hours after irradiation.

On a production basis, HARRIS is able to perform screens only for total dose hardness. Transient radiation tests, however, have shown the following results:

Latchup free to doses $\geq 5 \times 10^{11}$ rads/sec.
Upset (loss of stored data) typically $\geq 10^8$ rads/sec.

HARRIS SEMICONDUCTOR PRODUCT FLOW
MIL-M-38510/MIL-STD-883, METHOD 5004 CLASS B

100% SCREENING PROCEDURE

	SCREEN	MIL-STD-883 METHOD/COND.
1	Internal Visual	2010 Cond. B.
2	Stabilization Bake	1008 Cond. C (24 hrs. minimum)
3	Temperature Cycling	1010 Cond. C
4	Constant Acceleration	2001 Cond. E; Y1 plane
5	Seal: (A) Fine (B) Gross	1014 Cond. A or B 1014 Cond. C2
6	Initial Electrical	Harris Specifications
7	Burn-In Test	1015, 160 hrs. @ 125°C (or equivalent) (Burn-In circuits enclosed)
8	Final Electrical 100% go-no-go	Tested at Worst Case Operating Conditions
9	External Visual	2009 Sample Inspection

Note:

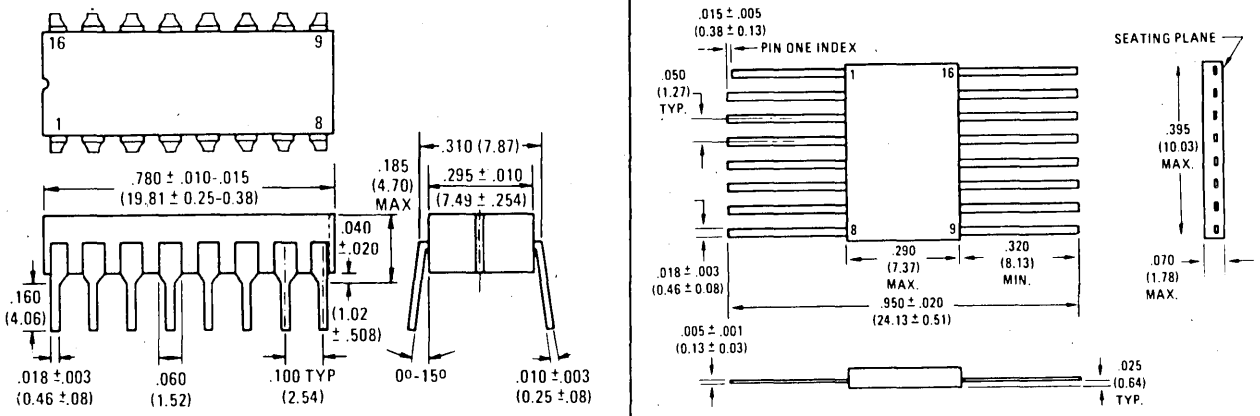
Traceability: All devices are assigned date code identification that provides traceability back to the inspection lot.

Branding: All devices are branded with the part number and EIA date code.

Aged Products: Product that has been held for more than 24 months will be reinspected prior to shipment to group A inspection requirements.

Additional Requirements: Sample Group A electrical tests are performed on a lot acceptance basis.

Packaging



1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions ± .010 (± 0.25mm) unless otherwise shown.

Ordering Information

Example: HS 1 - 6508 RH

- HS 1 - HARRIS PROGRAMS DIVISION
- 1 - PACKAGE
- 6508 - DEVICE
- RH - VERSION

PACKAGE

FLAT PACK	9-
CERDIP	1-

NOTICE: Harris Semiconductor's products are sold by description only. Harris Semiconductor reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders.

HARRIS

HS-6514RH

1024 x 4 CMOS RAM

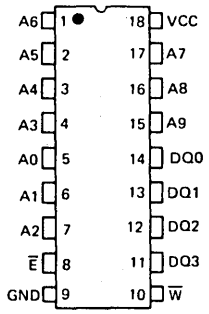
SEPTEMBER 1982 ***Preliminary***

Features

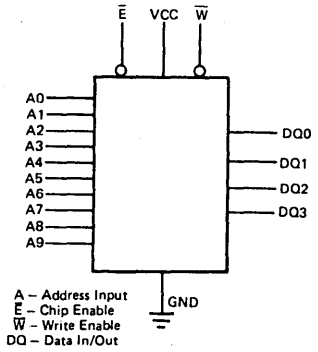
- LOW POWER STANDBY — 1250μW MAX.
- LOW POWER OPERATION — 35mW/MHz MAX.
- FUNCTIONAL TOTAL DOSE — 1×10^5 RAD Si
- DATA UPSET — $>10^8$ RADS Si/sec
- LATCH - UP FREE TO — $>5 \times 10^{11}$ RAD Si/soc
- TTL COMPATIBLE INPUT/OUTPUT
- COMMON DATA IN/OUT
- THREE - STATE OUTPUTS
- STANDARD JEDEC PINOUT
- FAST ACCESS TIME — 200 nsec TYP.
- MILITARY TEMPERATURE RANGE
- 18 PIN PACKAGE FOR HIGH DENSITY
- ON - CHIP ADDRESS REGISTER

Pinout

TOP VIEW



Logic Symbol



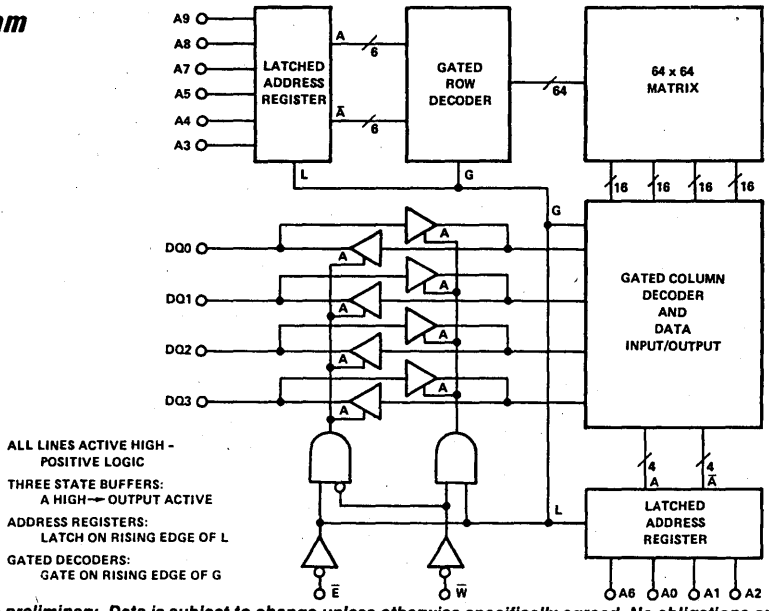
Description

The HS–6514RH is a 1024 x 4 static CMOS RAM fabricated using the Harris Custom Integrated Circuits Division radiation hardened self-aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

On-chip latches are provided for the addresses allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance state for use in expanded memory systems.

The HS–6514RH is a fully static RAM and may be maintained in any state for an indefinite period of time.

Functional Diagram



Information on this device is preliminary. Data is subject to change unless otherwise specifically agreed. No obligations are assumed for notice of change or future manufacture of this device.

CAUTION: These devices are sensitive to electrostatic discharge.

Symbols and Abbreviations

This data sheet utilizes a new set of specification nomenclature. This new format is an IEEE and JEDEC supported standard for semiconductor memories. It is intended to clarify the symbols, abbreviations and definitions, and to make all memory data sheets consistent. We believe that, once acclimated, you will find this standardized format easy to read and use.

ELECTRICAL PARAMETER ABBREVIATIONS

All abbreviations use upper case letters with no subscripts. The initial symbol is one of these four characters:

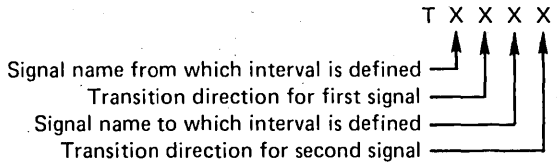
V (Voltage)
I (Current)
P (Power)
C (Capacitance)

The second letter specifies input (I) or output (O), and the third letter indicates the high (H), low (L) or off (Z) state of the pin during measurements. Examples:

VIL — Input Low Voltage
IOZ — Output Leakage Current

TIMING PARAMETER ABBREVIATIONS

All timing abbreviations use upper case characters with no subscripts. The initial character is always T and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal point specify the signal name and the signal transitions. Thus the format is:



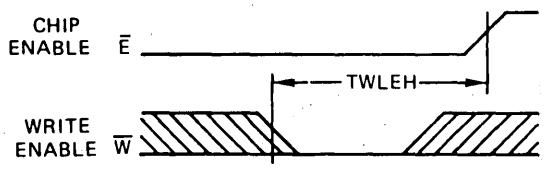
Signal Definitions:

A = Address
D = Data In
Q = Data Out
W = Write Enable
E = Chip Enable
S = Chip Select
G = Output Enable

Transition Definitions:

H = Transition to High
L = Transition to Low
V = Transition to Valid
X = Transition to Invalid or Don't Care
Z = Transition to Off (High Impedance)

EXAMPLE:



The example shows Write pulse setup time defined as TWLEH-Time from Write enable Low to chip Enable High.

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address set-up time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WAVEFORMS

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	—	HIGH IMPEDANCE

ABSOLUTE MAXIMUM RATINGS

Supply Voltage – (VCC -GND)	-0.3V to +7.0V
Input or Output Voltage Applied	(GND -0.3V) to (VCC + 0.3V)
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage	4.5V to 5.5V
Operating Temperature	–55°C to +125°C

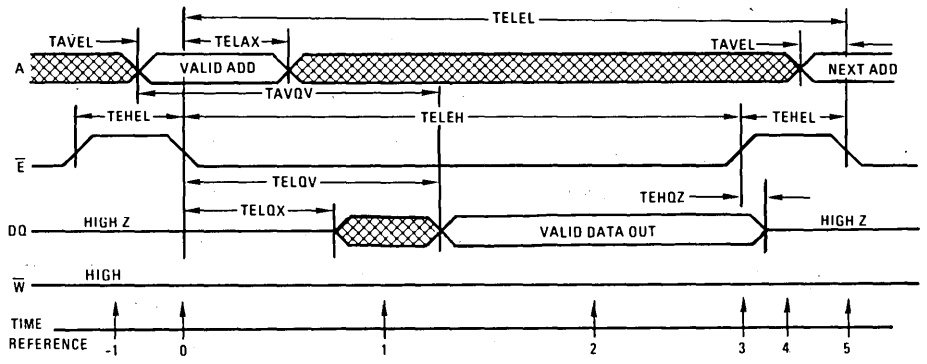
CAUTION: To prevent permanent damage to this device, care should be exercised to insure that the absolute maximum ratings for supply voltages, temperature and voltage or current at any pin is not exceeded during both static and dynamic operation.

ELECTRICAL CHARACTERISTICS ⑤

	SYMBOL	PARAMETER	TEMP. & VCC= OPERATING RANGE MIN	TEMP. & VCC= OPERATING RANGE MAX	TEMP = 25°C ① VCC = 5.0V TYPICAL PRE RAD	TEMP = 25°C ① VCC = 5.0V TYPICAL POST RAD	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		250	6	6	µA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		7	4.5		mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retenetion Current		50	4	4	µA	IO=0 VI=VCC or GND VCC=3.0V
	VCCDR	Data Retention Voltage		3.0	2.6	1.8	V	
	II	Input Leakage Current	–1	+1	0	0	µA	GND≤VI≤VCC
	IIOZ	Input/Output Leakage Current	–10	+10	±0.5	±0.5	µA	GND≤VIO≤VCC
	VIL	Input Low Voltage	–0.3	0.8	1.5	1.3	V	
	VIH	Input High Voltage	VCC –2.0	VCC +0.3	2.7	2.3	V	
	VOL	Output Low Voltage		0.40	0.2	0.15	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.7	4.1	V	IO = –1.0mA
	CI	Input Capacitance ③		8.0	5.0	5.0	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance ③		10.0	6.0	6.0	pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300	170	200	ns	④
	TAVQV	Address Access Time		320	170	200	ns	④
	TELQX	Chip Enable Output Enable Time		100	40	50	ns	④
	TWLQZ	Write Enable Output Disable Time	20	100	40	50	ns	④
	TEHQZ	Chip Enable Output Disable Time		100	40	50	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		170	200	ns	④
	TEHEL	Chip Enable Pulse Positive Width	120		40	80	ns	④
	TAVEL	Address Setup Time	20		–10	0	ns	④
	TELAX	Address Hold Time	100		50	60	ns	④
	TWLWH	Write Enable Pulse Width	300		150	150	ns	④
	TWLEH	Write Enable Pulse Setup Time	300		150	150	ns	④
	TELWH	Write Enable Pulse Hold Time	300		150	150	ns	④
	TDVWH	Data Setup Time	200		100	120	ns	④
	TWHDZ	Data Hold Time	30		10	15	ns	④
	TWLDV	Write Data Delay Time	100		50	60	ns	④
	TWLEL	Early Output High-Z Time	0		–20	–15	ns	④
	TEHWH	Late Output High-Z Time	0		–20	–15	ns	④
	TELEL	Read or Write Cycle Time	420		210	280	ns	④

NOTES:
1. All devices guaranteed at worst case limits. Room temp., 5 volt data provided for information and not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Post Rad data at TD = 1 X 10^5.
3. Capacitance sampled and guaranteed – not 100% rested.
4. AC test Conditions: Inputs: TRISE = TFALL≤ 20nsec; Outputs: 1 TTL Load and 50pF. All timing measurements at 1/2 VCC.
5. Pre-Radiation and Post-Radiation limits.

Read Cycle

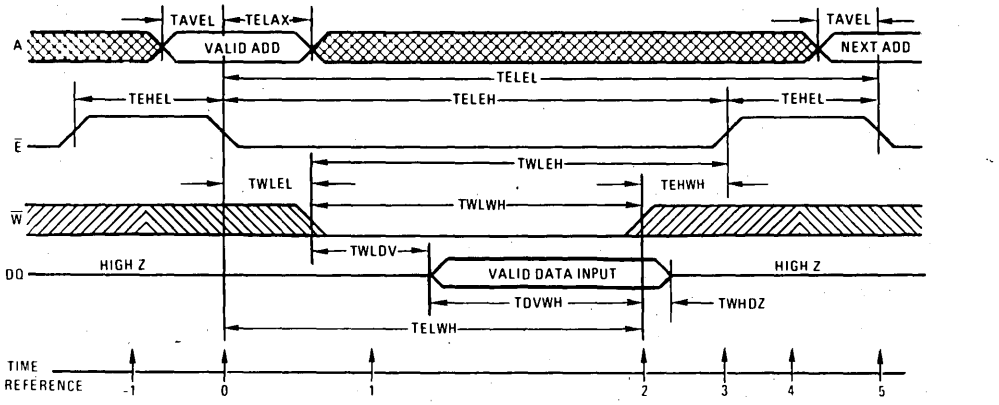


TRUTH TABLE

TIME REFERENCE	INPUTS Ē	W̄	A	DATA I/O DQ	FUNCTION
1	H	X	X	Z	MEMORY DISABLED
0	↘	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	OUTPUT ENABLED
2	L	H	X	V	OUTPUT VALID
3	↗	H	X	V	READ ACCOMPLISHED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address setup and hold time requirements must be met. After the required hold time the addresses may change state without affecting device operation. During time (T = 1) the outputs become enabled but data is not valid until time (T = 2). $\overline{W}$ must remain high throughout the read cycle. After the data has been read $\overline{E}$ may return high (T = 3). This will force the output buffers into a high impedance mode at time (T = 4). The memory is now ready for the next cycle.

Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS Ē	W̄	A	DQ	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	↘	X	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	X	Z	WRITE PERIOD BEGINS
2	L	↗	X	V	DATA IN IS WRITTEN
3	↗	H	X	Z	WRITE COMPLETED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The write cycle is initiated by the falling edge of $\overline{E}$ (T = 0), which latches the address information in the on chip registers. There are two basic types of write cycles, which differ in the control of the common data-in/data-out bus.

Case 1: $\overline{E}$ falls before $\overline{W}$ falls

The output buffers may become enabled (reading) if $\overline{E}$ falls before $\overline{W}$ falls. $\overline{W}$ is used to disable (three-state) the outputs so input data can be applied. TWLDV must be met to allow the $\overline{W}$ signal time to disable the outputs before applying input data. Also, at the end of the cycle the outputs may become active if $\overline{W}$ rises before E. The RAM outputs will disable (three-state) after E rises (TEHQZ). In this type of write cycle TWLEL and TEHWH may be ignored.

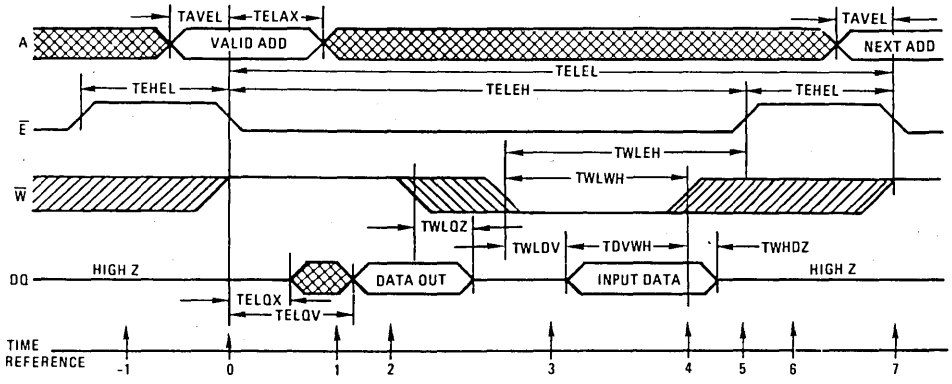
Case 2: $\overline{E}$ falls equal to or after $\overline{W}$ falls, and $\overline{E}$ rises before or equal to $\overline{W}$ rises.

This $\overline{E}$ and $\overline{W}$ control timing will guarantee that the data outputs will stay disabled throughout the cycle, thus simplifying the data input timing. TWLEL and TEHWH must be met but TWLDV becomes meaningless and can be ignored. In this cycle TDVWH and TWHDZ become TDVEH and TEHDZ. In other words, reference data setup and hold times to the $\overline{E}$ rising edge.

	IF	OBSERVE	IGNORE
Case 1	$\overline{E}$ falls before $\overline{W}$	TWLDV	TWLEL
Case 2	$\overline{E}$ falls after $\overline{W}$ & $\overline{E}$ rises before $\overline{W}$	TWLEL TEHWH	TWLDV TWHDV

If a series of consecutive write cycles are to be performed, $\overline{W}$ may be held low until all desired locations have been written (an extension of Case 2).

Read Modify Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	DATAI/O DQ	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	↘	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	READ MODE, OUTPUT ENABLED
2	L	H	X	V	READ MODE, OUTPUT VALID
3	L	L	X	Z	WRITE MODE, OUTPUT HIGH Z
4	L	↗	X	V	WRITE MODE, DATA IS WRITTEN
5	↗	H	X	Z	WRITE COMPLETED
6	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
7	↘	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

If the pulse width of $\overline{W}$ is relatively short in relation to that of $\overline{E}$ a combination read-write cycle may be performed. If $\overline{W}$ remains high for the first part of the cycle, the outputs will become active during time (T = 1). Data out will be valid during time (T = 2). After the data is read, $\overline{W}$ can go low. After minumum TWLWH, $\overline{W}$ may return high. The information just written may now be read or $\overline{E}$ may return high, disabling the output buffers and preparing the device for the next cycle. Any number or sequence of read-write operations may be performed while $\overline{E}$ is low providing all timing requirements are met.

NOTES:

In the above descriptions the numbers in parenthesis (T = n) refer to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

Radiation Screening Procedure

(1) Two (2) probed good samples per wafer will be selected from $\geq$ 20% of the wafers in a run. (All wafers in a "run" will have been processed together through all high temperature processing steps and through metallization.)

(2) The sample die shall be assembled and tested to the production test program for proper operation.

(3) The sample devices shall be subjected to a Total Dose Radiation level of 1×10^5 Rad Si (±10%) from a Gamma Cell 220 Cobalt 60 source or equivalent. The samples shall be biased at 5 volts with all inputs high. The dose rate shall be between 50 rads/sec and 200 rads/sec.

(4) The samples will be tested to the data sheet limits within one hour (±15 minutes) after irradiation. The lot will be accepted only if all units, exclusive of non-radiation failures, meet the data sheet limits.

Radiation Effects

The HS-6514RH is an RH memory designed to survive in a radiation environment and to meet the electrical characteristics and be pin compatible to the Harris equivalent commercial part. Latchup free operation, achieved by the use of special starting material and improved total dose hardness, is obtained with special high temperature processing cycles. These process techniques can, in principle, be applied to any standard HARRIS CMOS product.

On a production basis, HARRIS only performs screens for total dose hardness to a level of 1×10^5 rad-Si. Transient radiation tests, however, have shown the following results:

Latchup free to doses $\geq 5 \times 10^{11}$ rads/sec.
Upset (loss of stored data) typically $\geq 10^8$ rads/sec.

Test Product Flow

HARRIS SEMICONDUCTOR PRODUCT FLOW
MIL-STD-883 METHOD 5004 CLASS B

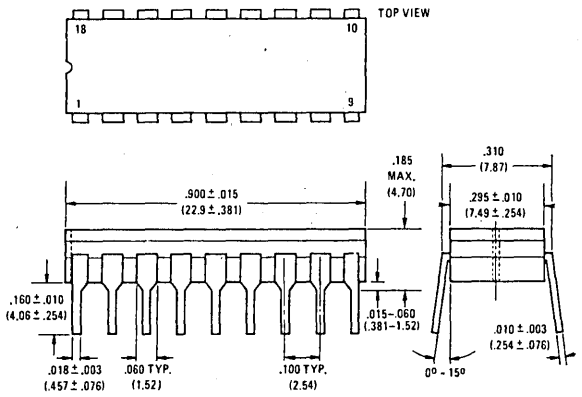
100% SCREENING PROCEDURE

	SCREEN	MIL-STD-883 METHOD/COND.
1	Internal Visual	2010 Cond. B.
2	Stabilization Bake	1008 Cond. C (24 hrs. minimum)
3	Temperature Cycling	1010 Cond. C
4	Constant Acceleration	2001 Cond. E; Y1 plane
5	Seal: A Fine B Gross	1014 Cond. A or B 1014 Cond. C2
6	Initial Electrical	Harris Specifications
7	Burn-In Test	1015, 160 hrs. @ 125°C (or equivalent) (Burn-In circuits enclosed)
8	Final Electrical 100% go-no-go	Tested at Worst Case Operating Conditions
9	External Visual	2009 Sample Inspection

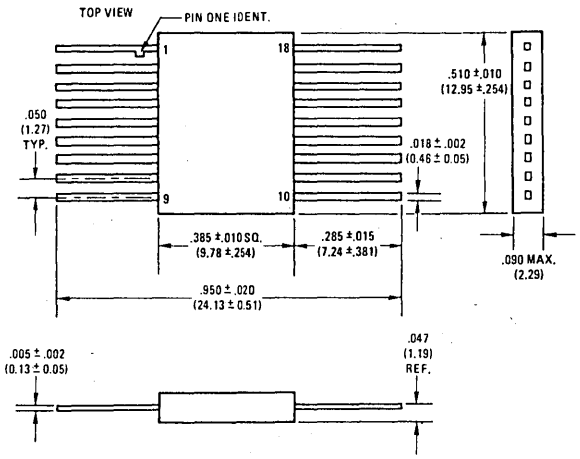
Notes:
- Traceability: All devices are assigned date code identification that provides traceability back to the inspection lot.
- Branding: All devices are branded with the part number and EIA date code.
- Aged Products: Product that has been held for more than 24 months will be reinspected prior to shipment to group A inspection requirements.
- Additional Requirements: Sample Group A electrical tests are performed on a lot acceptance basis.

Packaging

18 LEAD CERAMIC DIP



18 LEAD CERPACK



1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions ±.010 (±0.25mm) unless otherwise shown.

Ordering Information

Example: HS 1 - 6514RH

- HS — HARRIS CUSTOM INTEGRATED CIRCUITS DIVISION
- 1 — PACKAGE
- 6514 — DEVICE
- RH — VERSION

PACKAGE

FLAT PACK	9-
CERDIP	1-

NOTICE: Harris Semiconductor's products are sold by description only. Harris Semiconductor reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders.

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(612) 854-3224
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HARRIS

CUSTOM INTEGRATED CIRCUITS DIVISION

HS-6551RH

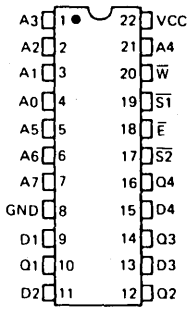
256 x 4 CMOS RAM

Features

- FUNCTIONAL TOTAL DOSE — 2×10^4 RAD Si
- LATCH-UP FREE TO — 5.0×10^{11} RAD Si/sec
- LOW STANDBY POWER — 550μW MAX
- LOW OPERATING POWER — 25mW/MHz MAX
- FAST ACCESS TIME — 300ns MAX
- TTL COMPATIBLE IN/OUT
- HIGH OUTPUT DRIVE - 1TTL LOAD
- HIGH NOISE IMMUNITY
- ON CHIP ADDRESS REGISTER
- MILITARY TEMPERATURE RANGE
- THREE-STATE OUTPUTS
- 22 PIN PACKAGE FOR HIGH DENSITY

Pinout

TOP VIEW



A – Address Input
$\overline{E}$ – Chip Enable
$\overline{S}$ – Chip Select
$\overline{W}$ – Write Enable
D – Data Input
Q – Data Output

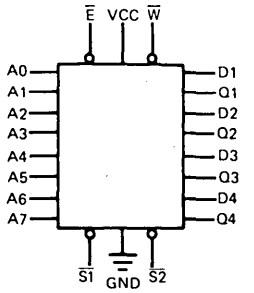
Description

The HS-6551RH is a 256 by 4 static CMOS RAM fabricated using the Harris Programs Division radiation hardened self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

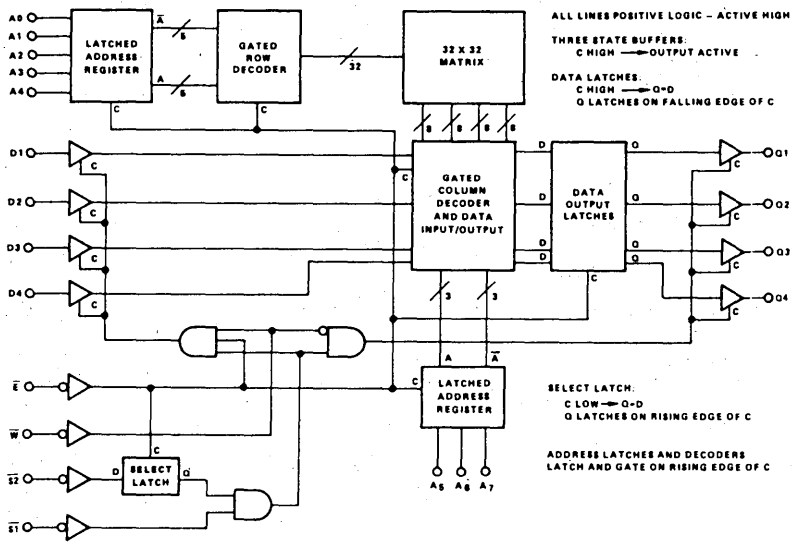
On-chip latches are provided for addresses, allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HS-6551RH is a fully static RAM and may be maintained in any state for an indefinite period of time.

Logic Symbol



Functional Diagram



Symbols and Abbreviations

This data sheet utilizes a new set of specification nomenclature. This new format is an IEEE and JEDEC supported standard for semiconductor memories. It is intended to clarify the symbols, abbreviations and definitions, and to make all memory data sheets consistent. We believe that, once acclimated, you will find this standardized format easy to read and use.

ELECTRICAL PARAMETER ABBREVIATIONS

All abbreviations use upper case letters with no subscripts. The initial symbol is one of these four characters:

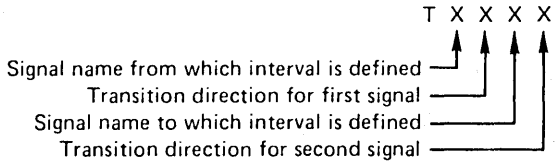
V (Voltage)
I (Current)
P (Power)
C (Capacitance)

The second letter specifies input (I) or output (O), and the third letter indicates the high (H), low (L) or off (Z) state of the pin during measurements. Examples:

VIL — Input Low Voltage
IOZ — Output Leakage Current

TIMING PARAMETER ABBREVIATIONS

All timing abbreviations use upper case characters with no subscripts. The initial character is always T and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal point specify the signal name and the signal transitions. Thus the format is:



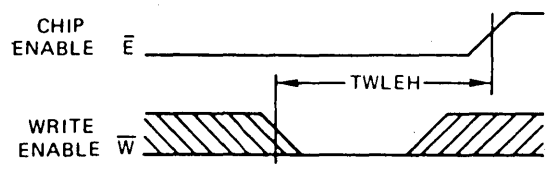
Signal Definitions:

A = Address
D = Data In
Q = Data Out
W = Write Enable
E = Chip Enable
S = Chip Select
G = Output Enable

Transition Definitions:

H = Transition to High
L = Transition to Low
V = Transition to Valid
X = Transition to Invalid or Don't Care
Z = Transition to Off (High Impedance)

EXAMPLE:



The example shows Write pulse setup time defined as TWLEH-Time from Write enable Low to chip Enable High.

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address set-up time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WAVEFORMS

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	—	HIGH IMPEDANCE

ABSOLUTE MAXIMUM RATINGS

Supply Voltage -VCC	+7V
Applied Input or Output Voltage	GND -0.3V VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage -VCC	4.5V to 5.5V
Operating Temperature	-55°C to +125°C

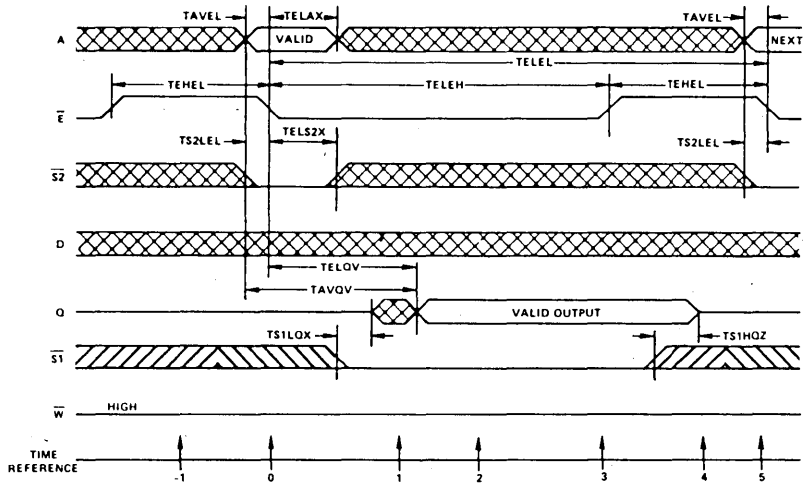
CAUTION: To prevent permanent damage to this device, care should be exercised to insure that the absolute maximum ratings for supply voltages, temperature and voltage or current at any pin is not exceeded during both static and dynamic operation.

ELECTRICAL CHARACTERISTICS ⑤

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100		10	100	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VI ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 2.0mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -1.0mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10		6	10	pF	VI = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300		160	240	ns	④
	TAVQV	Address Access Time		300		150	240	ns	④
	TS1LQX	Chip Select 1 Output Enable Time		150		60	120	ns	④
	TWLQZ	Write Enable Output Disable Time		150		60	120	ns	④
	TS1HQZ	Chip Select 1 Output Disable Time		150		60	120	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		240	160		ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		70	50		ns	④
	TAVEL	Address Setup Time	15		0	-10		ns	④
	TS2LEL	Chip Select 2 Setup Time	15		0	-10		ns	④
	TELAX	Address Hold Time	70		50	40		ns	④
	TELS2X	Chip Select 2 Hold Time	70		50	40		ns	④
	TDVWH	Data Setup Time	150		120	100		ns	④
	TWHDX	Data Hold Time	0		0	0		ns	④
	TWLS1H	Chip Select 1 Write Pulse Setup Time	180		150	120		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	180		150	120		ns	④
	TS1LWH	Chip Select 1 Write Pulse Hold Time	180		150	120		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	180		150	120		ns	④
	TWLWH	Write Enable Pulse Width	180		150	120		ns	④
	TELEL	Read or Write Cycle Time	450		270	170		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC Test Conditions: Inputs – TRISE = TFALL = 20nsec; Outputs – 1 TTL load and 50pF. All timing measurements at 1/2 VCC.
5. Pre-radiation characteristics, see radiation effects for Post-Radiation characteristics.

Read Cycle



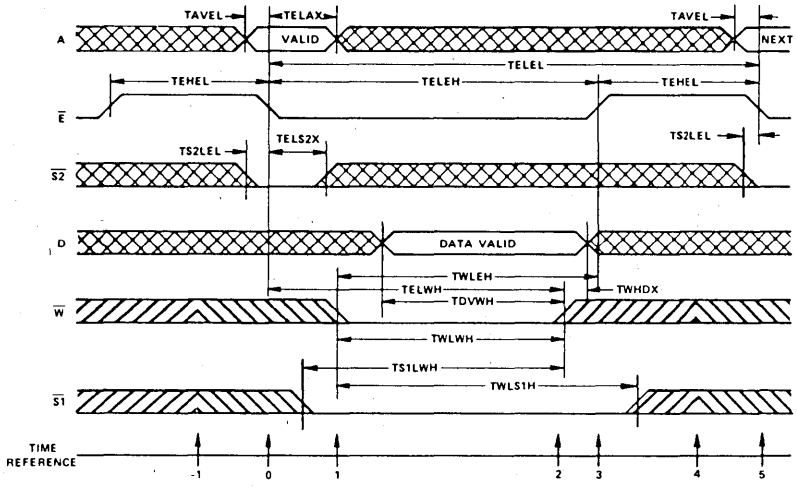
TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{S1}$	$\overline{S2}$	$\overline{W}$	A	D	OUTPUTS Q	FUNCTION
-1	H	H	X	X	X	X	Z	MEMORY DISABLED
0	↘	X	L	H	V	X	Z	ADDRESSES AND $\overline{S2}$ ARE LATCHED, CYCLE BEGINS
1	L	L	X	H	X	X	X	OUTPUT ENABLED BUT UNDEFINED
2	L	L	X	H	X	X	V	DATA OUTPUT VALID
3	↗	L	X	H	X	X	V	OUTPUTS LATCHES, VALID DATA
4	H	H	X	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	L	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The HS-6551RH Read Cycle is initiated by the falling edge of $\overline{E}$. This signal latches the input address word and $\overline{S2}$ into on-chip registers providing that minimum setup and hold times are met. After the required hold time, these inputs may change state without affecting device operation. $\overline{S2}$ acts as a higher order address and simplifies decoding. For the output to be read, $\overline{E}$, $\overline{S1}$ must be low and $\overline{W}$ must be high. $\overline{S2}$ must have been latched low on the falling edge of $\overline{E}$. The output data will be valid at access time (TELQV).

The HS-6551RH has output data latches that are controlled by $\overline{E}$. On the rising edge of $\overline{E}$ the present data is latched and remains in that state until $\overline{E}$ falls. Either or both $\overline{S1}$ or $\overline{S2}$ may be used to force the output buffers into a high impedance state.

Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS E	S1	S2	W	A	D	OUTPUTS Q	FUNCTION
-1	H	H	X	X	X	X	Z	MEMORY DISABLED
0	↘	X	L	X	V	X	Z	CYCLE BEGINS, ADDRESSES AND $\overline{S2}$ ARE LATCHED
1	L	L	X	↘	X	X	Z	WRITE PERIOD BEGINS
2	L	L	X	↗	X	V	Z	DATA IN IS WRITTEN
3	↗	X	X	H	X	X	Z	WRITE IS COMPLETED
4	H	H	X	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	L	X	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

In the Write Cycle the falling edge of $\overline{E}$ latches the addresses and $\overline{S2}$ into on-chip registers. $\overline{S2}$ must be latched in the low state to enable the device. The write portion of the cycle is defined as $\overline{E}$, $\overline{W}$, $\overline{S1}$ being low and $\overline{S2}$ being latched low simultaneously. The $\overline{W}$ line may go low at any time during the cycle providing that the write pulse setup times (TWLEH and TWLS1H) are met. The write portion of the cycle is terminated on the first rising edge of either $\overline{E}$, $\overline{W}$, or $\overline{S1}$.

If a series of consecutive write cycles are to be executed, the $\overline{W}$ line may be held low until all desired locations have been written. If this method is used, data setup and hold times must be referenced to the first rising edge of $\overline{E}$ or $\overline{S1}$. By positioning the write pulse at different times within the $\overline{E}$ and $\overline{S1}$ low time (TELEH) various types of write cycles may be performed. If the $\overline{S1}$ low time (TS1LS1H) is greater than the $\overline{W}$ pulse plus an output enable time (TS1LQX), a combination read-write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH).

The HS-6551RH may be used on a common I/O bus structure by tying the input and output pins together. The multiplexing is accomplished internally by the $\overline{W}$ line. In the write cycle, when $\overline{W}$ goes low, the output buffers are forced to a high impedance state. One output disable time delay (TWLQZ) must be allowed before applying input data to the bus.

Radiation Screening Procedure

(1) Two (2) probed good samples per wafer will be selected from $\geq$20% of the wafers in a run. (All wafers in a "run" will have been processed together through all high temperature processing steps and through metallization.)

(2) The sample die shall be assembled and tested for functionality.

(3) The sample devices shall be subjected to a Total Dose Radiation level of 2×10^4 Rad Si ($^+$10%) from a Gamma Cell 220 Cobalt 60 source or equivalent. The samples shall be biased at 5 volts with all inputs high. The dose rate shall be between 50 rads/sec and 200 rads/sec.

(4) I_{CCSB} at V_{CC} = 5 volts will be measured and recorded for each device within one hour ($\pm$15 minutes) after irradiation. The lot will be accepted only if the average of these measured values is $\leq$10mA.

Radiation Effects

The HS-6551RH is a radiation hardened memory processed with the same mask set as is used for HARRIS' equivalent commercial part. Latchup free operation is achieved by the use of special starting material and improved total dose hardness is obtained with special high temperature processing cycles. These process techniques can, in principal, be applied to any standard HARRIS CMOS product.

The primary failure mode under exposure to ionizing radiation is an increase in static leakage current (ICCSB). Functional failure due to the increased leakage currents will typically occur for dose levels in excess of 5×10^4 RAD-Si. AC and DC parameters other than ICC will change less than 10% for total dose levels under 5×10^4 RAD-Si. The excess leakage currents will anneal at room temperature and are typically reduced by a factor of 3-10 within 24 hours after irradiation.

On a production basis, HARRIS is able to perform screens only for total dose hardness. Transient radiation tests, however, have shown the following results:

Latchup free to doses $\geq 5 \times 10^{11}$ rads/sec.
Upset (loss of stored data) typically $\geq 10^8$ rads/sec.

HARRIS SEMICONDUCTOR PRODUCT FLOW
MIL-M-38510/MIL-STD-883, METHOD 5004 CLASS B

100% SCREENING PROCEDURE

	SCREEN	MIL-STD-883 METHOD/COND.
1	Internal Visual	2010 Cond. B.
2	Stabilization Bake	1008 Cond. C (24 hrs. minimum)
3	Temperature Cycling	1010 Cond. C
4	Constant Acceleration	2001 Cond. E; Y1 plane
5	Seal: (A) Fine (B) Gross	1014 Cond. A or B 1014 Cond. C2
6	Initial Electrical	Harris Specifications
7	Burn-In Test	1015, 160 hrs. @ 125°C (or equivalent) (Burn-In circuits enclosed)
8	Final Electrical 100% go-no-go	Tested at Worst Case Operating Conditions
9	External Visual	2009 Sample Inspection

Note:

Traceability: All devices are assigned date code identification that provides traceability back to the inspection lot.

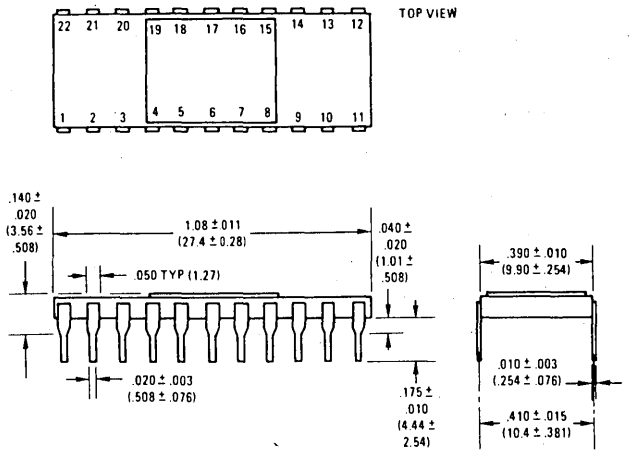
Branding: All devices are branded with the part number and EIA date code.

Aged Products: Product that has been held for more than 24 months will be reinspected prior to shipment to group A inspection requirements.

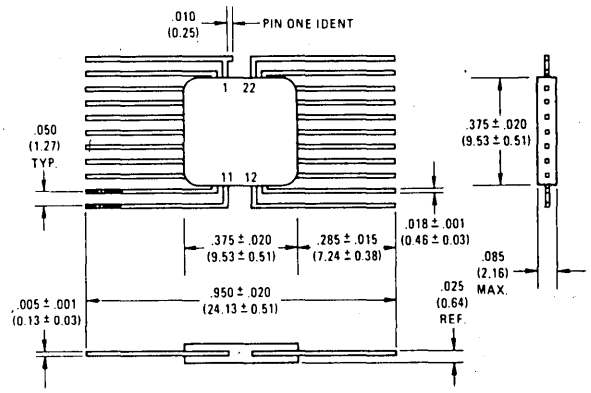
Additional Requirements: Sample Group A electrical tests are performed on a lot acceptance basis.

Packaging

22 LEAD SIDE BRAZE DIP



22 LEAD FLATPACK



1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions ± .010 (± 0.25mm) unless otherwise shown.

Ordering Information

Example: HS 1 - 6551 RH

- HS — HARRIS PROGRAMS DIVISION
- 1 — PACKAGE
- 6551 — DEVICE
- RH — VERSION

PACKAGE

FLAT PACK	9-
CERDIP	1-

HS-6564RH

Radiation Resistant 8K x 8, 16K x CMOS RAM

OCTOBER 1982

Preliminary

Features

- LOW POWER STANDBY — 8.8 mW MAX
- LOW POWER OPERATION — 308 mW/MHz MAX
- DATA RETENTION — 3.0 V MIN
- TTL COMPATIBLE IN/OUT
- THREE STATE OUTPUTS
- FAST ACCESS TIME — 250 nsec TYP.
- MILITARY TEMPERATURE RANGE — -55°C TO +125°C
- ON CHIP ADDRESS REGISTERS
- ORGANIZABLE 8K×8 OR 16K×4
- 40 PIN DIP PINOUT 2.000" × 0.900"
- FUNCTIONAL TOTAL DOSE — 1×10^5 RAD Si
- DATA UPSET — $>10^8$ RAD Si/SEC
- LATCH-UP FREE TO — $>5\times10^{11}$ RAD Si/SEC

Description

The HS-6564RH is a radiation resistant 64K bit, synchronous CMOS RAM. It consists of 16 HS-6504RH 4K×1 radiation resistant CMOS RAMs, in leadless carriers, mounted on a ceramic substrate. The HS-6564RH is configured as an extra wide, standard length 40 pin DIP. The memory appears to the system as an array of 16 4K×1 static RAMs. The array is organized as two 8K by 4 blocks of RAM sharing only the address bus. The data inputs, data outputs, chip enables and write enables are separate for each block of RAM. This allows the user to organize the HS-6564RH RAM as either an 8K by 8 or a 16K by 4 array.

This 64K memory provides a unique blend of low power CMOS semiconductor technology and advanced packaging techniques. The HS-6564RH is intended for use in radiation environments where a large amount of RAM is needed, and where power consumption and board space are prime concerns. On-chip latches are provided for addresses, data input and data output allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance for use in expanded memory arrays. The guaranteed low voltage data retention characteristics allow easy implementation of non-volatile read/write memory by using very small batteries mounted directly on the memory circuit board.

Pinout

TOP VIEW

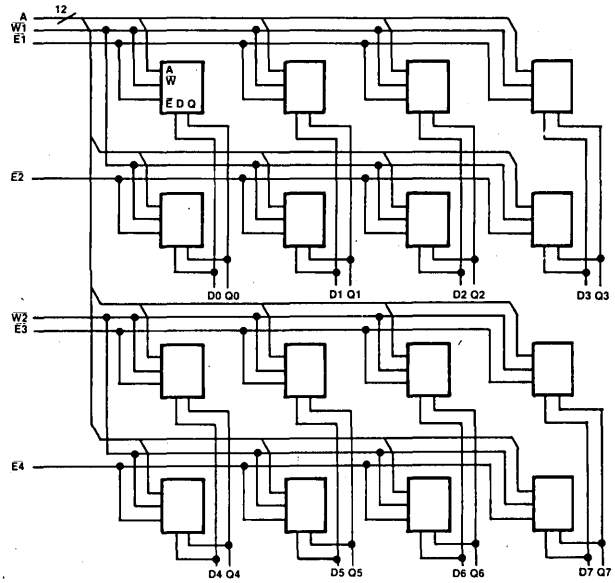
*GND	1	40	VCC*
Q4	2	39	Q0
D4	3	38	D0
Q5	4	37	Q1
D5	5	36	D1
A0	6	35	A6
A1	7	34	A7
A4	8	33	A8
$\overline{E}3$	9	32	$\overline{E}1$
*$\overline{W}2$	10	31	$\overline{W}1$
$\overline{W}2$	11	30	$\overline{W}1$*
$\overline{E}4$	12	29	$\overline{E}2$
A11	13	28	A3
A10	14	27	A2
A9	15	26	A5
D6	16	25	D2
Q6	17	24	Q2
D7	18	23	D3
Q7	19	22	Q3
*VCC	20	21	GND*

***NOTES:**

Pins 20 and 40 (VCC) are internally connected. Similarly pins 1 and 21 (Ground) are connected. The user is advised to connect all four VCC pins and Ground pins to his board busses. This will improve power distribution across the array and will enhance decoupling.

Pin 10 is internally connected to pin 11, and pin 30 is connected to pin 31. For those users wishing to preserve board compatibility with possible future RAM arrays, we recommend connections to the write lines be made at pins 11 and 31, leaving pins 10 and 30 free for future expansion.

Functional Diagram



Information on this device is preliminary. Data is subject to change unless otherwise specifically agreed. No obligations are assumed for notice of change or future manufacture of this device.

CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

Symbols and Abbreviations

This data sheet utilizes a new set of specification nomenclature. This new format is an IEEE and JEDEC supported standard for semiconductor memories. It is intended to clarify the symbols, abbreviations and definitions, and to make all memory data sheets consistent. We believe that, once acclimated, you will find this standardized format easy to read and use.

ELECTRICAL PARAMETER ABBREVIATIONS

All abbreviations use upper case letters with no subscripts. The initial symbol is one of these four characters:

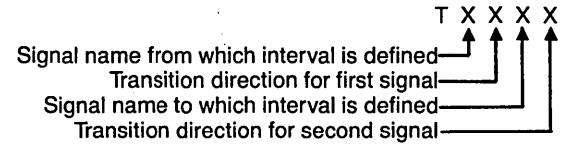
V (Voltage)
I (Current)
P (Power)
C (Capacitance)

The second letter specifies input (I) or output (O), and the third letter indicates the high (H), low (L) or off (Z) state of the pin during measurements. Examples:

VIL – Input Low Voltage
IOZ – Output Leakage Current

TIMING PARAMETER ABBREVIATIONS

All timing abbreviations use upper case characters with no subscripts. The initial character is always T and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal point specify the signal name and the signal transitions. Thus the format is:



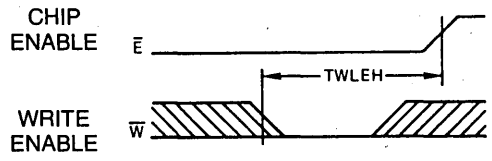
Signal Definitions:

A = Address
D = Data In
Q = Data Out
W = Write Enable
E = Chip Enable
S = Chip Select
G = Output Enable

Transition Definitions:

H = Transition to High
L = Transition to Low
V = Transition to Valid
X = Transition to Invalid or Don't Care
Z = Transition to Off (High Impedance)

EXAMPLE:



The example shows Write pulse setup time defined as TWLEH-Time from Write enable Low to chip Enable High.

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address set-up time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WAVEFORMS

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	—	HIGH IMPEDANCE

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage – (VCC – GND)	−0.3V to +7.0V
Input or Output Voltage Applied	(GND −0.3V) to (VCC +0.3V)
Storage Temperature	−65°C to +150°C

OPERATING RANGE

Operating Supply Voltage	+4.5 to +5.5V
Operating Temperature	−55°C to +125°C

** CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

ELECTRICAL CHARACTERISTICS ④

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TYPICAL TEMP. = 25°C ① VCC = 5.0V PRE RAD	TYPICAL TEMP. = 25°C ① VCC = 5.0V POST RAD	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		1600	80	80	μA	IO = 0 VI = VCC or GND
	ICCOP1	Operating Supply Current (8K × 8) ②		56	36		mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCOP2	Operating Supply Current (16K × 4) ②		28	18		mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		1600	48	48	μA	IO = 0, VCC = 3.0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	3.0		2.6	1.8	V	
	IIA	Address Input Leakage	−20	+20			μA	GND≤VI≤VCC
	IID1	Data Input Leakage (8K × 8)	−3	+3			μA	GND≤VI≤VCC
	IID2	Data Input Leakage (16K × 4)	−5	+5			μA	GND≤VI≤VCC
	IIE1	Enable Input Leakage (8K × 8)	−10	+10			μA	GND≤VI≤VCC
	IIE2	Enable Input Leakage (16K × 4)	−5	+5			μA	GND≤VI≤VCC
	IIW	Write Enable Input Leakage (Each)	−10	+10			μA	GND≤VI≤VCC
	IOZ1	Output Leakage (8K × 8)	−20	+20	±4	±4	μA	GND≤VO≤VCC
	IOZ2	Output Leakage (16K × 4)	−40	+40	±8	±8	μA	GND≤VO≤VCC
	VIL	Input Low Voltage	−0.3	0.8	1.5	1.3	V	
	VIH1	Input High Level (Except $\overline{E}$ and $\overline{W}$)	VCC −1.5	VCC +0.3	2.7	2.3	V	
	VIH2	Input High Level ($\overline{E}$ and $\overline{W}$)	VCC −1.0	VCC +0.3	2.9	1.9	V	
	VOL	Output Low Voltage		0.4	0.2	0.15	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		4.6	4.0	V	IO = −1.0mA
	CIA	Address Input Capacitance ③		200			pF	f = 1MHz, VI = VCC or GND
	CID1	Data Input Capacitance (8K × 8) ③		50			pF	f = 1MHz, VI = VCC or GND
	CID2	Data Input Capacitance (16K × 4) ③		100			pF	f = 1MHz, VI = VCC or GND
	CIE1	Enable Input Capacitance (8K × 8) ③		160			pF	f = 1MHz, VI = VCC or GND
	CIE2	Enable Input Capacitance (16K × 4) ③		80			pF	f = 1MHz, VI = VCC or GND
	CIW	Write Enable Input Capacitance (Each) ③		100			pF	f = 1MHz, VI = VCC or GND
	CO1	Output Capacitance (8K × 8) ③		50			pF	f = 1MHz, VO = VCC or GND
	CO2	Output Capacitance (16K × 4) ③		100			pF	f = 1MHz, VO = VCC or GND

NOTES:

① Each individual RAM in the leadless carrier is fully tested at worst case limits of temperature and voltage. The complete assembled HS-6564RH array is tested at room temperature only. The worst case parameters are guaranteed over the specified temperature and voltage ranges. Room temperature, 5 volt data is provided for information purposes and is not guaranteed.

② Operating supply current is proportional to operating frequency. ICCOP is specified at an operating frequency of 1MHz, indicating repetive accessing at a 1μs rate. Operation at slower rates will decrease ICCOP proportionally.

③ Capacitance sampled and guaranteed – not 100% tested.

④ Pre Radiation and Post Radiation limits.

ELECTRICAL CHARACTERISTICS

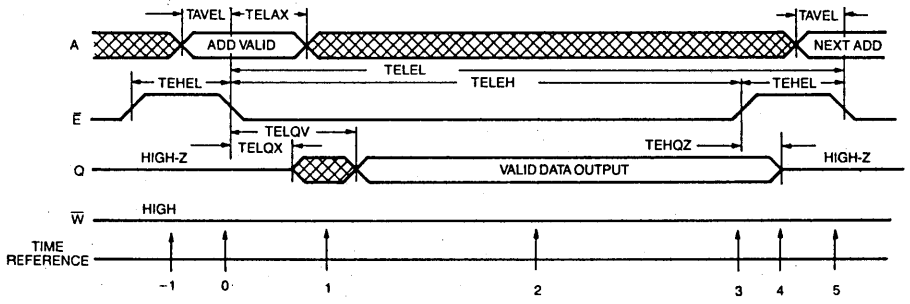
	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TYPICAL TEMP. = 25°C VCC = 5.0V PRE RAD	TYPICAL TEMP. = 25°C VCC = 5.0V POST RAD	UNITS	TEST CONDITIONS
A.C.	TELQV	Chip Enable Access		350	200	230	ns	⑤
	TAVQV	Address Access (TAVQV=TELQV+TAVEL)		400	220	260	ns	
	TELQX	Output Enable	20	120	70	80	ns	
	TEHQZ	Output Disable		130	80	90	ns	
	TELEL	Read or Write Cycle	480		250	320	ns	
	TELEH	Chip Enable Low	350		200	230	ns	
	TEHEL	Chip Enable High	130		50	90	ns	
	TAVEL	Address Setup	50		20	30	ns	
	TELAX	Address Hold	50		30	35	ns	
	TWLWH	Write Enable Low	150		90	100	ns	
	TWLEH	Write Enable Setup	250		190	190	ns	
	TWLEL	Early Write Setup (Write Mode)	10		−5	0	ns	
	TWHEL	Write Enable Read Setup	10		−5	0	ns	
	TELWX	Early Write Hold (Write Mode)	100				ns	
	TDVWL	Data Setup	10		−5	20	ns	
	TDVEL	Early Write Data Setup	10		−5	20	ns	
	TWLDX	Data Hold	100		70	80	ns	
	TELDX	Early Write Data Hold	100		70	80	ns	
	TQVWL	Data Valid to Write (Read-Modify-Write)	0		0	0	ns	⑤

NOTES:

⑤ AC Test Conditions:

Inputs – Trise = Tfall ≤ 20ns.
Outputs – CLOAD = 100pF.
Timing measured at 1.5V reference level.

Read Cycle

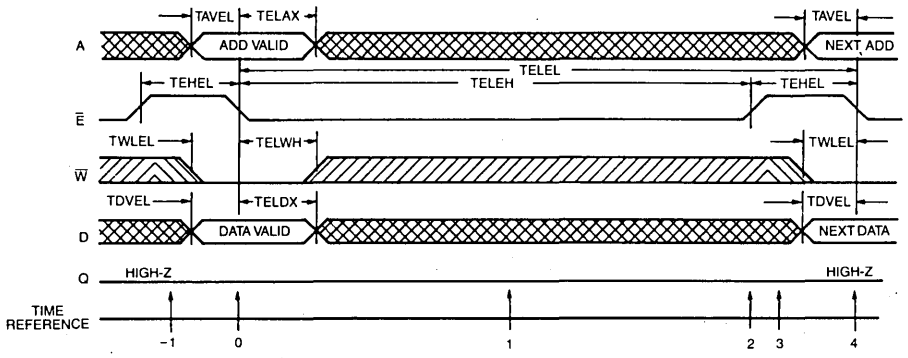


TRUTH TABLE

TIME REFERENCE	INPUTS E	INPUTS W	INPUTS A	OUTPUT Q	FUNCTION
−1	H	X	X	Z	MEMORY DISABLED
0	↘	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	OUTPUT ENABLED
2	L	H	X	V	OUTPUT VALID
3	↗	H	X	V	READ ACCOMPLISHED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS −1)
5	↘	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address set up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but data is not valid until during time (T = 2). $\overline{W}$ must remain high until after time (T = 2). After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the output buffer and ready the RAM for the next memory cycle (T = 4).

Early Write Cycle

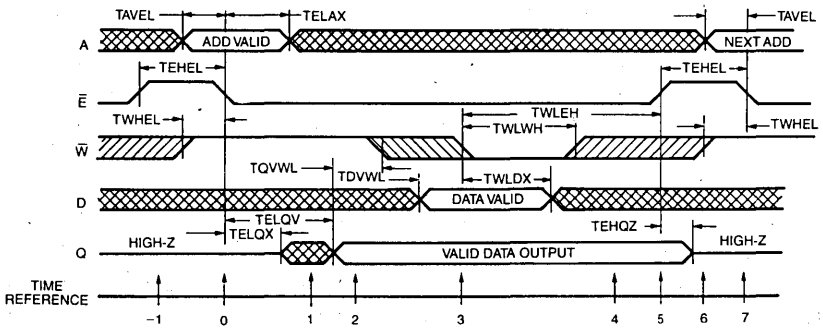


TRUTH TABLE

TIME REFERENCE	INPUTS Ē	W̄	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↘	L	V	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	X	X	X	Z	WRITE IN PROGRESS INTERNALLY
2	↗	X	X	X	Z	WRITE COMPLETED
3	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
4	↘	L	V	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The early write cycle is the only cycle where the output is guaranteed not to become active. On the falling edge of Ē (T = 0), the addresses, the write signal, and the data input are latched in on chip registers. The logic value of W̄ at the time Ē falls determines the state of the output buffer for that cycle. Since W̄ is low when Ē falls, the output buffer is latched into the high impedance state and will remain in that state until Ē returns high (T = 2). For this cycle, the data input is latched by Ē going low; therefore data set up and hold times should be referenced to Ē. When Ē (T = 2) returns to the high state, the output buffer disables and all signals are unlatched. The device is now ready for the next cycle.

Read Modify Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS Ē	W̄	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↘	H	V	X	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	X	OUTPUT ENABLED
2	L	H	X	X	V	OUTPUT VALID, READ AND MODIFY TIME
3	L	↘	X	V	V	WRITE BEGINS, DATA IS LATCHED
4	L	X	X	X	V	WRITE IN PROGRESS INTERNALLY
5	↗	X	X	X	V	WRITE COMPLETED
6	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
7	↘	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The read modify write cycle begins as all other cycles on the falling edge of Ē (T = 0). The W̄ line should be high at (T = 0) in order to latch the output buffers in the active state. During (T = 1) the output will be active but not valid until (T = 2). On the falling edge of the W̄ (T = 3) the data present at the output and input are latched. The W̄ signal also latches itself on its low going edge. All input signals excluding Ē have been latched and have no further effect on the RAM. The rising edge of Ē (T = 5) completes the write portion of the cycle and unlatches all inputs and output. The output goes to a high impedance and the RAM is ready for the next cycle.

NOTES: In the above descriptions the numbers in parenthesis (T = n) refer to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

Board Size Tradeoffs

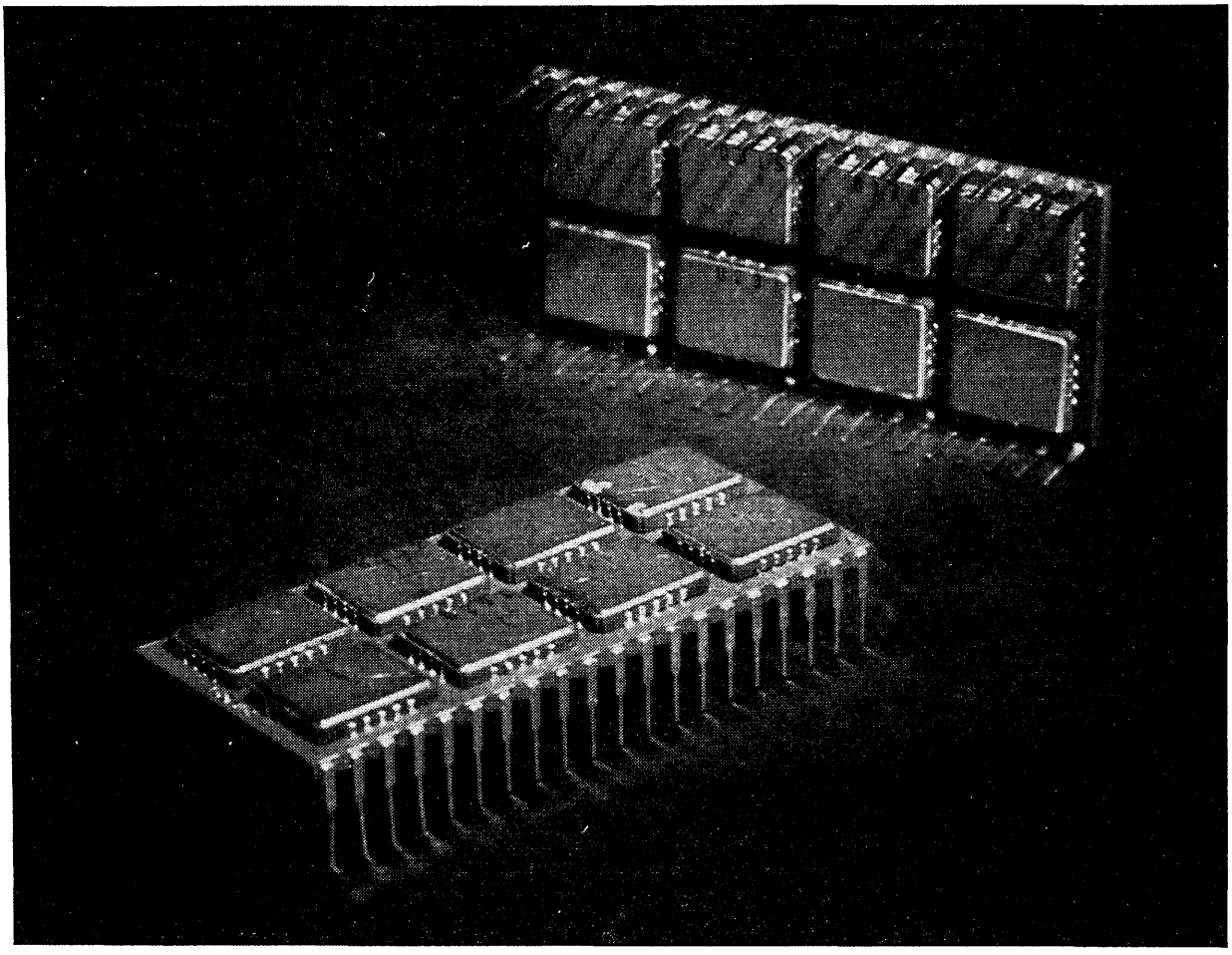
Printed circuit board real estate is a costly commodity. Actual board costs depend on layout tolerances, density, complexity, number of layers, choice of board material, and other factors.

The following table compares board space for 16 standard DIP 4K RAMs to the HS-6564RH RAM array. Both fine line, close tolerance layout and standard "easy" layout board sizes are shown in the comparison.

64K ARRAY OF 16 4K RAMs ON A PC BOARD V.S. THE HS-6564RH

PACKAGE	CIRCUIT SUBSTRATE	SIZE
18 Pin DIP	Standard Two Sided PCB	12 to 15 sq. in.
18 Pin DIP	Fine Line or Multilayer PCB	9 to 11 sq. in.
18 Pin Leadless Carrier	Multilayer Alumina Substrate	3 to 5 sq. in.
HS-6564RH	Two Sided Mounting Multilayer Alumina Substrate	2 sq. in.

The cost of semiconductor circuits decline with time. If actual costs were included, they would be out of date in a very short time. We urge you to contact your local Harris office or sales representative for accurate pricing allowing cost tradeoff analysis. In your cost analysis, also consider the advantages of a lighter, smaller overall package for your system. Consider how much more valuable your system will be when the memory array size is decreased to about 1/6 of normal size.



HS-6564RH – 64K BIT CMOS RAM

Organization Guide

To Organize 8K × 8:

Connect: $\overline{E}1$ with $\overline{E}3$	(Pins 9 + 32)
$\overline{E}2$ with $\overline{E}4$	(Pins 12 + 29)
$\overline{W}1$ with $\overline{W}2$	(Pins 11 + 31)

To Organize 16K × 4:

Connect: Q0 with Q4	(Pins 2 + 39)
D0 with D4	(Pins 3 + 38)
Q1 with Q5	(Pins 4 + 37)
D1 with D5	(Pins 5 + 36)
D2 with D6	(Pins 16 + 25)
Q2 with Q6	(Pins 17 + 24)
D3 with D7	(Pins 18 + 23)
Q3 with Q7	(Pins 19 + 22)
Optional $\overline{W}1$ may be common with $\overline{W}2$	(Pins 11 + 31)

Concerns for Proper Operation of Chip Enables:

The transition between blocks of RAM requires a change in the chip enable being used. When operating in the 8K × 8 mode, use the chip enables as if there were only two, $\overline{E}1$ and $\overline{E}2$. In the 16K × 4 mode, all chip enables must be treated separately. Transitions between chip enables must be treated with the same timing constraints that apply to any one chip enable. All chip enables must be high at least one chip enable high time (TEHEL) before any chip enable can fall. More than one chip enable low simultaneously, for devices whose outputs are tied common either internally or externally, is an illegal input condition and must be avoided.

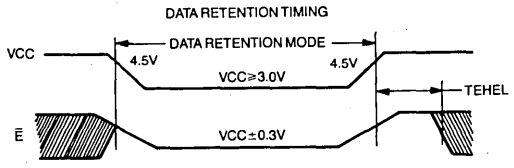
Printed Circuit Board Mounting:

The leadless chip carrier packages used in the HS-6564RH have conductive lids. These lids are electrically floating, not connected to VCC or GND. The designer should be aware of the possibility that the carriers on the bottom side could short conductors below if pressed completely down against the surface of the circuit board. The pins on the package are designed with a standoff feature to help prevent the leadless carriers from touching the circuit board surface.

Low Voltage Data Retention

HARRIS CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip Enable ($\overline{E}$) must be held high during data retention; within VCC + 0.3V to VCC − 0.3V.
2. All other inputs should be held either high (at CMOS VCC) or at ground to minimize ICCDR.
3. Inputs which are to be held high (e.g. $\overline{E}$) must be kept between VCC + 0.3V and 70% of VCC during the power up and power down transitions.
4. The RAM can begin operation one TEHEL after VCC reaches the minimum operating voltage (4.5 volts).



Radiation Screening Procedure

(1) Two (2) probed good samples per wafer will be selected from ≥ 20% of the wafers in a run. (All wafers in a "run" will have been processed together through all high temperature processing steps and through metallization.)

(2) The sample die shall be assembled and tested for functionality.

(3) The sample devices shall be subjected to a Total Dose Radiation level of 1×10^5 Rad Si (± 10%) from a Gamma Cell 220 Cobalt 60 source or equivalent. The samples shall be biased at 5 volts with all inputs high. The dose rate shall be between 50 rads/sec and 200 rads/sec.

(4) The samples will be tested to the data sheet limits within one hour (± 15 minutes) after irradiation. The lot will be accepted only if all units, exclusive of non-radiation failures, meet the data sheet limits.

Radiation Effects

The HS-6564RH is a radiation resistant memory module designed to survive in a radiation environment and to meet the electrical characteristics and be pin compatible to the Harris equivalent commercial part. Latchup free operation, achieved by the use of special starting material and improved total dose hardness, is obtained with special high temperature processing cycles. These process techniques can, in principle, be applied to any standard HARRIS CMOS product.

On a production basis, HARRIS only performs screens for total dose hardness to a level of 1×10^5 rad-Si. Transient radiation tests, however, have shown the following results:

Latchup free to doses $\geq 5 \times 10^{11}$ rads/sec.
Upset (loss of stored data) typically $\geq 10^8$ rads/sec.

Test Product Flow

HARRIS SEMICONDUCTOR PRODUCT FLOW
MIL-STD-883, METHOD 5004 CLASS B

100% SCREENING PROCEDURE*

	SCREEN	MIL-STD-883 METHOD/COND.
1	Internal Visual	2010 Cond. B.
2	Stabilization Bake	1008 Cond. C (24 hrs. minimum)
3	Temperature Cycling	1010 Cond. C
4	Constant Acceleration	2001 Cond. E; Y1 plane
5	Seal: Fine Gross	1014 Cond. A or B 1014 Cond. C2
6	Initial Electrical	Harris Specifications
7	Burn-In Test	1015, 160 hrs. @ 125°C (or equivalent)
8	Final Electrical 100% go-no-go	Tested at Worst Case Operating Conditions
9	External Visual	2009 Sample Inspection

*** ALL SCREENING IS PERFORMED AT LEADLESS CARRIER LEVEL EXCEPT FINAL ELECTRICAL**

NOTE:

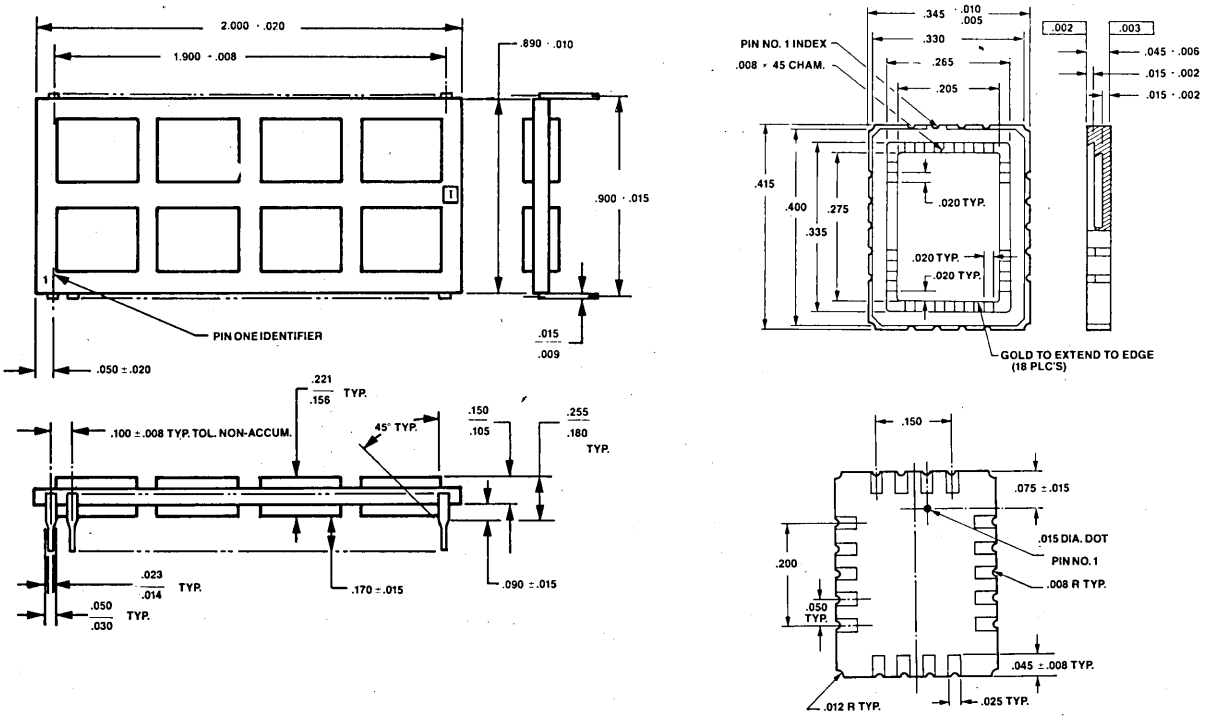
Traceability: All devices are assigned date code identification that provides traceability back to the inspection lot.

Branding: All devices are branded with the part number and EIA date code.

Aged Products: Product that has been held for more than 24 months will be reinspected prior to shipment to group A inspection requirements.

Additional Requirements: Sample Group A electrical tests are performed on a lot acceptance basis.

Packaging



NOTES:

1. ALL EXPOSED METALLIZED AREAS SHALL BE GOLD PLATED 50 MICRO INCHES MIN. THICKNESS OVER NICKEL PLATE.
2. FLATNESS PERTAINS TO METALLIZED PADS ONLY.
3. DIE ATTACH PAD TO BE ELECTRICALLY CONNECTED TO PIN NO. 18.

Sales Offices

EASTERN REGION

8300 Greensboro Drive
McLean, Virginia 22102
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TWX: 710-332-1074

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Garden City, NY 11530
(516) 747-6776
TWX: 510-220-1527

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Costa Mesa, CA 92626
(714) 957-6557
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TWX: 848174

HARRIS

CUSTOM INTEGRATED CIRCUITS DIVISION

HS-3511RH

High Slew Rate, Wideband, Radiation Resistant, Operational Amplifier

HARRIS

Preliminary

SEPTEMBER 1982

Features

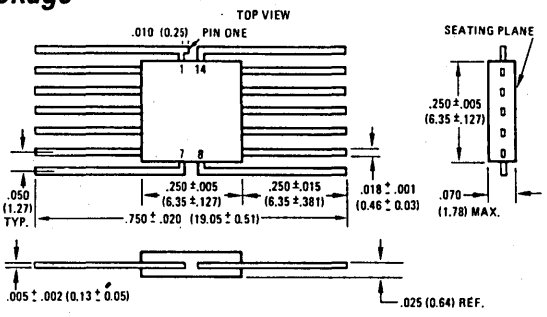
- HIGH SLEW RATE . . . . . >±22V/µs
- FAST SETTLING TIME 450ns
- WIDE POWER BANDWIDTH. 10MHz
- GAIN BANDWIDTH PRODUCT. . . . . > 20MHz
- LOW OFFSET VOLTAGE. . . . . ±5mV
- LOW POWER SUPPLY CURRENT 6.5mA
- SHORT CIRCUIT PROTECTION
- RADIATION ENVIRONMENT
  - NEUTRON FLUENCE (ϕ) $5 \times 10^{12} n/cm^2$ ($E \geq 10KeV$)
  - GAMMA RATE ($\dot{\gamma}$) . . . . . 1×10^9 RADs Si/s
  - GAMMA DOSE (γ) . . . . . 1×10^6 RADs Si

Description

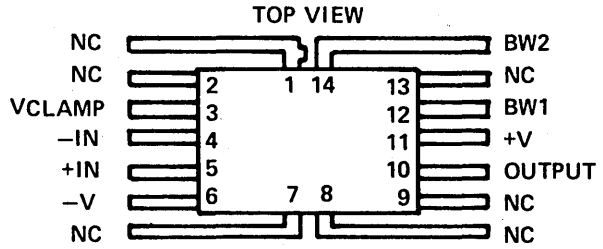
The HS-3511RH is a monolithic, high slew rate, wideband, radiation resistant, operational amplifier. It provides a bandwidth (unity gain stable) of greater than 10MHz and a slew rate in excess of 22V/µsec. Optional frequency compensation adjustment is provided. The HS-3511RH has an internal unity gain frequency compensation capacitor which is internally connected. A clamp node feature enables the user to clamp the output voltage via pin 3 which can source or sink up to 3mA for high frequency clamped switching purposes.

This device is designed to operate from −55°C to +125°C and in strategic-level radiation environments.

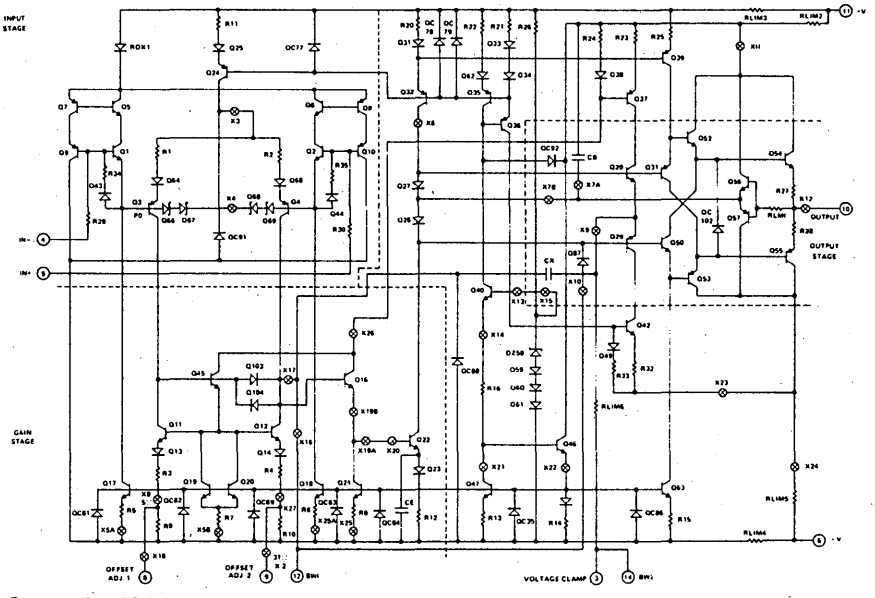
Package



Pinout



Schematic



ABSOLUTE MAXIMUM RATINGS

Voltage Between +V and −V terminals	40V	Internal Power Dissipation	625mW
Differential Input Voltage	±15V	Storage Temperature Range	−65°C to +175°C
Output Short Circuit Duration	Indefinite	Operating Temperature Range	−55°C to +125°C

CAUTION: To prevent permanent damage to this device, care should be exercised to insure that the absolute maximum ratings for supply voltages, temperature and voltage or current at any pin is not exceeded during both static and dynamic operation.

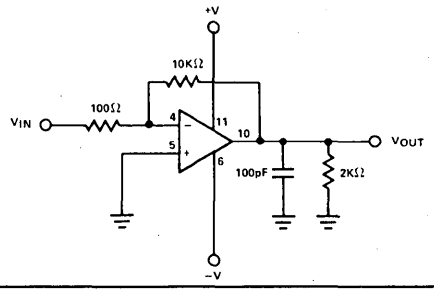
ELECTRICAL CHARACTERISTICS +V = 15V, −V = −15V, T_A = −55°C to +125°C

PARAMETER	TEMP	MIN	TYP	MAX	UNITS
Offset Voltage	25°C		1	3	mV
	125°C		2	5	mV
	−55°C		3	6	mV
Input Bias Current	25°C		35	100	nA
	125°C		50	100	nA
	−55°C			200	nA
Input Offset Current	25°C		30	100	nA
	125°C			150	nA
	−55°C			250	nA
Input Resistance	25°C		>100		MΩ
Large Signal Voltage Gain[1]	25°C	90			dB
	Full	90			dB
Common Mode Rejection Ratio[2]	25°C	80	115		dB
	Full	80	90		dB
Supply Current	25°C		5.0	6.5	mA
	125°C			6.5	mA
	−55°C			8.7	mA
Power Supply Rejection Ratio[3]	25°C	80			dB
	Full	80			dB
Output Voltage Swing	25°C	+12.5	+13.0		V
		−11.0	−12.0		V
	125°C	+12.5	+13.0		V
		−11.0	−12.0		V
	−55°C	+12.0			V
		−11.0			V
Output Short Circuit Current	25°C		27	45	mA
	125°C			45	mA
	−55°C			60	mA
Gain Bandwidth Product	25°C		12.0		MHz
	Full		10.0		MHz
Slew Rate[3, 5]	25°C	22	25		V/µs
Rise Time[4]	25°C		30	35	ns
Overshoot[4]	25°C		15	35	%
Overdrive Recovery Time	25°C		2	5	µs
Settling Time[4]	25°C		180	450	ns
	Full			450	ns
Output Clamp Voltage	25°C			0.4	V
Input Clamp (+) Icn− Current (pin 3)	25°C	−1.0		−3.3	mA
	125°C	−1.0		−3.3	mA
	−55°C	−0.8		−3.5	mA
Input Clamp (−) Icn+ Current (pin 3)	25°C	+0.5		+3.0	mA
	125°C	+0.5		+3.0	mA
	−55°C	+0.3		+3.2	mA

NOTES:

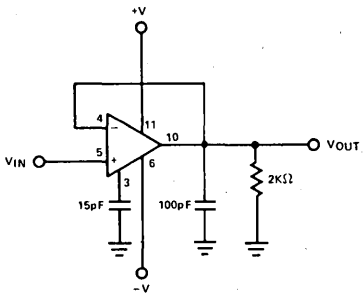
1. V_o = ±10V, R_L = 2K
2. V_{cm} = ±10V, R_L = 2K
3. ΔV = ±5.0V
4. A_V = +1, V_{IN} = 1V, R_L = 2K, C_L = 100pf
5. C_{BW} = 0, V_o = ±10V, R_L = 2K, C_L = 100pf

UNITY GAIN BANDWIDTH CIRCUIT



1. $V_{IN} = 0.2V_{pp}$ max 5.0 MHz
2. RESISTOR TOLERANCE = ±5%
3. BANDWIDTH = 5MHz X $(-V_{OUT}/V_{IN})$

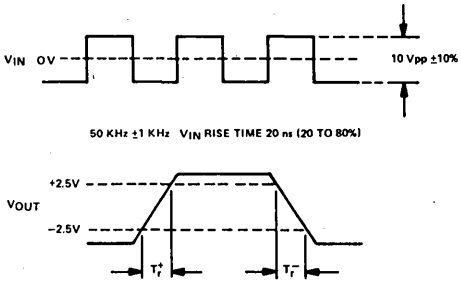
SLEW RATE CIRCUIT



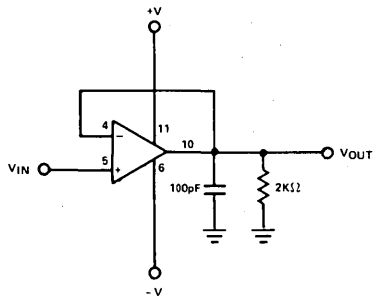
1. SLEW RATE = $\frac{5}{T_r^+ (\mu s)}$ V/μs

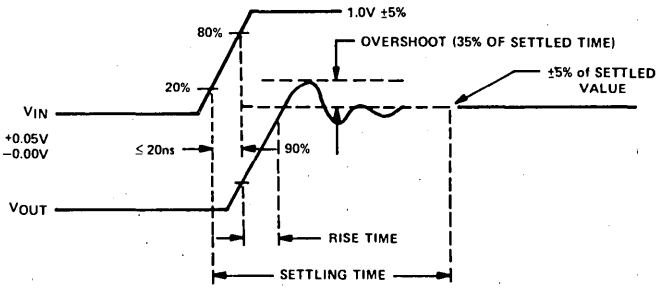
   OR — $\frac{5}{T_r^- (\mu s)}$ V/μs

2. INPUT BIAS CURRENT OF NON-INVERTING INPUT MAY INCREASE IF V_{IN} APPLIED BEFORE + V AND −V.

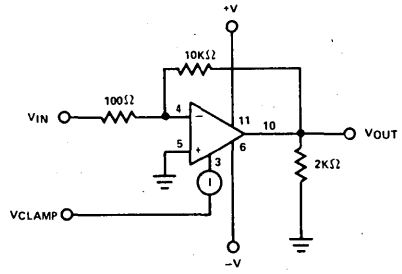


RISE TIME/SETTLING TIME CIRCUIT





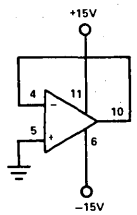
VOLTAGE CLAMP CIRCUIT



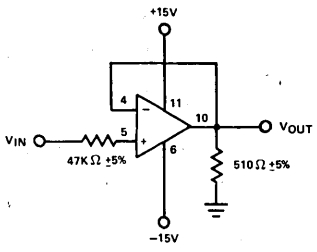
1. V_{IN} = +1.0 VDC
2. V_{CLAMP} = −3.0 VDC
3. MEASURE V_{OUT}; V_{OUT} SHALL BE WITHIN ±0.4 VDC OF V_{CLAMP}.
4. REPEAT STEPS 1, 2, 3 USING BOTH VOLTAGES OF OPPOSITE POLARITY.
5. REPEAT STEPS 1 THRU 4 USING A VALUE OF 6 VDC IN STEP 2.

6. I =	MIN	MAX
	−1.0mA	−3.3mA
	+0.5mA	+3.0mA

IRRADIATION CIRCUIT



BURN-IN CIRCUIT



V_{IN} = 50 KHz SQUARE WAVE 50% DUTY CYCLE −4.0V TO +4.0V

Radiation Screening Procedure

(1) Two (2) probed good samples per wafer will be selected from ≥ 20% of the wafers in a run. (All wafers in a "run" will have been processed together through all high temperature processing steps and through metallization.)

(2) The sample die shall be assembled and tested for functionality.

(3) The sample devices shall be subjected to a Total Dose Radiation level of 1 x 10^6 Rad (Si) ±10% from a gamma cell 220 cobalt 60 source or equivalent. The devices will be powered in the configuration illustrated with VSUPPLY = ±15V. The dose rate shall be between 50 rads/sec and 200 rads/sec.

(4) AVOL, VIO, and IBIAS, with VSUPPLY = ±15V, will be measured and recorded for each device within one hour after irradiation. The lot will be accepted only if the sample, exclusive of non-radiation failures, meets the limits of AVOL ≥ 80dB, VIO ≤ ±5.0mV and IBIAS ≤ ±400nA at room temperature.

Radiation Effects

(1) Total Dose

Little or no effect will be observed at 1 x 10^5 Rad (Si). IBIAS, IIO, and AVOL starts to degrade between 1 x 10^5 and 1 x 10^6 Rad (Si).

(2) Dose Rate

Devices are constructed in DI and consequently are latchup free.

(3) Neutron Fluence

Performance degradation is insignificant at 5 x 10^{12}n/cm^2.

Test Product Flow

HARRIS SEMICONDUCTOR PRODUCT FLOW
MIL-STD-883, METHOD 5004 CLASS B

100% SCREENING PROCEDURE

	SCREEN	MIL-STD-883 METHOD/COND.
1	Internal Visual	2010 Cond. B.
2	Stabilization Bake	1008 Cond. C (24 hrs. minimum)
3	Temperature Cycling	1010 Cond. C
4	Constant Acceleration	2001 Cond. E; Y1 plane
5	Seal: A Fine B Gross	1014 Cond. A or B 1014 Cond. C2
6	Initial Electrical	Harris Specifications
7	Burn-In Test	1015, 160 hrs. @ 125°C (or equivalent) (Burn-In circuits enclosed)
8	Final Electrical 100% go-no-go	Tested at Worst Case Operating Conditions
9	External Visual	2009 Sample Inspection

Note:

Traceability: All devices are assigned date code identification that provides traceability back to the inspection lot.

Branding: All devices are branded with the part number and EIA date code.

Aged Products: Product that has been held for more than 24 months will be reinspected prior to shipment to group A inspection requirements.

Additional Requirements: Sample Group A electrical tests are performed on a lot acceptance basis.

Sales Offices

EASTERN REGION

8300 Greensboro Drive
McLean, Virginia 22102
(703) 448-5400
TWX: 710-833-0340

Five Old Concord Road
Burlington, MA 01803
(617) 273-1020
TWX: 710-332-1074

106 Seventh Street
Garden City, NY 11530
(516) 747-6776
TWX: 510-220-1527

WESTERN REGION

1503 South Coast Drive
Suite 320
Costa Mesa, CA 92626
(714) 957-6557
TWX: 910-595-1533

EAST COAST

7040 Lake Ellenor Drive
Suite 113
Orlando, FL 32809
(305) 851-9450

MIDWEST REGION

2850 Metro Office Park
Bloomington, MN 55420
(612) 854-3224
TWX: 910-576-3418

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Melbourne, FL 32901
(305) 729-5585
TWX: 510-959-6259

EUROPEAN

Harris Systems Ltd.
Semiconductor Programs Division
P.O. Box 27
145 Farnham Road
Slough SL1 4XD
United Kingdom
Tel: 34666
TWX: 848174

CUSTOM INTEGRATED CIRCUITS DIVISION

HARRIS

HS-3530RH

Low Power-
Radiation Resistant
Programmable Operational Amplifier

APRIL 1982

Features

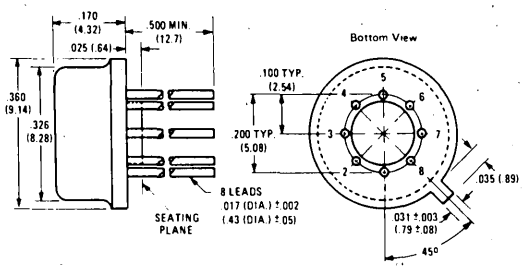
- WIDE RANGE AC PROGRAMMING
  - SLEW RATE 06 TO3V/μs
  - GAIN X BANDWIDTH . . . . . 100KHz TO 5.0MHz
- WIDE RANGE DC PROGRAMMING
  - POWER SUPPLY RANGE . . . . . $\pm$1.5V TO $\pm$18V
  - SUPPLY CURRENT . . . . . 10μA TO 1.2mA
- SHORT CIRCUIT PROTECTION
- RADIATION ENVIRONMENT
  - NEUTRON FLUENCE(ϕ) . 5×10^{12} n/cm^2 (E $\geq$ 10KeV)
  - GAMMA RATE($\dot{\gamma}$) . . . . . 1×10^9 RADS (Si)/s
  - GAMMA DOSE(γ) . . . . . 1×10^6 RADS (Si)

Description

The HS-3530 is a Low Power Operational Amplifier which is an internally compensated monolithic device offering a wide range of performance specifications. Parameters such as power dissipation, slew rate, bandwidth, noise and input DC parameters are programmed by selecting an external resistor or current source. Supply voltages as low as $\pm$3 volts may be used with little degradation of AC performance. The HS-3530 has been specifically designed to meet exposure to radiation environments. Operation from -55°C to $+125^{\circ}$C is guaranteed.

A major advantage of the HS-3530 is that operating characteristics remain virtually constant over a wide supply range (+3V to +15V), allowing the amplifier to offer maximum performance in almost any system, including battery operated equipment. A primary application for this device is in active filtering and conditioning for a wide variety of signals that differ in frequency and amplitude. Also, by modulating the set current, it can be used for designs such as current controlled oscillators/modulators, sample and hold circuits and variable active filters.

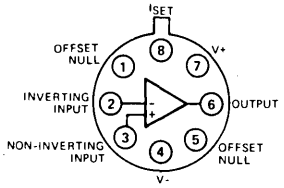
Package



1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions $^{+}$ .010 ($^{+}$0.25mm) unless otherwise shown.

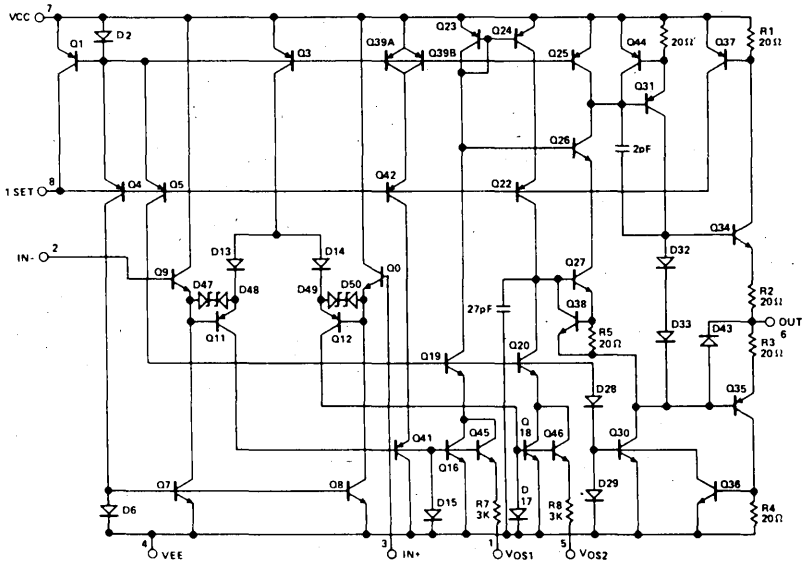
Pinout

TOP VIEW



NOTE: Case tied to V-

Schematic



ABSOLUTE MAXIMUM RATINGS

Voltage between V+ and V- terminals	40V
Differential Input Voltage	± 20V
Input Voltage (Note 1)	± 15V

I_{SET} (current at I_{SET})	500μA
V_{SET} (voltage to ground at I_{SET})	(V+ -2.0V)<V_{SET}<V+
Output Short Circuit Duration	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C

NOTE:
① For supply voltage less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

PRE-RADIATION ELECTRICAL CHARACTERISTICS

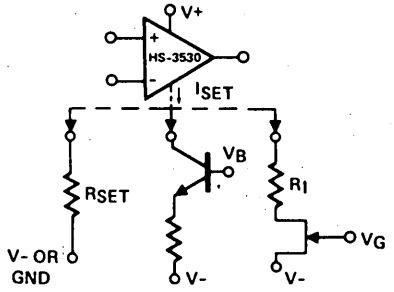
V_{SUPPLY} = ±15V		I_{SET} = 1.5μA (R_L = 75KΩ)			I_{SET} = 15μA (R_L = 5KΩ)			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
Offset Voltage	25°C Full		1	3 5		1	3 5	mV mV
Input Bias Current	25°C Full		1.2 2.5			10 22	20 40	nA nA
Input Offset Current	25°C Full		0.3			2	5 10	nA nA
Input Resistance	25°C		>100		50	>100		MΩ
Large Signal Voltage Gain[1]	25°C Full	65K 25K	115K 60K		80K 50K	130K 70K		V/V V/V
Common Mode Rejection Ratio[2]	25°C Full	80	115		80 80	115 110		dB dB
Supply Current	25°C Full		13 14	15 15		125 130	150 160	μA μA
Power Supply Rejection Ratio[3]	25°C Full	80	130		80 80	130 120		dB dB
Output Voltage Swing[2]	25°C Full	±12.5 ±10.5	±14.2 ±14.0		±12.5 ±10.5	±14.2 ±14.0		V V
Output Current	25°C Full		±.5 ±.4			±5 ±4		mA mA
Output Short-Circuit Current	25°C		2			14		mA
Gain-Bandwidth Product	25°C Full		85 65			850 640		kHz kHz
Slew Rate[5]	25°C		.05			.55		V/μS
Rise Time[4]	25°C		7.5			.7		μS
Overshoot[4]	25°C		5			10		%
Overdrive Recovery Time	25°C					2		μS

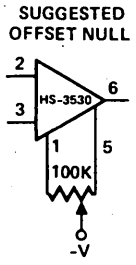
V_{SUPPLY} = ±3V		I_{SET} = 1.5μA (R_L = 75KΩ)			I_{SET} = 15μA (R_L = 5KΩ)			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
Large Signal Voltage Gain[1]	25°C Full	25K 15K	60K 40K		25K 25K	75K 50K		V/V V/V
Common Mode Rejection Ratio[2]	25°C Full	80 80	100 90		80	95		dB dB
Supply Current	25°C Full		12	15 15		115	150 160	μA μA
Power Supply Rejection Ratio[3]	25°C Full	80 80	105 100		80	105		dB dB
Output Voltage Swing[1]	25°C Full	±2.0 ±2.0			±2.0 ±2.0			V V
Gain-Bandwidth Product	25°C Full		72 60			730 600		kHz kHz
Slew Rate[5]	25°C		04			.4		V/μS
Offset Voltage	25°C Full		1	3 5		1	3 5	mV

NOTES:

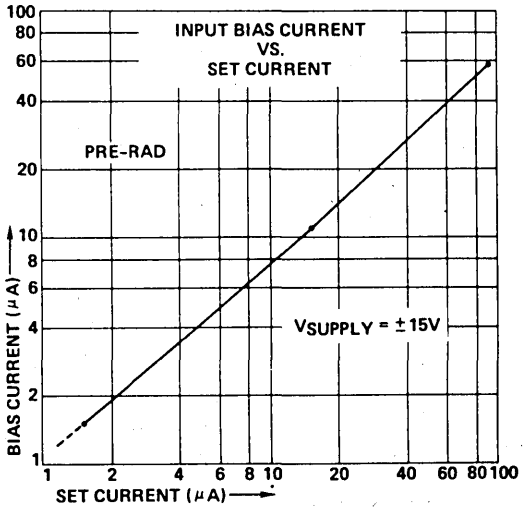
	$V_{SUPPLY} = \pm 3.0V$	$V_{SUPPLY} = \pm 15.0V$	$I_{SET} = 1.5\mu A$	$I_{SET} = 15\mu A$
1.	$V_O = \pm 1.0V$	$V_O = \pm 10.0V$	$R_L = 75K$	$R_L = 5K$ +25°C +125°C $R_L = 75K$ -55°C
2.	$V_{CM} = \pm 1.5V$	$V_{CM} = \pm 5.0V$		
3.	$V = \pm 1.5V$	$\Delta V = \pm 5.0V$		
4.	← $A_V = +1$, $V_{IN} = 400mV$, $R_L = 5K$, $C_L = 100pF$ →			
5.	$V_O = \pm 2.0V$	$V_O = \pm 10.0V$	$R_L = 20K$	$R_L = 5K$ +25°C +125°C $R_L = 75K$ -55°C

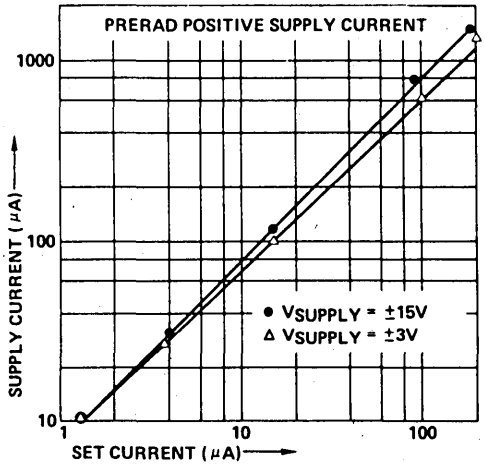
Typical Biasing Circuits

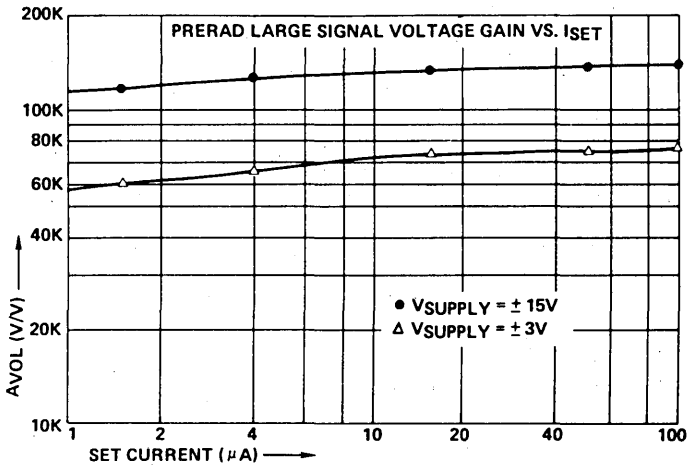




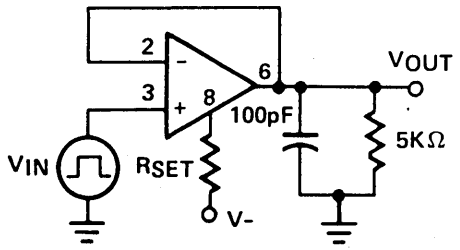
Typical Performance Curves



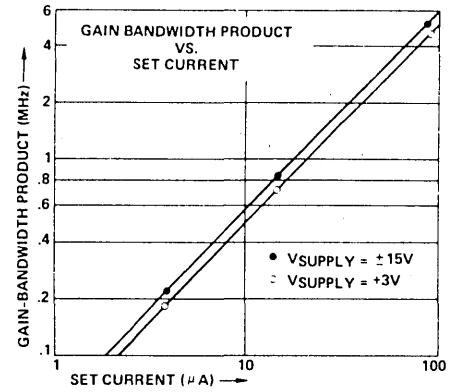


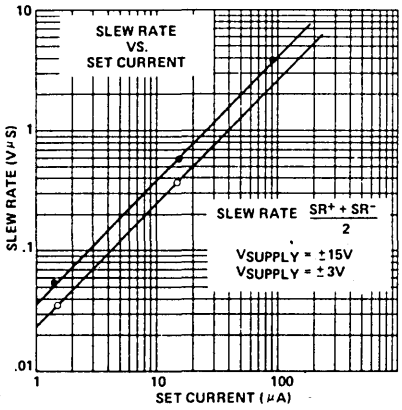


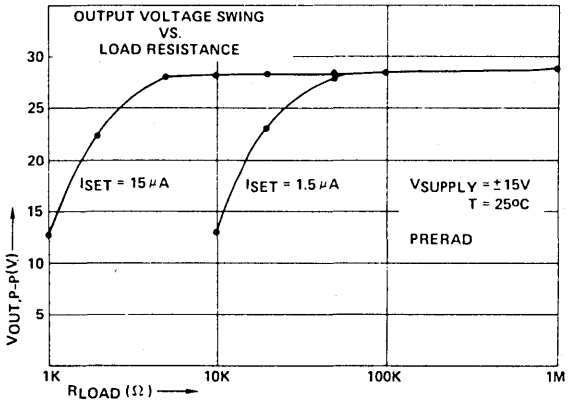
Transient Response/Slew Rate Circuit

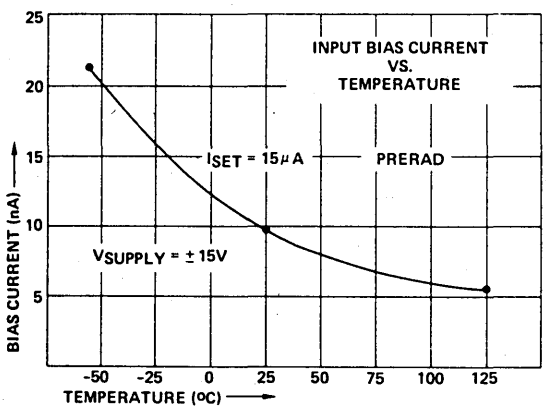


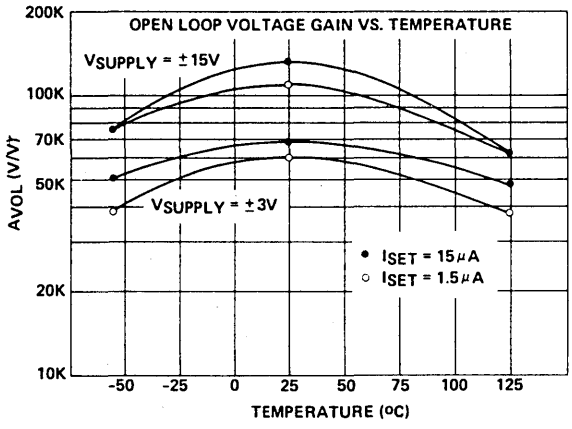
Typical Performance Curves











Radiation Screening Procedure

(1) Two (2) probed good samples per wafer will be selected from ≥20% of the wafers in a run. (All wafers in a "run" will have been processed together through all high temperature processing steps and through metallization.)

(2) The sample die shall be assembled and tested for functionality.

(3) The sample devices shall be subjected to a Total Dose Radiation level of 1×10^6 Rad (Si) ±10% from a Gamma Cell 220 Cobalt 60 source or equivalent. The devices will be powered in a voltage follower configuration, with I_{SET} = 15 μA and V_{SUPPLY} = ±15V. The dose rate shall be between 50 rads/sec and 200 rads/sec.

(4) A_{VOL} and V_{IO}, with I_{SET}= 15 μA, V_{SUPPLY} = +15V and R_L = 25K, will be measured and recorded for each device within one hour after irradiation. The lot will be accepted only if the sample, exclusive on non-radiation failures, meets the limits of $A_{VOL} \geq$ 20K V/V and $V_{IO} \leq$ 3.5 mV at room temperature.

Radiation Effects

(1) Total Dose:
Very little degradation of any of the parameters will be seen up to $\gamma = 10^4$ Rad (Si). Moderate degradation of open loop gain, bias current, and offset current begins at greater than 10^5 and less than 10^6 Rad (Si).

(2) Dose Rate:
During transient ionizing radiation at a level of 1×10^9 rad (Si)/s, the peak level of supply current will be about 150 to 200 mA. After about 0.1 to 0.5 μS this current drops about 10%. Maximum recovery time will be about 6 to 8 μS.

(3) Neutron Fluence:
Large signal voltage gain degrades rapidly for low supply voltages and low set currents. For V_{SUPPLY} = +15V and $I_{SET} > 10\mu A$, large signal voltage gain degrades by only about 50%. Input bias current doubles for $\phi = 5 \times 10^{12} n/cm^2$.

Test Product Flow

HARRIS SEMICONDUCTOR PRODUCT FLOW
MIL - STD - 883, METHOD 5004 CLASS B
100% SCREENING PROCEDURE

	SCREEN	MIL-STD-883 METHOD/COND.
1	Internal Visual	2010 Cond. B.
2	Stabilization Bake	1008 Cond. C (24 hrs. minimum)
3	Temperature Cycling	1010 Cond. C
4	Constant Acceleration	2001 Cond. E; Y1 plane
5	Seal: A Fine B Gross	1014 Cond. A or B 1014 Cond. C2
6	Initial Electrical	Harris Specifications
7	Burn-In Test	1015, 160 hrs. 125°C (or equivalent)
8	Final Electrical 100% go-no-go	Tested at Worst Case Operation Conditions
9	External Visual	2009 Sample Inspection

Note:

Traceability:	All devices are assigned date code identification that provides traceability back to the inspection lot.
Branding:	All devices are branded with the part number and E1A date code.
Aged Products:	Product that has been held for more than 24 months will be reinspected prior to shipment to group A inspection requirements.
Additional Requirements:	Sample Group A electrical tests are performed on a lot acceptance basis.

HARRIS

Preliminary

October 1982

HS-3546RH

Radiation Resistant High Performance Operational Amplifier

Features

- LOW OFFSET VOLTAGE — 0.3mV
- HIGH SLEW RATE — ±4V/μs
- WIDE BANDWIDTH — 8MHz
- LOW DRIFT — 2μV/°C
- FAST SETTLING (0.01%, 10V STEP) — 4.2μs
- LOW POWER CONSUMPTION — 35mW
- SUPPLY RANGE — ±5V TO ±20V
- RADIATION ENVIRONMENT
  - NEUTRON FLUENCE (ϕ) . 5×10^{12} n/cm^2 (E $\geq$ 10KeV)
  - GAMMA RATE ($\dot{\gamma}$) . . . . . 1×10^9 RADS (Si)/s
  - GAMMA DOSE (γ) . . . . . 1×10^6 RADS (Si)

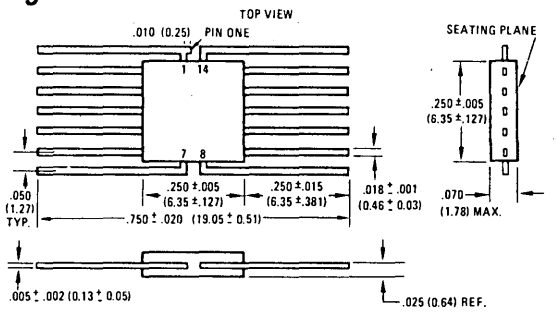
Description

The HS-3546RH is a radiation resistant, high performance dielectrically isolated monolithic operational amplifier with superior specifications. This amplifier offers excellent dynamic performance coupled with low values for offset voltage and drift, input noise voltage and power consumption.

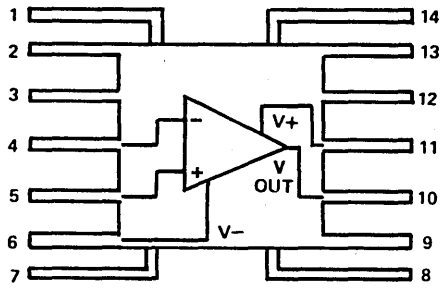
A wide range of applications can be achieved by using the features made available by the HS-3546RH. With wide bandwidth (8MHz), low power (35mW) and internal compensation, these devices are ideally suited for precision active filter designs. For audio applications these amplifiers offer low noise (8nV/$\sqrt{Hz}$) and excellent full power bandwidth (60 KHz). The HS-3546RH is particularly useful in designs requiring low offset voltage (0.3mV) and drift (2μV/°C), such as instrumentation and signal conditioning circuits. The high slew rate (4V/μs) and fast settling time (4.2 μs to 0.01%, 10V step) makes this amplifier a useful component in fast, accurate data acquisition systems.

The HS-3546RH has been specifically designed to meet exposure to radiation environments. It is available in a 14 Pin Ceramic Flatpack package and is guaranteed operational from -55°C to +125°C.

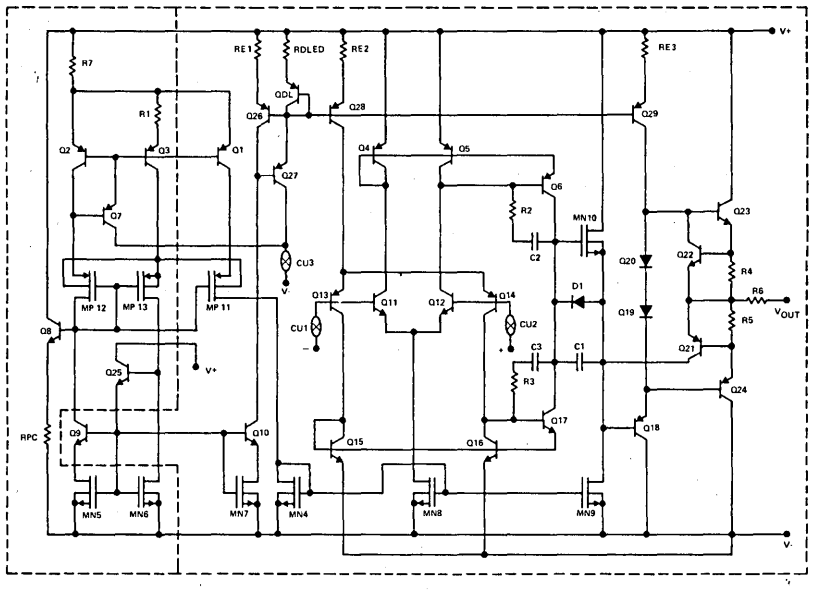
Package



Pinout



Schematic



ABSOLUTE MAXIMUM RATINGS (Note 1)

T_A = +25°C Unless Otherwise Stated

Voltage Between V+ and V- Terminals	40.0V	Power Dissipation (Note 4)	880mW
Differential Input Voltage	±7V	Operating Temperature Range	$-55^oC \leq T_A \leq +125^oC$
Input Voltage (Note 2)	±15.0V	Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$
Output Short Circuit Duration (Note 3)	Indefinite		

CAUTION: To prevent permanent damage to this device, care should be exercised to insure that the absolute maximum ratings for supply voltages, temperature and voltage or current at any pin is not exceeded during both static and dymanic operation.

ELECTRICAL CHARACTERISTICS V+ = 15V, V− = −15V T_A = −55°C to +125°C

PARAMETER	TEMP	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
* Offset Voltage	+25°C		0.3	2.5	mV
	Full			3.0	mV
Av. Offset Voltage Drift	Full		2		µV/°C
* Bias Current	+25°C		130	200	nA
	Full			325	nA
* Offset Current	+25°C		30	75	nA
	Full			125	nA
Common Mode Range	Full	±12			V
Input Noise Voltage (f = 1kHz)	+25°C		8		$nV/\sqrt{Hz}$
Input Resistance			500		kΩ
TRANSFER CHARACTERISTICS					
* Large Signal Voltage Gain (Note 5)	Full	100K	250K		V/V
* Common Mode Rejection Ratio (Note 8)	Full	86			dB
Small Signal Bandwidth	+25°C		8		MHz
OUTPUT CHARACTERISTICS					
* Output Voltage Swing (R_L = 10K)	Full	±12	±13		V
(R_L = 2K)	Full	±10	±12		V
Full Power Bandwidth (Note 5)	+25°C		60		kHz
Output Current (Note 6)	Full	±18	±25		mA
Output Resistance	+25°C		200		Ω
TRANSIENT RESPONSE (Note 7)					
Rise Time	+25°C		50	150	ns
Overshoot	+25°C		30	45	%
Slew Rate	+25°C	±1	±4		V/µs
Settling Time (Note 9)			4.2		µs
POWER SUPPLY CHARACTERISTICS					
* Supply Current	+25°C		4.6	5.5	mA
* Power Supply Rejection Ratio (Note 8)	Full	86			dB

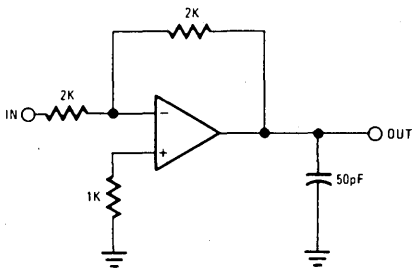
*100% tested

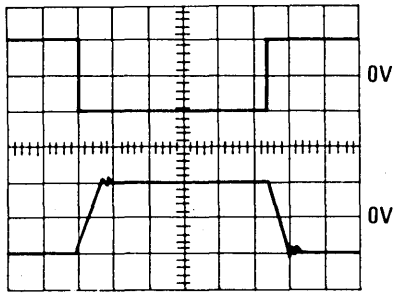
NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Any one amplifier may be shorted to ground indefinitely.
4. Derate 5.8mW/°C above T_A = +25°C.
5. V_{OUT} = ±10V; R_L = 2K ohms.
6. Output current is measured with V_{OUT} = ±5 volts.
7. For transient response test circuits and measurement conditions refer to Test Circuits section of the data sheet.
8. ΔV = ±5.0 volts.
9. Settling time is measured to 0.1% of final value for a 10 volt input step, A_V = -1.

Test Circuits

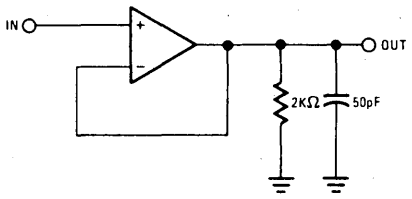
LARGE SIGNAL RESPONSE CIRCUIT (Volts: 5V/Div., Time: 5μs/Div.)

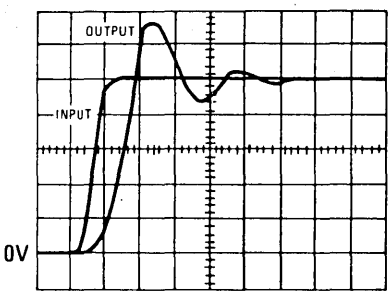




VERT. 5V/DIV.
HORZ. 5 μs/DIV.

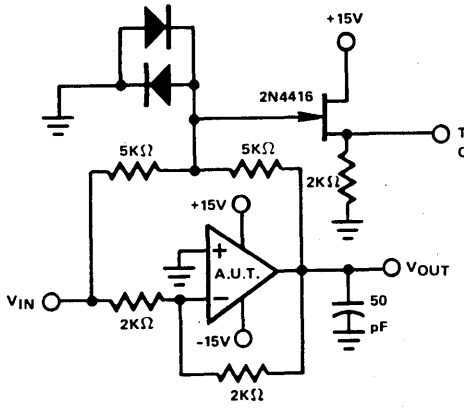
SMALL SIGNAL RESPONSE CIRCUIT (Volts: 10mV/Div., Time: 50ns/Div.)





HORIZONTAL: 50 NSEC/DIV.
VERTICAL: 10mV/DIV

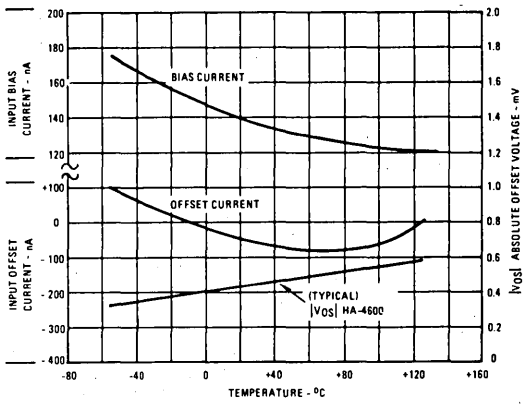
SETTLING TIME CIRCUIT



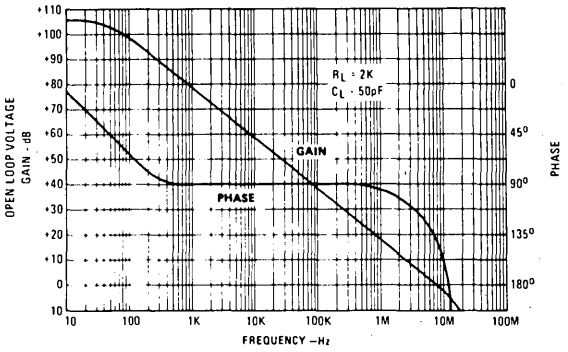
- A_V = -1.
- Feedback and summing resistors should be 0.1%.
- Clipping diodes are optional. HP5082-2810 recommended.

V+ = +15V, V- = -15V, T_A = +25°C Unless Otherwise Stated.

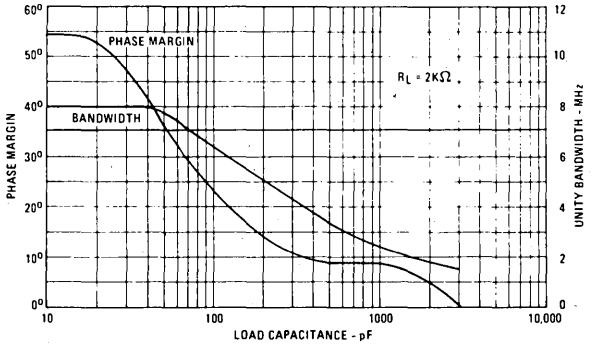
OFFSET VOLTAGE INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE



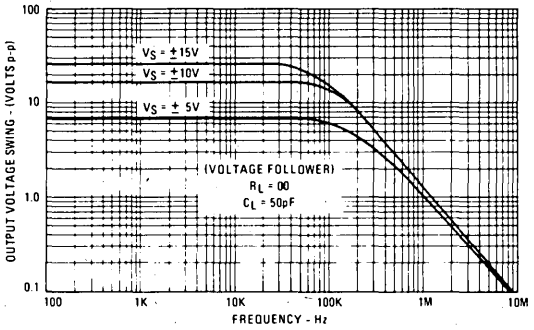
OPEN LOOP FREQUENCY RESPONSE



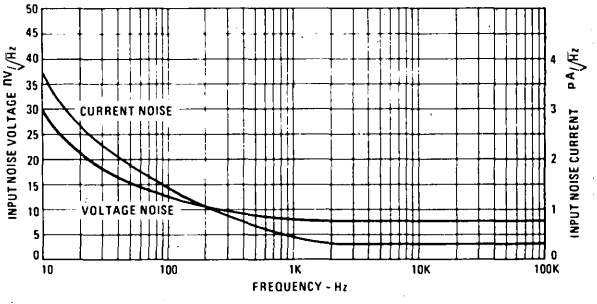
SMALL SIGNAL BANDWIDTH AND PHASE MARGIN VS. LOAD CAPACITANCE



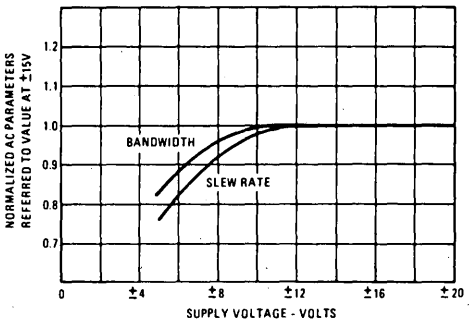
OUTPUT VOLTAGE SWING VS. FREQUENCY AND SUPPLY VOLTAGE



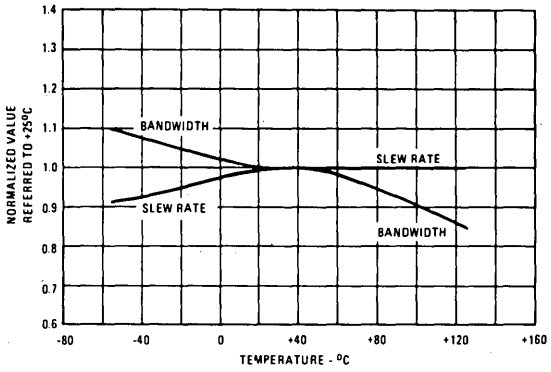
INPUT NOISE VS. FREQUENCY



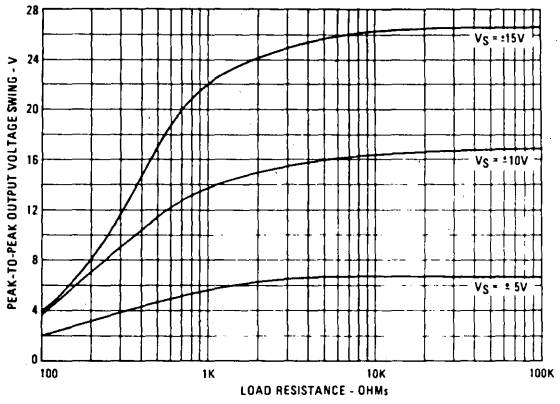
NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE



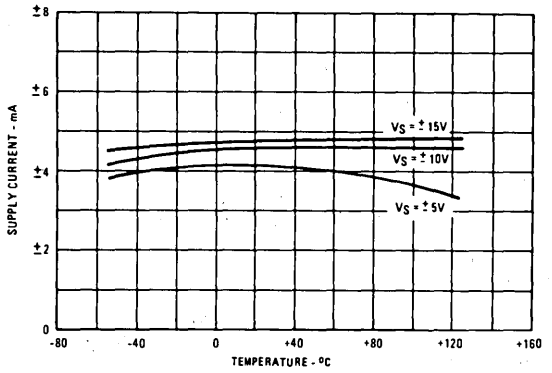
NORMALIZED AC PARAMETERS VS. TEMPERATURE



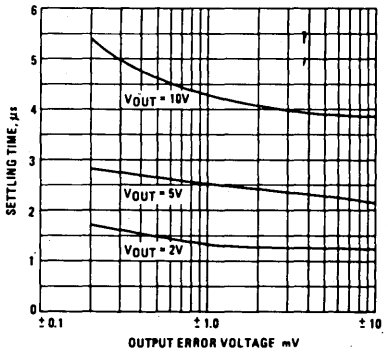
MAXIMUM OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE AND SUPPLY VOLTAGE



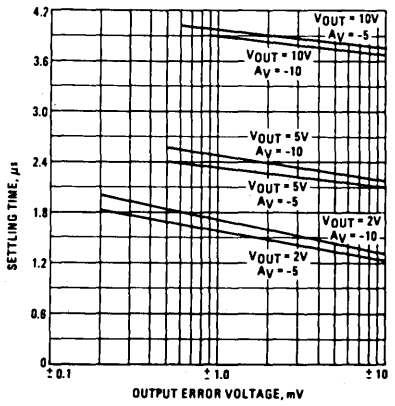
POWER SUPPLY CURRENT VS. TEMPERATURE AND SUPPLY VOLTAGE



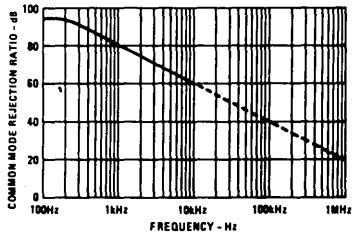
SETTLING TIME VS. OUTPUT AMPLITUDE (AV = -1)



SETTLING TIME VS. OUTPUT AMPLITUDE AND SIGNAL GAIN (AV = -5 AND AV = -10)



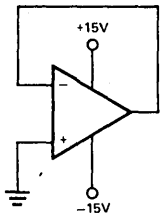
COMMON MODE REJECTION RATIO VS. FREQUENCY



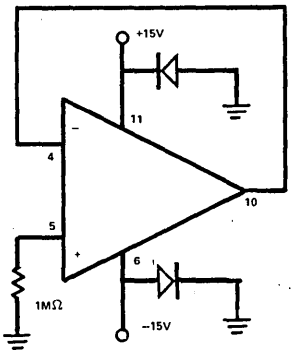
1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with .01 μ F ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.

2. In high frequency applications where large value feedback resistors are used, a small capacitor (3pF) may be needed in parallel with the feedback resistor to neutralize the pole introduced by input capacitance.

Irradiation Circuit



Burn-in Circuit



NOTES:
T_A = +125°C
D = IN4002 OR EQUIVALENT

Radiation Screening Procedure

(1) Two (2) probed good samples per wafer will be selected from $\geq$20% of the wafers in a run (All wafers in a "run" will have been processed together through all high temperature processing steps and through metallization.)

(2) The sample die shall be assembled and tested for functionality.

(3) The sample devices shall be subjected to a Total Dose Radiation level of 1 x 10^5 Rad (Si) ±10% from a gamma cell 220 cobalt 60 source or equivalent. The devices will be powered in the configuration illustrated with VSUPPLY = ±15V. The dose rate shall be between 50 rads/sec and 200 rads/sec.

(4) A_{VOL}, V_{IO}, AND I_{BIAS}, with VSUPPLY = ±15V, will be measured and recorded for each device within one hour after irradiation. The lot will be accepted only if the sample, exclusive of non-radiation failures, meets the limits of $A_{VOL} \geq$ 100K, $V_{IO} \leq$ ±2.5mV and $I_{BIAS} \leq$ 1.0 μA at room temperature.

Radiation Effects

(1) Total Dose
Little or no effect will be observed at 1 x 10^4 Rad (Si). I_{BIAS}, I_{IO} and A_{VOL} starts to degrade between 1 x 10^4 and 1 x 10^5 Rad (Si).

(2) Dose Rate
Devices are constructed in DI and consequently are latchup free.

Test Product Flow

HARRIS SEMICONDUCTOR PRODUCT FLOW
MIL-STD-883, METHOD 5004 CLASS B

100% SCREENING PROCEDURE

	SCREEN	MIL-STD-883 METHOD/COND.
1	Internal Visual	2010 Cond. B.
2	Stabilization Bake	1008 Cond. C (24 hrs. minimum)
3	Temperature Cycling	1010 Cond. C
4	Constant Acceleration	2001 Cond. E; Y1 plane
5	Seal: A Fine B Gross	1014 Cond. A or B 1014 Cond. C2
6	Initial Electrical	Harris Specifications
7	Burn-In Test	1015, 160 hrs. @ 125°C (or equivalent) (Burn-In circuits enclosed)
8	Final Electrical 100% go-no-go	Tested at Worst Case Operating Conditions
9	External Visual	2009 Sample Inspection

Notes:
- Traceability: All devices are assigned date code identification that provides traceability back to the inspection lot.
- Branding: All devices are branded with the part number and EIA date code.
- Aged Products: Product that has been held for more than 24 months will be reinspected prior to shipment to group A inspection requirements.
- Additional Requirements: Sample Group A electrical tests are performed on a lot acceptance basis.

Ordering Information

HS 9 3546RH - 2

- HS — HARRIS
- 9 — PACKAGE: 9 — Cerpack
- 3546RH — DEVICE NUMBER
- 2 — TEMPERATURE: 2 — -55°C to +125°C; 8 — MIL-STD-883B

Sales Offices

EASTERN REGION

8300 Greensboro Drive
McLean, Virginia 22102
(703) 448-5400
TWX: 710-833-0340

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Burlington, MA 01803
(617) 273-1020
TWX: 710-332-1074

106 Seventh Street
Garden City, NY 11530
(516) 747-6776
TWX: 510-220-1527

WESTERN REGION

1503 South Coast Drive
Suite 320
Costa Mesa, CA 92626
(714) 957-6557
TWX: 910-595-1533

EAST COAST

7040 Lake Ellenor Drive
Suite 113
Orlando, FL 32809
(305) 851-9450

MIDWEST REGION

2850 Metro Office Park
Bloomington, MN 55420
(612) 854-3224
TWX: 910-576-3418

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P.O. Box 883
Melbourne, FL 32901
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TWX: 510-959-6259

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Semiconductor Programs Division
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Slough SL1 4XD
United Kingdom
Tel: 34666
TWX: 848174

HARRIS

CUSTOM INTEGRATED CIRCUITS DIVISION

HARRIS

Preliminary

SEPTEMBER 1982

HS-4602RH

Radiation Resistant High Performance Quad Operational Amplifier

Features

- LOW OFFSET VOLTAGE — 0.3mV
- HIGH SLEW RATE — ±4V/μs
- WIDE BANDWIDTH — 8MHz
- LOW DRIFT — 2μV/°C
- FAST SETTLING (0.01%, 10V STEP) — 4.2μs
- LOW POWER CONSUMPTION — 35mW/AMP
- SUPPLY RANGE — ±5V TO ±20V
- RADIATION ENVIRONMENT
  - NEUTRON FLUENCE (ϕ) . 5×10^{12} n/cm^2 (E $\geq$ 10KeV)
  - GAMMA RATE ($\dot{\gamma}$) . . . . . 1×10^9 RADS (Si)/s
  - GAMMA DOSE (γ) . . . . . 1×10^6 RADS (Si)

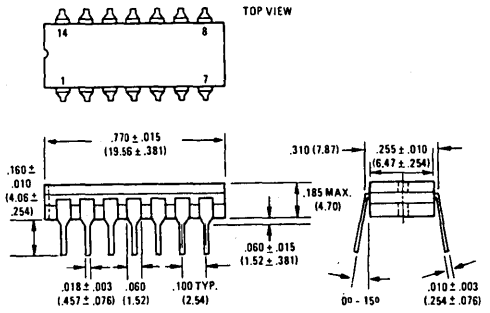
Description

The HS-4602RH is a radiation resistant, high performance dielectrically isolated monolithic quad operational amplifier with superior specifications not previously available in a quad amplifier. This amplifier offers excellent dynamic performance coupled with low values for offset voltage and drift, input noise voltage and power consumption.

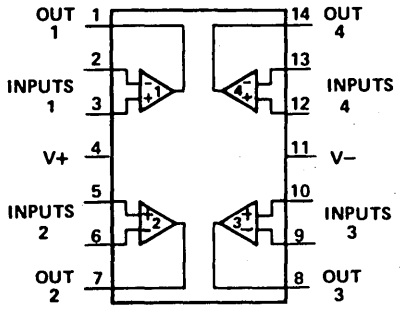
A wide range of applications can be achieved by using the features made available by the HS-4602RH. With wide bandwidth (8MHz), low power (35mW/amp), and internal compensation, these devices are ideally suited for precision active filter designs. For audio applications these amplifiers offer low noise ($8nV/\sqrt{Hz}$) and excellent full power band-width (60KHz). The HS-4602RH is particularly useful in designs requiring low offset voltage (0.3mV) and drift ($2\mu V/^oC$), such as instrumentation and signal conditioning circuits. The high slew rate ($4V/\mu s$) and fast settling time (4.2μs to 0.01%, 10V step) makes this amplifier a useful component in fast, accurate data acquisition systems.

The HS-4602RH has been specifically designed to meet exposure to radiation environments. It is available in a 14 pin dual-in-line package and is guaranteed operational from −55°C to +125°C.

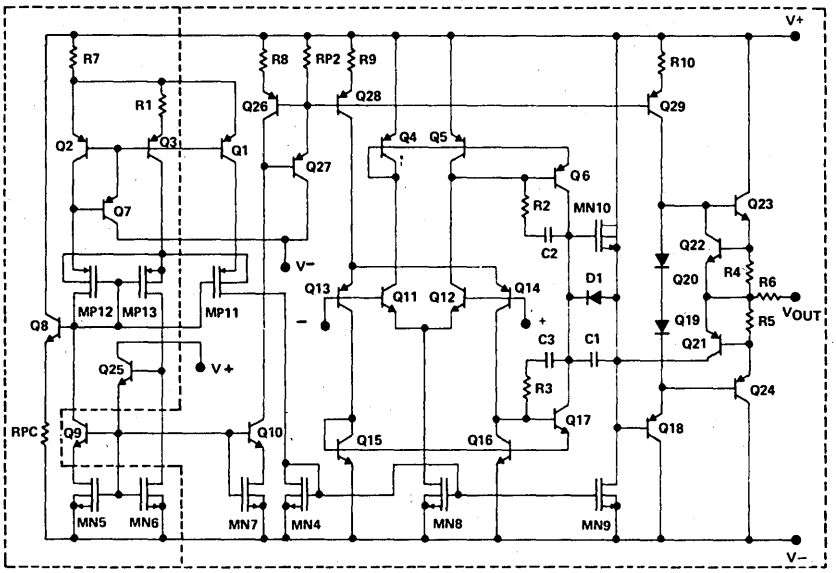
Package



Pinout



Schematic



(ONE FOURTH ONLY HS-4602-RH)

ABSOLUTE MAXIMUM RATINGS (Note 1)

T_A = +25°C Unless Otherwise Stated

Voltage Between V+ and V- Terminals	40.0V	Power Dissipation (Note 4)	880mW
Differential Input Voltage	±7V	Operating Temperature Range	$-55^oC \leq T_A \leq +125^oC$
Input Voltage (Note 2)	±15.0V	Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$
Output Short Circuit Duration (Note 3)	Indefinite		

CAUTION: To prevent permanent damage to this device, care should be exercised to insure that the absolute maximum ratings for supply voltages, temperature and voltage or current at any pin is not exceeded during both static and dymanic operation.

ELECTRICAL CHARACTERISTICS V+ = 15V, V− = −15V T_A = −55°C to +125°C

PARAMETER	TEMP	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
* Offset Voltage	+25°C		0.3	2.5	mV
	Full			3.0	mV
Av. Offset Voltage Drift	Full		2		µV/°C
* Bias Current	+25°C		130	200	nA
	Full			325	nA
* Offset Current	+25°C		30	75	nA
	Full			125	nA
Common Mode Range	Full	±12			V
Input Noise Voltage (f = 1kHz)	+25°C		8		$nV/\sqrt{Hz}$
Input Resistance			500		kΩ
TRANSFER CHARACTERISTICS					
* Large Signal Voltage Gain (Note 5)	Full	100K	250K		V/V
* Common Mode Rejection Ratio (Note 9)	Full	86			dB
Channel Separation (Note 6)	+25°C		-108		dB
Small Signal Bandwidth	+25°C		8		MHz
OUTPUT CHARACTERISTICS					
* Output Voltage Swing (R_L = 10K)	Full	±12	±13		V
(R_L = 2K)	Full	±10	±12		V
Full Power Bandwidth (Note 5)	+25°C		60		kHz
Output Current (Note 7)	Full	±10	±15		mA
Output Resistance	+25°C		200		Ω
TRANSIENT RESPONSE (Note 8)					
Rise Time	+25°C		50	150	ns
Overshoot	+25°C		30	45	%
Slew Rate	+25°C	±1	±4		V/µs
Settling Time (Note 10)			4.2		µs
POWER SUPPLY CHARACTERISTICS					
* Supply Current	+25°C		4.6	5.5	mA
* Power Supply Rejection Ratio (Note 9)	Full	86			dB

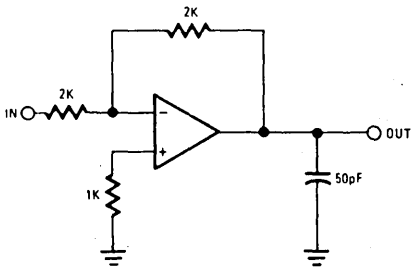
*100% tested

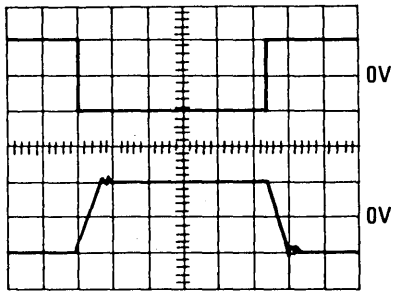
NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Any one amplifier may be shorted to ground indefinitely.
4. Derate 5.8mW/°C above T_A = +25°C.
5. V_{OUT} = ±10V; R_L = 2K ohms.
6. Channel separation value is referred to the input of the amplifier. Input test conditions are: f = 10kHz; V_{IN} = 200mV peak-to-peak; R_S = 1K ohms. (Refer to Channel Separation vs. Frequency Curve for test circuits.)
7. Output current is measured with V_{OUT} = ±5 volts.
8. For transient response test circuits and measurement conditions refer to Test Circuits section of the data sheet.
9. ΔV = ±5.0 volts.
10. Settling time is measured to 0.1% of final value for a 10 volt input step, A_V = -1.

Test Circuits

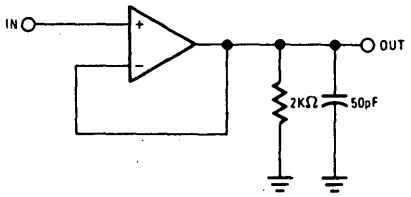
LARGE SIGNAL RESPONSE CIRCUIT (Volts: 5V/Div., Time: 5μs/Div.)

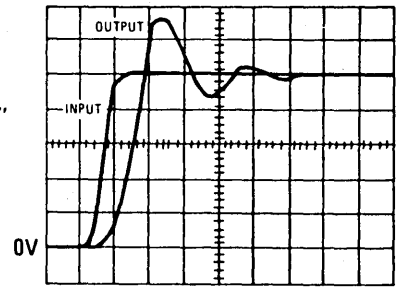




VERT. 5V/DIV.
HORZ. 5μs/DIV.

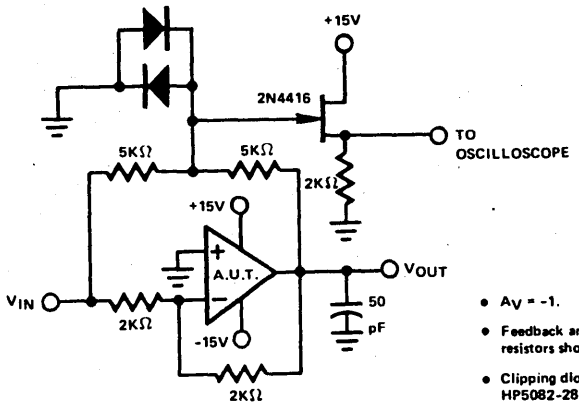
SMALL SIGNAL RESPONSE CIRCUIT (Volts: 10mV/Div., Time: 50ns/Div.)





HORIZONTAL: 50 NSEC/DIV.
VERTICAL: 10mV/DIV

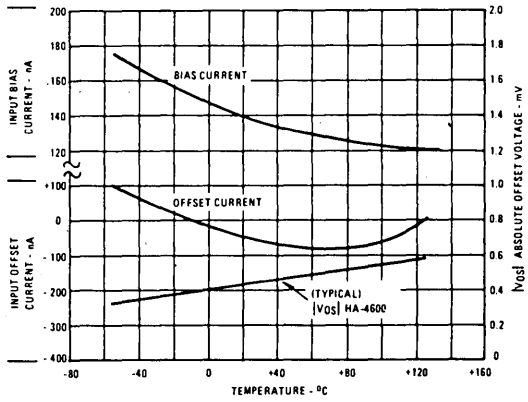
SETTLING TIME CIRCUIT



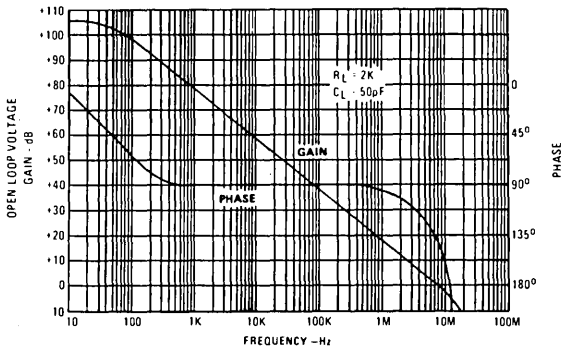
- A_V = -1.
- Feedback and summing resistors should be 0.1%.
- Clipping diodes are optional. HP5082-2810 recommended.

V+ = +15V, V- = -15V, T_A = +25°C Unless Otherwise Stated.

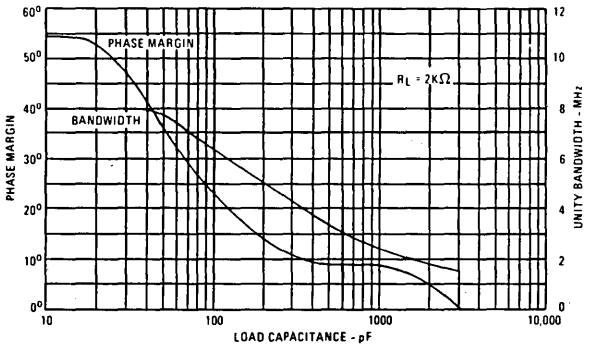
OFFSET VOLTAGE INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE



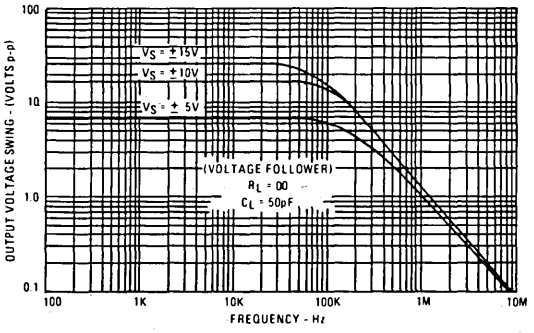
OPEN LOOP FREQUENCY RESPONSE



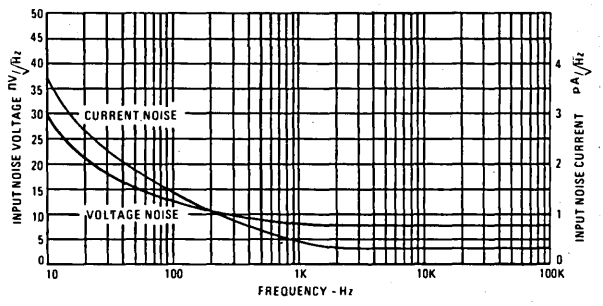
SMALL SIGNAL BANDWIDTH AND PHASE MARGIN VS. LOAD CAPACITANCE



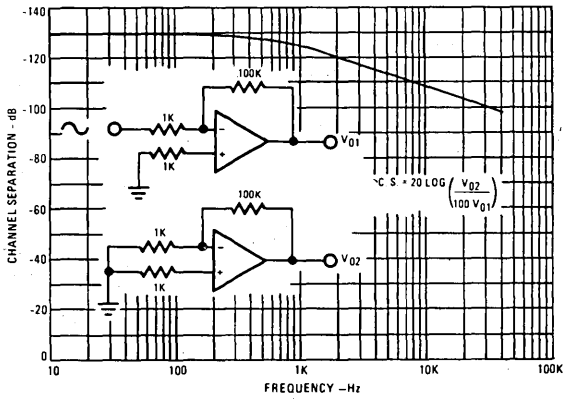
OUTPUT VOLTAGE SWING VS. FREQUENCY AND SUPPLY VOLTAGE



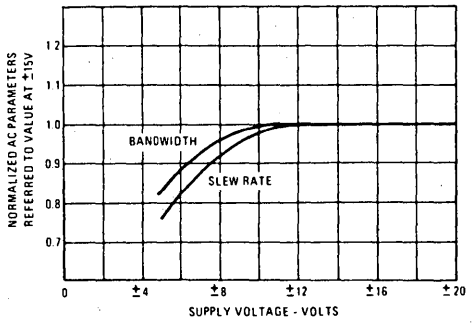
INPUT NOISE VS. FREQUENCY



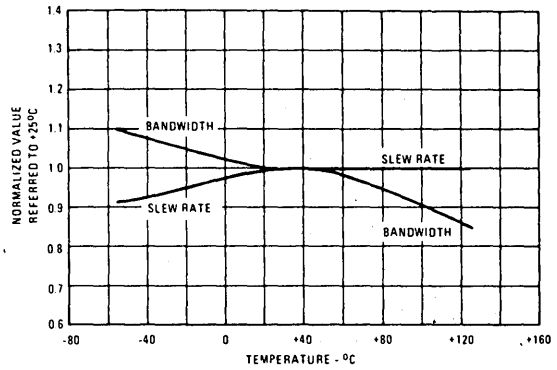
CHANNEL SEPARATION VS. FREQUENCY



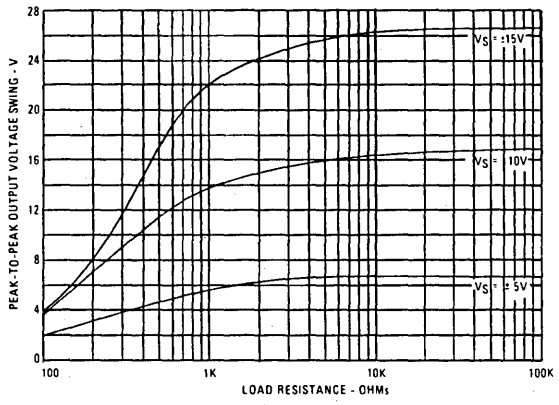
NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE



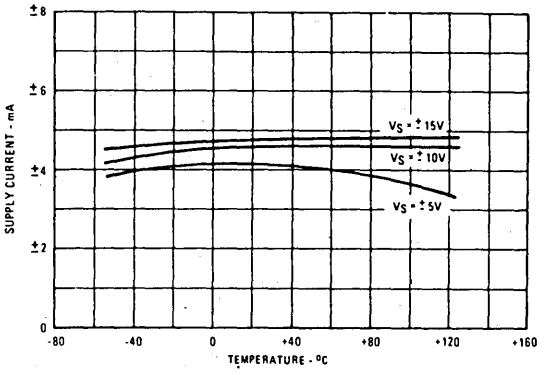
NORMALIZED AC PARAMETERS VS. TEMPERATURE



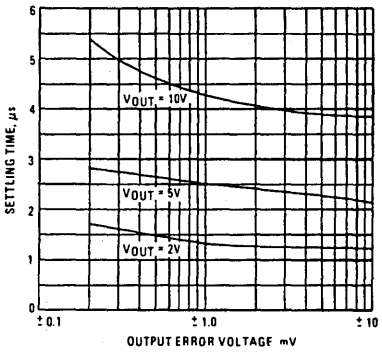
MAXIMUM OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE AND SUPPLY VOLTAGE



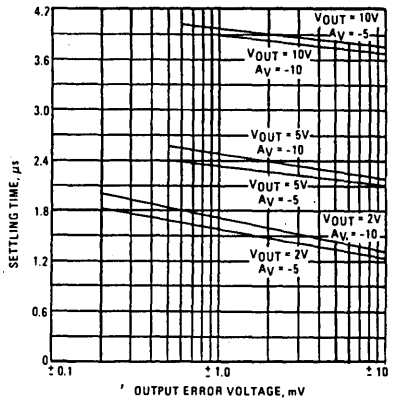
POWER SUPPLY CURRENT VS. TEMPERATURE AND SUPPLY VOLTAGE



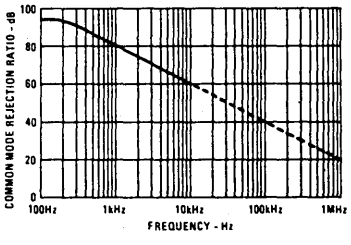
SETTLING TIME VS. OUTPUT AMPLITUDE (A_V = -1)



SETTLING TIME VS. OUTPUT AMPLITUDE AND SIGNAL GAIN (A_V = -5 AND A_V = -10)



COMMON MODE REJECTION RATIO VS. FREQUENCY



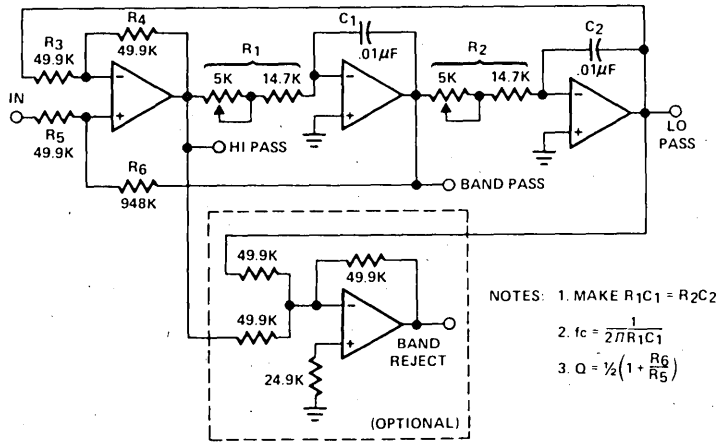
1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with .01 μF ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.

2. UNUSED OP AMPS: Unused op amp sections should be connected in a non-inverting follower configuration with the (+) input tied to ground in order to insure optimum performance of devices being used.

3. In high frequency applications where large value feedback resistors are used, a small capacitor (3pF) may be needed in parallel with the feedback resistor to neutralize the pole introduced by input capacitance.

Applications

2ND ORDER STATE VARIABLE FILTER (1kHz, Q = 10)



NOTES: 1. MAKE $R_1C_1 = R_2C_2$

2. $fc = \frac{1}{2\pi R_1 C_1}$

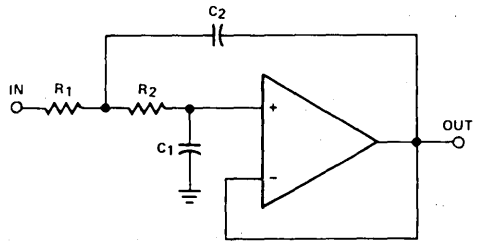
3. $Q = \frac{1}{2}\left(1 + \frac{R_6}{R_5}\right)$

The state variable filter is relatively insensitive to component changes (changes can be adjusted out with potentiometers) and also has low sensitivity to amplifier bandwidths. (Amplifier gain bandwidth product should be $\gg Q \times f_C$).

This filter finds wide application because multiple filtering functions are available simultaneously (High pass, Lo pass, Band pass, Band reject). In this circuit the various RC products are matched with pot adjustments allowing for non-interactive adjustment of Q and f_C. This allows capacitors (C_1, C_2) with loose tolerances to be used. To tune for f_C, apply a sine wave at f_C to the input, adjust R_1 for equal amplitudes at the Hi pass and Band pass terminals (they will be phased 90° apart) then adjust R_2 for equal amplitudes at the Band pass and Lo pass terminals.

The state variable filter is often used as building blocks in multiple pole Butterworth of Chebyshev filters. Many references contain normalized tables indicating settings for Q and f_C of each pole-pair section.

SALLEN AND KEY 2ND ORDER LO PASS FILTER



NOTES:

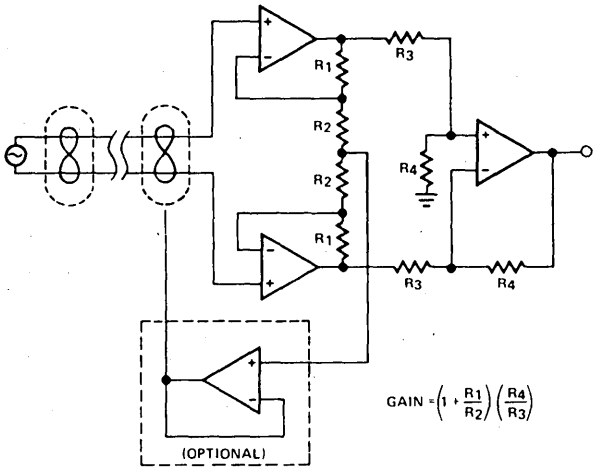
1. Make $R_1 = R_2$
2. $fc = \frac{1}{2\pi R_1 \sqrt{C_1 C_2}}$
3. $Q = \frac{1}{2}\sqrt{\frac{C_2}{C_1}}$

The advantage of using the Sallen and Key filter is simplicity, but in any application this must be weighed against the state-variable type filter for accuracy, practicality, and cost. Amplifier bandwidth limitations are much more apparent at moderate frequencies and Q values with this filter design. (For accuracy, amplifier gain-bandwidth product should be $\gg f_C \times Q^2$). The wide bandwidth of the HS-4602RH is particularly advantageous in this design even at audio frequencies.

In this filter all component values affect both Q and f_C. Precision, temperature stable resistors and capacitors must be used.

For economy, this filter could be used in the low Q stages of multiple-pole filter design, while the state variable type is used in the more critical stages.

INSTRUMENTATION AMPLIFIER

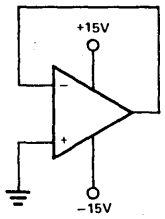


Instrumentation amplifiers (differential amplifiers) are specifically designed to extract and amplify small differential signals from much larger common mode voltages.

To serve as building blocks in instrumentation amplifiers, op amps must have very low offset voltage drift, high gain and wide bandwidth. The HS-4602RH is ideally suited for this application, delivering superior input and speed characteristics.

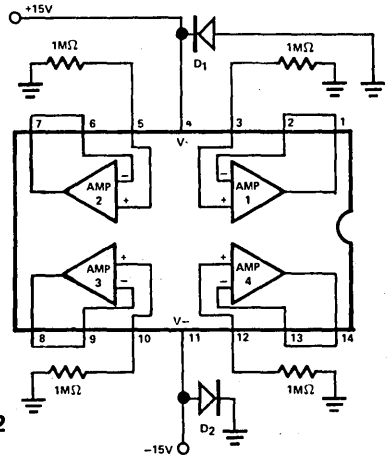
The optional circuitry makes use of the fourth amplifier section as a shield driver which enhances the AC common mode rejection by nullifying the effects of capacitance-to-ground mismatch between input conductors.

Irradiation Circuit



(1/4 OF HS-4602RH DEPICTED)

Burn-in Circuit



NOTES:
T_A = +125°C
D_1, D_2 = IN4002

Radiation Screening Procedure

(1) Two (2) probed good samples per wafer will be selected from ≥20% of the wafers in a run (All wafers in a "run" will have been processed together through all high temperature processing steps and through metallization.)

(2) The sample die shall be assembled and tested for functionality.

(3) The sample devices shall be subjected to a Total Dose Radiation level of 1×10^5 Rad (Si) ±10% from a gamma cell 220 cobalt 60 source or equivalent. The devices will be powered in the configuration illustrated with V_{SUPPLY} = ±15V. The dose rate shall be between 50 rads/sec and 200 rads/sec.

(4) A_{VOL}, V_{IO}, AND I_{BIAS}, with V_{SUPPLY} = ±15V, will be measured and recorded for each device within one hour after irradiation. The lot will be accepted only if the sample, exclusive of non-radiation failures, meets the limits of $A_{VOL} \geq 100K$, $V_{IO} \leq \pm 2.5mV$ and $I_{BIAS} \leq 1.0\ \mu A$ at room temperature.

Radiation Effects

(1) Total Dose
Little or no effect will be observed at 1×10^4 Rad (Si). I_{BIAS}, I_{IO} and A_{VOL} starts to degrade between 1×10^4 and 1×10^5 Rad (Si).

(2) Dose Rate
Devices are constructed in DI and consequently are latchup free.

Test Product Flow

HARRIS SEMICONDUCTOR PRODUCT FLOW
MIL-STD-883, METHOD 5004 CLASS B

100% SCREENING PROCEDURE

	SCREEN	MIL-STD-883 METHOD/COND.
1	Internal Visual	2010 Cond. B.
2	Stabilization Bake	1008 Cond. C (24 hrs. minimum)
3	Temperature Cycling	1010 Cond. C
4	Constant Acceleration	2001 Cond. E; Y1 plane
5	Seal: A Fine B Gross	1014 Cond. A or B 1014 Cond. C2
6	Initial Electrical	Harris Specifications
7	Burn-In Test	1015, 160 hrs. @ 125°C (or equivalent) (Burn-In circuits enclosed)
8	Final Electrical 100% go-no-go	Tested at Worst Case Operating Conditions
9	External Visual	2009 Sample Inspection

Notes:
- Traceability: All devices are assigned date code identification that provides traceability back to the inspection lot.
- Branding: All devices are branded with the part number and EIA date code.
- Aged Products: Product that has been held for more than 24 months will be reinspected prior to shipment to group A inspection requirements.
- Additional Requirements: Sample Group A electrical tests are performed on a lot acceptance basis.

Ordering Information

HS 1 4602RH - 2

- HS — HARRIS
- 1 — PACKAGE: 1 — Cerdip
- 4602RH — DEVICE NUMBER
- 2 — TEMPERATURE: 2 — -55°C to +125°C; 8 — MIL-STD-883B

Sales Offices

EASTERN REGION

8300 Greensboro Drive
McLean, Virginia 22102
(703) 448-5400
TWX: 710-833-0340

Five Old Concord Road
Burlington, MA 01803
(617) 273-1020
TWX: 710-332-1074

106 Seventh Street
Garden City, NY 11530
(516) 747-6776
TWX: 510-220-1527

WESTERN REGION

1503 South Coast Drive
Suite 320
Costa Mesa, CA 92626
(714) 957-6557
TWX: 910-595-1533

EAST COAST

7040 Lake Ellenor Drive
Suite 113
Orlando, FL 32809
(305) 851-9450

MIDWEST REGION

2850 Metro Office Park
Bloomington, MN 55420
(612) 854-3224
TWX: 910-576-3418

HOME OFFICE

P.O. Box 883
Melbourne, FL 32901
(305) 729-5585
TWX: 510-959-6259

EUROPEAN

Harris Systems Ltd.
Semiconductor Programs Division
P.O. Box 27
145 Farnham Road
Slough SL1 4XD
United Kingdom
Tel: 34666
TWX: 848174

HARRIS

CUSTOM INTEGRATED CIRCUITS DIVISION

HARRIS

Preliminary

JULY 1982

HS-508ARH

Radiation Resistant 8 Channel CMOS Analog Multiplexer With Overvoltage Protection

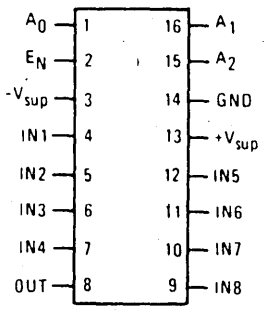
Features

- ANALOG/DIGITAL OVERVOLTAGE PROTECTION
- FAIL SAFE WITH POWER LOSS (NO LATCHUP)
- BREAK-BEFORE-MAKE SWITCHING
- DTL/TTL AND CMOS COMPATIBLE
- ANALOG SIGNAL RANGE ±15V
- ACCESS TIME (TYP.) 500ns
- SUPPLY CURRENT AT 1MHz ADDRESS TOGGLE (TYP.) 4mA
- STANDBY POWER (TYP.) 7.5mW
- RADIATION ENVIRONMENT

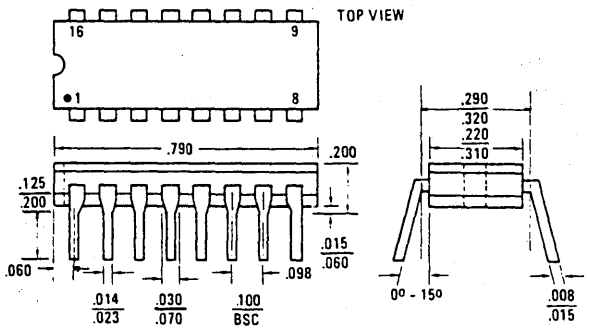
NEUTRON FLUENCE (ϕ) 1 x 10^9 n/cm^2 (E $\geqslant$ 10KeV)
GAMMA RATE ($\dot{\gamma}$) . . . . . 1 x 10^8 RADs(Si)/s
GAMMA DOSE (γ) . . . . . 1 x 10^5 RADs(Si)

Pinout

TOP VIEW



Package

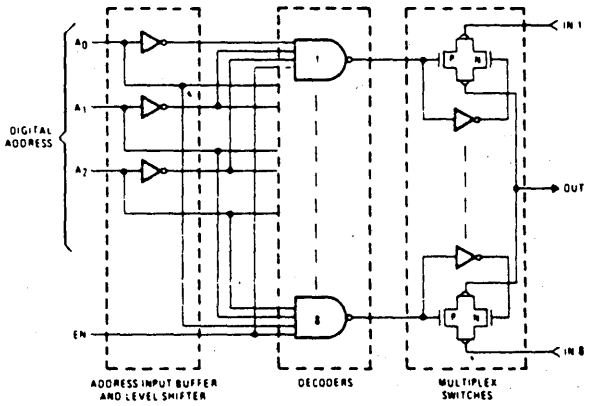


Description

The HS-508ARH is a dielectrically isolated, radiation resistant, CMOS analog multiplexer incorporating an important feature; it withstands analog input voltages much greater than the supplies. This is essential in any system where the analog inputs originate outside the equipment. They can withstand a continuous input up to 10 volts greater than either supply, which eliminates the possibility of damage when supplies are off, but input signals are present. Equally important, it can withstand brief input transient spikes of several hundred volts; which otherwise would require complex external protection networks. Necessarily, ON resistance is somewhat higher than similar unprotected devices, but very low leakage current combine to produce low errors. Reference Application Notes 520 and 521, available from the Analog Products Division of Harris, for further information on the 508A multiplexer in general.

The HS-508ARH has been specifically designed to meet exposure to radiation environments. Operation from −55°C to +125°C is guaranteed.

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge.

ABSOLUTE MAXIMUM RATINGS

Voltage between Supply Pins 40V

V+ to Ground 20V

V_{EN}, V_A, Digital Input Overvoltage:

V_A | V_{Supply}(+) +4V
V_{Supply} (-) -4V

Analog Input Overvoltage:

V_S | V_{Supply} (+) +20V
V_{Supply} (-) -20V

Total Power Dissipation* 725 mW

Operating Temperature -55°C to +125°C

Storage Temperature -65°C to +150°C

*Derate 8mW/°C above t_A = 75°C

ELECTRICAL CHARACTERISTICS (Unless Otherwise Specified)

Supplies = +15V, -15V; V_{AH} (Logic Level High) = +4.0V; V_{AL} (Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characteristics section.

PARAMETER	TEMP	-55°C to +125°C MIN	TYP	MAX	UNITS
ANALOG CHANNEL CHARACTERISTICS					
*V_S, Analog Signal Range	Full	-15		+15	V
*R_{ON}, On Resistance (Note 1)	+25°C		1.2	1.5	KΩ
	Full		1.5	1.8	KΩ
*$I_{S(OFF)}$, Off Input Leakage Current	+25°C		0.03		nA
	Full			±50	nA
*$I_{D(OFF)}$, Off Output Leakage Current	+25°C		1.0		nA
	Full			±250	nA
*$I_{D(OFF)}$ with Input Overvoltage Applied (Note 2)	+25°C		4.0		nA
	Full			2.0	μA
*$I_{D(ON)}$, On Channel Leakage Current	+25°C		0.1		nA
	Full			±250	nA
DIGITAL INPUT CHARACTERISTICS					
V_{AL}, Input Low Threshold (Note 6)	Full			0.8	V
V_{AH}, Input High Threshold (Note 6)	Full	4.0			V
*I_A, Input Leakage Current (High or Low)	Full			1.0	μA
SWITCHING CHARACTERISTICS					
t_A, Access Time	+25°C		0.5	1.0	μs
t_{OPEN}, Break - Before Make Delay	+25°C		80		ns
$t_{ON(EN)}$, Enable Delay (ON)	+25°C		300		ns
$t_{OFF(EN)}$, Enable Delay (OFF)	+25°C		300		ns
Settling Time (0.1%)	+25°C		1.2		μs
(0.025%)	+25°C		3.5		μs
"OFF Isolation" (Note 3)	+25°C		65		dB
$C_{S(OFF)}$, Channel Input Capacitance	+25°C		5		pF
$C_{D(OFF)}$, Channel Output Capacitance	+25°C		25		pF
C_A, Digital Input Capacitance	+25°C		5		pF
$C_{DS(OFF)}$, Input to Output Capacitance	+25°C		0.1		pF
POWER REQUIREMENTS					
P_D, Power Dissipation	Full		7.5		mW
*I+, Current (Note 4)	Full		0.5	2.0	mA
*I-, Current (Note 4)	Full		0.02	1.0	mA
*I+, Standby (Note 5)	Full		0.5	2.0	mA
*I-, Standby (Note 5)	Full		0.02	1.0	mA

Truth Table

A_2	A_1	A_0	E_N	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

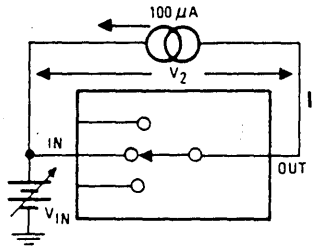
NOTES:
1. V_{OUT} = ± 10V, I_{OUT} = -100μA
2. Analog Overvoltage = ± 33V
3. V_{EN} = 0.8V, R_L = 1K, C_L = 7pF, V_S = 3V RMS, f = 500KHz
4. V_{EN} = +4.0V
5. V_{EN} = 0.8V
6. To drive from DTL/TTL Circuits, 1KΩ pull-up resistors to +5.0V supply are recommended

100% Tested for Dash 8 at +25°C and +125°C Only.

UNLESS OTHERWISE SPECIFIED: $T_A = 25^oC$, $V_{SUPPLY} = +15V$, $V_{AH} = +4V$, $V_{AL} = 0.8V$

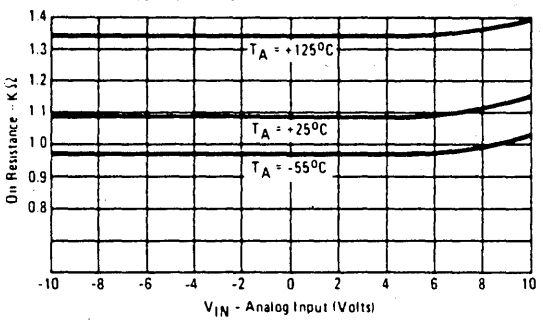
TEST CIRCUIT NO. 1

$R_{ON} = \frac{V_2}{100\mu A}$

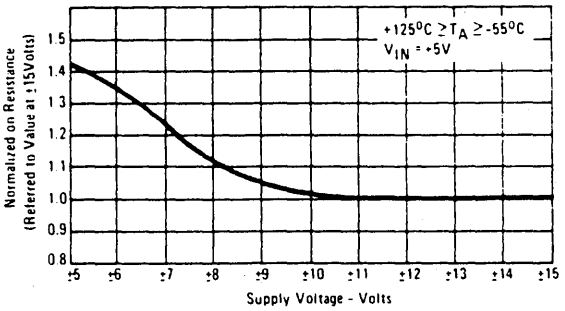


ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE

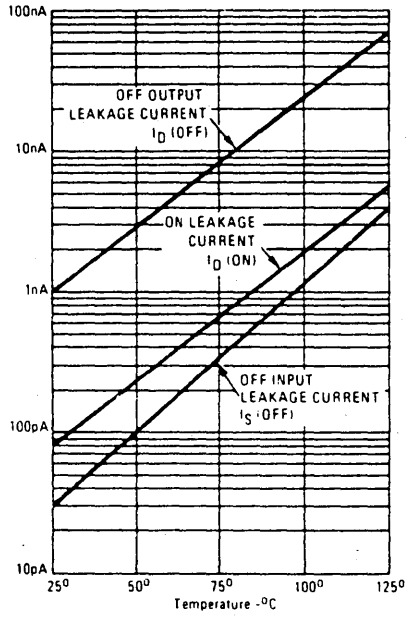
ON RESISTANCE vs. ANALOG INPUT VOLTAGE



NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE

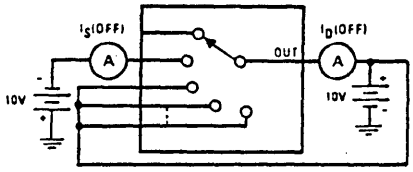


LEAKAGE CURRENT vs. TEMPERATURE



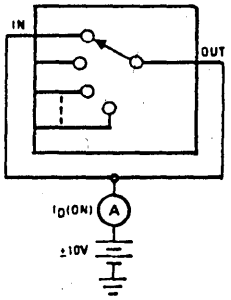
TEST CIRCUIT NO. 2

OFF LEAKAGE CURRENT vs. TEMPERATURE

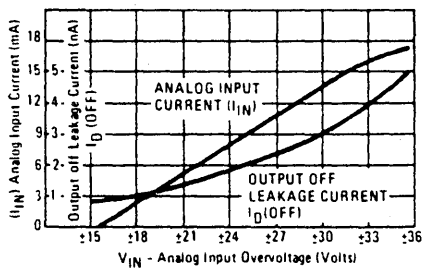


ON LEAKAGE CURRENT vs. TEMPERATURE

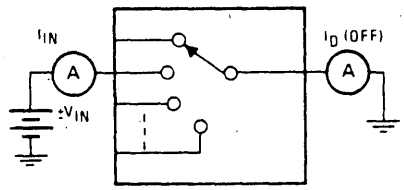
TEST CIRCUIT NO. 3



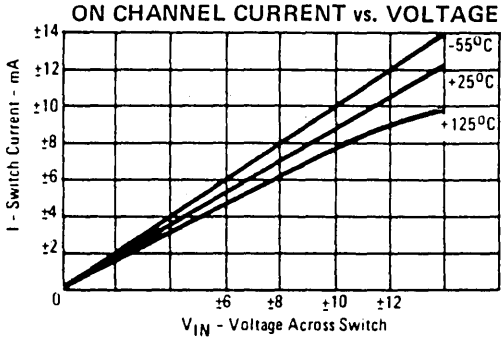
ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



TEST CIRCUIT NO. 4

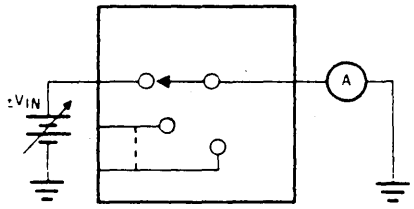


ON CHANNEL CURRENT vs. VOLTAGE



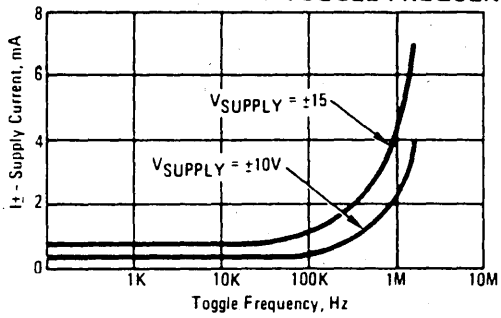
TEST CIRCUIT NO. 5

ON CHANNEL CURRENT vs. VOLTAGE

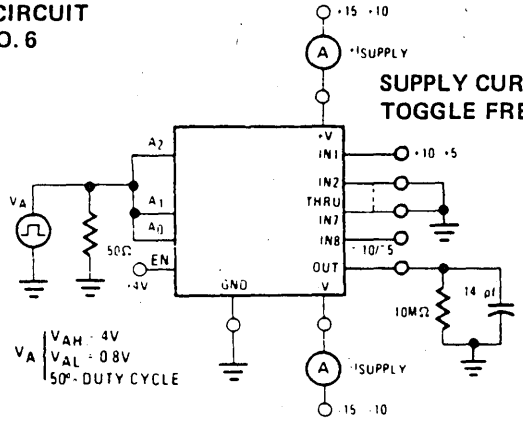


TEST CIRCUIT NO. 6

SUPPLY CURRENT vs. TOGGLE FREQUENCY

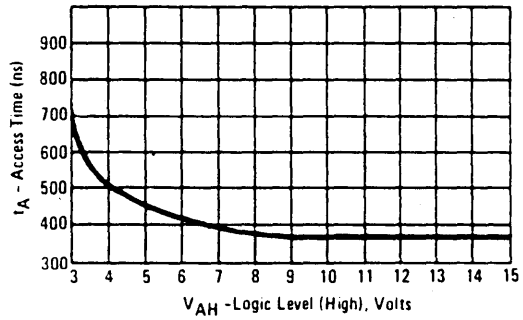


SUPPLY CURRENT vs. TOGGLE FREQUENCY

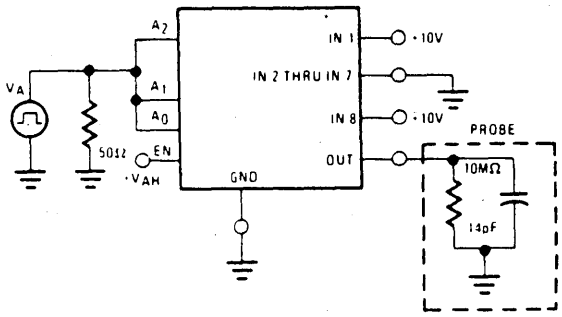


TEST CIRCUIT NO. 7

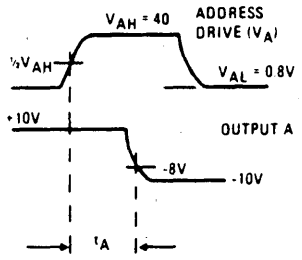
ACCESS TIME vs. LOGIC LEVEL (HIGH)



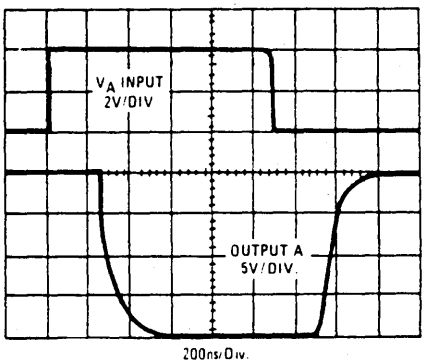
ACCESS TIME vs. LOGIC LEVEL (HIGH)



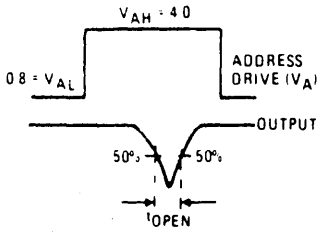
Switching Waveforms

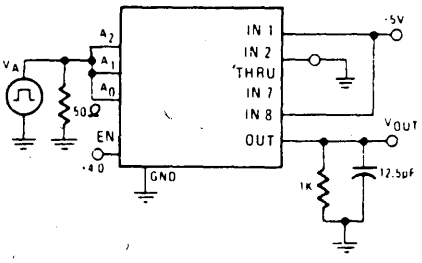


ACCESS TIME

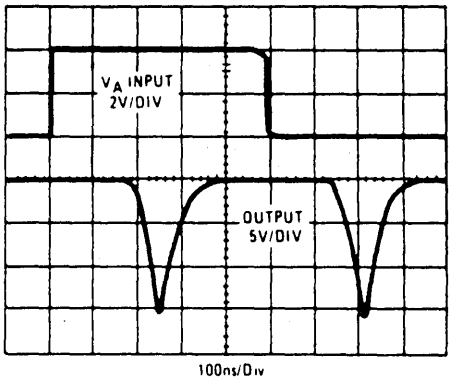


TEST CIRCUIT
NO. 8
BREAK BEFORE MAKE DELAY (t_{OPEN})

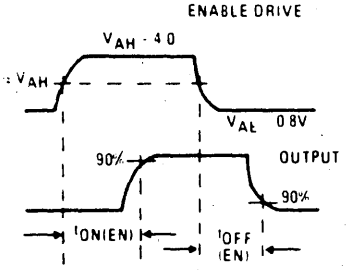


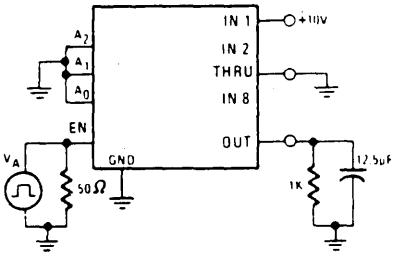


BREAK BEFORE MAKE DELAY (t_{OPEN})

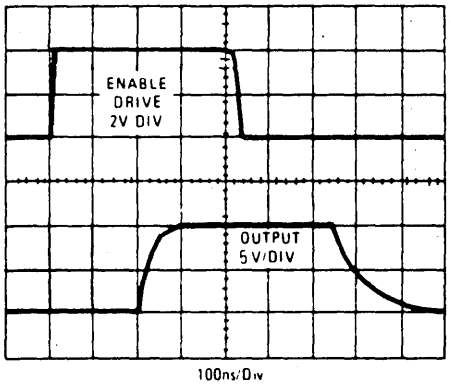


TEST CIRCUIT
NO. 9
ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)



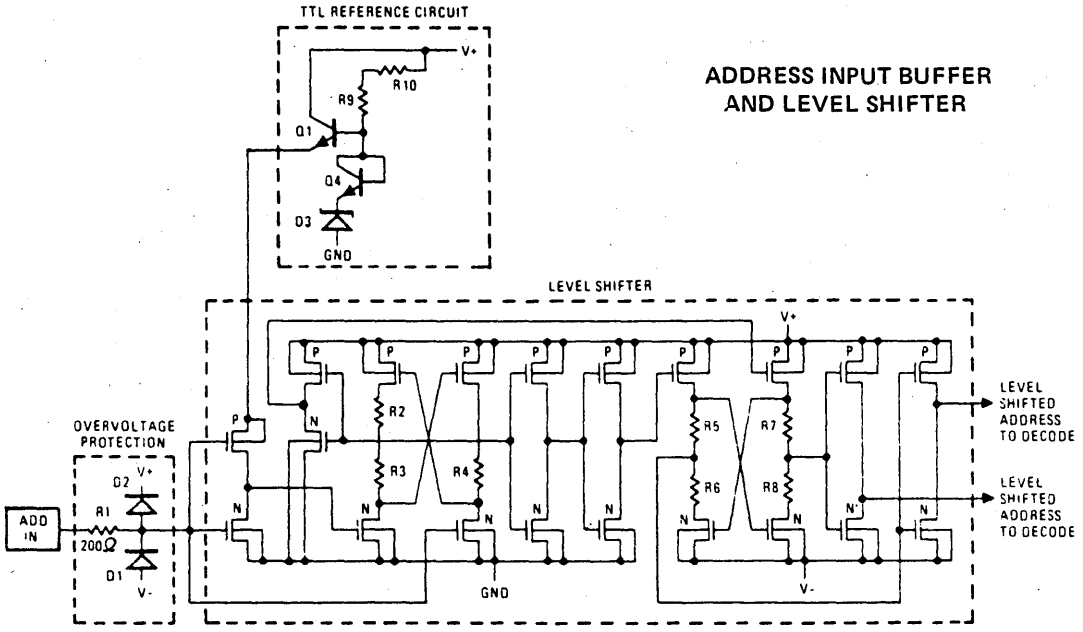


ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)

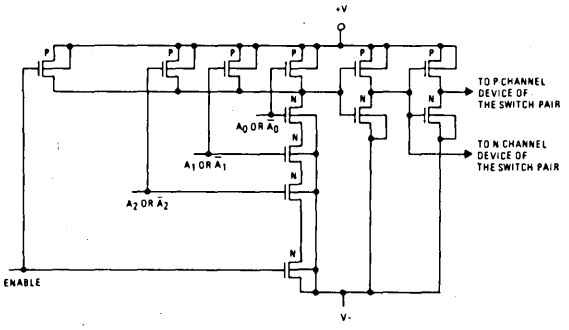


Schematic Diagrams

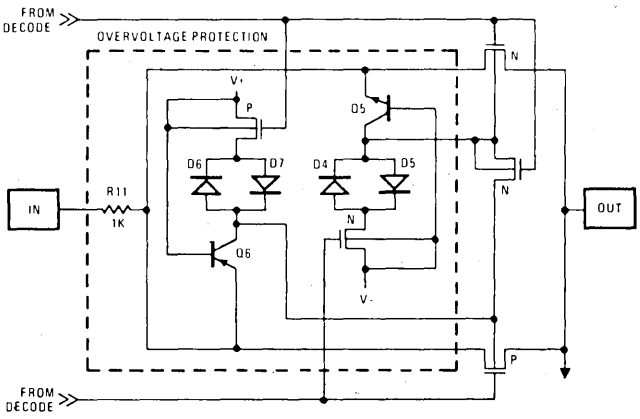
ADDRESS INPUT BUFFER
AND LEVEL SHIFTER



ADDRESS DECODER



MULTIPLEX SWITCH



Radiation Screening Procedure

(1) Two (2) probed good samples per wafer will be selected from ≥20% of the wafers in a run. (All wafers in a "run" will have been processed together through all high temperature processing steps and through metallization.)

(2) The sample die shall be assembled and tested for functionality.

(3) The sample devices shall be subjected to a Total Dose Radiation level of 1 x 10^5 Rad (Si) ±10% from a Gamma Cell 220 Cobalt 60 source or equivalent. The devices will be powered in the configuration illustrated with V_{SUPPLY} = ±15V. The dose rate shall be between 50 rads/sec and 200 rads/sec.

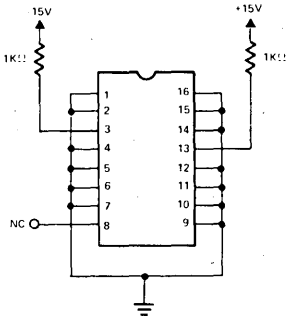
(4) On Current Leakage $I_{D(ON)}$ with V_{SUPPLY} = ±15V will be measured and recorded for each device within one hour after irradiation. The lot will be accepted only if the sample meets the limit of $I_{D(ON)} \leq 1\mu A$ when tested at 25°C.

Radiation Effects

(1) TOTAL DOSE:
Very little degradation of any of the parameters will be seen up to γ = 1 x 10^5 Rad (Si).

(2) DOSE RATE:
The HS508A RH is manufactured in DI, consequently, it is latch up free.

Irradiation Bias Circuit



Sales Offices

EASTERN REGION

8300 Greensboro Drive
McLean, Virginia 22102
(703) 448-5400
TWX: 710-833-0340

Five Old Concord Road
Burlington, MA 01803
(617) 273-1020
TWX: 710-332-1074

106 Seventh Street
Garden City, NY 11530
(516) 747-6776
TWX: 510-220-1527

WESTERN REGION

1503 South Coast Drive
Suite 320
Costa Mesa, CA 92626
(714) 957-6557
TWX: 910-595-1533

EAST COAST

7040 Lake Ellenor Drive
Suite 113
Orlando, FL 32809
(305) 851-9450

MIDWEST REGION

2850 Metro Office Park
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(612) 854-3224
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HARRIS

CUSTOM INTEGRATED CIRCUITS DIVISION

HARRIS

Preliminary

JULY 1982

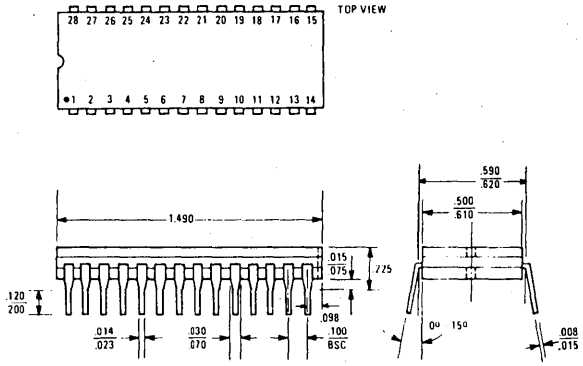
HS-1840RH

Radiation Resistant 16 Channel CMOS Analog Multiplexer with High-Z Analog Input Protection

Features

- HIGH ANALOG INPUT IMPEDANCE DURING POWER LOSS (OPEN) — 500MΩ
- LOW POWER CONSUMPTION (STANDBY) — 600μW
- ACCESS TIME — 500ns
- EXCELLENT IN HI-REL REDUNDANT SYSTEMS
- BREAK-BEFORE-MAKE SWITCHING
- NO LATCH-UP
- RADIATION ENVIRONMENT
  - NEUTRON FLUENCE (ϕ) . 1×10^9 n/cm^2 ($E \geq 10$KeV)
  - GAMMA RATE ($\dot{\gamma}$) . . . . . 1×10^8 RADs (Si)/s
  - GAMMA DOSE (γ) . . . . . 2×10^5 RADs(Si)

Package



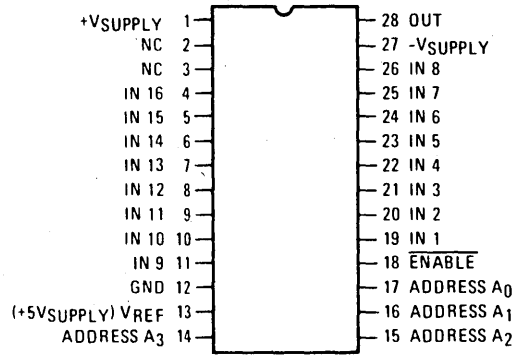
Description

The HS-1840RH is a radiation resistant, monolithic 16 channel multiplexer constructed with the Harris Linear Dielectric Isolation CMOS process. It is designed to provide a high input impedance to the analog source if device power fails (open) or the analog signal voltage inadvertently exceeds the supply rails during powered operation. Excellent for use in redundant applications, since the secondary device can be operated in a standby unpowered mode affording no additional power drain. But more significantly, a very high impedance exists between the active and inactive devices preventing any interaction. One of sixteen channel selection is controlled by a 4-bit binary address plus an Enable-Inhibit input which conveniently controls the ON/OFF operation of several multiplexers in a system. All digital inputs have electrostatic discharge protection.

The HS-1840RH has been specifically designed to meet exposure to radiation environments. It is available in a 28 pin dual-in-line package and is guaranteed operational from −55°C to +125°C.

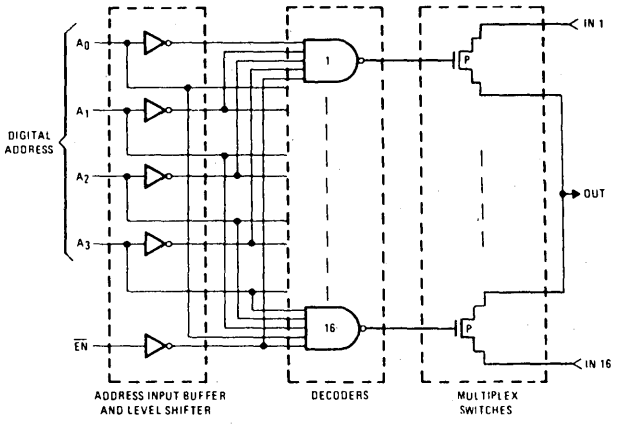
Pinout

TOP VIEW



CAUTION: These devices are sensitive to electronic discharge.

Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 1 and 27 +40V
V_{REF} to Ground +20V
V_{EN}, V_A, Digital Input Overvoltage:
V_A V_{REF} +4V
Ground -4V
Analog Input Overvoltage:
V_S V_{Supply} (+) +20V
V_{Supply} (-) −20V

Total Power Dissipation* 1200mW
Operating Temperature -55°C to +125°C
Storage Temperature -65°C to +150°C

*Derate 8mW/°C above T_A = +25°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified:
Supplies = +15V, -15V: V_{REF}(Pin 13) = +5V; V_{AH}(Logic Level High) = 4.0V; V_{AL}(Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characteristics section.

		-55°C to +125°C			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS					
*V_S, Analog Signal Range	Full	-5		+15	V
*R_{ON}, On Resistance (Note 1) V_{IN} = +15V	Full		0.5	1.0	KΩ
V_{IN} = -5V	Full		2.5	5.0	KΩ
*I_S(OFF), Off Input Leakage Current	+25°C		0.03		nA
	Full			±100	nA
*I_S(OFF), with Power Off (Note 8)	Full			±100	nA
*I_D(OFF), Off Output Leakage Current	+25°C		1.0		nA
	Full			±1000	nA
* I_D(OFF), or I_S(OFF) with Input Overvoltage Applied (Note 2)	+25°C		50		nA
	Full			±1000	nA
*I_D(ON), On Channel Leakage Current	+25°C		1.0		nA
	Full			±1000	nA
DIGITAL INPUT CHARACTERISTICS					
V_{AL}, Input Low Threshold | TTL Drive	Full			0.8	V
V_{AH}, Input High Threshold | (Note 7)	Full	4.0			V
V_{AL} | MOS Drive (Note 3)	+25°C			0.8	V
V_{AH} |	+25°C	6.0			V
*I_A, Input Leakage Current (High or Low)	Full			1.0	µA
SWITCHING CHARACTERISTICS					
t_A, Access Time	+25°C		500	1000	ns
t_{OPEN}, Break-Before-Make Delay	+25°C	20	80		ns
t_{ON}(EN), Enable Delay (ON)	+25°C		300	1000	ns
t_{OFF}(EN), Enable Delay (OFF)	+25°C		300	1000	ns
Settling Time (0.1%)	+25°C		1.2		µs
(0.025%)	+25°C		4.1		µs
"Off Isolation" (Note 4)	+25°C		65		dB
C_S(OFF), Channel Input Capacitance	+25°C		5		pF
C_D(OFF), Channel Output Capacitance	+25°C		50		pF
C_A, Digital Input Capacitance	+25°C		5		pF
C_{DS}(OFF), Input ot Output Capacitance	+25°C		0.15		pF
POWER REQUIREMENTS					
P_D, Power Dissipation (Note 5)	+25°C		0.6	15.0	mW
(Note 6)	+25°C		0.6	15.0	mW
*I+, Current Pin 1 (Note 5)	Full		0.02	0.5	mA
*I-, Current Pin 27 (Note 5)	Full		0.02	0.5	mA
*I+, Standby (Note 6)	Full		0.02	0.5	mA
*I-, Standby (Note 6)	Full		0.02	0.5	mA

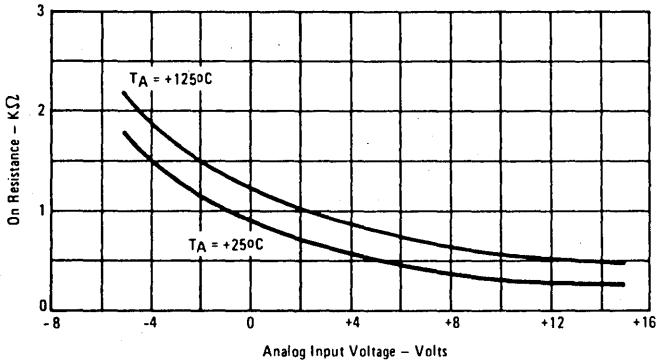
Truth Table

A_3	A_2	A_1	A_0	$\overline{EN}$	"ON" CHANNEL
X	X	X	X	H	NONE
L	L	L	L	L	1
L	L	L	H	L	2
L	L	H	L	L	3
L	L	H	H	L	4
L	H	L	L	L	5
L	H	L	H	L	6
L	H	H	L	L	7
I	H	H	H	L	8
H	L	L	L	L	9
H	L	L	H	L	10
H	L	H	L	L	11
H	L	H	H	L	12
H	H	L	L	L	13
H	H	L	H	L	14
H	H	H	L	L	15
H	H	H	H	L	16

NOTES:
1. I_{OUT} = 1mA
2. Analog Overvoltage = ±20V
3. V_{REF} = +10V
4. V_{EN} = 4.0V, R_L = 1K, C_L = 7pF, V_S = 3VRMS, f = 500kHz
5. V_{EN} = 0.8V
6. V_{EN} = 4.0V
7. To drive from DTL/TTL circuits 1K pull-up resistors to +5.0V supply are recommended
8. All supplies (V+, V-, +5V) and digital inputs (A_0, A_1, A_2, A_3, EN) opened. Analog input ±10V.

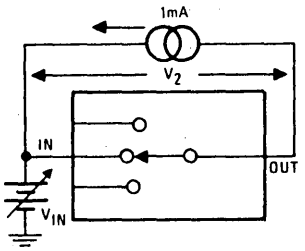
Unless Otherwise Specified: $T_A = 25^oC$, $V_{SUPPLY} = \pm 15V$, $V_{AH} = +4V$, $V_{AL} = 0.8V$ and $V_{REF} = 5V$.

ON RESISTANCE VS. ANALOG INPUT VOLTAGE

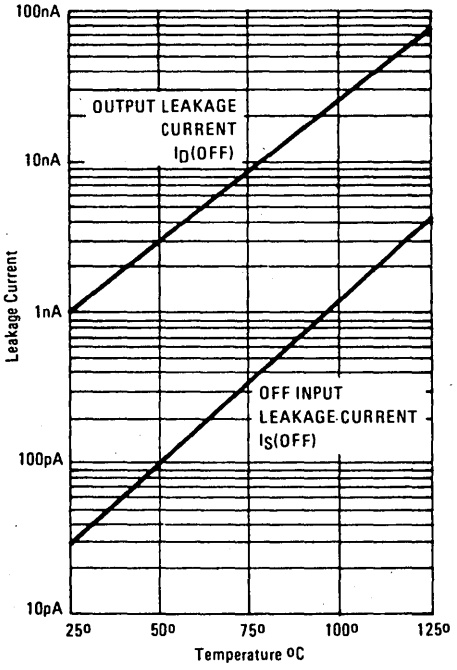


ON RESISTANCE vs INPUT SIGNAL LEVEL

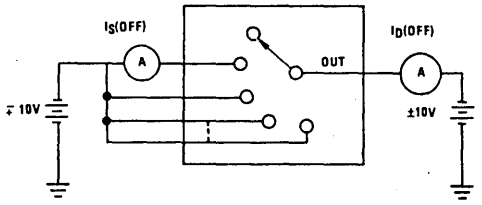
$R_{ON} = \frac{V_2}{1mA}$



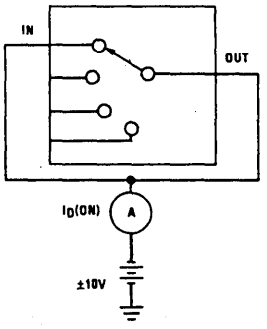
LEAKAGE CURRENT VS. TEMPERATURE



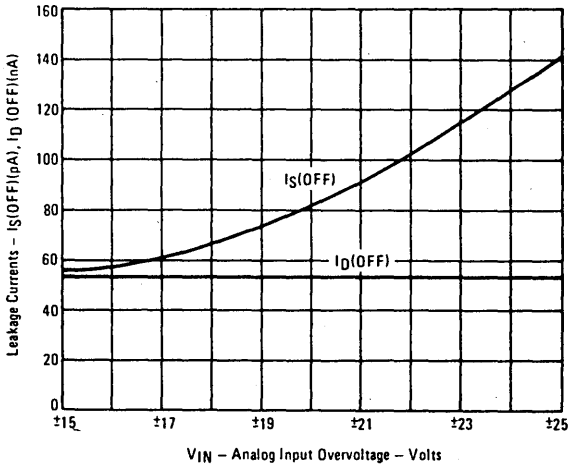
OFF LEAKAGE CURRENT vs TEMPERATURE



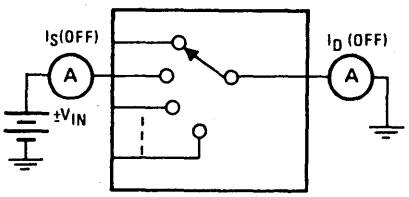
ON LEAKAGE CURRENT vs TEMPERATURE



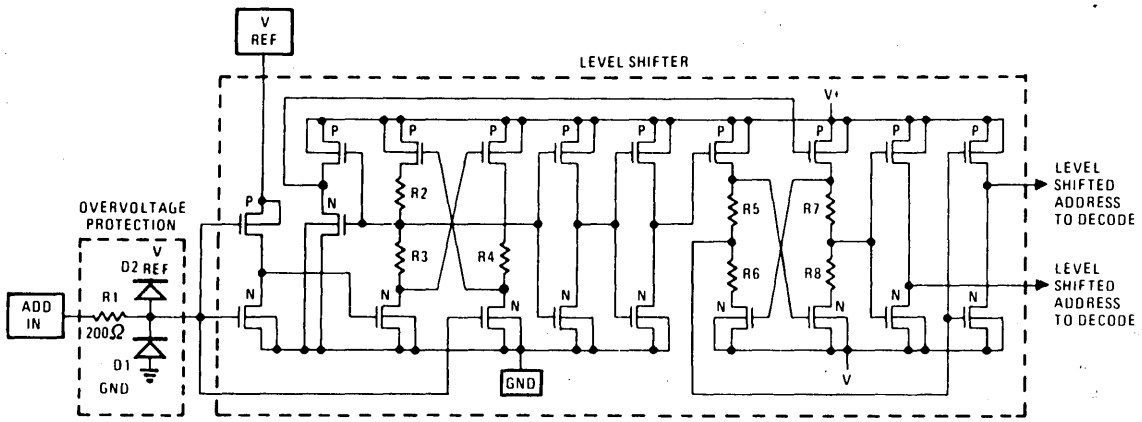
ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



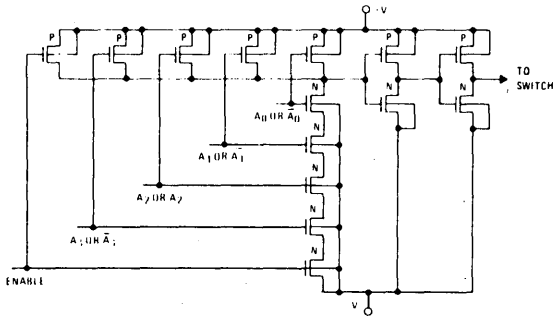
ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



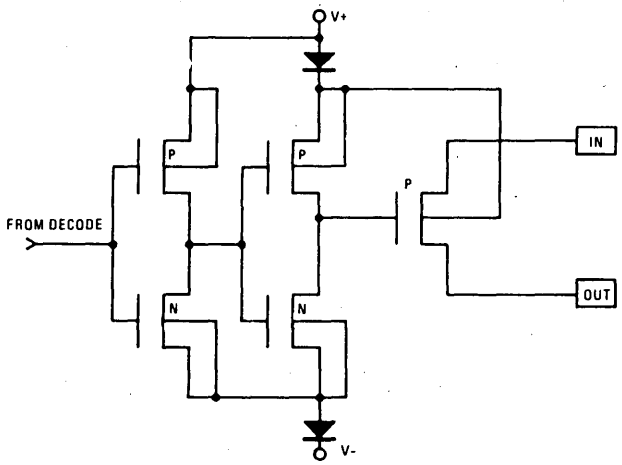
ADDRESS AND ENABLE INPUT BUFFER AND LEVER SHIFTER



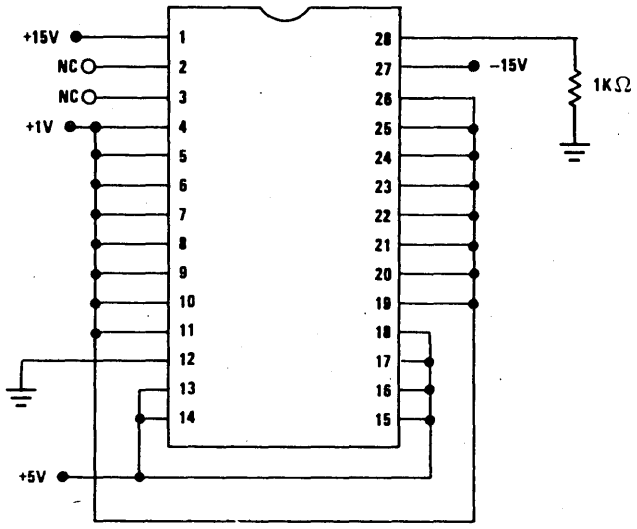
ADDRESS DECODER



MULTIPLEXER SWITCH



HS1840RH IRRADIATION CONFIGURATION



Radiation Screening Procedure

(1) Two (2) probed good die per wafer will be selected from $\geq$20% of the wafers in a run. (All wafers in a "run" will have been processed together through all high temperature processing steps and through metallization.)

(2) The sample die shall be assembled and tested for functionality.

(3) The sample devices shall be subjected to a Total Dose Radiation level of 2×10^5 Rad (Si) $\pm$ 10% from a Gamma Cell 220 Cobalt 60 source or equivalent. The devices will be powered in the configuration illustrated with $V_{SUPPLY} = \pm 15V$. The dose rate shall be between 50 rads/sec and 200 rads/sec.

(4) On Current Leakage $I_{D(ON)}$ with $V_{SUPPLY} = \pm 15V$ will be measured and recorded for each device within one hour after irradiation. The lot will be accepted only if the sample meets the limit of $I_{D(ON)} \leq 1\ \mu A$ when tested at 25°C.

Radiation Effects

(1) TOTAL DOSE:
Very little degradation of any of the parameters will be seen up to $\gamma = 2 \times 10^5$ Rad (Si).

(2) DOSE RATE:
The HS-1840RH is manufactured in DI, consequently, it is latch up free.

Product Test Flow

HARRIS SEMICONDUCTOR PRODUCT FLOW
MIL-STD-883, METHOD 5004 CLASS B

100% SCREENING PROCEDURE

	SCREEN	MIL-STD-883 METHOD/COND.
1	Internal Visual	2010 Cond. B.
2	Stabilization Bake	1008 Cond. C (24 hrs. minimum)
3	Temperature Cycling	1010 Cond. C
4	Constant Acceleration	2001 Cond. E; Y1 plane
5	Seal: A Fine B Gross	1014 Cond. A or B 1014 Cond. C2
6	Initial Electrical	Harris Specifications
7	Burn-In Test	1015, 160 hrs. 125°C (or equivalent)
8	Final Electrical 100% go-no-go	Tested at Worst Case Operating Conditions
9	External Visual	2009 Sample Inspection

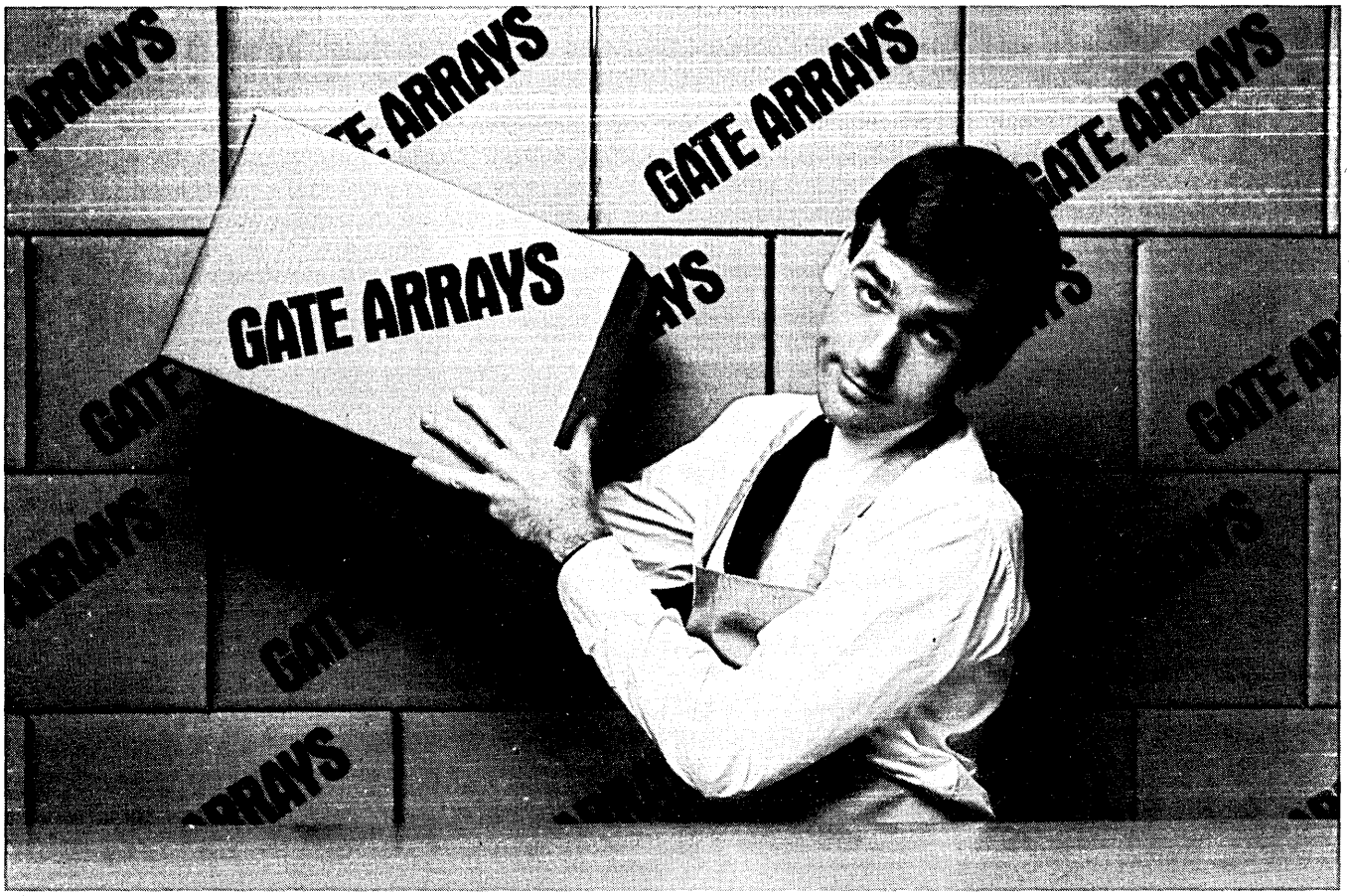
Note:

Traceability: All devices are assigned date code identification that provides traceability back to the inspection lot.

Branding: All devices are branded with the part number and EIA date code.

Aged Products: Product that has been held for more than 24 months will be reinspected prior to shipment to group A inspection requirements.

Additional Requirements: Sample Group A electrical tests are performed on a lot acceptance basis.



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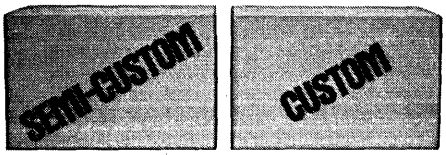

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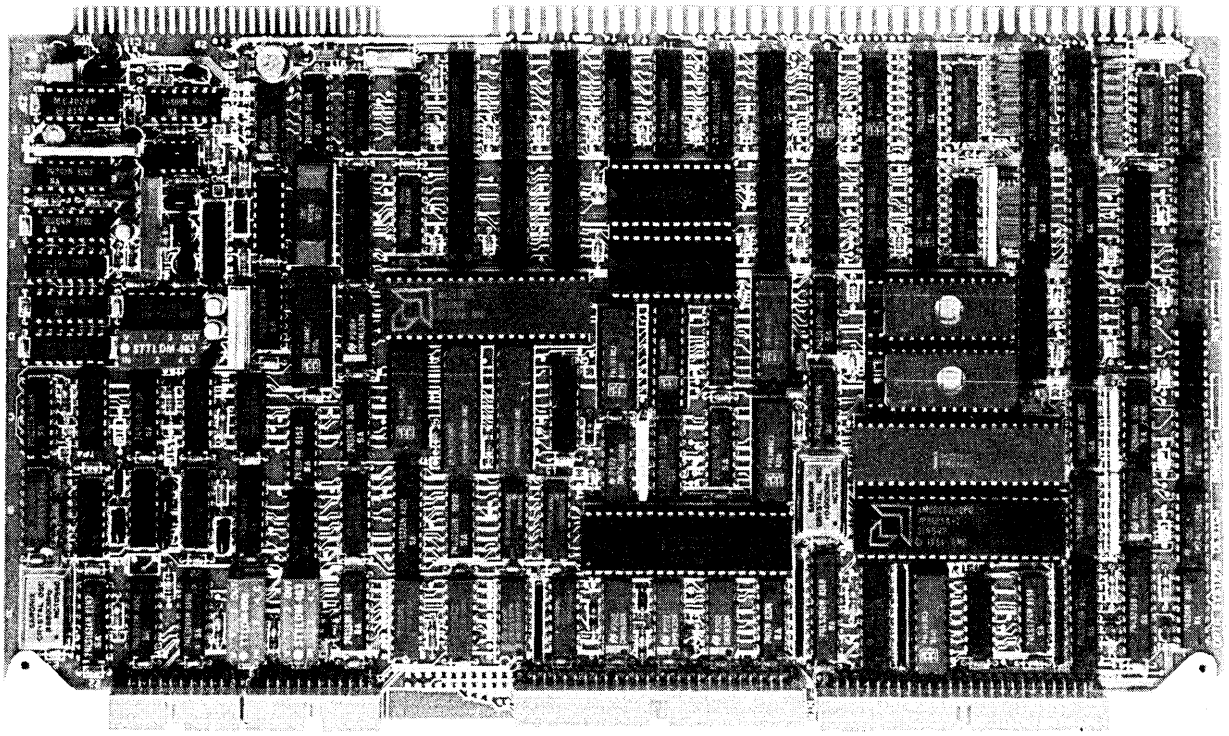

The Data System Design 7215 is a single-board controller with pipelined architecture that can simultaneously control Winchester, streaming tape, and floppy drives.

Device No.	Description
AM25LS2569	Up-Down Binary Counter with Synchronous Preset
AM2910	Dual Retriggerable Monostable Multivibrator
AM26S02	Programmable Schottky Read-Only Memory
AM27S35	12-Bit Microprogram Controller
AM8085	Complete 8-Bit Parallel Central Processing Unit
CA3130	5-to-16-Volt Single Stash Supply Op Amp
2732	4096 x 8 TTL PROM
8237	DMA Controller
DM7438	Quad 2-Input TTL NAND Buffer
DM8334	8-Bit Addressable TTL Latch
DS75107	Differential Line Receiver
F74S132	Quad 2-Input NAND Schmitt-Trigger
MC4024	Dual Voltage-Controlled TTL Multivibrator
MK4802	2048 x 8 Static NMOS RAM
PAL16L8	Field Programmable Logic Array
PAL16R6	Field Programmable Logic Array
PAL16R8	Field Programmable Logic Array
7407	Hex Buffer/Driver
74123	Dual Retriggerable Monostable Multivibrator
74368	Hex Inverter, 3-State
74LS02	Quad 2-Input TTL NOR Gate
74LS04	Hex Inverter
74LS125	Quad Gated TTL Buffer, 3-State
74LS138	3 Line to 8 Line Decoder/Demultiplexer
74LS151	8-Input Multiplexer
74LS161	Binary Counter
74LS166	8-Bit Parallel-In, Serial-Out Shift Register with Clear

Device No.	Description
74LS174	Hex D-Type Edge-Triggered Flip-Flop with Clear
74LS240	Octal Bus Driver (Schmitt Trigger)
74LS244	Octal Bus Driver (Schmitt Trigger), Non-Inverting
74LS257	Quad 2-Input Multiplexer, Non-Inverting
74LS273	Octal D-Type Edge-Triggered Flip-Flop, 3-State
74LS299	8-Bit Universal Shift Register
74LS365	Hex Buffer, 3-State
74LS373	8-Bit Latch
74LS374	Octal D-Type Edge-Triggered Flip-Flop, 3-State
74LS393	Dual 4-Bit Binary Counter
74LS533	D-Type 8-Bit Latch
74LS670	16-Bit (4x4) Register File with Simultaneous Read/Write
74S00	Quad 2-Input NAND Gate
74S03	Quad 2-Input NAND Gate, Open Collector
74S04	Hex Inverter
74S112	Dual "J-K" Negative Edge-Triggered Flip-Flop
74S151	8-Input Multiplexer
74S153	Dual 4-Input Multiplexer
74S174	Hex D-Type Edge-Triggered Flip-Flop with Clear
74S175	Quad D-Type Edge-Triggered Flip-Flop with Clear
74S240	Line Driver, Single Ended, 3-State, Inverting
74S32	Quad 2-Input OR Gate
74S51	Dual 2-Wide 2-Input AND-OR-Invert Gate
74S64	4-2-3-2-Input AND-OR-Invert Gate
74S74	Dual D-Type Positive Edge-Triggered Flip-Flop
75110	Line Driver, Differential, Twisted Pair Level Shifting

Representative list of ICs on the Data Systems Design 7215 board.
Key specifications for all of these ICs can be found in IC MASTER.

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LINEAR MONOCHIPS

Designation	Technology	Size-Mils	Components	Voltage	Pads	Integration Fee
MOA	Bipolar	71 x 81	260	20V max	16 max	$3700
MOB	"	81 x 81	300	20V max	24 max	$3700
MOC	"	51 x 56	110	20V max	14 max	$2800
MOD	"	80 x 80	194	36V max	16 max	$3700
MOE	"	70 x 70	187	20V max	18 max	$3100
MOF	"	91 x 110	437	20V max	24 max	$4500
MOG	"	75 x 78	310	20V max	18 max	$3400
MOH	"	77 x 88	382	20V max	18 max	$3400
MOJ	"	61 x 65	170	20V max	18 max	$2800
MOL	"	81 x 100	416	20V max	24 max	$3900
MOM	"	101 x 151	812	20V max	28 max	$7000
MON	"	123 x 157	1070	20V max	40 max	$10000
MOP	"	90 x 121	623	20V max	24 max	$5000
MOQ	"	73 x 76	304	20V max	18 max	$4000
MLA	CMOS	136 x 185	1695	3 to 15V	42 max	$8500

DIGITAL MONOCHIPS

Designation	Technology	Size-Mils	Logic Cells	Gates	Gate Delay	Gate Power	Voltage	Pads	Integration Fee
MDA	NMOS	138 x 138	224	262	20ns	0.2mW	5 to 12V	40 max	$4500
MUA	Bipolar	131 x 131	225	450	25ns	2.0mW	*1 to 1.5V	"	"
MUB	"	"	"	"	200ns	0.2mW	"	"	"
MUC	"	"	"	"	10ns	2.5mW	"	"	"
MSA	"	157 x 157	"	"	8ns	1mW	5V max	"	"
MSB	"	200 x 186	440	880	"	"	"	52 max	$7800
MSC	"	191 x 205	990	1980	"	"	"	64 max	$17000
MCA	CMOS	112 x 124	112	140	13ns	<5μW**	3 to 15V	32 max	$4000
MCB	"	136 x 136	162	200	"	"	"	38 max	$4250
MCC	"	136 x 174	216	270	"	"	"	44 max	$4500
MCD	"	174 x 174	224	440	"	"	"	52 max	$5000
MCE	"	136 x 174	160	340	"	"	"	44 max	$4750
MCF	"	195 x 197	504	630	"	"	"	60 max	$6500
MCG	"	219 x 216	640	800	"	"	"	68 max	$7500
MPX	Si-CMOS	195 x 235	400	1000	5ns	.14mW***	12V max	80 max	$9000
MPA	"	125 x 146	204	510	3.5ns	"	7V max	56 max	****
MPB	"	162 x 194	400	1000	"	"	"	70 max	"
MPC	"	187 x 230	600	1500	"	"	"	91 max	"
MPD	"	225 x 242	800	2000	"	"	"	104 max	"
MRA	Bipolar	135 x 125	224	500	2.5ns	0.3mW	5V max	40 max	"
MRB	"	168 x 153	378	900	"	"	"	50 max	"
MRC	"	185 x 169	504	1200	"	"	"	58 max	"
MRD	"	215 x 193	672	1600	"	"	"	68 max	"
MRE	"	215 x 215	784	1800	"	"	"	72 max	"
MRF	"	231 x 231	900	2000	"	"	"	80 max	"

*1 volt requires close work with Interdesign. **Frequency dependent, gate power at low frequency.
***Bipolar power at max frequency, CMOS at max frequency. ****Contact Interdesign Marketing.

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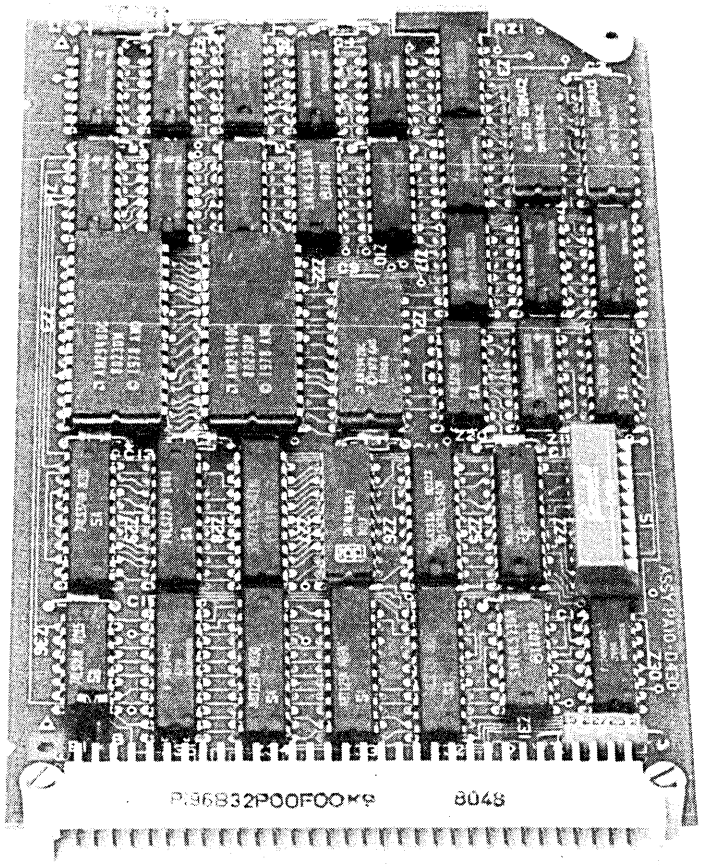
For Key Data On Every IC On This Board, The Place To Look Is...



This Rockwell RM65-5104(E) card is used to transfer data between memory and peripheral circuits.

Device No.	Description
74LS08	Quad 2-Input AND Gate
74F244	Octal Buffer/Line Driver
74LS240	Octal Bus Driver (Schmitt Trigger)
74LS136	Quad 2-Input Exclusive-OR Gate
74F04	Hex Inverter
74LS374	Octal D-Type Edge-Triggered Flip-Flop, 3-State
74LS273	Octal Edge-Triggered Flip-Flop with Clear
74LS541	Octal Bus Driver, Noninverting
74LS645	Octal Bus Transceiver
74LS540	Octal Bus Driver, Inverting

Device No.	Description
74LS682	8-Bit Magnitude Comparitor
AM2940	DMA Address Generator
AM2942	Programmable Timer
74LS155	Decoder/Demultiplexer
74LS148	Priority Encoder
74LS74	Dual D-Type Edge-Triggered Flip-Flop
74LS32	Quadruple 2-Input OR Gate
74LS112	Dual J-K Flip-Flop
74LS126	Quadruple Bus Buffer Gate
74LS00	Quadruple 2-Input NAND Gate
PAL12H6	Field Programmable Array

Representative list of ICs on Rockwell Direct Memory Access Card.
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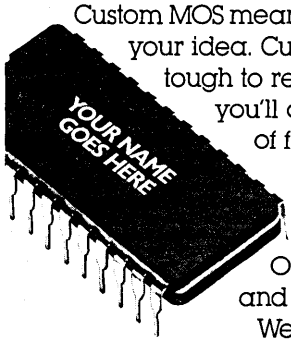

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CUSTOM/SEMICUSTOM

Points to ponder when looking for a custom LSI manufacturer.

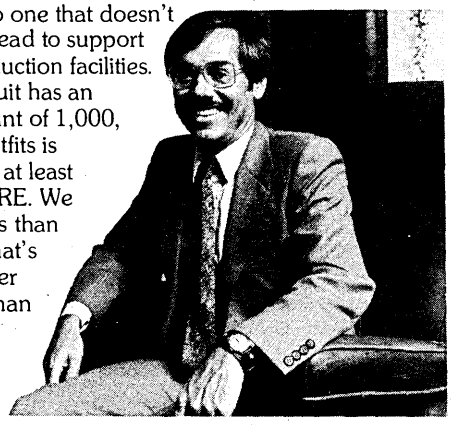
Can you work closely with their engineers?

It's really essential that you be able to. A custom MOS/LSI circuit is *truly* a custom job, and the more active the interplay between you (or your engineers) and the custom LSI manufacturers engineers, the more perfectly it will fit your product.

Our customers tell us that we, at LSI Computer Systems, are *very* easy to work with. We, of course, have no standard of comparison, but those who have, tell us that engineers at big LSI manufacturers are relatively inaccessible. We'd like to be big some day, too, but accessible is one thing we'll always be. It's one of the things that made us as big as we are.

What about development (NRE) costs?

They are, of course, a big part of *any* custom job. The important thing to look for here is a company that is custom oriented – and also one that doesn't have a huge overhead to support in the form of production facilities.



Now, if your circuit has an equivalent gate count of 1,000, one of those big outfits is going to quote you at least $100,000 for the NRE. We can design it for less than half of that, and what's more, we can deliver prototypes in less than 26 weeks, and produce your chip for less than a dollar apiece.

How fast can they turn around?

Another advantage of being relatively small is that you can get a chip out and into production fast. Again, customers who've had experience with bigger LSI manufacturers tell us we're more flexible, and move faster. If your chip has an equivalent gate count of much more than the 1,000 we mentioned above, it would be difficult to pin a definite design time on. But one thing we will say: when we give you a date, you can count on it.

Are they going to try out a glamorous new MOS process on you?

Being at the forefront of technology is exciting, but if you're counting on a chip for a product you've got a lot of money riding on, it can also be injurious to your health. That's why we stick to the stodgy, safe, tried and true techniques. And after all: even the stodgiest, safest MOS/LSI technology is pretty close to the forefront.

Can they take peaks?

This brings us to a very vital subject: in-house wafer processing versus subcontracting.

Naturally, LSI manufacturers that have their own production facilities will give you their side, but here's ours: if anything happens to *their* process line, where are *you*? If they can't process they can't deliver, but there's something else, too: no matter how big they are, they have limits, and if you're gearing up for, say, a big Christmas production run, they may have trouble keeping up with you.

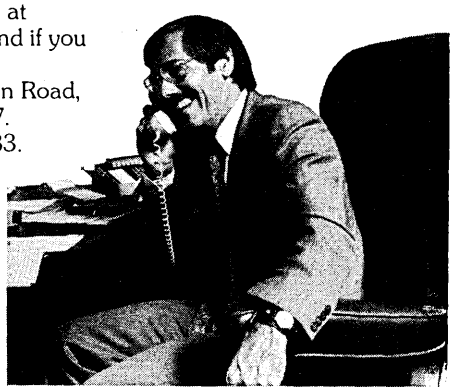
When you subcontract, as we do, if something happens to wafer foundry A, you switch to B. And we can keep up with any peak demand you may make, by just adding foundries.

Do they use conservative design rules?

Speaking of going from foundry to foundry, you can only do that if you use design rules conservative enough to be successfully processed at any foundry. Right here we have to say that our rules may make your chip a shade bigger, and hence cost a little more, but in terms of count-on-able delivery in any quantity, on time (and also, incidentally, in terms of reliability) we think it's well worth it.

There are other points worth considering, but these will do for a start. The man who can tell you about the others (and expand on these), is Ron Colino, our VP/Marketing.

You can reach him at (516) 271-0400, and if you want to write, it's 1235 Walt Whitman Road, Melville, NY 11747. TWX 510-226-7833.



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Since 1969
Manufacturers of Custom and Standard LSI circuits.

LSI Computer Systems

CUSTOM/SEMICUSTOM

For Standard LSI Circuits, see Volume I, Page 696.

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SUNNYVALE, CALIFORNIA, USA
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LINEAR SERIES (20-75V)

- 20V for normal use: A20A, A20B, A20C, A20E, A20F, A20G, A20H, A20J, A20L, A20M
  - up to 812 components on chip
- 20V for higher performance: A20AS, A20BS, A20CS, A20ES, A20FS, A20GS, A20HS, A20JS, A20LS, A20MS, A20WS
  - up to 812 components on chip
- 40V for normal use: A40D
  - 194 components on chip
- 40V for higher performance: A40AS, A40BS, A40DS
  - 245 components on chip
- 75V for normal use: A75X
  - 230 components on chip
- 75V for higher performance: A75XS
  - 230 components on chip

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- D15A, D15B, AD15C, D15D
  - up to 864 gates and additional interface components on chip

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  - up to 600 gates on chip
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  - up to 600 gates on chip

IC LICENSING AND SELF-DESIGN

- MCE offers extensive training programs in IC design
- All of MCE's tools are ready for licensing and in-house use by our customers, e.g., software for design, logic or circuit simulation, layout, and test verification
- Design tools including breadboarding system (UniDES™) and a wide range of kit parts
- Cell libraries for bipolar (analog and digital), CMOS metal gate (analog and digital) and CMOS Signate

MCE'S FOUNDRY SERVICES

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- Computer-monitored, 4" positive resist wafer fab
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- All types of plastic and ceramic packages
- Includes dual-in-line, flat packs, chip carriers, high-power packages, etc.

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- Laser trim option
- High temperature tolerance for operation above 200°C
- Radiation-tolerant
- Extensive component and functional cell library for UniCell™ custom available
- Supported by full computer-aided design simulation to assure circuit performance on first pass
- SNAP™ software for exact and easy layout
- Fast turnaround on prototypes

MCE'S FAMILY OF ADVANCED BIPOLAR ARRAYS (UNIRAY™) AND CELL CUSTOM (UNICELL™)

- Power/small signal Unirays™ and UniCells™ up to 80V or 15A on a single chip
- Proven wide range of advanced technologies from modern 4" computer-monitored wafer fab
- Higher performance at smaller chip sizes (and cost)
- Linear with BiFET, SiChrome thin-film resistors and implanted resistors, fuses, zener zap switches and various kinds of capacitors
- Laser trim option
- UniCell™ custom with extensive cell library with about 300 proven functions and components for easy design and layout
- Linear function block cell approach (UniCell™) allows easy PC board design on silicon
- Efficient digital functions available
- UniCell™ custom ICs with less than 3 months to prototypes
- Up to 1320 components on analog-digital arrays
- 300 components on power arrays combined with 14A output current
- Uniray™ turnaround less than 6 weeks
- Customized packages available
- SNAP™ software for exact and easy layout

MCE'S ADVANCED CMOS UNIRAYS™ AND UNICELLS

MCE'S FAMILY OF SILICON GATE OXIDE ISOLATED INTEGRATED CIRCUITS

- 336 to 2014 gate arrays in 4μ technology - single layer metal with maximum 4nsec delay
- Up to 5000 gate arrays in 3μ technology - dual layer metal with maximum 2nsec delay
- Extensive cell library with over 200 functions for Uniray™ and UniCell™ approach
- Full simulation practiced on all designs by use of MCE-developed software including auto-placement and auto-routing
- Logic test vectors and layout are included in the full simulation sequence
- Only fully tested parts supplied as prototypes
- Shortest turnaround with highest probability of first-time hit in the industry
- Full simulation practiced on all designs by use of MCE-developed software including auto-placement and auto-routing
- Software used to guarantee first-time hit
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- MCE 571..... 10-Bit A/D Converter
- MCE 574, MCE 574Z .... 12-Bit A/D Converter
- MCE 565A, MCE 566A, MCE 6012 ..... 12-Bit D/A Converter
- MCE VFC32..... V/F Converter

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- High-Speed Latching Comparator
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- MT 32003..... 512 Bit FI-FO Memory
- MT 34006..... Local Network Terminal Controller 5Mbit for μP
- MT 34009..... Arinc 429 Eight Channel Serial to Parallel Decoder
- MT 70003..... Arinc 429 Single Channel Serial to Parallel Decoder
- MT 70014..... Arinc 429 Dual Channel Parallel to Serial Decoder

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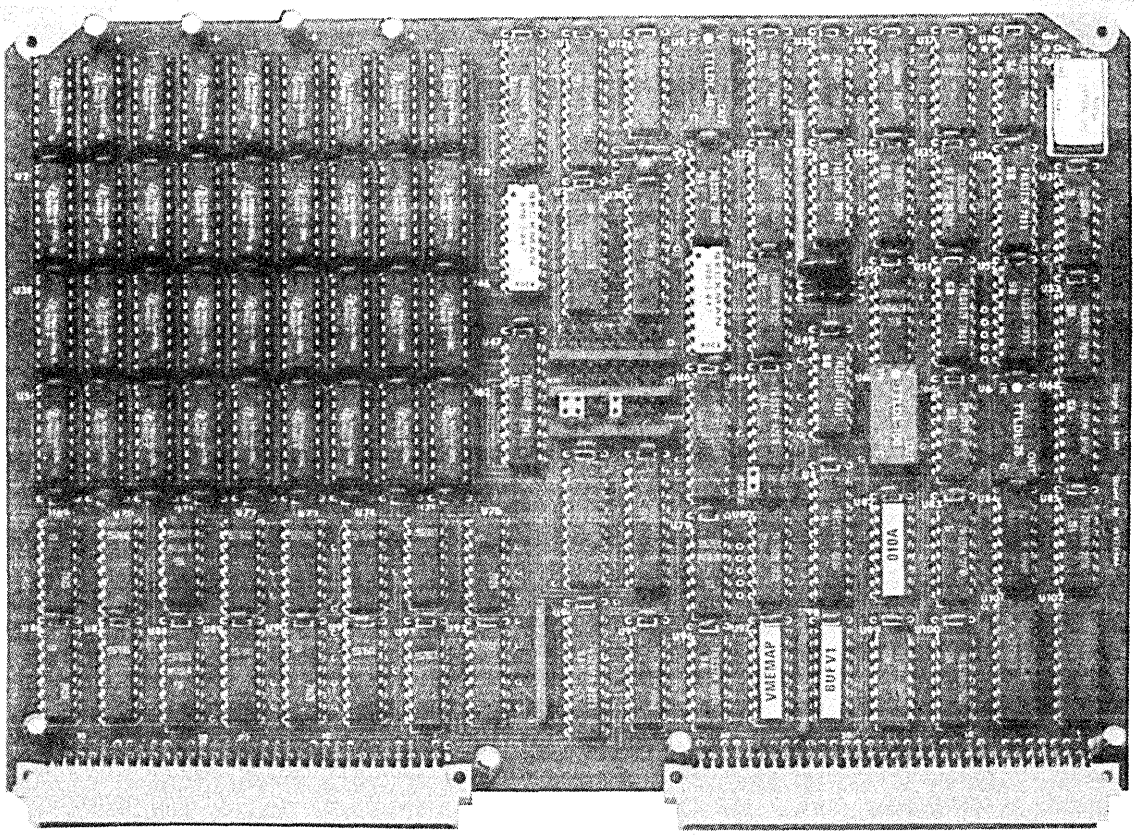
For Key Data On Every IC On This Board, The Place To Look Is...



This Signetics Memory Module provides 256K bytes of dynamic random access memory, plus parity protection.

Equipment and system design often require the use of a wide variety of integrated circuits in order to obtain optimum performance. One way for an engineer to be certain that he hasn't overlooked the best device for his application is to refer to the pages of IC MASTER.

Surveys conducted by IC MASTER, integrated circuit manufacturers, and independent research agencies confirm that four out of five IC MASTER users have specified one or more products as the result of using IC MASTER.

Device No.	Description
74LS00	Quadruple 2-Input NAND Gate
74LS08	Quadruple 2-Input AND Gate
74LS04	Hex Inverter
74LS20	Dual 4-Input NAND Gate
74LS32	Quadruple 2-Input OR Gate
74LS37	Quadruple 2-Input NAND Buffer
74LS24	Schmitt Trigger
74LS74	Dual D-Type Edge-Triggered Flip-Flop
74LS132	Quadruple 2-Input Schmitt Trigger
74LS112	Dual J-K Edge-Triggered Flip-Flop
74LS10	Triple-3-Input NAND Gate
74LS244	Octal Buffer/Line Driver
74LS645	Octal Bus Transceiver
AM25LS2521	8-Bit Equal-to Comparator
74S38	AND/NAND Gate
N7411	Triple-3-Input AND Gate
N74S40	Dual 4-Input NAND Buffer
TMS4164	64K Dynamic RAM
7641	512 x 8 PROM
7642	1K x 4 PROM

Representative list of ICs on Signetics SMVME3100 Memory Card. Key specifications for all of these ICs can be found in IC MASTER.

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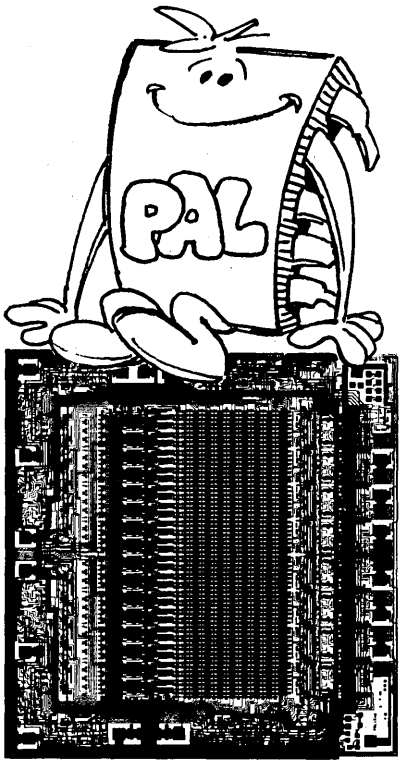

The PAL™ Concept

Monolithic Memories' family of PAL devices gives designers a powerful tool with unique capabilities for use in new and existing logic designs. The PAL saves time and money by solving many of the system partitioning and interface problems brought about by increases in semiconductor device technology.

Rapid advances in large scale integration technology have led to larger and larger standard logic functions; single I.C.s now perform functions that formerly required complete circuit cards. While LSI offers many advantages, advances have been made at the expense of device flexibility. Most LSI devices still require large numbers of SSI/MSI devices for interfacing with user systems. Designers are still forced to turn to random logic for many applications.

The designer is confronted with another problem when a low to medium complexity product is designed. Often the function is well defined and could derive significant benefits from fabrication as an integrated circuit. However, the design cycle for a custom circuit is long and the costs can be very high. This makes the risk significant enough to deter most users. The technology to support maximum flexibility combined with fast turn around on custom logic has simply not been available. Monolithic Memories offers the programmable solution.

The PAL family offers a fresh approach to using fuse programmable logic. PALs are a conceptually unified group of devices which combine programmable flexibility with high speed and an extensive selection of interface options. PALs can lower inventory, cut design cycles and provide high complexity with maximum flexibility. These features, combined with lower package count and high reliability, truly make the PAL a circuit designer's best friend.

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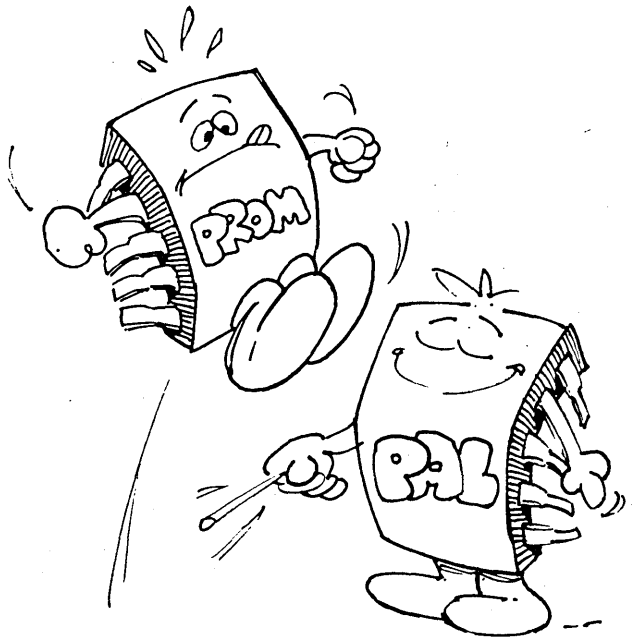
Monolithic Memories

The PAL—Teaching Old PROMs New Tricks



MMI developed the modern PROM and introduced many of the architectures and techniques now regarded as industry standards. As the world's largest PROM manufacturer, MMI has the proven technology and high volume production capability required to manufacture and support the PAL.

The PAL is an extension of the fusible link technology pioneered by Monolithic Memories for use in bi-polar PROMs. The fusible link PROM first gave the digital systems designer the power to "write on silicon." In a few seconds he was able to transform a blank PROM from a general purpose device into one containing a custom algorithm, microprogram, or Boolean transfer function. This opened up new horizons for the use of PROMs in computer control stores, character generators, data storage tables and many other applications. The wide acceptance of this technology is clearly demonstrated by today's multi-million dollar PROM market.

The key to the PROM's success is that it allows the designer to quickly and easily customize the chip to fit his unique requirements. The PAL extends this programmable flexibility by utilizing proven fusible link technology to implement logic functions. Using PALs the designer can quickly and effectively implement custom logic varying in complexity from random gates to complex arithmetic functions.

ANDs and ORs

The PAL implements the familiar sum of products logic by using a programmable AND array whose output terms feed a fixed OR array. Since the sum of products form can express any Boolean transfer function, the PAL's uses are only limited by the number of terms available in the AND - OR arrays. PAL's come in different sizes to allow for effective logic optimization.

Figure 1 shows the basic PAL structure for a two input, one output logic segment. The general logic equation for this segment is

$$\text{Output} = (I_1+\overline{f_1})(\overline{I_1}+\overline{f_2})(I_2+\overline{f_3})(\overline{I_2}+\overline{f_4}) + (I_1+\overline{f_5})(\overline{I_1}+\overline{f_6})(I_2+\overline{f_7})\ (\overline{I_2}+\overline{f_8})$$

where the "f" terms represent the state of the fusible links in the PAL's AND array. An unblown link represents a logic 1. Thus,

fuse blown, f = 0

fuse intact, f = 1

An unprogrammed PAL has all fuses intact.

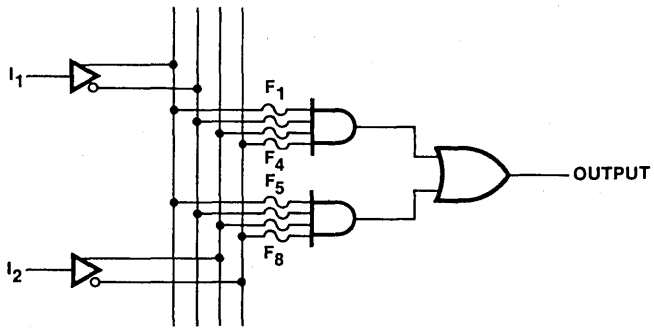


Figure 1

PAL Notation

Logic equations, while convenient for small functions, rapidly become cumbersome in large systems. To reduce possible confusion, complex logic networks are generally defined by logic diagrams and truth tables. Figure 2 shows the logic convention adopted to keep PAL logic easy to understand and use. In the figure, an "x" represents an intact fuse used to perform the logic AND function. (Note: the input terms on the common line with the x's are not connected together.) The logic symbology shown in Figure 2 has been informally adopted by integrated circuit manufacturers because it clearly establishes a one-to-one correspondence between the chip layout and the logic diagram. It also allows the logic diagram and truth table to be combined into a compact and easy to read form, thereby serving as a convenient shorthand for PALs. The two input - one output example from Figure 1 redrawn using the new logic convention is shown in Figure 3.

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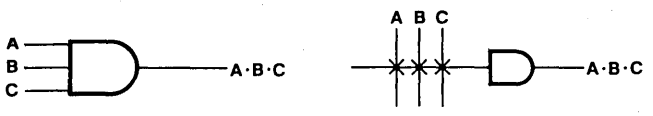


Figure 2

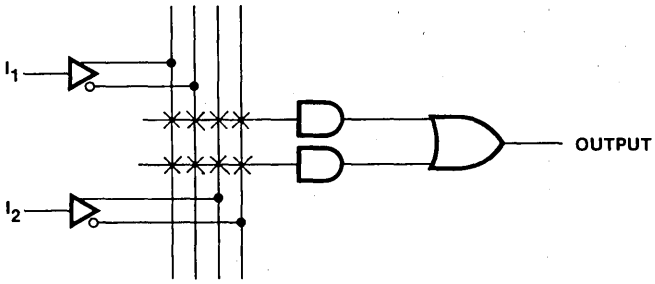


Figure 3

As a simple PAL example, consider the implementation of the transfer function:

$$\text{Output} = I_1\overline{I_2} + \overline{I_1}I_2$$

The normal combinatorial logic diagram for this function is shown in figure 4, with the PAL logic equivalent shown in figure 5.

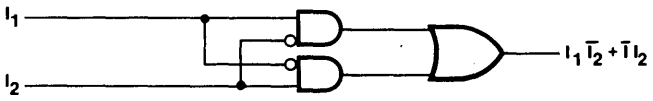


Figure 4

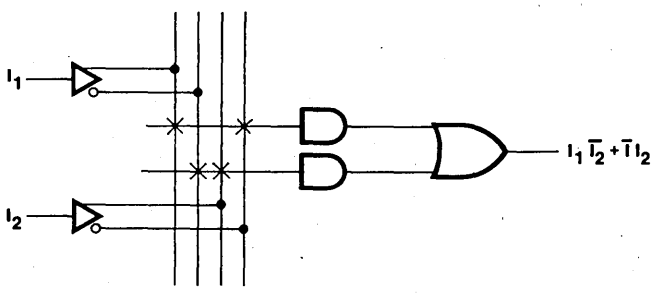


Figure 5

Using this logic convention it is now possible to compare the PAL structure to the structure of the more familiar PROM and PLA. The basic logic structure of a PROM consists of a fixed AND array whose outputs feed a programmable OR array (figure 6). PROMs are low-cost, easy to program, and available in a variety of sizes and organizations. They are most commonly used to store computer programs and data. In these applications the fixed input is a computer memory address; the output is the contents of that memory location.

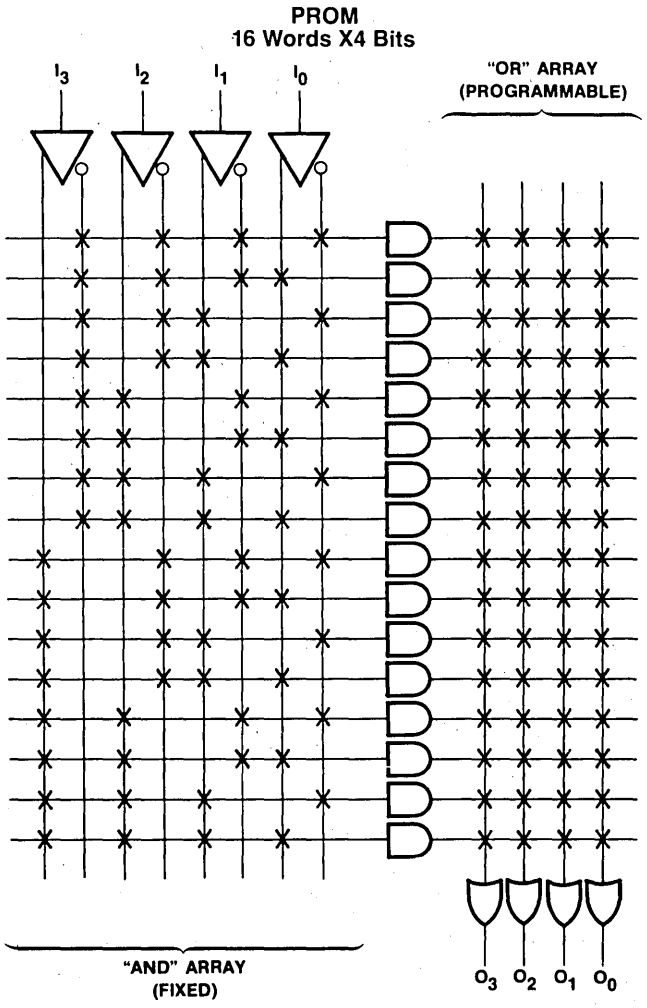


Figure 6

The basic logic structure of the PLA consists of a programmable AND array whose outputs feed a programmable OR array (Figure 7). Since the designer has complete control over all inputs and outputs, the PLA provides the ultimate flexibility for implementing logic functions. They are used in a wide variety of applications. However, this generality makes PLA's expensive, quite formidable to understand, and are costly to program (they require special programmers).

The basic logic structure of the PAL, as mentioned earlier, consists of a programmable AND array whose outputs feed a fixed OR array (Figure 8). The PAL combines much of the flexibility of the PLA with the low cost and easy programmability of the PROM. Table 1 summarizes the characteristics of the PROM, PLA, and PAL logic families.

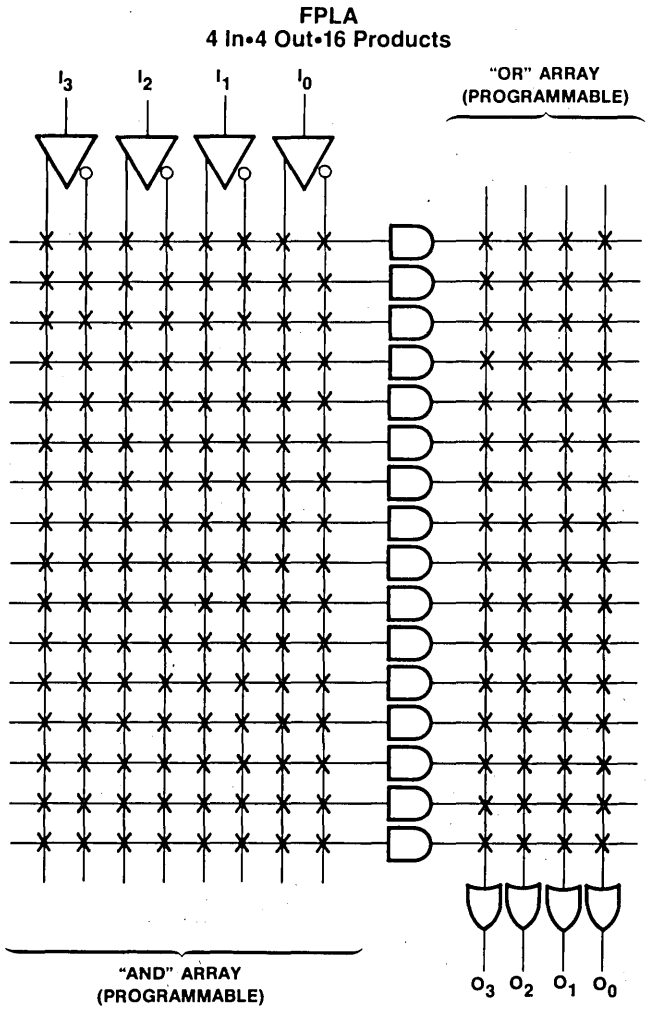


Figure 7

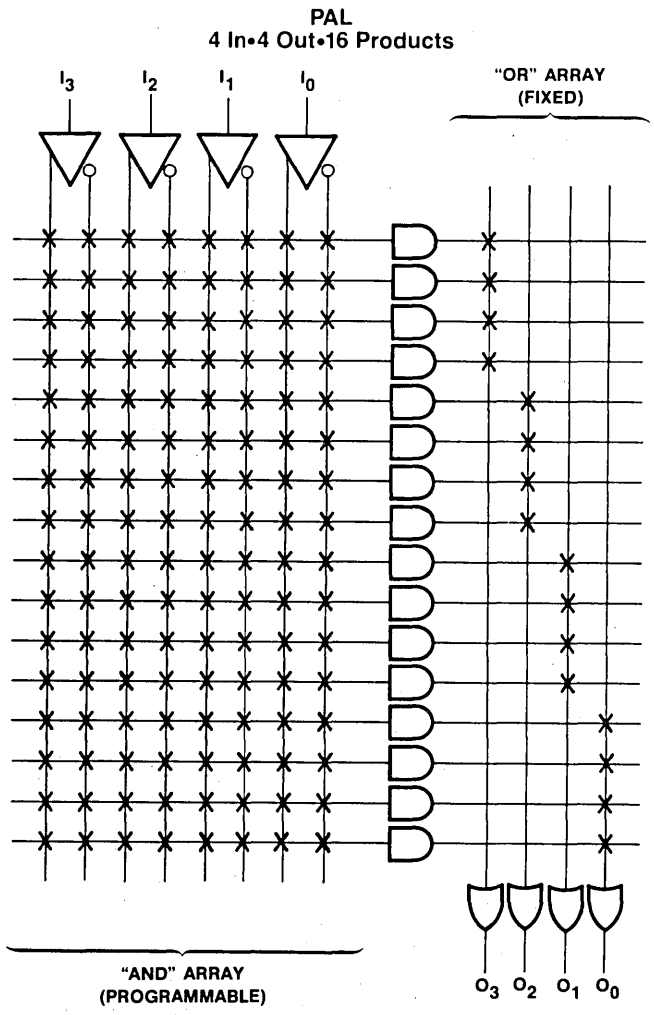


Figure 8

	AND	OR	OUTPUT OPTIONS
PROM	Fixed	Prog	TS, OC
FPLA	Prog	Prog	TS, OC, Fusible Polarity
FPGA	Prog	None	TS, OC, Fusible Polarity
FPLS	Prog	Prog	TS, Registered Feedback, I/O
PAL	Prog	Fixed	TS, Registered, Feedback, I/O

Table 1

PAL Input/Output/Function Chart

PART NUMBER	INPUT	OUTPUT	PROGRAMMABLE I/O'S	FEEDBACK REGISTER	OUTPUT POLARITY	FUNCTIONS	T_{PD} ns, TYP	I_{OL} mA	I_{CC} mA, TYP
PAL10H8	10	8			AND-OR	AND-OR Gate Array	25	8	55
PAL12H6	12	6			AND-OR	AND-OR Gate Array	25	8	55
PAL14H4	14	4			AND-OR	AND-OR Gate Array	25	8	55
PAL16H2	16	2			AND-OR	AND-OR Gate Array	25	8	55
PAL16C1	16	2			BOTH	AND-OR Gate Array	25	8	55
PAL20C1	20	2			BOTH	AND-OR Gate Array	25	8	60
PAL10L8	10	8			AND-NOR	AND-OR Invert Gate Array	25	8	55
PAL12L6	12	6			AND-NOR	AND-OR Invert Gate Array	25	8	55
PAL14L4	14	4			AND-NOR	AND-OR Invert Gate Array	25	8	55
PAL16L2	16	2			AND-NOR	AND-OR Invert Gate Array	25	8	55
PAL12L10	12	10			AND-NOR	AND-OR Invert Gate Array	25	8	60
PAL14L8	14	8			AND-NOR	AND-OR Invert Gate Array	25	8	60
PAL16L6	16	6			AND-NOR	AND-OR Invert Gate Array	25	8	60
PAL18L4	18	4			AND-NOR	AND-OR Invert Gate Array	25	8	60
PAL20L2	20	2			AND-NOR	AND-OR Invert Gate Array	25	8	60
PAL16L8	10	2	6		AND-NOR	AND-OR Invert Gate Array	25	24	120
PAL20L10	12	2	8		AND-NOR	AND-OR Invert Gate Array	35	24	90
PAL16R8	8	8		8	AND-NOR	AND-OR Invert Array w/Reg's	25	24	120
PAL16R6	8	6	2	6	AND-NOR	AND-OR Invert Array w/Reg's	25	24	120
PAL16R4	8	4	4	4	AND-NOR	AND-OR Invert Array w/Reg's	25	24	120
PAL20X10	10	10		10	AND-NOR	AND-OR-XOR Invert w/Reg's	35	24	120
PAL20X8	10	8	2	8	AND-NOR	AND-OR-XOR Invert w/Reg's	35	24	120
PAL20X4	10	4	6	4	AND-NOR	AND-OR-XOR Invert w/Reg's	35	24	120
PAL16X4	8	4	4	4	AND-NOR	AND-OR-XOR Invert w/Reg's	25	24	160
PAL16A4	8	4	4	4	AND-NOR	AND-CARRY-OR-XOR Invert w/Reg's	25	24	170

[1]Simultaneous AND-OR and AND-NOR outputs

Table 2

PALs For Every Task

The members of the PAL family and their characteristics are summarized in Table 2. They are designed to cover the spectrum of logic functions at reduced cost and lower package count. This allows the designer to select the PAL that best fits his application. PALs come in the following basic configurations:

Gate Arrays

PAL gate arrays are available in sizes from 12x10 (12 input terms, 10 output terms) to 20x2, with both active high and active low output configurations available. This wide variety of input/output formats allows the PAL to replace many different sized blocks of combinatorial logic with single packages.

Programmable I/O

A feature of the high-end members of the PAL family is programmable input/output. This allows the product terms to directly control the outputs of the PAL (Figure 9). One product term is used to enable the three-state buffer, which in turn gates the summation term to the output pin. The output is also fed back into the PAL array as an input. Thus the PAL drives the I/O pin when the three-state gate is enabled; the I/O pin is an input to the PAL array when the three-state gate is disabled. This feature can be used to allocate available pins for I/O functions or to provide bi-directional output pins for operations such as shifting and rotating serial data.

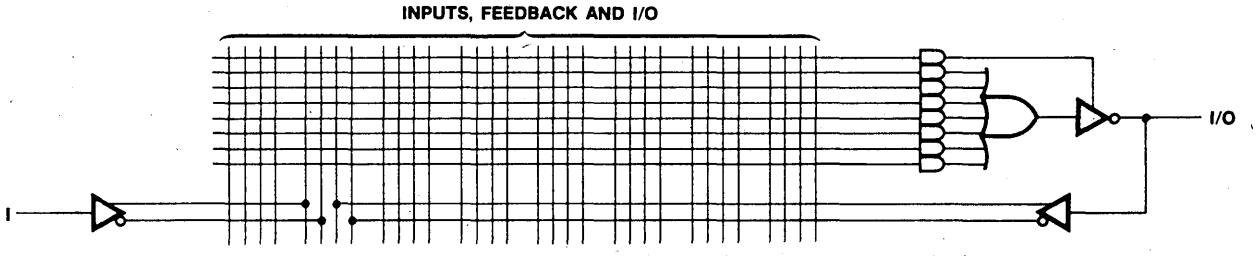


Figure 9

Registered Outputs with Feedback

Another feature of the high end members of the PAL family is registered data outputs with register feedback. Each product term is stored into a D-type output flip-flop on the rising edge of the system clock (Figure 10).The Q output of the flip-flop can then be gated to the output pin by enabling the active low three-state buffer.

In addition to being available for transmission, the Q output is fed back into the PAL array as an input term. This feedback allows the PAL to "remember" the previous state, and it can alter its function based upon that state. This allows the designer to configure the PAL as a state sequencer which can be programmed to execute such elementary functions as count up, count down, skip, shift, and branch. These functions can be executed by the registered PAL at rates of up to 20 MHz.

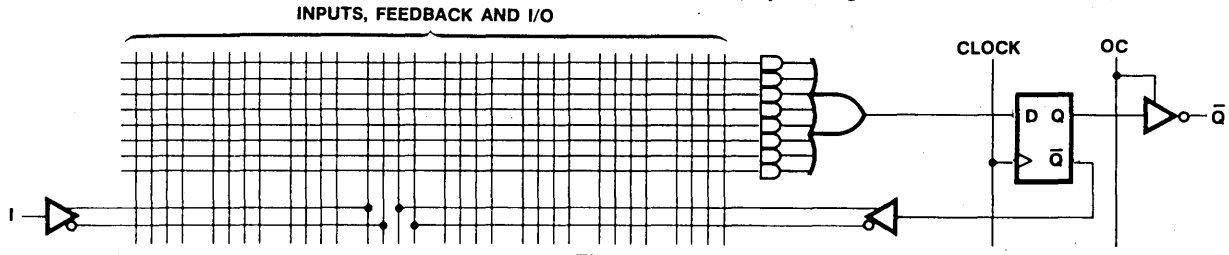


Figure 10

XOR PALs

These PALs feature an exclusive OR function. The sum of products is segmented into two sums which are then exclusive ORed (XOR) at the input of the D-type flip-flop. All of the features of the Registered PALs are included in the XOR PALs. The XOR function provides an easy implementation of the HOLD operation used in counters.

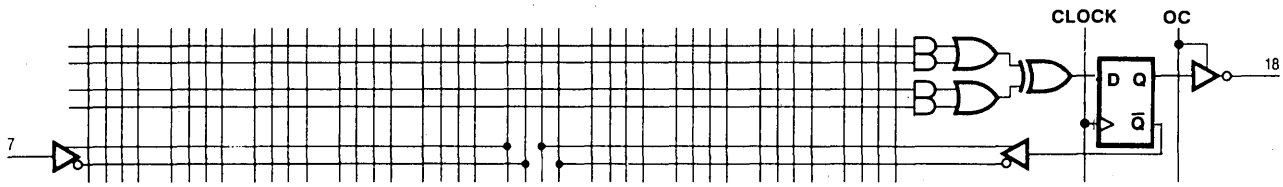


Figure 11

Arithmetic Gated Feedback

The arithmetic functions add, subtract, greater than, and less than are implemented by addition of gated feedback to the features of the XOR PALs. The XOR at the input of the D-type flip-flop allows carrys from previous operations to be XORed with two variable sums generated by the PAL array. The flip-flop Q output is fed back to be gated with input terms I. This gated feedback provides any one of the 16 possible Boolean combinations which are mapped in the Karnaugh map (figure 14). Figure 13 shows how the PAL array can be programmed to perform these 16 operations. These features provide for versatile operations on two variables and facilitate the parallel generation of carrys necessary for fast arithmetic operations.

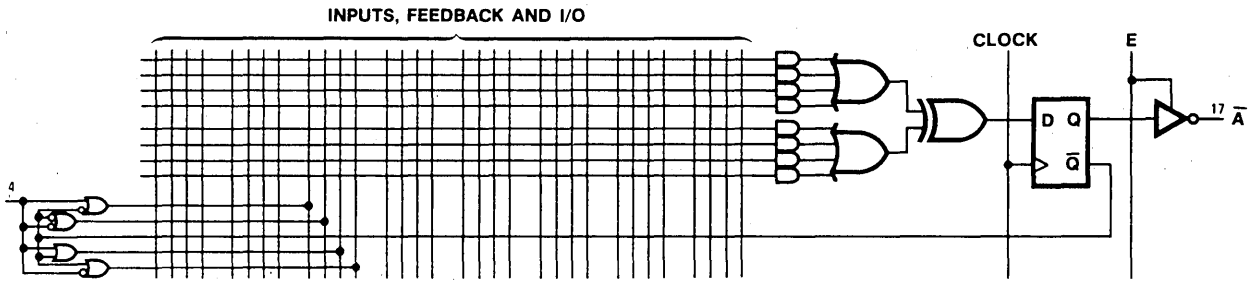


Figure 12

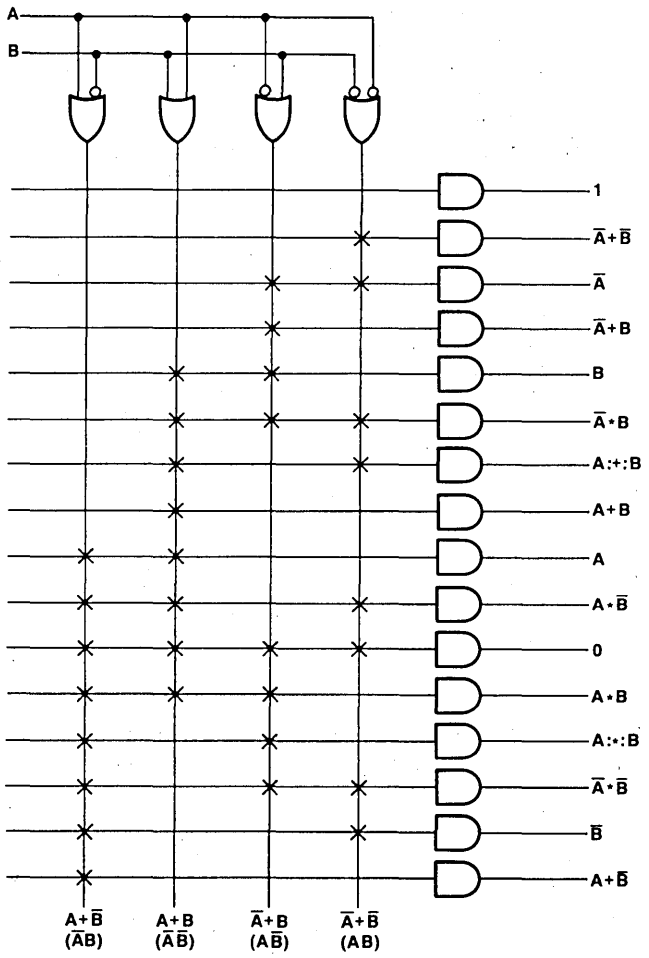


Figure 13

$(\overline{A}+B),(\overline{A}+\overline{B})$ / $(A+\overline{B}),(A+B)$	--	-x	xx	x-
--	1	$\overline{A}+\overline{B}$	$\overline{A}$	$\overline{A}+B$
-x	A+B	A:+:B	$\overline{A}*B$	B
xx	A	$A*\overline{B}$	0	A * B
x-	$A+\overline{B}$	$\overline{B}$	$\overline{A}*\overline{B}$	A:*:B

Figure 14

It should now be clear that the PAL family can replace most Small-Scale Integrated Logic (SSI) logic in use today, thereby lowering product cost and giving the designer even greater flexibility in implementing logic functions.

PAL Programming

PALs can be programmed in most standard PROM programmers with the addition of a PAL personality card. The PAL appears to the programmer as a PROM. During programming half of the PAL outputs are selected for programming while the other outputs and the inputs are used for addressing. The outputs are then switched to program the other locations. Verification uses the same procedure with the programming lines held in a low state.

PAL Technology

PALs are manufactured using the proven TTL Schottky bipolar Ti-W fuse process used to make fusible-link PROMs. An NPN emitter follower array forms the programmable AND array. PNP inputs provide high-impedance inputs (0.25 mA max) to the array. All outputs are standard TTL drivers with internal active pull-up transistors. Typical PAL propagation delay time is 25 ns, and all PALs are packaged in space saving 20-pin and 24-pin SKINNYDIP™.

PAL Data Security

The circuitry used for programming and logic verification can be used at any time to determine the logic pattern stored in the PAL array. For security, the PAL has a "last fuse" which can be blown to disable the verification logic. This provides a significant deterrent to potential copiers, and it can be used to effectively protect proprietary designs.

Programmable Array Logic Family

PAL® Series 20

U.S. Patent 4124899

March 1981

Features/Benefits

- **Programmable replacement for conventional TTL logic.**
- **Reduces IC inventories substantially and simplifies their control.**
- **Reduces chip count by 4 to 1.**
- **Expedites and simplifies prototyping and board layout.**
- **Saves space with 20-pin SKINNY DIP® packages.**
- **High speed: 25ns typical propagation delay.**
- **Programmed on standard PROM programmers.**
- **Programmable three-state outputs.**
- **Special feature reduces possibility of copying by competitors.**

Description

The PAL family utilizes an advanced Schottky TTL process and the Bipolar PROM fusible link technology to provide user programmable logic for replacing conventional SSI/MSI gates and flip-flops at reduced chip count.

The family lets the systems engineer "design his own chip" by blowing fusible links to configure AND and OR gates to perform his desired logic function. Complex interconnections which previously required time-consuming layout are thus "lifted" from PC board etch and placed on silicon where they can be easily modified during prototype check-out or production.

The PAL transfer function is the familiar sum of products. Like the PROM, the PAL has a single array of fusible links. Unlike the PROM, the PAL is a programmable AND array driving a fixed OR array (the PROM is a fixed AND array driving a programmable OR array). In addition the PAL provides these options:

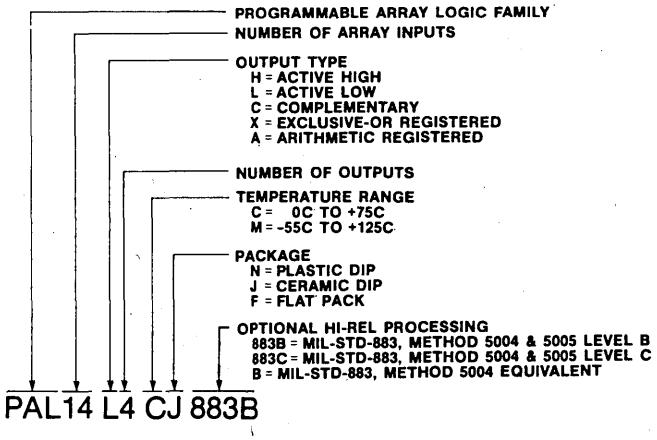
- Variable input/output pin ratio
- Programmable three-state outputs
- Registers with feedback
- Arithmetic capability

PART NUMBER	PKG	DESCRIPTION
PAL10H8	N,J,F	Octal 10 Input And-Or Gate Array
PAL12H6	N,J,F	Hex 12 Input And-Or Gate Array
PAL14H4	N,J,F	Quad 14 Input And-Or Gate Array
PAL16H2	N,J,F	Dual 16 Input And-Or Gate Array
PAL16C1	N,J,F	16 Input And-Or/And-Or-Invert Gate Array
PAL10L8	N,J,F	Octal 10 Input And-Or-Invert Gate Array
PAL12L6	N,J,F	Hex 12 Input And-Or-Invert Gate Array
PAL14L4	N,J,F	Quad 14 Input And-Or-Invert Gate Array
PAL16L2	N,J,F	Dual 16 Input And-Or-Invert Gate Array
PAL16L8	N,J,F	Octal 16 Input And-Or-Invert Gate Array
PAL16R8	N,J,F	Octal 16 Input Registered And-Or Gate Array
PAL16R6	N,J,F	Hex 16 Input Registered And-Or Gate Array
PAL16R4	N,J,F	Quad 16 Input Registered And-Or Gate Array
PAL16X4	N,J	Quad 16 Input Registered And-Or-Xor Gate Array
PAL16A4	N,J	Quad 16 Input Registered And-Carry-Or-Xor Gate

Unused inputs are tied directly to V_{CC} or GND. Product terms with all fuses blown assume the logical high state, and product terms connected to both true and complement of any single input assume the logical low state. Registers consist of D type flip-flops which are loaded on the low to high transition of the clock. PAL Logic Diagrams are shown with all fuses blown, enabling the designer use of the diagrams as coding sheets.

The entire PAL family is programmed on inexpensive conventional PROM programmers with appropriate personality and socket adapter cards. Once the PAL is programmed and verified, two additional fuses may be blown to defeat verification. This feature gives the user a proprietary circuit which is very difficult to copy.

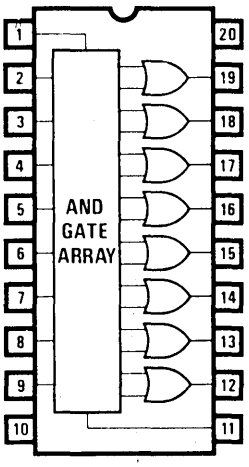
Ordering Information



PAL® is a registered trademark of Monolithic Memories

1165 East Arques Avenue, Sunnyvale, CA 94086 Tel: (408) 739-3535 TWX: 910-339-9229

PAL10H8



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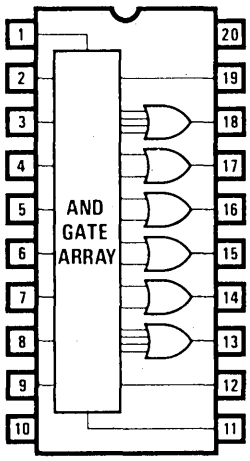

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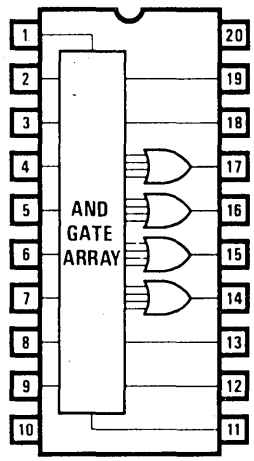

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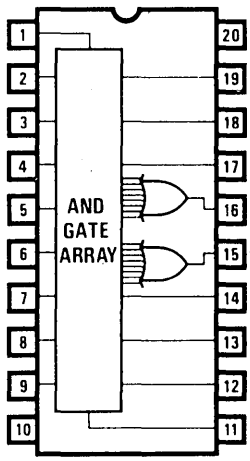
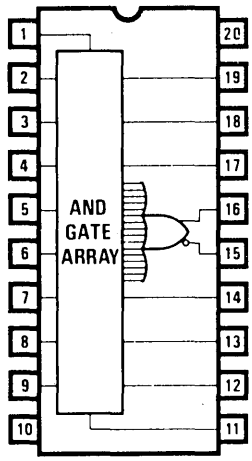


PAL16C1



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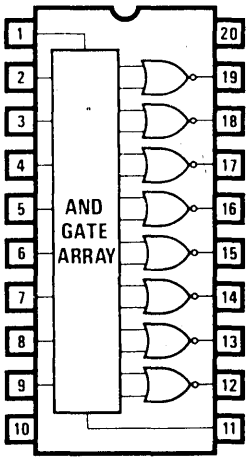

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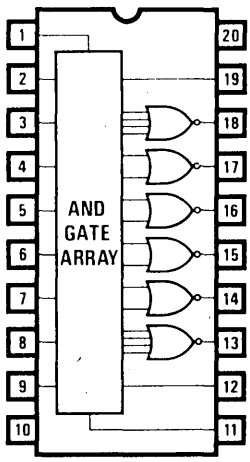

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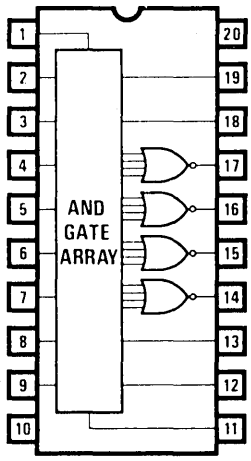

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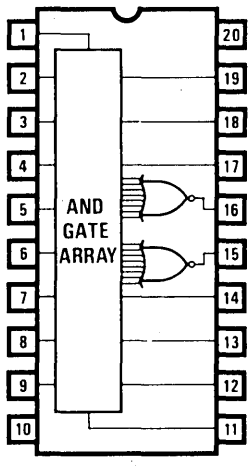
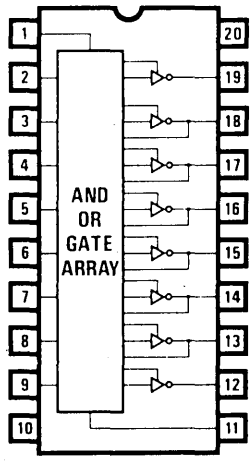
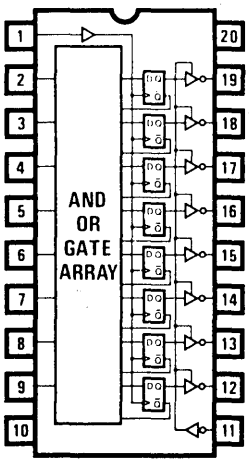


PAL16L8



PAL16R8



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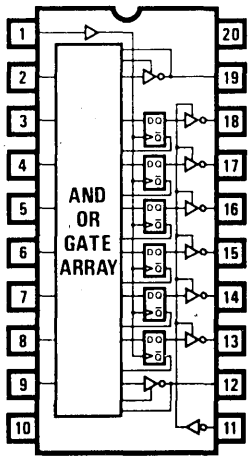

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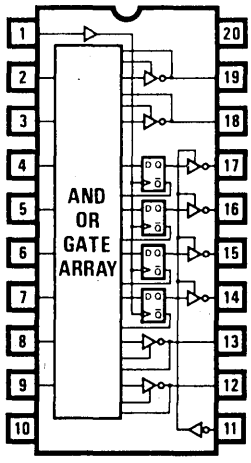

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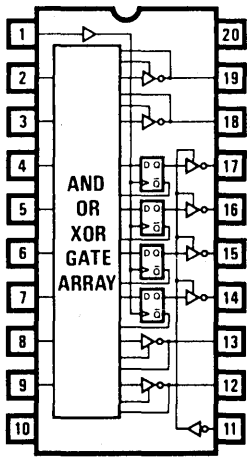

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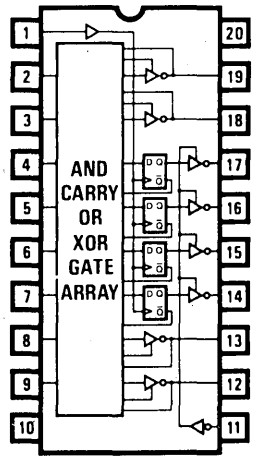

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Absolute Maximum Ratings

	Operating
Supply Voltage, V_{CC}	7
Input Voltage	5.5V
Off-state output Voltage	5.5V
Storage temperature	–65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	25	10		25	10		ns
		High	25	10		25	10		
t_{su}	Set up time from input or feedback	16R8 16R6 16R4	45	25		35	25		ns
		16X4 16A4	55	30		45	30		
t_h	Hold time		0	–15		0	–15		ns
T_A	Operating free-air temperature		–55			0	5	75	°C
T_C	Operating case temperature				125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN		I_I = –18mA		–0.8	–1.5	V
I_{IL}	Low-level input current †	V_{CC} = MAX		V_I = 0.4V		–0.02	–0.25	mA
I_{IH}	High-level input current †	V_{CC} = MAX		V_I = 2.4V			25	μA
I_I	Maximum input current	V_{CC} = MAX		V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	10H8, 12H6, 14H4, 16H2, 16C1, 10L8, 12L6, 14L4, 16L2	MIL COM I_{OL} = 8mA		0.3	0.5	V
			16L8 16R8 16R6 16R4 16X4 16A4	MIL I_{OL} = 12mA				
				COM I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL	I_{OH} = –2mA	2.4	2.8		V
			COM	I_{OH} = –3.2mA				
I_{OZL}	Off-state output current †	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V	16L8 16R8 16R6 16R4	V_O = 0.4V			–100	μA
I_{OZH}			16X4 16A4	V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current**	V_{CC} = 5V		V_O = 0V	–30	–70	–130	mA
I_{CC}	Supply current	V_{CC} = MAX	10H8, 12H6, 14H4, 16H2, 16C1 10L8, 12L6, 14L4, 16L2			55	90	mA
			16R4, 16R6, 16R8, 16L8			120	180	
			16X4			160	225	
			16A4			170	240	

† I/O pin leakage is the worst case of I_{OZX} or I_{IX} e.g., I_{IL} and I_{OZH}

†† All typical values are at V_{CC} = 5V, T_A = 25°C.

* These are absolute voltages with respect to pin 10 on the device and includes all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

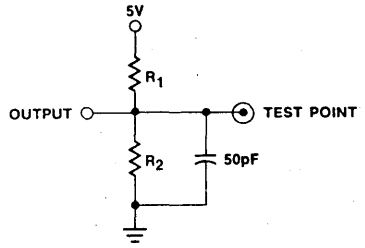
** Only one output shorted at a time.

Switching Characteristics

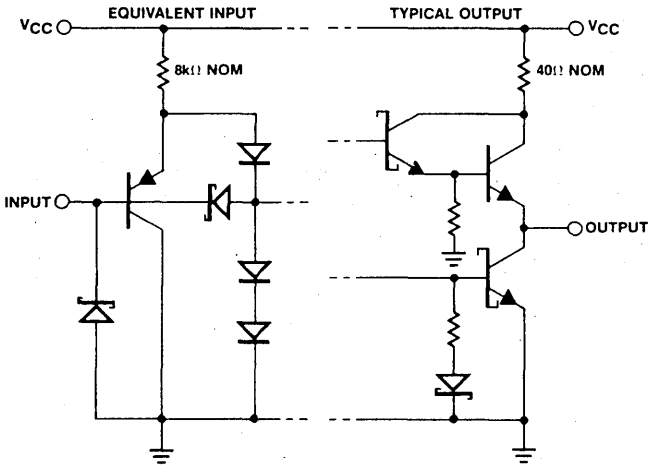
Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input to output	10H8 12H6 14H4 16H2 10L8 12L6 14L4 16L2	R_1 = 560Ω R_2 = 1.1kΩ		25	45		25	35	ns
		16C1			25	45		25	40	
t_{PD}	Input or feedback to output	16R6 16R4 16L8	R_1 = 200Ω R_2 = 390Ω		25	45		25	35	ns
		16X4 16A4			30	45		30	40	
t_{CLK}	Clock to output or feedback				15	25		15	25	ns
t_{PZY}	Pin 11 to output enable				15	25		15	25	ns
t_{PXZ}	Pin 11 to output disable				15	25		15	25	ns
t_{PZX}	Input to output enable	16R6 16R4 16L8			25	45		25	35	ns
		16X4 16A4			30	45		30	40	
t_{PXZ}	Input to output disable	16R6 16R4 16L8			25	45		25	35	ns
		16X4 16A4			30	45		30	40	
f_{MAX}	Maximum frequency	16R8 16R6 16R4		14	25		16	25		MHz
		16X4 16A4		12	22		14	22		

Test Load



Schematic of Inputs and Outputs



Available Programmers

MANUFACTURER	PERSONALITY CARD SET	SOCKET ADAPTER CONFIGURATION
Data I/O Corporation	909-1427	715 1428-1 715 1428-2 715 1428-3
Pro-Log Corporation	PM9068	
Stag Systems	PM202	AM10H8 AM10L8 AM12H6 AM12L6 AM14H4 AM14L4 AM16H2 AM16L2 AM16C1
Structured Design	SD20/24	

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Monolithic Memories

Programming

PAL fuses are programmed using a low-voltage linear-select procedure which is common to all 15 PAL types. The array is divided into two groups, products 0 thru 31 and products 32 thru 63, for which pin identifications are shown in Pin Configurations below. To program a particular fuse, both an input line and a product line are selected according to the following procedure:

Step 1 Raise Output Disable, OD, to V_{IHH}

Step 2 Select an input line by specifying I_0, I_1, I_2, I_3, I_4, I_5, I_6, I_7 and L/R as shown in Table 1.

Step 3 Select a product line by specifying A_0, A_1 and A_2 one-of-eight select as shown in Table 2.

Step 4 Raise V_{CC} (pin 20) to V_{IHH}

Step 5 Program the fuse by pulsing the output pins, O, of the selected product group to V_{IHH} as shown in Programming Waveform.

Step 6 Lower V_{CC} (pin 20) to 6.0 V

Step 7 Pulse the CLOCK pin and verify the output pin, O, to be Low for active Low PAL types or High for active High PAL types.

Step 8 Lower V_{CC} (pin 20) to 4.5 V and repeat step 7.

Step 9 Should the output not verify, repeat steps 1 thru 8 up to five (5) times.

This procedure is repeated for all fuses to be blown (see Programming Waveforms).

To prevent further verification, two last fuses may be blown by raising pin 1 and pin 11 to V_P. V_{CC} is not required during this operation.

Voltage Legend

L = Low-level input voltage, V_{IL}
H = High-level input voltage, V_{IH}
HH = High-level program voltage, V_{IHH}
Z = High impedance (e.g., 10kΩ to 5.0V)

INPUT LINE NUMBER	PIN IDENTIFICATION								
	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	L/R
0	HH	HH	HH	HH	HH	HH	HH	L	Z
1	HH	HH	HH	HH	HH	HH	HH	H	Z
2	HH	HH	HH	HH	HH	HH	HH	L	HH
3	HH	HH	HH	HH	HH	HH	HH	H	HH
4	HH	HH	HH	HH	HH	HH	L	HH	Z
5	HH	HH	HH	HH	HH	HH	H	HH	Z
6	HH	HH	HH	HH	HH	HH	L	HH	HH
7	HH	HH	HH	HH	HH	HH	H	HH	HH
8	HH	HH	HH	HH	HH	L	HH	HH	Z
9	HH	HH	HH	HH	HH	H	HH	HH	Z
10	HH	HH	HH	HH	HH	L	HH	HH	HH
11	HH	HH	HH	HH	HH	H	HH	HH	HH
12	HH	HH	HH	HH	L	HH	HH	HH	Z
13	HH	HH	HH	HH	H	HH	HH	HH	Z
14	HH	HH	HH	HH	L	HH	HH	HH	HH
15	HH	HH	HH	HH	H	HH	HH	HH	HH
16	HH	HH	HH	L	HH	HH	HH	HH	Z
17	HH	HH	HH	H	HH	HH	HH	HH	Z
18	HH	HH	HH	L	HH	HH	HH	HH	HH
19	HH	HH	HH	H	HH	HH	HH	HH	HH
20	HH	HH	L	HH	HH	HH	HH	HH	Z
21	HH	HH	H	HH	HH	HH	HH	HH	Z
22	HH	HH	L	HH	HH	HH	HH	HH	HH
23	HH	HH	H	HH	HH	HH	HH	HH	HH
24	HH	L	HH	HH	HH	HH	HH	HH	Z
25	HH	H	HH	HH	HH	HH	HH	HH	Z
26	HH	L	HH	HH	HH	HH	HH	HH	HH
27	HH	H	HH	HH	HH	HH	HH	HH	HH
28	L	HH	HH	HH	HH	HH	HH	HH	Z
29	H	HH	HH	HH	HH	HH	HH	HH	Z
30	L	HH	HH	HH	HH	HH	HH	HH	HH
31	H	HH	HH	HH	HH	HH	HH	HH	HH

Table 1 Input Line Select

PRODUCT LINE NUMBER	PIN IDENTIFICATION						
	O_3	O_2	O_1	O_0	A_2	A_1	A_0
0, 32	Z	Z	Z	HH	Z	Z	Z
1, 33	Z	Z	Z	HH	Z	Z	HH
2, 34	Z	Z	Z	HH	Z	HH	Z
3, 35	Z	Z	Z	HH	Z	HH	HH
4, 36	Z	Z	Z	HH	HH	Z	Z
5, 37	Z	Z	Z	HH	HH	Z	HH
6, 38	Z	Z	Z	HH	HH	HH	Z
7, 39	Z	Z	Z	HH	HH	HH	HH
8, 40	Z	Z	HH	Z	Z	Z	Z
9, 41	Z	Z	HH	Z	Z	Z	HH
10, 42	Z	Z	HH	Z	Z	HH	Z
11, 43	Z	Z	HH	Z	Z	HH	HH
12, 44	Z	Z	HH	Z	HH	Z	Z
13, 45	Z	Z	HH	Z	HH	Z	HH
14, 46	Z	Z	HH	Z	HH	HH	Z
15, 47	Z	Z	HH	Z	HH	HH	HH
16, 48	Z	HH	Z	Z	Z	Z	Z
17, 49	Z	HH	Z	Z	Z	Z	HH
18, 50	Z	HH	Z	Z	Z	HH	Z
19, 51	Z	HH	Z	Z	Z	HH	HH
20, 52	Z	HH	Z	Z	HH	Z	Z
21, 53	Z	HH	Z	Z	HH	Z	HH
22, 54	Z	HH	Z	Z	HH	HH	Z
23, 55	Z	HH	Z	Z	HH	HH	HH
24, 56	HH	Z	Z	Z	Z	Z	Z
25, 57	HH	Z	Z	Z	Z	Z	HH
26, 58	HH	Z	Z	Z	Z	HH	Z
27, 59	HH	Z	Z	Z	Z	HH	HH
28, 60	HH	Z	Z	Z	HH	Z	Z
29, 61	HH	Z	Z	Z	HH	Z	HH
30, 62	HH	Z	Z	Z	HH	HH	Z
31, 63	HH	Z	Z	Z	HH	HH	HH

Table 2 Product Line Select

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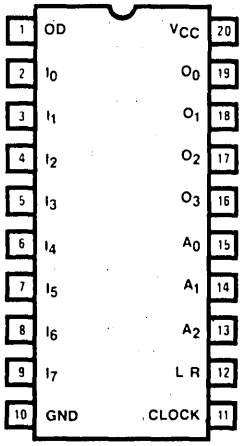
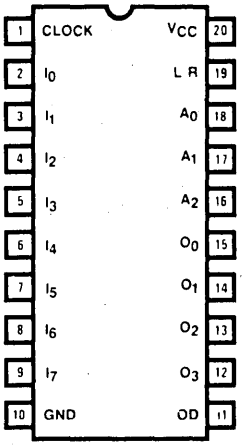
Pin Configurations

PRODUCTS 0 THRU 31



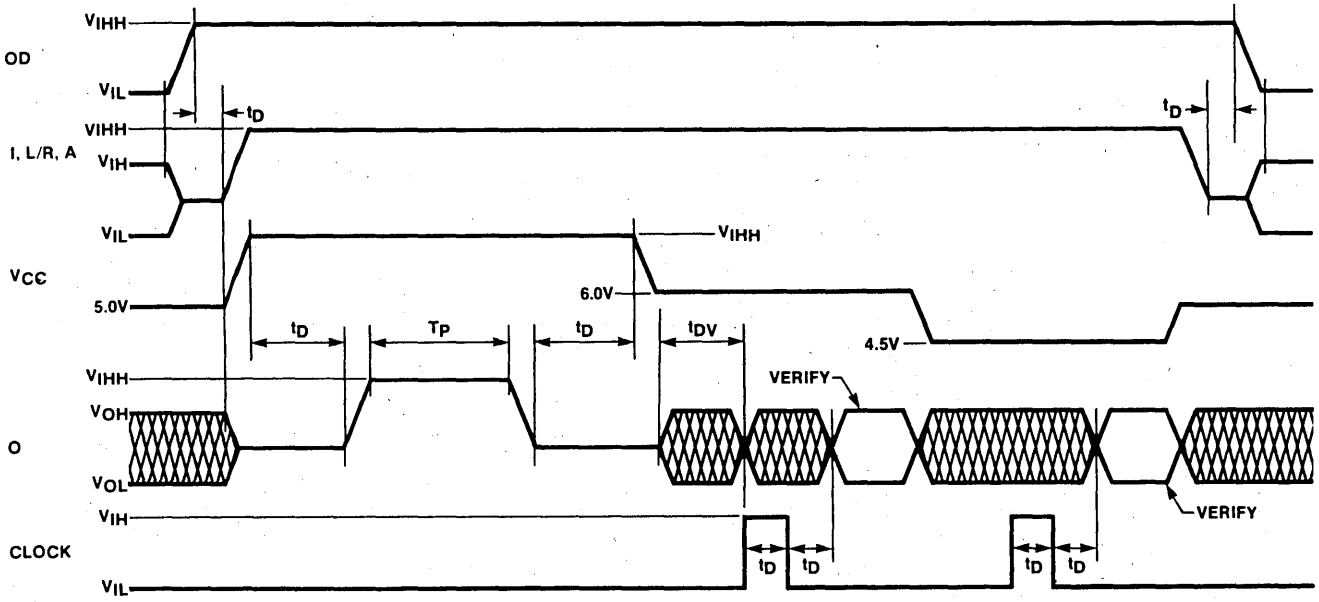
PRODUCTS 32 THRU 63



Programming Parameters $T_A = 25°C$

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNIT
V_{IHH}	Program-level input voltage		11	11.5	12	V
I_{IHH}	Program-level input current	Output Program Pulse			50	mA
		OD, L/R			25	
		All Other Inputs			5	
I_{CCH}	Program Supply Current				400	mA
T_P	Program Pulse Width		10		50	μs
t_D	Delay time		100			ns
t_{DV}	Delay Time to Verify		100			μs
	Program Pulse duty cycle				25	%
V_P	Verify-Protect-input voltage		20	21	22	V
I_P	Verify-Protect-input current				400	mA
T_{PP}	Verify-Protect Pulse Width		20		50	msec

Programming Waveforms



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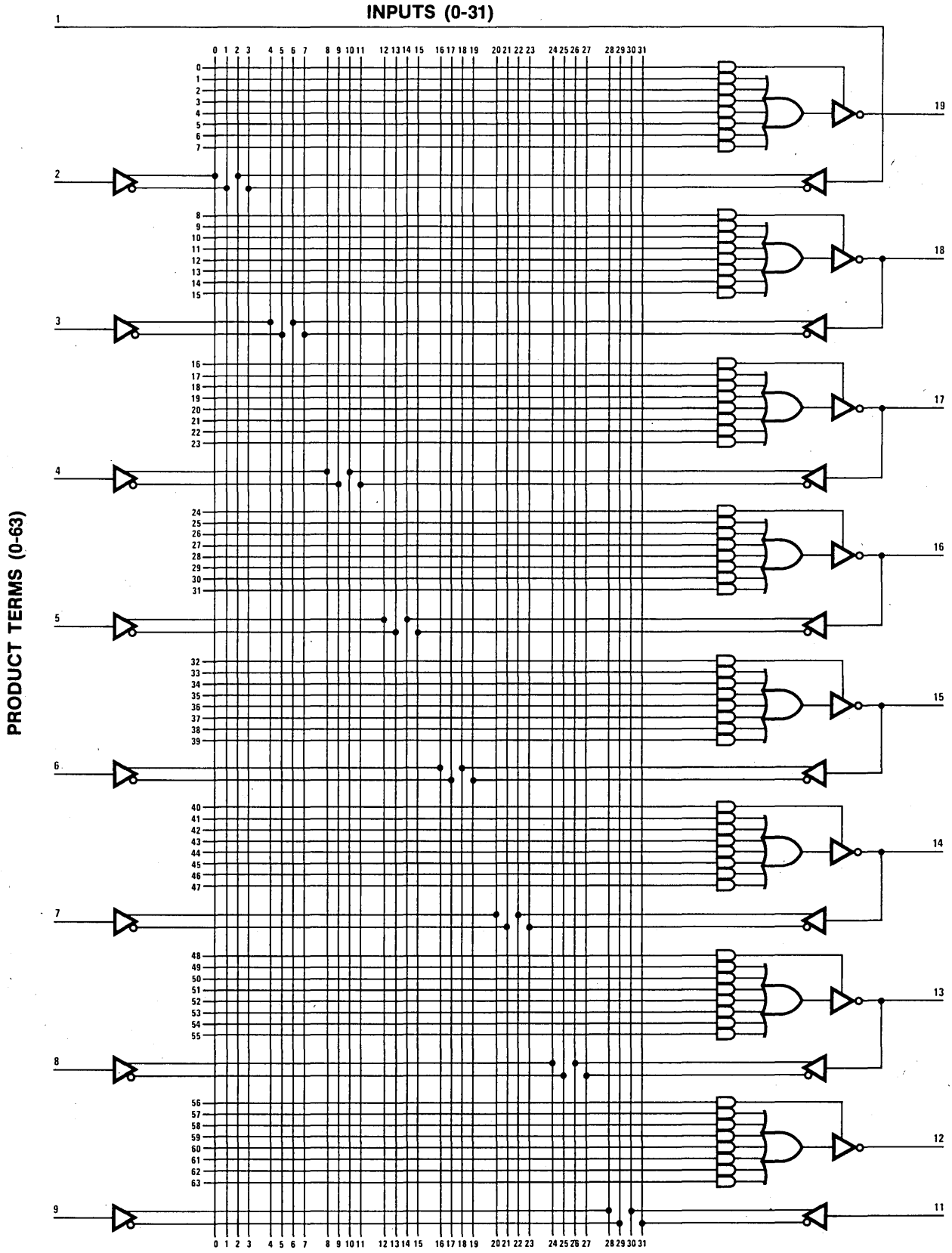
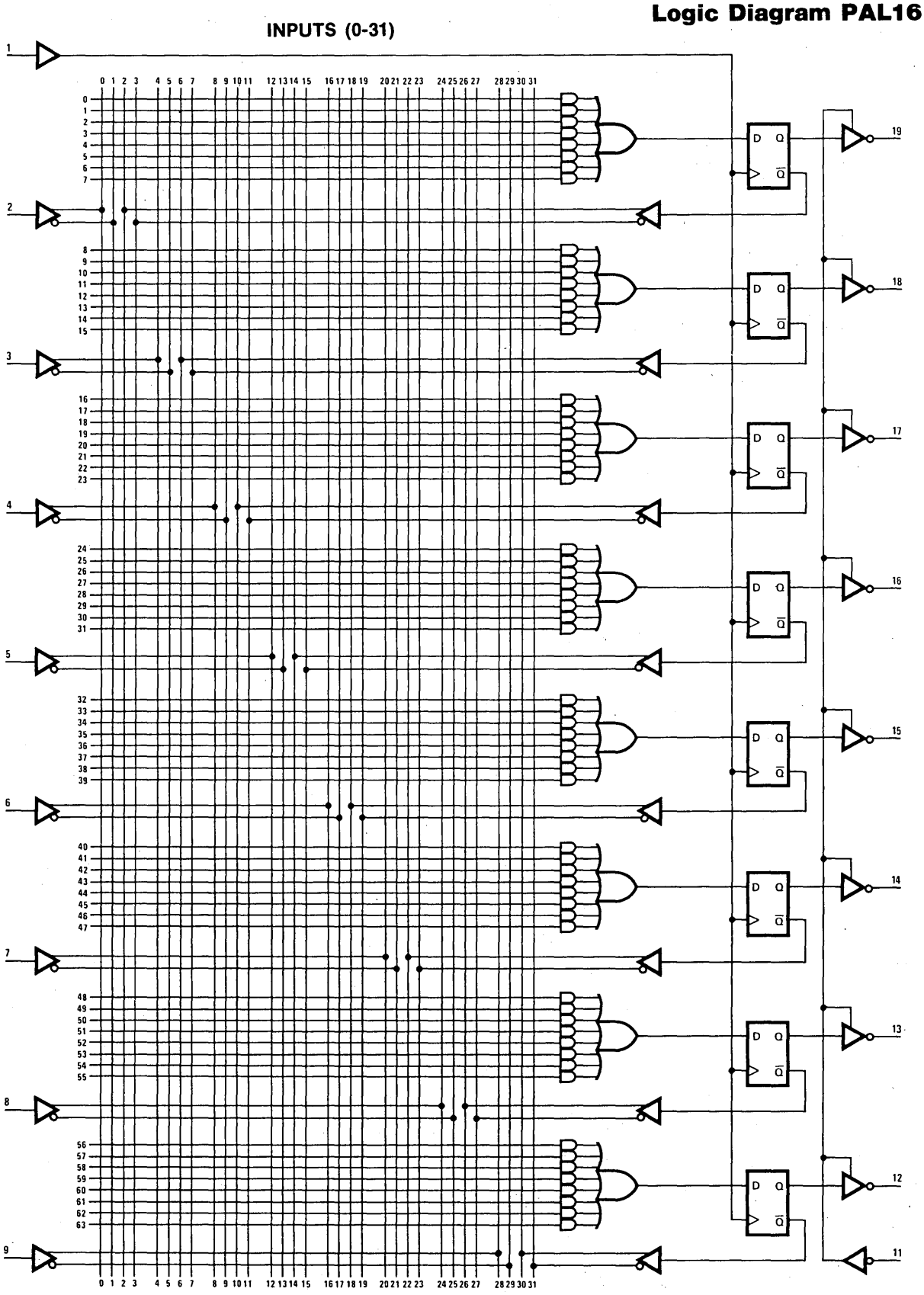
Logic Diagram PAL16L8



Logic Diagram PAL16R8



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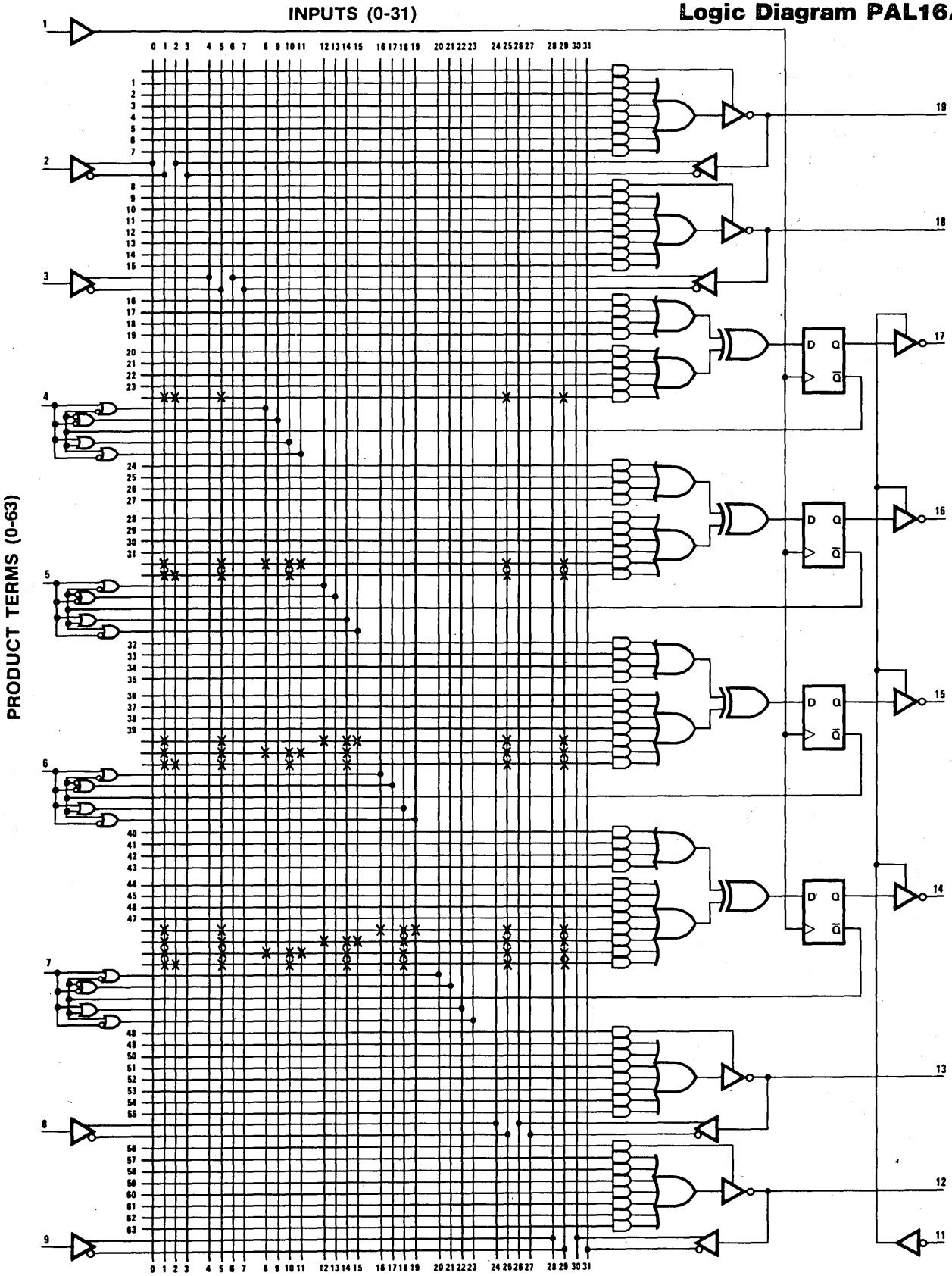
Logic Diagram PAL16A4



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Programmable Array Logic Family

PAL® Series 24

U.S. Patent 4124899

Features/Benefits

- **Programmable replacement for conventional TTL logic.**
- **Reduces IC inventories substantially and simplifies their control.**
- **Reduces chip count by 5 to 1.**
- **Expedites and simplifies prototyping and board layout.**
- **Saves space with 24-pin SKINNYDIP™ packages.**
- **Programmed on standard PROM programmers.**
- **Programmable three-state outputs.**
- **Special feature reduces possibility of copying by competitors.**

Description

The PAL Series 24 family complements the PAL Series 20 family by providing two additional inputs and two additional outputs, allowing more complex functions in a single package. This new family is made feasible by the Monolithic Memories new and revolutionary 24-pin SKINNYDIP™.

In addition to providing more logic function per chip, 24 pins allows for many natural functions which were previously unavailable in skinny 300 mil-wide packages. Examples include:

- 8-bit parallel-in parallel-out counters
- 8-bit parallel-in parallel-out shift registers
- 16-Line-to-1-Line Multiplexors
- Dual 8-Line-to-1-Line Multiplexors
- Quad 4-Line-to-1-Line Multiplexors

These natural functions provide twice the density of traditional 16-pin packages.

The PAL family utilizes an advanced Schottky TTL process and the Bipolar PROM fusible link technology to provide user programmable logic for replacing conventional SSI/MSI gates and flip-flops at reduced chip count.

The family lets the systems engineer "design his own chip" by blowing fusible links to configure AND and OR gates to perform his desired logic function. Complex interconnections which previously required time-consuming layout are thus "lifted" from PC board etch and placed on silicon where they can be easily modified during prototype check-out or production.

The PAL transfer function is the familiar sum of products. Like the PROM, the PAL has a single array of fusible links. Unlike the PROM, the PAL is a programmable AND array driving a fixed OR array (the PROM is a fixed AND array driving a programmable OR array). In addition the PAL provides these options:

- Variable input/output pin ratio
- Programmable three-state outputs
- Registers with feedback

PART NUMBER	PKG	DESCRIPTION
PAL12L10	J,N	Deca 12 Input And-Or-Invert Gate Array
PAL14L8	J,N	Octal 14 Input And-Or-Invert Gate Array
PAL16L6	J,N	Hex 16 Input And-Or-Invert Gate Array
PAL18L4	J,N	Quad 18 Input And-Or-Invert Gate Array
PAL20L2	J,N	Dual 20 Input And-Or-Invert Gate Array
PAL20C1	J,N	20 Input And-Or/And-Or Invert Gate Array
PAL20L10	J,N	Deca 20 Input And-Or-Invert Gate Array
PAL20X10	J,N	Deca 20 Input Registered And-Or-Xor Gate Array
PAL20X8	J,N	Octal 20 Input Registered And-Or-Xor Gate Array
PAL20X4	J,N	Quad 20 Input Registered And-Or-Xor Gate Array

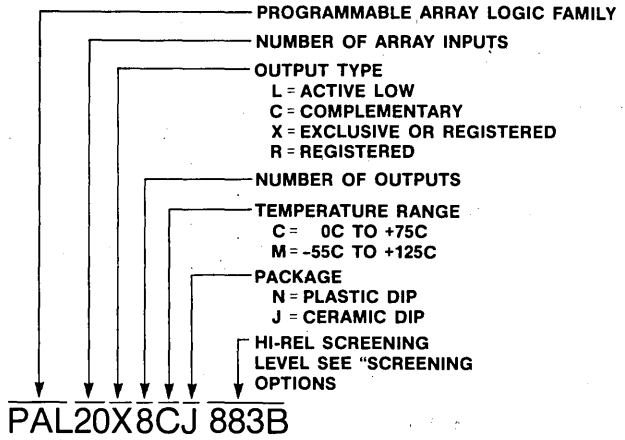
Unused inputs are tied directly to V_{CC} or GND. Product terms with all fuses blown assume the logical high state, and product terms connected to both true and complement of any single input assume the logical low state. Registers consist of D type flip-flops which are loaded on the low to high transition of the clock. PAL Logic Diagrams are shown with all fuses blown, enabling the designer use of the diagrams as coding sheets.

To design a PAL, the user writes the logic equations using PAL DESIGN SPECIFICATION standard format (F108). This specification may be submitted to Monolithic Memories where it is computer processed and assigned a bit pattern number, eg P0123. Monolithic Memories accepts the PAL DESIGN SPECIFICATION in one of the three forms:

1. Computer generated listings.
2. Typed or hand-written forms F107 and F108.
3. Direct on line data transmission to Monolithic Memories Timeshare computer system via telephone, (local telephone network to major U.S. cities, London and Paris) or TWX online Boston TWX No.).

The entire PAL family is programmed on inexpensive conventional PROM programmers with appropriate personality and socket adapter cards. Once the PAL is programmed and verified, two additional fuses may be blown to defeat verification. This feature gives the user a proprietary circuit which is very difficult to copy.

Ordering Information



SKINNYDIP is a registered trademark of Monolithic Memories

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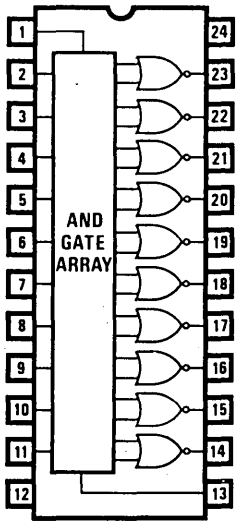
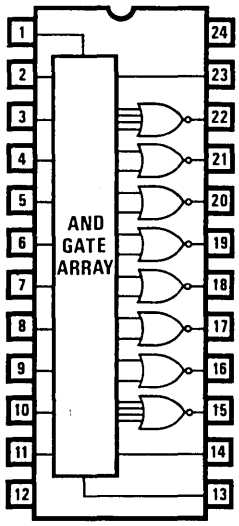
Monolithic Memories

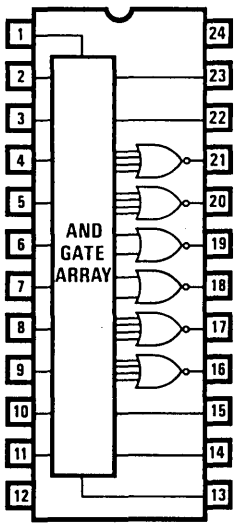
PAL12L10



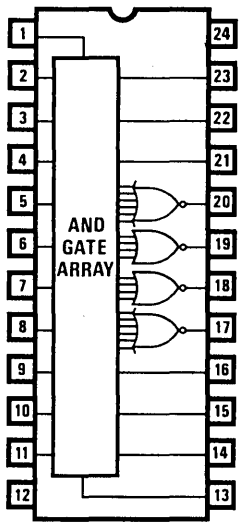
PAL14L8



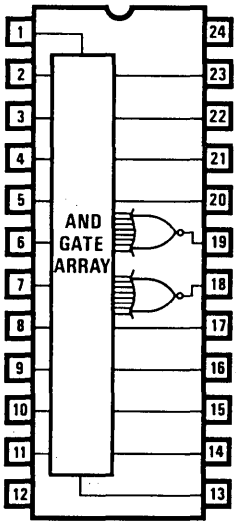
PAL16L6



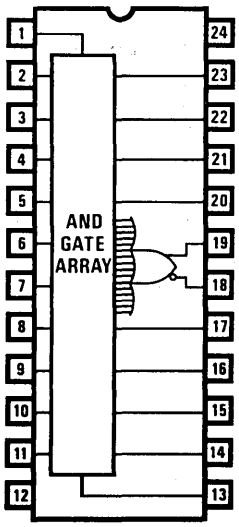
PAL18L4



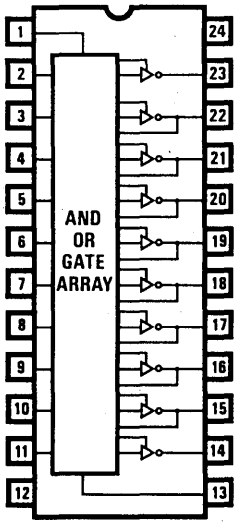
PAL20L2



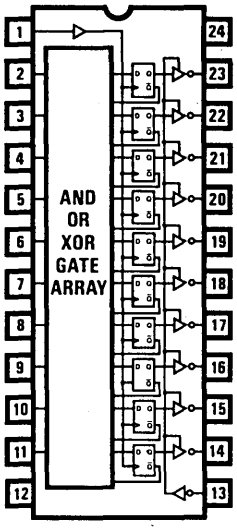
PAL20C1



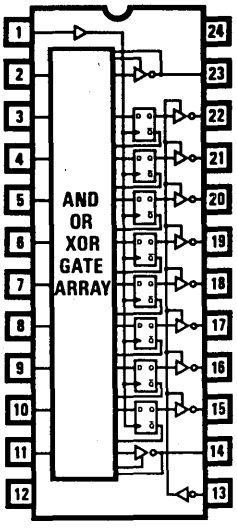
PAL20L10



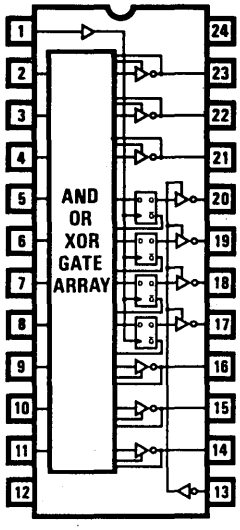
PAL20X10



PAL20X8



PAL20X4



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Absolute Maximum Ratings

	Operating	Programming
Supply Voltage, VCC	7	12V
Input Voltage	5.5V	12V*
Off-state output Voltage	5.5V	12V
Storage temperature	−65° to +150°C	

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	40	20		35	20		ns
		High	30	10		25	10		
t_{su}	Set up time		60	38		50	38		ns
t_h	Hold time		0	−15		0	−15		
T_A	Operating free air temperature		−55			0		75	°C
T_C	Operating case temperature				125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP††	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA			−0.8	−1.5	V
I_{IL}	Low-level input current †	V_{CC} = MAX	V_I = 0.4V			−0.02	−0.25	mA
I_{IH}	High-level input current †	V_{CC} = MAX	V_I = 2.4V				25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	12L10, 14L8, 16L6, 18L4, 20L2, 20C1	I_{OL} = 8mA		0.3	0.5	V
			20L10, 20X10, 20X8, 20X4	MIL I_{OL} = 12mA				
				COM I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OH} = −2mA	MIL	2.4	2.8		V
			I_{OH} = −3.2mA	COM				
I_{OZL}	Off-state output current †	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V	V_O = 0.4V				−100	μA
I_{OZH}			V_O = 2.4V				100	μA
I_{OS}	Output short-circuit current**	V_{CC} = 5V	V_O = 0V		−30	−70	−130	mA
I_{CC}	Supply current	V_{CC} = MAX	12L10, 14L8, 16L6, 18L4, 20L2, 20C1			60	100	mA
			20X4, 20X8, 20X10			120	180	
			20L10			90	165	

† I/O pin leakage is the worst case of I_{OZX} or I_{IX} e.g. I_{IX} and I_{OZH}

†† All typical values are at V_{CC} = 5V, T_A = 25°C.

* Pins 1 and 13 may be raised to 22V max.

** Only one output shorted at a time.

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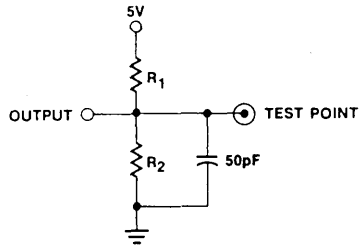
Switching Characteristics

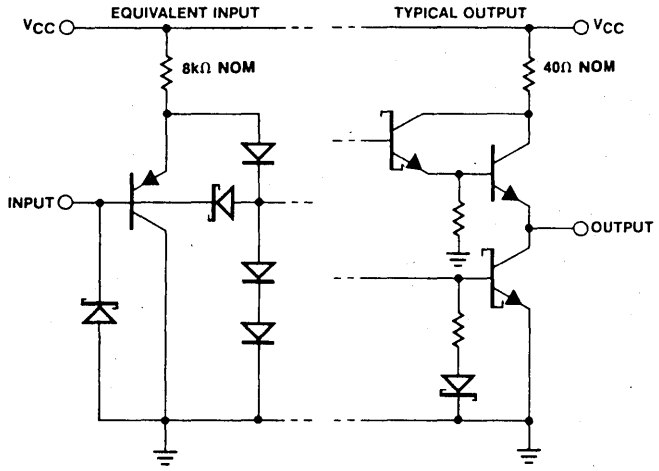
Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input to output	12L10, 14L8, 16L6, 18L4, 20L2, 20C1	R_1 = 560Ω R_2 = 1.1kΩ		25	45		25	40	ns
t_{PD}	Input or feedback to output		20L10, 20X10 20X8, 20X4 R_1 = 200Ω R_2 = 390Ω		35	60		35	50	ns
t_{CLK}	Clock to output or feedback				20	35		20	30	ns
t_{PZX}	Pin 13 to output enable				20	45		20	35	ns
t_{PXZ}	Pin 13 to output disable				20	45		20	35	ns
t_{PZX}	Input to output enable				35	55		35	45	ns
t_{PXZ}	Input to output disable				35	55		35	45	ns
f_{MAX}	Maximum frequency			10.5	16		12.5	16		MHz

Test Load



Schematic of Inputs and Outputs



Programming

PAL fuses are programmed using a low-voltage linear-select procedure which is common to all PAL types. The array is divided into two groups, products 0 thru 39 and products 40 thru 79, for which pin identifications are shown in Pin Configurations below. To program a particular fuse, both an input line and a product line are selected according to the following procedure:

Step 1 Raise Output Disable, OD, to V_{IHH}.

Step 2 Select an input line by specifying I_0, I_1, I_2, I_3, I_4, I_5, I_6, I_7, I_8, I_9 and L/R as shown in Table 1.

Step 3 Select a product line by specifying A_0, A_1 and A_2 one-of-eight select as shown in Table 2.

Step 4 Raise V_{CC} (pin 24) to V_{IHH}.

Step 5 Program the fuse by pulsing the output pins, O, of the selected product group to V_{IHH} as shown in Programming Waveform.

Step 6 Lower V_{CC} (pin 24) to 6.0 V.

Step 7 Pulse the CLOCK pin and verify the output pin, O, to be Low for active Low PAL types or High for active High PAL types.

Step 8 Lower V_{CC} (pin 24) to 4.5 V and repeat step 7.

Step 9 Should the output not verify, repeat steps 1 thru 8 up to five (5) times.

This procedure is repeated for all fuses to be blown (see Programming Waveforms).

To prevent further verification, two last fuses may be blown by raising pin 1 and pin 13 to V_P. V_{CC} is not required during this operation.

Voltage Legend

L = Low-level input voltage, V_{IL}
H = High-level input voltage, V_{IH}
HH = High-level program voltage, V_{IHH}
Z = High impedance (e.g. 10K Ω to 5.0V)

INPUT LINE NUMBER	PIN IDENTIFICATION										
	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	L/R
0	HH	HH	HH	HH	HH	HH	HH	HH	HH	L	Z
1	HH	HH	HH	HH	HH	HH	HH	HH	HH	H	Z
2	HH	HH	HH	HH	HH	HH	HH	HH	HH	L	HH
3	HH	HH	HH	HH	HH	HH	HH	HH	HH	H	HH
4	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	Z
5	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	Z
6	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	HH
7	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	HH
8	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	Z
9	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	Z
10	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	HH
11	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	HH
12	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	Z
13	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	Z
14	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	HH
15	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	HH
16	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	Z
17	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	Z
18	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	HH
19	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	HH
20	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	Z
21	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	Z
22	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	HH
23	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	HH
24	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	Z
25	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	Z
26	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	HH
27	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	HH
28	HH	HH	L	HH	HH	HH	HH	HH	HH	HH	Z
29	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	Z
30	HH	HH	L	HH	HH	HH	HH	HH	HH	HH	HH
31	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	HH
32	HH	L	HH	HH	HH	HH	HH	HH	HH	HH	Z
33	HH	H	HH	HH	HH	HH	HH	HH	HH	HH	Z
34	HH	L	HH	HH	HH	HH	HH	HH	HH	HH	HH
35	HH	H	HH	HH	HH	HH	HH	HH	HH	HH	HH
36	L	HH	HH	HH	HH	HH	HH	HH	HH	HH	Z
37	H	HH	HH	HH	HH	HH	HH	HH	HH	HH	Z
38	L	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH
39	H	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH

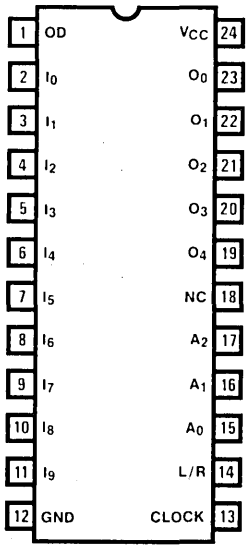
Table 1 Input Line Select

PRODUCT LINE NUMBER	PIN IDENTIFICATION							
	O_4	O_3	O_2	O_1	O_0	A_2	A_1	A_0
0, 40	Z	Z	Z	Z	HH	Z	Z	Z
1, 41	Z	Z	Z	Z	HH	Z	Z	HH
2, 42	Z	Z	Z	Z	HH	Z	HH	Z
3, 43	Z	Z	Z	Z	HH	Z	HH	HH
4, 44	Z	Z	Z	Z	HH	HH	Z	Z
5, 45	Z	Z	Z	Z	HH	HH	Z	HH
6, 46	Z	Z	Z	Z	HH	HH	HH	Z
7, 47	Z	Z	Z	Z	HH	HH	HH	HH
8, 48	Z	Z	Z	HH	Z	Z	Z	Z
9, 49	Z	Z	Z	HH	Z	Z	Z	HH
10, 50	Z	Z	Z	HH	Z	Z	HH	Z
11, 51	Z	Z	Z	HH	Z	Z	HH	HH
12, 52	Z	Z	Z	HH	Z	HH	Z	Z
13, 53	Z	Z	Z	HH	Z	HH	Z	HH
14, 54	Z	Z	Z	HH	Z	HH	HH	Z
15, 55	Z	Z	Z	HH	Z	HH	HH	HH
16, 56	Z	Z	HH	Z	Z	Z	Z	Z
17, 57	Z	Z	HH	Z	Z	Z	Z	HH
18, 58	Z	Z	HH	Z	Z	Z	HH	Z
19, 59	Z	Z	HH	Z	Z	Z	HH	HH
20, 60	Z	Z	HH	Z	Z	HH	Z	Z
21, 61	Z	Z	HH	Z	Z	HH	Z	HH
22, 62	Z	Z	HH	Z	Z	HH	HH	Z
23, 63	Z	Z	HH	Z	Z	HH	HH	HH
24, 64	Z	HH	Z	Z	Z	Z	Z	Z
25, 65	Z	HH	Z	Z	Z	Z	Z	HH
26, 66	Z	HH	Z	Z	Z	Z	HH	Z
27, 67	Z	HH	Z	Z	Z	Z	HH	HH
28, 68	Z	HH	Z	Z	Z	HH	Z	Z
29, 69	Z	HH	Z	Z	Z	HH	Z	HH
30, 70	Z	HH	Z	Z	Z	HH	HH	Z
31, 71	Z	HH	Z	Z	Z	HH	HH	HH
32, 72	HH	Z	Z	Z	Z	Z	Z	Z
33, 73	HH	Z	Z	Z	Z	Z	Z	HH
34, 74	HH	Z	Z	Z	Z	Z	HH	Z
35, 75	HH	Z	Z	Z	Z	Z	HH	HH
36, 76	HH	Z	Z	Z	Z	HH	Z	Z
37, 77	HH	Z	Z	Z	Z	HH	Z	HH
38, 78	HH	Z	Z	Z	Z	HH	HH	Z
39, 79	HH	Z	Z	Z	Z	HH	HH	HH

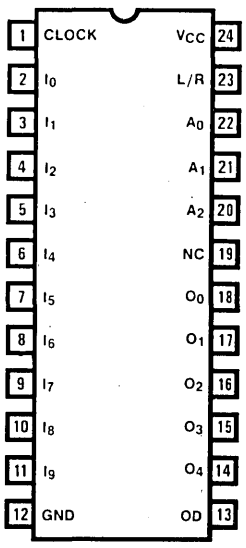
Table 2 Product Line Select

Pin Configurations

PRODUCTS 0 THRU 39



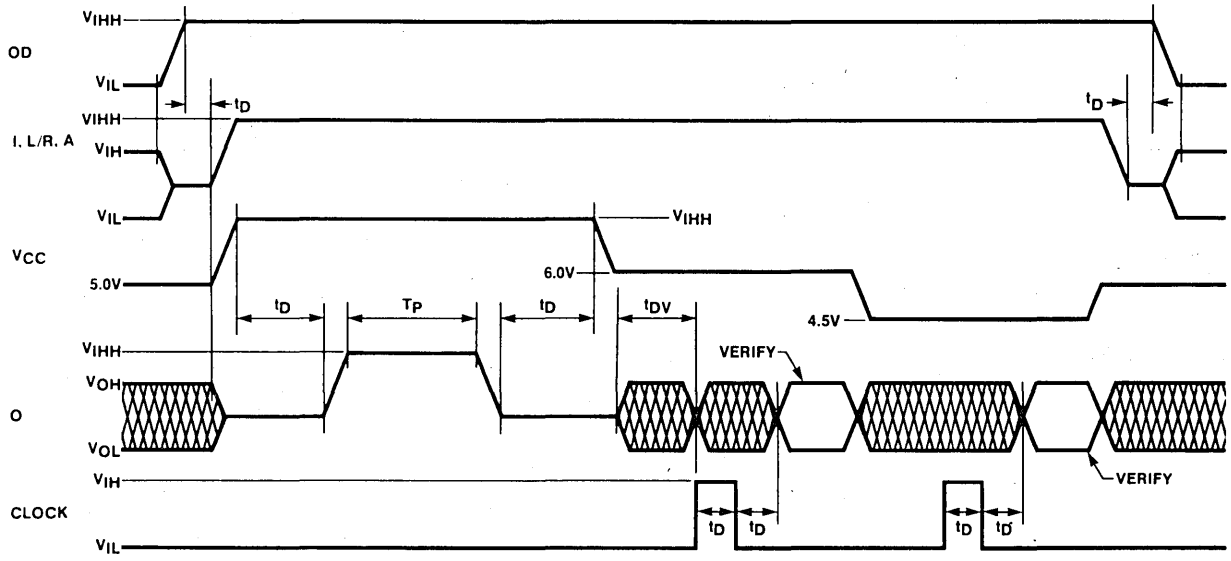
PRODUCTS 40 THRU 79



Programming Parameters $T_A = 25°C$

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNIT
V_{IHH}	Program-level input voltage		11.5	11.75	12	V
I_{IHH}	Program-level input current	Output Program Pulse			50	mA
		OD, L/R			50	
		All Other Inputs			5	
I_{CCH}	Program Supply Current				400	mA
T_P	Program Pulse Width		10		50	μs
t_D	Delay time		100			ns
t_{DV}	Delay Time to Verify		100			μs
	Program Pulse duty cycle				25	%
V_P	Verify-Protect-input voltage		20	21	22	V
I_P	Verify-Protect-input current				400	mA
T_{PP}	Verify-Protect Pulse Width		20		50	msec

Programming Waveforms



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High Speed Programmable Array Logic Family

PAL® Series 20A

U.S. Patent 4124899

March 1982

Features/Benefits

- **15ns typical propagation delay**
- **Programmable replacement for TTL logic**
- **Reduces IC inventories**
- **Reduces chip count by greater than 4 to 1**
- **Expedites prototyping and board layout**
- **Saves space with 20-pin SKINNYDIP™ packages**
- **Programmed on standard PROM programmers**
- **Programmable three-state outputs**
- **Last fuse prevents duplication on a PROM/PAL programmer**

PART NUMBER	PKG	GATE ARRAY DESCRIPTION
PAL16L8A	N,J,F,L	Octal 16 Input And-Or-Invert
PAL16R8A	N,J,F,L	Octal 16 Input Registered And-Or
PAL16R6A	N,J,F,L	Hex 16 Input Registered And-Or
PAL16R4A	N,J,F,L	Quad 16 Input Registered And-Or

Unused inputs are tied directly to V_{CC} or GND. Product terms with all fuses blown assume the logical high state, and product terms connected to both true and complement of any single input assume the logical low state. Registers consist of D type flip-flops which are loaded on the low to high transition of the clock. PAL Logic Diagrams are shown with all fuses blown, enabling the designer use of the diagrams as coding sheets.

Description

The PAL Series 20A family utilizes Monolithic Memories advanced self-aligned washed emitter high speed bipolar process and the bipolar PROM fusible link technology to provide user programmable logic for replacing conventional SSI/MSI gates and flip-flops at reduced chip count.

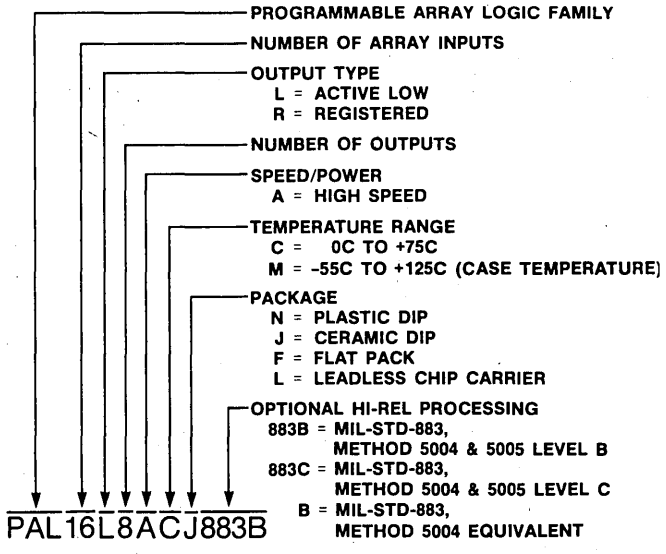
The family lets the systems engineer "design his own chip" by blowing fusible links to configure AND and OR gates to perform his desired logic function. Complex interconnections which previously required time-consuming layout are thus "lifted" from the PC board and are placed on silicon where they can be easily modified during prototype check-out or production.

The PAL transfer function is the familiar sum of products. Like the PROM, the PAL has a single array of fusible links. Unlike the PROM, the PAL is a programmable AND array driving a fixed OR array (the PROM is a fixed AND array driving a programmable OR array). In addition the PAL provides these options:

- Variable input/output pin ratio
- Programmable three-state outputs
- Registers with feedback

The entire PAL family is programmed on inexpensive conventional PROM programmers with appropriate personality and socket adapter cards. Once the PAL is programmed and verified, two additional fuses may be blown to defeat verification. This feature gives the user a proprietary circuit which is very difficult to copy.

Ordering Information



Monolithic Memories

CUSTOM/SEMICUSTOM

PAL® is a registered trademark of Monolithic Memories.

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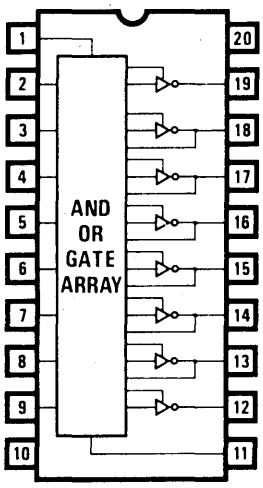
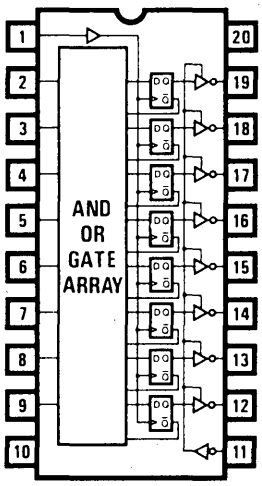
Monolithic Memories

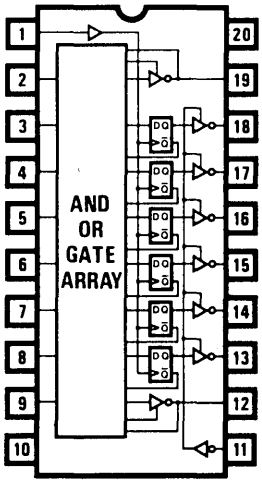
PAL16L8A



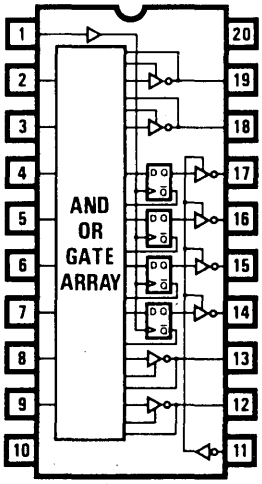
PAL16R8A



PAL16R6A



PAL16R4A



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Absolute Maximum Ratings

	Operating	Programming
Supply Voltage, V_{CC}	-0.5 to 7.0V	-0.5 to 12.0V
Input Voltage	-1.5 to 5.5V	-1.0 to 12.0V⊕
Off-state output Voltage	5.5V	12.0V
Storage temperature	-65° to +150°C	

Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	Low	20	10		15	10		ns
		High	20	10		15	10		
t_{su}	Set up time from input or feedback to clock	16R8A 16R6A 16R4A	30	16		25	16		ns
t_h	Hold time		0	-10		0	-10		ns
T_A	Operating free-air temperature		-55			0	25	75	°C
T_C	Operating case temperature				125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18mA			-0.8	-1.5	V
I_{IL}	Low-level input current †	V_{CC} = MAX	V_I = 0.4V			-0.02	-0.25	mA
I_{IH}	High-level input current †	V_{CC} = MAX	V_I = 2.4V				25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL	I_{OL} = 12mA		0.3	0.5	V
			COM	I_{OL} = 24mA				
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL	I_{OH} = -2mA	2.4	2.8		V
			COM	I_{OH} = -3.2mA				
I_{OZL}	Off-state output current †	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V		V_O = 0.4V			-100	μA
I_{OZH}				V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current**	V_{CC} = 5V		V_O = 0V	-30	-70	-130	mA
I_{CC}	Supply current	V_{CC} = MAX				120	180	mA

† I/O pin leakage is the worst case of I_{OZX} or I_{IX} e.g., I_{IL} and I_{OZH}.

†† All typical values are at V_{CC} = 5V, T_A = 25°C.

* These are absolute voltages with respect to pin 10 on the device and includes all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

** Only one output shorted at a time.

⊕Pins 1 and 11 may be raised to 22V max.

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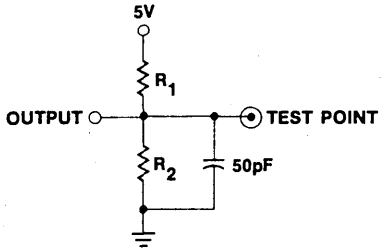
Switching Characteristics

Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feedback to output	16R6A 16R4A 16L8A	$R_1 = 200\Omega$ $R_2 = 390\Omega$		15	30		15	25	ns
t_{CLK}	Clock to output or feedback				10	20		10	15	ns
t_{PZX}	Pin 11 to output enable				10	25		10	20	ns
t_{PXZ}	Pin 11 to output disable				11	25		11	20	ns
t_{PZX}	Input to output enable	16R6A 16R4A 16L8A			10	30		10	25	ns
t_{PXZ}	Input to output disable	16R6A 16R4A 16L8A			13	30		13	25	ns
f_{MAX}	Maximum frequency	16R8A 16R6A 16R4A		20	30		25	30		MHz

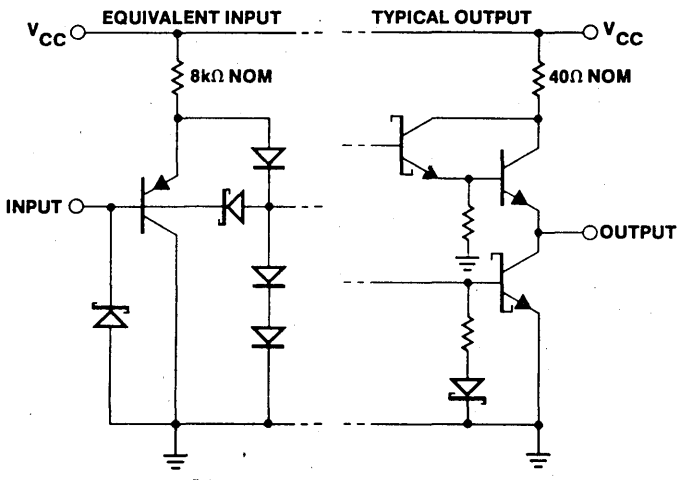
Test Load



Available Programmers

MANUFACTURER	PERSONALITY CARD SET	SOCKET ADAPTER CONFIGURATION
Data I/O Corporation	909-1427	715 1428-1 715 1428-2 715 1428-3
Pro-Log Corporation	PM9068	
Stag Systems	PM202	AM10H8 AM10L8 AM12H6 AM12L6 AM14H4 AM14L4 AM16H2 AM16L2 AM16C1
Structured Design	SD20/24	
Kontron	MPP-80S	

Schematic of Inputs and Outputs



Programming

PAL fuses are programmed using a low-voltage linear-select procedure which is common to all 4 PAL types. The array is divided into two groups, products 0 thru 31 and products 32 thru 63, for which pin identifications are shown in Pin Configurations below. To program a particular fuse, both an input line and a product line are selected according to the following procedure:

Step 1 Raise Output Disable, OD, to V_{IHH}

Step 2 Select an input line by specifying $I_0, I_1, I_2, I_3, I_4, I_5, I_6, I_7$ and L/R as shown in Table 1.

Step 3 Select a product line by specifying A_0, A_1 and A_2 one-of-eight select as shown in Table 2.

Step 4 Raise V_{CC} (pin 20) to V_{IHH}

Step 5 Program the fuse by pulsing the output pins, O, of the selected product group to V_{IHH} as shown in Programming Waveform.

Step 6 Lower V_{CC} (pin 20) to 6.0 V

Step 7 Pulse the CLOCK pin and verify the output pin, O, to be Low for active Low PAL types or High for active High PAL types.

Step 8 Lower V_{CC} (pin 20) to 4.5 V and repeat step 7.

Step 9 Should the output not verify, repeat steps 1 thru 8 up to five (5) times.

This procedure is repeated for all fuses to be blown (see Programming Waveforms).

To prevent further verification, two last fuses may be blown by raising pin 1 and pin 11 to V_P. V_{CC} is not required during this operation.

Voltage Legend

L = Low-level input voltage, V_{IL}
H = High-level input voltage, V_{IH}
HH = High-level program voltage, V_{IHH}
Z = High impedance (e.g., 10kΩ to 5.0V)

INPUT LINE NUMBER	PIN IDENTIFICATION								
	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	L/R
0	HH	HH	HH	HH	HH	HH	HH	L	Z
1	HH	HH	HH	HH	HH	HH	HH	H	Z
2	HH	HH	HH	HH	HH	HH	HH	L	HH
3	HH	HH	HH	HH	HH	HH	HH	H	HH
4	HH	HH	HH	HH	HH	HH	L	HH	Z
5	HH	HH	HH	HH	HH	HH	H	HH	Z
6	HH	HH	HH	HH	HH	HH	L	HH	HH
7	HH	HH	HH	HH	HH	HH	H	HH	HH
8	HH	HH	HH	HH	HH	L	HH	HH	Z
9	HH	HH	HH	HH	HH	H	HH	HH	Z
10	HH	HH	HH	HH	HH	L	HH	HH	HH
11	HH	HH	HH	HH	HH	H	HH	HH	HH
12	HH	HH	HH	HH	L	HH	HH	HH	Z
13	HH	HH	HH	HH	H	HH	HH	HH	Z
14	HH	HH	HH	HH	L	HH	HH	HH	HH
15	HH	HH	HH	HH	H	HH	HH	HH	HH
16	HH	HH	HH	L	HH	HH	HH	HH	Z
17	HH	HH	HH	H	HH	HH	HH	HH	Z
18	HH	HH	HH	L	HH	HH	HH	HH	HH
19	HH	HH	HH	H	HH	HH	HH	HH	HH
20	HH	HH	L	HH	HH	HH	HH	HH	Z
21	HH	HH	H	HH	HH	HH	HH	HH	Z
22	HH	HH	L	HH	HH	HH	HH	HH	HH
23	HH	HH	H	HH	HH	HH	HH	HH	HH
24	HH	L	HH	HH	HH	HH	HH	HH	Z
25	HH	H	HH	HH	HH	HH	HH	HH	Z
26	HH	L	HH	HH	HH	HH	HH	HH	HH
27	HH	H	HH	HH	HH	HH	HH	HH	HH
28	L	HH	HH	HH	HH	HH	HH	HH	Z
29	H	HH	HH	HH	HH	HH	HH	HH	Z
30	L	HH	HH	HH	HH	HH	HH	HH	HH
31	H	HH	HH	HH	HH	HH	HH	HH	HH

Table 1 Input Line Select

PRODUCT LINE NUMBER	PIN IDENTIFICATION						
	O_3	O_2	O_1	O_0	A_2	A_1	A_0
0, 32	Z	Z	Z	HH	Z	Z	Z
1, 33	Z	Z	Z	HH	Z	Z	HH
2, 34	Z	Z	Z	HH	Z	HH	Z
3, 35	Z	Z	Z	HH	Z	HH	HH
4, 36	Z	Z	Z	HH	HH	Z	Z
5, 37	Z	Z	Z	HH	HH	Z	HH
6, 38	Z	Z	Z	HH	HH	HH	Z
7, 39	Z	Z	Z	HH	HH	HH	HH
8, 40	Z	Z	HH	Z	Z	Z	Z
9, 41	Z	Z	HH	Z	Z	Z	HH
10, 42	Z	Z	HH	Z	Z	HH	Z
11, 43	Z	Z	HH	Z	Z	HH	HH
12, 44	Z	Z	HH	Z	HH	Z	Z
13, 45	Z	Z	HH	Z	HH	Z	HH
14, 46	Z	Z	HH	Z	HH	HH	Z
15, 47	Z	Z	HH	Z	HH	HH	HH
16, 48	Z	HH	Z	Z	Z	Z	Z
17, 49	Z	HH	Z	Z	Z	Z	HH
18, 50	Z	HH	Z	Z	Z	HH	Z
19, 51	Z	HH	Z	Z	Z	HH	HH
20, 52	Z	HH	Z	Z	HH	Z	Z
21, 53	Z	HH	Z	Z	HH	Z	HH
22, 54	Z	HH	Z	Z	HH	HH	Z
23, 55	Z	HH	Z	Z	HH	HH	HH
24, 56	HH	Z	Z	Z	Z	Z	Z
25, 57	HH	Z	Z	Z	Z	Z	HH
26, 58	HH	Z	Z	Z	Z	HH	Z
27, 59	HH	Z	Z	Z	Z	HH	HH
28, 60	HH	Z	Z	Z	HH	Z	Z
29, 61	HH	Z	Z	Z	HH	Z	HH
30, 62	HH	Z	Z	Z	HH	HH	Z
31, 63	HH	Z	Z	Z	HH	HH	HH

Table 2 Product Line Select

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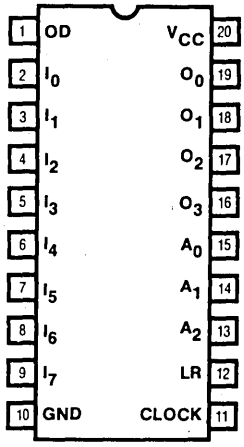
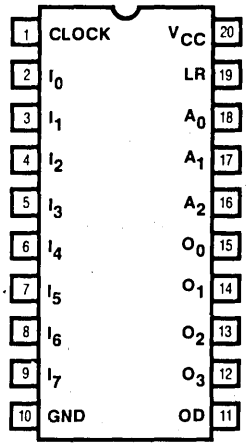
Pin Configurations

PRODUCTS 0 THRU 31



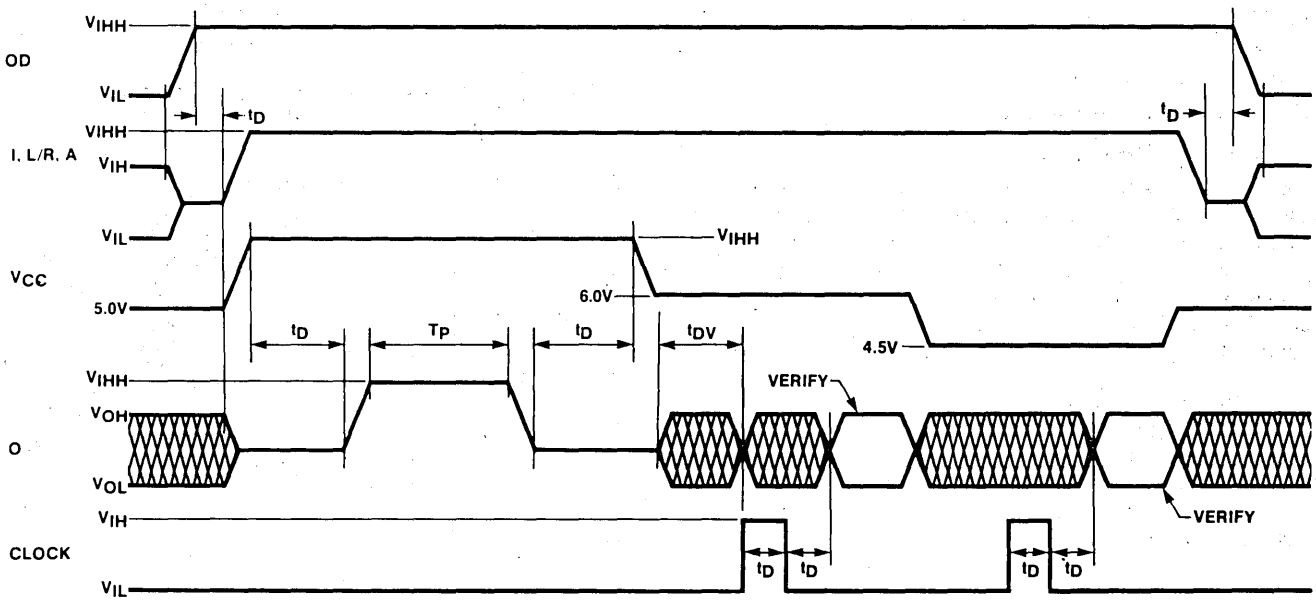
PRODUCTS 32 THRU 63



Programmer Requirement T_A = 25°C

SYMBOL	DEFINITION		LIMITS MIN	TYP	MAX	UNIT
V_{IHH}	Program-level input voltage		11	11.5	12	V
I_{IHH}	Program-level input current	Output Program Pulse			50	mA
		OD, L/R			25	
		All Other Inputs			5	
I_{CCH}	Program Supply Current				400	mA
T_P	Program Pulse Width		10		50	μs
t_D	Delay time		100			ns
t_{DV}	Delay Time to Verify		100			μs
	Program Pulse duty cycle				25	%
V_P	Verify-Protect-input voltage		20	21	22	V
I_P	Verify-Protect-input current				400	mA
T_{PP}	Verify-Protect Pulse Width		20		50	msec

Programming Waveforms



Low Power Programmable Array Logic Family

PAL® Series 20-2/-4

U.S. Patent 4124899

July 1982

Features/Benefits

- **Low power: 1/2 and 1/4 power options off standard PAL**
- **Programmable replacement for TTL logic**
- **Reduces IC inventories**
- **Reduces chip count by more than 4 to 1**
- **Expedites prototyping and board layout**
- **Save space with 20-pin SKINNYDIP® packages**
- **Programmed on standard PROM programmers**
- **Programmable three-state outputs**
- **Last fuse reduces possibility of copying**

Description

The PAL family utilizes an advanced Schottky Low Power TTL process and the Bipolar PROM fusible link technology to provide user programmable logic for replacing conventional Low Power SSI/MSI gates and flip-flops at reduced chip count.

The family lets the systems engineer "design his own chip" by blowing fusible links to configure AND and OR gates to perform his desired logic function. Complex interconnections which previously required time-consuming layout are thus "lifted" from PC board etch and placed on silicon where they can be easily modified during prototype check-out or production.

The PAL transfer function is the familiar sum of products. Like the PROM, the PAL has a single array of fusible links. Unlike the PROM, the PAL is a programmable AND array driving a fixed OR array (the PROM is a fixed AND array driving a programmable OR array). In addition the PAL provides these options:

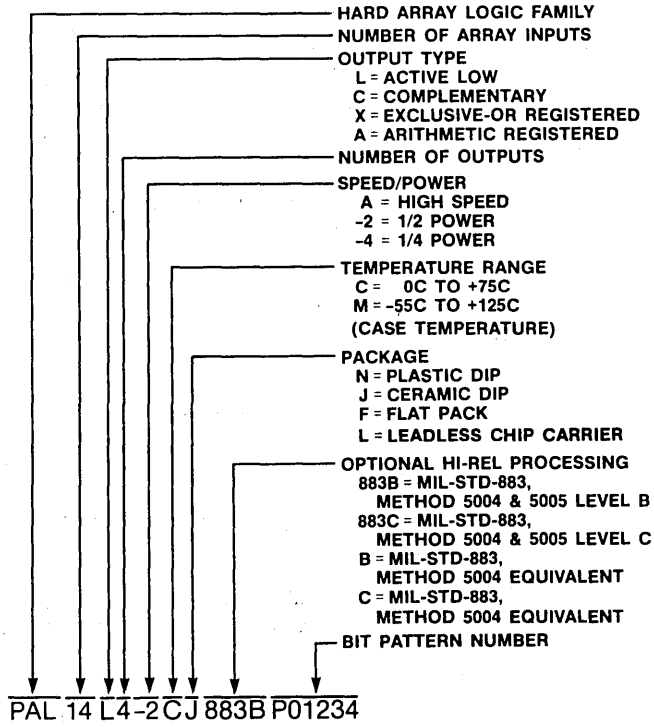
- Variable input/output pin ratio
- Programmable three-state outputs
- Registers with feedback

Unused inputs are tied directly to V_{CC} or GND. Product terms with all fuses blown assume the logical high state, and product terms connected to both true and complement of any single input assume the logical low state. Registers consist of D type flip-flops which are loaded on the low to high transition of the clock. PAL Logic Diagrams are shown with all fuses blown, enabling the designer use of the diagrams as coding sheets.

The entire PAL family is programmed on inexpensive conventional PROM programmers with appropriate personality and socket adapter cards. Once the PAL is programmed and verified, two additional fuses may be blown to defeat verification. This feature gives the user a proprietary circuit which is very difficult to copy.

PART NUMBER	PKG	GATE ARRAY DESCRIPTION
PAL10H8-2	N,J,F,L	Octal 10 Input And-Or
PAL12H6-2	N,J,F,L	Hex 12 Input And-Or
PAL14H4-2	N,J,F,L	Quad 14 Input And-Or
PAL16H2-2	N,J,F,L	Dual 16 Input And-Or
PAL16C1-2	N,J,F,L	16 Input And-Or/And-Or-Invert
PAL10L8-2	N,J,F,L	Octal 10 Input And-Or-Invert
PAL12L6-2	N,J,F,L	Hex 12 Input And-Or-Invert
PAL14L4-2	N,J,F,L	Quad 14 Input And-Or Invert
PAL16L2-2	N,J,F,L	Dual 16 Input And-Or-Invert
PAL16L8-2	N,J,F,L	Octal 16 Input And-Or-Invert
PAL16R8-2	N,J,F,L	Octal 16 Input Registered And-Or
PAL16R6-2	N,J,F,L	Hex 16 Input Registered And-Or
PAL16R4-2	N,J,F,L	Quad 16 Input Registered And-Or
PAL16L8-4	N,J,F,L	Octal 16 Input And-Or-Invert
PAL16R8-4	N,J,F,L	Octal 16 Input Registered And-Or
PAL16R6-4	N,J,F,L	Hex 16 Input Registered And-Or
PAL16R4-4	N,J,F,L	Quad 16 Input Registered And-Or

Ordering Information



Monolithic Memories

CUSTOM/SEMICUSTOM

PAL® is a registered trademark of Monolithic Memories

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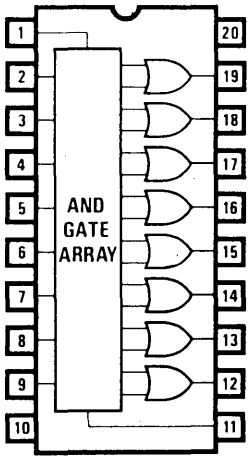
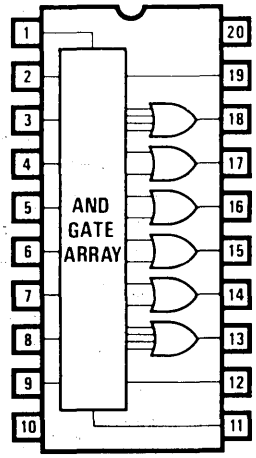
Monolithic Memories

PAL10H8-2



PAL12H6-2



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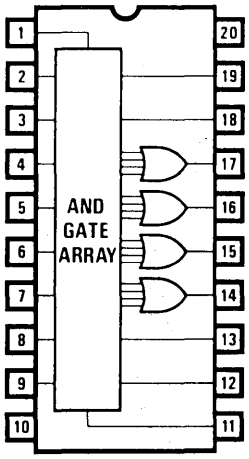

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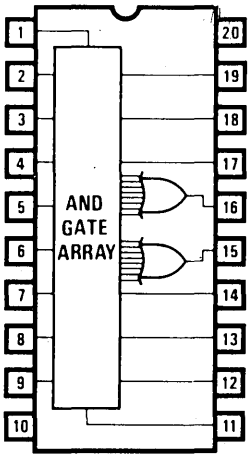

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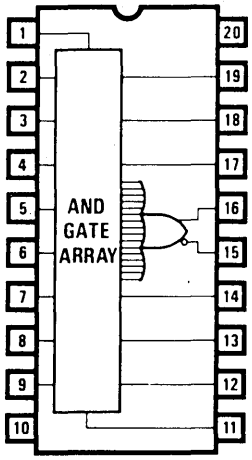

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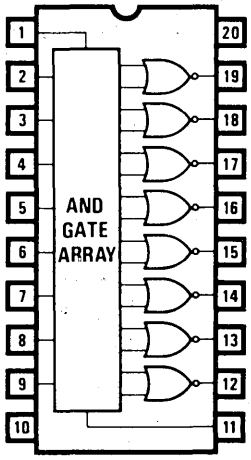
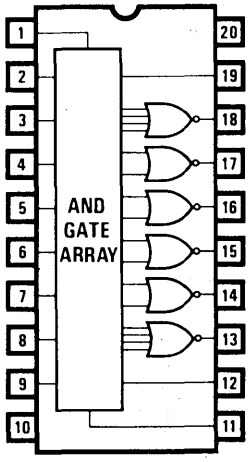


PAL12L6-2



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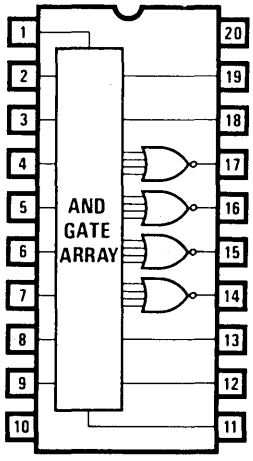
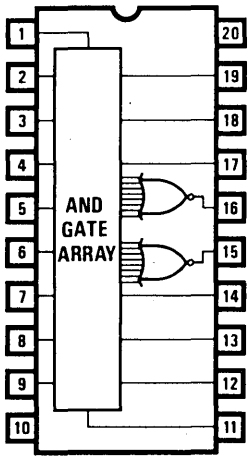


PAL16L2-2



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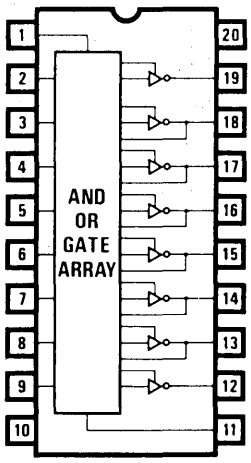

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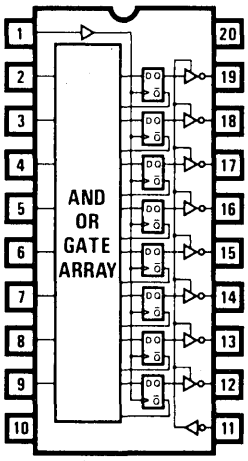

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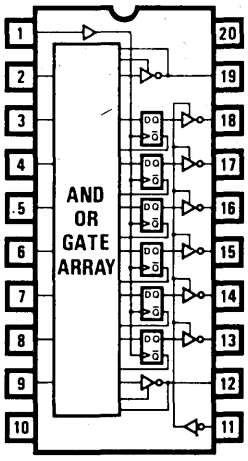

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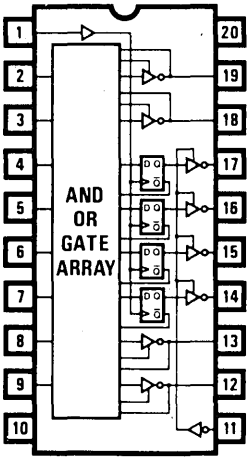

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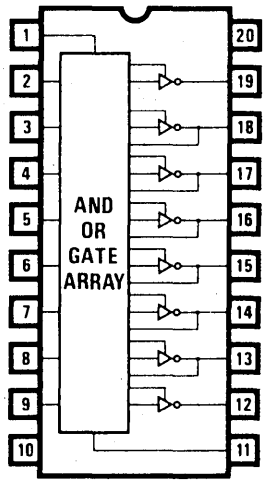
PAL16L8-4



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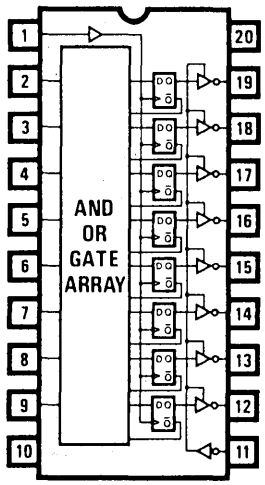

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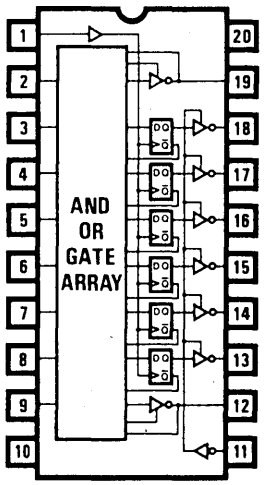

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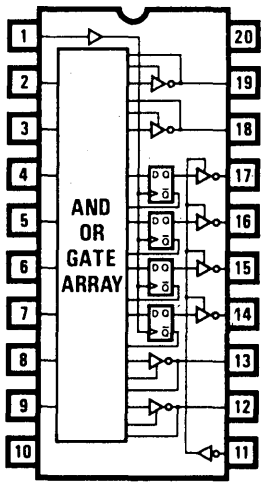

Absolute Maximum Ratings

	Operating	Programming
Supply Voltage, V_{CC}	-0.5 to 7.0V	-0.5 to 12.0V
Input Voltage	-1.5 to 5.5V	-1.0 to 12.0V⊕
Off-state output Voltage	5.5V	12.0V
Storage temperature		-65° to +150°C

Operating Conditions

SYMBOL	PARAMETER			MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage			4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	16R8-2 16R6-2 16R4-2	Low	50	25		40	25		ns
			High	50	25		40	25		
t_{su}	Set up time from input or feedback	16R8-2 16R6-2 16R4-2		70	40		55	40		ns
t_h	Hold time			0	-15		0	-15		ns
T_A	Operating free-air temperature			-55			0	5	75	°C
T_C	Operating case temperature					125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	II = -18mA			-0.8	-1.5	V
I_{IL}	Low-level input current†	V_{CC} = MAX	VI = 0.4V			-0.02	-0.25	mA
I_{IH}	High-level input current†	V_{CC} = MAX	VI = 2.4V				25	μA
I_I	Maximum input current	V_{CC} = MAX	VI = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	10L8-2 10H8-2 12L6-2 12H6-2 14L4-2 14H4-2 16L2-2 16H2-2 16C1-2	MIL I_{OL} = 4mA				V
				COM I_{OL} = 4mA		0.3	0.5	
			16L8-2 16R8-2 16R6-2 16R4-2	MIL I_{OL} = 4mA				
				COM I_{OL} = 8mA				
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	10L8-2 10H8-2 12L6-2 12H6-2 14L4-2 14H4-2 16L2-2 16H2-2 16C1-2	MIL I_{OH} = -1mA	2.4	2.8		V
				COM I_{OH} = -1mA				
			16L8-2 16R8-2 16R6-2 16R4-2	MIL I_{OH} = -1mA				
				COM I_{OH} = -1mA				
I_{OZL}	Off-state output current†	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V	16L8-2 16R8-2 16R6-2 16R4-2	V_O = 0.4V			-100	μA
I_{OZH}				V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current**	V_{CC} = 5V		V_O = 0V	-30	-70	-130	mA
I_{CC}	Supply current	V_{CC} = MAX	10H8-2 12H6-2 14H4-2 16H2-2 16C1-2 10L8-2 12L6-2 14L4-2 16L2-2			30	45	mA
			16R4-2 16R6-2 16R8-2 16L8-2			60	90	

* These are absolute voltages with respect to pin 10 on the device and includes all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

⊕ Pins 1 and 11 may be raised to 22V MAX.

** Only one output shorted at a time.

† I/O pin leakage is the worst case of I_{OZX} or I_{IX} e.g., I_{IL} and I_I

†† All typical values are at V_{CC} = 5V, T_A = 25°C.

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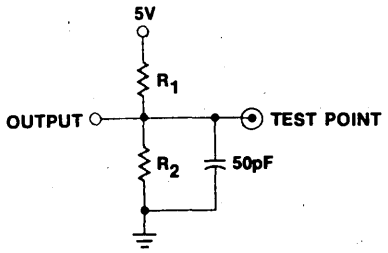
Switching Characteristics

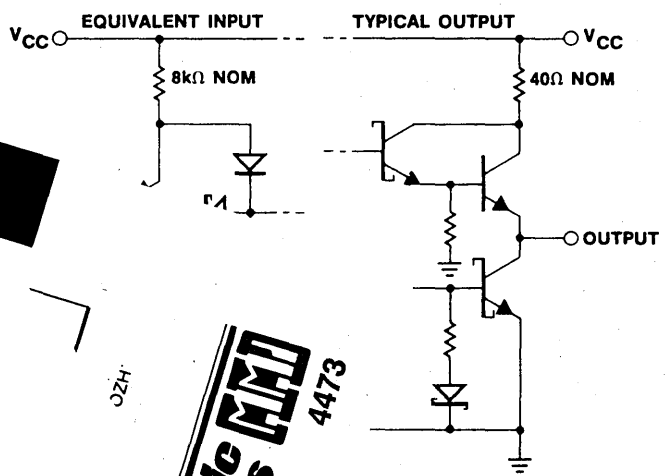
Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input to output	10H8-2 12H6-2 14H4-2 16H2-2 10L8-2 12L6-2 14L4-2 16L2-2 16C1-2	R_1 = 1.12kΩ R_2 = 2.2kΩ		45	80		45	60	ns
t_{PD}	Input or feedback to output	16R6-2 16R4-2 16L8-2	R_1 = 400Ω R_2 = 780Ω		30	65		30	50	ns
t_{CLK}	Clock to output or feedback — 2				20	50		20	40	ns
$t_{PXZ/ZY}$	Pin 11 to output disable/enable — 2				15	40		15	30	ns
t_{PZX}	Input to output enable	16R6-2 16R4-2 16L8-2			30	65		30	50	ns
t_{PXZ}	Input to output disable	16R6-2 16R4-2 16L8-2			30	65		30	50	ns
f_{MAX}	Maximum frequency	16R8-2 16R6-2 16R4-2		8	20		11	20		MHz

Test Load



Schematic of Inputs and Outputs



Available Programmers

MANUFACTURER	PERSONALITY CARD SET	SOCKET ADAPTER CONFIGURATION
Data I/O Corporation	909-1427	715 1428-1 715 1428-2 715 1428-3
Pro-Log Corporation	PM9068	
Stag Systems	PM202	AM10H8 AM10L8 AM12H6 AM12L6 AM14H4 AM14L4 AM16H2 AM16L2 AM16C1
Structured Design	SD20/24	

Absolute Maximum Ratings

	Operating	Programming
Supply Voltage, V_{CC}	-0.5 to 7.0V	-0.5 to 12.0V
Input Voltage	-1.5 to 5.5V	-1.0 to 12.0V⊕
Off-state output Voltage	5.5V	12.0V
Storage temperature		-65° to +150°C

Operating Conditions

SYMBOL	PARAMETER			MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage			4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	16R8-4 16R6-4 16R4-4	Low	70	25		50	25		ns
			High	70	25		50	25		
t_{su}	Set up time from input or feedback	16R8-4 16R6-4 16R4-4		120	45		100	45		ns
t_h	Hold time			0	-15		0	-15		ns
T_A	Operating free-air temperature			-55			0	5	75	°C
T_C	Operating case temperature					125				°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}*	Low-level input voltage						0.8	V
V_{IH}*	High-level input voltage				2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	II = -18mA			-0.8	-1.5	V
I_{IL}	Low-level input current†	V_{CC} = MAX	VI = 0.4V			-0.02	-0.25	mA
I_{IH}	High-level input current†	V_{CC} = MAX	VI = 2.4V				25	μA
I_I	Maximum input current	V_{CC} = MAX	VI = 5.5V				1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	16L8-4 16R8-4 16R6-4 16R4-4	MIL I_{OL} = 4mA		0.3	0.5	V
				COM I_{OL} = 4mA				
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	16L8-4 16R8-4 16R6-4 16R4-4	MIL I_{OH} = -1mA	2.4	2.8		V
				COM I_{OH} = -1mA				
I_{OZL}	Off-state output current†	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V	16L8-4 16R8-4 16R6-4 16R4-4	V_O = 0.4V			-100	μA
I_{OZH}				V_O = 2.4V			100	μA
I_{OS}	Output short-circuit current**	V_{CC} = 5V		VO = 0V	-30	-70	-130	mA
I_{CC}	Supply current	V_{CC} = MAX	16R4-4 16R6-4 16R8-4 16L8-4			30	50	mA

* These are absolute voltages with respect to pin 10 on the device and includes all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

⊕ Pins 1 and 11 may be raised to 22V MAX.

** Only one output shorted at a time.

† I/O pin leakage is the worst case of I_{OZX} or I_{IX} e.g., I_{IL} and I_{OZH}

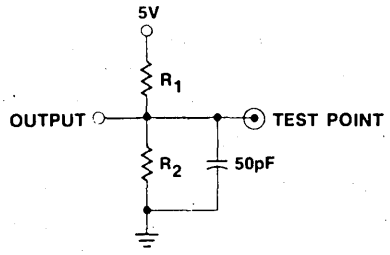
†† All typical values are at V_{CC} = 5V, T_A = 25°C.

Switching Characteristics

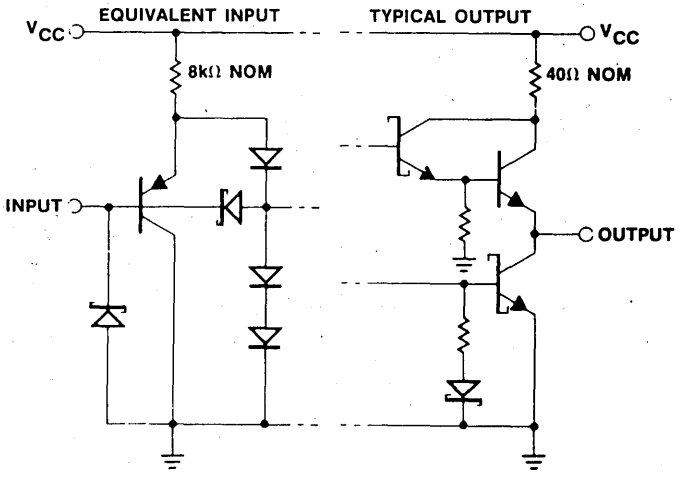
Over Operating Conditions

SYMBOL	PARAMETER		TEST	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{PD}	Input or feedback to output	16R6-4 16R4-4 16L8-4	R_1 = 800 Ω R_2 = 1.56K Ω		55	100		55	80	ns
t_{CLK}	Clock to output or feedback — 4				40	80		40	60	ns
$t_{PXZ/ZY}$	Pin 11 to output disable/enable — 4				25	50		25	40	ns
t_{PZX}	Input to output enable	16R6-4 16R4-4 16L8-4			50	100		50	75	ns
t_{PXZ}	Input to output disable	16R6-4 16R4-4 16L8-4			50	100		50	75	ns
f_{MAX}	Maximum frequency	16R8-4 16R6-4 16R4-4		5	10		7	10		MHz

Test Load



Schematic of Inputs and Outputs



Available Programmers

MANUFACTURER	PERSONALITY CARD SET	SOCKET ADAPTER CONFIGURATION
Data I/O Corporation	909-1427	715 1428-1 715 1428-2 715 1428-3
Pro-Log Corporation	PM9068	
Stag Systems	PM202	AM10H8 AM10L8 AM12H6 AM12L6 AM14H4 AM14L4 AM16H2 AM16L2 AM16C1
Structured Design	SD20/24	

1165 East Arques Avenue, Sunnyvale, CA 94086 Tel: (408) 739-3535 TWX: 910-339-9229

Programming

PAL fuses are programmed using a low-voltage linear-select procedure which is common to all 19 PAL types. The array is divided into two groups, products 0 thru 31 and products 32 thru 63, for which pin identifications are shown in Pin Configurations below. To program a particular fuse, both an input line and a product line are selected according to the following procedure:

Step 1 Raise Output Disable, OD, to V_{IHH}

Step 2 Select an input line by specifying I_0, I_1, I_2, I_3, I_4, I_5, I_6, I_7 and L/R as shown in Table 1.

Step 3 Select a product line by specifying A_0, A_1 and A_2 one-of-eight select as shown in Table 2.

Step 4 Raise V_{CC} (pin 20) to V_{IHH}

Step 5 Program the fuse by pulsing the output pins, O, of the selected product group to V_{IHH} as shown in Programming Waveform.

Step 6 Lower V_{CC} (pin 20) to 6.0 V

Step 7 Pulse the CLOCK pin and verify the output pin, O, to be Low for active Low PAL types or High for active High PAL types.

Step 8 Lower V_{CC} (pin 20) to 4.5 V and repeat step 7.

Step 9 Should the output not verify, repeat steps 1 thru 8 up to five (5) times.

This procedure is repeated for all fuses to be blown (see Programming Waveforms).

To prevent further verification, two last fuses may be blown by raising pin 1 and pin 11 to V_P. V_{CC} is not required during this operation.

Voltage Legend

L = Low-level input voltage, V_{IL}
H = High-level input voltage, V_{IH}
HH = High-level program voltage, V_{IHH}
Z = High impedance (e.g., 10kΩ to 5.0V)

INPUT LINE NUMBER	PIN IDENTIFICATION								
	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	L/R
0	HH	HH	HH	HH	HH	HH	HH	L	Z
1	HH	HH	HH	HH	HH	HH	HH	H	Z
2	HH	HH	HH	HH	HH	HH	HH	L	HH
3	HH	HH	HH	HH	HH	HH	HH	H	HH
4	HH	HH	HH	HH	HH	HH	L	HH	Z
5	HH	HH	HH	HH	HH	HH	H	HH	Z
6	HH	HH	HH	HH	HH	HH	L	HH	HH
7	HH	HH	HH	HH	HH	HH	H	HH	HH
8	HH	HH	HH	HH	HH	L	HH	HH	Z
9	HH	HH	HH	HH	HH	H	HH	HH	Z
10	HH	HH	HH	HH	HH	L	HH	HH	HH
11	HH	HH	HH	HH	HH	H	HH	HH	HH
12	HH	HH	HH	HH	L	HH	HH	HH	Z
13	HH	HH	HH	HH	H	HH	HH	HH	Z
14	HH	HH	HH	HH	L	HH	HH	HH	HH
15	HH	HH	HH	HH	H	HH	HH	HH	HH
16	HH	HH	HH	L	HH	HH	HH	HH	Z
17	HH	HH	HH	H	HH	HH	HH	HH	Z
18	HH	HH	HH	L	HH	HH	HH	HH	HH
19	HH	HH	HH	H	HH	HH	HH	HH	HH
20	HH	HH	L	HH	HH	HH	HH	HH	Z
21	HH	HH	H	HH	HH	HH	HH	HH	Z
22	HH	HH	L	HH	HH	HH	HH	HH	HH
23	HH	HH	H	HH	HH	HH	HH	HH	HH
24	HH	L	HH	HH	HH	HH	HH	HH	Z
25	HH	H	HH	HH	HH	HH	HH	HH	Z
26	HH	L	HH	HH	HH	HH	HH	HH	HH
27	HH	H	HH	HH	HH	HH	HH	HH	HH
28	L	HH	HH	HH	HH	HH	HH	HH	Z
29	H	HH	HH	HH	HH	HH	HH	HH	Z
30	L	HH	HH	HH	HH	HH	HH	HH	HH
31	H	HH	HH	HH	HH	HH	HH	HH	HH

Table 1 Input Line Select

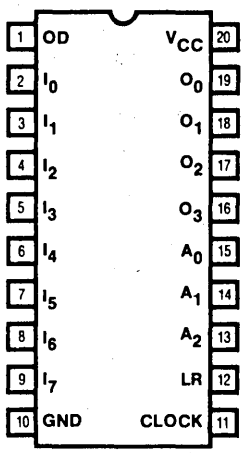
PRODUCT LINE NUMBER	PIN IDENTIFICATION						
	O_3	O_2	O_1	O_0	A_2	A_1	A_0
0, 32	Z	Z	Z	HH	Z	Z	Z
1, 33	Z	Z	Z	HH	Z	Z	HH
2, 34	Z	Z	Z	HH	Z	HH	Z
3, 35	Z	Z	Z	HH	Z	HH	HH
4, 36	Z	Z	Z	HH	HH	Z	Z
5, 37	Z	Z	Z	HH	HH	Z	HH
6, 38	Z	Z	Z	HH	HH	HH	Z
7, 39	Z	Z	Z	HH	HH	HH	HH
8, 40	Z	Z	HH	Z	Z	Z	Z
9, 41	Z	Z	HH	Z	Z	Z	HH
10, 42	Z	Z	HH	Z	Z	HH	Z
11, 43	Z	Z	HH	Z	Z	HH	HH
12, 44	Z	Z	HH	Z	HH	Z	Z
13, 45	Z	Z	HH	Z	HH	Z	HH
14, 46	Z	Z	HH	Z	HH	HH	Z
15, 47	Z	Z	HH	Z	HH	HH	HH
16, 48	Z	HH	Z	Z	Z	Z	Z
17, 49	Z	HH	Z	Z	Z	Z	HH
18, 50	Z	HH	Z	Z	Z	HH	Z
19, 51	Z	HH	Z	Z	Z	HH	HH
20, 52	Z	HH	Z	Z	HH	Z	Z
21, 53	Z	HH	Z	Z	HH	Z	HH
22, 54	Z	HH	Z	Z	HH	HH	Z
23, 55	Z	HH	Z	Z	HH	HH	HH
24, 56	HH	Z	Z	Z	Z	Z	Z
25, 57	HH	Z	Z	Z	Z	Z	HH
26, 58	HH	Z	Z	Z	Z	HH	Z
27, 59	HH	Z	Z	Z	Z	HH	HH
28, 60	HH	Z	Z	Z	HH	Z	Z
29, 61	HH	Z	Z	Z	HH	Z	HH
30, 62	HH	Z	Z	Z	HH	HH	Z
31, 63	HH	Z	Z	Z	HH	HH	HH

Table 2 Product Line Select

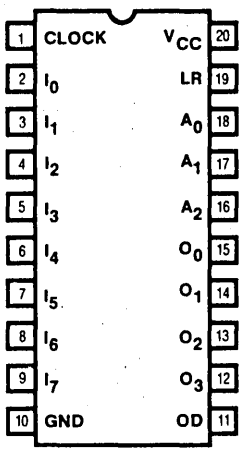
1165 East Arques Avenue, Sunnyvale, CA 94086 Tel: (408) 739-3535 TWX: 910-339-9229

Pin Configurations

PRODUCTS 0 THRU 31



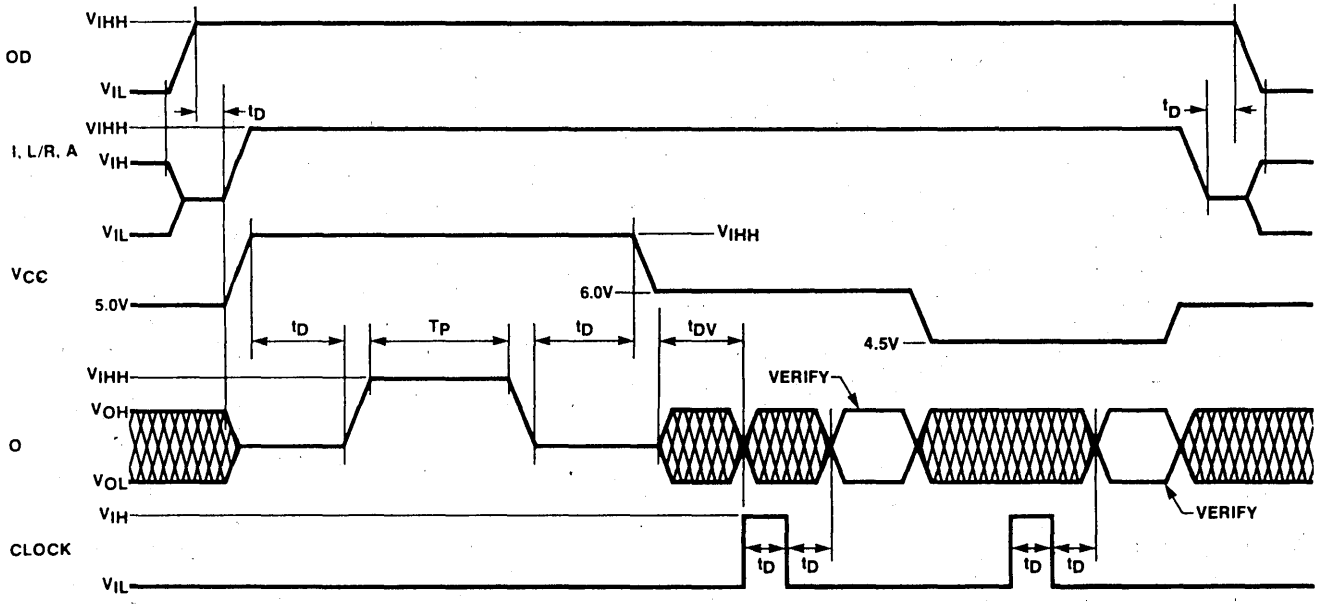
PRODUCTS 32 THRU 63



Programming Parameters $T_A = 25°C$

SYMBOL	PARAMETER		LIMITS MIN	TYP	MAX	UNIT
V_{IHH}	Program-level input voltage		11	11.5	12	V
I_{IHH}	Program-level input current	Output Program Pulse			50	mA
		OD, L/R			25	
		All Other Inputs			5	
I_{CCH}	Program Supply Current				400	mA
T_P	Program Pulse Width		10		50	μs
t_D	Delay time		100			ns
t_{DV}	Delay Time to Verify		100			μs
	Program Pulse duty cycle				25	%
V_P	Verify-Protect-input voltage		20	21	22	V
I_P	Verify-Protect-input current				400	mA
T_{PP}	Verify-Protect Pulse Width		20		50	msec

Programming Waveforms



MOTOROLA

FOR CUSTOM LSI/VLSI BIPOLAR CIRCUITS

The Expanding Motorola Macrocell Family

Parameter	MCA 600ECL	MCA 1200ECL	MCA 2500ECL	MCA 1000R ECL	MCA 500ALS	MCA 1300ALS	MCA 2800ALS
Maximum Gate Equivalent	625	1192	2472	960	533	1280	2720
Major Macrocells	24	48	110	40	24	60	130
Input/Interface Cells	25	32	—	—	26	40	120 I/O
Output Macrocells	18	26	68	40	24	40	
Memory Bits	—	—	—	512	—	—	—
Maximum Gate Delay	1.2	1.2	0.5	0.5	4.0	4.0	1.6
Maximum Toggle Freq.	160	160	300	300	50	50	80
Power Dissipation	2.5	4.0	8	8	1.0	1.6	2.5
Package: Dual-In-Line	28,40	—	—	—	28,48	40,48	—
Package: Chip Carrier	68	68	149	149	68	68,84	84,149
Temperature Range	0–70	0–70	0–70	0–70	0–70	0–70	0–70
I/O Interface	10K	10K	10KH/100K	10KH/100K	TTL/ALS	TTL/ALS	TTL/ALS
Design Interface	CAD	CAD	CAD	CAD	CAD	CAD	CAD
Availability	Now	Now	4Q82	1Q83	Now	Now	1Q83

M10900 FAMILY

The M10900 family is a series of very high performance bipolar LSI products designed off the MECL Macrocell Array offering. While the Macrocell Array is normally used for custom circuits which require option development time and costs, the M10900 family is a standard product ordered like any other MECL 10,000 circuit.

MC10900Z — 8-Bit ALU with Parity
MC10901Z — 8 x 8 Bit Expandable Multiplier
MC10902Z — 8-Bit BCD/Binary ALU
MC10904Z — Micro-Code Sequencer
MC10905Z — Error Detect and Correct

Macrocell Array Literature — Available from Motorola Semiconductor Sales Offices.

Order No.	Title
BR-107	Design Manual-MECL 10,000 Macrocell Arrays
BR-110	Design Manual-High Performance TTL Macrocell Arrays
BR-112	Brochure-High Performance TTL Compatible Macrocell Arrays
By Full Title	Motorola Regional Computer-Aided Design Center
By Full Title	Macrocell Arrays — An Alternative to Custom LSI
By Full Title	Remote CAD System Helps Designers Develop Custom VLSI Chips
AN-874	Macrocell Arrays: Concept-Features-CAD Interface

MACROCELL ARRAY

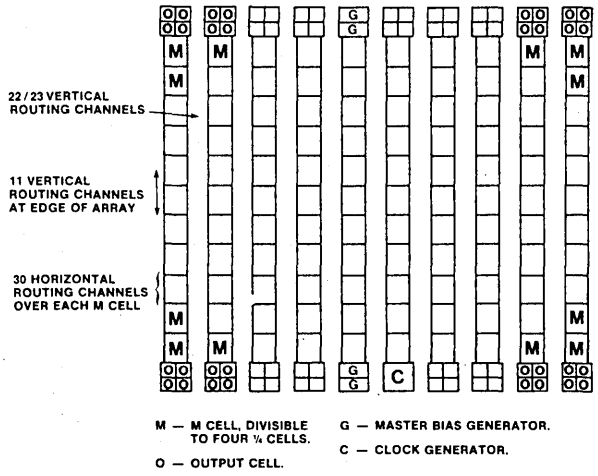
Motorola's Macrocell Array products provide a means for economical custom LSI/VLSI logic circuits. Performance is achieved by the combination of an advanced MOSAIC (Motorola Oxide Isolated Self-Aligned Implanted Circuit) bipolar integrated circuit process and a series gated emitter-coupled logic (ECL) macrocell circuit technology.

In ALS-TTL arrays, a series of input and output circuits provide level translation from the ECL macrocells to the outside TTL world.

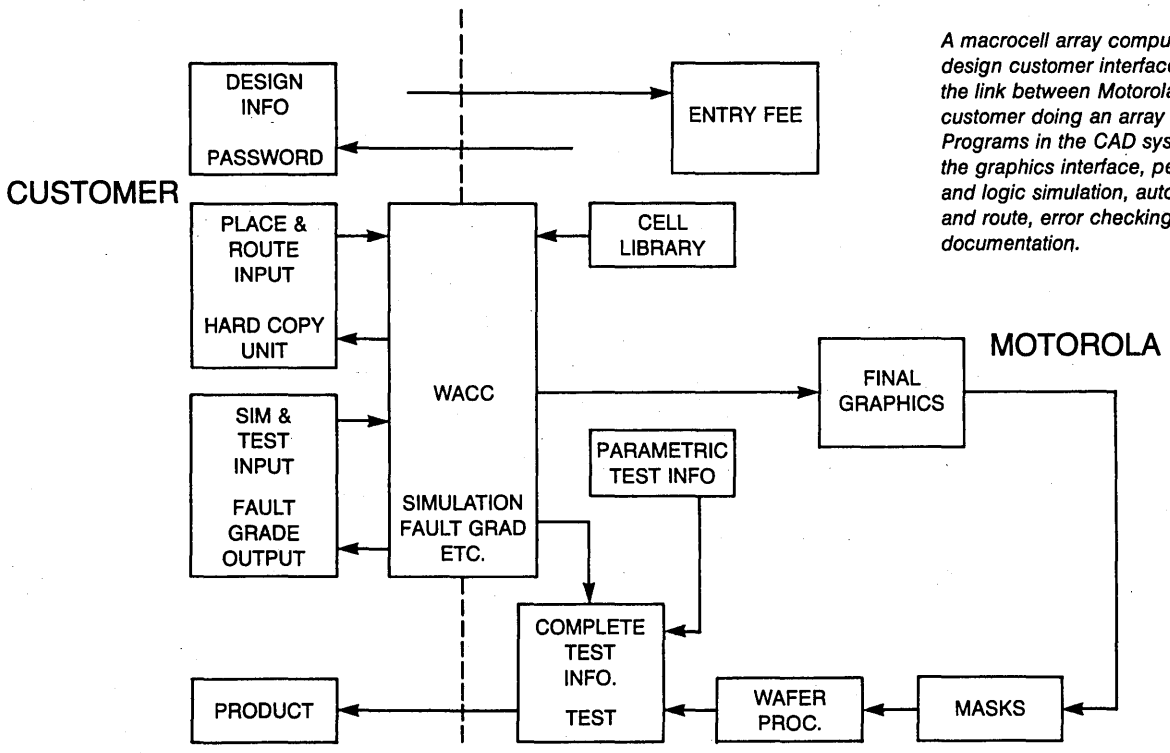
Advantages of the macrocell array concept include:

1. Proprietary custom LSI circuits.
2. Quick design turn-around time. Normally within 7 weeks!
3. MSI complexity macrocell logic blocks rather than basic gates.
4. Computer Aided Design (CAD) csutomer interface.
5. Family of array complexities, so the cost, performance, power dissipation and package can be optimized to match the system need.
6. Common macrocell library, design rules and CAD interface for all arrays.

MCA2500ECL MACROCELL ARRAY LAYOUT



The CAD Interface System



A macrocell array computer aided design customer interface provides the link between Motorola and a customer doing an array option. Programs in the CAD system handle the graphics interface, performance and logic simulation, automatic place and route, error checking, and documentation.

National Semiconductor

Custom Capabilities

National Semiconductor has been meeting the need for efficient, reliable, CUSTOM MOS/LSI design and fabrication since 1975. Our fabrication expertise makes us a logical source for CUSTOM MOS/LSI circuits, whether of our design or produced from customer-owned tooling. (COT).

WHY USE CUSTOM?

Today's multifaceted electronics industry presents several approaches to systems design, including discrete, integrated and programmable circuitry. How can designers determine which will be the most effective for implementing a distinctive system?

For many applications, standard integrated circuits may be inappropriate. The tradeoffs between board real estate, power consumption, complexity, and reliability must somehow be measured in terms of system cost reduction coupled with confidentiality.

One approach, large scale integration (LSI), incorporates thousands of electronic functions into a single chip, reducing the number of components required in a system. A variety of standard LSI circuits are available through distribution, and they will allow fast development of many standard systems. A unique design, however, could require several standard circuits, wasting much of the capability of each. As system complexity and unit volume increase, a more space and cost-effective solution will need to be found.

System cost reductions begin with grouping functions that require numerous components into one or two CUSTOM LSI chips. As the component count is lowered, the number of electrical interconnections is lessened. This results in a reduction in:

- troubleshooting time and cost
- initial checkout costs
- assembly costs
- field repairs and warranty costs

and an increase in product reliability.

Lower costs mean improved profits. A custom chip is invariably less expensive than off-the-shelf or semi-custom because you do not pay for unused capabilities. In addition, many of the costs associated with handling, assembly and inspection are eliminated. The more complex your product, the more profitable a high density custom chip can be.

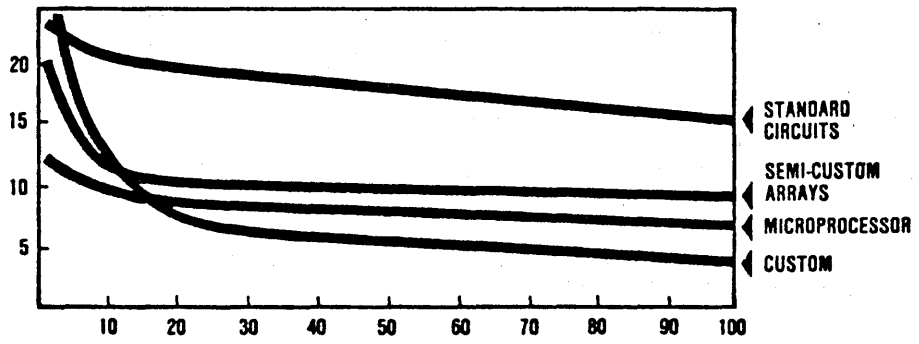
When design expenses are amortized, the total cost per average chip declines dramatically with volume. As demonstrated in this break-even graph, the CUSTOM MOS/LSI approach becomes cost-effective above 20 thousand units annually.

EXCLUSIVITY BROADENS AND PROTECTS MARKET SHARE!!

A CUSTOM LSI circuit requires less space and often less power than a series of discrete components. Design and style options are wider, and problems associated with heat dissipation are reduced. This gives you a real competitive edge.

National Semiconductor's advanced process technologies let you design exciting features into your circuit which might otherwise be impossible or too costly for advantageous pricing. Our broad product line allows us to offer you a wide selection of fabrication processes that is difficult to find elsewhere in the industry.

Technology					
Silicon Gate			Metal Gate		
CMOS	single poly	3μ	CMOS	(guard band)	7μ
	single poly	4μ			
	dual poly	3μ		(field implant)	7μ
	dual poly	4μ			
	dual metal	4μ			
NMOS		5μ	NMOS		5μ
XMOS	(HMOS)	3μ	PMOS		8μ



This versatility allows us to use the most economical process for your circuit. Our vast experience is available to you throughout the development of your circuit. National Semiconductor's custom design group is prepared to work with your organization on any level, whether we design a circuit from your specifications or fabricate it from your tooling.

A PRODUCTIVE PARTNERSHIP

An increasing number of systems manufacturers prefer to design their own custom circuits, or refer the design to an engineering consulting firm. Others, especially high volume users, may already have a circuit in production and are seeking the security of a second manufacturing source. In any case, National Semiconductor is a logical choice for fabricating, assembling and testing circuits from customer-owned tooling.

The following responsibility and flow diagrams indicate the role played by you, the customer, and/or your designated design house (it can be your own in-house design team, an outside consultant, or NSC), and National Semiconductor as your silicon foundry.

Our design specialists are available for consultation with either your staff or an independently contracted design firm—at any point in the development cycle.

NATIONAL SEMICONDUCTOR — BECAUSE YOUR SYSTEMS ARE DISTINCTIVE

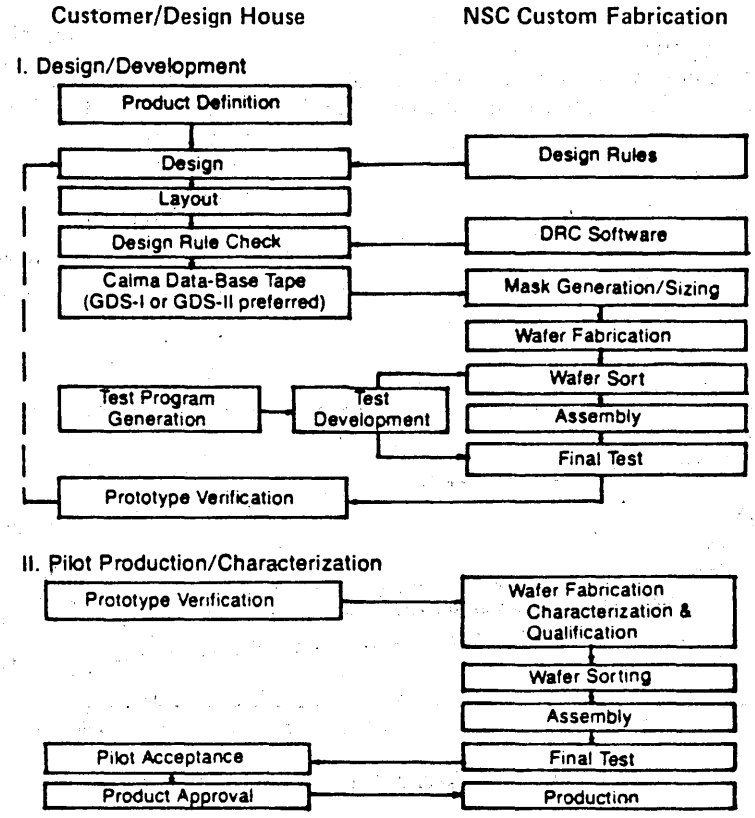
National Semiconductor's CUSTOM LSI circuits have helped many large and small companies meet the increasing demand for compact, sophisticated electronic products. We're ready to devote our vast knowledge and experience to designing and/or fabricating high-quality, reliable, cost-effective custom circuitry for your systems. With your success as our goal, we'll dedicate our resources to your needs and hope that you will consider us as your own semiconductor facility.

These resource facilities include:

- Ability to perform as our own second source through multiple fabrication and assembly facilities
- 5″ wafer fabrication facilities
- Dedicated design engineering
- Dedicated product engineering
- Dedicated CAD/CAM design
- Remote CAD/CAM hook-up (via MODEM)
- 3 design centers (U.S. and Europe)
- Cell Array library
- Dedicated assembly and test
- Dedicated marketing staff

Let's get together now to develop the right program for your company. Call your National sales representative or one of our field applications engineers—or contact us directly at one of our offices—to arrange a preliminary meeting.

Custom Fabrication Responsibilities



National Semiconductor

PRELIMINARY
October 1982

SCX Gate-Array Design Automation System

Product Overview

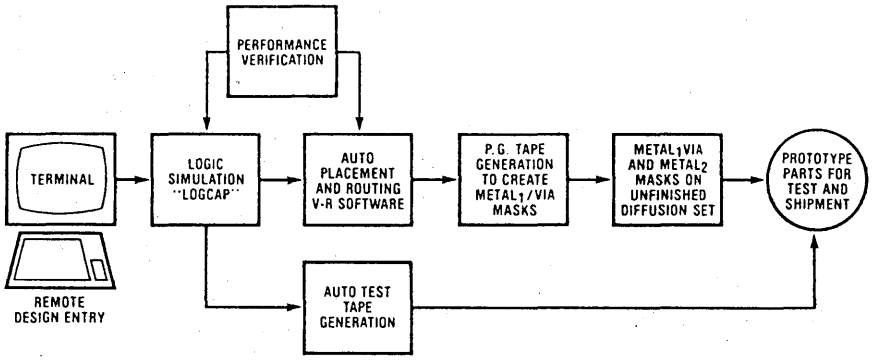
The objectives of National's Gate Array Design Automation System are

- To achieve automated layouts of complex logic circuits by using "macrocells" from the reference library with 2-layer metal interconnects.
- Automatic cell placement and high-yield interconnect routing.
- To provide automatic layout and logic verification for error-free designs.

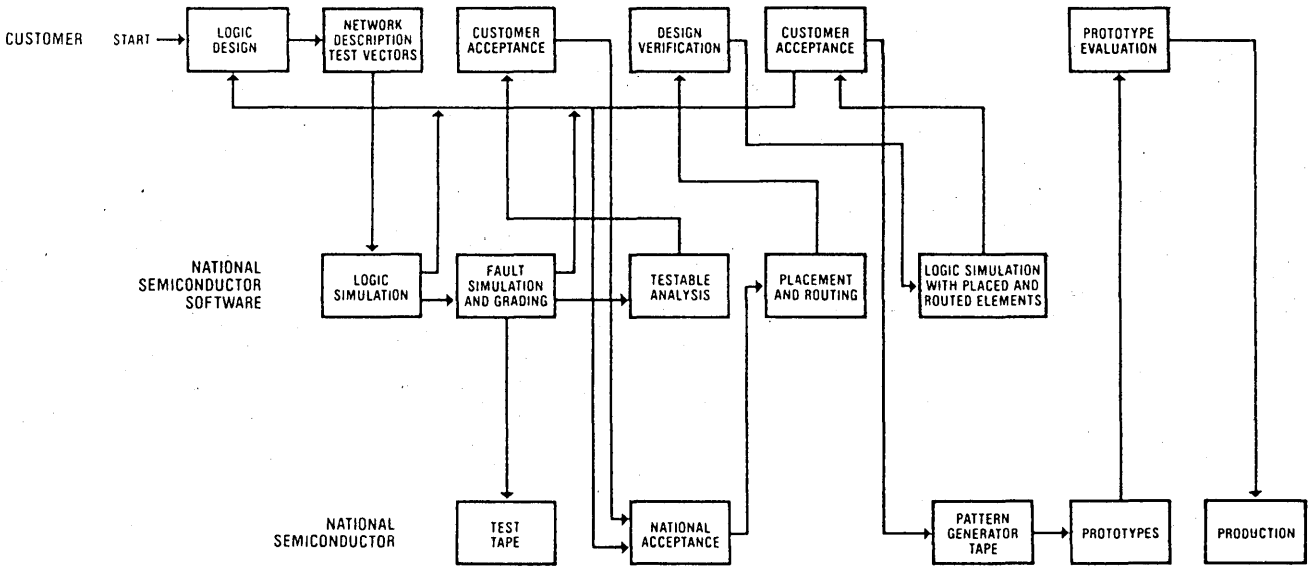
Features

- Graphics entry
- Logic simulation
- Fault grading
- Testability analysis
- Automatic placement
- Automatic routing
- Performance verification
- P.G. tape compatibility

Development System for Gate-Arrays Diagram



Design Automation System



September 1982

SCX 6324A High-Performance 2.4k CMOS Gate Array Macro Library Specifications

General Description

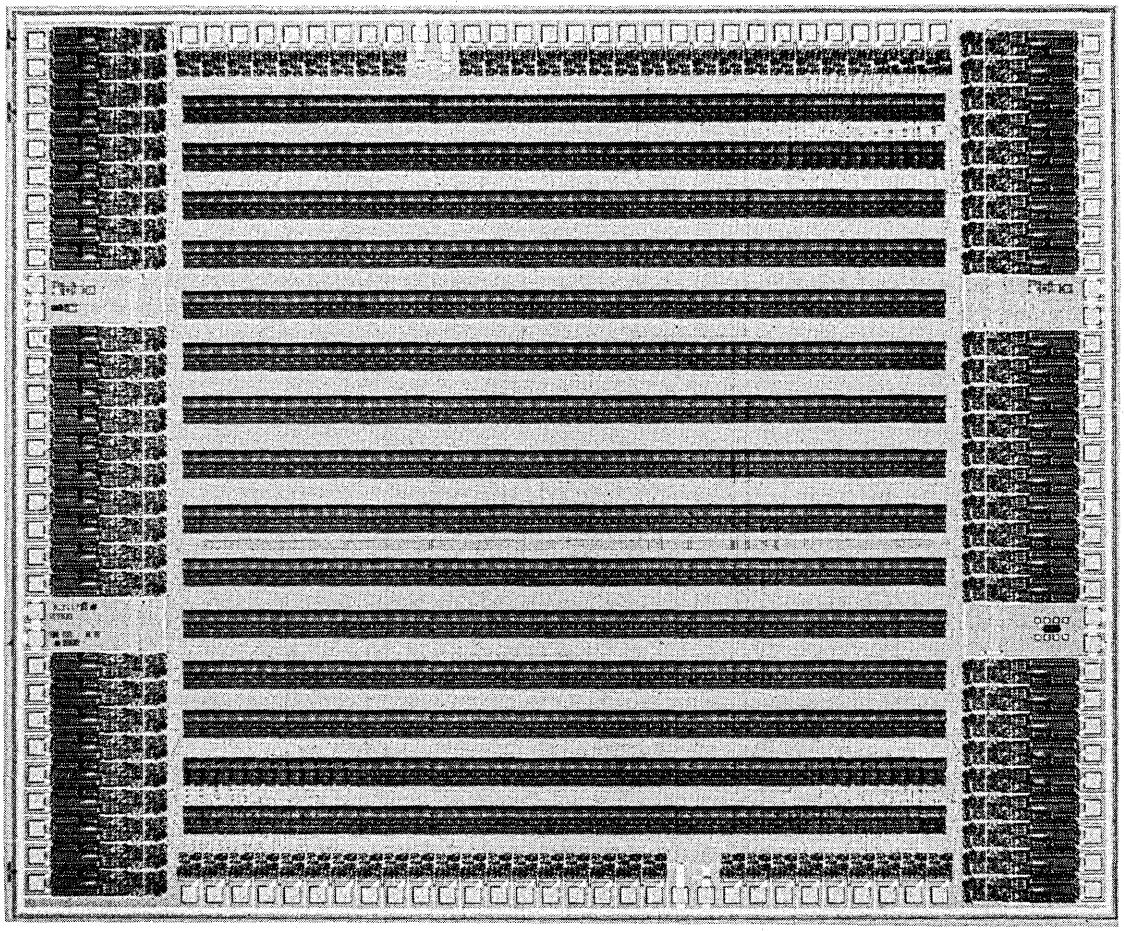
This versatile 2.4k gate array utilizes silicon-gate dual-layer metal CMOS (M^2CMOS) technology to achieve operating speeds similar to S-TTL with the inherent lower power consumption of standard CMOS integrated circuits. All outputs have the ability to drive 10 LSTTL loads. All inputs have high noise immunity and are protected from damage due to static discharge.

To enhance user applications, the device is offered in three attractive 124-pin package options. Smaller pin count packages are available upon request.

Features

- 2.4k gates
- 2.0ns internal t_{PD}
- CMOS power dissipation
- "LS" drive capability
- Full design automation support
  - —80% utilization
  - —100% auto place and route
- 124 pins maximum
  - —55 inputs
  - —56 I/Os
  - —6 V_{DD}
  - —6 V_{SS}
  - —1 test

SCX 6324A Topology



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DA-B25M92/Printed in U.S.A.

SCX 6324A High-Performance 2.4k CMOS Gate Array
Macro Library Specifications

National Semiconductor

SCX 6324A

Absolute Maximum Ratings

Supply Voltage	−0.5 to 7V
Input or Output Voltage	−0.5 to V_{CC}+0.5V
Storage Temperature	−65°C to 150°C
Power Dissipation (Package Dependent)	1W
Lead Temperature	300°C

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	DC Supply Voltage	3	6	V
V_I, V_O	Input or Output Voltage	0	V_{CC}	V
I_O	High or Low Level Output Current	0	±25	mA
I_{CC}	V_{CC} or Ground Current per pad	0	±50	mA
T_A	Operating Temperature Range	−40	+85	°C

DC Electrical Characteristics

V_{CC} = 5V ± 10%, Min./Max. limits apply across temperature unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{IH}	High Level Input Voltage	V_O = 0.5V or V_{CC}−1V, $\|I_O\|$ = 1μA	V_{CC} − 1.4		V
V_{IL}	Low Level Input Voltage	V_O = 0.5V or V_{CC}−1V, $\|I_O\|$ = 1μA		0.9	V
V_{OH}	High Level Output Voltage	V_I = V_{CC} or GND, $\|I_O\|$ = 1μA	V_{CC}−0.05	V	
V_{OL}	Low Level Output Voltage	V_I = V_{CC}or GND, $\|I_O\|$ = 1μA		0.05	V
I_{OH}	High Level Output Current	V_I = V_{CC} or GND, V_O = V_{CC}−0.8V	−4		mA
I_{OL}	Low Level Output Current	V_I = V_{CC} or GND, V_O = 0.4V	4		mA
$V_{IH_{TTL}}$	Min. High Level TTL i/p voltage (for TTL i/p option)	V_O = 0.5V or V_{CC}−1V, $\|I_O\|$ = 1μA	2		V
$V_{IL_{TTL}}$	Max. Low Level TTL i/p voltage (for TTL i/p option)	V_O = 0.5V or V_{CC}−1V, $\|I_O\|$ = 1μA		0.8	V
I_I	Input Current (without pull-up resistor)	V_I = V_{CC} or GND		±1	μA
I_{CC}	Supply Current	V_I = V_{CC} or GND, T_A = 25°C		100	μA

AC Electrical Characteristics

V_{CC} = 5V at 25°C.

Symbol	Parameter	Conditions	Min.	Max.	Unit
t_{PLH} t_{PHL}	Output buffer (Non-inverting, non-TRI-STATE®)	t_r = t_f = 5ns, 0-5V C_L = 15pF		6 6	ns ns
t_{PLH} t_{PHL}	Input Buffer (TTL type — non-inverting)	t_r = t_f = 5ns, 0-3V C_L = 1pF		4 6	ns ns
t_{PLH} t_{PHL}	Input Buffer (CMOS type — inverting)	t_r = t_f = 5ns, 0-5V C_L = 1pF		3 2	ns ns
t_{PLH}, t_{PHL}	Output TRI-STATE (Non-inverting)	t_r = t_f = 5ns		8	ns
t_{PZL} t_{PZH}		0-5V C_L = 50pF Delays measured at 50% point between start and target voltage		9 7	ns ns
t_{PLZ}, t_{PHZ}		R_L = 1kΩ		21	ns
t_{PLH}	Internal 2 i/p NAND	t_r = t_f = 5ns		3.2	ns
t_{PHL}		0-5V, load equivalent to fanout of 3 and 100 mils of interconnect		3.5	ns
t_{PHL}, t_{PLH}		As above with C_L = 0pF		1.2	ns

Packaging

Two 124-pin packages are available

1. Ceramic Chip Carrier
2. Plastic Chip Carrier

A 120-pin area grid package is also available and package options down to a 48-pin dual-in-line are available.

The area grid packaging provides rapid turn-around capability to the user. This package type consumes less board area.

Chip carriers provide "footprint" compatible alternatives to the user, enabling fast building of prototypes with ceramic and less expensive production parts with plastic.

Power Dissipation

Power dissipation is a function of clock rate and circuit configuration. For power dissipation estimation purposes, the value 35μW/GateMHz can be used for gates within the array. Note: Output buffers driving large capacitive loads at high bit rates generally tend to dominate the power consumption of most options.

Array Organization

The array has 795 cells organized in 15 columns of 53 cells per column. With three 2-input gates per cell, there are 2385 total gates (795 × 3). To guarantee routeability of a user's chip system or "option," it is recommended that not more than 80% of the cells be used, which equals 1906 gates. The routeability is, of course, dependent upon the specific logic implemented.

Load Factor: A load factor of one, equal to 0.155pF, is equivalent to driving a single inverter (P- and N-channel transistors). Some macro inputs have load factors greater than 1, i.e., total capacitance on any input equals load factor multiplied by 0.155pF.

Library of Macro Cells

The following is a list of "hardware" macros from which the user may select functions to implement his system. The intracellular wiring of these macros is constant regardless of where they appear in the array. NSC plans to expand the library to cover 80 macros. In addition to this list, "software" macros having functions such as counters, shift registers, arithmetic logic, and other large functions composed of many cells will be available to the user via the NSC CAD software. The cells comprising these "software" macros may have varying spatial relationships to each other from chip to chip.

Truth Table

TMC	DT	TSTC	Output Conditions
L	X	H	TRI-STATE
L	H	L	L
L	L	L	H
H	← NO TEST MODE →		

Hardware Macro Library

Macro	Macro Type	Qty. of Elements/ Cells	Page Number
NAND, Triple 2-Input	S1	3/1	5
NAND, Dual 2-Input plus complement	S3	2/1	6
NAND, Dual 3-Input	S2	2/1	5
NAND, Triple 3-Input plus complement	D3	3/2	11
NAND, Triple 4-Input	D1	3/2	10
NAND, 5-Input	D2	1/2	10
NOR, Triple 2-Input	S4	3/1	6
NOR, Dual 2-Input plus complement	S6	2/1	7
NOR, Dual 3-Input	S5	2/1	6
NOR, Triple 3-Input plus complement	D6	3/2	12
NOR, Triple 4-Input	D4	3/2	11
NOR, 5-Input	D5	1/2	11
XOR, 2-Input	S11	1/1	8
AND-NOR, 2-2 with complement	S15	1/1	9
OR-NAND, 2-2 with complement	S14	1/1	9
LATCH, 2-Input NAND R-S with 2-I NAND	S12	1/1	8
LATCH, 2-Input NOR R-S with 2-I NOR	S13	1/1	9
D-FLIP-FLOP	D9	1/2	12
D-FLIP-FLOP with Set and Reset	T1	1/3	13
INVERTER, Quad	S8	4/1	7
BUFFER, CLOCK Triple	S7	3/1	7
BUFFER, Dual TRI-STATE® INVERTING	S9	2/1	7
BUFFER, TRI-STATE NON-INVERTING	S10	1/1	8
MUX, 2→1	S16	1/1	10

Library of Input Cells

Input Cell	Macro Type	Page Number
Input Buffer, Non-inverting, TTL IN with pull-up resistor	I 1	13
Input Buffer, Non-inverting, TTL IN without pull-up resistor	I 2	14
Input Buffer, Inverting, CMOS IN with pull-up resistor	I 3	14
Input Buffer, Inverting, CMOS IN without pull-up resistor	I 4	14
*Input Buffer, Short circuit with pull-up resistor	I 5	14
*Input Buffer, Short circuit without pull-up resistor	I 6	14

On-Chip Test Circuit

All options of the SCX 6324 are provided with an on-chip test circuitry at the cost of a single input pin, to create TEST MODE. With this pin active (LOW), two additional pre-defined inputs are jointly employed to force all outputs to HIGH, LOW or HI-Z states and thus reduce test time in gathering output parametrics at sort. These two pins further function as conventional (either TTL or CMOS) inputs (when TEST MODE, HIGH) with no performance penalty apparent to the user in terms of AC or DC performance.

TEST MODE (TMC): A low at this input will activate the test circuitry. All output buffers are to be driven by TEST DATA (DT) and TRI-STATE (TEST) pins.

TRI-STATE (TSTC): A HI at this input together with TMC low puts all TRI-STATE output buffers to HI-Z state.

TEST DATA (DT): Input to this pin, with TMC low, forces all outputs to either high or low (reversed polarity).

SCX 6324A

Library of I/O Cells

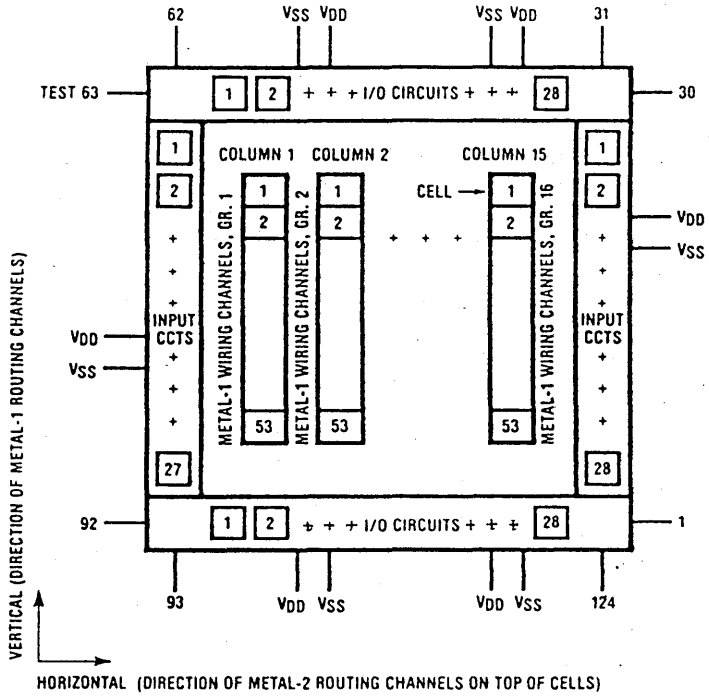
I/O Cell	Macro Type	Page Number
I/O Buffer, TRI-STATE® Output, TTL Input without pull-up resistor	I/O 1	15
I/O Buffer, TRI-STATE Output, CMOS Input without pull-up resistor	I/O 2	16
I/O Buffer, TRI-STATE Output, Short Circuit Input without pull-up resistor	I/O 3	17
Non-inverting, CMOS Output	I/O 4	17
Non-inverting, TTL Input with pull-up resistor	I/O 6	18
Non-inverting, TTL Input without pull-up resistor	I/O 7	18
Inverting, CMOS Input with pull-up resistor	I/O 8	18
Inverting, CMOS Input without pull-up resistor	I/O 9	19
*Short Circuit Input with pull-up resistor	I/O 10	19
*Short Circuit Input without pull-up resistor	I/O 11	19
I/O Buffer, TRI-STATE Output, TTL Input with pull-up resistor	I/O 12	20
I/O Buffer, TRI-STATE Output, CMOS Input with pull-up resistor	I/O 13	21
*I/O Buffer, TRI-STATE Output, Short Circuit Input with pull-up resistor	I/O 14	22

*Short circuit inputs may not be employed without written approval from a National Semiconductor design center

Future Additional Macros:

- Full adder
- 2-Bit magnitude comparator
- 4-Bit PI/SO shift register
- 4-Bit SI/SO, PO shift register
- Schmitt trigger
- 4-to-1 TRI-STATE® MUX with enable
- 4-bit parity checker
- "D" latch with reset, enable
- 1-to-4 decoder with enable
- "D" flip-flop with reset, preset
- Toggle enable flip-flop with reset
- JK flip-flop with set, reset
- Up/down counter with set, preset
- 4-to-1 data MUX
- MUX'd "D" flip-flop with reset
- 1-Bit ALU

SCX 6324A Routing Resource Distribution



1. Number of Vertical Tracks in Metal — 1 Layer:

Channel Group No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Track Quantity	15	16	16	17	18	19	20	21	21	20	19	18	17	16	16	15

Total = 284

2. Number of Horizontal Tracks in Metal — 2 Layers:

558 Tracks = (53 cells × 10 tracks/cell) + (2 ends × 14 tracks)

National Semiconductor

National Semiconductor
Application Note 320
I.R. Mackintosh
R. Sowell
B. Cheng
M. Rohm
October 1982

PRELIMINARY

A 2.4k CMOS Gate Array

Abstract. *This paper describes a 2.4k CMOS gate array and comments upon design considerations incorporated in its definition. An evaluation is made of the effects of simultaneous switching of outputs, with inductive parasitics considered.*

Die organization is described and key features of the M²CMOS™ process provided. Fabrication on a dual-layer, Si-gate process allows users to define options by programming metal 1, metal 2 and second contact. These options (or personalizations) are created employing fully automated routing and placement software.

INTRODUCTION

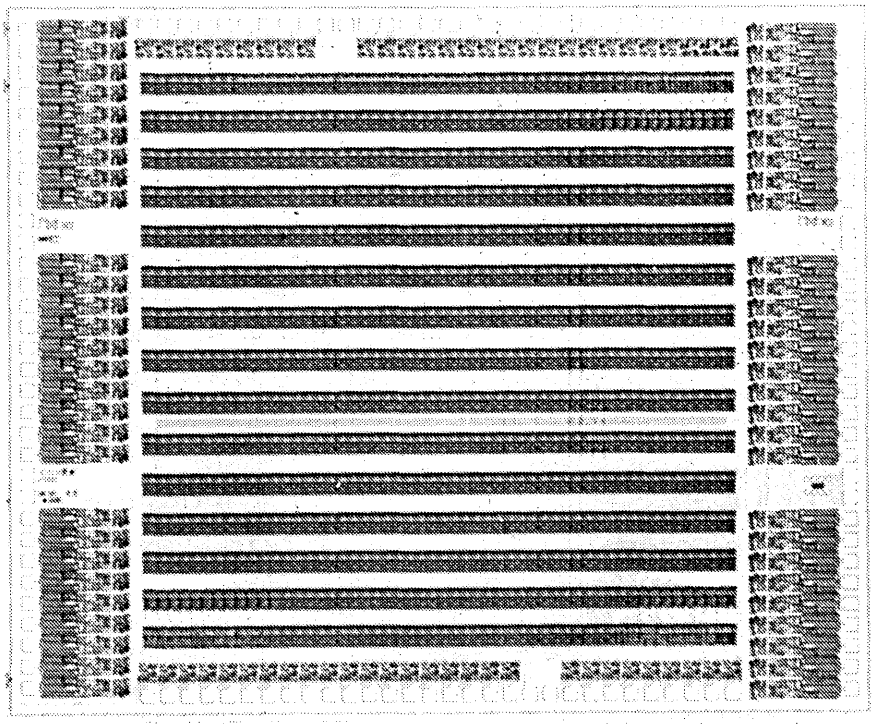
A broad base of information is provided to illustrate the total integration required in the definition of array products which almost uniquely require consideration of software capabilities, available process, packaging restrictions/limitations and system applications.

DIE ORGANIZATION

A photograph of the die is provided in *Figure 1*; this particular option was implemented as a characterization vehicle. The die is organized in 15 columns of basic elements, with 53 such elements in each column. As three 2-input gates can be created in each cell, there are approximately 2.4k gates available in the array itself. In addition to this, there are a total of 56 I/O sites and 55 inputs.

Routing channels are allocated such that metal 1 channels occur between the vertical columns of cells and metal 2 routes across the die, passing over the columns. The number of metal 1 channels is biased such that more occur between the individual columns of elements toward the die center, where demand for available resources is greatest.

The basic cell is shown in *Figure 2*. This element is preprogrammed for the user in metal 1 to create the individual logic configurations available in the library. All logic functions are built from unit multiples of this element.



TL/U/5124-1

FIGURE 1. Die Photomicrograph

M²CMOS™ is a trademark of National Semiconductor Corp.

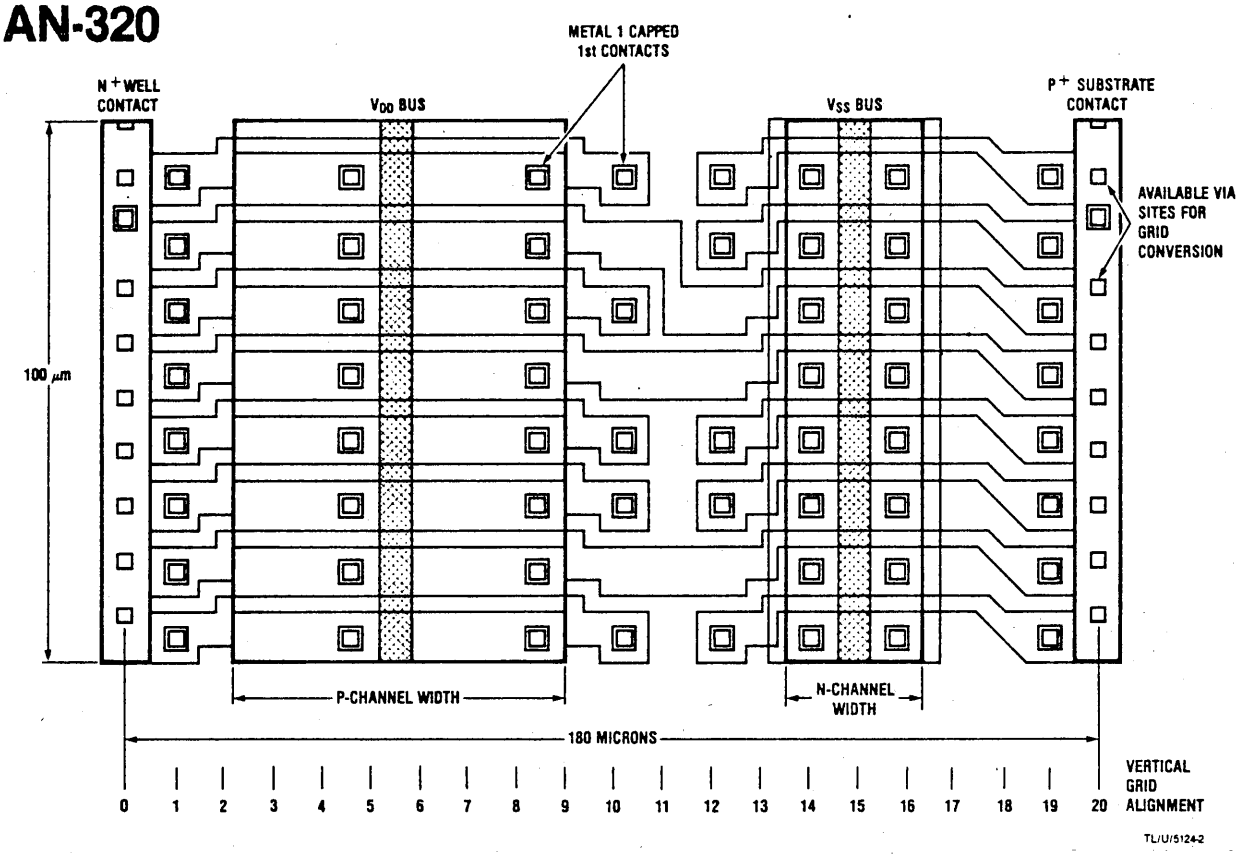


FIGURE 2. The Basic Cell Element

Occasional use is made of second layer metal in creating the library functions; where this occurs, the auto-routing software is inhibited from passing through the particular cell on that specific grid. Logic functions are defined such that they remain adequately "permeable" to metal 2 and the channel allocation is biased to second layer resources, thus optimizing the ratio of the two layers of connect during personalization.

PROCESS

A process cross-section and key electrical parameters are provided in *Figures 3a and 3b,* respectively. It is basically the ability to minimize metal pitches which determines die size on arrays. Some creative use can be made of software here, in minimizing route-grid pitches by (say) the prohibition of adjacent vias. If this is an unintelligent restriction in the software, a large number of otherwise available via sites can be lost and this can lead to the unroutability of locally congested areas of connection.

On this particular array, metal 2 may only contact to metal 1 (through the programmed via, or second contact) and no use is made of "contact stacking" at the 3×3 feature size.

PERFORMANCE AND COMPATIBILITY

Both I/Os and inputs are user selectable as either HCMOS or TTL (0.8V to 2V) compatible at the inputs, with outputs LS-TTL compatible at 4 mA sink/source capability—enabling 10 LS loads to be driven.

The part is recommended for 3V to 6V operation, with typical propagation delays of 2 ns for a 2-input gate driving a 1 pF load at room temperature and $V_{DD} = 5V$. A typical CMOS output buffer (non-inverting) driving a 15 pF load under these conditions demonstrates propagation delays of <8 ns.

THE EFFECTS OF INDUCTANCE

A study has been made of the effects of supply and signal lead inductance with respect to device performance and system interface. Here, a worst-case situation was considered when a large number (14 in this instance) of outputs are switched simultaneously and a particularly high supply lead inductance exists. The dominant inductive component was, in this case, the trace on the ceramic package—in the order of 15 nH. Clearly, this can readily be reduced to the order of 2 nH or 3 nH by redefining the silk-screening of the package, but this desirable reduction may not be possible for all packages (particularly, say, for chip carriers where there are upper limits on trace widths attainable and a relatively long connection must be made to the pin itself).

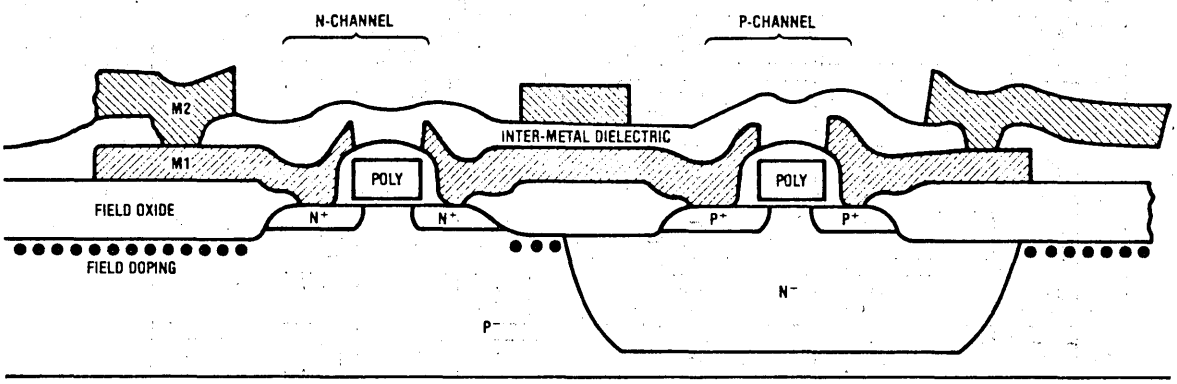
The SLX6324 has six each of V_{DD} and V_{SS} pads available which (when all are employed) dramatically reduce the effective inductance in the supply lead, at the die (see Note 1).

An evaluation was then made of the effective supply inductance, capacitance and resistance at the site of the adjacent outputs. This included all bond-wire, package-pin,

Note 1: We additionally require this number of supply pins to accommodate large DC currents on the die itself, while avoiding electron migration.

package trace and die-bus parasitics, reduced from their matrix to a lumped form. It was found that even in the worst-case condition where all outputs are "unloaded", the degradation in propagation delay through the individual buffers remained $\ll 0.5$ ns with these parasitics present.

A similar evaluation was then made with a single (one of the 14) output driving the equivalent circuit of a 20 inch PCB trace of 75Ω characteristic impedance, loaded with 10 pF. The simulated voltage waveform at the 10 pF load is shown in *Figure 4*.



a. Process Cross-Section

Gate Material	: N-Type, Polysilicon
Gate Oxide	: 600 Å
Effective Channel Length	: 2.2μ P-Channel
Metal 1 to Subs	: 14 kÅ
Metal 2 to Subs	: 22 kÅ
Thresholds	: |0.7V|
Contact 1 and 2	: 3 × 3
Metal 1 Line/Space	: 4/3μ
Metal 2 Line/Space	: 5/4μ

b. Key Electrical and Physical Features

FIGURE 3

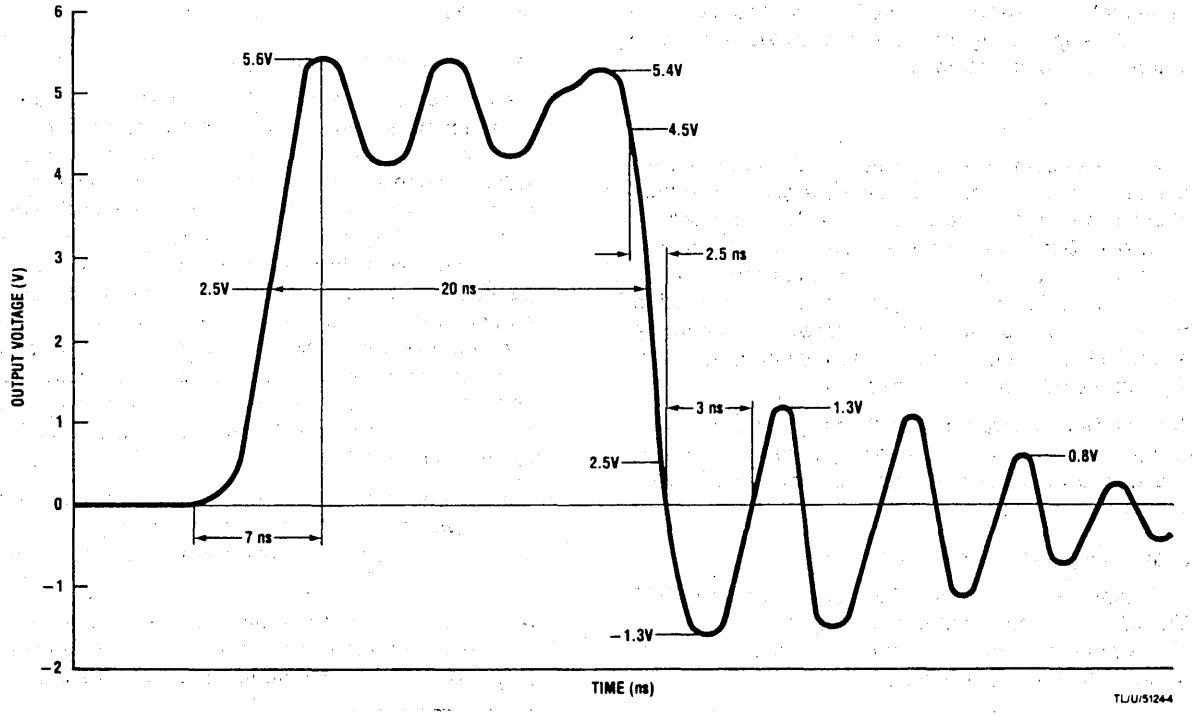


FIGURE 4. Illustrating ringing seen at a 10 pF load at the end of a 20" PCB trace of $Z_O = 75\Omega$, driven by a single output buffer (with 13 others switching simultaneously).

The supply and ground overshoots were evaluated and empirically proven incapable of latching (by SCR action) even the most susceptible HCMOS or gate array-type input; this is due to the inability of the outputs to source/sink a sufficient amount of charge in the time available. The "ring-back" after V_{SS} overshoot is of such short duration that it is incapable of erroneously transferring a logic level through even the fastest responding (HCMOS or gate array) TTL input buffer; this too was proven both empirically and by simulation.

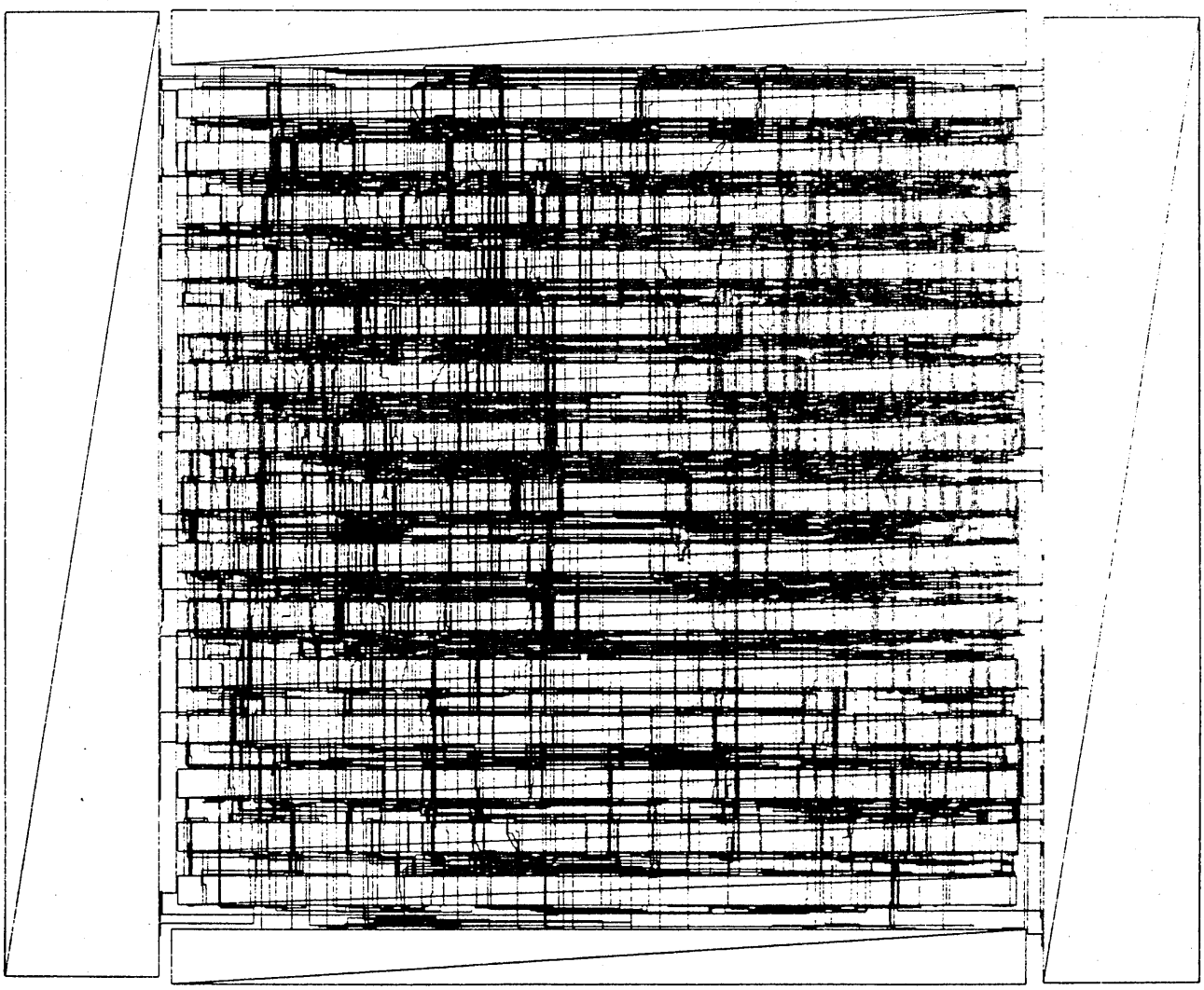
The conclusion is that even with a package that is *not* optimized (by reduction of supply-lead trace inductance) to support such array performance, parasitic inductances should not cause users any inordinate problems. It is clear however, that with a next generation product featuring (say) 2 × AC improvement, care must be taken in evaluating such parasitics, simultaneous output switching and in defining package characteristics accordingly.

ROUTING

Figure 5 illustrates a routed personalization of the 2.4k array with 85% utilization of internal cell-sites. In general, options will be approached first by optimizing placement of the individual logic elements. This is achieved by mosaic placement, where "different" (by the number of basic elements employed in the logic function) size functions are swapped until the relative amount of projected interconnect required to route the option is minimized. The bulk of the array is then routed by a channel router and remaining nets are completed by a maze router.

The channel router is inherently faster (>3×) than the maze and it is inhibited from making routes with routing resources immediately adjacent to the inputs and I/Os. The maze router is then rapidly (and with total freedom) able to complete the balance of the connections; most of which are inevitably to the interface buffers themselves.

Critical delay paths can be readily optimized by forced placement (if desired) by the user, followed by pre-route of these connections, as required.



TL/U/5124-5

FIGURE 5. Automatically Placed and Routed Example of the 2.4k Array

Gate Array and Custom VLSIC Fabrication with the M²CMOS™ Process

National Semiconductor
Application Note 321
A. London
M. Tsou
C. S. Teng
V. Kulkarni
S. Huang
October 1982

Abstract. *A bulk CMOS N-well process, containing a single level of polysilicon and two layers of metal, has been developed for the fabrication of gate arrays. The process is scalable to smaller dimensions with technology improvements. Current results being reported are for 3-micron and 2-micron feature size versions of the process. Delays of 600 ps for unloaded ring oscillators have been measured for the 3-micron process. This process will be used to build a 2.4k gate array having typical internal gate delay per stage of 2 ns.*

INTRODUCTION

The emergence of gate array technology promises important benefits to the users of VLSI circuits. Virtually any random logic configuration will be realizable in shorter times and at lower costs than is possible using conventional IC design procedures. These economies are brought about by requiring unique masking layers only at the final stage of wafer processing. The customers' logic requirements are met by generating appropriate metal interconnect masking layers with the vendor's routing software.

To implement this type of a product, a bulk CMOS, N-well[1,2] process containing a single level of polysilicon and two layers of metal, M²CMOS, has been developed. The desired logic function is achieved by generating three unique layers: metal 1 (M1), metal 2 (M2), and metal 1 to metal 2 interconnect (via). To achieve typical propagation delays of 2 ns/stage, it is necessary to use a double layer metal rather than a double poly interconnect system. The propagation delay of stages driving long interconnects on the order of hundreds of mils is limited by the RC time constant of the interconnect line. Worst-case propagation delays in the microsecond range will be obtained on gates driving long polysilicon interconnects, since the poly resistance is nearly three orders of magnitude greater than that of aluminum.

Conventional 1:1 scanning projection lithography is used in the initial version of the process to produce 3-micron minimum feature sizes. Improvements in density and performance will be realized in a more advanced version of the process, now under development, using wafer stepper lithography. Feature sizes with this process will be in the 2-micron range and further development work is expected to get the M²CMOS feature size to the 1-micron range within the next several years.

3-MICRON PROCESS

Figure 1 illustrates cross-sectionally some key features of the M²CMOS process. The N and P-channel device regions as well as substrate contact diffusions are defined by a selectively grown field oxide. A single level of N^+ doped polysilicon provides the gate electrode for both device types. Contacts to N^+, P^+ and polysilicon regions are made with metal 1. Metal 2 contacts only metal 1 through an insulating SiO_2 layer.

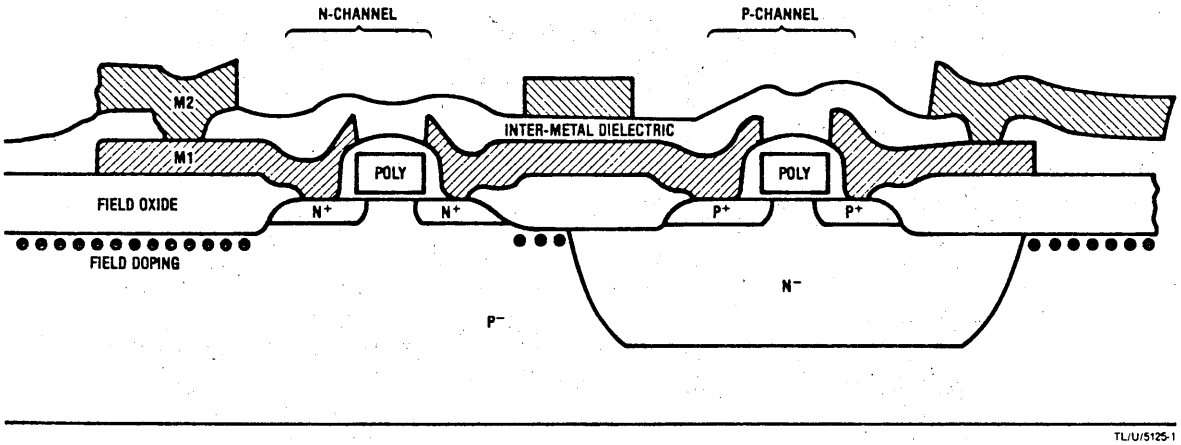


FIGURE 1. M²CMOS Cross-Section

Reprinted from PROCEEDINGS OF THE CUSTOM INTEGRATED CIRCUITS CONFERENCE, May 1982

National Semiconductor

AN-321

The process contains a total of 10 masking steps. Three of these are for implant blocking only and do not require etching. All doping of the lightly doped P-type substrate for junction formation and threshold voltage modification is performed by ion implantation. Plasma etching is used extensively in the process. The use of sputtered silicon-aluminum films for metal 1 and metal 2 provides very good coverage of surface contours.

An N-well, rather than P-well, process was chosen for several reasons. The M^2CMOS process is closely related to the XMOS™ process (Si-gate N-channel process) using the same starting material. This permits rapid integration of XMOS advances, such as memory cells, into M^2CMOS. Because of lower substrate doping levels in the M^2CMOS process with respect to the conventional P-well process, and lower resultant values of junction capacitance and body effect factor, speed improvements on random logic circuits on the order of 10% are realized. Finally, N and P-channel threshold voltages are simultaneously adjusted in M^2CMOS. Hence, one less masking step is required in this process with respect to a conventional P-well process.

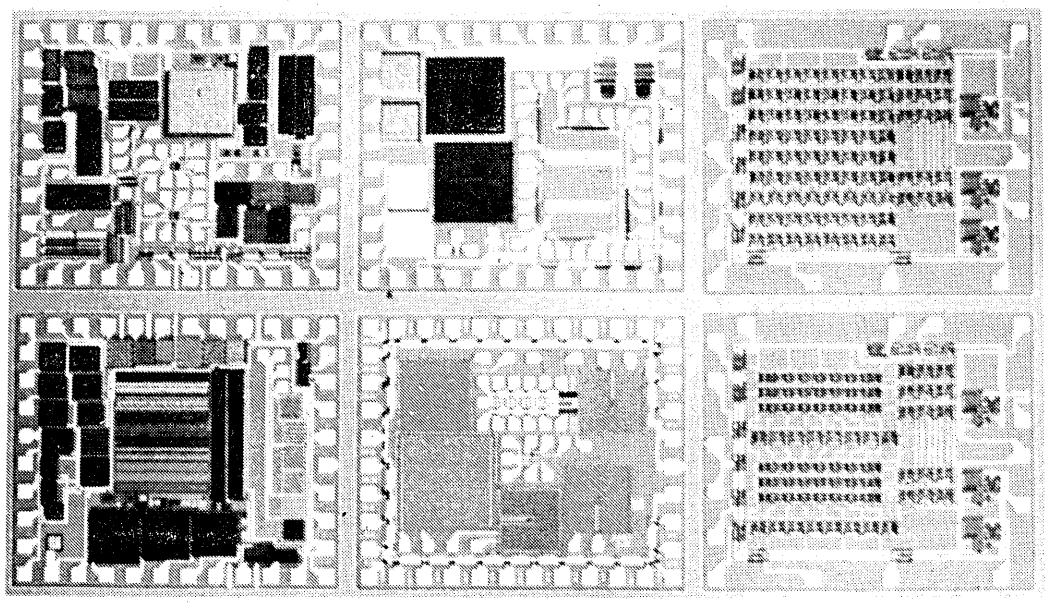
Figure 2 illustrates a test chip used to develop and characterize the 3-micron M^2CMOS process. Divided into six individual sections, it has provided information on device parameters, process parameters, yield loss mechanisms, design rule validity, and ring oscillator electrical performance.

Table I lists typical measured process and device parameters. Table II lists typical key dimensions and layout rules associated with the 3-micron M^2CMOS process. The inclusion of stacked contacts (via contact positioned directly over contact 1) in the process layout rules provides improvement in array packing density.

TABLE I. TYPICAL 3-MICRON M^2CMOS PROCESS PARAMETERS

Parameter	Units	N-Channel (25/3)	P-Channel (25/3)
V_T @ $V_{DS} = 0.1V$, $V_{BS} = 0V$	(V)	0.7	−0.7
Body Effect Factor, M @ $\lvert V_{BS}\rvert = 0-2.55V$	$(V^{1/2})$	0.16	0.45
$\lvert BV_{DSS}\rvert$ @ $\lvert I_D\rvert = 1\ \mu A$	(V)	14	19
μC_{OX} @ $\lvert V_{GS} - V_T\rvert = 0.5V$	$(\mu A/V^2)$	40	15
$\lvert V_T$ poly field$\rvert$ @ $\lvert I_D\rvert = 1\ \mu A$	(V)	17	14

Parameter	Units	Value
Sheet Res. (N^+)	Ω/sq.	25
Sheet Res. (P^+)	Ω/sq.	90
Sheet Res. (N^-)	Ω/sq.	6000
Sheet Res. (M1)	Ω/sq.	0.045
Sheet Res. (M2)	Ω/sq.	0.025
Sheet Res. (Poly)	Ω/sq.	20



TL/U/5125-2

FIGURE 2. Test Chip used for the M^2CMOS Process Development and Characterization

TABLE II. TYPICAL DIMENSIONAL FEATURES OF 3-MICRON M²CMOS PROCESS

Leff, N-channel = 2.4μ;	Leff, P-channel = 2.2μ
Contact Sizes : First	= 3 × 3 microns
Second	= 3 × 3 microns
M1 Pitch	= 7 microns
M2 Pitch	= 9 microns
Gate Oxide	= 600 Å
Poly Pitch	= 6 microns
N^+/P^+ Pitch	= 8 microns
Xj:	$N^+ = 0.35\mu$, $P^+ = 0.5\mu$, $N^- = 5\mu$

The basic process now uses SiO_2 as an insulating layer between metal 1 and metal 2. *Figure 3a* illustrates parallel metal 2 lines (pitch = 10μ) demonstrating good coverage of worst-case surface topology with very good edge definition. A polyimide[3] film, because of the planar nature of its surface and excellent insulating properties, has also been studied as the M1-M2 insulator. *Figure 3b* illustrates under somewhat smaller magnification, the improved planarity offered by polyimide over the same topology configuration shown in *Figure 3a*.

The area density of metal 1 to metal 2 shorts as well as the frequency of occurrence of metal 2 opens covering severe topology steps, have been calculated from numerous measurements on the test pattern shown in *Figure 2*. These values have been applied to the configuration of the SLX6324, 2.4k gate array now in design, indicating these two mechanisms will have only a small effect on the yield of this product for either the SiO_2 or polyimide insulator system. Both systems have measured values of M1-M2 contact resistance of 0.02Ω per 3 × 3 micron contact. Excellent initial reliability results have been obtained on several hundred ring oscillators built with both the SiO_2 and polyimide insulators after 1000 hours of operation at 125°C (0 failures in each group). At this time, the deposited oxide insulator system is being used in the M²CMOS process because it is a proven material with a strong supporting technology base. The polyimide system may prove useful as metal pitches are further reduced. It should also prove useful when the process is modified to include one or more additional layers of metal interconnect.

3-MICRON M²CMOS ELECTRICAL PERFORMANCE

Electrical measurements have been made on a series of ring oscillators contained on the M²CMOS test chip. These oscillators vary from 7 to 13 stages and have different degrees of loading. *Figure 4* illustrates the performance predicted for a 13 stage unloaded oscillator by the SNAP[4] model using measured electrical parameters from an M²CMOS wafer. The average propagation delay/stage for 53 ring oscillators built from this wafer was 0.56 ns with a standard deviation of 0.091 ns, in good agreement with the simulated value of 0.61 ns. The speed•power product of this oscillator has been measured to be 10 fJ/MHz. (Since power in CMOS circuits is directly proportional to frequency of operation, fJ/MHz is considered a more meaningful unit of comparison than fJ.)

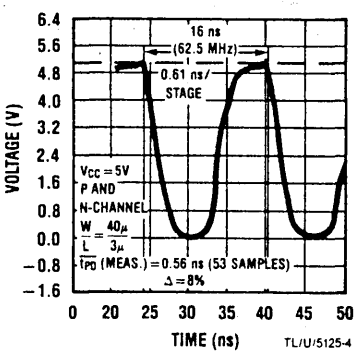


FIGURE 4. SNAP Simulation for 13-Stage M²CMOS (3μ) Ring Oscillator, Having a Fan-Out = 1 and Operating at T_A = 25°C

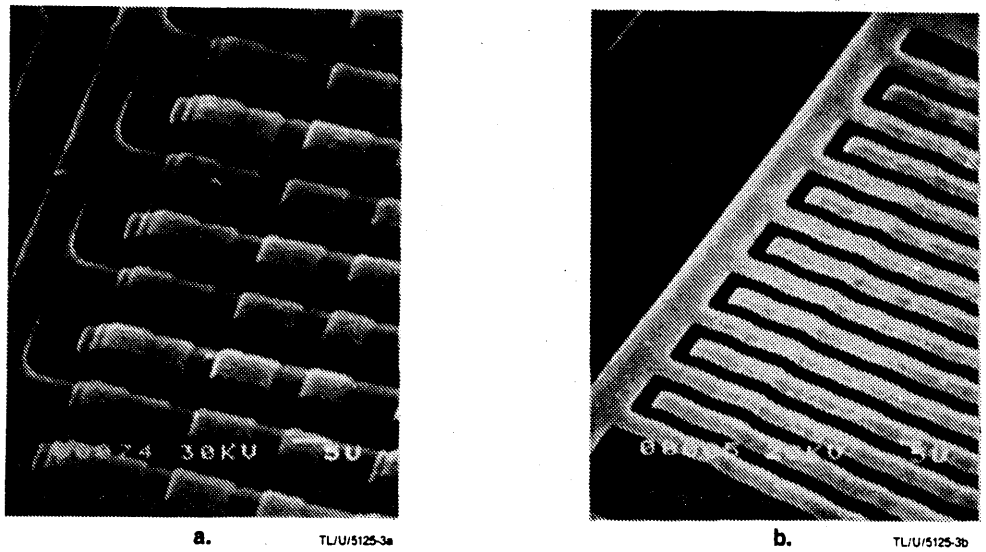


FIGURE 3. Metal 2 Lines (10μ Pitch) Covering Severe Surface Topology using: (a) Deposited SiO_2 Insulator (b) Polyimide Insulator

Figure 5 illustrates the dependence of ring oscillator propagation delay on operating supply voltage, V_{CC}, and fan-out, FO. The FO = 5 curve used a large metal 1 load capacitor at each stage and showed an approximate doubling of unloaded propagation delay/stage. The above results indicate that the predicted performance characteristics of the SLX6324, 2.4k gate array[5] of 2 ns typical and 5 ns worst-case delay per stage are realistic.

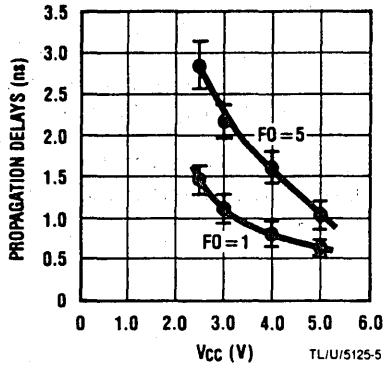


FIGURE 5. Test-Chip Ring Oscillator Results (Sample Size 5, Log #1003, Wafer #3)

2-MICRON M²CMOS

A second generation version of the M²CMOS process is now being developed. It will feature improved speed and density by reducing minimum feature size to 2μ and improving overlay tolerance by the use of direct step on wafer lithography. Lower temperature process steps after source-drain region formation are used in this process to achieve even shallower N^+ and P^+ junction depths than those obtained in the 3μ process. A summary of the dimensional features of this process is listed in Table III.

TABLE III. KEY DIMENSIONAL FEATURES OF 2-MICRON M²CMOS PROCESS

Leff, N-channel = 1.5μ;	Leff, P-channel = 1.4μ
Contact Sizes : First	= 2 × 2 microns
Second	= 2 × 2 microns
M1 Pitch	= 5.5 microns
M2 Pitch	= 7.0 microns
Gate Oxide Thickness	= 400 Å
Poly Pitch	= 4 microns
N^+/P^+ Pitch	= 7 microns
Xj: $N^+ = 0.3\mu$,	$P^+ = 0.4\mu$, $N^- = 5\mu$

To obtain satisfactory operation at 5V of transistors having patterned poly gate lengths of 2μ, it is necessary to increase substrate doping levels to values greater than those used in the 3μ process. The SUPREM[6] and GEMINI[7] process and device modeling programs have been very useful for this purpose. Since good agreement has been obtained between simulated and actual device parameters, it has been possible to make detailed comparisons of various processing approaches with a minimum of wafer fabrication expense.

Table IV summarizes simulated parameters of interest for three different processing approaches under consideration. The simplest approach, C, merely increases the doping level of the starting material and well implant to improve upon the punchthrough characteristics of the 3μ process. By adding an extra blanket implant in the early stages of process A, it is possible to make improvements in junction capacitance and body effect factor of the N-channel device. The blanket implant approach is designed to give nearly the same P-substrate surface doping level as obtained in approach C, but about an order of magnitude lower doping level at the depth of the N^+ junction. Approach B, requiring the most additional processing steps of the three, uses a masked deep boron implant into N-channel regions to reduce punchthrough problems.[8]

TABLE IV. SUPREM/GEMINI SIMULATIONS FOR 2-MICRON M²CMOS DOPING APPROACH

Parameter	A. Blanket Implant Approach	B. Double Implant Approach	C. High-Doped Material Approach
V_{Tn}, (V)	0.56	0.54	0.53
M_n, ($V^{1/2}$)	0.26	0.28	0.29
Xj (N^+), (μ)	0.296	0.298	0.298
N^+ Sheet Res. (Ω/sq.)	27.16	27.10	27.20
N^+ Junction Cap. @ 0V:			
C_{ja}, (pF/μ^2)	0.9875×10^{-4}	1.10×10^{-4}	2.385×10^{-4}
C_{js}, (pF/μ)	1.175×10^{-4}	1.56×10^{-4}	2.53×10^{-4}
Process Complexity	One Extra Implant	One Extra Implant One Extra Mask Step	Least

National Semiconductor

PRELIMINARY

A 2.4k M²CMOS™ Gate Array, System Design Facility

National Semiconductor
Application Note 322
I. R. Mackintosh
J. Bunik
D. Sowell
J. Jorgensen
B. H. Cheng
M. Rohm
October 1982

Abstract. *This paper describes a gate array (SLX6324) fabricated on a 3-micron, dual-metal, N-well, 5V process which typically provides internal propagation delays of < 2 ns. The part is optionable through metal 1, metal 2 and common via mask programming, enabling rapid turnaround on wafers inventoried to first metal. A novel, empirically derived cell configuration maximizes the efficiency of interconnection of individual library functions.*

The SLX6324 features a desirably low gate to I/O count to alleviate traditional system partitioning difficulties and optionally provides user-selectable (high speed) CMOS and TTL input compatibility.

INTRODUCTION

Details of the basic cell element, die organization, electrical performance, process highlights and software capabilities are presented to provide an overview of the total integrated design concept associated with this array.

THE BASIC CELL ELEMENT

This configuration (*Figure 1*) contains several key features which are interrelated in providing the inherent flexibility of the element. The functional block itself is utilized in unit multiples to construct the various logical elements available in the array library. For example, a basic D-type (with preset and clear) can be constructed from 3 basic cell elements; 4 separate inverters from a single element, etc.

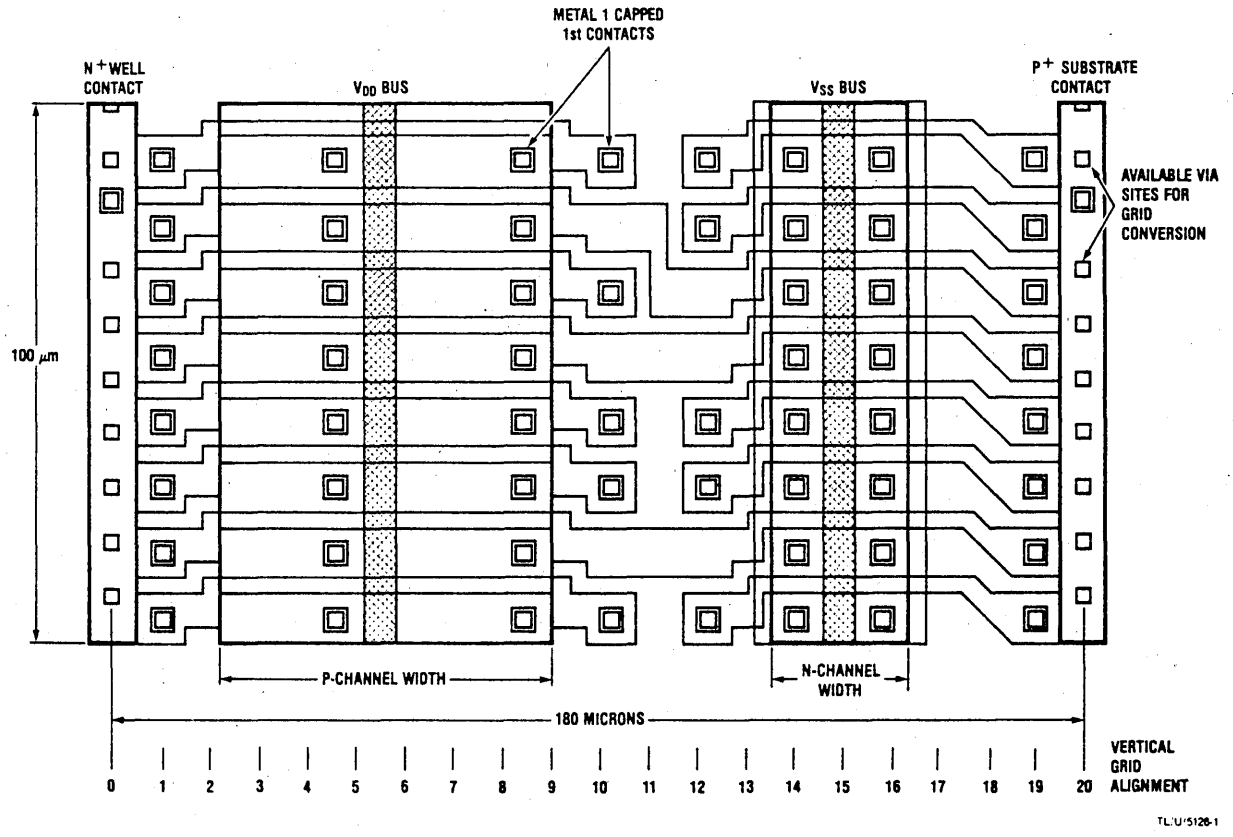


FIGURE 1. The Basic Cell Element

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Key features are as follows:

1. The supply rails are located over the N and P-channel devices with sources/drains accessible either side of the supply with an empirically optimized number of channels occurring between supply and contact on the P-channel/V_{DD} side.
2. Grid conversion channels occur either side of the element for interface with the routing grid.
3. Despite the larger number of poly gates than found in more conventional organizations, the element has been demonstrated inherently more flexible than its counterpart due in part to the use of poly stripes that act not only as MOSFET gates, but also as diffusion isolators, and the empirically optimized pattern of the polysilicon as a circuit construction element.
4. Substrate contacts are forced once per element for both P and N-channel devices to eliminate internal latch-up susceptibility that could be inherent in the personality of some option constructed with the array.
5. Library functions are constructed by the use of metal 1 (M1) to pre-program the element(s). A limited use of M2 (and via) is permitted in the element to optimize the flexibility of the configuration while not detracting from the permeability of the logic function for routing purposes.

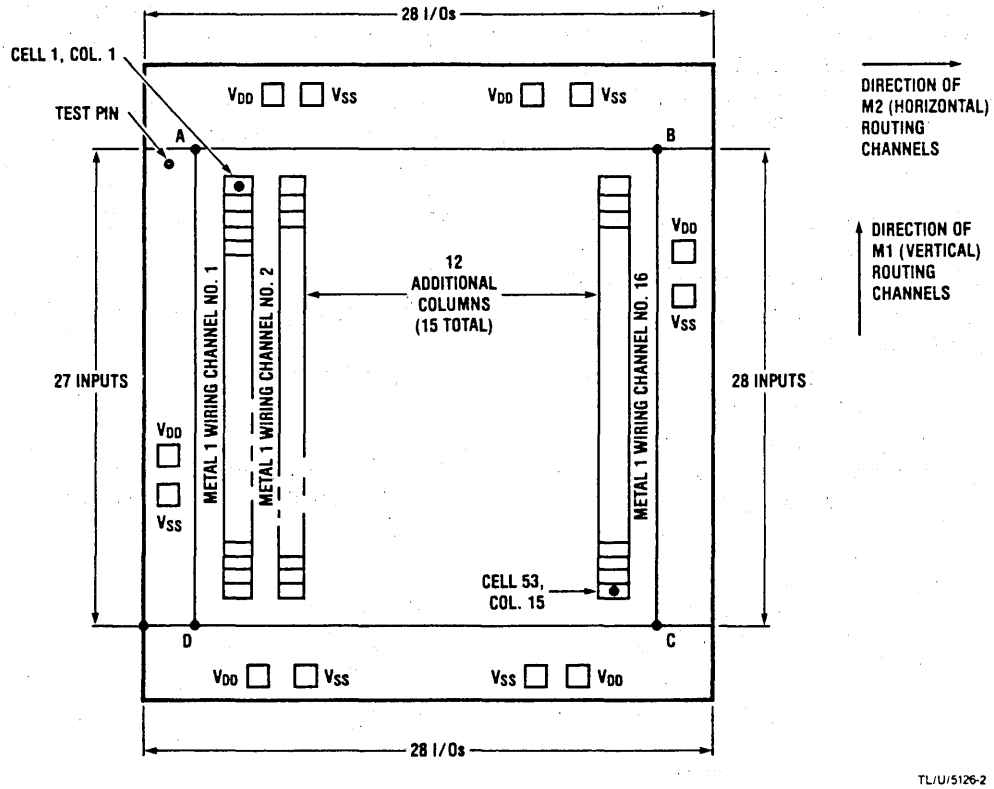
THE SLX6324 ARCHITECTURE (*Figure 2*)

The die is organized with 15 vertical columns of basic cell elements stacked 53 deep. A total of 56 I/O sites are available, 28 top and bottom of the columns; 28 inputs are available at either side of the die.

Vertical (M1) resources occur between the columns on a 9-micron pitch and horizontal resources (M2) are available across the columns on a 10-micron grid—except where logic functions contain metal 2 in a particular channel.

The array is configured with M2 resources exceeding those of M1, so that in high utilization personalizations the ratio of vertical to horizontal resources will approach the optimum, unity.

The grid arrangement in the routing channels permits the use of adjacent vias and thus further ensures the routability of locally congested interconnect inherent in most personalizations. To guarantee autoroutability the array has vertical channels allocated more liberally toward the die center (*Figure 3*).



Note 1: Routing area occurs between A, B, C and D.
Note 2: Metal 2 (horizontal) routing occurs over cell columns.

FIGURE 2. SLX6324 Architecture

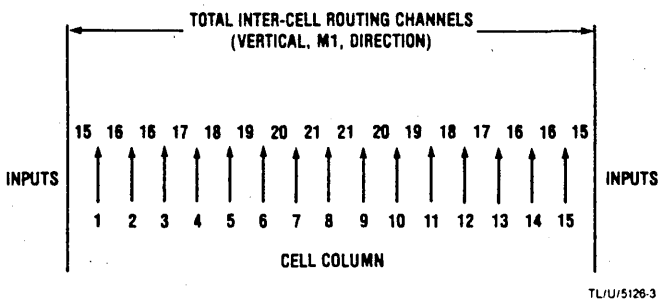


FIGURE 3. Distribution of Routing Channels Between Vertical Columns

COMPATIBILITY

A further important feature of this array product is the electrical compatibility of the I/O. Inputs are user-selected as either full-TTL or CMOS (HC family) compatible, with I/O sites featuring similar input compatibility and either TRI-STATE® or CMOS outputs with 4 mA sink/source capability—enabling 10 LS-TTL loads to be driven.

All I/O and input buffer sites are pre-programmed functions available in numbers compatible with system design demands, typical for gates/input and gates/output ratios.

TEST FEATURE

A test facility is provided at the cost of a single input pin, to create TEST MODE. With this pin active (LO) two additional pre-defined inputs are jointly employed to force all outputs to HI, LO or HI-IMPEDANCE states and thus reduce test time in gathering output parametrics at sort. These two pins further function as conventional (either CMOS or TTL) inputs (when TEST MODE, HI) with no performance penalty apparent to the user. All inputs are selectable with or without pull-up resistors.

DISSIPATION

Typical individual personalizations of the array are envisaged as operating at <500 mW. Dissipation in CMOS is dependent on clock rate and typical power demands are:

- CMOS output buffer driving 15 pF, 1 Mbit, 5V operation at 25°C; dissipation ≈ 0.7 mW.
- A single 2-input gate driving a 1 pF load, 1 Mbit, 5V operation at 25°C; dissipation typically <30 μW.

Note: A load of 1 pF is equivalent in the array to the mean from-to length associated with a typical personalization (scaled to incorporate the effect of fringing capacitance) and a fan-out of 4 (scaled to incorporate Miller effect).

PERFORMANCE

This 3μ process (designed for 3V–6V recommended operation) enables worst-case propagation delays of $t_{PHL} \approx t_{PLH} = 4.5$ ns to be achieved (*Figure 4a*) with a 2-input gate driving a 1 pF load.

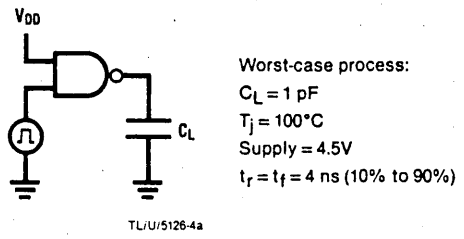


FIGURE 4a. Gate Speed Benchmark

A 13-stage ring oscillator structure (*Figure 4b*) operating at 5V and 25°C is typically found to operate with propagation delays of 600 ps per stage. Key process features enabling this performance are shown in *Figure 5*.

Current in-house modeling capability enables AC circuit performance to be predicted with less than 10% error on the existing 3-micron process. It is envisaged that the 2-micron advanced version of this process currently in development will enable a 2× improvement in performance.

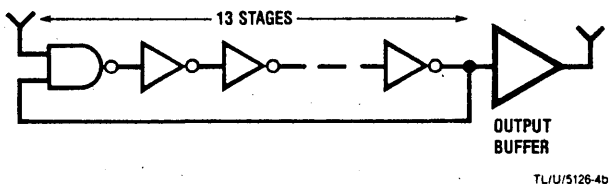


FIGURE 4b. Ring Oscillator from MK230 Test Vehicle Featuring Minimum Loading and Interconnect Capacitance

Gate Material	: N-Type, Polysilicon
Gate Oxide	: 600 Å
Effective Channel Length	: 2.2μ P-Channel
Metal 1 to Subs	: 14 kÅ
Metal 2 to Subs	: 22 kÅ
Thresholds	: |0.7V|
Contact 1 and 2	: 3×3
Metal 1 Line/Space	: 4/3μ
Metal 2 Line/Space	: 5/4μ

FIGURE 5. Key Electrical and Physical Process Features TL/U/5126-5

SOFTWARE

Software aids completing the system design facility include:

1. Data Entry—Manual netlist coding, transfer of netlist from an existing CAD data base, or schematic capture on a stand-alone microcomputer-based graphics system using previously defined logic symbol libraries. After schematic capture or netlist coding, a central file is created which is suitable for data base access for all other software packages.
2. Layout Difficulty Analysis—A package capable of evaluating the routability of a particular personalization. All arrays utilizing less than 80% of the total available basic cell elements are currently envisaged as being 100% autoroutable. This feature is for evaluation of high utilization personalizations.
3. Testability Analysis—To evaluate the testability of a personalization. This output will aid users in altering logic design to enhance the overall testability of the configuration.
4. Logic Simulation—Prior to physical layout of a personalization, this package is employed to validate the logic design. Successful completion of this step results in useful data for both layout and test program generation.
5. Test Program Generation Aids—Software to extract test vectors from simulation results, grade the fault coverage of the extracted and user-supplied vectors and generate sentry tester tapes.
6. Autoplacement and Autorouting—An integrated set of programs optimized for a particular array family. Interactive graphics are available to complete any failed from-to's on densely populated (>80% utilization) personalizations.
7. Geometric Verification—Should any interactive editing be performed, checks for layout rule violations will be made.
8. Topological Verification—To validate a personalization against the initial netlist. This is required where any interactive editing has occurred.
9. Performance Verification—Actual from-to lengths and computed capacitive loading (extracted from the completed design file) are combined with fan-out data to enable re-simulation of the personalization and verification of the original timing specification.

PACKAGING

Almost uniquely, the evolution of gate arrays has made new demands on packaging technology. The SLX6324 is available in 3 package options.

(a) 120-pin ceramic pin-grid array with 100 mil centers

(b) 124-lead ceramic chip carrier (50 mil centers)

(c) 124-lead plastic chip carrier (50 mil centers)

These packages provide the user with both thru-hole insertion and surface mounting options.

The ceramic packages [options (a) and (b)] utilize aluminum ultrasonic wire bonding, the standard for ceramic packages. With the high lead-count there are pitfalls specifically associated with bond loop count and density, which require careful attention when defining suitable packaging:

- Bond-wire length
- Post target size and layout
- Die pad size and layout
- Wire diameter and hardness
- Type of wire bonder and its physical abilities

The plastic package [option (c)] is targeted for tape automated bonding. This technique avoids obvious difficulties in molding over large numbers of closely-spaced wire bonds.

All the above packages feature interlead capacitances of < 3 pF and low lead inductances tolerant of large numbers of outputs switching simultaneously.

CONCLUSION

This paper has outlined the majority of the base parameters requiring evaluation and consideration during the definition and design of a gate array. The significant features of a 2.4k CMOS array (SLX6324) have been presented and details of a comprehensive system design facility defined.

ACKNOWLEDGEMENT

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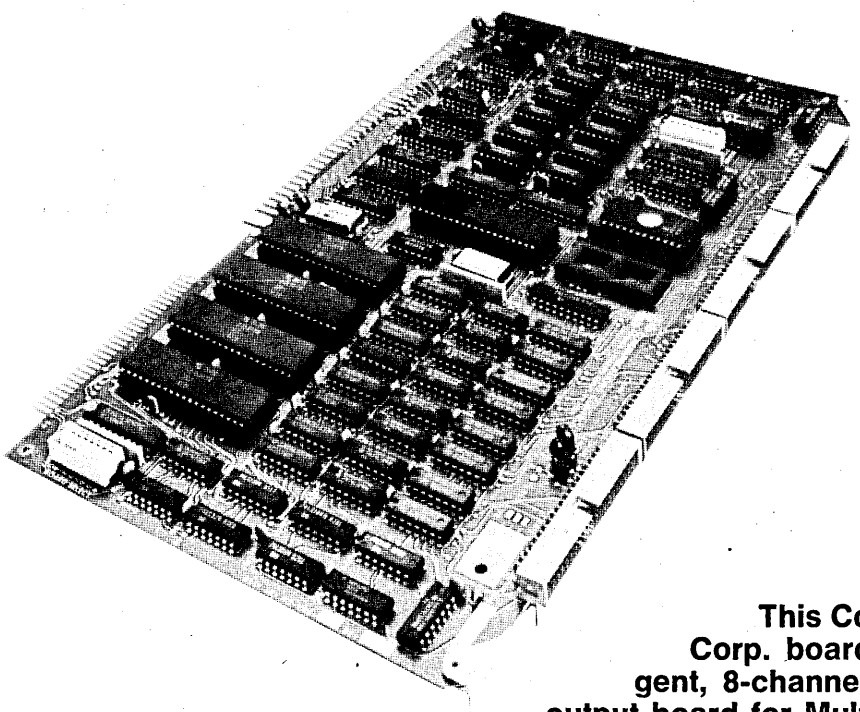

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Equipment and system design often require the use of a wide variety of integrated circuits in order to obtain optimum performance. One way for an engineer to be certain that he hasn't overlooked the best device for his application is to refer to the pages of IC MASTER.

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AM26LS32	Line Receiver, Differential
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74LS08	Quad 2-Input AND Gate
74LS32	Quad 2-Input OR Gate
74LS74	Dual D-Type Positive Edge Triggered Flip-Flop with Preset and Clear
74LS138	3 Line to 8 Line Decoder/Demultiplexer
74LS164	8-Bit Gated Serial-In, Parallel-Out Shift Register
74LS244	Octal Bus Driver (Schmitt trigger) Non-Inverting, 3-State, Complementary Control
74LS273	Octal D-Type Edge-Triggered Flip-Flop
MBM2716	Fujitsu 248 by 8 PROM
SN74LS04	Hex Inverter
SN74LS133	13-Input NAND Gate
SN74S240	Octal Buffer/Line Driver/Line Receiver Inverted 3-State Outputs
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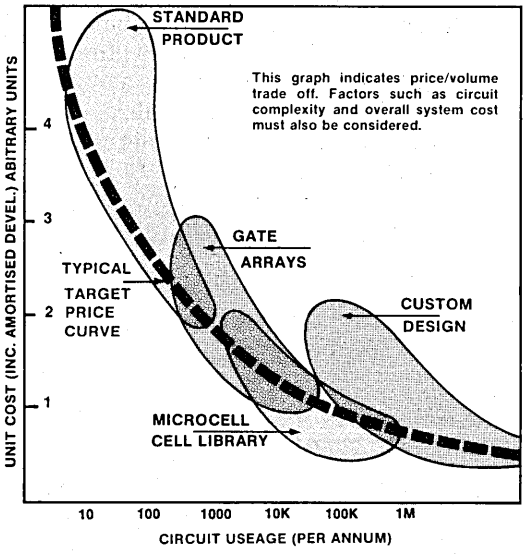

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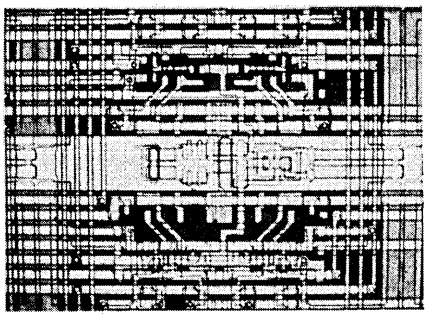

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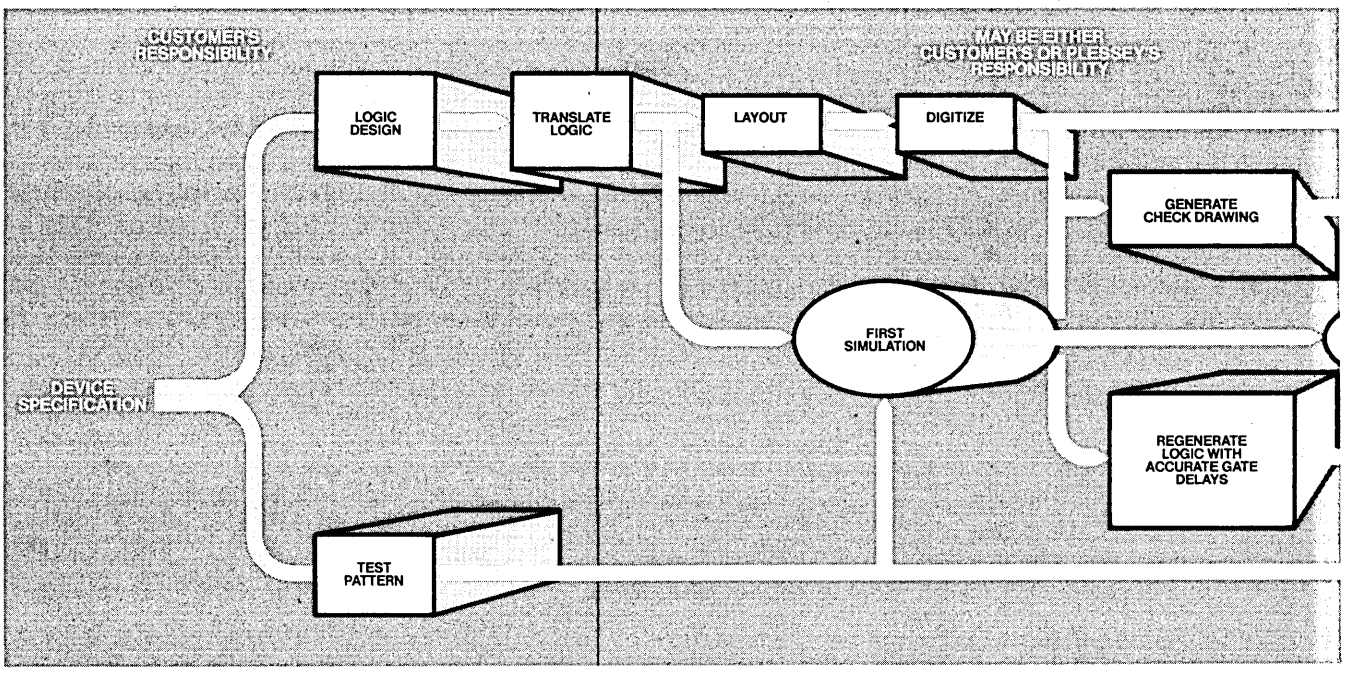

Plessey Semi-Custom LSI

the cells you need from the software library, and the computer generates the distributed gate diffusion and metallization patterns needed to perform the selected functions. After simulation and verification on our computer, your design is diffused into your proprietary wafer.

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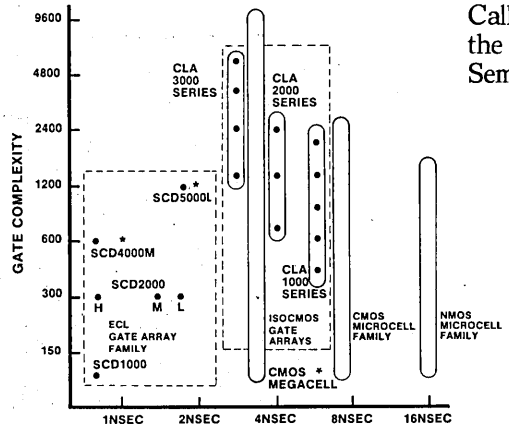
In our design center, you'll find all the computer and graphic design aids necessary to provide the quick, interactive response you need. The design center includes facilities for multi-layer metallization of gate arrays for faster turn-around on your prototypes, while our silicon foundry does all the diffusions and volume production of your devices.

The chart below indicates the process of producing your semi-custom LSI.

For your first project, we can start with your logic or circuit diagram and convert it to the appropriate array form (MICROGATE, MICROCELL or MICROLIN). If our solution is acceptable, we then use computer simulation to check out the design, while also generating a test sequence for the final testing of the IC.

When the circuit has been checked out, we digitize the chip layouts and interconnection patterns, then run a second simulation based on our process parameters. The design is tested for normal and worst case component values, under quiescent and dynamic conditions.



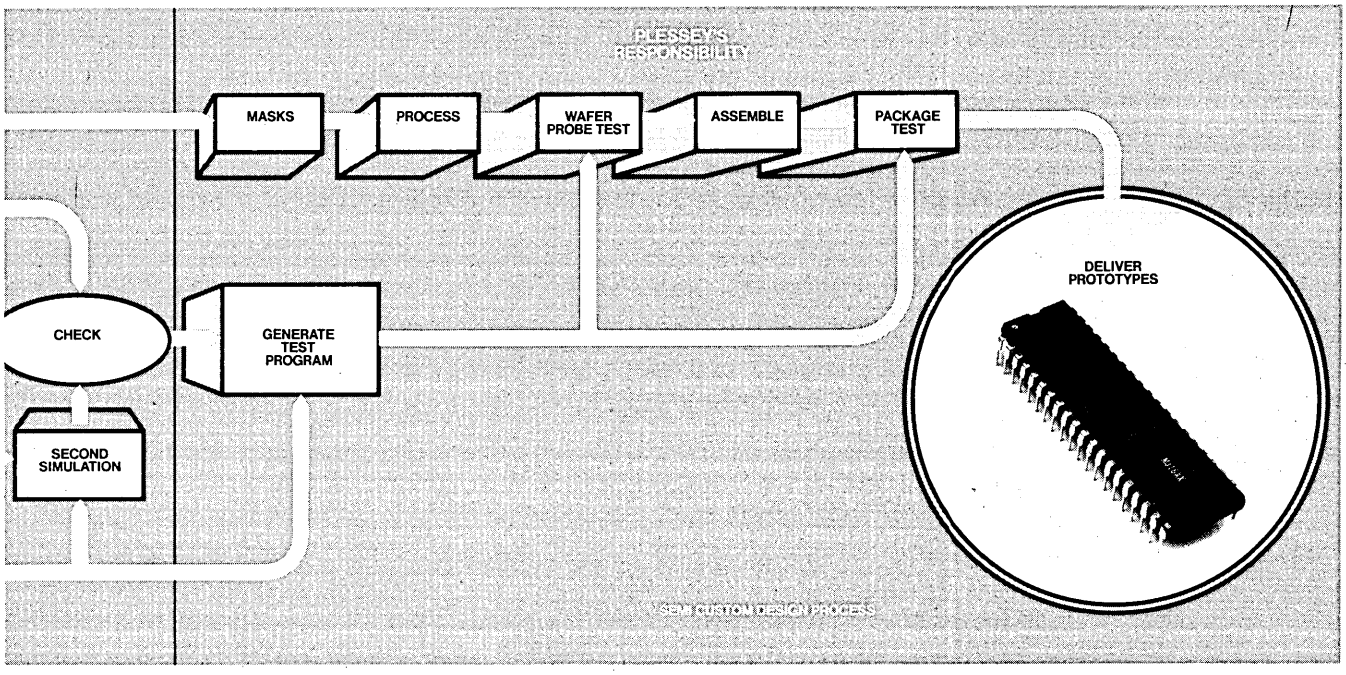
COMPLEXITY Vs. GATE DELAY CHART

We've found that a designer with no previous IC design experience can learn enough over the course of his first project to be able to handle the next project up to this point with minimal assistance from us. The savings in engineering costs on subsequent jobs can be very significant.

We have the facilities and technology, the range and the reliability to help you get your new designs to market faster for less.

The next few pages describe our semi-custom capabilities in more detail. After you've looked at them, we'd like to hear from you. Call (714) 540-9979 and ask for the Marketing Manager of our Semi-Custom Operations.

ISOCMOS is a trademark of Mitel Inc.



Plessey Semi-Custom LSI

PLESSEY CMOS LSI GATE ARRAYS.

Plessey ISOCMOS LSI Gate Arrays are available in commercial, industrial and military versions. Inputs and outputs are TTL/CMOS-compatible, and they require only a single supply voltage (3V to 6V) and provide very low power dissipation. Typical propagation delay is 3 ns for a 2-input NAND gate.

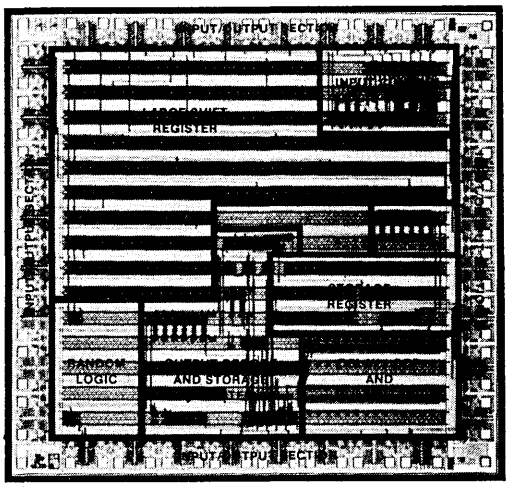
Designing with Plessey CMOS LSI Gate Arrays is similar to designing printed circuit boards for conventional SSI/MSI IC's, and you can expect prototypes within 6 to 10 weeks from your layout.

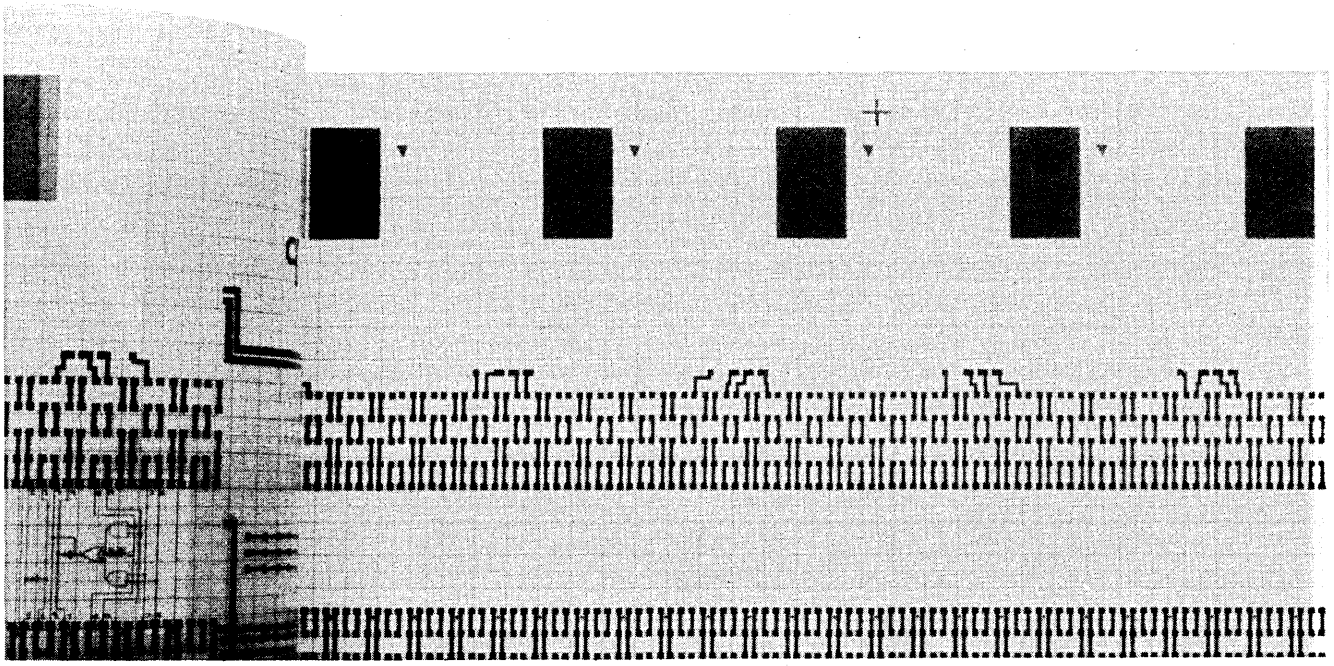
The Gate Array consists of alternating rows of basic logic cells and interconnection areas diffused into a master slice of silicon. Surrounding the logic cells are the universal input/output buffer cells.

To design your semi-custom Microgate-C circuit, you select decals that represent the logic functions you need (listed on page 8) and place them in the active area of the chip. The computer interconnects the primitive cells to create the complete logic functions you need, so you do not have to be concerned with the internal circuit design.

Chip efficiencies as high as 100% can be achieved by using the interconnection areas of the chip and a second layer of metallization that can be routed anyplace on the surface of the chip. If only a single layer of metal is going to be used, the interconnection areas are diffused with extensive polysilicon cross-under paths (in green in the photo below) for maximum design flexibility.

When your design is complete, we use our Computer Aided Design facilities to simulate circuit operation for all maximum, nominal and minimum component values. This includes all quiescent and dynamic conditions, as well as circuit operation over a temperature range of −55° to +125°C. Any circuit errors can be pinpointed and corrected before fabrication begins.





Plessey Semi-Custom LSI

THE INPUT OUTPUT CELLS.

The cells around the edge of the chip consist of an input section and an output section.

Each peripheral cell also has a bonding pad which is linked, inside the cell, to the input and/or output sections and is the point to which external bond wires to the chip are connected. Diodes provide anti-static protection.

THE INTERCONNECTION AREAS.

The interconnection highways between the rows of cells accommodate up to twelve tracks. The second layer of metal, if it is used, crosses over these tracks with no interaction.

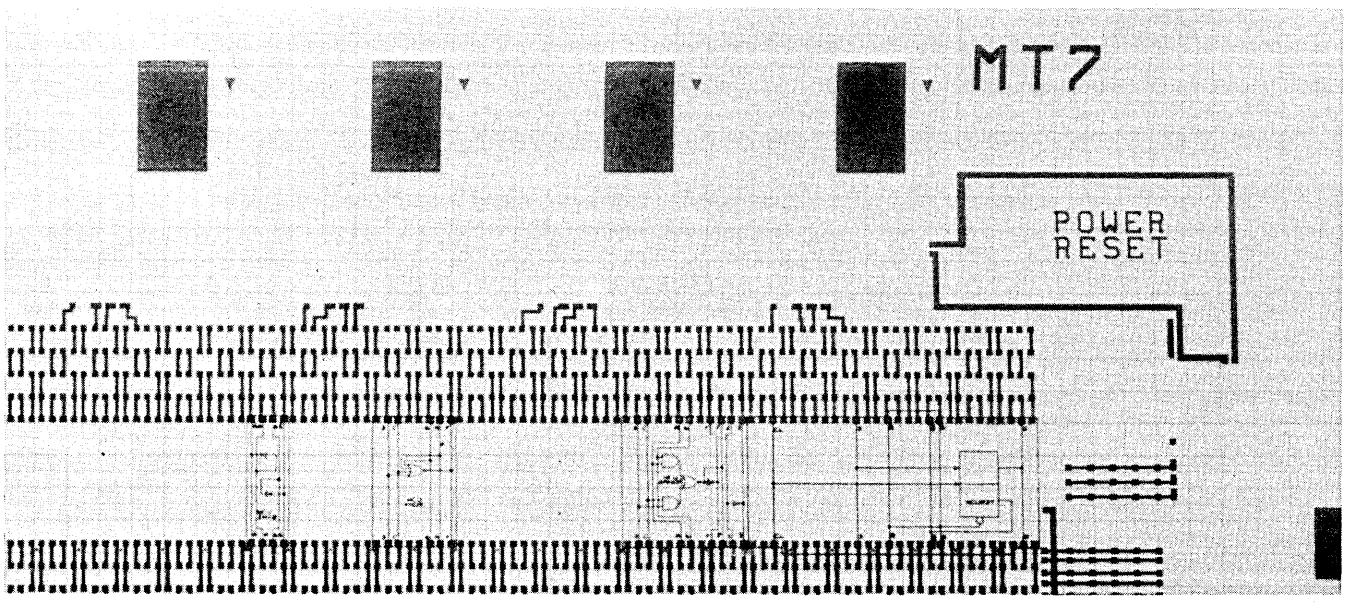
If only a single layer of metal is to be used, the integral polysilicon under-crossings diffused into the interconnection area provide a great deal of freedom. Connections are made between the underpasses and the metal tracks only at the contact windows.

AUTOMATIC CHIP ROUTING.

A major strength offered by Plessey is its auto-routing for multi-layer metallization. In comparisons with hand-packed, optimized chips, the program has provided better packing, shorter tracks and fewer "via's." And has done in it in minutes rather than days or weeks.

CMOS CHIP SIZE CHART

PRODUCT FAMILY	EQUIV. GATES	NO. PADS	TYPICAL GATE DELAY	LAYERS OF INTERCONNECT
CLA 1000 10XX	560	40	6NSEC	SINGLE
12XX	964	52	6NSEC	SINGLE
15XX	1440	64	6NSEC	SINGLE
18XX	2014	76	6NSEC	SINGLE
CLA 2000 20XX	840	48	4NSEC	DOUBLE
21XX	1440	64	4NSEC	DOUBLE
24XX	2400	80	4NSEC	DOUBLE
CLA 3000 3XXX	4000	80	3NSEC	DOUBLE



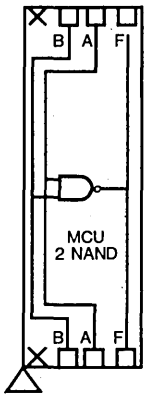
Plessey Semi-Custom LSI

PLESSEY CMOS LSI FUNCTION LIBRARY.

CELL DESCRIPTION	CELL NAME	EQUIV. GATES	CMOS EQUIV.
Gates			
Inverter Fast	MCUINV1	1	4069
Dual Inverter	MCUINV2	1	4069
2IP NAND Gate	MCU2NAND	1	4011
2IP NAND/AND Gate = Inverter	MCU2AND	2	4018
3IP NAND Gate = Inverter	MCU3NAND	2	4023
3IP NAND/AND Gate	MCU3NAD	2	4073
4IP NAND Gate	MCU4NAND	2	4012
4IP AND/NAND Gate = Inverter	MCU4AND	3	4082
2IP NOR Gate	MCU2NOR	1	4001
2IP NOR/OR Gate = Inverter	MCU2OR	2	4071
3IP NOR Gate = Inverter	MCU3NOR	2	4025
3IP NOR/OR Gate	MCU3OR	2	4075
4IP NOR Gate	MCU4NOR	2	4002
4IP NOR/OR Gate = Inverter	MCU4OR	3	4072
2 AND 2 NOR Gate	MCU2ANNO	2	4085
2 AND NOR/OR Gate = Inverter	MCU2ANOR	3	4019
TRI-State Gate = Inverter	MCUTRI	2	
Exclusive OR/NOR Gate	MCUEXORN	3	4070 4077
Arithmetic			
Half Adder = Inverter	MCUHAD	4	
Full Adder	MCUFAD	7	4008
Registers & Latches			
Set-Reset D Type Flip-Flop	MCUSRDT	8	4013
Reset D Type Flip—Flop	MCURDT	7	4013
Set D Type Flip-Flop	MCUSDT	7	4013
D Type Flip-Flop	MCUDT	6	4013
Set-Reset D Latch	MCUSRDL	5	
Reset D Latch	MCURDL	4	
Set D Latch	MCUSDL	4	
D Latch	MCUDL	4	
NOR S/R Latch	MCUNOSR	3	4043
NAND S/R Latch	MCUNASR	3	4044
D Register (First Bit)	MCUDREGF	5	
D Register (Middle Bit) Dual	MCUDREGM	5	4042
D Register (End Bit)	MCUDREGE	3	
Shift Register (First Bit)	MCUSHRF	10	
Shift Register (Middle Bit)	MCUSHRM	5	
Shift Register (End Bit)	MCUSHRE	5	4015
Half Parallel Loading Shift Reg Clock Divers	MCUHPLSF	8	
Half Parallel Loadin Shift Reg First and Middle Bit	MCUHPLSM	7	4021
Half Parallel Loading Shift Reg End Bit	MCUHPLSE	7	
Decoders			
Expandable 7-Segment Decode Segment a	MCU7SGA	7	
Expandable 7-Segment Decode Segment b	MCU7SGB	7	
Expandable 7-Segment Decode Segment c	MCU7SGC	5	
Expandable 7-Segment Decode Segment d	MCU7SGD	8	4055
Expandable 7-Segment Decode Segment e	MCU7SGE	5	
Expandable 7-Segment Decode Segment f	MCU7SGF	8	
Expandable 7-Segment Decode Segment g	MCU7SGG	8	
Service Elements			
2 Row Interconnect	MCU2INT	1	
Power Access	MCUPA	1	
Peripheral			
Input Buffer Inverting	MCUNIP		
Input Buffer Inverting with 15 k Pull Up Resistor	MCURINIP		
Input BUffer Inverting with 2 k Pull Up Resistor	MCUR2NIP		
Output Buffer Inverting	MCUNOP		
Output Buffer Inverting Open Drain	MCUODNOP		
Tri-State Output Buffer plus Inverting Input Buffer	MCU3IO		
Tri-State Output Buffer plus Inverting Input Buffer with 15 k Pull Up Resistor	MCUR13IO		
Tri-State Output Buffer plus Inverting Input Buffer with 2 k Pull Up Resistor	MCUR23IO		
Dummy Pad	MCUDUM		

2 INPUT NAND

CHARACTERISTICS	TYP	MAX	UNITS
PROPAGATION DELAY TIME HIGH TO LOW LEVEL	0	0	nS
PROPAGATION DELAY TIME LOW TO HIGH LEVEL	0	0	nS
TRANSITION TIME HIGH TO LOW LEVEL	4	5.2	ns/pf
TRANSITION TIME LOW TO HIGH LEVEL	4.5	5.8	ns/pf
INPUT CAPACITANCE	.35	.5	pf
INHERENT OUTPUT CAPACITANCE	.7	.9	pf



Plessey Semi-Custom LSI

NMOS MICROCELL LIBRARY

D-TYPE FLIP-FLOP
D-TYPE FLIP-FLOP WITH S & R
AS 1 BUT WITH 3X DRIVE CAPABILITY
AS 2 BUT WITH 3X DRIVE CAPABILITY
AS 1 BUT WITH SERIAL/PARALLEL LOAD
TTL/CMOS O/P BUFFER
TTL/CMOS INVERTING O/P BUFFER
TTL TRISTATE O/P BUFFER
OPEN-DRAIN O/P BUFFER
TTL INPUT BUFFER
INTERNAL INVERTER/BUFFER
TTL INPUT SCHMITT TRIGGER
DATA LATCH
INPUT SHIFT BIT
INTERMEDIATE SHIFT BIT
OUTPUT SHIFT BIT
CLOCK DRIVER FOR 14-16

SUPPLY PAD
INPUT PAD
NOR GATE
NAND GATE
NOR GATE WITH 4X DRIVE CAPABILITY

C-MOS MICROCELL LIBRARY

D-TYPE FLIP-FLOP
D-TYPE FLIP-FLOP WITH PRE AND CLR
DUAL CLK D-TYPE PRE AND CLR
NAND MULTIPLE INPUT
NOR MULTIPLE INPUT

SMALL BUFFER/INVERTER
LARGE BUFFER/INVERTER

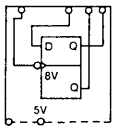
2 I/P NOR
2 I/P NOR/EXT. I/Ps
3 I/P NOR
3 I/P NOR/EXT. I/Ps
2 I/P NAND
2 I/P NAND/EXT. I/Ps
3 I/P NAND
3 I/P NAND/EXT. I/Ps
MED. BUFFER/INVERTER
2 I/P 2 NAND-NOR
2 I/P 2 OR—NAND
EXCLUSIVE-OR-INVERT
EXCLUSIVE-NOR-INVERT

SHIFT REGISTER
D-ELEMENT
LATCH ELEMENT

CLK GENERATOR FOR SR, SRD, MUX AND LATCH. GENERATORS COMPATIBLE WITH CELLS.

INPUT PROTECTION
OUTPUT INVERTER/BUFFER
OUTPUT TRISTATE/BUFFER
I/O TRISTATE/BUFFER

BASIC D-TYPE FLIP-FLOP (NCELLDTI)
A negative edge triggered flip-flop.



A.	POWER DISSIPATION	mW	1.8
B.	SUPPLY CURRENT	μA	360
C.	DELAY ESTIMATE		
	1) Output rising (from negative clock edge)	nS	160
	2) Output falling (from negative clock edge)	nS	80
	3) Data set up and hold time		40
D.	DELAY CALCULATION		
	1) Output rising		
	a) Intrinsic delay * (clock to output)	nS	51
	b) Diffusion interconnect loading	nS/gu	2.1
	c) Metal interconnect loading	nS/gu	1.4
	d) Output loading	nS/fi	2.0
	2) Output falling		
	a) Intrinsic delay (clock to output)	nS	35
	b) Diffusion interconnect loading	nS/gu	0.6
	c) Metal interconnect loading	nS/gu	0.6
	d) Output loading	nS/fi	0.8
	3) Data set up time	nS	38
	4) Data hold time	nS	38
E.	INPUT LOADING i) D	fi	2
	ii) Clock	fi	3
F.	MAXIMUM CLOCK FREQUENCY	MHz	8

* The delay due to the loading of the falling complementary output must be added to give the total delay to the rising output.

Plessey Semi-Custom LSI

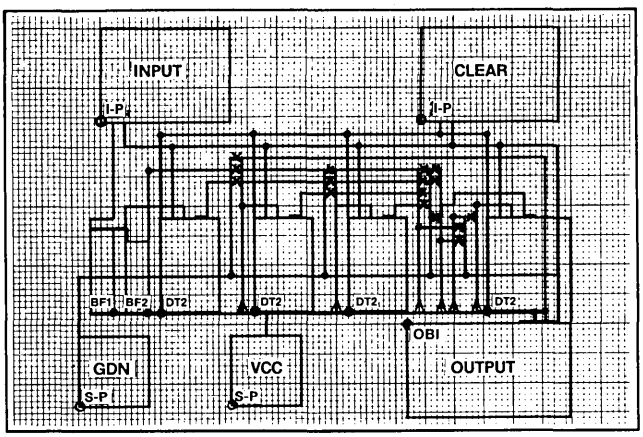
PLESSEY MICROCELL LSI.

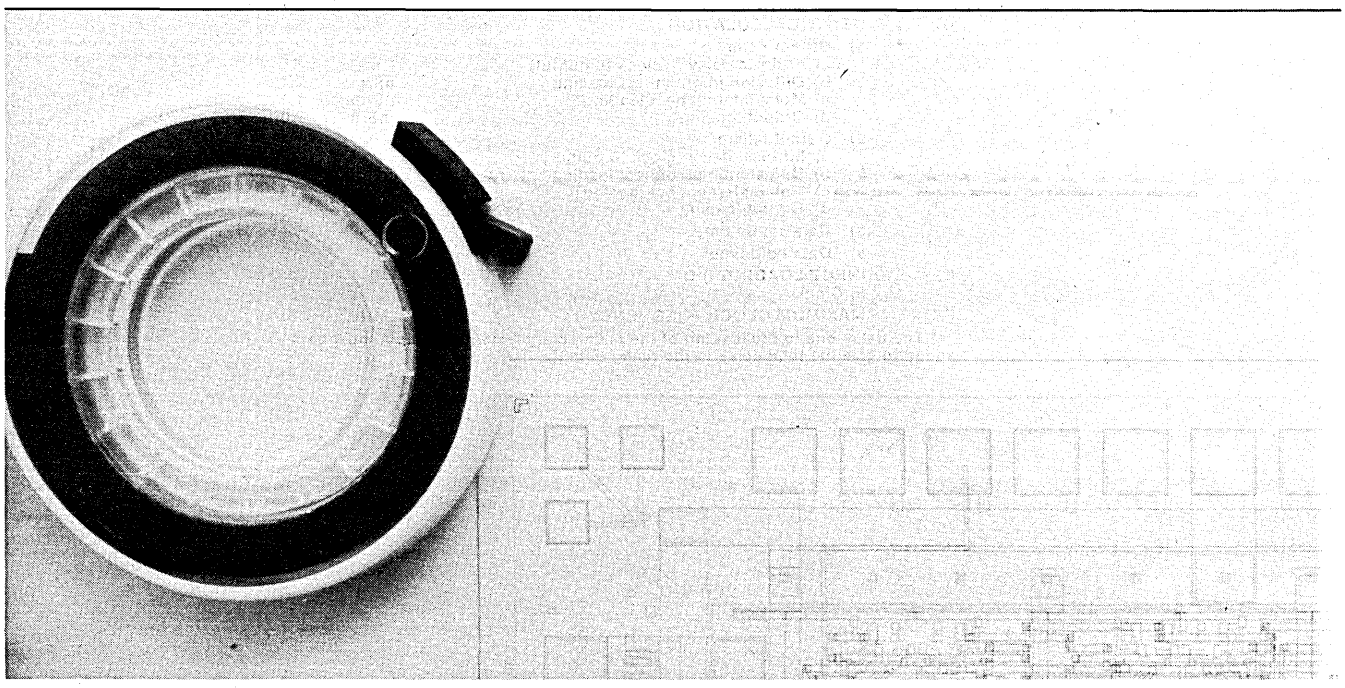
The MICROCELL concept falls between gate arrays and full custom IC's: you work with standard cells, but they are in a software library rather than already diffused into a silicon wafer. You get short development times (18 weeks for a prototype from your logic diagram) and 100% silicon utilization.

Logic functions are built up from a basic library of function cells which are not pre-positioned but can be called up and positioned wherever the system logic demands. When you specify a standard logic function, the computer selects the pattern for the function from a software library and produces a mask tape used to convert it to silicon. Since interconnection highways are not needed, die size is greatly reduced, increasing wafer yields and significantly lowering device cost.

Typical functions that you can select from our library are listed on page 12. These functions are fully characterized, with data sheets as detailed as those for any standard integrated circuit. You are not limited to the library functions, and can construct gating as complex as necessary by combining standard cells with additional gates.

Layout of your chip is about as straightforward as laying out a printed circuit board. The diagram below is typical of the detail required in a logic schematic for a 4-bit counter.

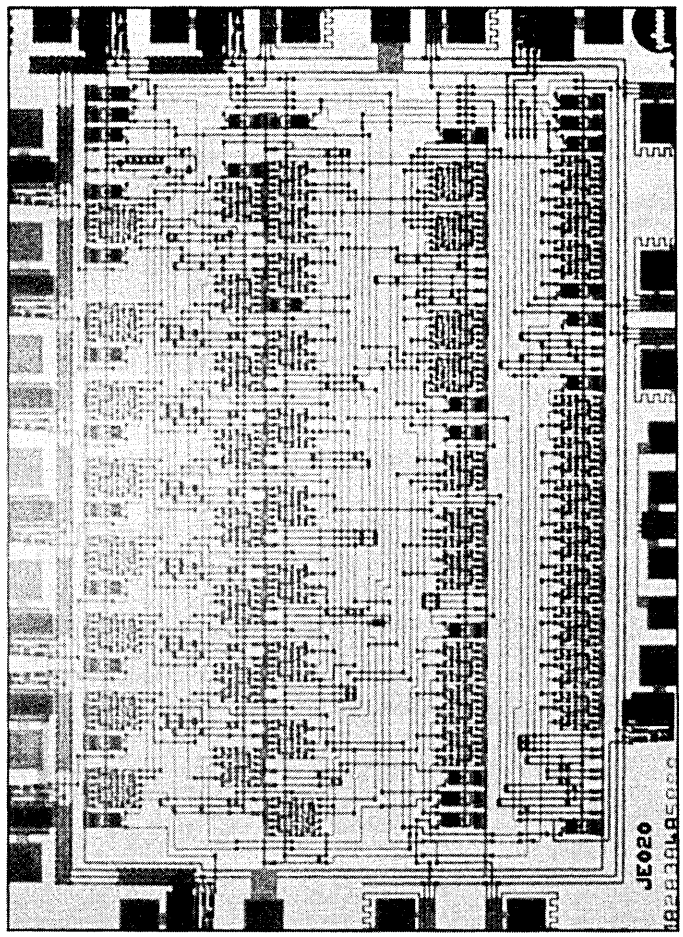




Plessey Semi-Custom LSI

Plessey then enters your schematic into a Calma digitizer using a special-purpose button menu with the standard Calma graphics and software. While the 4-bit counter circuit is quite simple, even the largest circuits can be digitized in only a few hours. The adjacent diagram is a Calma plot of the schematic diagram for a more complex integrated circuit.

Besides generating the tapes for making the masks, our complete CAD system also generates a logic description, complete with interconnection loading delays, from the digitized layout. This can be used for an accurate post-layout simulation and for generating the test program.



Plessey Semi-Custom LSI

PLESSEY ECL LSI GATE ARRAYS.

Plessey ECL LSI Gate Arrays are an economical solution to your need for high performance integrated circuits on a limited development budget.

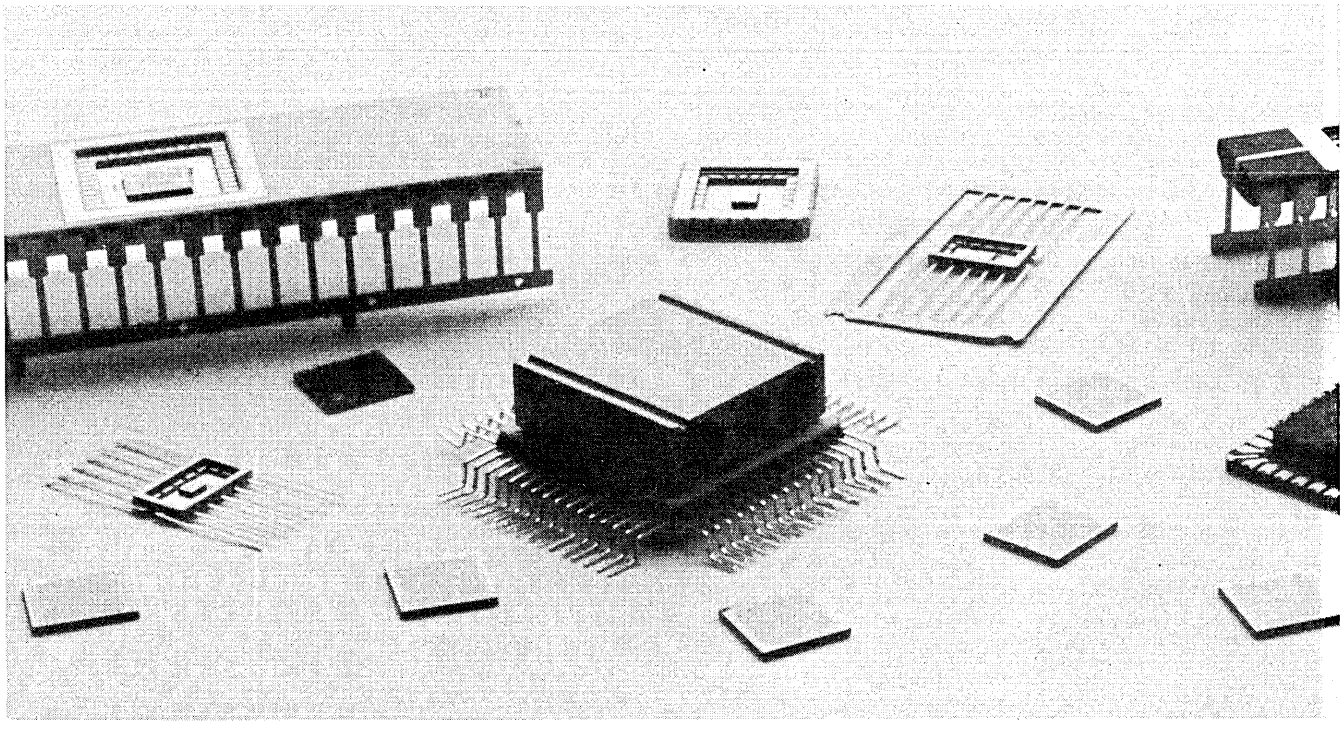
Fully-compatible with industry ECL 10K logic, our arrays are available in different speed/power versions and in different sizes to allow you to make the best choices for your systems.

The basic customization procedure for Microgate-E logic is similar to that for our CMOS LSI Arrays. You do not need any specialized knowledge of our processes to be able to produce your custom circuits with a high degree of confidence. Double-layer and triple-layer metallization with computer-aided interconnection allow you to achieve the maximum in performance, and chip area utilization as high as 100%.

After your design is specified, complete circuit operation is simulated on our computer before any fabrication is performed. The design is tested for normal and worst-case conditions, quiescent and dynamic, over the applicable temperature range to ensure proper operation.

Typically, you will have your first operational high-performance prototype in about 12 to 14 weeks even if you've never designed a custom IC before.

PRODUCT FAMILY	LAYERS OF INTER-CONNECT	NO. OF EQUIV. GATES	NO. OF PADS
SCD 1000	2 or 3	75	24
SCD 2000L	2 or 3	300	56
SCD 2000M	2 or 3	300	56
SCD 2000H	2 or 3	300	56
SCD 4000L	2 or 3	600	54
SCD 4000M	2 or 3	600	54
SCD 4000H	2 or 3	600	54
SCD 5000	2 or 3	1200	80



Plessey Semi-Custom LSI

THE BASIC MICROGATE-E ECL LOGIC CELLS.

ECL gate arrays are built up from basic cells that are already diffused into the silicon wafers.

The basic gate cell (called a "minor cell") consists of nine transistors and five resistors, the components necessary for a multi-output, two-input ECL OR/NOR gate. Optional connections allow this cell to be used for constructing more complex gates.

Four minor cells placed around a bias cell create a "major cell" that is used to produce the logic functions you need for your designs. The bias cell simply generates the industry-standard ECL 10K-compatible voltage reference and temperature coefficient.

A number of simple buffer cells are placed around the edges of the chip. These consist of a large transistor and a resistor, and may be programmed for logic input, logic output or as a power supply.

LOGIC INTERCONNECTIONS.

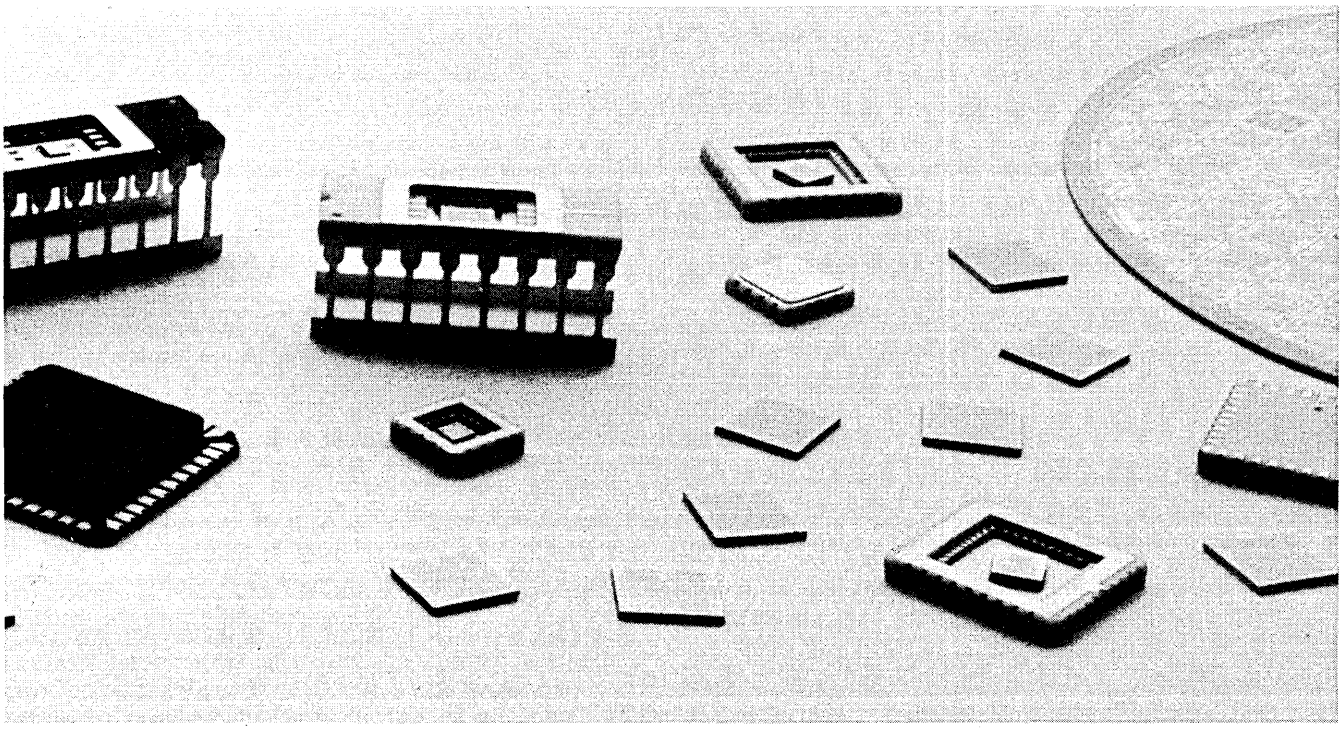
ECL LSI Gate Arrays are customized using multiple layers of metallization to maintain the high performance inherent in our technology. Up to 8 first layer tracks may pass over each major cell in the X direction, and up to 16 second layer tracks in the Y direction.

You start by specifying the functions you need from our library (listed on page 9). The computer provides the links to produce the chosen logic blocks using the first layer of metallization.

Now you specify the start and end points for interconnections between your logic functions, and let our computer perform the time-consuming and tedious task of routing the metallization tracks. If chip area utilization is over 90%, some manual interaction may be necessary, but typically the program will automatically route 95% of the interconnections for even the most complex circuit.

ECL PERFORMANCE CHART

	SCDS1000	SCD2000H	SCD2000M	SCD2000L	SCD4000H	SCD4000M	SCD4000L	SCD5000
NO. OF GATES	75	300	300	300	600	600	600	1200
NO. OF PADS	24	56	56	56	54	54	54	80
TYPICAL OR/NOR GATE DELAY	.5NSEC	.5NSEC	1.0NSEC	1.5NSEC	.5NSEC	1.0NSEC	1.5NSEC	1.5NSEC
TOGGLE FREQUENCY (D TYPE FLIP-FLOP)	400MHz	400MHz	250MHz	150MHz	400MHz	250MHz	150MHz	150MHz
APPROX GATE POWER	5MW	5MW	3MW	2MW	5MW	3MW	2MW	2MW
10K COMPATABILITY	YES	YES	YES	YES	YES	YES	YES	YES



Plessey Semi-Custom LSI

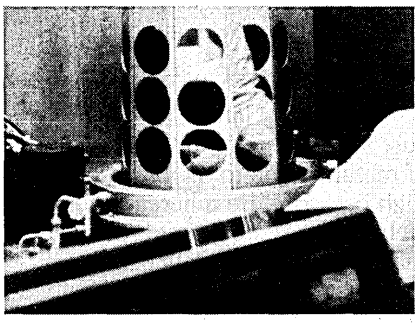
PLESSEY BIPOLAR ANALOG ARRAYS.

Plessey Microlin Bipolar Analog Arrays are a simple means of integrating your analog circuits.

As with our digital arrays, you get a short design cycle, low overhead, predictable performance and computer verification of your designs.

Our bipolar arrays consist of a pattern of transistors and resistors in fixed positions on a wafer. As with our digital arrays, these components are converted to the Microlin circuits you need by specifying the metal interconnection paths, much as you would when laying out a printed circuit board.

Plessey Analog LSI Arrays are fabricated using an industry-



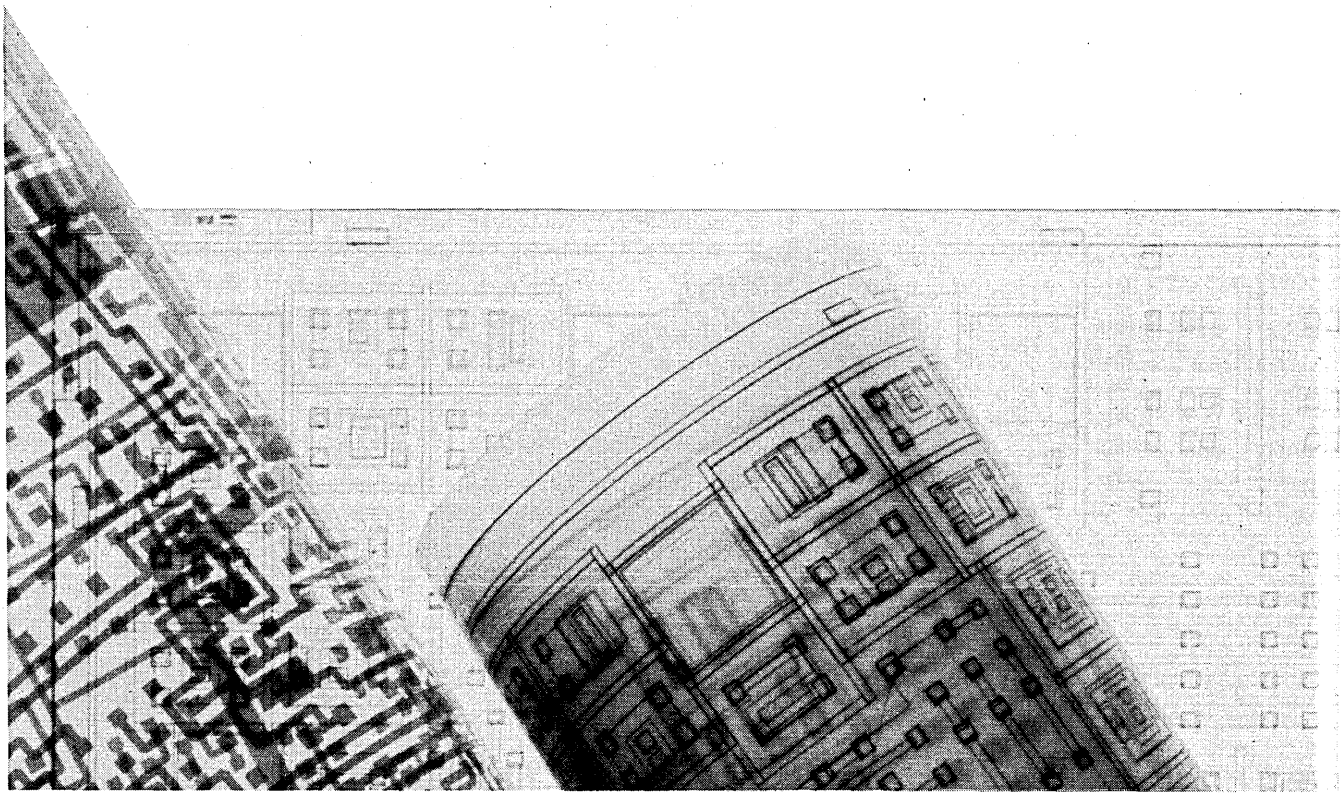
standard medium performance bipolar process. The components are fully tested and fully characterized. All the parasitics are also known, and accurate nominal and worst case computer simulations can be performed.

The result is that most circuits can be designed with no breadboarding. This can result in a significant saving in design time and much higher confidence in the finished design.

ANALOG LSI DESIGN CONSIDERATIONS.

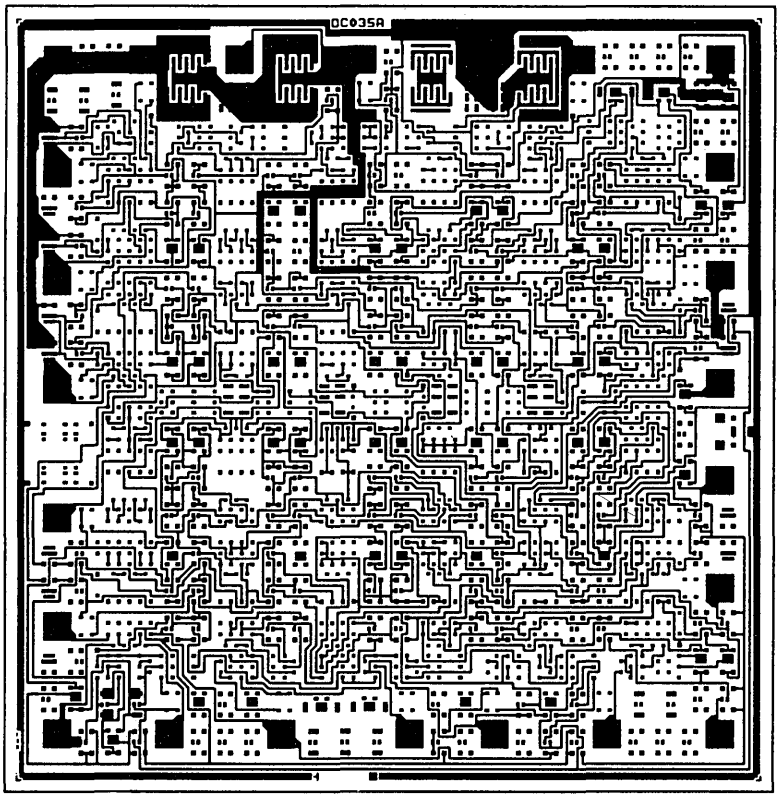
Integrated circuits have inherent limitations of tolerance and performance, but frequently these can be compensated for in your designs:

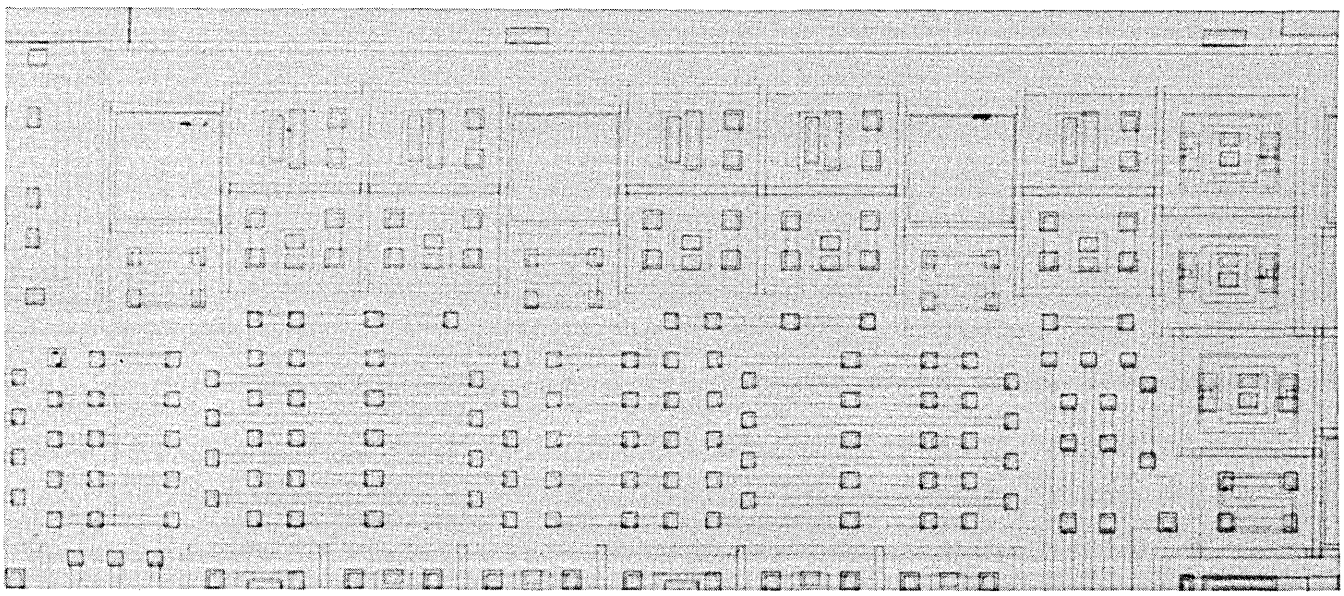
- Since absolute tolerances are large, but ratio tolerances are good, use techniques that depend on ratios (e.g. differential amplifiers, current mirrors).
- Circuits using lots of NPN's are easy to integrate and provide good performance up to a few tens of megahertz.
- Lateral PNP's have poor performance, but are well matched and useful where speed and gain are not important.



Plessey Semi-Custom LSI

- Transistors can be connected in parallel for higher currents or to produce current ratios.
- Use DC coupling exclusively if you can, since there are no on-chip capacitors.
- Minimize reactive components, since they must be off-chip and thus use up connecting pins.
- Make the design as modular as possible to minimize cross-connections.



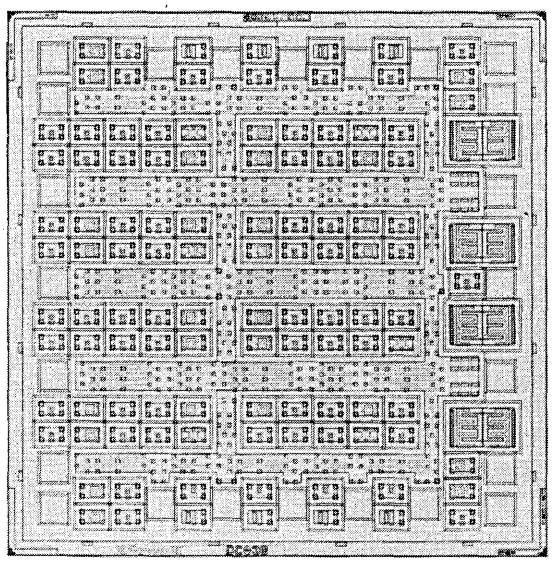


Plessey Semi-Custom LSI

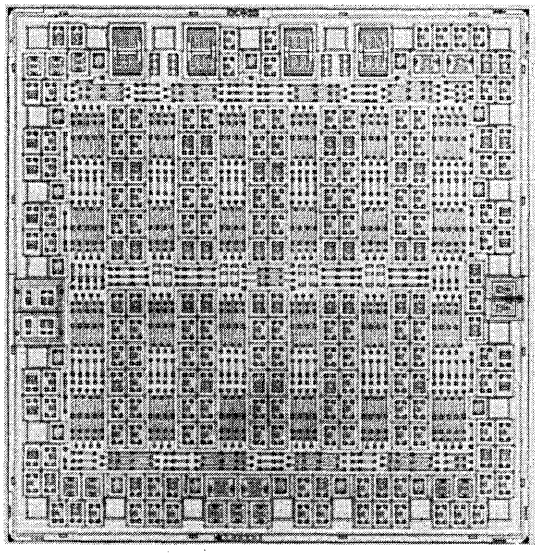
ANALOG ARRAYS	BAA 1000	BAA 2000
TRANSISTORS TOTAL NO.	109	221
RESISTORS TOTAL NO.	163	339
TOTAL BASE RESISTANCE	895K ohms	1.55Meg ohms
NO. OF PADS	24	24
LAYER OF INTERCONNECT	SINGLE	SINGLE
FT	500MHz	500MHz
ZENER VOLTAGE	7.1 Volts	7.1 Volts
BVceo	20V	20V
HFe (NPN) TYPICAL	100	100

	Gain			Ft (MHz)			Capacitance (pF)		
NPN	1μA	1mA	10mA	100μA	1mA	10mA	Cbc	Cl	Cbe
SMALL	90	120	110	140	450	400	.73	3.43	.54
MEDIUM	85	110	115	80	300	450	1.07	3.43	1.14
LARGE	75	105	120	10	80	450	9.53	12.0	13.0

	Gain			Ft (MHz)			Capacitance (pF)		
PNP	1μA	100μA	1mA	1μA	100μA	1mA	Cbc	Cl	Cbe
SMALL	18	30	10	3	5	2	1.72	3.43	.39



BAA 1000



BAA 2000

Plessey Semi-Custom LSI

COMPUTER AIDED DESIGN.

The demand for more complex, faster, smaller, less expensive integrated circuits can only be met by corresponding advances in computer-aided design.

Recognizing this aspect of custom design several years ago, Plessey Semiconductors has developed an advanced software system that will keep us on the leading edge of semi-custom technology.

We call our approach SCAMP —Semi-Custom Array Mask Production. It is a complete system that extends from initial circuit layout data capture to verified mask production. SCAMP quickly turns a new design into a prototype, with a very high probability of obtaining the correct circuit the first time through the loop.

SCAMP is based on the concept of software modules, with a central core that remains constant irrespective of technology or circuit complexities in the IC designs. The system can be readily extended to future design methodologies and integrated circuit technologies.

SCAMP can be used at a Plessey design center, from within your company using a single terminal and modem, or running on your own integrated graphics system. The central SCAMP algorithms have been especially designed and otpimized to reduce elapsed terminal time and to use computer resources efficiently to keep costs down.

Because SCAMP is relatively technology independent, it can be used with the following technologies and methodologies.

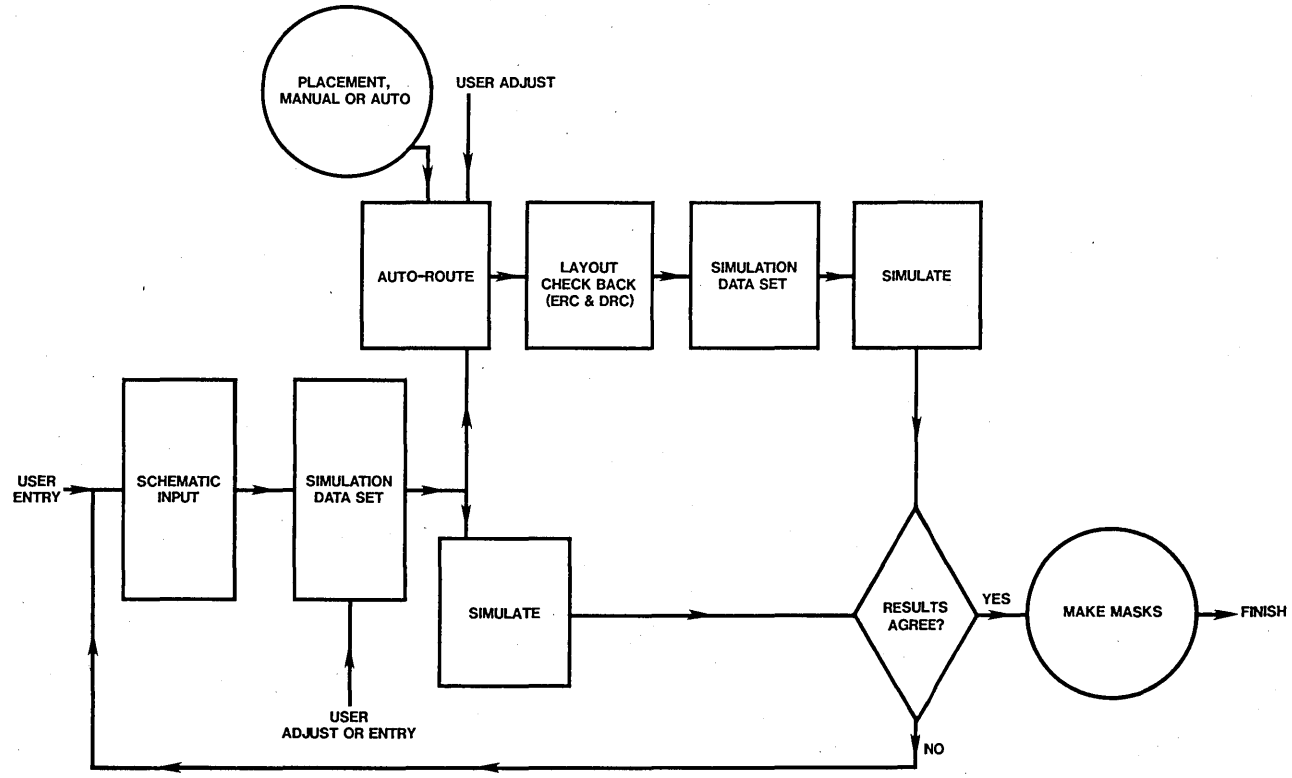
	Single Layer Metal			Double Layer Metal	
Methodology	Bipolar	N Channel	CMOS	Bipolar	CMOS
MICROCELL		X	X		X
LINEAR ARRAY	X			X	
LOGIC ARRAYS	X		X	X	X

The system schematic below gives an overview of SCAMP operation and shows the key elements that make design throughout faster and more reliable.

The digitized schematic input is first used to develop a data set for final device testing and for a direct functional simulation. Logic cells are automatically placed, then metallization is automatically routed on the chip. With auto-routing, a design step that previously took days or weeks is now done in minutes.

This layout is then checked against design and electrical rules (placement, spacings, fan-out, etc.). If it satisfies these, a second simulation is run. When the results of both simulations match, the masks are made.

The end result is prototypes that work the first time virtually every time.



Plessey Semi-Custom LSI

FABRICATION AND TESTING.

With the layouts complete and simulations run, digitization, checking and production of the masks is simple and straightforward.

We can then provide you with probed slices, chips or packaged devices. We can use any commercially-available or customer-supplied package, but it should be selected early in your design, as it may affect the size of array used and the power dissipation that can be tolerated.

The next important step is testing, and the test specification should form part of your target specifications.

Testing is a major consideration in semi-custom LSI because volumes are usually low. For high volume IC's, the effort expended to obtain good, economical tests is spread over the cost of a large number of devices. When the development cost is spread over a much smaller number of devices, a compromise may be necessary.

Electrical testing is done on the wafer before division into chips, followed by final testing after encapsulation.

At wafer probe, each chip on every slice is tested. On the basis of these tests, all chips which are not expected to pass the final test program are marked for rejection, while the cost of scrap is still relatively low.

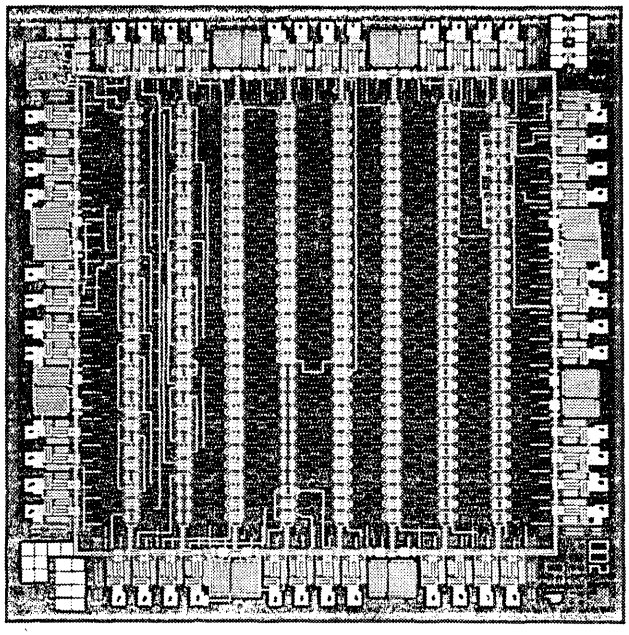
For the final tests after encapsulation and packaging, devices are normally tested at an ambient of 25°C. Facilities also exist for hot and cold testing, lot-by-lot release and burn-in.

The equipment used for all probing and most final testing is computer controlled and ranges from the Fairchild Sentry Series to systems specially developed at Plessey.

Depending on your applications, our semi-custom and custom IC's are available to meet the most stringent commercial, industrial and military specifications.

Plessey Semiconductors
Semi-Custom Operations
1641 Kaiser Avenue
Irvine, CA 92714 U.S.A.
TWX 910-595-1930.

Custom and Semicustom LSI



Features

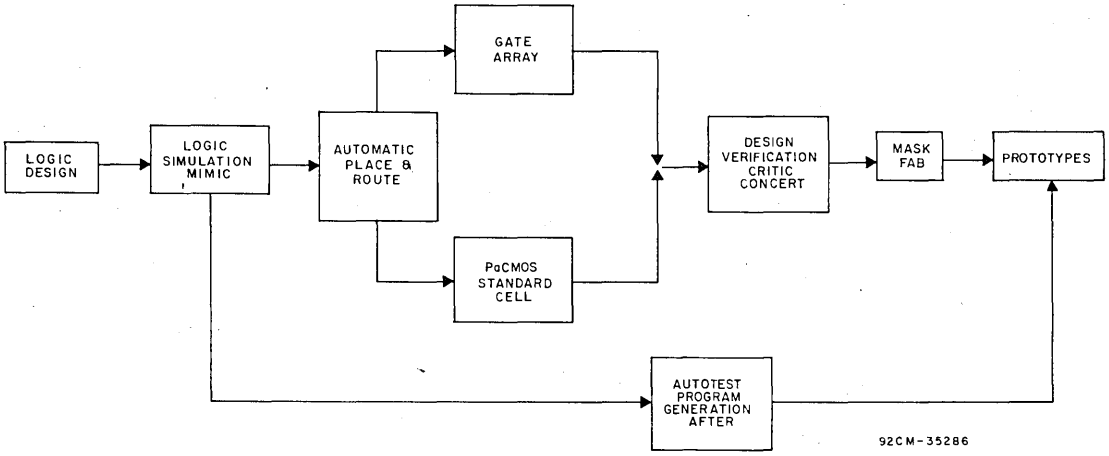
- **Full Range of Cost-Effective Design Capabilities**
  Gate Arrays—automatic and manual
  Metal Gates CMOS—C²L CMOS—
  CMOS I (5μ) — CMOS II (3μ)
  PaCMOS — standard cells
  Full Custom LSI
- **Fully Supported Design Automation**
  MIMIC—logic simulation
  CRITIC—design rule vertification
  AFTER—test program generation
  CONCERT—connectivity check
- **Long Experience**
  More than 15 years of custom/semicustom service to demanding customers.

Comparison Of Custom/Semicustom LSI Options*

	Semicustom		*Full Custom*
	Gate Array	**PaCMOS Std. Cell**	
Development Cost	0.2	0.3	1
Development Time	0.17	0.23	1
Risk (1st time success)	0.5	0.5	1
Final Die Size	1.5-2.0	1.1-1.4	1
Production Die Cost	3-4	1.5-2.0	1
Efficiency of Chip Utilization	0.8	1	1

*All comparisons normalized to a full custom basis assuming a 1000 gate complexity function.

RCA Design Automation System



RCA's Semicustom Capabilities

RCA presently offers a variety of GAs classified according to:

Gate complexity	138 to 1200 gates
Process technology	CMOS metal gate (bulk CMOS)—Manual layout
	CMOS silicon gate (C^2L)—Manual layout
	CMOS silicon on sapphire (CMOS/SOS)—Manual layout
	CMOS I—Automated layout
Package types	Plastic
	Ceramic
	Side-brazed ceramic
	Leadless chip carrier

RCA will soon offer additional Automated Universal Arrays (AUAs). The interconnect mask patterns for AUAs are generated solely by user-accessible software via the techniques of design automation (DA). AUAs are classified according to:

Gate complexity	800 to 5000 gates
Process technology	CMOS I
	CMOS II
	CMOS/SOS
Package types	Plastic
	Ceramic
	Side-brazed ceramic
	Leadless chip carrier

RCA presently offers a variety of APAR cell libraries.

Gate complexity	User defined
Process technology	CMOS silicon gate (C_2L)
	CMOS silicon on sapphire (CMOS/SOS)
	CMOS I — 5 μ bulk CMOS
Package types	Plastic
	Ceramic
	Side-brazed ceramic
	Leadless chip carrier

RCA will soon offer additional APAR cell libraries. They are classified by:

Process technology	CMOS II
	CMOS/SOS
Package types	Plastic
	Ceramic
	Side-brazed ceramic
	Leadless chip carrier

AUTOMATED GATE ARRAYS

	Types	Total Gates	Internal Gates	Array Size (mils)	Total Pads	Projected Availability
CMOS I (5μ)	PA20250	317	264	168 x 150	46	NOW
	PA20450	517	440	168 x 214	66	NOW
	PA20650	735	640	216 x 214	78	NOW
	PA20850	953	840	264 x 214	90	NOW
	PA21000	1133	1008	264 x 246	98	NOW
CMOS/SOS (4μ)	PA60650	725	640	208 x 208	74	NOW
	PA61200	1313	1176	256 x 272	102	NOW
CMOS II (3μ)	PA40650	725	640	181 x 191	74	4Q82
	PA40850	953	840	221 x 191	86	4Q82
	PA41000	1133	1008	221 x 220	94	4Q82
	PA41200	1313	1176	221 x 249	102	4Q82
	—	1900	—	—	126	2Q83
	—	2500	—	—	—	2Q83
	—	5000	—	—	220	4Q83
CMOS/SOS (2μ)	—	2500	—	—	—	1Q84

MANUAL GATE ARRAYS

Metal Gate CMOS	MA30150	168	138	189 x 188	40	NOW
	MA30250	276	240	229 x 232	48	NOW
Silicon Gate CMOS (C^2L)	MA10150	168	138	156 x 155	40	NOW
	MA10250	276	240	186 x 188	48	NOW
	MA10350	400	370	216 x 220	48	NOW
	MA10500	576	528	245 x 252	64	NOW
CMOS/SOS	MA60150	182	144	150 x 150	40	NOW
	MA60250	300	256	180 x 180	48	NOW
	MA60400	452	400	210 x 210	64	NOW
	MA60550	632	576	240 x 240	64	NOW
	MA60800	848	784	270 x 270	80	NOW

Automated GAs
The latest step in RCA Semicustom LSI

- **Easy to Design and Change**
- **Fast Turnaround**
- **CMOS Performance**
- **Wafer Stockpiling**
- **CAD Compatible**
- **Library of Logic Macros**

As gate counts and design complexities increase, manual layout of GAs becomes costly and time consuming. Therefore, RCA has developed automated placement and routing techniques.

The Automated GA System requires only one unique metal mask level. Artwork for this level is generated automatically from RCA's extensive library of logic cells.

The metal mask describes the required logic functions on the array and then defines a unique interconnect pattern. Artwork for the mask is generated automatically from RCA's extensive library of logic macros (predefined logic structures or cells). Most RCA logic macros are common for both GAs and PaCMOS standard cells. The design process for GA and PaCMOS is essentially common and may be transparent to the designer.

Automated GA software has proved to be very effective, providing 100% connectivity and gate utilization up to 98% for complex random logic applications.

PERIPHERAL FUNCTIONS

Each of the input/output pads of an RCA GA has a spark gap (on CMOS/SOS) and gated diode circuit to protect against static discharge. An n device and a p device are also associated with each pad and can be used as an input inverter, an output inverter, or as a transmission gate.

To provide longer delays and active pull-up resistors, high-impedance cells are placed strategically along the periphery of the GA. In order to source and sink TTL levels of current or to drive off-chip capacitive loads at high speed, low-impedance cells are also provided along each side of the array.

Two high-speed binary dividers, without set or reset, are available in each SOS GA. Capable of operating as high as 100 MHz, they can be used singly as pre-scalers for division by two or in cascade for division by four.

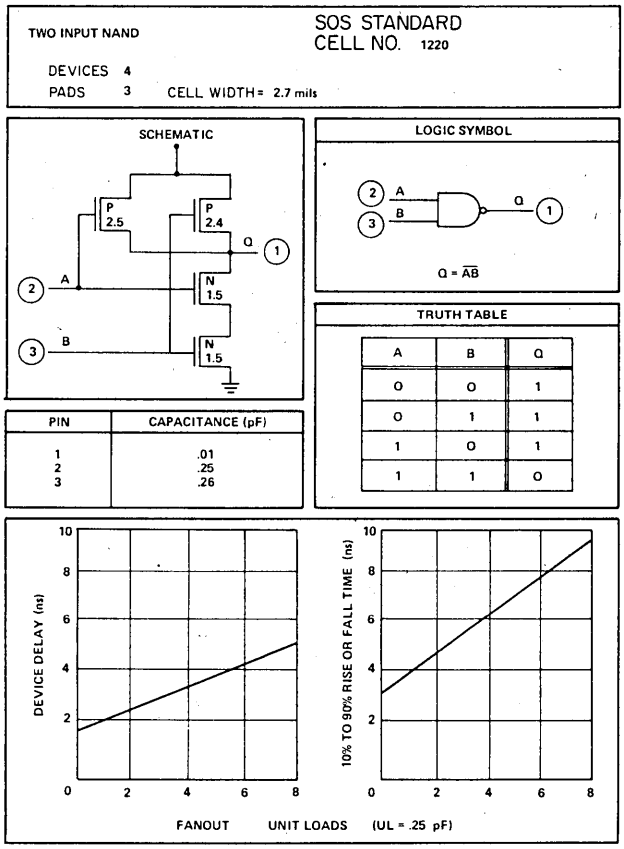
PaCMOS
(Programmable Automated Cell CMOS) Standard Cells

PaCMOS is an RCA computer-automated design approach to LSI. It is based on a group of circuit building blocks, called standard cells, that can be automatically chosen, placed, and interconnected by a computer program.

RCA has a large and expanding library of previously designed, verified, and life-tested standard cells—available in metal-gate CMOS, C²L (closed-geometry silicon-gate CMOS-bulk), and silicon-gate CMOS on sapphire substrate. Some of their characteristics are summarized below.

As a design aid in selecting appropriate cells, a standard cell notebook is available. In it, all of the logic cells are fully characterized and documented in the form of data sheets. A typical data sheet is shown.

It provides the name and function of the cell, in this case a 2-Input NAND, the circuit and logic configuration, the Boolean equation, the truth table, and the dynamic performance data.



By using the standard cell notebook, the designer can match his particular circuit configuration with the available standard cells and generate an input net list. Each multiport standard cell is characterized by its input and output pin connections. Pin connections are accessible for interconnect wiring at both the top and bottom of each cell. Sophisticated algorithms automatically select the most appropriate I/O connections to minimize wire length and area and to produce a densely packed, efficient layout. This structured computerized layout also simplifies the checking of both interconnection and design rules. Because each individual cell has been previously verified, only the computer-generated interconnections must be checked.

PaCMOS CELL CHARACTERISTICS

	Metal gate	C²L	SOS	CMOS I
Cell Height, mils	14.0	12.6	4.2	6.72
Pin Spacing, mils	1.9	0.8	0.9	0.56
Channell Length, microns	7.5	6.2	5.0	5.0
Delay, nanoseconds[1]	20.0	10.0	6.0	6.0[2]
Internal Logic Density	8-21	6-10	2-3	1.5-3
Overall Chip Density	40-50	12-30	14-18	6-10

(1) Stage delay = 2 inut NOR, fanout = 2
10 volts, no interconnect
(2) 5 volt stage delay

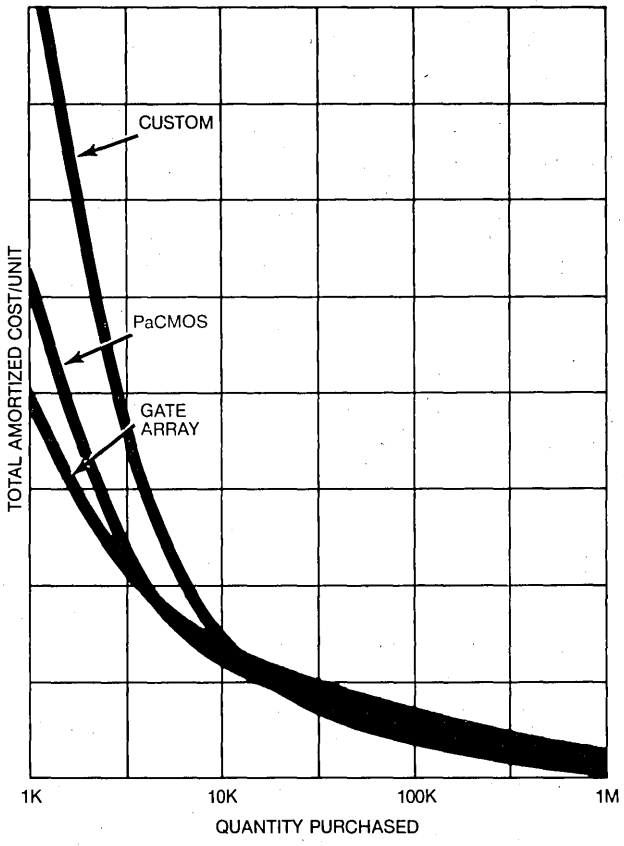
ADDED OPTIONS

In addition to the standard cells, PaCMOS can also accommodate subchip options. Regular structures such as RAMs, ROMs, PLAs, PROMs, EPROMS, and register stacks, which have been remotely designed by conventional handcrafted techniques, can be automatically connected while the remainder of the host chip is computer generated. The net effect of incorporating the subchip option into the standard cell layout is to combine the high density and performance optimization associated with handcrafted designs with the low-cost, quick-turnaround capability that the standard cell automatic layout program provides.

Another option available in PaCMOS is a critical path technique. Under ordinary circumstances, the placement and routing of algorithms place all cells on the chip in a manner to minimize total wire lengths and crossovers. When the critical path option is selected, the program will place those cells identified as part of each critical path, not only as close to each other as possible, but also in a manner to maximize the use of metal for interconnections, as opposed to the somewhat higher resistivity polysilicon interconnects.

PaCMOS VERSUS GA

A PaCMOS semicustom LSI offers attractive tradeoffs between development time, die size, and cost for many IC designs. Although its development time is slightly longer than a gate array, its die size is smaller. And in volume production PaCMOS can provide significant cost advances over GA designs.



Design Automated Tools

- MIMIC
- CRITIC
- AFTER
- CONCERT

MIMIC, RCA'S SOFTWARE SIMULATION PROGRAM

A powerful software simulation program, called MIMIC, allows designers of GAs, as well as other RCA semicustom and custom LSI devices, to model the logical operation of digital circuits before device fabrication. Through the program, designers can discover logical flaws, race, hazard, or spike conditions, and timing and critical path uncertainies.

The entire software program, including a standard cell library, is available to customers through RCA's commercial computer services in Cherry Hill, N.J.

MIMIC, has a number of features that contribute to its effectiveness:

☐ It models circuit elements such as bus connections, wire-tied elements, and bidirectional transmission gates.

☐ It is supported by an extensive library of built-in logic elements including gates, latches, clocked flip-flops, and multiplexers.

☐ Through its hierarchal network-description, designers can define their own standard library of common circuit elements.

☐ It is capable of generating a variety of output reports whose contents and format are largely user-defined.

☐ And, perhaps most important, it has the ability to generate a test-pattern file acceptable as an input to automatic test equipment. Because the number of test patterns increases exponentially with the complexity of a design, this ATE interface can materially reduce test times and costs.

CRITIC (Computer Recognition of Illegal Technology in Integrated Circuits)

Another software tool available in the design of GAs, as well as other RCA semicustom and custom LSI devices, is the CRITIC program. An acronym for Computer Recognition of Illegal Technology in Integrated Circuits, CRITIC checks mask artwork by describing the mask as a series of polygons in terms of the vertices that define them. The program then automatically searches for and reports on minimum tolerance violations (width, spacing, and enclosure) and illegal topology relations (overlap, abut, cross, contain, and disjoint).

DESIGN AUTOMATION PROGRAMS

AFTER

The AFTER program (*A*utomatic *F*unctional *T*est *E*ncoding *R*outine) aids the IC designer in generating functional test patterns required for the testing of digital IC's on Automatic Test Equipment (ATE). Input/output truth tables, representing these tests, can be created by the designer using the MIMIC logic simulation program by specifying the IC's inputs to MIMIC; its outputs are calculated by MIMIC. Alternatively, AFTER provides an option for a high level manually generated test specification (both inputs and expected outputs). AFTER automatically translates either type of input into test patterns suitable for execution on a variety of ATEs. ATEs currently supported are the Fairchild Sentry/Sentinel/Series 20, the Teradyne J283, and the Datatron test systems.

CONCERT

(*CON*nectivity *CERT*ification) is a layout analysis program which aids the verification of the logical and electrical correctness of the mask artwork produced by the APAR automatic layout programs. The layout generated by RCA's APAR programs (MP2D and GA) consists of standard cell placements and wire interconnects. By examining this information, CONCERT can extract a net list from the artwork and automatically produce the logic description in the exact language required by the MIMIC logic simulator. This is used to verify corrections of the wiring.

Ordinarily, since the IC layout is computer generated, no errors will be found. However, in those cases where the designer chooses to perform some manual modifications, CONCERT is an important tool for validating the changes. In addition, parasitic capacitances of the interconnections, as laid out, are added to the MIMIC network description file. This provides the designer with the ability to effectively simulate the physical layout itself including layout parasitics. This re-simulation increases confidence that the layout is free from timing problems caused by the possibly excessive capacitance of signal lines. These capabilities make CONCERT a key ingredient in producing quick-turnaround custom chips that work to specifications the first time through.

BIPOLAR LSI SEMICUSTOM ACE/CCL/8AXXXX SERIES

PRODUCT DESCRIPTION

The Signetics family of high speed bipolar semicustom offers a viable means of replacing ECL, 74S or 74LS logic components with a proprietary LSI device. The primary advantages are reduced size, weight, and power, improved system reliability, and significant manufacturing cost savings. These devices also offer full −55°C to +125°C temperature range, and have superior radiation-hardened properties.

8AXXXX Series Gate Arrays

Gate Arrays employ a fixed array of gates and I/O's which can be "personalized" by custom metalization. The 8AXXXX Series, with a maximum of 2100 gates/chip and gate delays of 4 to 6ns, can replace up to 100 SSI/MSI devices in any LS application. By reducing device count and saving PCB area, 8AXXXX devices can improve IC system reliability by 100 times and save 80% in manufacturing costs. The ISL gate only dissipates 250μW maximum which reduces power consumption by 10 times as compared with a 74LS implementation.

To attain 74LS speeds with LSI packing density and low power, Signetics gate arrays use integrated Schottky Logic (ISL), a proprietary gate design implemented in a standard bipolar process.

Composite Cell Logic

CCL uses functional logic cells which can be placed on the chip and interconnected by metalization. The cells are equivalent to standard SSI/MSI logic functions; hence, design is similar to the usual "catalog" PCB approach.

With CCL the designer can choose from two libraries: the EPL Library, with 3ns or 4ns typical gate delay for 74S applications; and the ISL Library, with 6ns worst case delay for 74LS applications. Like ISL gate arrays, CCL offers significant improvements in power usage, system reliability, and system manufacturing economy.

Current technology allows up to 600 EPL gates or 1000 ISL gates on a chip, with I/O's limited by available packages.

ACE Masterslice Logic Arrays

The Masterslice array uses composite cells but requires them to be placed at fixed locations. Design is similar to the "catalog" approach but analogous to a PCB having fixed socket locations. The cell library contains a full contingent of standard SSI/MSI functions.

With 500 psec gate delays and elimination of PCB traces, ACE Masterslice arrays offer a 50% speed increase as compared with standard 100K ECL. They also reduce power dissipation by 75% and implementation costs by 55%.

FEATURES

- 0.5ns, 3ns, 4ns or 6ns Gate Delay
- Up to 2200 Gates/Chip
- 250μW to 6mW Per Gate
- Up to 128 I/O's
- Up to 80mA Drive
- −55°C to +125°C
- Radiation Hardened
- Plastic or Ceramic DIP's
- Leadless Chip Carriers
- Space Array Packages

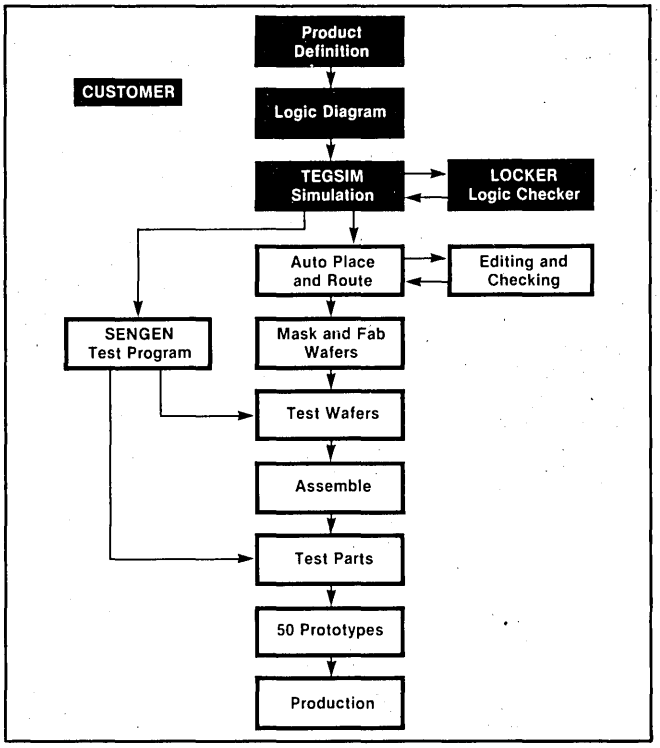
BENEFITS

- Proprietary LSI Device
- Replaces ECL, 74S or 74LS Devices
- Reduces PCB Area
- Saves Manufacturing Costs
- Reduces Size, Weight and Power
- Improves System Reliability

PROGRAM

- Easy Logic Simulation
- Comprehensive Design Seminars
- Complete Documentation
- Fast Development Cycle
- Extensive CAD Testing
- Ensures First-Pass Success
- Full Design Support

SEMICUSTOM PROGRAM



Signetics

BIPOLAR LSI SEMICUSTOM ACE/CCL/8AXXXX SERIES

Signetics ACE Masterslice arrays achieve their high speed by use of a CML gate implemented with the P-Subilo process. Current ACE products have from 600 to 2200 gates and 58 to 128 I/Os.

Designing With Semicustom

Signetics Bipolar LSI Semicustom devices have well-defined parameters to simplify design and allow extensive use of computer aides. This speeds device development, simplifies the Signetics-Customer interface and ensures first-pass success.

To design a semicustom chip, the customer uses any standard terminal with Signetics time-shared TEGSIM software. The designer merely describes the circuit and input test sequence. The TEGSIM software simulates the logic function, generates the output waveforms and fault-grades the circuit.

The customer submits the simulation result as a specification. Signetics then lays out the chip, runs additional CAD tests to ensure design integrity, and builds first prototypes. The customer-defined test sequence is used to test the device and is available on tape for customer use in device testing.

Total Product

Signetics bipolar semicustom products are on the forefront of technology, both in silicon and in software. Semicustom devices combine high speed, low power and high packing density for optimum performance and low device cost. The semicustom development program makes extensive use of CAD and is devised to simplify the Signetics-customer interface yet provide fast turn-around with ensured success. Customers using the program have come to expect close rapport with Signetics technical personnel and full support through design completion.

ISL Gate Arrays, 5 or 6nsec Delay*

Part No.	Gates	Internal Buffers	I/O Pads
8A1200	1144	52	36
8A1260	1144	52	62
8A1542	1408	64	42
8A1664	1560	60	64
8A2176	2016	72	76

*Variety of packages, Temperature: 0 to 70°C or −55 to 125°C. Gates use 250μW/gate maximum.

Composite Cell Logic, 3 to 6nsec Delay*

Library	Power/Gate (Max*)	Equivalent Gate Delay (Max)	Trace-Length Delay	Gates (Max)
EPL	5.6mW	3.0nsec	Negligible	300
	2.6mW	4.0nsec	Negligible	600
ISL	0.3mW	6.0nsec	50psec/mil	1000

*Temperature range: 0 to 70°C or −55 to 125°C. Variety of packages; pin-out limited by package.

ACE Series Masterslice Arrays, 0.5nsec Delay*

Part No.	Gates	RAM	I/O Pads*	Power Pads	Power (Typical)
ACE600	638	—	58	6	1.8W
ACE900	878	—	74	6	2.3W
ACE1320M	1000	320	96	20	3.5W
ACE1400	1414	—	96	20	3.5W
ACE2200	2204	—	128	20	5W

*Package is pin grid array, air cooled, heat sink optional. Temperature range: 0 to 70°C.

NOTE
All delay times are worst case numbers. This allows computer simulation under worst case conditions to ensure circuit functionality and first-pass success. Typical delay times are much lower than worst case.

GATE ARRAY SCC700

Preliminary

DESCRIPTION

The Signetics SCC700 Gate Array is a single chip programmable device that allows customization of user logic. Only metalization and contact are programmed in this state-of-the-art CMOS device. Thus, fast turn-around from logic to completed silicon is achieved.

The SCC700 is one of a family of low-power gate arrays in oxide-isolated CMOS (LOCMOS). It contains 352 identical cell-units (see figure 1) which are interconnected by two custom masks (metal and contacts). Each unit contains four pairs of N- and P-transistors and thus the complete array contains a total of 704 two-input gate equivalents. Access to the transistors is from both the top and bottom of the cells and additionally there are two poly feed-throughs at each side of the cell. Because of this routing flexibility, many designs result in better than 90% utilization of the gates available.

The SCC700 Gate Array is built on the mature LOCMOS process. LOCMOS is a state-of-the-art Si-gate CMOS process which uses an epi-substrate, which significantly reduces the potential for latch as compared with other bulk CMOS processes.

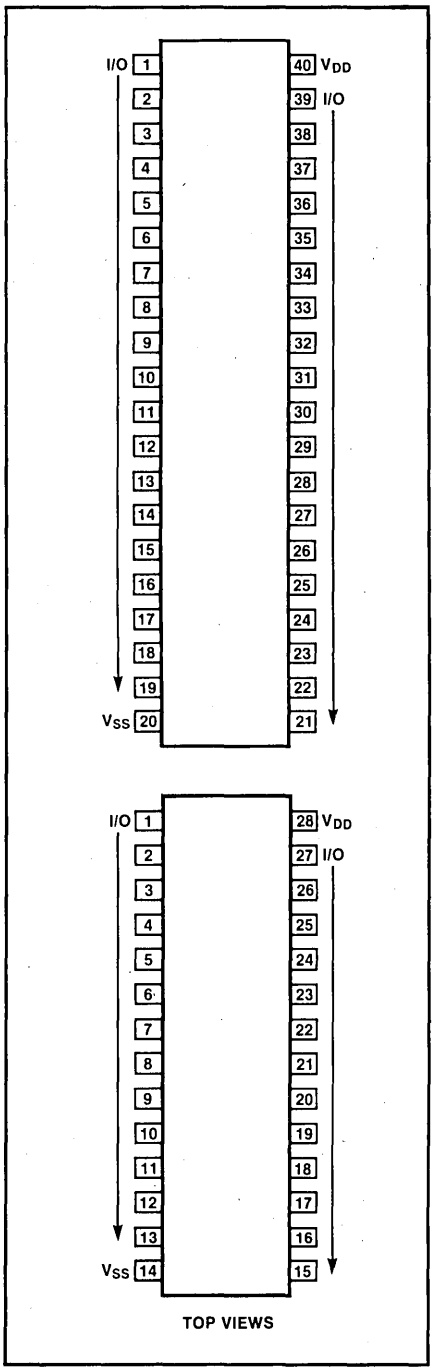
FEATURES

- **704 two input gate equivalents[1]**
- **Power supply range 3 to 15V**
- **High speed silicon gate technology with local oxidation (LOCMOS)**
- **12MHz typical clock rate at 10V**
- **Very low power consumption (standby power 0.25mW)**
- **High noise immunity**
- **Input protection by series resistor and diode clamp to V_{SS}**
- **TTL outputs (buffers) drive up to four LSTTL loads**
- **Full CAD for quick, error-free design**
- **38 versatile I/O pins, each having a wide range of functions**
- **48 pre-designed, fully characterized library of logic cells available**
- **Over 90% maximum utilization typical**
- **−40°C to +85°C operating temperature**
- **40- and 28-lead DIL packages**

Computer aided design (CAD) is used throughout the design process to insure accurate implementation of customer logic (see figure 2 for a typical process flow structure).

[1] Future arrays available are 0330, 0440, 1100, and 1700 gate-equivalents.

PIN CONFIGURATION



TOP VIEWS

ORDERING CODE

PACKAGES	V_{DD} = 3 to 15V, T_A = −40°C to +85°C	
	28-Pin	40-Pin
Ceramic DIP	SCC0700CCGI28	SCC0700CCGI40
Plastic DIP	SCC0700CCGN28	SCC0700CCGN40

CMOS GATE ARRAY PART NUMBERING SYSTEM

SC C 0700 C C G N 28

- MOS Microprocessor Division — Identifier — Always SC
- Process Variation — C = CMOS
- Basic Part Number — 0330, 0440, 0700, 1100, 1700
- Special Array Code — C = Custom, S = Standard
- Temperature Range — C = 0°C to +70°C (Commercial); A = −40°C to +85°C (Automotive); M = −55°C to +125°C (Military)
- Timing Variation — G = Medium speed wafers; H = High speed wafers (Also see appropriate data sheet)
- Package — I = Ceramic; N = Plastic
- Pin Count 28, 40, 68

Signetics

CUSTOM/SEMICUSTOM

GATE ARRAY SCC700

Preliminary

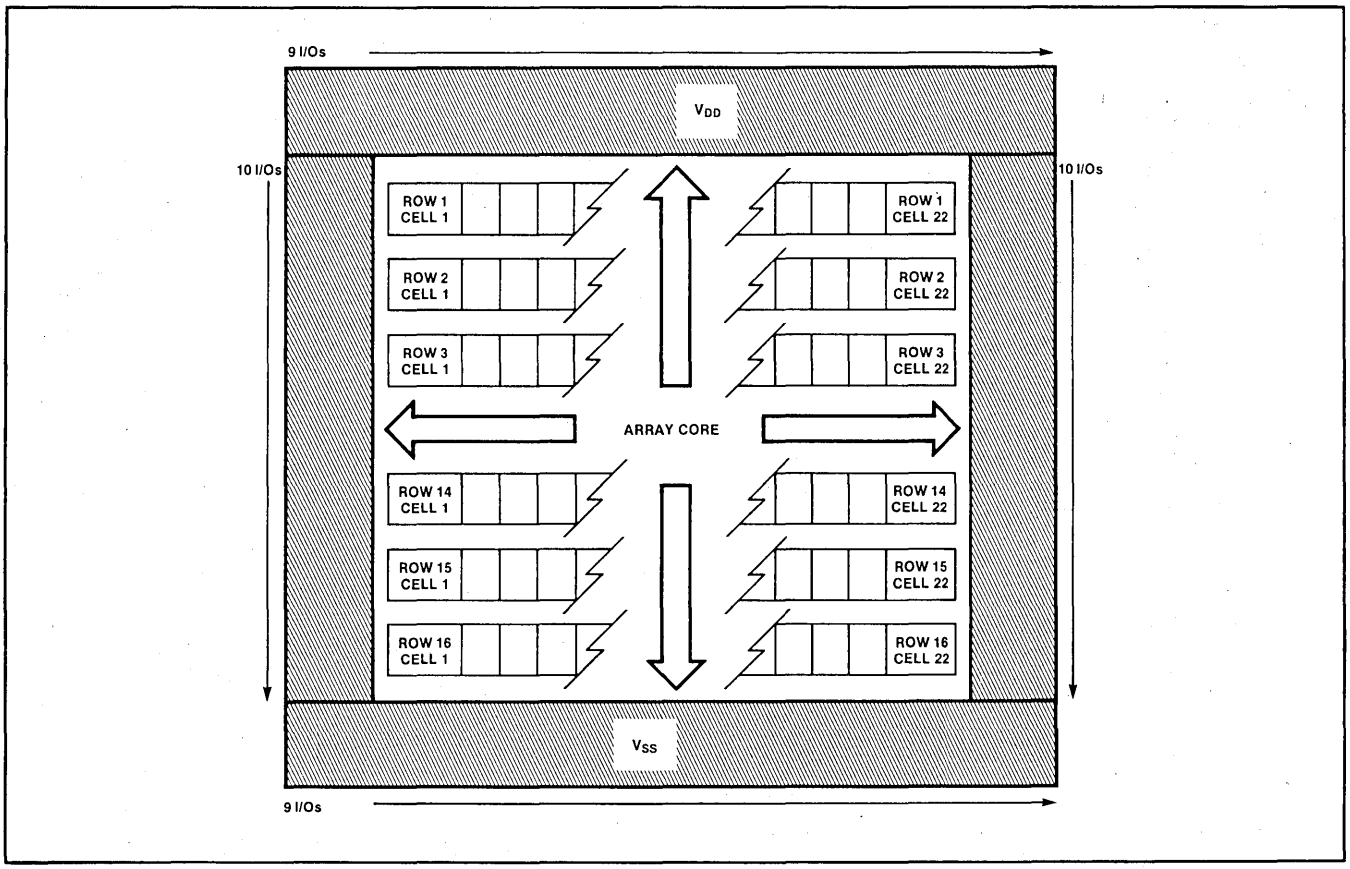


Figure 1. Topological Diagram

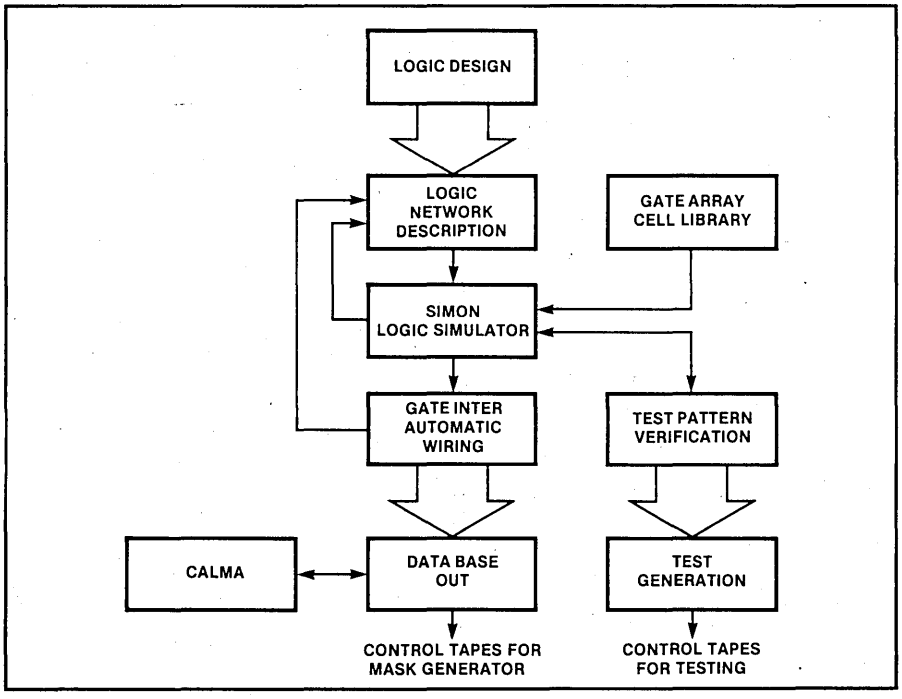


Figure 2. CAD Flow Chart

CELL LIBRARY

To facilitate design, a library of 48 pre-designed, fully-characterized overlay cells is available in the CAD package. The library contains:

- 16 simple logic functions including:
  2-, 3-, 4-input NAND and NOR gates
  2-, 3-input AND and OR gates
- 10 complex 4-input logic functions, e.g.,
  $(A1 \times A2) + B1 \times B2)$
  $(A1 \times B1) + C1 \times C2)$
- 4 master and 4 slave flip-flops including set and reset options
- 14 functions using transmission gates including:
  Exclusive NOR/OR
  Strobed D-latches with set and reset options
  Master-slave flip-flops with set and reset options

GATE ARRAY SCC700

Preliminary

PERIPHERY

To provide a versatile interface, the SCC700 has 38 input/output pads. These peripheral elements can be configured to match the input or output requirements of a wide variety of logic families and accordingly a bonding pad may have assigned to it one of the following functions:

- Input stage which includes an input protection circuit (series resistor and single diode clamp to V_{SS}). The recommended maximum load is 20 array gates, or 10 array gates for optimum speed performance. Because the input voltage is not clamped to V_{DD} input voltages, greater than the supply voltage is possible thus allowing voltage level shifting.
- Schmitt trigger input stage (ten available) for noise rejection, pulse shaping, or suppression of spurious oscillations associated with slow input clock transitions. The recommended maximum load is ten array gates, or five for optimum speed performance.
- Complementary output with driver or buffer performance capability.
- Three-state output with driver or buffer performance capability for bussing applications.
- Transceiver input/output stage.
- Open drain N- or P-transistor output.

In addition a pull up/down resistor (34 available) may be added at various I/O stages. The values available are 5, 10, 15, 60, 65, 70 and 75 Kohms.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Operating ambient temperature	−40 to +85	°C
Storage temperature	−65 to +150	°C
Supply voltage	−0.5 to +18	V

DC ELECTRICAL CHARACTERISTICS $V_{SS} = 0V$

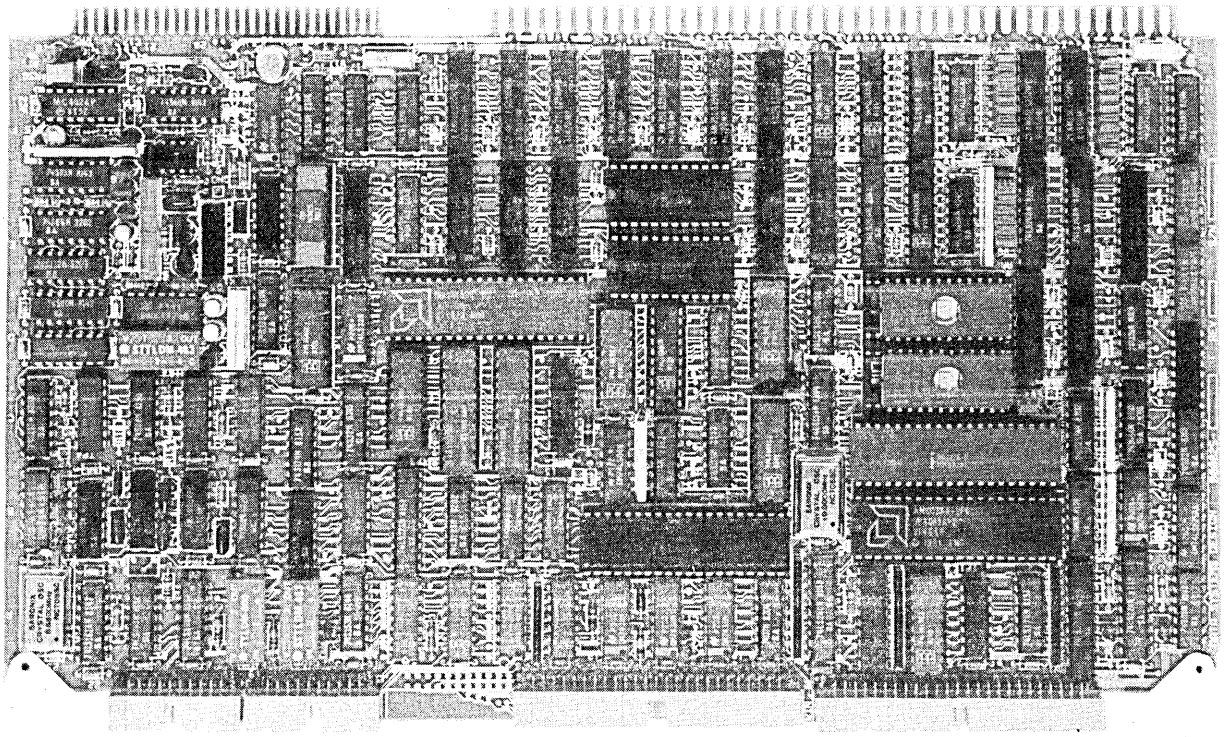
PARAMETER	TEST CONDITIONS	TENTATIVE LIMITS			UNIT
		Min	Typ	Max	
Input leakage Standby current	$V_{DD} = 15V$ $V_{DD} = 5V$, T = 25°C $V_{DD} = 10V$, T = 25°C $V_{DD} = 15V$, T = 25°C		0.3 50 100 200		µA µA µA µA
Output sink current Low — buffer	$V_{OL} = 0.4V$, $V_{DD} = 5V$ $V_{OL} = 0.5V$, $V_{DD} = 10V$ $V_{OL} = 1.5V$, $V_{DD} = 15V$		1.6 4.0 12.0		mA mA mA
Output sink current Low — driver	$V_{OL} = 0.4V$, $V_{DD} = 5V$ $V_{OL} = 0.5V$, $V_{DD} = 10V$ $V_{OL} = 1.5V$, $V_{DD} = 15V$		0.8 2.0 6.0		mA mA mA
Output source current High — buffer or driver	$\|V_{OH}\| = 0.4V$, $V_{DD} = 5V$ $\|V_{OH}\| = 0.5V$, $V_{DD} = 10V$ $\|V_{OH}\| = 0.5V$, $V_{DD} = 15V$		0.6 1.5 5.0		mA mA mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $C_{LOAD} = 50pF$, $V_{SS} = 0V$

PARAMETER	TEST CONDITIONS	TENTATIVE LIMITS			UNIT
		Min	Typ	Max	
Propagation delay 2 input NAND — FO = 2	5 volts 10 volts 15 volts		20 10 7		ns ns ns
Maximum toggle frequency FO = 1	5 volts 10 volts 15 volts		3 6 9		MHz MHz MHz
Output transition time High to low driver	5 volts 10 volts 15 volts		60 30 20		ns ns ns
Output transition time High to low buffer	5 volts 10 volts 15 volts		30 15 10		ns ns ns
Output transition time Low to high buffer or driver	5 volts 10 volts 15 volts		40 18 12		ns ns ns

NOTE:
Above electricals reflect performance characteristics of medium speed (G) wafer process.

For Key Data On Every IC On This Board, The Place To Look Is...



The Data System Design 7215 is a single-board controller with pipelined architecture that can simultaneously control Winchester, streaming tape, and floppy drives.

Device No.	Description
AM25LS2569	Up-Down Binary Counter with Synchronous Preset
AM2910	Dual Retriggerable Monostable Multivibrator
AM26S02	Programmable Schottky Read-Only Memory
AM27S35	12-Bit Microprogram Controller
AM8085	Complete 8-Bit Parallel Central Processing Unit
CA3130	5-to-16-Volt Single Stash Supply Op Amp
2732	4096 x 8 TTL PROM
8237	DMA Controller
DM7438	Quad 2-Input TTL NAND Buffer
DM8334	8-Bit Addressable TTL Latch
DS75107	Differential Line Receiver
F74S132	Quad 2-Input NAND Schmitt-Trigger
MC4024	Dual Voltage-Controlled TTL Multivibrator
MK4802	2048 x 8 Static NMOS RAM
PAL16L8	Field Programmable Logic Array
PAL16R6	Field Programmable Logic Array
PAL16R8	Field Programmable Logic Array
7407	Hex Buffer/Driver
74123	Dual Retriggerable Monostable Multivibrator
74368	Hex Inverter, 3-State
74LS02	Quad 2-Input TTL NOR Gate
74LS04	Hex Inverter
74LS125	Quad Gated TTL Buffer, 3-State
74LS138	3 Line to 8 Line Decoder/Demultiplexer
74LS151	8-Input Multiplexer
74LS161	Binary Counter
74LS166	8-Bit Parallel-In, Serial-Out Shift Register with Clear

Device No.	Description
74LS174	Hex D-Type Edge-Triggered Flip-Flop with Clear
74LS240	Octal Bus Driver (Schmitt Trigger)
74LS244	Octal Bus Driver (Schmitt Trigger), Non-Inverting
74LS257	Quad 2-Input Multiplexer, Non-Inverting
74LS273	Octal D-Type Edge-Triggered Flip-Flop, 3-State
74LS299	8-Bit Universal Shift Register
74LS365	Hex Buffer, 3-State
74LS373	8-Bit Latch
74LS374	Octal D-Type Edge-Triggered Flip-Flop, 3-State
74LS393	Dual 4-Bit Binary Counter
74LS533	D-Type 8-Bit Latch
74LS670	16-Bit (4x4) Register File with Simultaneous Read/Write
74S00	Quad 2-Input NAND Gate
74S03	Quad 2-Input NAND Gate, Open Collector
74S04	Hex Inverter
74S112	Dual "J-K" Negative Edge-Triggered Flip-Flop
74S151	8-Input Multiplexer
74S153	Dual 4-Input Multiplexer
74S174	Hex D-Type Edge-Triggered Flip-Flop with Clear
74S175	Quad D-Type Edge-Triggered Flip-Flop with Clear
74S240	Line Driver, Single Ended, 3-State, Inverting
74S32	Quad 2-Input OR Gate
74S51	Dual 2-Wide 2-Input AND-OR-Invert Gate
74S64	4-2-3-2-Input AND-OR-Invert Gate
74S74	Dual D-Type Positive Edge-Triggered Flip-Flop
75110	Line Driver, Differential, Twisted Pair Level Shifting

Representative list of ICs on the Data Systems Design 7215 board.
Key specifications for all of these ICs can be found in IC MASTER.

IC MASTER

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BIPOLAR PROCESS CHART

Process Designation	h_{FE}	BV_{CEO} volts	BV_{CBO} volts	Base		epi		n+BL		Min. geometry (microns)	M1 Pitch (microns)	M2 Pitch (microns)	Options/ Comments
				ρ_s	x_j	ρ_t	t	ρ_s	x_j				
B A	60	45	70	135	2.5	5	17	23	5.5	6	20	—	Single Metal High Voltage
B B	60	16	40	135	2.5	1	10	23	5.5	6	20	—	Single Metal Medium Voltage
B C	60	10	25	200	1.2	0.75	3.4	23	5.5	5	14	24	Double Metal Al Schottky
B D	50	6	18	200	1.2	0.3	3.4	23	5.5	5	14	24	Low Voltage Double Metal
B F	60	6	18	200	1.2	0.3	2.5	13	5.8	4	12	24	Double Metal Barier Schottky Washed Emitter

SSi offers it all—custom,

Three levels of service.
SSi offers three levels of service: (1) custom IC design, development, and production; (2) COT services that start with the customer's own design and tooling and provide him with volume production of packaged units; and (3) foundry services that start with the customer's own tooling and provide him with wafer fabrication only. The above charts show the processes available from SSi.

For more information on SSi's total capability, send for a copy of the new brochure entitled "SSi Today."

SSi procedures for foundry service customers.
For any customer, the first step is definition of his product. The next step is selection of the appropriate process and development of the tooling. SSi COT customers can choose either bipolar or CMOS technologies. For customer designers who need help, SSi will provide layout rules, test requirements, and design assistance. But the COT customer who already has his own design tooling can start farther ahead.

If you already have a compatible tape, we can perform a design rule check to make sure that there are no layout violations and start from there. If you have a Calma tape we can go right to mask-making. If you have acceptable working plates, we can go immediately into fabrication of prototype wafers.

After prototype wafers are fabricated, we perform prototype wafer probe, assembly, and final testing in-house. We can test your circuits using your existing test programs, or we can help you create a test program from your specifications. After device testing, we deliver prototype units to you for evaluation in your system or application.

You approve the prototypes, and in most cases we go right to production. We can produce characterization lots for your evaluation under worst case operating conditions. If you require complete COT

CMOS PROCESS CHART

Process Designation	Channel	V_{TFO} (volts)	V_{TO} (volts)	BV_{DSS} (volts)	K′	N or P (Ω/□)	Poly (Ω/□)	Channel Length (microns)	Poly Pitch (microns)	M1 Pitch (microns)	M2 Pitch (microns)	Options/ Comments
CB01	P	-20	-0.9	-20	11.0	80	—	9	—	12.5	—	High Voltage Al Gate
	N	20	9	20	17.0	16	—	7.2	—	12.5	—	
CB02	P	-10	-0.9	-20	11.0	70	—	7.2	—	12.5	—	Low Voltage Al Gate
	N	10	0.9	20	17.0	12	—	7.2	—	12.5	—	
CC01*	P	-15	-0.9	-13	14.0	100	20	3	7	9	12	Double Metal Single Poly (includes cap) Si Gate
	N	15	0.7	13	28.0	25	20	3	7	9	12	

*In development.

COT services, or foundry.

services, the final step is off-shore assembly at one of our highly qualified locations for the volume production of your packaged product. We can also perform hi-rel screening and burn-in, if desired.

SSi uses standard multi-sourced wafer processes.
SSi offers circuits in junction-isolated bipolar single and double-layer metal. CMOS metal-gate and silicon-gate are also available. These are the most popular and reliable processes in the two basic technologies. Although these standard processes are available from multiple sources, SSi's advanced ultra-clean wafer fab produces higher yields than ordinary facilities.

SSi offers 11 variations of the above core processes. These variations permit you to select the optimum process when fabricating a new circuit or when matching a process already being used for an existing circuit.

The charts above provide guideline parameters for both the bipolar and CMOS processes available from SSi. For more detailed information on electrical and topological design rules and available processes, consult our engineers. They can determine which process variation is best for your particular circuit.

Silicon Systems incorporated,
14351 Myford Road, Tustin, CA 92680,
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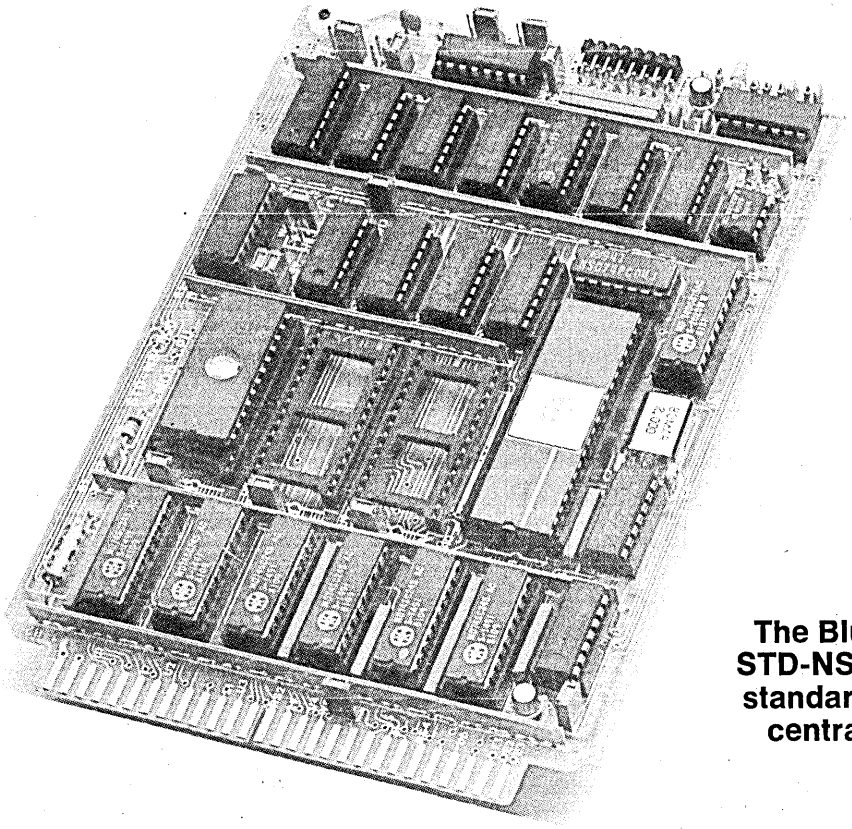
CUSTOM/SEMICUSTOM

For Key Data On Every IC On This Board, The Place To Look Is...



The Blue Chip Computer STD-NSC800 is a CMOS standard bus compatible central processor card.

Equipment and system design often require the use of a wide variety of integrated circuits in order to obtain optimum performance. One way for an engineer to be certain that he hasn't overlooked the best device for his application is to refer to the pages of IC MASTER.

Surveys conducted by IC MASTER, integrated circuit manufacturers, and independent research agencies confirm that four out of five IC MASTER users have specified one or more products as the result of using IC MASTER.

Device No.	Description
NMC27C16	Erasable CMOS PROM
NSC800	8-bit Microprocessor
74SC245	3-State Octal Bus Driver
MD74SC373	Noninverted D-Type Transparent Latch
ICL8212C	Micropower Voltage Detector
MM74PC00	Quad 2-Input NAND Gate
MM74PC32	Quad 2-Input OR Gate
MM74PC08	Quad 2-Input AND Gate
MD74SC139	Octal Decoder/Demultiplexer
MM74PC74	Dual Type-D Flip-Flop
MSC74PC07	Hex Inverter
MM74C30	8-Input NAND Gate

Representative list of ICs on the Blue Chip Computer STD-NSC800 card. Key specifications for all of these ICs can be found in IC MASTER.

IC MASTER

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Why Go Custom and Why Use Synertek?

Synertek.

Your decision to use a Custom circuit rests basically on the requirements of your system. You'll want to consider the alternatives available to you:

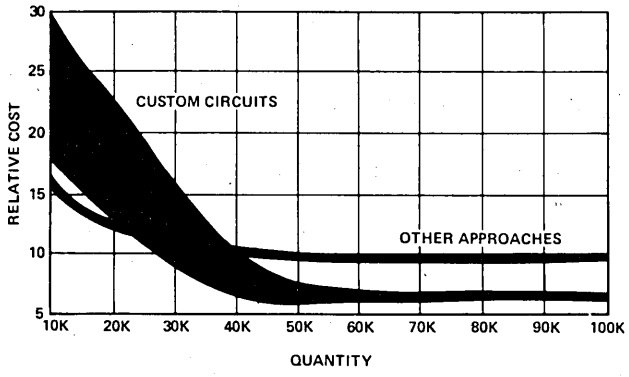
- **Standard circuits** are off-the-shelf products designed for general product applications. If your yearly system volume will be less than 10,000, SSI (small scale integration) and MSI (medium scale integration) circuits may be your best solution.
- **Microprocessors** may fill your need if your application requires great flexibility and cost is not an overriding factor. They are most practical when total circuit volume does not exceed 50,000.

Advantages of Custom Circuits

A Custom circuit is an exclusive proprietary design built specifically to meet your product requirements. Its advantages are:

- **Reduced system cost** — Through circuit integration the total number of discrete and integrated components can be cut by 75-90%. This dramatically reduces component inventory, PC board assembly, and power supply costs.
- **Increased reliability** — As circuit device count and total system size is reduced, system reliability increases. For you, the more reliable a system you sell to your customers, the less you will have to expend on warranty costs.
- **Features** — Special features not available in standard circuits or microprocessors can be cost-effectively designed into a Custom circuit.
- **Market leadership** — CUSTOM MOS/LSI technology can revolutionize a product. It enables new features to be built which would otherwise be unavailable or too expensive to implement. When your product is manufactured with a proprietary design, competitors have a more difficult time copying it. As a result, you can enjoy longer periods of market leadership and penetration.

Custom Costs vs. Other Alternatives



Why Use Synertek?

You don't want just anyone to develop your Custom design. You want a company with experience, skill and an understanding of how important your design is to you. As a major supplier of Custom circuits, we fulfill those requirements and offer competitive design and process solutions.

Our ability to develop sophisticated technologies insures our market leadership position in custom integrated circuits. We currently offer silicon gate HMOS, NMOS, and HCMOS technologies. Our advanced computer-aided design facilities, projection alignment equipement, 4-inch wafer fabrication lines, and VLSI testing equipment further demonstrate Synertek's commitment to state-of-the-art technology. Your choice depends on your need.

- **Classic Custom circuit design** — We will design your circuit from concept. You may initially provide us with a written explanation of the function you want, or with a logic diagram of the circuit, or with just a specification. We will create your work-of-art from beginning to full production.
- **Customer Design Teams (C.D.T.)** — We will train your engineers to do their own custom design. The full spectrum of design capability can be approached: classic custom hand-drawn circuits, designs using The Cell Library™, or seminars for C.O.T.™ customers. Your systems knowledge is combined with our IC design capability for optimum circuits.
- **C.O.T.™** — Synertek will become the manufacturing arm of your in-house design group or your consulting design house. By providing you with process design rules, parameters, computer simulation programs and, most of all, our total cooperation, we can assure you the manufacturing capability you want.
- **Standard Products** — The Logic Products Group has developed, with the cooperation of some of our customers, circuits which fulfill the needs of the marketplace. We continue to search for unique designs which expand our ability to serve our customers requirements.

We advocate a firm policy of partnership in all three of these circuit production services. Your success is directly related to ours, and a close working relationship promotes understanding and efficiency between us. It also insures that the Custom circuit is produced exactly to your specifications. This spirit of cooperation and teamwork will heighten your feeling of ownership for your proprietary Custom circuit.

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Evolution of a Masterpiece

A masterpiece is never developed overnight. An artist needs time to think, plan, and create. At Synertek, the average length of time needed to bring a circuit from the concept stage to prototype production is 6-9 months. Depending on the complexity of the device, this may be longer or shorter. Simple circuits can be completed within 3-4 months. All circuits, however are subjected to the same stringent testing, quality control, and verifications checks.

Keeping with our philosophy of partnership, our engineers will confer with you often throughout the design and development phases.

The Custom Design and Development Process

- **System definition** — Synertek and the customer establish block diagrams, flow charts, and mechanical and electrical specifications. A program milestone schedule is confirmed.
- **Logic design and computer simulation** — Our design engineers convert system functions to MOS logic. Computer simulations of critical logic deisgn characteristics are done in our DA (design automation) center. SCEPT™ (Synertek Circuit Emulation Program and Test) is a conventionally designed breadboard which duplicates MOS logic. We consider SCEPT™ an indispensible tool for verifying the functionality of the design. It also gives you your first opportunity for hands-on verification of the actual logic functions. Once approved by you, SCEPT™ is used to write and debug a test program. From this point, SCEPT™ is the functional reference for the remaining design steps.

  1-10 wks.
- **Circuit design and analysis** — Individual transistors are laid out to implement the SCEPT™ logic. Particular attention is paid to critical speed paths. Additional computer-aided circuit simulation information is analyzed and incorporated into the actual circuit design.

  1-4 wks.
- **Composite layout design** — A layout of the circuit design, called a composite, is hand drawn to minimize final chip size. Composites are drawn at 500 to 2000 times the size of the finished chip.
- **Digitizing** — The composite drawing is converted in our CAD (Computer Aided Design) center to a database tape using a Calma interactive graphic system. This digitized information is used to generate plots of each circuit layer. The plots are compared to the original composite and editing changes are made. Editing and checking continues until the database tape is approved for the entire composite. Design rule checks (DRCs) and electrical rule checks (ERCs) are accomplished by our CAD system using the database tape.

  4-14 wks.
- **Mask generation** — Once the database tape is approved, a PC (pattern generation) tape is produced. This tape is used to create each mask level.

  We use three methods in mask making — photolithography, E-beam and a combination of both.

  In the photolithographic process the 10X reticles are created on a pattern generator. These reticles are photo reduced to the actual 1X mask size and reproduced by a step-and-repeat camera.

  With E-beam technology, the PG tape is converted to E-beam format. The full array is then written directly at the 1X mask size.

  In the combination method, 10X reticles are generated from the E-beam-formatted tape. As in the photolithographic process, these reticles are then photo reduced to the actual 1X mask size and reproduced by a step-and-repeat camera.
  Which method should be used is determined by device complexity, die size, and the process chosen for wafer fabrication.

  4-9 wks.
- **Prototype wafer fabrication** — During prototype fabrication, numerous quality and electrical inspections are performed to assure that every wafer lot meets our specifications.
- **First samples** — Thses are untested devices commonly referred to as "Cut & Go's." They are placed in ceramic packages, assembled, and sent to your for initial evaluation.

  2-3 wks.
- **Test generation** — The Cut & Go's play an essential role in the completion of the test program, which was initiated during the circuit design stage. The test program must be verified with the Cut & Go's before it is finalized.
- **Prototype production** — After fully tested samples are approved, prototype production begins.
- **Full production** — Scheduled delivery commences after prototype qualification and test verification are completed.

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Customer Design Teams (C.D.T.)

C.D.T. is a program by which customers can be trained to do their own IC designs. It encompases the full spectrum of custom design from the classical, hand-drawn approach, with Synertek's engineers doing the full design, to the customer owned tooling program. CDT's are designed to take advantage of the customer's system knowledge and Synertek's IC design and production capabilities. The customer has access to our facilities, design courses, The Cell Library™, advanced CAD tools, processes, design expertise, and on-going support.

The design course is approximately ten weeks long and is based upon the structured design methodology. The major portion of the course demonstrates how to use The Cell Library™, with hands-on experience using our CAD tools to complete a simple design. Very little time is spent on design physics. References will be furnished to those interested in further studies. As an on-going project we are continually developing additional short courses as updates as well as video tapes on specific topics.

Our CAD tools revolve around our mainframe computer, a VAX 11/780 to enable our customers to use commercially available software written for the VAX. NCA corporation's software is used for layout verification, including Design Rule Check, Electrical Rule Check and Network Continuity Check. The Network Continuity Check compares the layout data to the Netlist derived from schematic entry. Other services, such as sizing and PG tape generation can also be performed on the VAX.

Silvar-Lisco's SOS package including CASS and CAL-MP is installed on the VAX. CASS is used for schematic entry via a Genisco 1000 terminal. Once the schematic has been entered, a design database is created from which several output data formats can be generated. The following outputs are presently available: Netlist, TEGAS for logic generation and test verification, SPICE for circuit simulation, Network Continuity Checker and CAL-MP.

CAL-MP is used for automatic placement and routing of the cells in The Cell Library™. All cells are designed to take advantage of the CAL-MP program capability. The program can handle up to 1800 cells (not gates) with 3600 cell capability to be installed soon. Chips of larger size can be created by assemblying partitioned sections of up to 3600 cells each.

We are constantly updating and improving our software. Any improvements in the NCA or Silvar-Lisco software will be installed so that design capability and turn-around times can constantly be improved. Dial-up facilities to the VAX will be available beginning Q1, 83 enabling our CDT customers to access the above software via remote terminals.

As an important part of the CDT program Synertek provides support in the form of helping with the design, instruction in the use of our CAD equipment, providing updates in the course, and providing advancements in our process capabilities. Synertek's CDT team is organized to assist the customer in all the crucial steps of the design. Once the customer reaches design proficiency, we have a separate Customer Owned Tooling (C.O.T.™) team to move designs quickly into production. As a customer's needs or designs change, CDT's are flexible enough to tailor on-going support to the specific requirements of the customer.

C.O.T.™

Synertek.

Perhaps you have your own MOS design group, or have chosen to have your circuit designed by a consulting firm. Or maybe another MOS supplier designed the chip and you want to tool-up a second-source supplier. Whatever your design source, we can produce your circuit on a customer owned tooling (C.O.T.™) basis.

Because of our extensive experience with MOS/LSI technology, we understand your reasons for going C.O.T.™. You want to minimize design cost and production time while maximizing proprietary design control. We guarantee that your Custom circuit will receive the same confidential, proprietary treatment as our own in-house designed circuits.

You may enter the production cycle at a number of various stages. We'll accept your design on a database tape, a pattern generator tape, or working plate. You'll be given an initial documentation package that includes an overview of design rules and parameters for our MOS processes.

C.O.T.™ customers provide Synertek's Product Engineering with their chosen form of tooling along with the test tape and specifications for testing the customer's circuit.

Synertek maintains a policy of requiring characterization data for all circuits prior to transfer to production. This measure enables Synertek to do further studies on yield enhancements and correlation. Synertek strives to maximize yields at final test and ultimately reduce circuit costs to the customer. We view C.O.T.™ as a joint effort on the part of vendor and customer. Our goal is to work with the customers design group, to lend the necessary technical support and to build a successful working relationship.

Again, we will meet with you as early in the program as possible to establish a close working relationship. If you wish to design your own proprietary circuit, our engineering staff is available for design workshops and general program guidance, on a consulting basis. We take measures to enhance a smooth product flow. Our program managers monitor your circuit from our CAD center through production. We also have a back-log control system that continually updates you on product schedules and shipments.

As a C.O.T.™ customer, you have access to our extensive manufacturing and assembly facilities in addition to our advanced processes.

MOS Processes

SILICON GATE CMOS

Process	FLDI²	ENHI²	DEPI²	V_{SB}	V_{TEO}	Volts V_{TDO}	V_{TFO}	V_{VDSS}	Beta A/V²	Gamma V 1/2	
NSJ2	Yes	Yes	Yes	0	+0.7	-4.0	10	10	12	0.95	
NPJ4	Yes	No	Yes	-2.5	0.45	-3.3	15	20	12	0.65	
NDK4	Yes	Yes	Yes	0	+0.2	-3.0	16	10	11	0.25	
NPK4	Yes	Yes	Yes	0	0.45	-3.3	15	20	12	0.65	
NTK4/NSK4	Yes	Yes	Yes	-3.0	+0.8 VTI	-3.5 +0.3V	15	10	15	0.30	
NPM5	Yes	Yes	Yes	0	+0.5 -0.2	-3.0 -1.3	15	7	19	0.26	
NDM5	Yes	Yes	Yes	0	+0.5 -0.2	-2.7	15	7(2.5μ)	17	0.35	
NPM6	Yes	Yes	Yes	0	+0.5 -0.0	-3.0 -1.3	15	7(1.6μ)	29	0.25	
NFN5	Yes	Yes	Yes	0	+0.8	-2.8	27	11	17	0.75	

SILICON GATE NMOS

Process	Channel	V_{TFO}	V_{TO}	Beta UA/V²	B_{VDSS}	Gamma	pNopP Ω/□	pPoly Ω/□	Channel Length μ	
CPN5	P	-16	-0.9	5.5	-19	0.7	50	20	3μ	
	N	+10	+0.9	17	+17	0.5	25	15	3μ	
CA62	P	-16	-0.9	5.5	-19	0.7	50	1) 20 15	3μ	
	N	+10	+0.9	17	+17	0.0	25	2) <100 <100	3μ	

A Process for Every Masterpiece

Selecting the right process for your Custom circuit is one of your most important decisions in the design cycle.

Synertek's offering of fully proven manufacturing processes has the right answer for you. It includes state-of-the-art HMOS, HCMOS and EEPROM in addition to the industry standard NMOS silicon gate technology.

The chart on these pages contains conservative data on Process Characteristics and Topology. This data is provided only as a guideline to help you determine the general "fit" to new circuits and those already in production. Detailed Electrical and Topolgical Design Rules are available under a non-disclosure agreement.

Again, we encourage potential C.O.T.™ customers to notify us at the early stages of the program so that we can provide the necessary guidance to your designers to ensure process compatibility with circuit performance. You may find the process requirements for your circuit differ from what is shown on our chart. If so, be assured that our process engineers will work with you to determine any needed variations for your circuit.

C_{DA} $F/cm^2 \times 10^{-8}$	pN Ω/□	pP Ω/□	X_j	Channel Length μ	Topological Pitch: Poly w/s μ	Topological Pitch: Diff w/s μ	Topological Pitch: Al-Al w/s μ	Comments
1.5	20	45	1.1	6	6/7	6/7	7/7	Shrinkable by 16% for low voltage Applications
1.6	15	45	1.2	6	6/6	6/6	7/7	Planox; shrinkable by 16%
0.7	15	60	1.5	6	6/6	6/6	6/6	Planox, 2 poly process, switched capacitor techniques for analog circuits
1.6	15	45	1.2	6	6/6	6/6	7/7	Planox; shrinkable by 16%
1.5	12	45	1.1	5	5/5	5/5	5/5	Process has an intrinsic transistor mask option. High speed applications.
0.7	27	30	0.45	3 (E & D) 4 (I)	4/5	5/5	5/5	HMOSI. Dual implants for each ENH and DEP transistor (optional)*.
0.8	24	27	0.35	3	3/3	5/4	5/5	Planox; 2 poly HMOS.
0.8	24	27	0.35	2 (O) 3.5 (I)	3/3	3.5/3.5	3.5/3	Planox; single poly. Stepper technology and all dry etch process.
0.7	15	65	1.2	5	5/4	5/5	5/5	Planox; E^2PROM process

*Also available with dry etch processing at metal.

Topological Pitch: Poly w/s	Topological Pitch: N-Well w/s	Topological Pitch: Diff. w/s	Topological Pitch: Al-Al w/s	Comments
3/3.5	3.5/14	3/5	4/5	Single poly, n-well process.
3/3.5		3/5	4/5	Available up to 12V. (Channel lengths = 5μ).
3/3.5	3.5/14	3/5	4/5	Double poly, high voltage.
3/3.5		3/5	4/5	

Synertek.

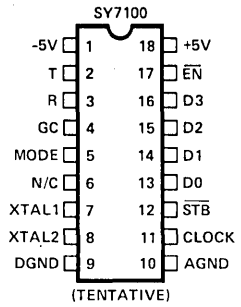
SY7100

DTMF Receiver

Features

- No External Filters Required
- TTL-Compatible Three-State Outputs
- Uses Low Cost 3.579545 MHz Crystal
- Fully Immune to Normal Noise Conditions
- Excellent Speech Immunity
- 18-Pin Package for Low Cost
- +5V and -5V Power Supplies

Pin Configuration

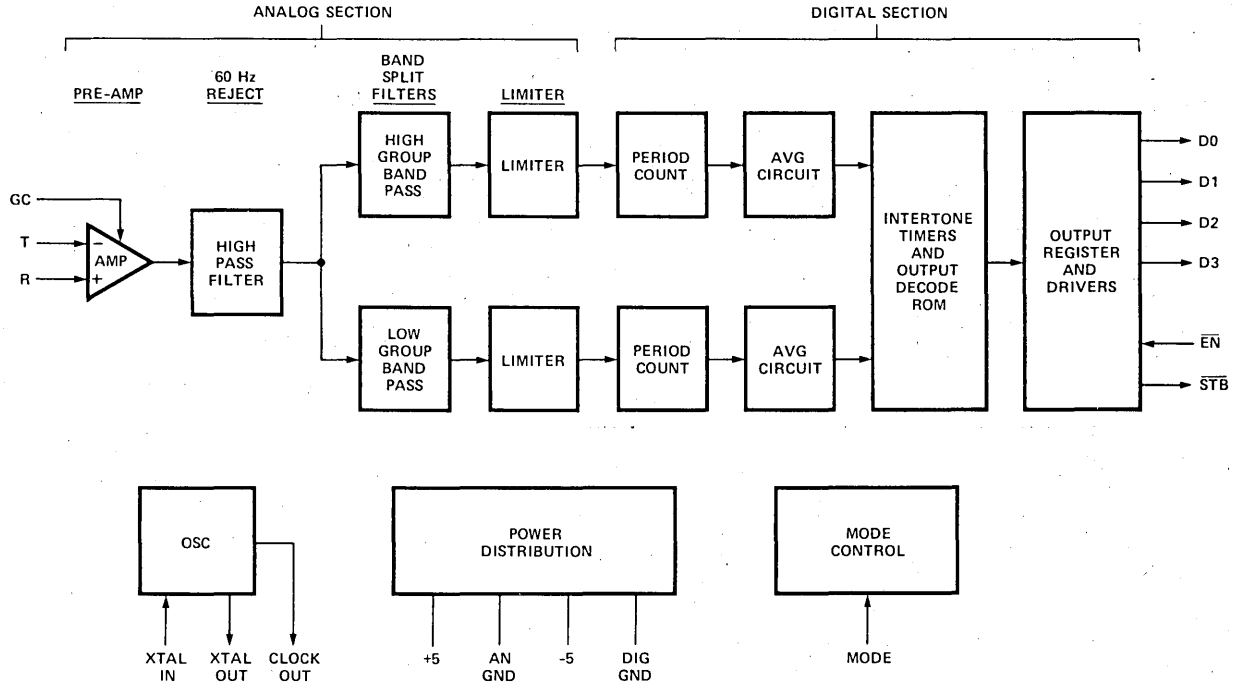


(TENTATIVE)

Description

The SY7100 is a fully monolithic Dual-Tone Multi-Frequency (DTMF) Receiver intended for use in a wide variety of telephone applications. Standard Bell System tone frequencies are automatically decoded into a 4-bit binary coded output. No external band-separation filters are required and, in fact, only a small number of external components are needed. The device is fabricated using NMOS switched capacitor technology to optimize cost and performance.

Block Diagram



Synertek

CUSTOM/SEMICUSTOM

Synertek.

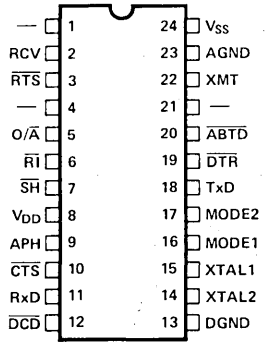
SY7110/SY7111

300 BPS FSK Modem

Features

- Bell System 103 or CCITT v.21 types
- Phase Coherent FSK Modulation
- No External Filters Needed
- Minimal External Components Required
- Uses Low-Cost TV Color Burst Crystal (3.579545 MHz)
- Low Distortion Signal Generation (5%)
- Highly Sensitive Receiver (-50 dBm)
- Automatic Answer and Disconnect
- Fully Automatic Handshake Operation
- RS-232C Interface Signals
- Local and Remote Loop-Back Test Capabilities
- 0-70° C Operating Range

Pin Configuration



(TENTATIVE)

Description

The SY7110 and SY7111 are modem devices intended to provide for data communications over the switched telephone network or via dedicated private lines. Complete analog and digital functions are incorporated on a single monolithic substrate by the use of switched-capacitor NMOS technology. The SY7110 provides for 300 BPS data rates compatible with Bell System model 103 modems, whereas the SY7111 is compatible with the CCITT recommendation v.21.

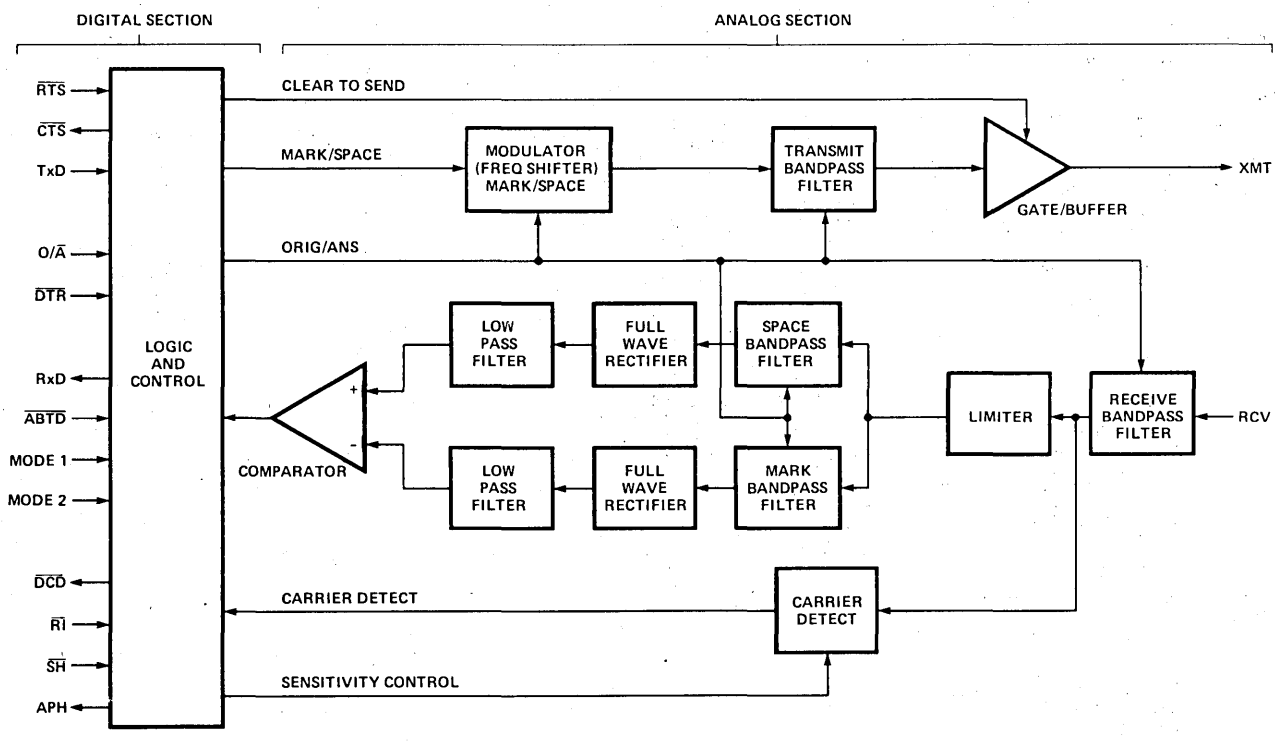


FIGURE 1. BLOCK DIAGRAM

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CUSTOM/SEMICUSTOM

ABBREVIATIONS OF COMPANY NAMES

Action Ins	Action Instruments
AD	Analog Devices
ADT	Advanced Digital Technology
Adapt Sci	Adaptive Science Corp.
Advent	Advent Products, Inc.
Alphatron	Alphatron
AMA	American Automation
AMD	Advanced Micro Devices
AMI	American Microsystems, Inc.
Amperex	Amperex Electronic Corp.
Analogic	Analogic
Analog Sys	Analog Systems
APC	Applied Micro Circuits
Apex	Apex Microtechnology
APM	Applied Microsystems Corp.
Appl Sys	Applied Systems Corp.
APT	Applied Microtechnology
Aptek	Aptek Microsystems
Array Tech	Array Technology
AWI	Analog West
Bedford	Bedford Computer Systems Inc.
Burr-Brown	Burr-Brown Research
CAE	Computer Aided Engineering
Cal Devices	California Devices
Cent Data	Central Data Corp.
Cermetek	Cermetek
CGRS	CGRS Microtech Inc.
Cherry	Cherry Semiconductor
CIC	Custom Integrated Circuits
Citel	Citel, Inc.
Comlinear	Comlinear Corporation
CMA	Custom MOS Arrays
Comark	Comark Corp.
Comdial	Comdial Semiconductor
Comp Auto	Computer Automation
Compas	Compas Microsystems
Cont Logic	Control Logic Inc.
Control Sys	Control Systems Microsystems Div.
CreMicro	Creative Micro Systems
Cromemco	Cromemco, Inc.
CSG	Commodore Semiconductor Group
Cubit	Cubit Inc.
Curtis	Curtis Electro Devices, Inc.
Cybernetic	Cybernetic Micro Systems
Cybersys	Cybersystems
Cybertek	Cybertek Inc.
Data General	Data General
Data I/O	Data I/O
Data Trans	Data Translation
Datel	Datel-Intersil
Datricon	Datricon Corporation
DDC	Data Devices Corporation
DEC	Digital Equipment Corporation
Delco	Delco Electronics
DGM	Digital Microsystems
Digelec	Digelec Corp.
Digitek	Digitek, Inc.
Dionics	Dionics Inc.
Dist Comp	Distributed Computer Systems
Divers Tech	Diversified Technology
E-HI	E-H International, Inc.
Elind	Elind Elettronica Industriale
EL Instr	E & L Instruments
EMM	EMM
Emulogic	Emulogic Inc.
Epson	Epson America, Inc.
ETI Micro	ETI Micro
Exar	Exar Integrated Systems
Fairchild	Fairchild
Ferranti	Ferranti Electric
Fujitsu A	Fujitsu America
Fujitsu	Fujitsu Microelectronics, Inc.
GI	General Instrument
GMS	General Microsystems
GTE Micro	GTE Microcircuits
Harris	Harris Semiconductor
Heurikon	Heurikon Corp.
Hilevel	Hilevel Technology, Inc.
Hitachi	Hitachi America, Ltd.
Holt	Holt Inc.
HP	Hewlett-Packard
Hughes	Hughes Aircraft, Solid State Products
Hybrid Sys	Hybrid Systems
Hycom	Hycom Incorporated
IDT	Integrated Device Technology
IMI	International Microcircuits, Inc.
IMP	International Microelectronic Products
IMS	Industrial Micro-systems Inc.
Inconix	Inconix Corporation
Ind Tech	Inductive Technology
Inmos	Inmos
IntCirEng	Integrated Circuit Engineering
IntCirSys	Integrated Circuit Systems
IntCompSys	Integrated Computer Systems
IntCyber	International Cybernetics
Int Micro	International Microsystems
Int Tech	Integrated Technology Corp.
Intech/FMI	Intech/Function Modules Inc.
Intel	Intel
Interdesign	Interdesign
Intersil	Intersil
Intronics	Intronics
IPI	Integrated Photomatrix Inc.
ITT	ITT Semiconductors
Kinetic Sys	Kinetic Systems
Kontron	Kontron Electronics
Lambda	Lambda Semiconductor
Laserdyne	Laserdyne
LSI Comp	LSI Computer Systems
LSI Logic	LSI Logic Corporation
Master Logic	Master Logic Corporation
Matrix	Matrix Corp.
Matrox	Matrox Electronic Systems
MCC	Microcomputer Control
Micrel	Micrel
Micro Eng	Micro Circuit Engineering
Micro Innov	Micro Innovators
Micropac	Micropac Industries
Micro Net	Micro Networks
Micro Pwr	Micro Power Systems
Micro Sci	Micro Sciences Corp.
Micro Tech	Microcircuits Technology
Micro-Link	Micro-Link Corporation
Micron	Micron Technology
MilerTron	MilerTronics
Miller	Miller Technology
Mitel	Mitel Semiconductor
Mitsubishi	Mitsubishi Electronics
MMI	Monolithic Memories, Inc.
Monosil	Monosil
MonSys	Monolithic Systems Corp.
Mostek	Mostek
Motorola	Motorola Semiconductor
MRC	MRC Systems
Murray	Murray Consulting
National	National Semiconductor
NCR	NCR Corp., Microelectronics Division
NEC-EA	NEC/Electronic Arrays Division
NEC Electron	NEC/Electron Division
NEC Micro	NEC/Microcomputer Division
Nitron	Nitron
Nortek	Nortek
OAE	Oliver Advanced Engineering
Octagon	Octagon Systems Corp.
OEI	Optical Electronics Inc.
Ohio Sci	Ohio Scientific
OKI	OKI Semiconductor
Omnibyte	Omnibyte Corp.
Oscar	I. S. Oscar Assoc.
Panasonic	Panasonic
PC/M	Pacific/Cyber Metrix
Percom	Percom Data Co.
Phoenix	Phoenix Digital Corp.
Pico Design	Pico Design
Polycore	Polycore Electronics
Plessey	Plessy Semiconductors
PMI	Precision Monolithics, Inc.
PragDes	Pragmatic Design Inc.
PREMA	PREMA GmbH
Pro-Log	Pro-Log Corp.
Quay	Quay Corp.
Raytheon	Raytheon Semiconductor
RCA	RCA Solid State Division
RCI Data	RCI Data
RELMS	Relational Memory Systems
Reticon	Reticon
RIFA	RFIA
Rockwell	Rockwell, Microelectronic Devices
RTC	Riehl Time Corporation
Sanken	Sanken Electric
Sanyo	Sanyo
SEEQ	SEEQ Technology, Inc.
Semi Proc	Semi Processes
Siemens	Siemens
Signetics	Signetics
SGS	SGS-ATES Semiconductor
Sharp	Sharp
Silicon G	Silicon General
Siliconix	Siliconix
Silicon Sys	Silicon Systems Inc.
Siltronics	Siltronics
SMC	Standard Microsystems Corp.
Solarise	Solarise Enterprises
Solitron	Solitron Devices
Sprague	Sprague Electric Company
SSM	Solid State Micro Technology for Music
SSS	Solid State Scientific
Stag	Stag Microsystems
Struc. Des.	Structured Design Inc.
Stynetic	Stynetic Systems
Sunrise	Sunrise Electronics
Sunshine	Sunshine Semiconductor
Supertex	Supertex Inc.
Symtek	Symtek Corp.
Synapse	Synapse Corp.
Synertek	Synertek
Sys Innov	Systems Innovations
Tau Zero	Tau Zero Inc.
Tektronix	Tektronix
Telaris	(See Laserdyne)
Teledyne C	Teledyne Crystalonics
Teledyne P	Teledyne Philbrick
Teledyne S	Teledyne Semiconductor
Telefunken	Telefunken
Telephonics	Telephonics LSI
Telmos	Telmos
Teltone	Teltone Corporation
TI	Texas Instruments
Thomson-CSF	Thompson-CSF Components Corp.
TMX	TMX
Topanga	Topanga Data Systems
Toshiba	Toshiba America
Trans-Data	Trans-Data
TRW	TRW-LSI Products
Unitrode	Unitrode
Universal	Universal Semiconductor, Inc.
Vantage	Vantage Data Products
VTI	VLSI Technology, Inc.
Votrax	Votrax
Weitek	Weitek Corporation
Western	Western Digital
Wintek	Wintek Corp.
Xicor	Xicor, Inc.
Xycom	Xycom
Zendex	Zendex Corp.
Zilog	Zilog
Zymos	Zymos Corporation

Logic Array Products

Texas Instruments provides several distinct families of VLSI Logic Arrays. Master bars are processed using low-power Schottky TTL Logic (LPSTTL) with double-level-metal (DLM) routing interconnect, high performance Schottky-Transistor-Logic (STL) with triple-level metal (TLM) interconnect and low power, reverse silicon CMOS with DLM interconnect. These arrays are mask configured to satisfy unique logic requirements, allowing effiecient implementation of custom IC functions, SSI/MSI logic replacement, and in many cases complete board replacement.

The Low-Power Schottky TTL (LPSTTL) master arrays employ a cellular organization of NAND gates. Array interiors consist of low-power Schottky TTL gates with LPSTTL input/output buffers surrounding the periphery. Schottky-Transistor-Logic (STL) master arrays likewise employ a cellular orgainization of interior gates. Each interior gate performs the INVERT function and is processed using high-performance STL technology. Input/output buffers on the TAT004/TAT008 are compatable with low-power Schottky TTL while the TAT010/TAT020 buffers are compatible with either low-power Schottky TTL or high-speed ECL logic. THe CMOS master arrays employ an interior organization of basic NAND/NOR functional cells arranged into column structures. This array interior interfaces directly to low-power Schottky TTL logic via the periphery buffer organization.

All Texas Instruments Master Arrays employ vertical and horizontal routing channels dedicated to signal interconnect. The LPSTTL arrays require manual interconnect routing, with predesigned/prerouted buffer logic functions referenced for ease of interconnect. All STL and CMOS arrays are supported by a fully integrated software design utility, assisting the user in specifying his logic design and test pattern set. This offers the capability for verification and analysis of the design prior to automated mask patterning of the specific logic function. This automated layout system is typically able to achieve an 80% utilization of internal logic gates.

TIs advanced design automation system dramatically reduces engineering costs and turnaround time in the design of complex LSI/VLSI curcuitry. The totally integrated nature of the design data base allows a completely automated design technique for high-density logic arrays - from simulation and verification through layout and routing.

To access this system, you need only describe the functionality of your circuit and its test conditions using TIs computer readable design languages: Hardware Description Language (HDL) and Test Description Language (TDL).

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Logic Array Products (Continued)

HDL is a hierarchical block-structured design language which allows the user to describe logic circuitry in multiple levels of detail. Essentially, user-created logic blocks are interconnected with TIs predesigned software functions in order to define the structure and functionality of the overall design. The user blocks and software functions are defined via HDL; interconnecting them is achieved by referencing logic subroutines and assigning I/O signal variables. These logic blocks are interconnected to build larger sections of circuitry until the entire function is defined. Signal cirticality may be assigned at each level of interconnect as a forward-looking aid to routing. Actual package pin locations are assigned at the final "design block" level.

TDL is used to define inputs and outputs for simulating the total logic function. I/Os are defined as TDL vectors, specifying both input logic levels for circuit simulation and expected output levels for verification with simulated results.

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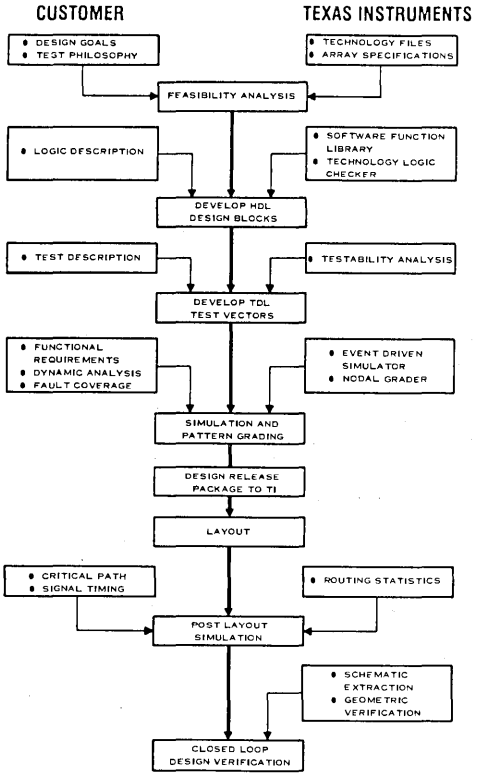
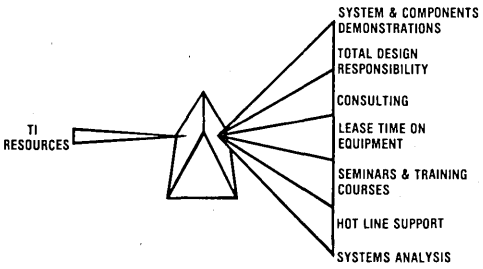
Logic Array Products
Design Support



Designing logic arrays requires two parties: Texas Instruments and you. TI provides design automation facilities staffed by experts and you provide the requirements of your logic design. To make this process more convenient, TI is enlarging its computer and engineering support resources. Assistance is available at either TIs Houston logic array facility or at Regional Technology Centers (RTCs) located in Boston, Chicago, Los Angeles, Santa Clara, Dallas and Atlanta. Design automation software may be accessed through these facilities or via dial-up communications links tied directly to TIs computing network in Dallas.

This network provides closed-loop customer support throughout the entire logic array design cycle: From initial training and documentation; through actual design, analysis and consulting services; to computer interfacing for communications and remote entry of batch jobs. TI concentrates resources in areas of greatest customer need to assure cost-effective support and effective communications.

REGIONAL TECHNOLOGY CENTER'S FULL SPECTRUM OF SUPPORT



Texas Instruments technology centers are staffed with experienced systems analysts and design engineers who examine your circuit applications and determine design feasibility for TI Logic Arrays. They compare specific logic design requirements with the capabilities of the various array products in order to determine which master array best satisfies your design. Next, I/O requirements are considered in order to specify packaging needs. Special requirements and design advice may then be discussed in order to reduce potential test or environmental difficulties.

The results of these analyses are product/package recommendations which capitalize on the technical capabilities of TIs Logic Array families to provide the most cost-effective solution to your design requirements. This service is extended at no charge for logic array applications. Full system feasibility analysis is also available whenever full system partitioning will be the initial procedure.

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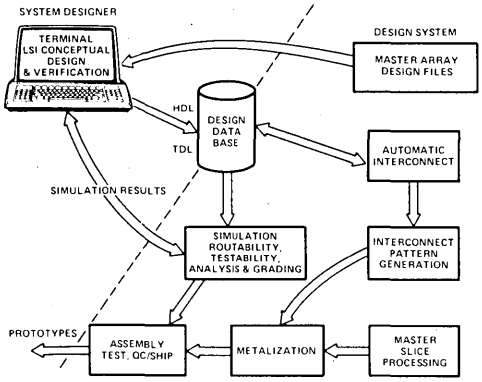
Logic Array Products
Design Support

AUTOMATED ARRAY DESIGN SYSTEM



TIs automated design system is driven by two standardized design lasnguages: Hardware Description Language (HDL) and Test Description Language (TDL). These languages are used hierarchically to define complex logic functions in a generalized format for compilation into a computer-readable database. The data is then accessed by TIs automated design software for simulation, analysis, autorouting, and array fabrication.

This procedure leads to the quickest, most reliable and most cost-effective method for designing LSI circuits. To acquaint you with these new design techniques, a complete line of user documentation and training seminars is provided by Texas Instruments. The documentation consists of a detailed Logic Array Designers Manual, data sheets of logic array characteristics, information packets on library-accessible predesigned software functions, and related technology notes. This information may be purchased separately for individual user study. However, the preferred training process is through attendance at the specially coordinated technology classes offerd at any of the various technology centers. Presently, two level of structured class study are offered, with advanced instruction available informally to experienced users.

TRAINING SCHOOL

OBJECTIVES

TO PROVIDE CUSTOMER TRAINING ON DESIGN PROCEDURES - SUFFICIENT DETAIL IS GIVEN TO ALLOW CUSTOMERS TO PROCEED WITH THEIR OWN DESIGNS

- COURSE IS VERY PRACTICALLY ORIENTATED (HANDS ON EXPERIENCE)

COURSE CONTENT

DAY 1	DAY 2	DAY 3	DAY 4	DAY 5
Introduction & Overview Wired And Logic Network	STL/ASTL Design Rules JCL	Introduction to TDL, CSL SIMCL	Introduction to Load Checker Testability Analyzer Workshop Run Load Checker Testability Analyzer	Workshop Packaging & Thermal Considerations
Introduction to HDL	Workshop Run HDL	Workshop Run TDL	Introduction to Test Pattern Grading Workshop Run Grader	Tour Automated Layout Processing Facilities

- N.B. DETAILED CONTENT & COURSE NOTES AVAILABLE 4081

This class structuring offers a concise one-day introductory seminar aimed toward technical managerial-level personnel. The focus is on the cost-effective benefits of designing with Texas Instruments design automated logic arrays. Business issues, present and future technological comparisons, and an analysis of the pre-engagement decision process conclude this general overview.

A more detailed design-level instruction is offered during the second, five-day session. This course familiarizes engineering personnel with the techniques and capabilities of TIs design languages and automated software system. Actual workshop experience is stressed throughout. Further, advanced instruction on behavioral design analysis, use of transportable software routines and advanced simulation/timing techniques are also offered on an individual basis for the experienced designer interested in accessing these capabilities.

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Logic Array Products
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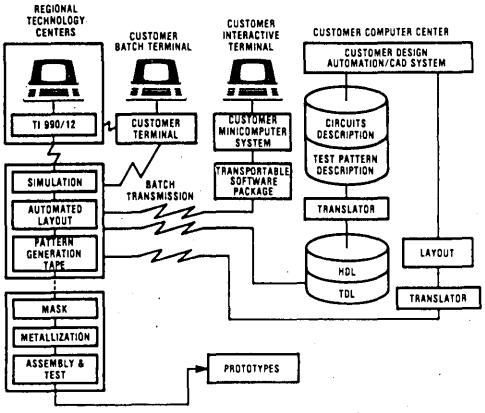
CUSTOMER-DESIGN AUTOMATION INTERFACE OPTIONS



After the circuit description and test vector condtions are coded, access to simulation and analysis software is required to exercise your design. Texas Instruments has developed an in-house, closed-loop design system consisting of routines for logic description and compilation, logic simulation, testability analysis, interconnect rule checking, and test vector grading. Depending on the extent of your design automation capabilities, access to some or all of these routines may be required. TI offers a variety of accesses into its centralized computer network.

The simplest interface is through private terminal access available at Houston and each local RTC. Terminals may be reserved by advanced notification. This allows edit, store and print fuctions on the local hardware, while maintaining remote job entry into TIs central design automation facility for batch access to the design automation simulation and analysis routines.

COMPATIBILITY REQUIREMENTS FOR DIRECT DIAL-UP INTERFACE TO TILADS AUTOMATION SOFTWARE

REQUIREMENT	RESPONSIBILITY
• MODEM INTERFACE PORT	REQUIREMENT OF CUSTOMER SYSTEM
• DEDICATED PHONE LINE FOR MODEM/D.A.A.	CUSTOMER/TI
• MODEM:	CUSTOMER/TI – MODEM SUPPLIER
– BELL TYPE 201C (2400 BAUD)	
– BELL TYPE 208B (4800 BAUD)	
• COMMUNICATION PROTOCOL:	CUSTOMER SYSTEM RESIDENT EMULATOR
– IBM 3780	

EXCEPTIONS: THE ABOVE OUTLINE REPRESENTS A MINIMUM COST APPROACH TO D.A. – CUSTOMER COMPUTER INTERFACE. OTHER MODEM/PROTOCOL SELECTIONS ARE ACCEPTED. HOWEVER, SPECIAL HARDWARE/SOFTWARE/CONSULTING REQUIREMENT MAY ADD TO THE CUSTOMER COST.

Customers with sufficient in-house computing hardware may access the TI design automation system via a variety of dial-up links. This dial-up capability requires your system to support local edit, storage, and print functions in order to format the HDL/TDL data and print processing results. Communication to TI facilities for processing is done by emulating IBM 3780 data communications to transmit bits over dial-up telephone lines. MODEMs are used for modulation/demodulation of transmitted signals, and either 2400 or 4800 bit-per-second line speeds are supported, depending on requested data transaction rate. This procedure is generally followed in order to minimize your charges. Systems analysts located at the RTC will assist in the determination of the most appropriate communications link.

Communication ports are available for transmission access at either central or regional facilities. Customer charges are figured according to total computer and telephone line usage.

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Logic Array Products
Design Support

TRANSPORTABLE DESIGN UTILITY

- PURPOSE: TO PROVIDE A TRANSPORTABLE LOGIC ARRAY DEVELOPMENT SYSTEM FOR COMPILATION ON CUSTOMER IN-HOUSE COMPUTING FACILITIES.
- CAPABILITIES:
  - INITIAL RELEASE
    - HDL, TDL COMPILER/SYNTAX CHECKER
    - INTERCONNECT (TECHNOLOGY) CHECKER
    - TESTABILITY ANALYZER
    - INTEGRATED, EVENT-DRIVEN SIMULATOR
  - FUTURE RELEASES
    - TEST PATTERN GRADER W/RANDOM FAULT SIMULATION CAPABILITY
    - ROUTABILITY ANALYZER
    - PREDEFINED SOFTWARE FUNCTION LIBRARIES WITH SORT/MERGE/MINIMIZATION ROUTINES
- INITIAL TARGET MACHINES:
  - DEC 11/780 WITH VMS OPERATING SYSTEM
  - IBM 4341 OR LARGER MAINFRAME WITH IBM OS OPERATING SYSTEM
- TARGET MACHINE REQUIREMENTS:
  - 32 BIT ADDRESSING STRUCTURE
  - PASCAL COMPILER (WIRTH STANDARD PASCAL)
  - 512 K BYTES USER PARTITIONED MAIN MEMORY
  - 50 M BYTE DIRECT ACCESS DISK

Customers with in-house minicomputer/mainframe facilities will be able to install a Transportable Design Utility (TDU) package for in-house circuit design analysis. The TDU includes the HDL compiler/syntax checker, TDL compiler, an interconnect rule checker, a design testability analyzer, and an event-driven logic simulator. Later, the TDU will include a routability analyzer and test pattern grader as transportable utilities.

The TDU is written in Pascal. Initially, object code will be available for installation on VAX 11/780 computers with the DEC VMS Operating System and the IBM 4341 or larger mainframes. TDU versions are also planned for other 32-bit computers with Pascal compilers and adequate system resources: Typically 512K bytes of main memory for user tasks, 50M byte direct access disks, and sufficient user resident support to aid in integrating the design routines into the new operating environment.

Regardless of environment, the TDU allows you to utilize all or part of the design automation software on an in-house development system. Result: Cost-effective use of both yuur hardware and the TI software.

Customers with adequate design automation software systems may design and test their logic circuitry using their in-house resources and then translate the resulting databases to HDL/TDL format for transmission to a TI support facility. Texas Instruments personnel are available to work with you to validate the translation stage of this process. Once check-out is performed, HDL/TDL databases may be transfered directly to TIs automated layout and routing facilities. The database transfer may be accomplished via either direct dial-up telephone communications or 9-track 800/1600 BPI magnetic tapes. This final interface technique minimizes your expenditures by maximizing use of you in-house resources in the design and analysis prior to the logic placement and routing analysis performed by Texas Instruments.

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TEXAS INSTRUMENTS
Logic Array Products
Design Support

The software function library (SFL) is a collectin of software files that describe logic functions most commonly used by logic designers. The most frequenty used TTL SSI/MSI functions were selected and have been implemented by Texas Instruments in Schottky-Transistor-Logic (STL). TI provides this library as a convenient starting point for designing logic arrays.

* Provides standard and frequently used functions for the design engineers convenience.
* Aids the user to understand Harware Description Language and coding techniques.
* Reduces design effort to develop its own files and eliminates the need to document for general usage.
* Accelerates translation and verification of an existing SSI/MSI system into logic array(s).
* Reduces turn-around time for logic array prototype implementation.

For more information on TIs Logic Array family, please contact the RTC in your region or call the Houston Logic Array Department. A list of contacts is provided below.

ATLANTA REGIONAL TECHNOLOGY CENTER	404/452-4686
BOSTON REGIONAL TECHNOLOGY CENTER	617/890-4271
CHICAGO REGIONAL TECHNOLOGY CENTER	312/228-6008
DALLAS REGIONAL TECHNOLOGY CENTER	214/680-5096
N. CALIFORNIA REGIONAL TECHNOLOGY CENTER	408/980-0305
S. CALIFORNIA REGIONAL TECHNOLOGY CENTER	714/641-2064
HOUSTON LOGIC ARRAY DEPARTMENT	713/490-4051

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TEXAS INSTRUMENTS
Logic Array Products
Logic Array Master Bars

DEVICE NUMBER	GATE TECHNOLOGY	MINIMUM PROCESSING GEOMETRY (MICRONS)	INTER-CONNECT	AUTOROUTIBLE GATE COUNT	INTERNAL GATE PROPAGATION DELAY(TYP)	INTERNAL GATE POWER DISSAPATION (TYP)	TOTAL ARRAY STATIC POWER DISSAPATION	NO SIGNAL PADS
TAL002	JUNCTION ISOLATED LPSTTL	4.5	DOUBLE LEVEL METAL (DLM)	200	5.0ns	1.25mW		28
TAL004	JUNCTION ISOLATED LPSTTL	4.5	DOUBLE LEVEL METAL (DLM)	400	5.0ns	1.25mW	900mW	42
TAT004	JUNCTION ISOLATED STL	4.5	TRIPLE LEVEL METAL (TLM)	400*	2.5ns	600 µW	1.4W	76
TAT008	JUNCTION ISOLATED STL	4.5	TLM	800*	2.5ns	600 µW	2.0W	104
TAT010 *NOTE 6	OXIDE ISOLATED STL	2.0	TLM	1000*	1.0ns	300 µW	1.0W	88
TAT020	OXIDE ISOLATED STL	2.0	TLM	2000*	1.0ns	300 µW	1.5W	120
TAC010 *NOTE 6	REVERSE SILICON CMOS	3.6	DLM	1000*	6.0ns	150 µW AT 5 MHZ	10 µW	64

*FULLY AUTOROUTABLE

DEVICE NUMBER	INPUT BUFFERS (MAX)	OUTPUT BUFFERS (MAX)	OPERATING FREE AIR TEMPERATURE RANGE	POWER SUPPLY ±10% (VOLTS)	I/O BUFFER COMPATIBILITY	MAX TOGGLE FREQUENCY (D FLIP-FLOP)	BASIC GATE LOGIC FUNCTION
TAL002	30	30	0° C – 70° C	+5	LSTTL	25 MHZ	4-INPUT NAND GATES
TAL004	42	42	0° C – 70° C	+5	LSTTL	25MHZ	4-INPUT NAND GATES
TAT004	76	38	0° C – 70° C	+5,+2	LSTTL	80MHZ	WIRE-AND INVERTER
TAT008	104	52	0° C – 70° C	+5,+2	LSTTL	80MHZ	WIRE-AND INVERTER
TAT010	88	*NOTE 1 44(STD LS) 19(BUFFER)	*NOTE 3 0° C – 70° C –55° C – 125° C	*NOTE 5 +5,+2 +3 +2 +5,+2,–5.2	*NOTE 5 LSTTL LSTTL ECL LSTTL,ECL	160MHZ	WIRE-AND INVERTER
TAT020	120	*NOTE 2 60(STD LS) 36(BUFFER)	*NOTE 3 0° C – 70° C –55° C – 125° C	*NOTE 5 +5,+2 +3 +2 +5,+2,–5.2	*NOTE 5 LSTTL LSTTL ECL LSTTL,ECL	160MHZ	WIRE-AND INVERTER
TAC010	64	64	*NOTE 4 0° C – 70° C	+5	CMOS LSTTL	25MHZ	2-INPUT NAND

FOOTNOTES

*1 THE TAT010 DEVICE HAS STANDARD/BUFFER OUTPUT BUFFER CAPABILITY. 44 OUTPUT BUFFER PADS ARE AVAILABLE, ALL OF WHICH ARE STANDARD LOW-POWER SCHOTTKY COMPATABLE. OPTIONALLY, UP TO 19 PREPOSITIONED OUTPUTS MAY OPERATE AS HIGH-POWER BUFFERS DRIVING HIGH CAPACITIVE LOADS.

*2 SIMILAR TO *1. DIFFERENCE IS TAT020 HAS 60 AVAILABLE OUTPUTS. ALL 60 OPERATE IN STANDARD LOW-POWER SCHOTTKY MODE. UP TO 36 PREPOSITIONED OUTPUTS MAY OPERATE IN BUFFER MODE FOR HIGH CAPACITIVE LOADS.

*3 TAT010, TAT020 WILL BE QUALIFIED OVER TWO SEPARATE FREE-AIR OPERATING TEMPERATURE RANGES.

*4 TAC010 FREE-AIR OPERATING TEMPERATURE RANGE UNQUALIFIED AT PUBLICATION TIME. QUALIFICATION WILL EXTEND BEYOND STANDARD COMMERCIAL RANGE.

*5 TAT010, TAT020, OPERATE FROM SEVERAL POWER OPTIONS TO PROVIDE A VARIETY OF BUFFER INTERFACE CAPABILITIES.

- STANDARD +5V, +2V, GND CONFIGURATION OPERATES INTERNAL STL BETWEEN +2 AND GND; +5V PROVIDES LSTTL BUFFER INTERFACE.
- +3V WITH GND OPERATES STL ARRAY INTERIOR AND PERIPHERY BUFFERS PROVIDING LOW-LEVEL LSTTL INTERFACE.
- –2V WITH GND OPERATES STL ARRAY INTERIOR AND PROVIDES 10K ECL BUFFER INTERFACE.
- +5V, +2V, GND, –5.2V OPERATES STL ARRAY INTERIOR BETWEEN +2V AND GND, +5V PROVIDES LSTTL BUFFER CAPABILITY. –5.2V ALLOWS OPTIONAL 10K ECL TRANSLATOR BUFFER SELECTION.

*6 PLANNED NEW PRODUCTS.

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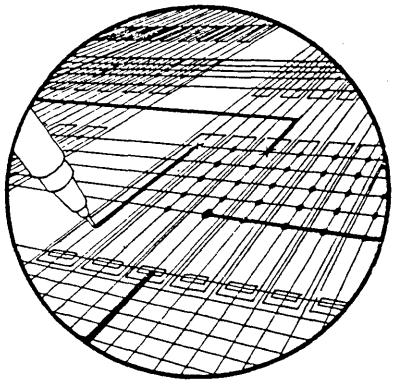


FAMILY

Two Arrays	Internal Gates	I.O. Buffers
TAL-004	500	42
TAL-002	320	28

TECHNOLOGY

Established Double Level Metal Low Power Schottky.

LAYOUT

Designed for the user at his own location.

INTERNAL GATES

-Single 5V Power Supply.
-5nS Maximum Gate Delay at 1.25mW Gate Dissipation.
-Toggle Rate 25Mhz.
-Nineteen Standard Macros currently available.

I.O. BUFFERS

Current List
-Standard True & Complement Input.
-Nand Output.
-Tristate Output.
-Standard I.O.
-Open Collector Output.
-Schmitt Trigger Input.

DESIGN VERIFICATION

-Closed Loop Logic to layout check.
-Test Pattern & Design Rule Check.
-Logic,Timing & Fault Simulation.
-Easy access by user to TI software.

DESCRIPTION

The TAL family of devices are Low Power Schottky master slices which are held in stock at TI. The master slices are converted into LSI slices by the deposition of two layers of metal according to an interconnection pattern drawn by the user on a TI supplied translucent grid. The resulting devices are tested according to input-output logic patterns devised by the user, and become the user's proprietary LSI parts.

A comprehensive design manual sets out the logic and layout rules for the process and also explains a simple shorthand method of describing the circuit so that a detailed check of layout and test patterns can be carried out at TI. This computer aided check comprehends logic,layout and test patterns and results in a dialogue in which the user and TI work together to eliminate errors prior to mask fabrication.

DESCRIPTION(continued). The layout task is considerably eased by the availability of standard overlays for commonly used logic functions and standard buffers are provided for inputs and outputs. The user is also able to specify his own blocks of logic in cases where a number of identical pieces of circuit occur in the design.

As can be seen from Fig 1, the array consists of blocks of five input Nand gates of which any four are useable in any one cell. The gates consist of output transistor T1 and multi-emitter transistor T2. The emitter of T1 is normally connected to ground and it's collector can feed up to eight subsequent multi-emitter inputs within the array. The logic design rules for the interconnection of gates are explained in detail in the design manual.

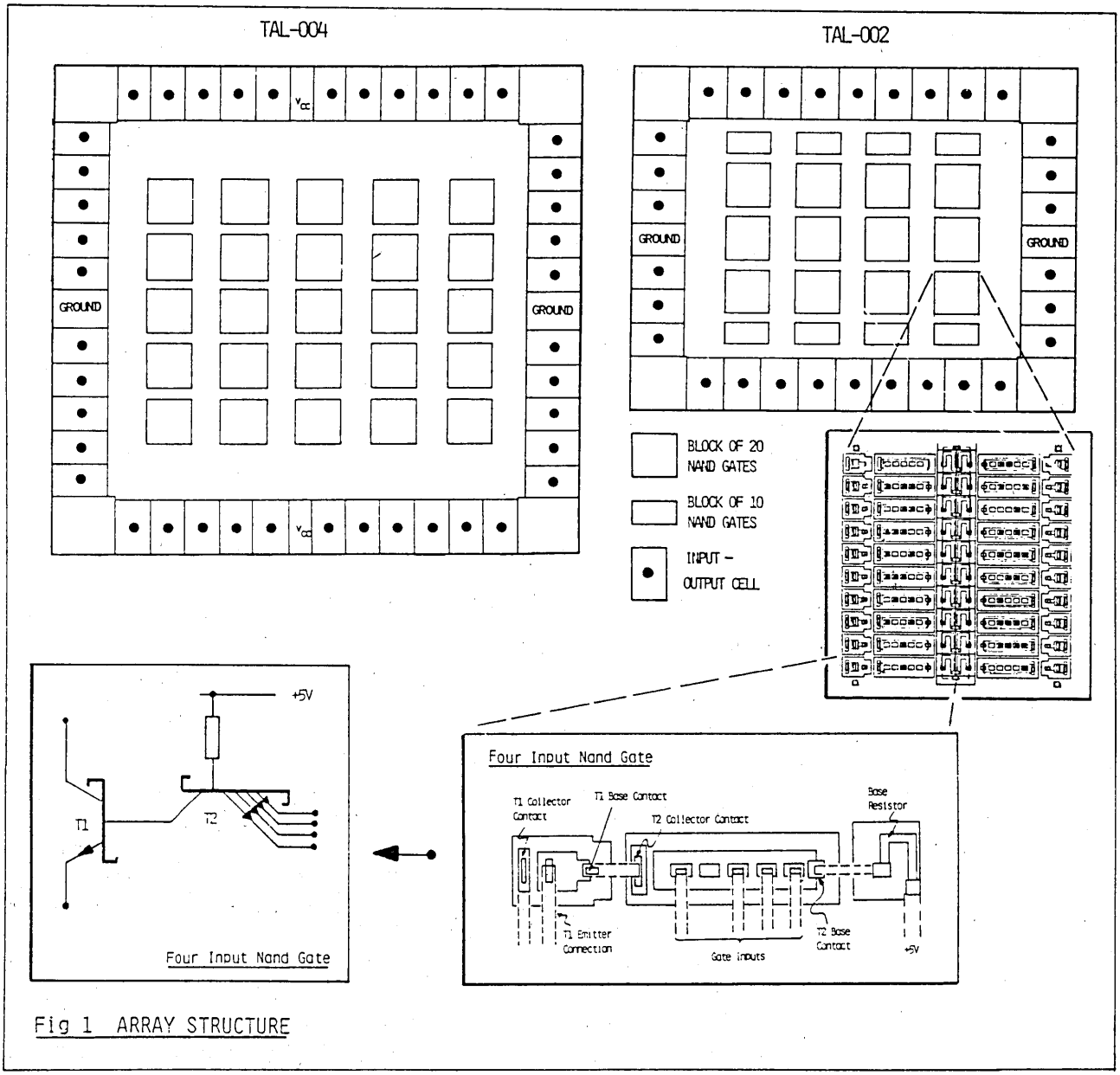


Fig 1 ARRAY STRUCTURE

DESCRIPTION(continued)

The TAL-004 has 500 internal four input Nand gates and the TAL-002 has 320. A single 5V power supply is needed for the arrays and both device types are available in 28 and 40 pin DIL plastic packages, with the option also, of a 20 pin package for the TAL-002.

MANUAL LAYOUT

A reproduction of the translucent user layout grid is shown in Fig 2. The lower level of metal interconnect on the finished device is called Metal 1 and is specified on the grid by marking the vertical lines and the upper level, Metal 2, is similarly designated by marking the horizontal lines. Electrical connection between the two layers is made by so called 'vias' and to underlying gates by 'contacts'. Layout design rules govern the location of interconnections, vias and contacts and these are clearly explained in the design manual.

Standard logic functions and I.O buffers are specified by attaching cut outs to the user grid. Symbols for the logic function overlays(macros) and I.O's are supplied on a sheet similar to the user grid.

ABSOLUTE MAXIMUM RATINGS OPERATING FREE AIR TEMPERATURE RANGE

	TAL-002	TAL-004	UNITS
Supply Voltage V_{CC}	7	7	V
Input Voltage	7	7	V
Operating Junction Temperature	150	150	^0C
Operating Free Air Temperature Range	0 to 70		^0C
Storage Temperature Range	-65 to 150		^0C

RECOMMENDED OPERATING CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High Level Output Current	I_{OH}			-400	uA
Low Level Output Current	I_{OL}			8	mA
Input Rise Time	t_I	2.4		30	nS

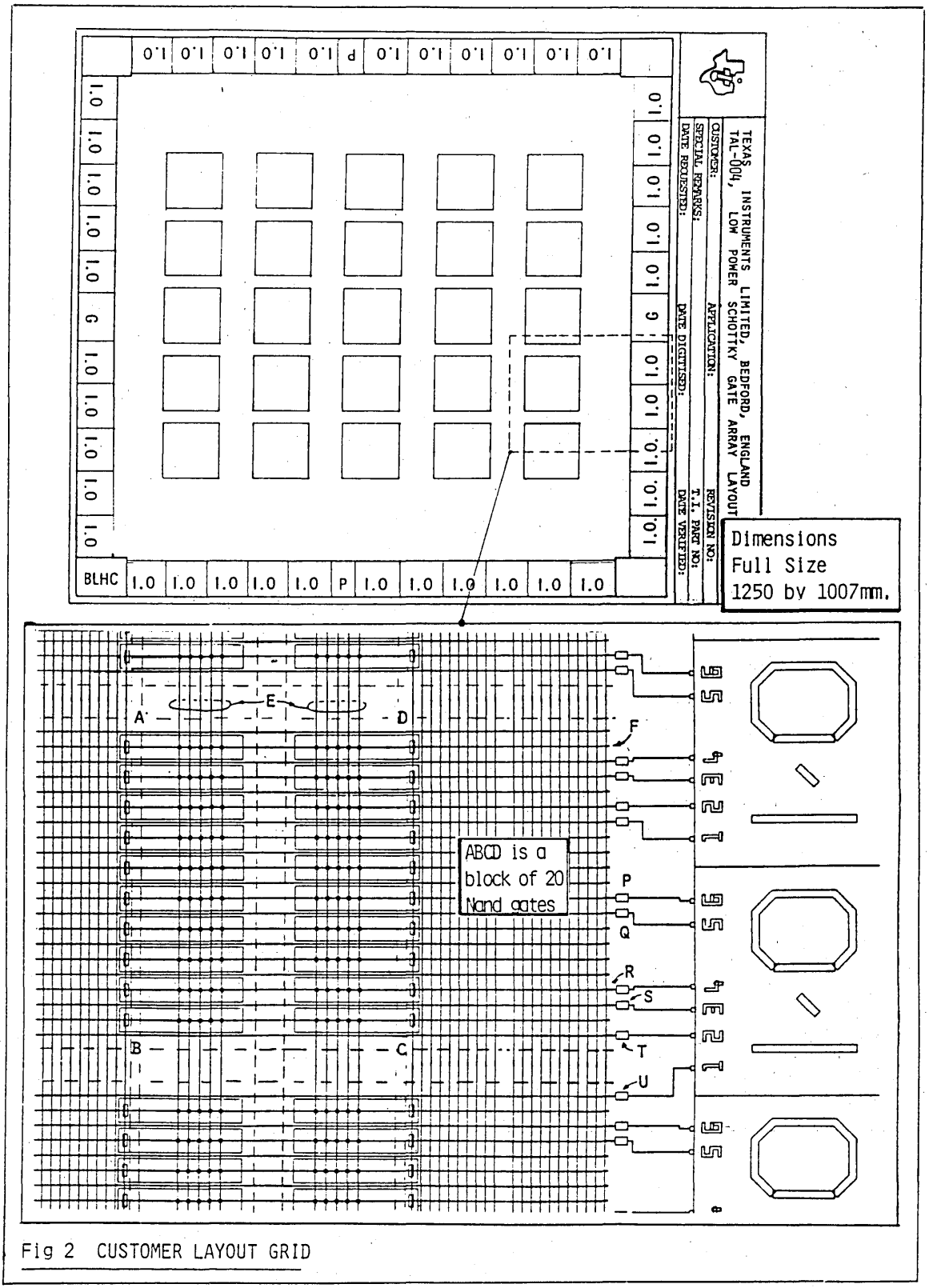
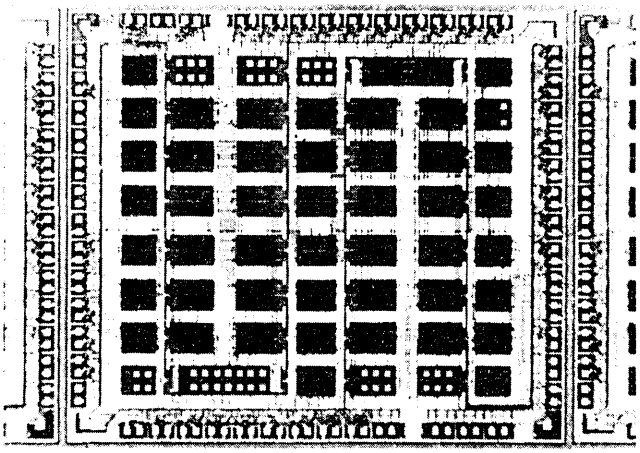


Fig 2 CUSTOMER LAYOUT GRID

TAT SERIES
STL LOGIC ARRAYS

DECEMBER 1980



- High-Performance Master Logic Arrays
  - ☐ Designed for Automated Layout
  - ☐ Mask Programmable
  - ☐ Supported by TI Software Design Utility
- Choice of Two Master Arrays

	Internal Gates	I/O Buffers
TAT008	1008	104
TAT004	540	76

- High-Performance Schottky-Transistor-Logic (STL) Design
  - ☐ 2.5 ns Typical Gate Propagation Delay at 600 μW
  - ☐ 80-MHz Toggle Rate
- Low-Power Schottky TTL Compatible Input and Output Buffers
  - ☐ Inverting and Non-Inverting Inputs Offered
  - ☐ Choice of 3-State Totem Pole and Open-Collector outputs

description

The TAT series is a family of high-performance VLSI arrays, using Schottky-transistor-logic (STL) technology. The arrays can be mask configured to unique logic requirements, allowing efficient implementation of custom IC functions, SSI/MSI logic replacement, and in many cases, complete board replacement.

The master array employs cellular organization, with channels dedicated to intercellular connections. The array interior employs high-performance STL gates with low-power Schottky-TTL-compatible inputs and outputs.

All Texas Instruments logic arrays are supported by a totally integrated software design utility, allowing the user to specify his logic design and test pattern set. This offers the capability of verification and analysis of the design prior to automated mask patterning of the specific logic function. The automated layout system is typically able to achieve an 80% utilization of the internal gates.

The TAT family is available in plastic and ceramic dual-in-line packages and ceramic chip carriers. The devices are specified for operation over the 0°C to 70°C temperature range.

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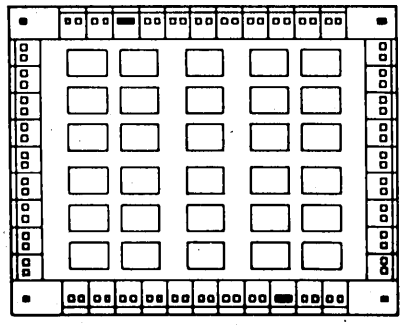
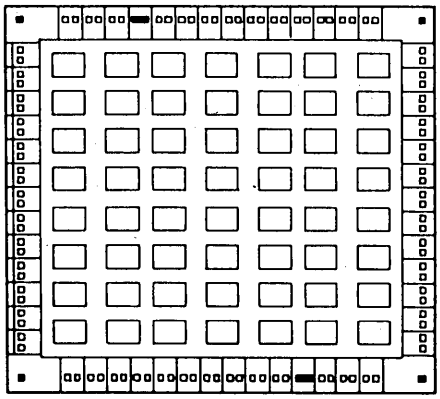
TAT SERIES
STL LOGIC ARRAYS

array organization



TAT004

■ Bond pad locations reserved for supply voltages

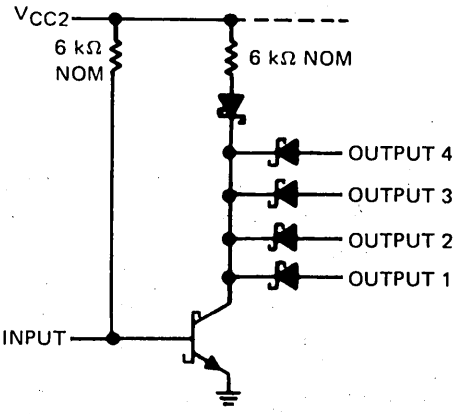


TAT008

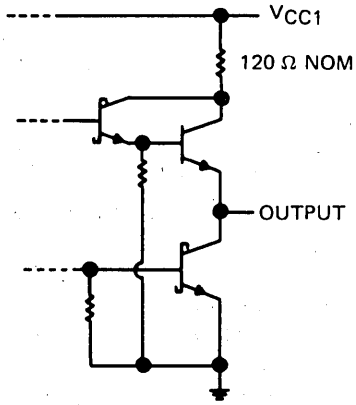
• No. of Cells	30	• No. of Gates	540	• No. of Cells	56	• No. of Gates	1008
• Cell Organization	5X6	• No. of Buffers	76	• Cell Organization	7X8	• No. of Buffers	104
• Power Pads	8	Max Inputs	76	• Power Pads	8	Max Inputs	104
		Max Outputs	38			Max Outputs	52

schematics of internal logic gates, inputs, and outputs

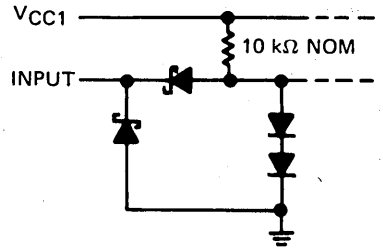
TYPICAL OF ALL INTERNAL LOGIC GATES



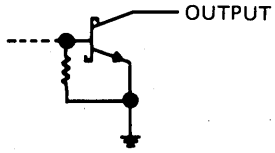
TYPICAL OF EACH 3-STATE AND TOTEM POLE OUTPUT



EQUIVALENT OF ALL INPUTS



TYPICAL OF EACH OPEN-COLLECTOR OUTPUT



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absolute maximum ratings over operating free-air temperature range

Supply voltages, V_{CC1} (see Note 1)		7 V
V_{CC2}		3 V
Input voltage		7 V
Output voltage		7 V
Power dissipation (see Figures 3 and 4):	TAT004	1.4 W
	TAT008	2.2 W
Operating free-air temperature range		0°C to 70°C
Operating junction temperature		125°C
Storage temperature range		−65°C to 150°C

NOTE 1: All voltages are with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	4.5	5	5.5	V
Supply voltage, V_{CC2}	1.8	2	2.2	V
Fan in (internal gate)			8	
Fan out (internal gate)			4	
High-level output current, I_{OH}			−400	μA
Low-level output current, I_{OL}			8	mA
Transition time at any input, t_T	2.4		30	ns
Operating free-air temperature range, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltages and operating free-air temperature

PARAMETER			TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage		I_I = −18 mA			−1.5	V
V_{OH}	High-level output voltage		I_{OH} = −400 μA	2.7	3.4		V
V_{OL}	Low-level output voltage		I_{OL} = 8 mA			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied		V_O = 2.4 V			20	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_O = 0.4 V			−20	μA
I_I	Input current at maximum input voltage		V_I = 7 V			0.1	mA
I_{IH}	High-level input current		V_I = 2.7 V			20	μA
I_{IL}	Low-level input current		V_I = 0.4 V			0.8	mA
I_{OS}	Short-circuit output current§			−30		−100	mA
I_{CC1}	Supply current from V_{CC1} (per buffer)	Input	V_I = 2.7 V		1.0	1.5	mA
		Output	V_O = 0.4 V		2.0	3	mA
I_{CC2}	Average internal gate supply current from V_{CC2} (per gate)		50% duty cycle		0.3	0.5	mA

‡ All typical values are at T_A = 25°C, V_{CC1} = 5 V, V_{CC2} = 2 V.

§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

switching characteristics of internal gate

	PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
t_{pd}	Propagation delay time per gate	Fan-in = 1, Fan out = 1	1.5	2.5	3.5	ns
	Increased propagation delay time for each additional input		0.1	0.2	0.3	ns
	Additional propagation delay time for each 10 mils of metalized interconnect pattern		0.08	0.15	0.2	ns

switching characteristics of input buffer

	PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Fan-out = 1	1	2	4	ns
t_{PHL}	Propagation delay time, high-to-low-level output		2	3.5	6	ns

switching characteristics of output buffer

	PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 2 kΩ, See Figure 5	4	7	11	ns
t_{PHL}	Propagation delay time, high-to-low-level output		6	12	19	ns
t_{PHZ}	Disable time from high level	C_L = 15 pF, R_L = 2 kΩ, See Figure 5	8	14	20	ns
t_{PLZ}	Disable time from low level		6	10	15	ns
t_{PZH}	Enable time to high level		4	8	12	ns
t_{PZL}	Enable time to low level		5	10	16	ns

‡ All typical values are at T_A = 25°C, V_{CC1} = 5 V, V_{CC2} = 2 V.

TYPICAL CHARACTERISTICS

AVERAGE PROPAGATION DELAY TIME OF INTERNAL GATES vs V_{CC2} SUPPLY VOLTAGE

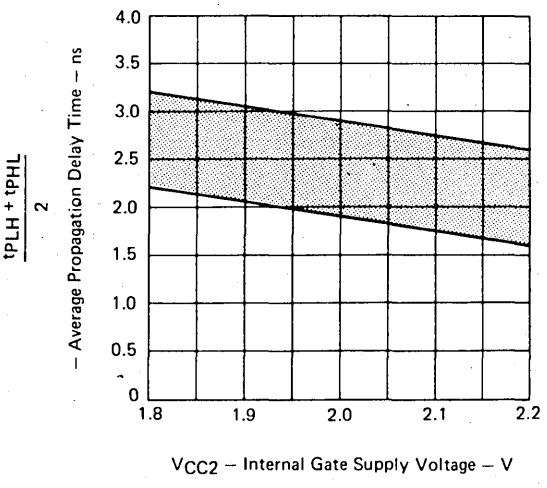


FIGURE 1

AVERAGE PROPAGATION DELAY TIME OF INTERNAL GATE vs LENGTH OF METALIZED INTERCONNECT PATTERN TO BASE

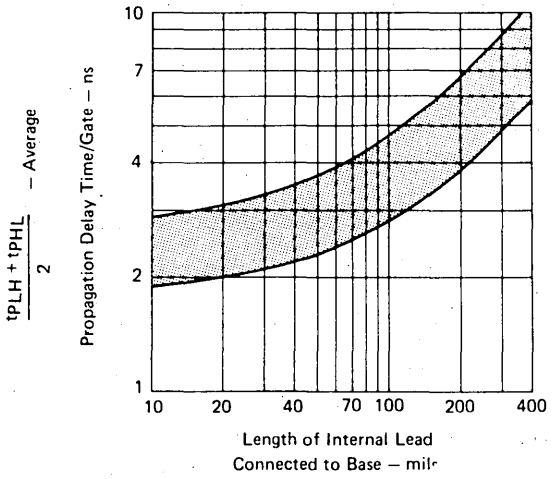


FIGURE 2

The average propagation delay times typically fall within the shaded area over the operating free-air temperature range of the device.

static power dissipation graphs

The following graphs show the maximum power dissipation for the TAT004 and TAT008. The graphs give Pmax for various combinations of gate and buffer utilization. For the given curves, it is assumed that half of the signals are inputs and half are outputs. For other combinations of inputs and outputs, the following equations may be used:

TAT004: Pmax = 0.540U + 0.016B + 0.0064I
TAT008: Pmax = 1.008U + 0.016B + 0.0064I

U is the percentage gate utilization
B is the number of output buffers
I is the number of input buffers

A bidirectional signal is counted as one input buffer and one output buffer.

TAT004
POWER DISSIPATION

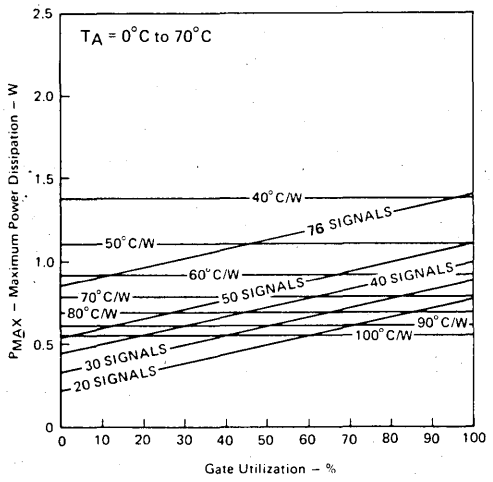


FIGURE 3

TAT008
POWER DISSIPATION

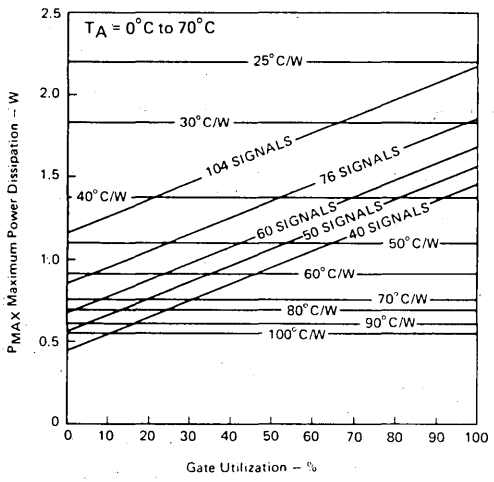
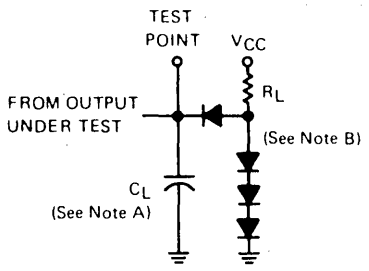


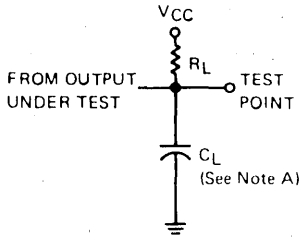
FIGURE 4

The horizontal lines indicate the maximum thermal resistance allowed from junction to ambient for a given power dissipation.

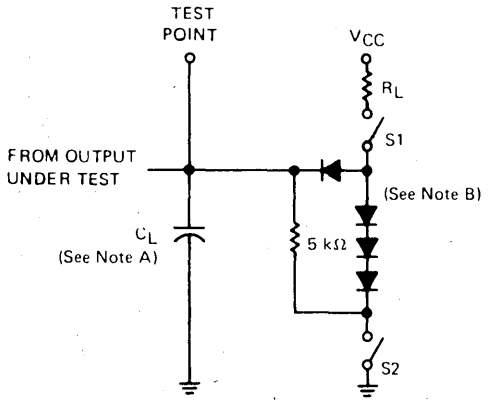
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS

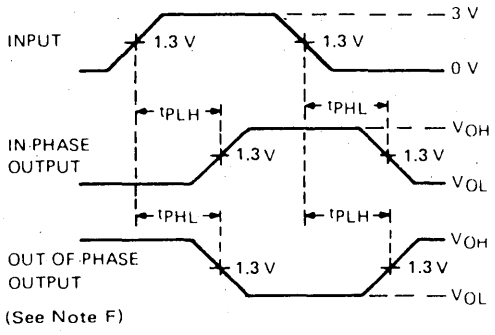


LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS

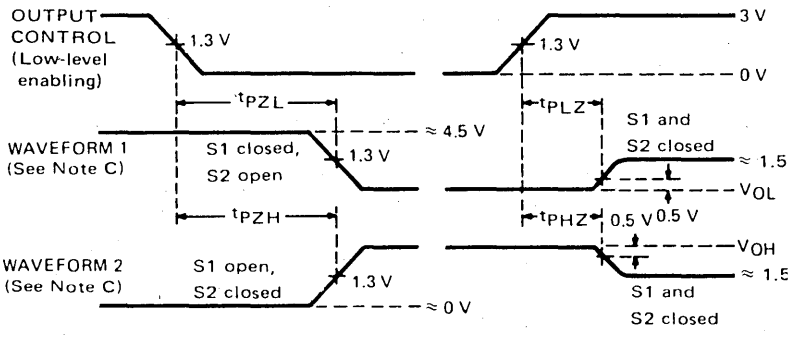


LOAD CIRCUIT FOR THREE-STATE OUTPUTS

NOTES. A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
E. All input pulses are supplied by generators having the following characteristics: $t_r \leq 15$ ns, $t_f \leq 15$ ns, PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$.
F. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

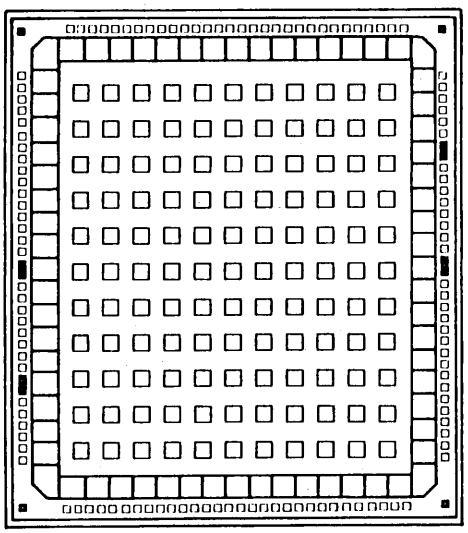
FIGURE 5

- High Performance Master Logic Arrays
  - Designed for Automated Layout
  - Mask Programmable
  - Supported by the Computer-Automated Texas Instruments Logic Array Design System (TILADS)
- Advanced Schottky Transistor Logic (ASTL) Technology
  - 1 ns Typical Gate Delay @ 300 uW
  - DC to 150 MHz Toggle Frequency
- Choice of Two Master Arrays

	Internal Gates	Typical Usable Internal Gates	I/O Buffers
TAT010	1280	1000	88
TAT020	2420	2000	120

- Flexible Interface/Power Supply Options
  - 5- and 2-Volt Supplies with Standard Low-Power Schottky TTL-Compatible I/O
  - Single 3.3-Volt Supply with Standard Low-Power Schottky TTL-Compatible I/O
  - Single 2-Volt Supply with ECL-Compatible I/o
- Choice of Operating Free-Air Temperature Range
  - Commercial: 0 C to 70 C
  - Military: -55 C to 125 C

BAR MAP



Description

The TAT010 and TAT020 are both members of a family of LSI Master Logic Arrays offered by Texas Instruments. These devices utilize Advanced Schottky Transistor Logic (ASTL) and can be mask-configured to unique logic requirements, allowing efficient implementation of custom IC functions, SSI/MSI logic replacement, and, in many cases, complete board replacement.

The TAT010 and TAT020 employ a cellular organization with 1280 and 2420 internal gates, respectively, arranged in cells containing twenty gates each. Internal gates are implemented in ASTL circuit technology, offering excellent speed/power characteristics. Internal logic cells are separated by horizontal and vertical channels where interconnections between logic cells are made and whose size is optimized to accomodate a wide range of logic requirements.

The periphery of each ASTL array is occupied by 88 and 120 I/O buffers, respectively, which are programmable to provide a wide variety of I/O functions. I/O electrical interface options include an Advanced Low-Power Schottky TTL-compatible interface, a 10,000 series ECL-compatible interface, and a low-voltage (3.3 v) interface.

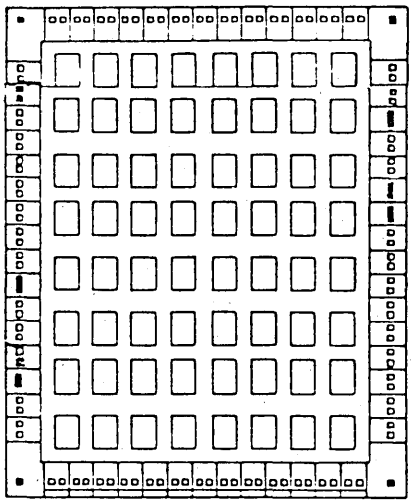
Additional information concerning a military-grade ASTL LOGIC ARRAY is available in a separate data sheet.

TEXAS INSTRUMENTS
Logic Array Products
Design Support

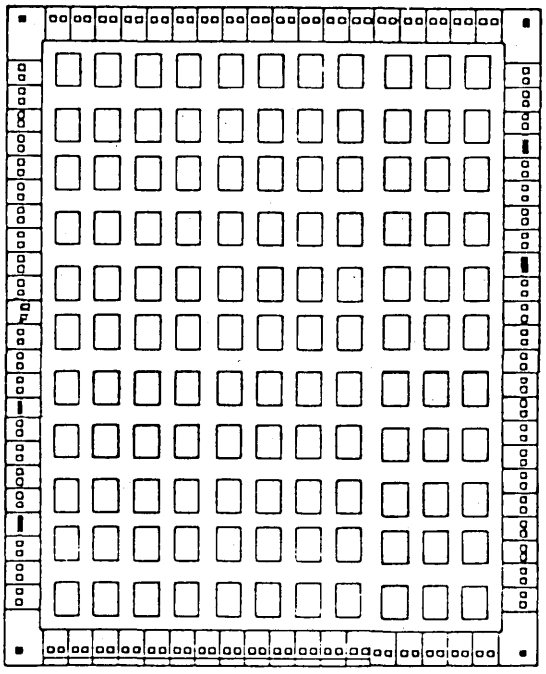
The complete family of Texas Instruments Logic Arrays is fully supported by a totally integrated software design utility (TILADS), allowing the user to specify and verify his logic design, test patterns, and parametric requirements prior to hardware fabrication. The Automated Layout Subsystem which is typically able to interconnect 80% of the internal gates with no manual routing of interconnect metalization, utilizes the logic description database also, as does the Geometric rule verificaton and the Schematic verification subsystem. Use of TILADS design and verification capabilities offers maximum probability of successful customer prototype fabrication during the initial design cycle. The ASTL Logic Array user Supplies the TLADS utility with two databases, one for logic description and one for test description, which are input to the major subsystems of TILADS which then checks parametric and functional performance test description accuracy and completeness and logic design rule compliance.

TAT010 and TAT020 are offered ,in two operating free-air temperature range versions: 0°C to 70°C for commercial applications and -55° C to 150°C for severe environments/military applications. Operating free-air temperature conditions are subject to array utilization, package selection and final end-use thermal environment.

ARRAY ORGANIZATION



TAT010



TAT020

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TEXAS INSTRUMENTS
Logic Array Products
Design Support

	TAT010	TAT020
Number of typically usable gates	1000	2000
Number of gates	1280	2420
Cell organization	8 x 8	11 x 11
Number of cells	64	121
Power pads	8*	8*
Signal pads	88*	120*
Maximum inputs	88*	120*
Maximum outputs	44	60

*The use of an ECL translator interface I/O buffer requires the use of at least one additional power pad for the -5.2 volt supply pin, which simultaneously reduces the total number of available signal pads and maximum inputs. The use of high drive output buffers (output buffers designed to handle large dynamic current loads) requires the use of an additional eight ground pins, which also reduces the total number of maximum signal pads and maximum inputs by eight.

- Standard Dual-in-Line packages
- Ceramic chip carriers for higher packaging densities
- Pin grid arrays provide excellent thermal characteristics, through-the-board 100-mil centers for standard assembly, and allow higher packaging densities than chip carriers.

	24-PIN	28-PIN	40-PIN	48-PIN	64-PIN	68-PIN	84-PIN	108-PIN	132-PIN
DUAL-IN-LINE PLASTIC(N) PACKAGES	TAT004 TAT008	TAL002 TAL004 TAT004 TAT008	TAL002 TAL004 TAT004 TAT008	–	–	–	–	–	–
DUAL-IN-LINE CERAMIC(J) PACKAGES	TAT004 TAT008	TAL002 TAL004 TAT004 TAT008	TAL002 TAL004 TAT004 TAT008	TAT004 TAT008	TAT004 TAT008				
CERAMIC CHIP CARRIERS	–	–	–	–		TAT004 TAT008	TAT004 TAT008	–	–
CERAMIC PIN GRID ARRAY							TAT010 TAT020	TAT010 TAT020	TAT010 TAT020

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VLSI DESIGN TOOLS

VLSI FOR THE SYSTEMS DESIGNER

VTI's VLSI Design System is a complete set of software tools to aid system designers in creating custom integrated circuits. It is based upon a design methodology developed to allow the designer to fully utilize the potential of VLSI The design approach is hierarchical, with successive decomposition of functions. Regular structures and minimized interconnect through cell-abutment are emphasized in order to efficiently utilize the potential of high-density MOS technology. Design rules are defined in terms of the scaling variable *lambda*. Scalable design rules provide a degree of process independence, since designs can be automatically adapted to new processes.

In support of this methodology, VTI has developed a fully-integrated computer-aided design system to manage much of the detail inherent in a VLSI design. The design system is aimed at producing designs on time and with predictable performance: *On time* because design schedules are often critical to the success of a product; *Predictability* because the ability to foretell chip behavior and performance on "first silicon" greatly affects both cost and design time. VTI's VLSI Design System gives designers a fully integrated set of IC design tools that result in short development times and high user confidence in early success.

VTI's VLSI Design System produces a layout data-base in Caltech Intermediate Form (CIF). This data-base can be transmitted directly to silicon foundries, including VTI.

VTI's VLSI Design System consists of three subsystems: *the Kernel*, which provides the basic capabilities; *Graphics Editors*, which offer improved designer productivity; and *the Window Environment*, which provides a simple, consistent, and powerful user interface.

THE KERNEL

The *Kernel* includes five tools that form an integrated VLSI design system:

- The VIP procedural design language is used to specify layouts in terms of parameterized high-level-language statements. This capability is particularly useful for cells which are repeated, either identically, or modified by parameters that alter their physical configuration or performance.
- The VSIM switch-level simulator allows designers to validate logic designs before layout begins. This tool also verifies accuracy after layout is done.
- The PLOT graphics utility provides graphic display.
- The DRC design-rule checker helps ensure that the layout adheres to design rules.
- The EXTRACT circuit extractor creates circuit models from the layout data-base for use by functional and performance simulators. Functional simulation can be used to verify the logic design. The performance of the extracted models can be analyzed in detail with circuit simulators such as SPICE.

THE GRAPHICS EDITORS

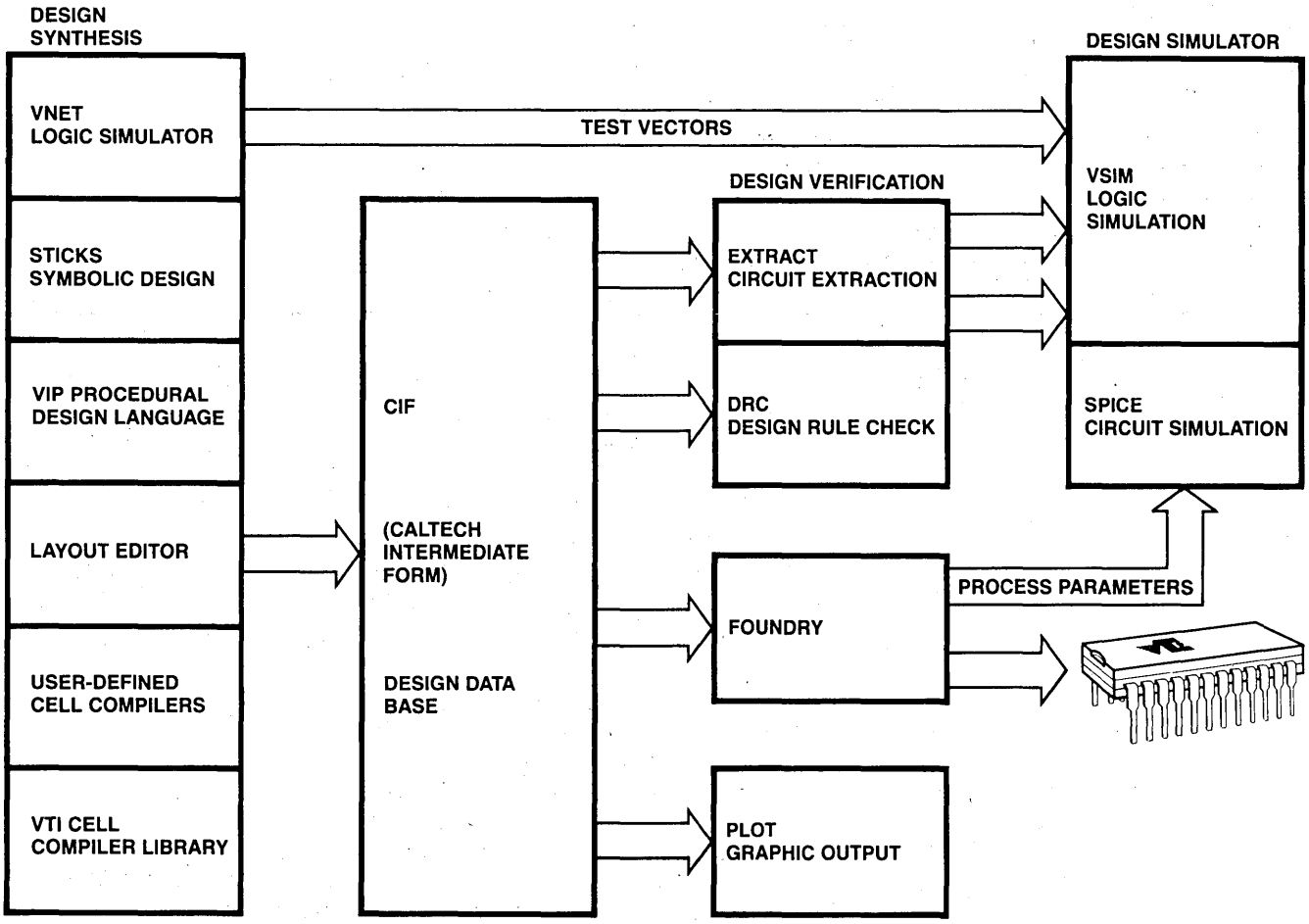
The *Graphics Editors* improve designer productivity by providing a more powerful user interface. They are specifically intended for use on leaf cells, i.e. cells of 100 transistors or less. They include a symbolic editor (STICKS) and a geometric editor (LAYOUT). With STICKS, users work with a symbolic representation of their circuit. The computer does the detailed layout automatically and compacts it to the minimal area. The geometry editor can be used to optimize the area, speed or other characteristics of critical leaf cells. These tools speed the design of cells which do not occur often enough to require the development of a parameterized description in VIP, the procedural design language. After all of the leaf cells are defined, they can be extracted, simulated and interconnected by means of *Kernel* programs.

THE WINDOW ENVIRONMENT

The *Window Environment* provides the user with a flexible interface to VTI's VLSI Design System. In this environment, designers can open an arbitrary number of display "windows". Each window occupies a user-specified portion of the display within which designers can create a memo, draw a cell, or access the Kernel, etc. Windows can be freely opened, moved, re-sized or closed, as the designer wishes. They can be placed adjacent to each other to show different design elements at the same time, or overlapped to use the display-screen area more efficiently.

A four-button cursor controller moves the display cursor so that designers can draw new elements or point to existing items displayed on the screen. Commands can be entered, and drawings made, by pressing buttons mounted on the cursor controller.

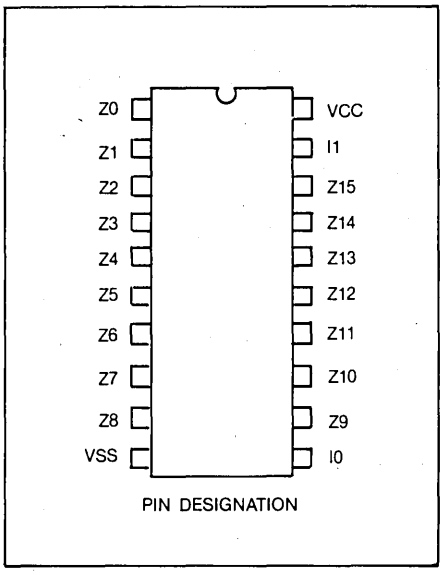
BLOCK DIAGRAM OF THE SYSTEM



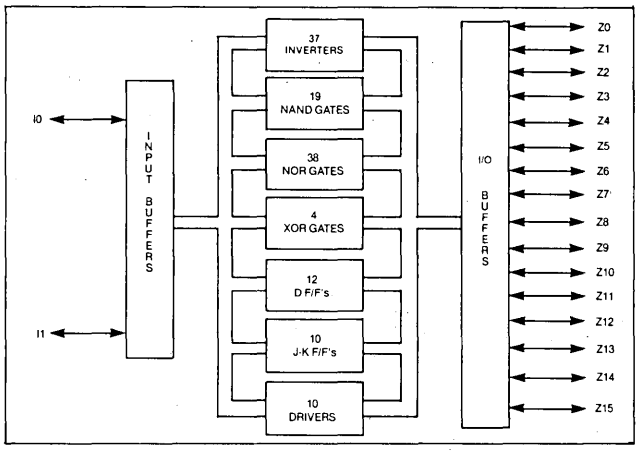
WD1820 Logic Array Device

FEATURES

- SINGLE +5V SUPPLY
- REPLACES 74LSXX LOGIC
- MASK PROGRAMMABLE
- THREE-STATE, OPEN COLLECTOR, OR TOTEM-POLE OUTPUTS
- PROGRAMMABLE PULL-UP/PULL-DOWN RESISTORS ON ALL PINS
- 130 LOGIC ELEMENTS
- 10 "LS" LOAD DRIVE CAPABILITY
- LOW POWER DISSIPATION
- QUICK TURN-AROUND
- 20 PIN DUAL-IN-LINE PACKAGE



PIN DESIGNATION



DEVICE DESCRIPTION

The WD1820 Logic Array Device contains 130 uncommitted logic elements that can be interconnected to replace a large amount of discrete S.S.I. Logic functions. Unlike a cell matrix or gate array, this mask programmable device contains prefabricated logic elements such as NAND gates, NOR gates, 'D' and 'JK' Flip/Flops, and a variety of other functions. Gates and Flip/Flops are interconnected using a special coding sheet, which is easily prepared directly from the user's schematic. This coding sheet is then digitized at the factory to produce a two-level mask. The mask is then applied to a pre-fabricated wafer, producing qualification samples typically 4 weeks after receipt of coding form.

For Bus-Oriented applications, sixteen pins of the device may be programmed for Three-State operation. These pins provide I/O capability, with standard TTL Totem-Pole or Open Collector configurations. Two pins are provided as input only pins. All pins are programmable with Pull-Up or Pull-Down resistors on-chip.

The WD1820 is implemented in N-Channel Silicon Gate Technology operating from a single 5 volt power supply. The device is available in either a plastic or ceramic 20 pin Dual-In-Line package.

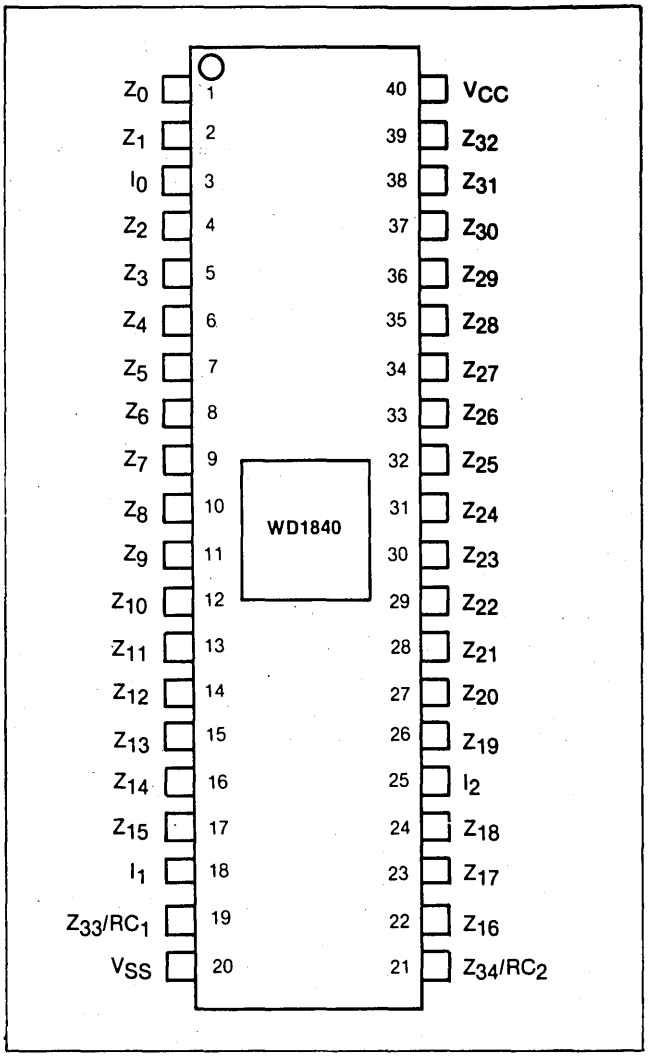
PIN	SYMBOL	NAME	DESCRIPTION
1-9 and 12-18	Z_0-Z_{15}	Three-state 0 to Three-state 15	Three-state, Totem-pole, or Open Collector I/O pins
11,19	I_0, I_1	Input 0, Input 1	Input only pins
V_{SS}	V_{SS}	GND	Ground
V_{CC}	V_{CC}	+5V	+5Volts ± 10% power supply input

ADVANCE INFORMATION

WD1840 Logic Array Device

FEATURES

- SINGLE +5V SUPPLY
- REPLACES 74LSXX LOGIC
- MASK PROGRAMMABLE
- 35 PROGRAMMABLE THREE-STATE OPEN COLLECTOR, OR TOTEM POLE OUTPUTS
- OVER 400 LOGIC ELEMENTS
- 2 ON-CHIP MULTIVIBRATORS
- ON CHIP PLA FOR STATE MACHINE IMPLEMENTATION
- TTL COMPATIBLE
- QUICK TURNAROUND
- AVAILABLE IN EITHER 40 OR 28 PIN DUAL-IN LINE PACKAGE



PIN DESIGNATION

DEVICE DESCRIPTION

The WD1840 Logic Array Device contains over 400 uncommitted logic elements that can be interconnected to replace a large amount of discrete MSI logic functions. It is an addition to the WD1820 family, offering the designer extended I/O capability and more logic elements. The device also contains dual monostable multivibrators and a general purpose PLA configured as a state machine.

Unlike a cell matrix or gate array, this mask programmable device contains prefabricated logic elements such as NAND, NOR, XOR, and Invertor gates, plus 'D' and 'JK' or 'JK̄' Flip/Flops. Gates and Flip/Flops are interconnected using a special coding sheet, which is easily prepared from the user's schematic. This coding sheet is then digitized at the factory to produce a two-level mask. The mask is then applied to a prefabricated wafer, producing qualified samples typically 6 weeks after receipt of the coding form.

The WD1840 is implemented in N-channel silicon gate technology operating from a single +5V power supply. It is available in either plastic or ceramic DIP.

TABLE 1

PIN NUMBER	SYMBOL	DESCRIPTION
1, 2, 4-17, 22-24, 26-39	Z_0-Z_{32}	Programmable I/O pins with 3-state, open collector, or push pull capability.
3, 18, 25	I_0-I_2	Input only pins.
19 and 21	Z_{33}/RC_1 Z_{34}/RC_2	Programmable I/O pins which at S_0 can function as the external RC inputs for one-shot operations.
20	V_{SS}	Ground
40	V_{CC}	+5V ± 10% power supply input.

LOGIC ELEMENTS

The WD1840 contains thirty-five input/output buffers and three input only buffers. The I/O buffers are high current inverting drivers and receivers used to interface an external pin to the internal logic elements. These 35 pins may be programmed for either three-state, totem pole, or open collector operation. When programmed for three-state operation an active high